



**ORDERING INFORMATION**

Part Number	Package	Top Marketing
MP6906GS	SOIC-8	<i>See Below</i>
MP6906GJ	TSOT23-6	<i>See Below</i>

- \* For Tape & Reel, add suffix -Z (e.g. MP6906GS-Z)
- \* For Tape & Reel, add suffix -Z (e.g. MP6906GJ-Z)

**TOP MARKING (MP6906GS)**

**MP6906**  
**LLLLLLL**  
**MPSYWW**

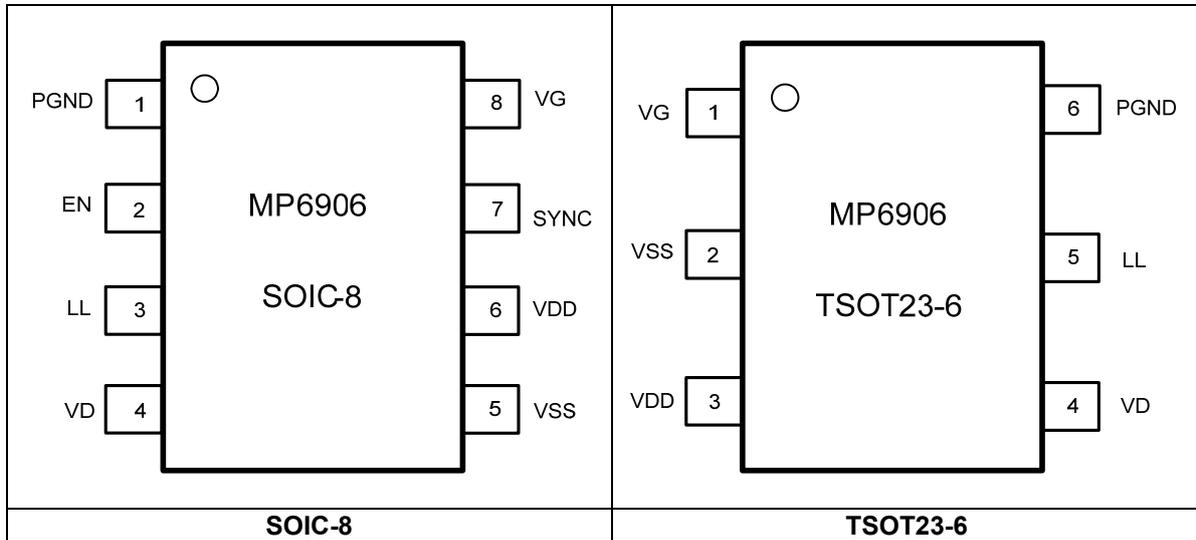
MP6906: Product code of MP6906GS  
MPS: MPS prefix  
Y: Year code  
WW: Week code  
LLL: Lot number

**TOP MARKING (MP6906GJ)**

**|AMQY**

MMQ: Product code of MP6906GJ  
Y: Year code

### PACKAGE REFERENCE



#### ABSOLUTE MAXIMUM RATINGS <sup>(2)</sup>

$V_{DD}$ to $V_{SS}$ .....	-0.3V to +38V
PGND to $V_{SS}$ .....	-0.3V to +0.3V
$V_G$ to $V_{SS}$ .....	-0.3V to +20V
$V_D$ to $V_{SS}$ .....	-1V to +180V
SYNC, LL, EN to $V_{SS}$ .....	-0.3V to +6.5V
Continuous power dissipation ( $T_A = +25^\circ\text{C}$ ) <sup>(3)</sup>	
SOIC-8 .....	1.4W
TSOT23-6 .....	0.57W
Junction temperature .....	150°C
Lead temperature (solder) .....	260°C
Storage temperature .....	-55°C to +150°C

#### Recommended Operation Conditions <sup>(4)</sup>

$V_{DD}$ to $V_{SS}$ .....	4.2V to 35V
Operating junction temp. ( $T_J$ ) ..	-40°C to +125°C

#### Thermal Resistance <sup>(5)</sup>    $\theta_{JA}$    $\theta_{JC}$

SOIC-8 .....	90	45	°C/W
TSOT23-6 .....	220	110	°C/W

#### NOTES:

- 2) Exceeding these ratings may damage the device.
- 3) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J(\text{MAX})$ , the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D(\text{MAX}) = (T_J(\text{MAX}) - T_A) / \theta_{JA}$ . Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 4) The device is not guaranteed to function outside of its operating conditions.
- 5) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{DD} = 12V$ ,  $-40^{\circ}C \leq T_J \leq +125^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
$V_{DD}$ voltage range			4.2		35	V
$V_{DD}$ UVLO rising					4.2	V
$V_{DD}$ UVLO hysteresis			0.13			V
Operating current	$I_{CC}$	$C_{LOAD} = 5nF$ , $F_{SW} = 100kHz$		8	10	mA
Quiescent current	$I_q$	$V_{SS} - V_D = 0.5V$		2	3	mA
Shutdown current <sup>(6)</sup>		$V_{DD} = 4V$ , $EN=0V$			150	$\mu A$
		$V_{DD} = 20V$ , $EN = 0V$			200	
Light-load mode current				150	220	$\mu A$
Thermal shutdown <sup>(7)</sup>				150		$^{\circ}C$
Thermal shutdown hysteresis <sup>(7)</sup>				30		$^{\circ}C$
Enable UVLO rising	$V_{EN-R}$		1.2	1.5	1.8	V
Enable UVLO hysteresis			0.1	0.2		V
Internal pull-up current on EN				10	18	$\mu A$
<b>Control Circuitry Section</b>						
$V_{SS}-V_D$ forward voltage	$V_{fwd}$		12	23	34	mV
Turn-off threshold ( $V_{SS}-V_D$ )			-6	3	12	mV
Turn-on delay	$T_{Don}$	$C_{LOAD} = 5nF$ , $V_{GS} = 2V$		200	300	ns
		$C_{LOAD} = 10nF$ , $V_{GS} = 2V$		250	450	ns
Input bias current on VD		$V_D = 180V$			1	$\mu A$
Turn-on blanking time	$T_{B\_ON}$	$C_{LOAD} = 5nF$	1.2	1.9	2.7	$\mu s$
Turn-off blanking $V_{DS}$ threshold	$V_{B\_OFF}$		1.4		2	V
Turn-off threshold on SYNC	$V_{SYN}$		1.6	2	2.4	V
Internal pull-down current on SYNC		$V_{SYN} = 5V$		10	15	$\mu A$
Light-load-enter SYNC duration	$T_{SYN}$		75	95	115	$\mu s$
Light-load-enter pulse width	$T_{LL}$	$R_{LL} = 200k\Omega$	2.2	3.6	4.9	$\mu s$
Light-load-enter pulse width hysteresis	$T_{LL-H}$	$R_{LL} = 200k\Omega$		0.6		$\mu s$
Gate disable threshold on LL	$V_{LL\_DIS}$			0.2	0.31	V
Turn-on threshold ( $V_{DS}$ )	$V_{LL-DS}$	$V_{DD} = 12V$	-400	-275	-150	mV
<b>Gate Driver Section</b>						
$V_G$ (low)	$V_{G-L}$	$I_{LOAD} = 1mA$		0.05	0.1	V
$V_G$ (high)	$V_{G-H}$	$V_{DD} > 10.5V$	10.5	12	13	V
		$V_{DD} \leq 10.5V$		$V_{DD}$		
SYNC turn-off propagation delay				40	70	ns
Turn-off propagation delay		$V_D = V_{SS}$		25	50	ns
Turn-off total delay	$T_{Doff}$	$V_D = V_{SS}$ , $C_{LOAD} = 5nF$ , $R_{GATE} = 0\Omega$ , $V_{GS} = 2V$		35	60	ns
		$V_D = V_{SS}$ , $C_{LOAD} = 10nF$ , $R_{GATE} = 0\Omega$ , $V_{GS} = 2V$		45	95	ns
Pull-down impedance				1	2	$\Omega$

**NOTE:**

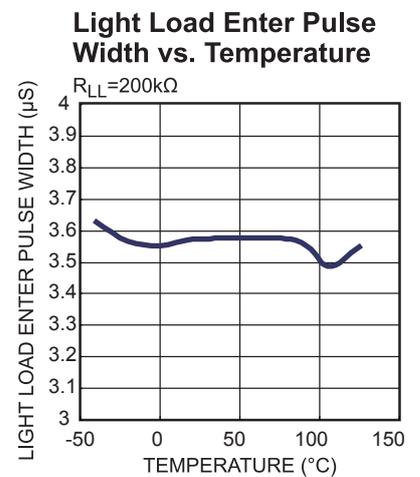
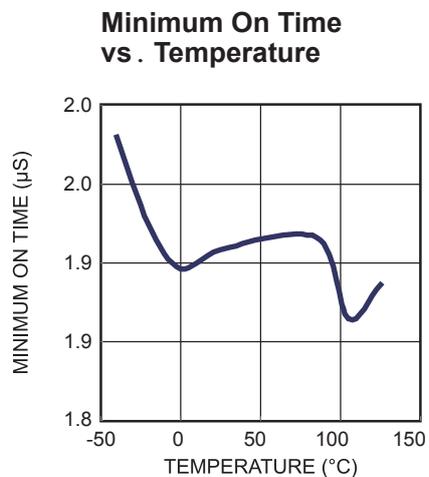
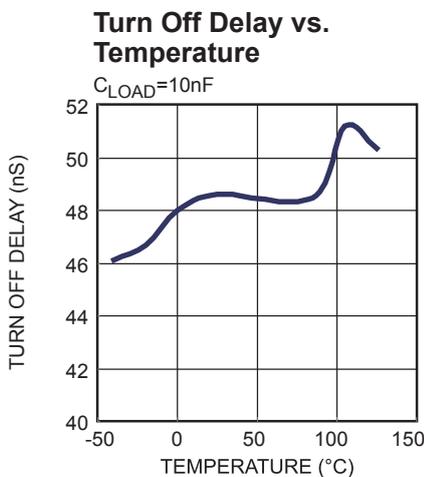
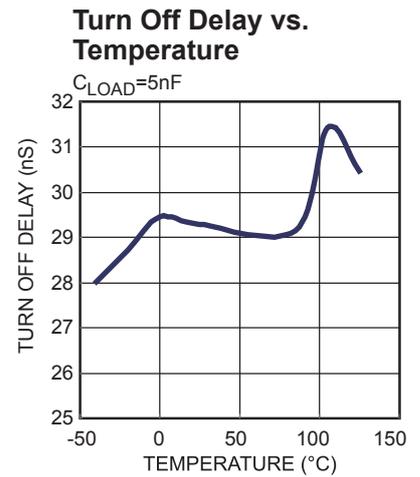
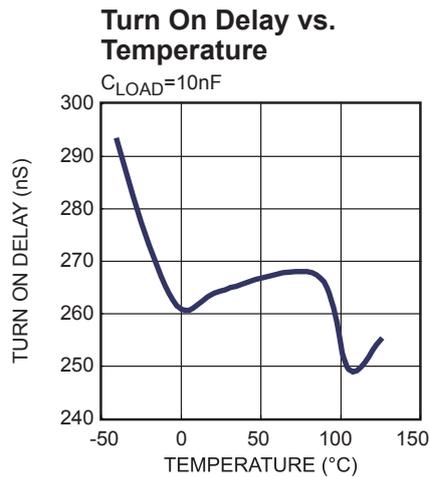
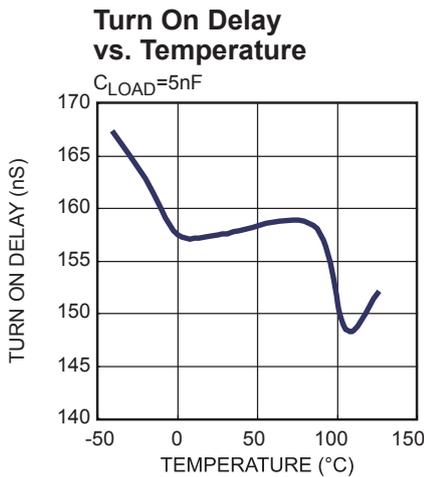
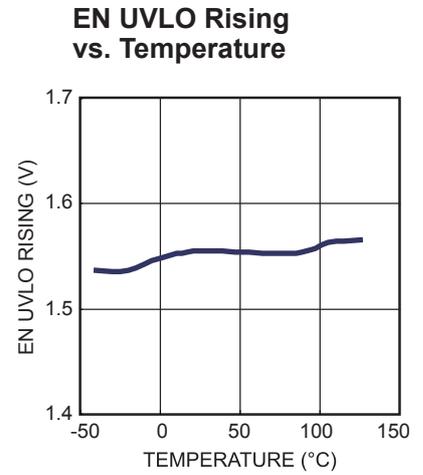
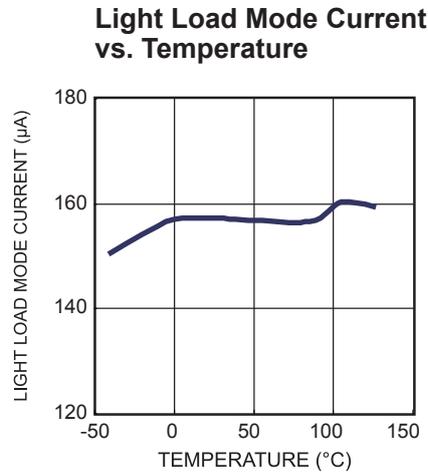
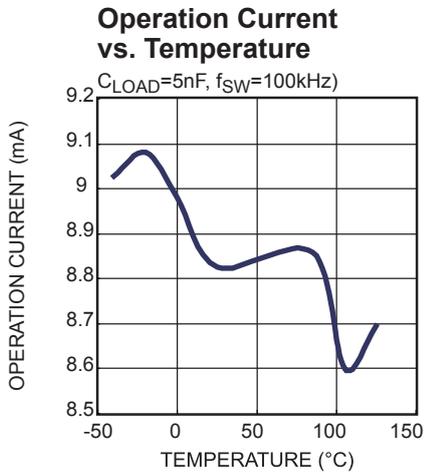
- 6) Only for SOIC package
- 7) Guaranteed by characterization.

**PIN FUNCTIONS**

Pin # (SOIC-8)	Pin # (TSOT23-6)	Name	Description
1	6	PGND	<b>Power ground.</b> PGND is the return for the driver switch.
2	-	EN	<b>Enable.</b> Active high.
3	5	LL	<b>Light-load timing setting.</b> Connect a resistor to set the light-load timing. Leave LL open, or the IC will never enter light-load mode. Pulling LL low disables the gate driver.
4	4	VD	<b>FET drain voltage sense.</b>
5	2	VSS	<b>Ground.</b> VSS is also used as reference for VD.
6	3	VDD	<b>Supply voltage.</b>
7	-	SYNC	<b>Interface for external signal control.</b> Pulling SYNC high shuts down the gate driver immediately.
8	1	VG	<b>Gate drive output.</b>

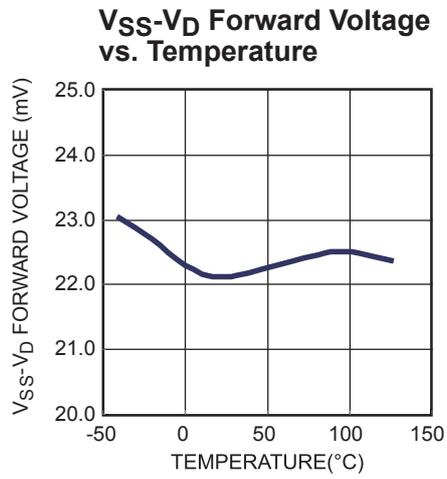
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 12V$ , unless otherwise noted.



**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$V_{DD} = 12V$ , unless otherwise noted.

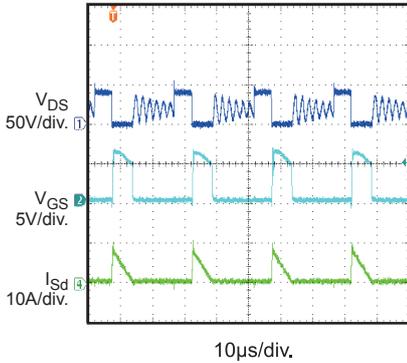


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

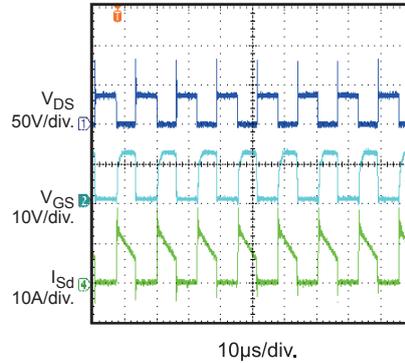
$V_{DD} = 12V$ , unless otherwise noted.

**Operation in 90W Flyback Application**

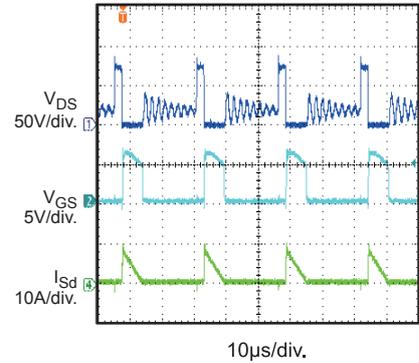
$V_{IN}=90Vac$   $I_{OUT}=1A$


**Operation in 90W Adapter Application**

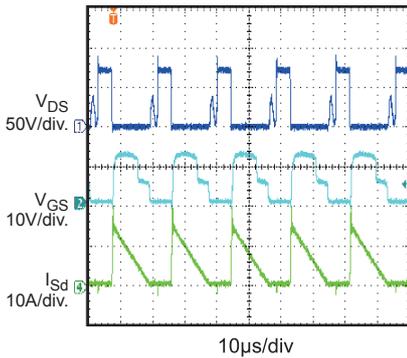
$V_{IN}=90Vac$   $I_{OUT}=4.7A$


**Operation in 90W Flyback Application**

$V_{IN}=250Vac$   $I_{OUT}=1A$


**Operation in 90W Adapter Application**

$V_{IN}=250Vac$   $I_{OUT}=4.7A$


**NOTE:**

8) See Figure 20 for test circuit.

### FUNCTIONAL BLOCK DIAGRAM

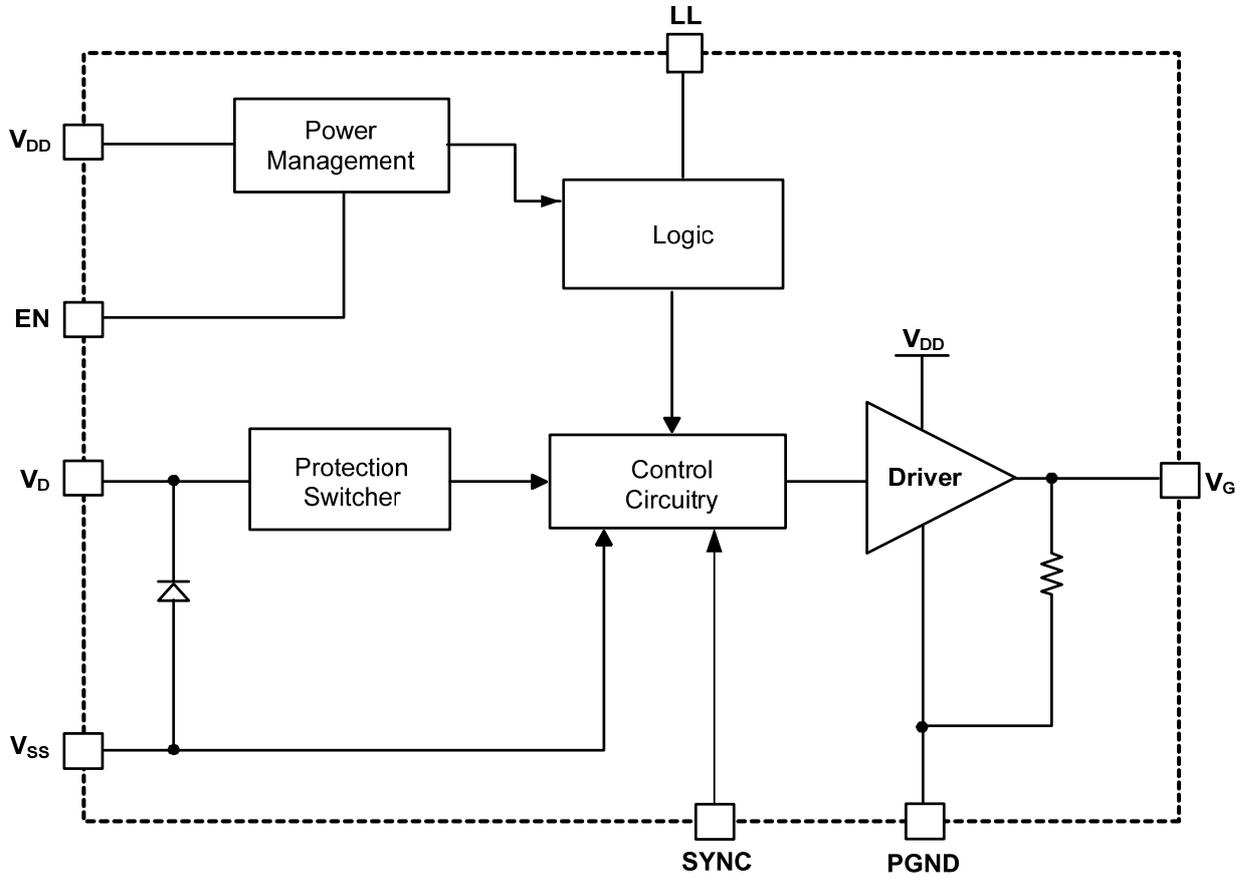


Figure 1: MP6906 Block Diagram

## OPERATION

The MP6906 supports operation in DCM and quasi-resonant flyback converters. The control circuitry controls the gate in forward mode and turns the gate off when the MOSFET current is fairly low.

### VD Clamp

Because  $V_D$  can go as high as 180V, a high-voltage JFET is used at the input. To avoid excessive currents when  $V_g$  drops below  $-0.7V$ , a  $1k\Omega$  resistor is recommended between  $V_D$  and the drain of the external MOSFET.

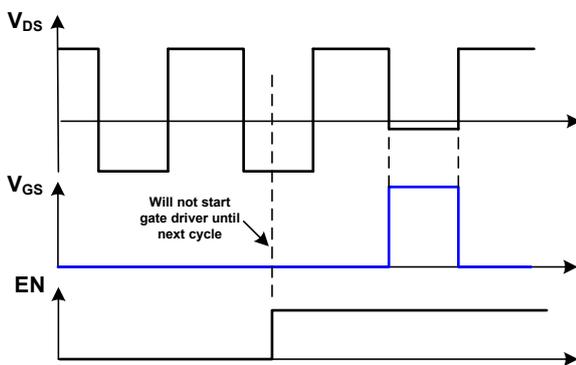
### Under-Voltage Lockout (UVLO)

When  $V_{DD}$  is below the 4.2V UVLO threshold, the part enters sleep mode, and  $V_G$  remains at a low level.

### Enable (EN)

If EN is pulled low, the part is in shutdown mode, which consumes  $<150\mu A$  shutdown current.

If EN is pulled high during the rectification cycle, the gate driver will not start until the next rectification cycle starts (see Figure 2).



**Figure 2: EN Control Scheme**

### Thermal Shutdown

If the junction temperature of the chip exceeds  $150^\circ C$ ,  $V_g$  is pulled low, and the part stops switching. The part returns to normal operation after the junction temperature has dropped to  $120^\circ C$ .

### Turn-On Phase

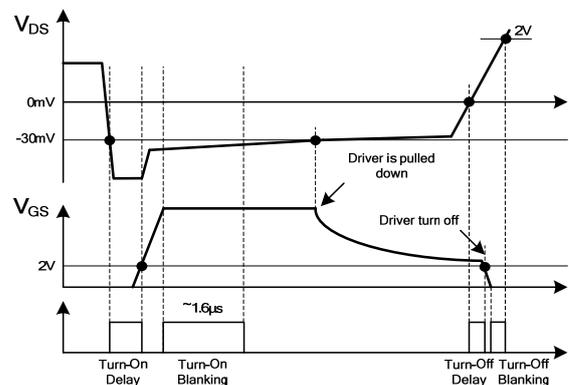
When the switch current flows through the body diode of the MOSFET, there is a negative  $V_{DS}$  ( $V_D - V_{SS}$ ) across it ( $<-500mV$ ). The  $V_{DS}$  is much lower than the forward voltage drop of the control circuitry ( $-30mV$ ), which turns on the MOSFET

after a turn-on delay (see Figure 3). **Turn-On Blanking**

The control circuitry contains a blanking function. When the MOSFET turns on, the control circuitry ensures the on state lasts for a specific period of time. The turn-on blanking time is  $\sim 1.6\mu s$ , during which the turn-off threshold is blanked (see Figure 3).

### Conduction Phase

When  $V_{ds}$  rises above the forward voltage drop ( $-30mV$ ), according to the decrease of the switching current, the MP6906 pulls down the gate voltage level to make the on resistance of the synchronous MOSFET larger to ease the rise of  $V_{ds}$ .



**Figure 3: Turn On/Off Timing Diagram**

With this control scheme,  $V_{DS}$  is adjusted to around  $-30mV$ , even when the current through the MOSFET is fairly low. This function keeps the driver voltage at a very low level when the synchronous MOSFET is about to be turned off, which boosts the turn-off speed.

### Turn-Off Phase

When  $V_{DS}$  rises to trigger the turn-off threshold ( $0mV$ ), the gate voltage is pulled to zero after a very short turn-off delay (see Figure 3).

### Turn-Off Blanking

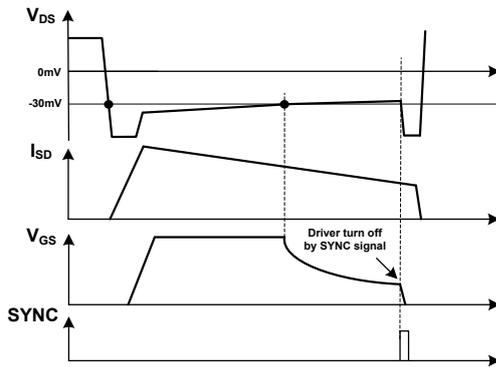
After the gate driver is pulled to zero by  $V_{DS}$  reaching the turn-off threshold ( $0mV$ ), a turn-off blanking time is applied, during which the gate driver signal is latched off. The turn-off blanking is removed when the  $V_{DS}$  voltage rises above 2V (see Figure 3).

### SYNC Turn-Off for CCM Operation

An external turn-off signal can be applied on SYNC to turn-off the gate driver signal, which provides more reliable operation in CCM.

A rising edge, exceeding 2V, applied on SYNC turns off the gate driver signal immediately (see Figure 4).

The gate driver of the MP6906 will remain low as long as the SYNC voltage is high.

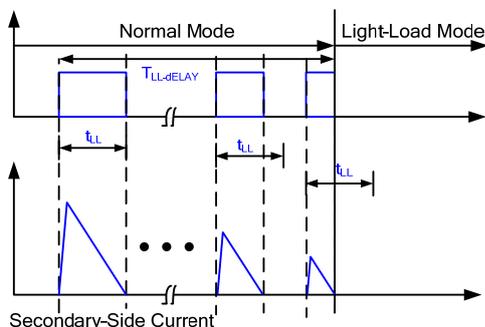


**Figure 4: SYNC Turn Off for CCM**

### Light-Load Latch-Off Function

The gate driver of the MP6906 is latched off to save driver loss and improve efficiency during a light-load condition.

When the synchronous MOSFET conducting period remains lower than  $T_{LL}$  for longer than the light-load-enter delay ( $T_{LL-Delay}$ ), the MP6906 enters light-load mode and latches off the gate driver (see Figure 5). The synchronous MOSFET conducting period lasts from the time the gate driver turns on until  $V_{GS}$  drops below 1V ( $V_{LL-GS}$ ).



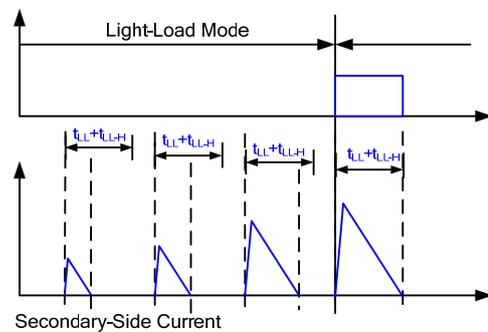
**Figure 5: MP6906 Enters Light-Load Mode**

The light-load-enter timing ( $T_{LL}$ ) is programmable by connecting a resistor ( $R_{LL}$ ) on LL. By

monitoring the LL current (the LL voltage remains at  $\sim 2V$  internally),  $T_{LL}$  is set. A 1nF capacitor is recommended to decouple the noise on LL. See Equation (1)

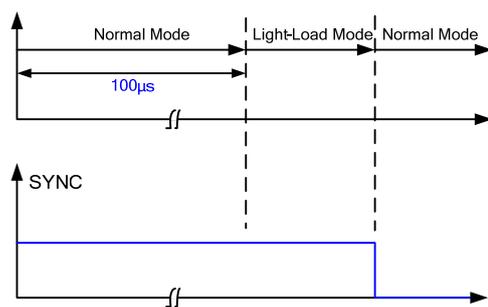
$$T_{LL} = R_{LL} (k\Omega) \cdot \frac{3.6\mu s}{200k\Omega} \quad (1)$$

During light-load mode, the MP6906 monitors the synchronous MOSFET body diode conducting period by sensing the time duration of when  $V_{DS}$  is below  $-250mV$  ( $V_{LL-DS}$ ). If the time duration is longer than  $T_{LL}+T_{LL-H}$  ( $T_{LL-H}$  is the light-load-enter pulse width hysteresis), the light-load mode ends, and the gate driver is unlatched to re-start the synchronous rectification (see Figure 6).



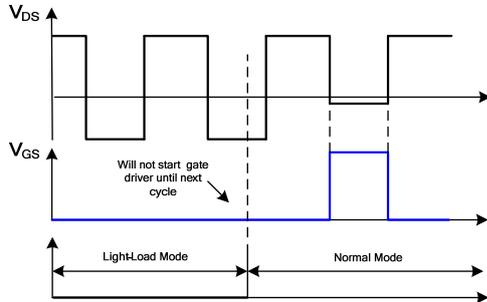
**Figure 6: MP6906 Exits Light-Load Mode**

The MP6906 enters light-load mode when the SYNC voltage is pulled high ( $>2V$ ) for more than 100 $\mu s$ . The light-load mode ends once the SYNC voltage is pulled low (see Figure 7).



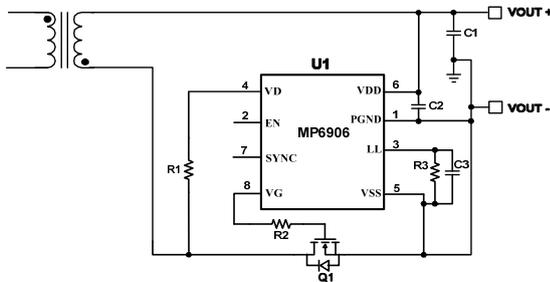
**Figure 7: Light-Load Mode Controlled by SYNC**

If the light-load mode ends during the rectification cycle, the gate driver signal will not show up until the next rectification cycle starts (see Figure 8).



**Figure 8: Gate Driver Start after Existing Light-Load Mode**

**Typical System Implementations**



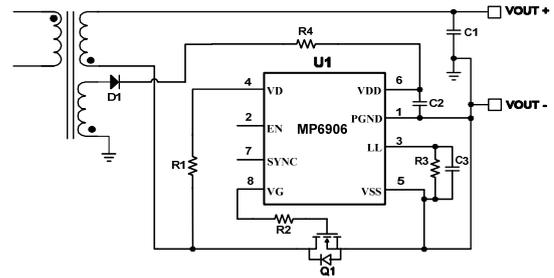
**Figure 9: IC Power derived directly from Output Voltage**

Figure 9 shows the typical system implementation for the IC power supply directly derived from the output voltage, which is available in low-side rectification. The IC benefits from the wide  $V_{DD}$  operating range (4.2V to 35V). The MP6906 supports most application fields with low-side rectification by directly deriving the supply power from the system output.

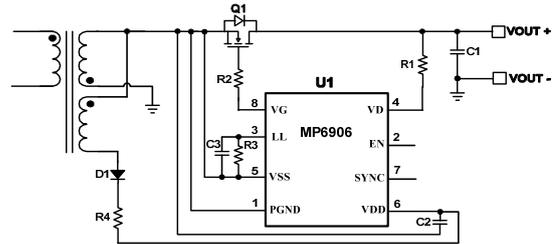
If the output voltage is out of the  $V_{DD}$  operating range or high-side rectification is used, an auxiliary winding solution for the IC's power supply is recommended (see Figure 10 and Figure 11). The auxiliary winding turn count ( $N_{au}$ ) can be set using Equation (2):

$$N_{au} = \frac{V_{DD}}{V_{OUT}} \cdot N_s \quad (2)$$

Where  $N_s$  is the secondary winding turn count.

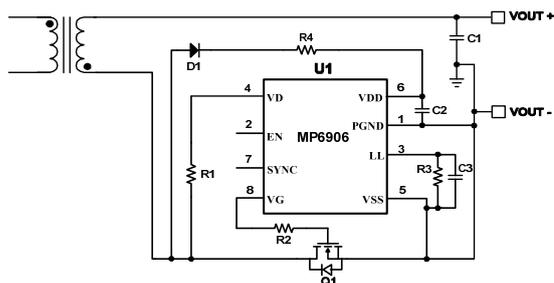


**Figure 10: IC Power Derived from the Auxiliary Winding in Low-Side Rectification**



**Figure 11: IC Power Derived from the Auxiliary Winding in High-Side Rectification**

A simple non-auxiliary-winding solution for the IC's power supply is provided in Figure 12 and Figure 13. The IC power is derived from the secondary transformer winding through a diode. When using this power solution, make sure the winding voltage is lower than the higher limit of the  $V_{DD}$  operating range (35V). The winding voltage is  $V_s = V_{OUT} + V_{IN\_MAX}/n$  in Figure 12 where  $V_{OUT}$  is the output voltage;  $V_{IN\_MAX}$  is the maximum input voltage, and  $n$  is the transformer turn ratio.  $V_s = V_{IN\_MAX}/n$  in Figure 13.



**Figure 12: IC Power Derived from the Secondary Winding in Low-Side Rectification**



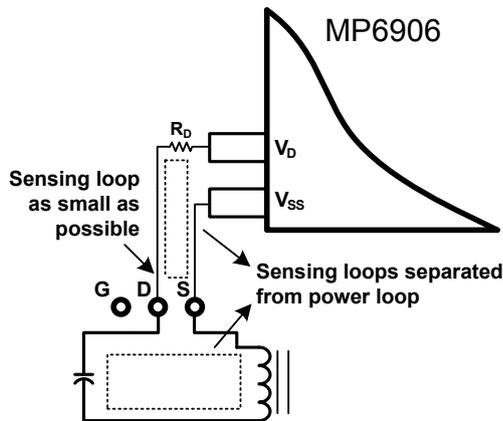


Figure 17: Voltage Sensing for  $V_D/V_{SS}$  on MP690

- Place a decoupling ceramic capacitor (no smaller than  $1\mu F$ ) from  $V_{DD}$  to  $PGND$  close to the IC to get adequate filtering.

**Gate Driver Loop**

- Make the gate driver loop as small as possible in order to minimize the parasitic inductance.
- Keep the driver signal far away from the  $V_D$  sensing trace on the layout.

**Layout Example**

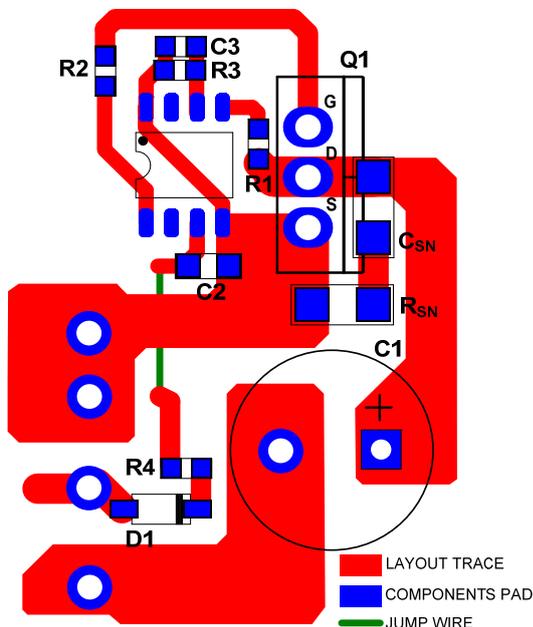


Figure 18: Layout Example with TO220 package SR FET

Figure 18 shows a layout example of a single layer with a through-hole transformer and a TO220 package SR FET.  $R_{SN}$  and  $C_{SN}$  are the RC snubber network for the SR FET.

The sensing loop ( $V_D$  and  $V_{SS}$  to the SR FET) is minimized and kept separate from the power loop. The  $V_{DD}$  decoupling capacitor ( $C_4$ ) is placed beside  $V_{DD}$ .

Figure 19 shows another layout example of a single layer with a PowerPAK/SO8 package SR FET, which also has a minimized sensing loop and power loop to avoid the loops interfering with one another.

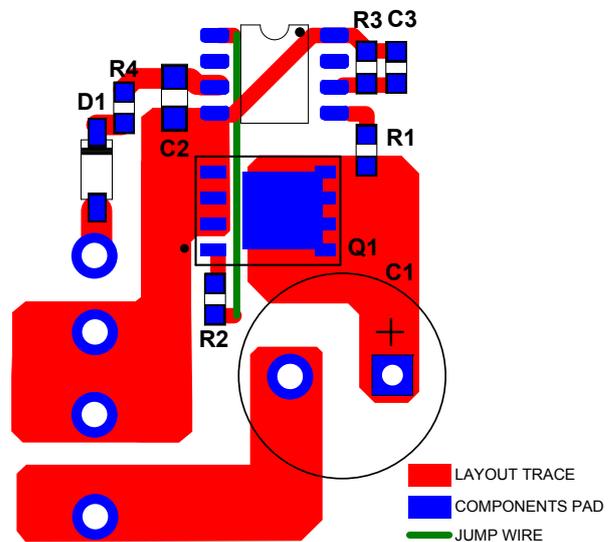


Figure 19: Layout Example with PowerPAK/SO8 Package SR FET

### TYPICAL APPLICATION CIRCUIT

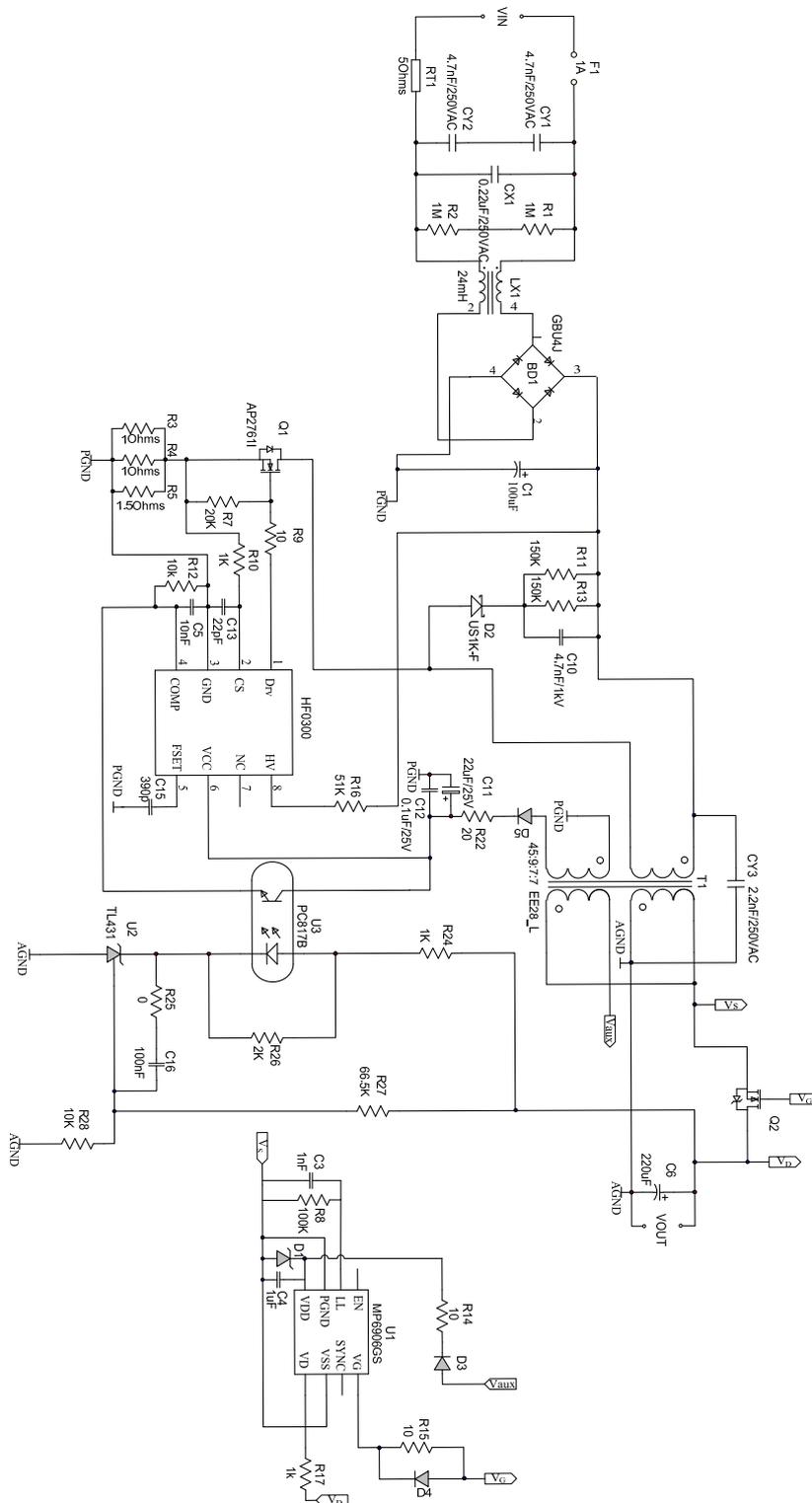
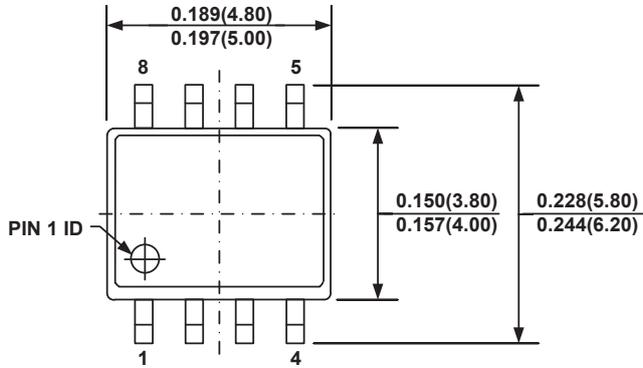


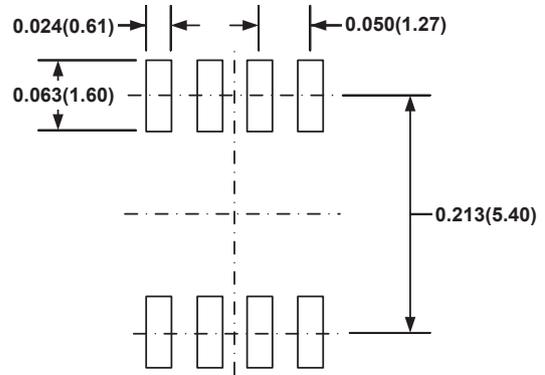
Figure 20: MP6906 for a Secondary Synchronous Controller in a 90W Flyback Application

### PACKAGE INFORMATION

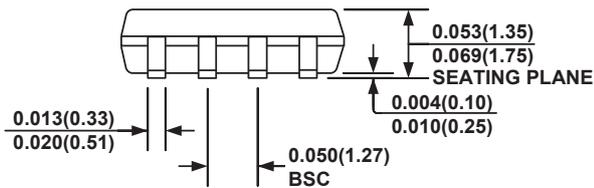
#### SOIC-8



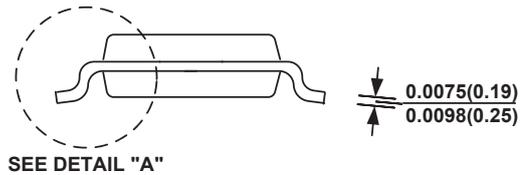
**TOP VIEW**



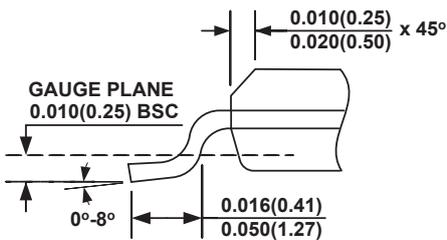
**RECOMMENDED LAND PATTERN**



**FRONT VIEW**



**SIDE VIEW**

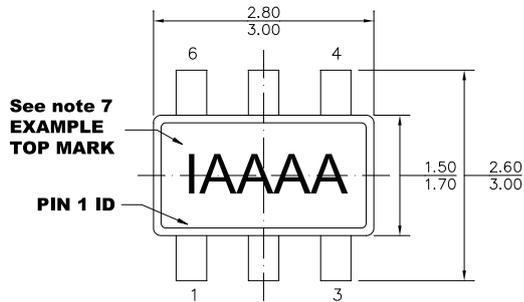


**DETAIL "A"**

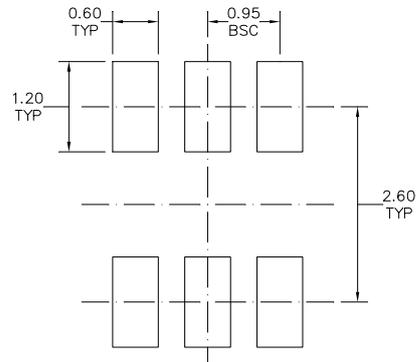
**NOTE:**

- CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- DRAWING IS NOT TO SCALE.

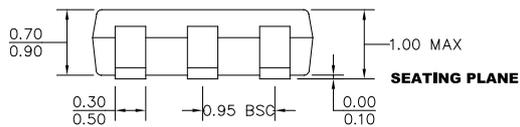
**TSOT23-6**



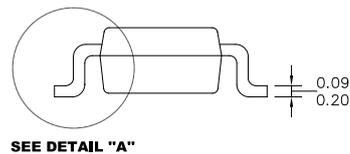
**TOP VIEW**



**RECOMMENDED LAND PATTERN**



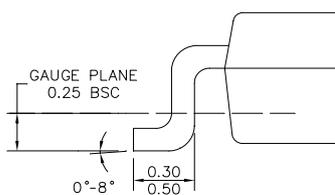
**FRONT VIEW**



**SIDE VIEW**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
- 6) DRAWING IS NOT TO SCALE.
- 7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)



**DETAIL "A"**

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