# MP6902A

## Fast Turn-Off Intelligent Controller

## DESCRIPTION

The MP6902A is a low-drop diode emulator IC for flyback converters, which replaces Schottky rectification diodes to achieve high efficiency when combined with an external switch.

The MP6902A regulates the forward drop of an external switch to about 70mV and switches it off as soon as the voltage becomes negative. The MP6902A has a light-load sleep mode that reduces the quiescent current to 300µA.

## FEATURES

- Supports CCM, DCM and Quasi-Resonant Flyback Converters
- Works with 12V Standard and 5V Logic Level MOSFETs
- Compatible with Energy Star, 1W Standby Requirements
- $V_{DD}$ Range from 8V to 24V
- 70mV $V_{DS}$ Regulation Function(1)
- Fast Turn-Off Total Delay of 20ns
- Max 400kHz Switching Frequency
- Light-Load Mode Function(1) with 300µA Quiescent Current
- Supports High-Side and Low-Side Rectification
- Power Savings of Up to 1.5W in a Typical Notebook Adapter
- Available in a TSOT23-6 Package

## APPLICATIONS

- Industrial Power Systems
- Distributed Power Systems
- Battery-Powered Systems
- Flyback Converters

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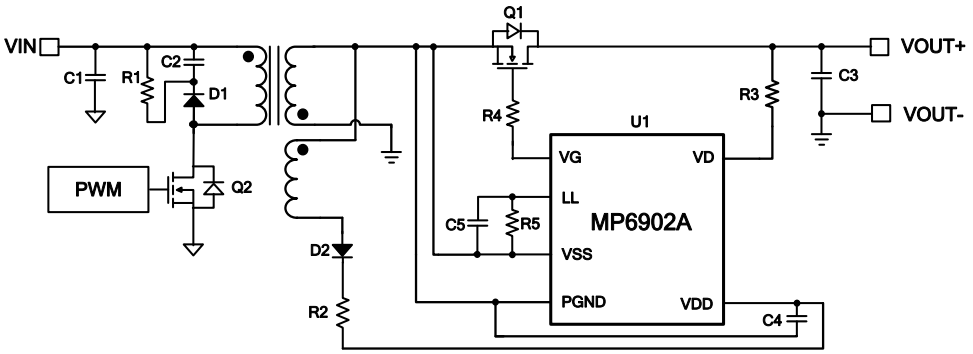
**NOTE:**

1) Related issued patent: US Patent US8,067,973; US8,400,790. CN Patent ZL201010504140.4; ZL200910059751.X. Other patents pending.

## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MP6902AGJ | TSOT23-6 | *See Below* |

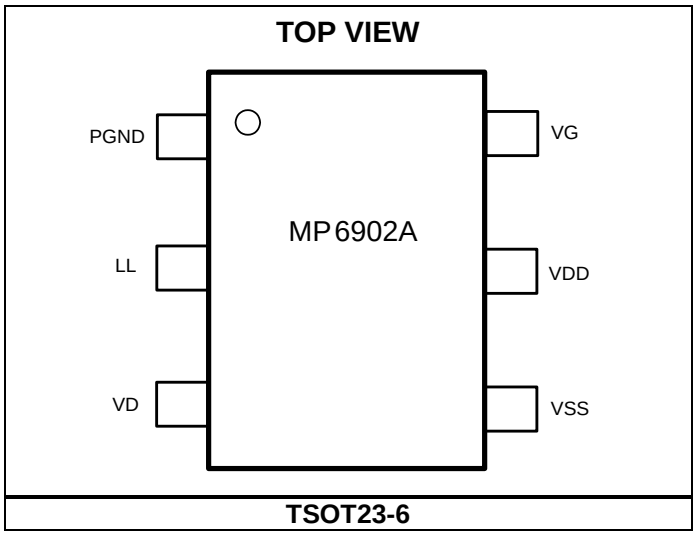
* For Tape & Reel, add suffix –Z (e.g. MP6902AGJ–Z)

## TOP MARKING

|AUTY

AUT: Product code of MP6902AGJ
Y: Year code

## PACKAGE REFERENCE



## ABSOLUTE MAXIMUM RATINGS (2)

VDD to VSS ..... -0.3V to +27V
PGND to VSS ..... -0.3V to +0.3V
VG to VSS ..... -0.3V to $V_{CC}$
VD to VSS ..... -0.7V to +180V
LL to VSS ..... -0.3V to +6.5V
Maximum operating frequency ..... 400kHz
Continuous power dissipation ($T_A$ = +25°C) (3) ..... 1.4W
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C
Storage temperature ..... -55°C to +150°C

## *Recommended Operation Conditions* (4)

VDD to VSS ..... 8V to 24V
Operating junction temp. ($T_J$). .. -40°C to +125°C

## *Thermal Resistance* (5) $\theta_{JA}$ $\theta_{JC}$

| | $\theta_{JA}$ | $\theta_{JC}$ | |
|---|---|---|---|
| TSOT23-6 | 220 | 110 | °C/W |

**NOTES:**

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$(MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$(MAX)=($T_J$(MAX)-$T_A$)/ $\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

**$V_{DD}$ = 12V, -40°C ≤ $T_J$ ≤ +125°C, unless otherwise noted.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| VDD voltage range | | | 8 | | 24 | V |
| VDD UVLO rising | | | 4.5 | 6.0 | 7.0 | V |
| VDD UVLO hysteresis | | | 0.8 | 1 | 1.25 | V |
| Operating current | $I_{CC}$ | $C_{LOAD}$ = 5nF, $F_{SW}$ = 100kHz | | 8 | 10 | mA |
| Quiescent current | $I_Q$ | VSS - VD = 0.5V | | 2 | 3.6 | mA |
| Shutdown current | | VDD = 4V, light-load mode | | 150 | 260 | µA |
| Light-load mode current | | | | 300 | 420 | µA |
| Thermal shutdown | | | | 170 | | °C |
| Thermal shutdown hysteresis | | | | 30 | | °C |
| **Control Circuitry Section** | | | | | | |
| VSS - VD forward voltage | $V_{fwd}$ | | 50 | 70 | 85 | mV |
| Turn-on delay | $T_{Don}$ | $C_{LOAD}$ = 5nF, -20°C < $T_J$ ≤ 125°C | | 150 | 260 | ns |
| | | $C_{LOAD}$ = 5nF, -40°C ≤ $T_J$ ≤ -20°C | | 250 | | |
| | | $C_{LOAD}$ = 10nF, -20°C < $T_J$ ≤ 125°C | | 200 | 350 | |
| | | $C_{LOAD}$ = 10nF, -40°C ≤ $T_J$ ≤ -20°C | | 350 | | |
| Input bias current on VD | | VD = 180V | | | 1 | µA |
| Pull-down resistance of VG | | | | 10 | 20 | kΩ |
| Minimum on time | $T_{MIN}$ | $C_{LOAD}$ = 5nF | 0.6 | 1.2 | 2.4 | µs |
| Light-load enter delay | $T_{LL-Delay}$ | $R_{LL}$ = 100kΩ | 70 | 100 | 130 | µs |
| Light-load enter pulse width | $T_{LL}$ | $R_{LL}$ = 100kΩ | 1.2 | 1.9 | 2.6 | µs |
| Light-load enter pulse-width hysteresis | $T_{LL-H}$ | $R_{LL}$ = 100kΩ | | 0.2 | | µs |
| Light-load resistor value | $R_{LL}$ | | 30 | | 300 | kΩ |
| Light-load mode exit pulse-width threshold ($V_{DS}$) | $V_{LL-DS}$ | | -460 | -250 | -120 | mV |
| Light-load mode enter pulse width threshold ($V_{GS}$) (6) | $V_{LL-GS}$ | | | 1.0 | | V |
| **Gate Driver Section** | | | | | | |
| VG (low) | | $I_{LOAD}$ = 1mA | | 0.05 | 0.1 | V |
| VG (high) | | VDD > 17V | 13 | 14.8 | 16.5 | V |
| | | VDD < 17V | | VDD - 2.2 | | |
| Turn-off threshold (VSS - VD) | $V_{OFF}$ | | 20 | 30 | 45 | mV |
| Turn-off propagation delay | | VD = VSS | | 15 | | ns |
| Turn-off total delay | $T_{Doff}$ | VD = VSS, $C_{LOAD}$ = 5nF, $R_{GATE}$ = 0Ω | | 20 | 60 | ns |
| | $T_{Doff}$ | VD = VSS, $C_{LOAD}$ = 10nF, $R_{GATE}$ = 0Ω | | 40 | 70 | ns |
| Pull-down impedance | | | | 1 | 2 | Ω |
| Pull-down current (6) | | 3V < VG < 10V | | 2 | | A |

**NOTE:**

6) Guaranteed by design and characterization.

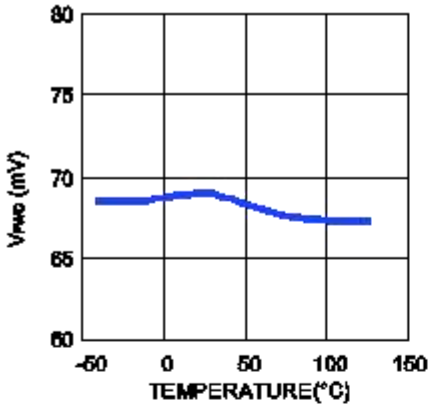
## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | PGND | **Power ground.** PGND is the return for the driver switch. |
| 2 | LL | **Light-load timing setting.** Connect a resistor to LL to set the light-load timing. |
| 3 | VD | **MOSFET drain voltage sense.** |
| 4 | VSS | **Ground.** VSS is also used as the reference for VD. |
| 5 | VDD | **Supply voltage.** |
| 6 | VG | **Gate drive output.** |

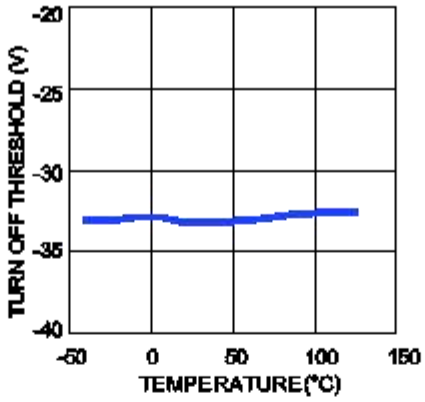
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{DD}$ = 12V, unless otherwise noted.**

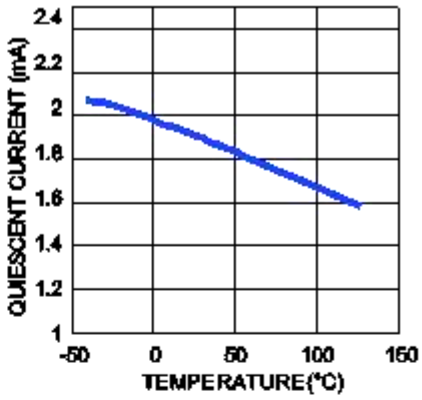
**$V_{FWD}$ vs. Temperature**



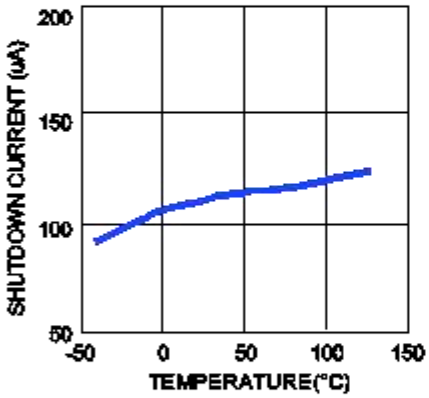

**Turn-Off Threshold vs. Temperature**



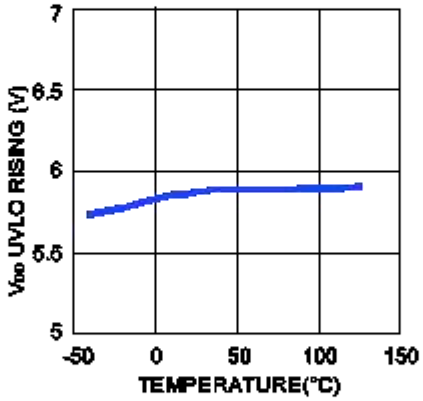

**Quiescent Current vs. Temperature**




**Shutdown Current vs. Temperature**

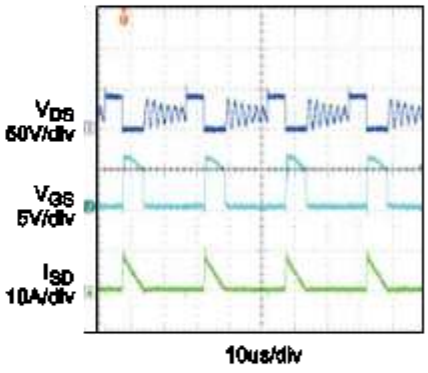



**$V_{DD}$ UVLO Rising vs. Temperature**



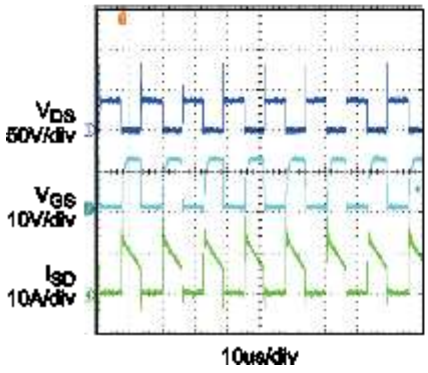

**Operation in 90W Flyback Application[7]**

**($V_{IN}$=90Vac, $I_{OUT}$=1A)**



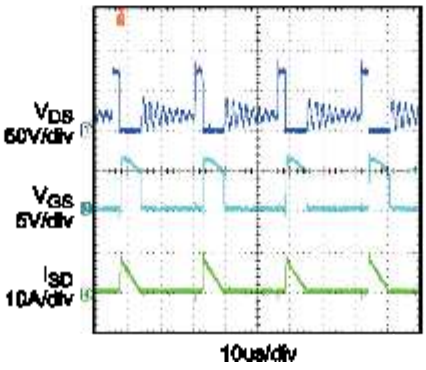

**Operation In 90W Flyback Application**

**($V_{IN}$=90Vac, $I_{OUT}$=4.7A)**



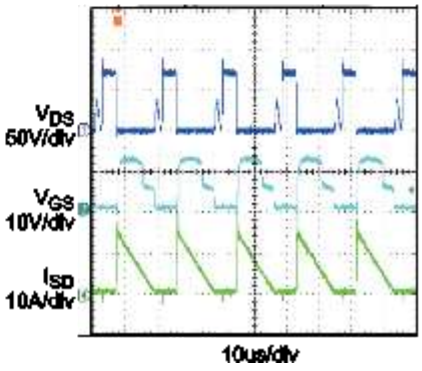

**Operation In 90W Flyback Application**

**($V_{IN}$=250Vac, $I_{OUT}$=1A)**




**Operation in 90W Flyback Application**

**($V_{IN}$=250Vac, $I_{OUT}$=4.7A)**




**NOTE:**

7) See Figure 13 for the test circuit.

## BLOCK DIAGRAM

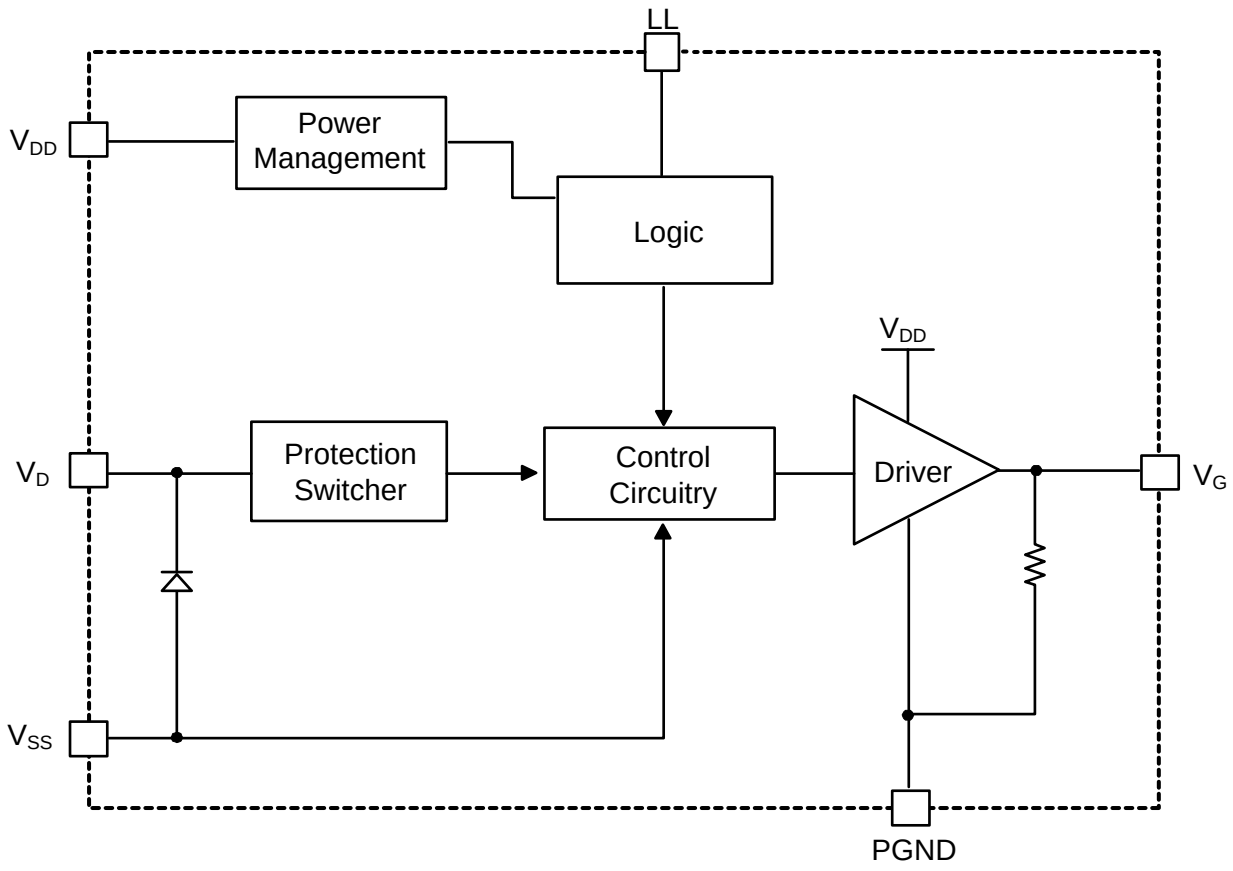



**Figure 1: Functional Block Diagram**

## OPERATION

The MP6902A supports operation in continuous conduction mode (CCM), discontinuous conduction mode (DCM) and quasi-resonant flyback converters. The control circuitry controls the gate in forward mode and turns the gate off when the MOSFET current is fairly low.

### Blanking

The control circuitry contains a blanking function. When the gate pulls the MOSFET on or off, the blanking function ensures that the on or off state lasts for at least 0.6ms. The turn-on blanking time ($T_{MIN}$) determines the minimum on time. During the turn-on blanking period, the turn-off threshold is not blanked completely, but changes the threshold voltage to about +50mV (instead of $-V_{OFF}$). This assures that the part can always be turned off, even during the turn-on blanking period, although it does so slower.

### VD Clamp

Since VD can rise as high as 180V, a high-voltage JFET is used at the input. To avoid excessive currents when VG drops below -0.7V, a small resistor is recommended between VD and the drain of the external MOSFET.

### Under-Voltage Lockout (UVLO)

When VDD is below the UVLO threshold, the MP6902A is in sleep mode, and VG is pulled low by a 10kΩ resistor.

### Thermal Shutdown

If the junction temperature of the chip exceeds 170°C, VG is pulled low, and the MP6902A stops switching. The MP6902A resumes normal function after the junction temperature has dropped to 140°C.

### Thermal Design

If the dissipation of the chip is higher than 100mW due to switching frequencies above 100kHz, the thermal dissipation should be considered carefully.

### Turn-On Phase

When the synchronous MOSFET is conducting, current flows through its body diode and generates a negative drain-source voltage ($V_{DS}$) across it.

This body diode voltage drop (<-500mV) is much smaller than the turn on threshold of the control circuitry (-70mV). Therefore, the gate driver voltage is pulled high to turn on the synchronous MOSFET after a turn-on delay of about 150ns (see Figure 2).

Once the turn-on threshold (-70mV) is triggered, a blanking time (minimum on-time, $T_{MIN}$) is added, during which the turn-off threshold is changed from -30mV to +50mV. This blanking time can help prevent an erroneous trigger at the turn-off threshold caused by the turn-on ringing of the synchronous MOSFET.

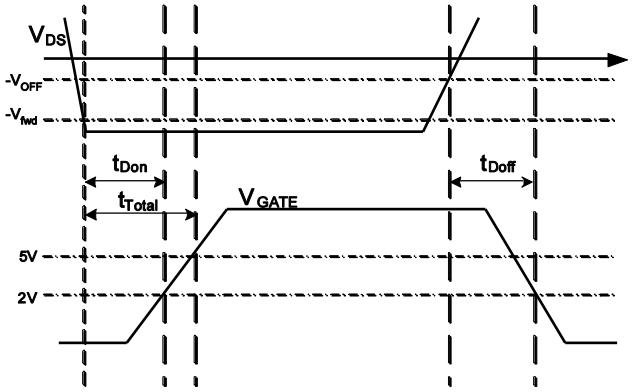



**Figure 2: Turn-On and Turn-Off Delay**

### Conducting Phase

When the synchronous MOSFET is turned on, $V_{DS}$ rises according to its on resistance. Once $V_{DS}$ rises above the turn-on threshold (-70mV), the control circuitry stops pulling up the gate driver, and the gate voltage is forced low by the internal pull-down resistance (10kΩ) to enlarge the on resistance of the synchronous MOSFET to limit the rise of $V_{DS}$. This way, $V_{DS}$ is adjusted to be $-V_{fwd}$, even when the current through the MOSFET is fairly small. This function can make the driver voltage fairly low when the synchronous MOSFET is turned off to make the turn-off speed faster. This function is still active during the turn-on blanking time, which means that the gate driver can still be turned off even with a very small duty of the synchronous MOSFET.

### Turn-Off Phase

When $V_{DS}$ rises to trigger the turn-off threshold ($-V_{OFF}$), the gate voltage is pulled low after a turn-off delay of about 20ns by the control circuitry (see Figure 2). Similar with the turn-on phase, a 200ns blanking time is added after the synchronous MOSFET is turned off to prevent an erroneous trigger.

Figure 3 shows synchronous rectification operation at heavy-load condition. Due to the high current, the gate driver is first saturated, during which the gate driver voltage is kept ~2.2V lower than VDD (when VDD > 17V, the gate driver is clamped internally at ~14.8V). After $V_{DS}$ rises above $-V_{fwd}$, the gate driver voltage decreases to adjust $V_{DS}$ to the typical $-V_{fwd}$.

Figure 4 shows synchronous rectification operation at light-load condition. Due to the low current, the gate driver voltage never saturates but begins decreasing once the synchronous MOSFET is turned on and adjusts $V_{DS}$.

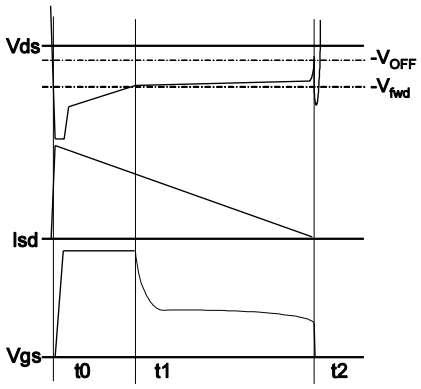



**Figure 3: Synchronous Rectification Operation at Heavy Load**

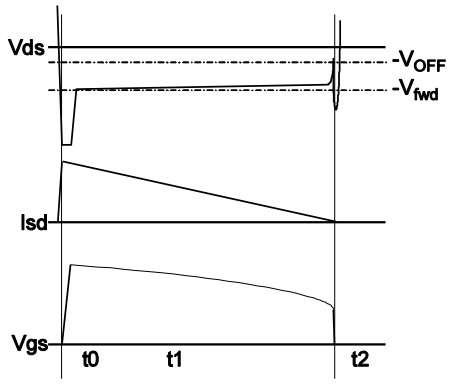



**Figure 4**: **Synchronous Rectification Operation at Light Load**

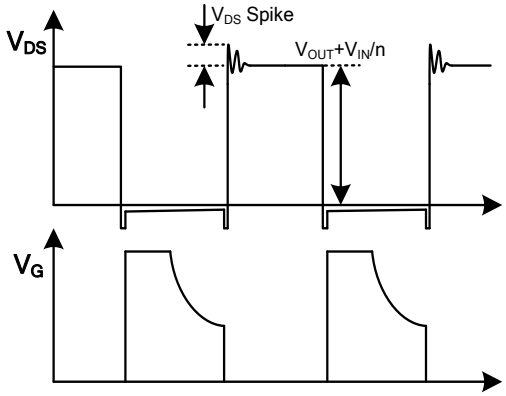



**Figure 5: Drain Source and Gate Driver Voltage on the SR MOSFET**

Figure 5 shows the entire synchronous rectification waveform on the drain-source voltage ($V_{DS}$) and the gate driver signal ($V_{GS}$). For safe operation of the IC, use Equation (1):

$$V_{OUT} + V_{IN}/n + V_{DS\_Spike} < 180V * k \quad (1)$$

Where 180V is the maximum voltage rating on VD, $V_{IN}$ is the input DC voltage, $V_{OUT}$ is the output DC voltage, n is the primary-to-secondary turn ratio of the power transformer, $V_{DS\_Spike}$ is the spike voltage of the drain source (which is led by the leakage inductance), and k is the de-rating factor, which is usually selected as 0.7~0.8.

### Light-Load Latch-Off Function

The gate driver of the MP6902A is latched to save driver loss at light-load condition to improve efficiency. When the synchronous MOSFET's conducting period is lower than the light-load timing ($T_{LL}$) for longer than the light-load enter delay ($T_{LL\text{-}Delay}$), the MP6902A enters light-load mode and latches off the gate driver.

The synchronous MOSFET's conducting period is from the gate driver turning on to the moment $V_{GS}$ drops below 1V ($V_{LL\_GS}$). During light-load mode, the MP6902A monitors the synchronous MOSFET's body diode conducting period by sensing the time duration of $V_{DS}$ below -250mV ($V_{LL\_DS}$). If the time duration is longer than $T_{LL}$ + $T_{LL\text{-}H}$ (where $T_{LL\text{-}H}$ is light-load enter pulse-width hysteresis), the light-load mode is finished, and the gate driver of the MP6902A is unlatched to restart synchronous rectification.

Light-load enter timing ($T_{LL}$) is programmable by connecting a resistor ($R_{LL}$) to LL. By monitoring the LL current (the LL voltage remains at ~2V internally), $T_{LL}$ can be set with Equation (2):

$$T_{LL} \approx R_{LL}(k\Omega) \cdot \frac{2.2\mu s}{100k\Omega} \quad (2)$$

### SR MOSFET Selection and Driver Ability

Power MOSFET selection is a trade-off between $R_{ON}$ and $Q_g$. To achieve high efficiency, a MOSFET with a smaller $R_{ON}$ is always preferred, while a larger $Q_g$ with a smaller $R_{ON}$ makes the turn-on/-off speed lower and leads to a larger power loss. Because $V_{DS}$ is regulated at $-V_{fwd}$ during the driving period, a MOSFET with an $R_{ON}$ that is too small is not recommend because the gate driver may be pulled down to a low level when the MOSFET current is still high, which make the advantage of the low $R_{ON}$ inconspicuous.

Figure 6 shows the typical waveform of QR flyback. Assume the duty cycle is 50% and the output current is $I_{OUT}$.

To achieve a fairly high usage of the MOSFET's $R_{ON}$, it is expected that the MOSFET be fully turned on for at least 50% of the SR conduction period. Calculate $V_{DS}$ with Equation (3):

$$Vds = -Ic \times Ron = -2 \cdot I_{OUT} \times Ron \le -Vfwd \quad (3)$$

Where $V_{DS}$ is the drain-source voltage of the MOSFET, and $V_{fwd}$ is the forward voltage threshold of the MP6902A, which is ~70mV.

The MOSFET's $R_{ON}$ is recommended to be no lower than ~35/$I_{OUT}$ (mΩ). For example, for a 5A application, the $R_{ON}$ of the MOSFET is recommended to be no lower than 7mΩ.

Figure 7 shows the corresponding total delay during the turn-on period ($t_{Total}$) with driving different $Q_g$ MOSFETs. When driving a 120nC $Q_g$ MOSFET, the driver ability of the MP6902A is able to pull up the gate driver voltage of the MOSFET to ~5V in 300ns once the body diode of the MOSFET is conducting, which greatly saves turn-on power loss in the MOSFET's body diode.

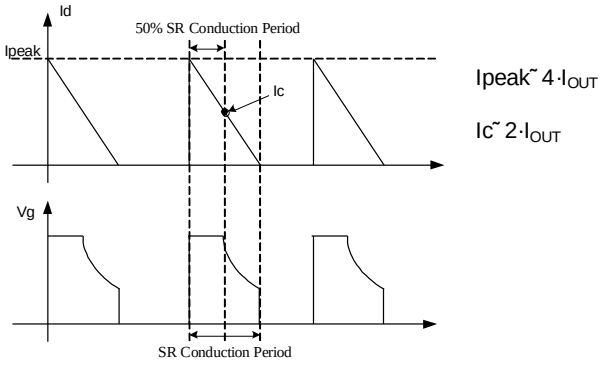



**Figure 6: Synchronous Rectification Typical Waveforms in QR Flyback**

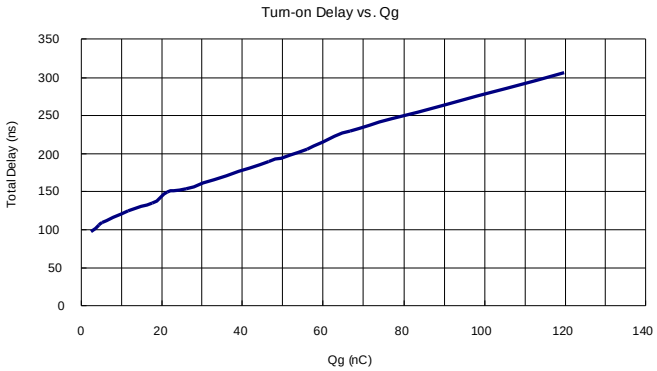



**Figure 7: Total Turn-On Delay vs. $Q_g$**

### Typical System Implementations

Figure 8 shows the typical system implementation for the IC supply derived from the output voltage, which is available in low-side rectification. The output voltage is recommended to be in the VDD range (8V to 24V).

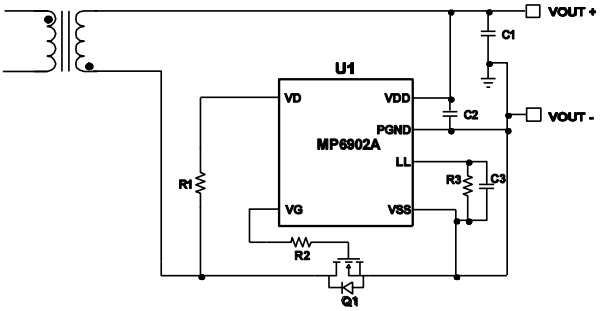



**Figure 8: IC Supply Derived Directly from the Output Voltage**

If the output voltage is out of the VDD range, or if high-side rectification is used, it is recommended to use an auxiliary winding from the power transformer for the IC supply (see Figure 9 and Figure 10).

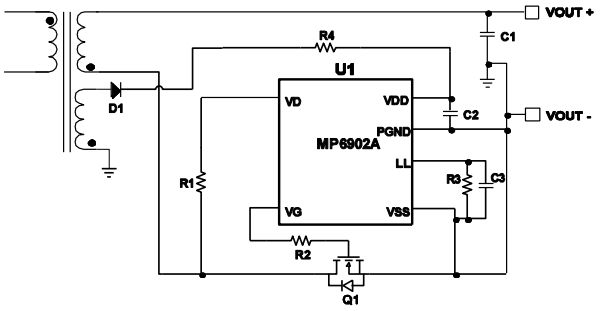



**Figure 9: IC Supply Derived from Auxiliary Winding in Low-Side Rectification**

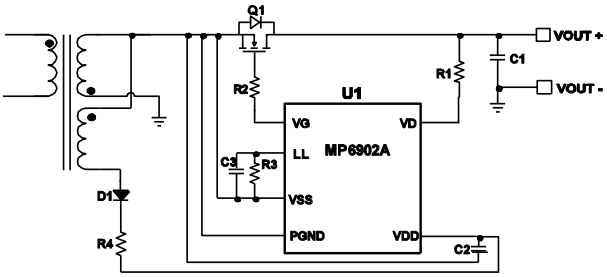



**Figure 10: IC Supply Derived from Auxiliary Winding in High-Side Rectification**

There is another non-auxiliary winding solution for the IC supply that uses an external LDO circuit from the secondary transformer winding. Compared with using auxiliary winding for IC supply, this solution has a higher power loss, which is dissipated on the LDO circuit, especially when the secondary winding voltage is high (see Figure 11 and Figure 12).

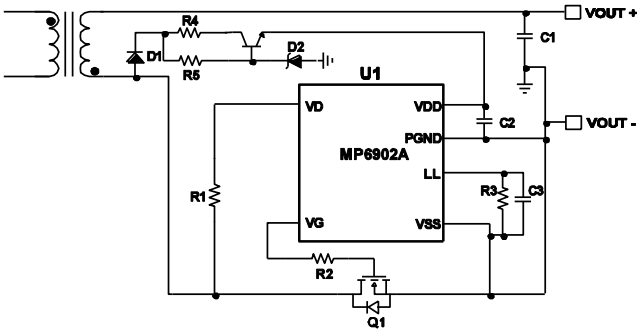



**Figure 11: IC Supply Derived from Secondary Winding through External LDO in Low-Side Rectification**

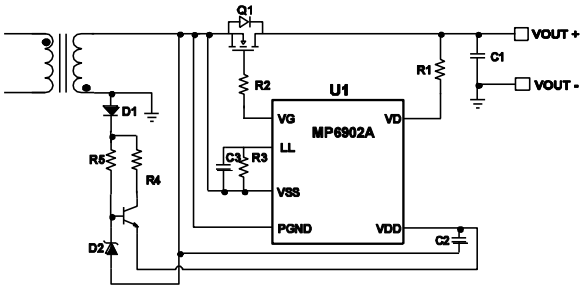



**Figure 12: IC Supply Derived from Secondary Winding through External LDO in High-Side Rectification**

## TYPICAL APPLICATION CIRCUIT

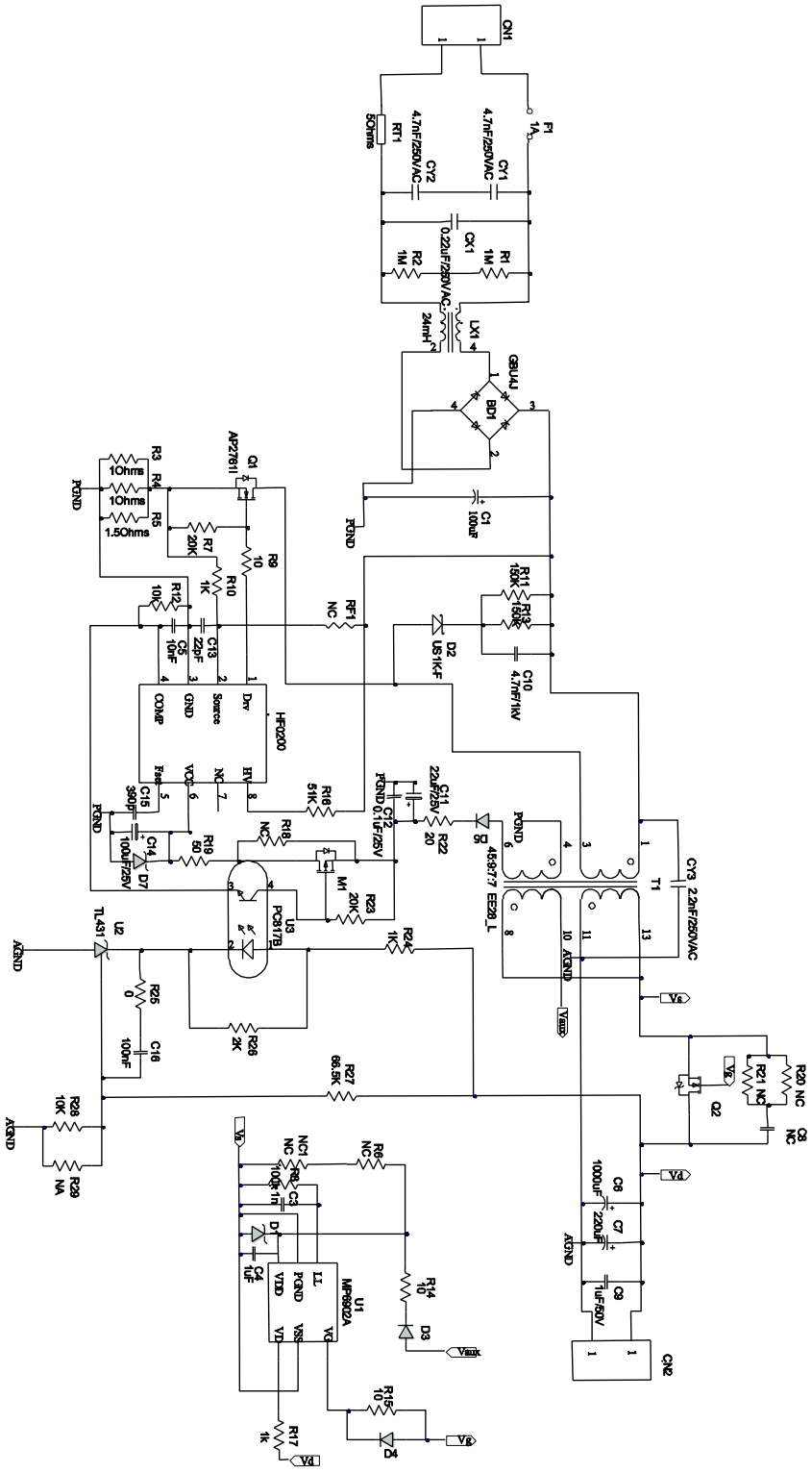
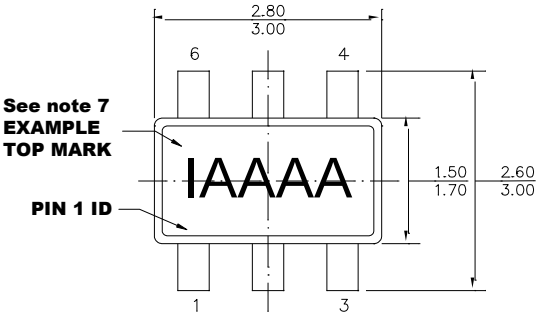


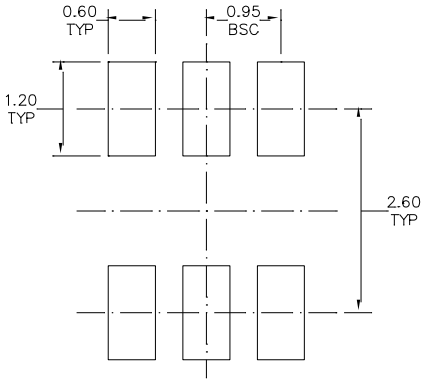

**Figure 13: MP6902A for Secondary Synchronous Controller in 90W Flyback Application**

# PACKAGE INFORMATION

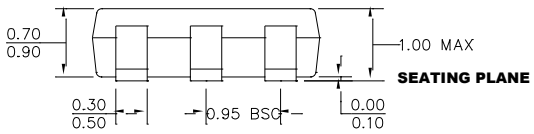
## TSOT23-6



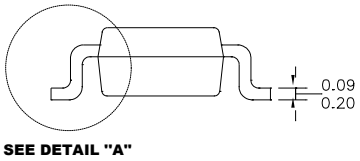

**TOP VIEW**



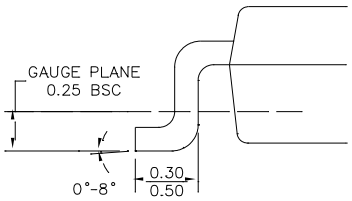

**RECOMMENDED LAND PATTERN**




**FRONT VIEW**




**SIDE VIEW**




**DETAIL "A"**

## NOTE:

**1) ALL DIMENSIONS ARE IN MILLIMETERS.**
**2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.**
**3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.**
**4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.**
**5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.**
**6) DRAWING IS NOT TO SCALE.**
**7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)**