MITSUBISHI SEMICONDUCTOR <GaAs FET>

# MGF1802



FOR MICROWAVE POWER AMPLIFIERS

## DESCRIPTION

The MGF1802, high-power GaAs FET with an N-channel Schottky gate, is designed for use in C- to X-band amplifiers. The hermetically sealed metal-ceramic package assures minimum parasitic losses and has a configuration suitable for microstrip circuits.

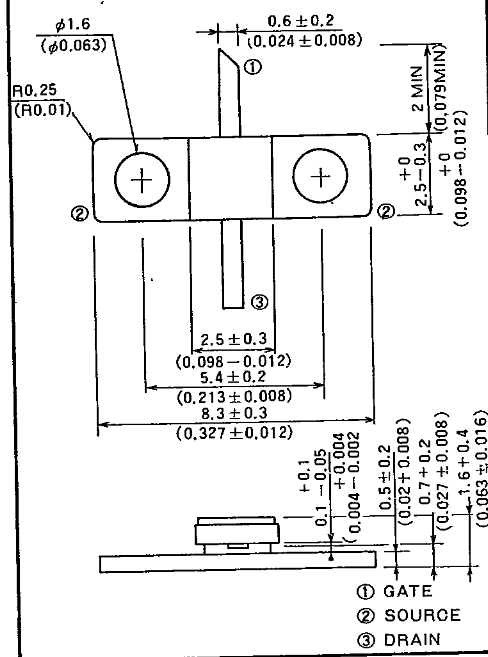
## FEATURES

- High output power
  $P_{1dB}$ = 150 mW (TYP.) @f = 12 GHz
- High linear power gain
  $G_{LP}$ = 7.0 dB (TYP.) @f = 12 GHz
- High power added efficiency
  $\eta_{add}$ = 20% (TYP.) @f = 12 GHz, $P_{1dB}$

## QUALITY GRADE

- IG, IGX, IGV, HRG

## OUTLINE DRAWING Unit: millimeters (inches)




## ABSOLUTE MAXIMUM RATINGS ($T_a$=25°C)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{GDO}$ | Gate to drain voltage | −8 | V |
| $V_{GSO}$ | Gate to source voltage | −8 | V |
| $I_D$ | Drain current | 250 | mA |
| $I_{GR}$ | Reverse gate current | −0.6 | mA |
| $I_{GF}$ | Forward gate current | 1.5 | mA |
| $P_T$ | Total power dissipation | 1.8 | W |
| Tch | Channel temperature | 175 | °C |
| Tstg | Storage temperature | −55～+175 | °C |
| Rth(ch-c) | Thermal resistance | 83 | °C/W |

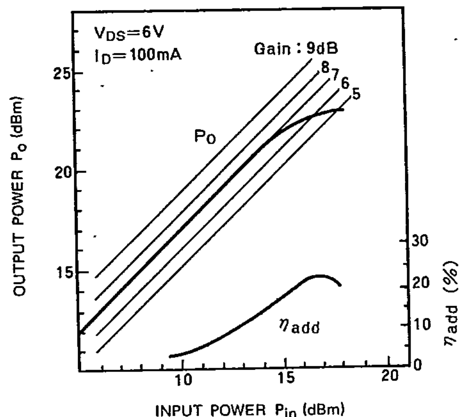
## ELECTRICAL CHARACTERISTICS ($T_a$=25°C)

| Symbol | Paramter | Conditions | Limits Min | Limits Typ | Limits Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DSS}$ | Saturated drain current | $V_{DS}$=3V, $V_{GS}$=0V | 150 | 200 | 250 | mA |
| $V_{GS(off)}$ | Gate to source cut-off voltage | $V_{DS}$=3V, $I_D$=1mA | −1.5 | | −4.5 | V |
| gm | Transconductance | $V_{DS}$=3V, $I_D$=100mA | 70 | 90 | | mS |
| $P_{1dB}$ | Output power at 1 dB gain compression | $V_{DS}$=6V, $I_D$=100mA, f=12GHz | 130 | 150 | | mW |
| $G_{LP}$ | Linear power gain | $V_{DS}$=6V, $I_D$=100mA, f=12GHz | 6 | 7 | | dB |
| $\eta_{add}$ | Power added efficiency | $V_{DS}$=6V, $I_D$=100mA, f=12GHz | | 20 | | % |

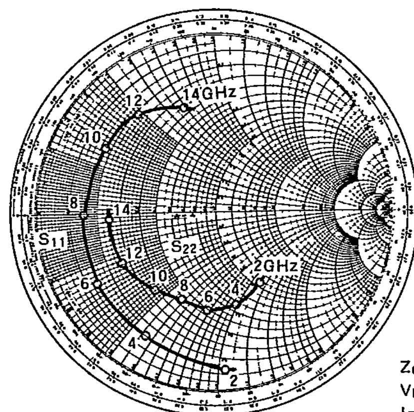
T-31-25

## TYPICAL CHARACTERISTICS (Ta=25°C)

$P_o$, $\eta_{add}$ vs. $P_{in}$
(f = 12 GHz)

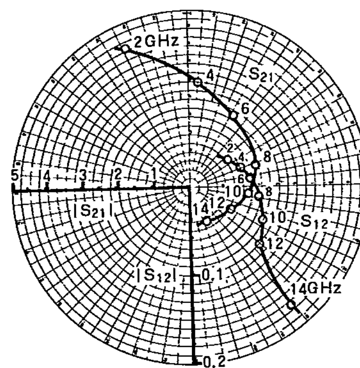



$S_{11}$, $S_{22}$ vs. f




Z0=50Ω
VDS=6V
ID=100mA

$S_{12}$, $S_{21}$ vs. f




Z0=50Ω
VDS=6V
ID=100mA

## S PARAMETERS (Ta=25°C, VDS=6V, ID=100mA)

| f (GHz) | S Parameters (TYP.) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | $S_{11}$ | | $S_{12}$ | | $S_{21}$ | | $S_{22}$ | |
| | Magn. | Angle (deg.) | Magn. | Angle (deg.) | Magn. | Angle (deg.) | Mag. | Angle (deg.) |
| 2 | 0.88 | −86 | 0.044 | 40 | 4.3 | 113.5 | 0.5 | −52 |
| 4 | 0.78 | −119 | 0.056 | 22 | 3.0 | 84.5 | 0.51 | −70 |
| 6 | 0.75 | −149 | 0.06 | 5.5 | 2.3 | 58.0 | 0.515 | −89 |
| 8 | 0.73 | 179.5 | 0.072 | −10.5 | 1.8 | 19.5 | 0.53 | −109 |
| 10 | 0.71 | 149 | 0.08 | −25 | 1.45 | −8.0 | 0.545 | −128 |
| 12 | 0.69 | 129 | 0.104 | −40.5 | 1.25 | −28.0 | 0.58 | −150 |
| 14 | 0.6 | 104 | 0.175 | −52 | 1.0 | −59.5 | 0.6 | −178 |

T-31-25

## HANDLING PRECAUTIONS FOR GaAs FETs

**1. Check of Electrical Characteristics**

(1) Measurement of DC Characteristics by Curve Tracer
Many curve tracers, if not properly grounded, exhibit a high leakage current from the high-voltage transformer, which can be a prime cause of failure or degradation of the FET. Measurement of the DC characteristics using a curve tracer is therefore not recommended. However, when tests using a curve tracer are required, first of all, check that the curve tracer is grounded to earth.
(2) Measurement of RF Characteristics
Before measurement, check that the measuring instruments are grounded to earth. Many instruments to measure RF characteristics such as RF power meters, network analyzers and so on, if not properly grounded to earth, sometimes allow a high AC leakage of up to 20 or more volts, which can be a cause of failure or degradation of the FET.

**2. Installation of GaAs FET**

When GaAs FET is soldered on a microstrip circuit, the following should be attended to,
(1) Properly ground the soldering iron to earth.
Leakage current from the soldering iron could cause failure or degradation of the FET.
(2) Solder the FET as promptly as possible at a low temperature. For a criterion, soldering in less than 8 seconds at a temperature of less than 250°C is recommended for each soldering process.

**3. Bias Procedure and Conditions**

When GaAs FET is biased, the following procedure is recommended.
(1) Slowly adjust the gate to source voltage, $V_{GS}$, to about $-1V$.
(2) Gradually increase the drain to source voltage, $V_{DS}$, from zero to a desired value.
(3) Adjust the drain current, $I_D$, to the desired value by controlling the gate to source voltage, $V_{GS}$.
When bias is released, the reverse procedure is recommended.
Be careful that the FET is not operated under conditions exceeding the absolute maximum ratings.

**4. Guaranteed Characteristics**

All the graphic characteristics illustrated in this catalog are typical examples. The characteristics of individual devices as specified in the tables of absolute maximum ratings and electrical characteristics are guaranteed under the specified conditions.