**M5M44C256P, J, L-10, -12, -15**

T-46-23-17

FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM**DESCRIPTION**

This is a family of 262144-word by 4-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

In addition to the RAS-only refresh mode, the hidden refresh mode and CAS before RAS refresh mode are available.

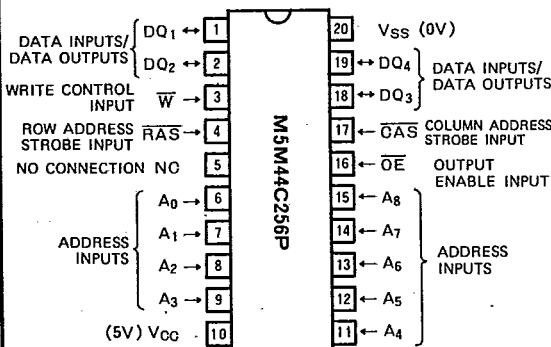
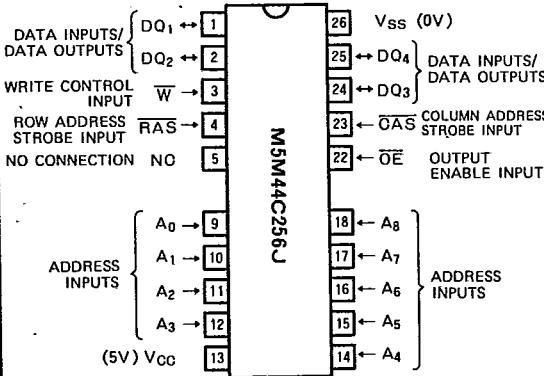
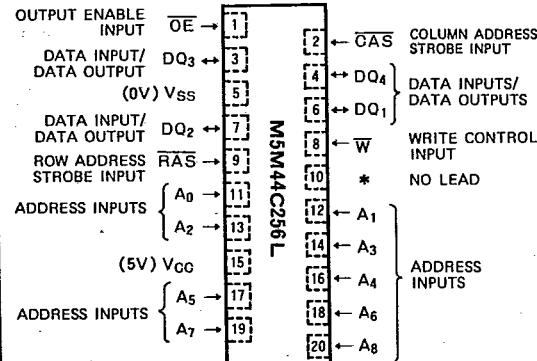
FEATURES

Type name	RAS access time (max. ns)	CAS access time (max. ns)	Address access time (max. ns)	OE access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ.mW)
P M5M44C256J-10 L	100	25	50	25	190	300
P M5M44C256J-12 L	120	30	55	30	220	250
P M5M44C256J-15 L	150	40	70	40	260	200

- High performance CMOS technology
- Standard 20 pin DIP, 26 pin SOJ, 20 pin ZIP
- Single 5V±10% supply
- Low standby power dissipation 5.5mW (Max) CMOS Input level
- Low operating power dissipation M5M44C256P, J, L-10 413mW (Max)
M5M44C256P, J, L-12 358mW (Max)
M5M44C256P, J, L-15 303mW (Max)
- All inputs, outputs TTL compatible and low capacitance
- Tri-state unlatched output
- 512 refresh cycles/8ms
- Early write mode and OE control output buffer impedance
- Read-Modify-write, RAS-only refresh, Fast-page mode capabilities
- CAS before RAS refresh mode capability
- CAS controlled output allows hidden refresh
- Wide RAS pulse width for Fast page mode . . . 50μs max

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)**Outline 20P4Y (DIP)****Outline 26P0J (SOJ)****Outline 20P5L (ZIP)**

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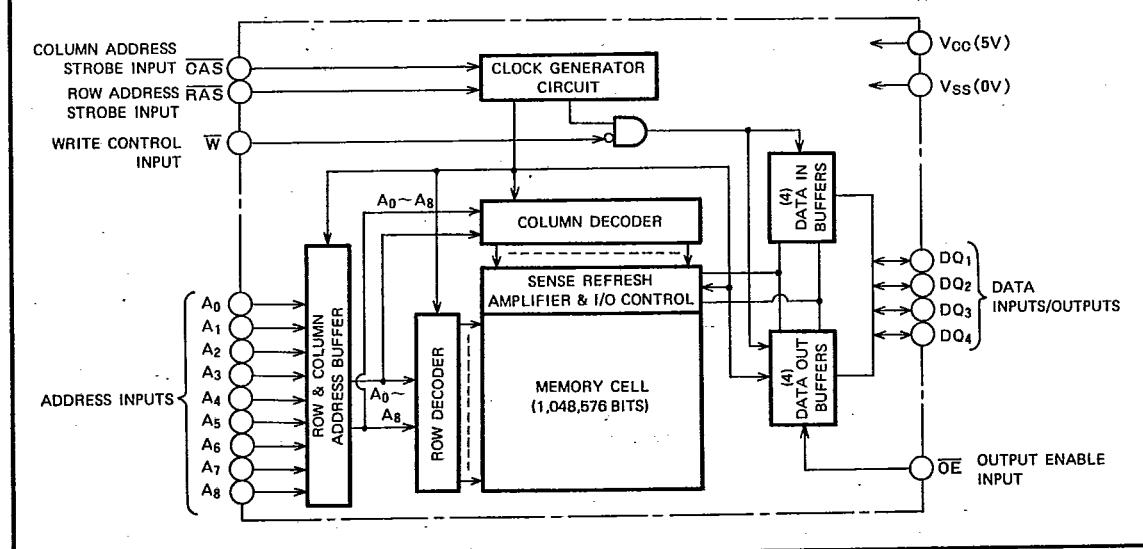
FUNCTION

The M5M44C256P, J, L provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, RAS-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	RAS	CAS	W	OE	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Read-Modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
RAS-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
CAS before RAS refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open

BLOCK DIAGRAM

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{DD}	Supply voltage	With respect to V _{SS}	-1~7	V
V _I	Input voltage		-1~7	V
V _O	Output voltage		-1~7	V
I _O	Output current		50	mA
P _D	Power dissipation	T _A =25°C	1000	mW
T _{OPR}	Operating temperature		0~70	°C
T _{STG}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (T_A=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.4		6.5	V
V _{IL}	Low-level input voltage, all inputs	-2.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.**ELECTRICAL CHARACTERISTICS (T_A=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)**

Symbol	Parameter	Test conditions			Limits	Unit
		Min	Typ	Max		
V _{OH}	High-level output voltage	I _{OH} =-2mA	2.4		V _{CC}	V
V _{OL}	Low-level output voltage	I _{OL} =4.2mA	0		0.4	V
I _{OZ}	Off-state output current	Q floating 0V≤V _{OUT} ≤5.5V	-10		10	μA
I _I	Input current	0V≤V _{IN} ≤6.5V, Other inputs pins = 0V	-10		10	μA
I _{CC1(AV)}	Average supply current from V _{CC} , operating (Note 3, 4)	M5M44C256-10 M5M44C256-12 M5M44C256-15	RAS, CAS cycling t _{RC} =t _{WC} = min, output open	75 65 55		mA
I _{CC2}	Supply current from V _{CC} , standby		RAS=CAS=V _{IH} , output open RAS=CAS=OE≥V _{CC} -0.5, output open	2 1		mA
I _{CC3(AV)}	Average supply current from V _{CC} , refreshing (Note 3)	M5M44C256-10 M5M44C256-12 M5M44C256-15	RAS cycling, CAS=V _{IH} t _{RC} = min, output open	75 65 55		mA
I _{CC4(AV)}	Average supply current from V _{CC} , Fast-Page-Mode (Note 3, 4)	M5M44C256-10 M5M44C256-12 M5M44C256-15	RAS=V _{IL} , CAS cycling t _{PC} = min, output open	65 55 45		mA
I _{CC6(AV)}	Average supply current from V _{CC} , CAS before RAS refresh mode (Note 3)	M5M44C256-10 M5M44C256-12 M5M44C256-15	CAS before RAS refresh cycling t _{RC} = min, output open	75 65 55		mA

Note 2: Current flowing into an IC is positive, out is negative.

3: I_{CC1(AV)}, I_{CC3(AV)} and I_{CC4(AV)} are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.4: I_{CC1(AV)} and I_{CC3(AV)} are dependent on output loading. Specified values are obtained with the output open.**CAPACITANCE (T_A=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)**

Symbol	Parameter	Test conditions			Limits	Unit
		Min	Typ	Max		
C _{I(A)}	Input capacitance, address inputs	V _I =V _{SS} f=1MHz Vi=25mVrms			6	pF
C _{I(Œ)}	Input capacitance, Œ input				7	pF
C _{I(W)}	Input capacitance, write control input				7	pF
C _{I(RAS)}	Input capacitance, RAS input				7	pF
C _{I(CAS)}	Input capacitance, CAS input				7	pF
C _{I/O}	Input/Output capacitance, data ports				7	pF

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SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70^\circ C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted) (Note 5)

Symbol	Parameter	Limits						Unit	
		M5M44C256-10		M5M44C256-12		M5M44C256-15			
		Min	Max	Min	Max	Min	Max		
t_{OAO}	Access time from \bar{CAS}	(Note 6, 7)	25	30		40		ns	
t_{RAO}	Access time from \bar{RAS}	(Note 6, 8)	100	120		150		ns	
t_{CAA}	Column Address access time	(Note 6, 9)	50	55		70		ns	
t_{OPA}	Access time from \bar{CAS} precharge	(Note 6, 10)	55	60		75		ns	
t_{OEA}	Access time from \bar{OE}	(Note 6)	25	30		40		ns	
t_{CLZ}	Output low impedance time from \bar{CAS} low	(Note 6)	5	5		5		ns	
t_{OFF}	Output disable time after \bar{CAS} high	(Note 11)	0	20	0	25	0	30	
$t_{dis(OE)}$	Output disable time after \bar{OE} high	(Note 11)	0	20	0	25	0	30	

Note 5: An initial pause of 500μs is required after power-up followed by any 8 RAS or \bar{RAS}/\bar{CAS} cycles before proper device operation is achieved.Note that \bar{RAS} may be cycled during the initial pause. And any 8 RAS or \bar{RAS}/\bar{CAS} cycles are required after prolonged periods of \bar{RAS} inactivity before proper device operation is achieved.

6: Measured with a load circuit equivalent to 2TTL loads and 100pF.

7: Assume that $t_{RCD(max)} \leq t_{RCD}$ and $t_{RAD(max)} \geq t_{RAD}$.8: Assume that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$.9: Assume that $t_{RCD} - t_{RAD} \leq t_{CAA(max)} - t_{CAC(max)}$ and $t_{RCD} \geq t_{RCD(max)}$.10: Assume that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.11: $t_{OFF(max)}$ and $t_{dis(OE)(max)}$ define the time at which the output achieves the high impedance state ($|I_{OUT}| \leq |\pm 10\mu A|$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.**TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Cycles)**($T_a = 0 \sim 70^\circ C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 12, 13)

Symbol	Parameter	Limits						Unit	
		M5M44C256-10		M5M44C256-12		M5M44C256-15			
		Min	Max	Min	Max	Min	Max		
t_{REF}	Refresh cycle time		8		8		8	ms	
t_{RP}	RAS high pulse width		80		90		100	ns	
t_{RCD}	Delay time, \bar{RAS} low to \bar{CAS} low	(Note 14)	20	75	25	90	30	110	
t_{CRP}	Delay time, \bar{CAS} high to \bar{RAS} low	(Note 15)	10		10		10	ns	
t_{CPN}	\bar{CAS} high pulse width	(Note 16)	25		30		35	ns	
t_{RAD}	Column address delay time from \bar{RAS} low	(Note 17)	15	50	20	65	25	80	
t_{ASR}	Row address setup time before \bar{RAS} low		0		0		0	ns	
t_{ASC}	Column address setup time before \bar{CAS} low	(Note 18)	0	20	0	20	0	25	
t_{RAH}	Row address hold time after \bar{RAS} low		10		15		20	ns	
t_{CAH}	Column address hold time after \bar{CAS} low or \bar{W} low		20		20		25	ns	
t_{AR}	Column address hold time after \bar{RAS} low		95		110		135	ns	
t_T	Transition time	(Note 19)	3	50	3	50	3	50	

Note 12: The timing requirements are assumed $t_T = 5ns$.13: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.14: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC} . If t_{RCD} is greater than $t_{RCD(max)}$, access time is defined as t_{CAC} and t_{CAA} as shown in notes 7, 9.15: t_{CRP} requirement is applicable for all \bar{RAS}/\bar{CAS} cycles.16: $t_{CPN(min)}$ is specified as $t_{CPN(min)} = t_{RCD(min)} + t_{CRP(min)} - t_T$ except for t_{CP} of fast page mode cycle.17: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$, access time is assumed by t_{CAA} for read cycle.18: $t_{ASC(max)}$ is specified as a reference point only of address access time.19: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

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FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

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Read and Refresh Cycles

Symbol	Parameter	Limits						Unit	
		M5M44C256-10		M5M44C256-12		M5M44C256-15			
		Min	Max	Min	Max	Min	Max		
t_{RC}	Read cycle time	190		220		260		ns	
t_{RAS}	RAS low pulse width	100	10000	120	10000	150	10000	ns	
t_{CAS}	CAS low pulse width	25	10000	30	10000	40	10000	ns	
t_{CSH}	CAS hold time after RAS low	100		120		150		ns	
t_{RSH}	RAS hold time after CAS low	25		30		40		ns	
t_{ROS}	Read Setup time before CAS low	0		0		0		ns	
t_{RCH}	Read hold time after CAS high	(Note 20)	0	0		0		ns	
t_{RRH}	Read hold time after RAS high	(Note 20)	10	10		10		ns	
t_{RAL}	Column address to RAS setup time	50		55		70		ns	
t_{RPC}	Precharge to CAS active time	0		0		0		ns	
$t_h(OLOE)$	\overline{OE} hold time after CAS low	25		30		40		ns	
$t_h(RLOE)$	\overline{OE} hold time after RAS low	100		120		150		ns	
t_{DOEL}	Delay time, Data to \overline{OE} low	0		0		0		ns	
t_{OEHD}	Delay time, \overline{OE} high to Data	20		25		30		ns	
$t_h(OEOH)$	CAS hold time after \overline{OE} low	25		30		40		ns	
$t_h(OERH)$	RAS hold time after \overline{OE} low	25		30		40		ns	

Note 20: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.**Write Cycle (Early Write and Delayed Write)**

Symbol	Parameter	Limits						Unit	
		M5M44C256-10		M5M44C256-12		M5M44C256-15			
		Min	Max	Min	Max	Min	Max		
t_{WO}	Write cycle time	190		220		260		ns	
t_{RAS}	RAS low pulse width	100	10000	120	10000	150	10000	ns	
t_{CAS}	CAS low pulse width	25	10000	30	10000	40	10000	ns	
t_{CSH}	CAS hold time after RAS low	100		120		150		ns	
t_{RSH}	RAS hold time after CAS low	25		30		40		ns	
t_{WOS}	Write setup time before CAS low	(Note 22)	-5	-5		-5		ns	
t_{WCH}	Write hold time after CAS low	20		25		30		ns	
t_{WCR}	Write hold time after RAS low	95		115		140		ns	
t_{OWL}	CAS hold time after write low	25		30		35		ns	
t_{RWL}	RAS hold time after write low	25		30		35		ns	
t_{WP}	Write pulse width	20		25		30		ns	
t_{DS}	Data setup time	0		0		0		ns	
t_{DH}	Data hold time after CAS low	20		25		30		ns	
t_{DHR}	Data hold time after RAS low	95		115		140		ns	
t_{OEHD}	Delay time, \overline{OE} high to data	20		25		30		ns	
$t_h(WOE)$	\overline{OE} hold time after write low	20		25		30		ns	

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FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

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Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit	
		M5M44C256-10		M5M44C256-12		M5M44C256-15			
		Min	Max	Min	Max	Min	Max		
t_{RWC}	Read write/read modify write cycle time (Note 21)	245		285		335		ns	
t_{RAS}	\bar{RAS} low pulse width	155	10000	185	10000	225	10000	ns	
t_{CAS}	\bar{CAS} low pulse width	80	10000	95	10000	115	10000	ns	
t_{CSH}	\bar{CAS} hold time after \bar{RAS} low	155		185		225		ns	
t_{RSH}	\bar{RAS} hold time after \bar{CAS} low	80		95		115		ns	
t_{ROS}	Read setup time before \bar{CAS} low	0		0		0		ns	
t_{CWD}	Delay time, \bar{CAS} low to write low (Note 22)	50		60		75		ns	
t_{RWD}	Delay time, \bar{RAS} low to write low (Note 22)	125		150		185		ns	
t_{CWL}	\bar{CAS} hold time after write low	25		30		35		ns	
t_{RWL}	\bar{RAS} hold time after write low	25		30		35		ns	
t_{WP}	Write pulse width	20		25		30		ns	
t_{DS}	Data setup time	0		0		0		ns	
t_{DH}	Data hold time after write low	20		25		30		ns	
t_{AWD}	Delay time, address to write low (Note 22)	75		85		105		ns	
$t_h(\bar{OLOE})$	\bar{OE} hold time after \bar{CAS} low	25		30		40		ns	
$t_h(\bar{RLOE})$	\bar{OE} hold time after \bar{RAS} low	100		120		150		ns	
t_{DOEL}	Delay time, Data to \bar{OE} low	0		0		0		ns	
t_{OEHD}	Delay time, \bar{OE} high to Data	20		25		30		ns	
$t_h(\bar{WOE})$	\bar{OE} hold time after write low	20		25		30		ns	

Note 21: t_{RWC} is specified as $t_{RWC(min)} = t_{RAC(max)} + t_{OEHD(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_{CWL}$.22: t_{WCS} , t_{CWD} , t_{RWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the DQ (at access time and until \bar{CAS} or \bar{OE} goes back to V_{IH}) is indeterminate.**Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle)**

Symbol	Parameter	Limits						Unit	
		M5M44C256-10		M5M44C256-12		M5M44C256-15			
		Min	Max	Min	Max	Min	Max		
t_{PC}	Read, Write cycle time	60		65		80		ns	
t_{RWPO}	Read write/read modify write cycle time	110		120		145		ns	
t_{RAS}	RAS low pulse width for Read, write cycle	155	50000	175	50000	220	50000	ns	
t_{CAS}	CAS low pulse width for read cycle	25	10000	30	10000	40	10000	ns	
t_{CP}	CAS high pulse width (Note 23)	15	25	15	25	20	30	ns	
t_{RSH}	RAS hold time after CAS low	25		30		40		ns	

Note 23: $t_{CP(max)}$ is specified as a reference point only. If $t_{CP(max)} \leq t_{CP}$, access time is assumed by t_{CAC} .**CAS before RAS Refresh Cycle (Note 24)**

Symbol	Parameter	Limits						Unit	
		M5M44C256-10		M5M44C256-12		M5M44C256-15			
		Min	Max	Min	Max	Min	Max		
t_{CSR}	CAS setup time for \bar{CAS} before \bar{RAS} refresh	10		10		10		ns	
t_{CHR}	\bar{CAS} hold time for \bar{CAS} before \bar{RAS} refresh	20		25		30		ns	
t_{RPC}	Precharge to \bar{CAS} active time	0		0		0		ns	

Note 24: Eight or more CAS before RAS cycles is necessary for proper operation of CAS before RAS refresh mode.

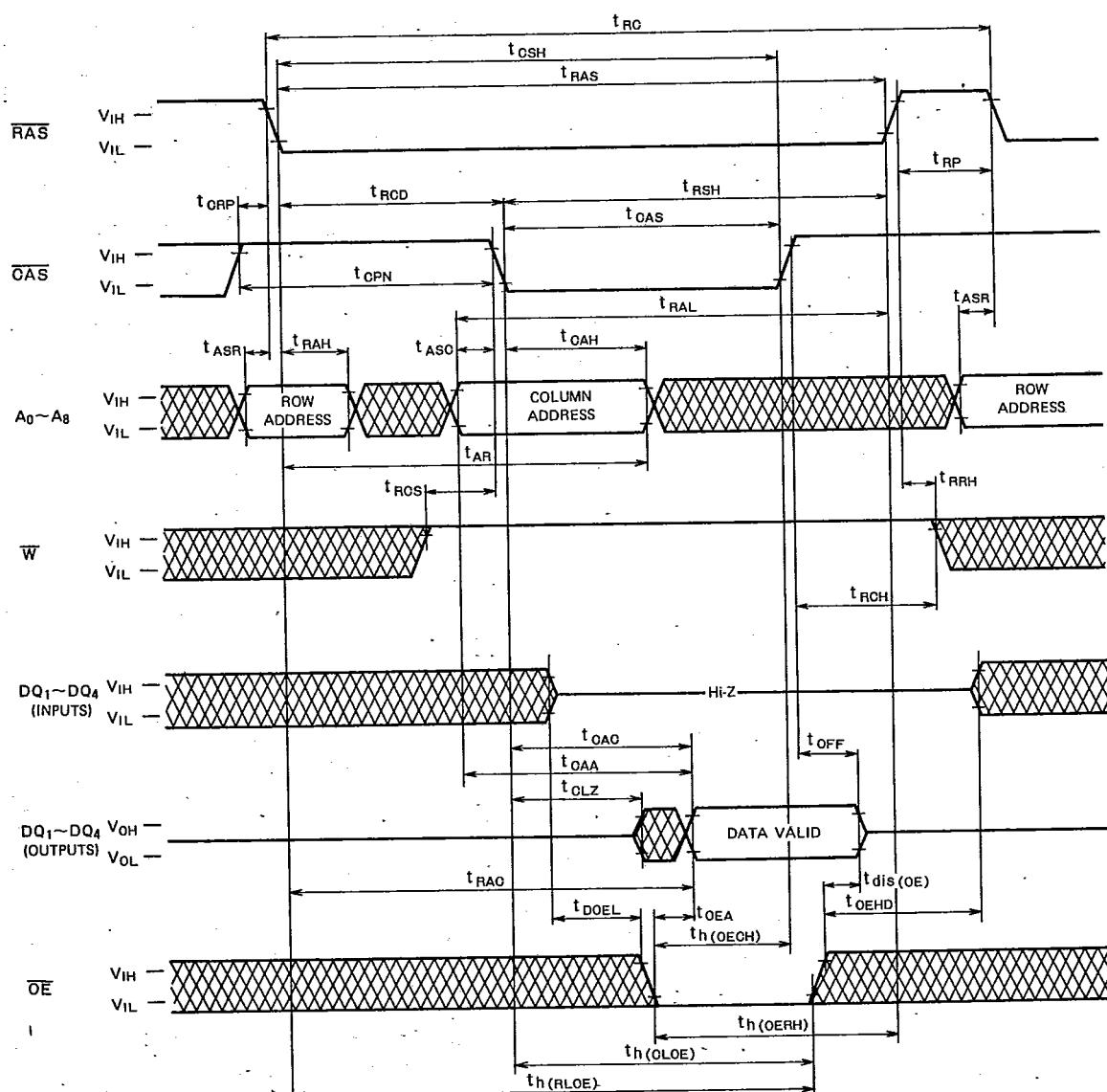
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Timing Diagrams (Note 25)**Read Cycle**

Note 25 indicates the don't care input.

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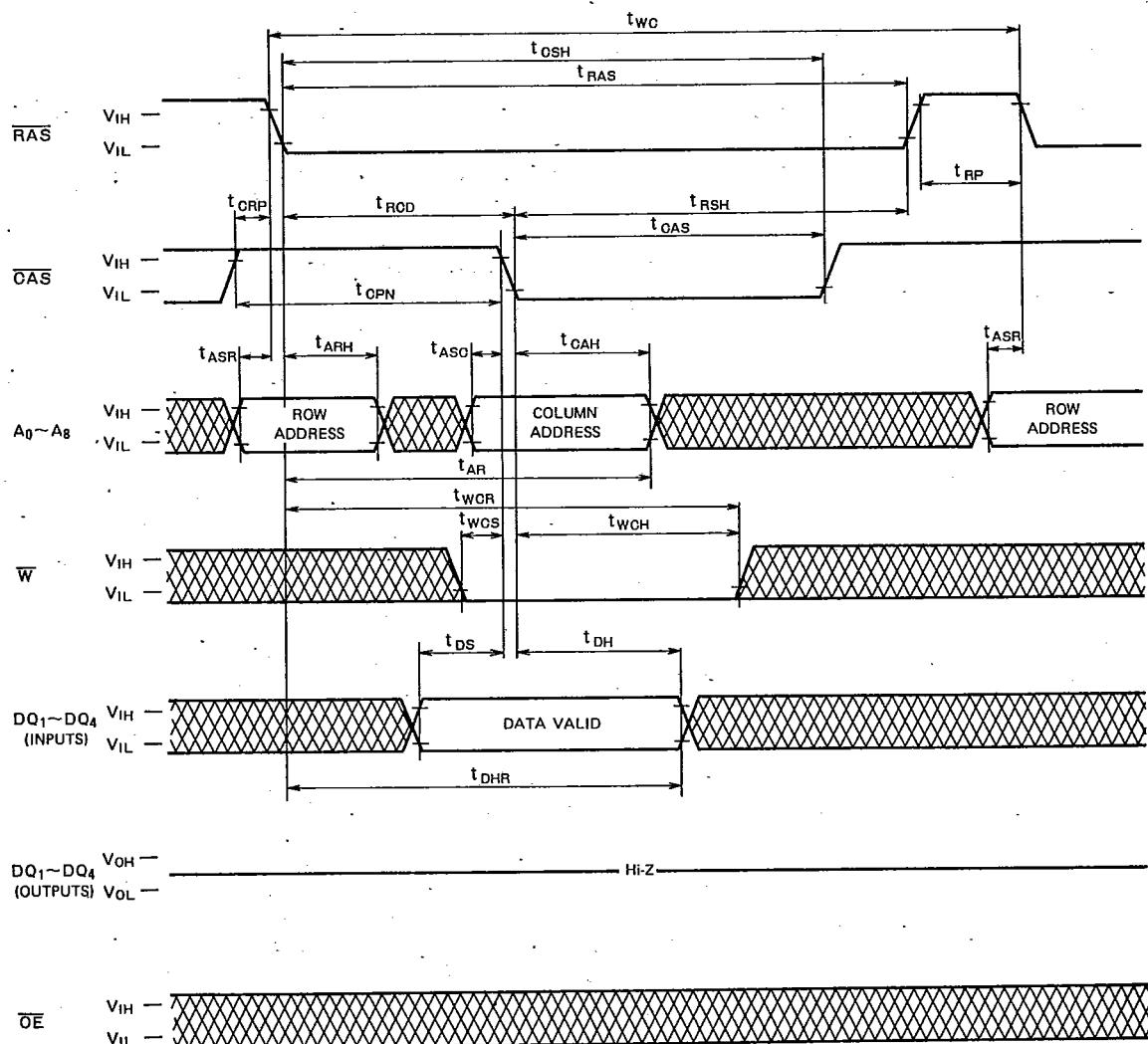
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Write Cycle (Early write)



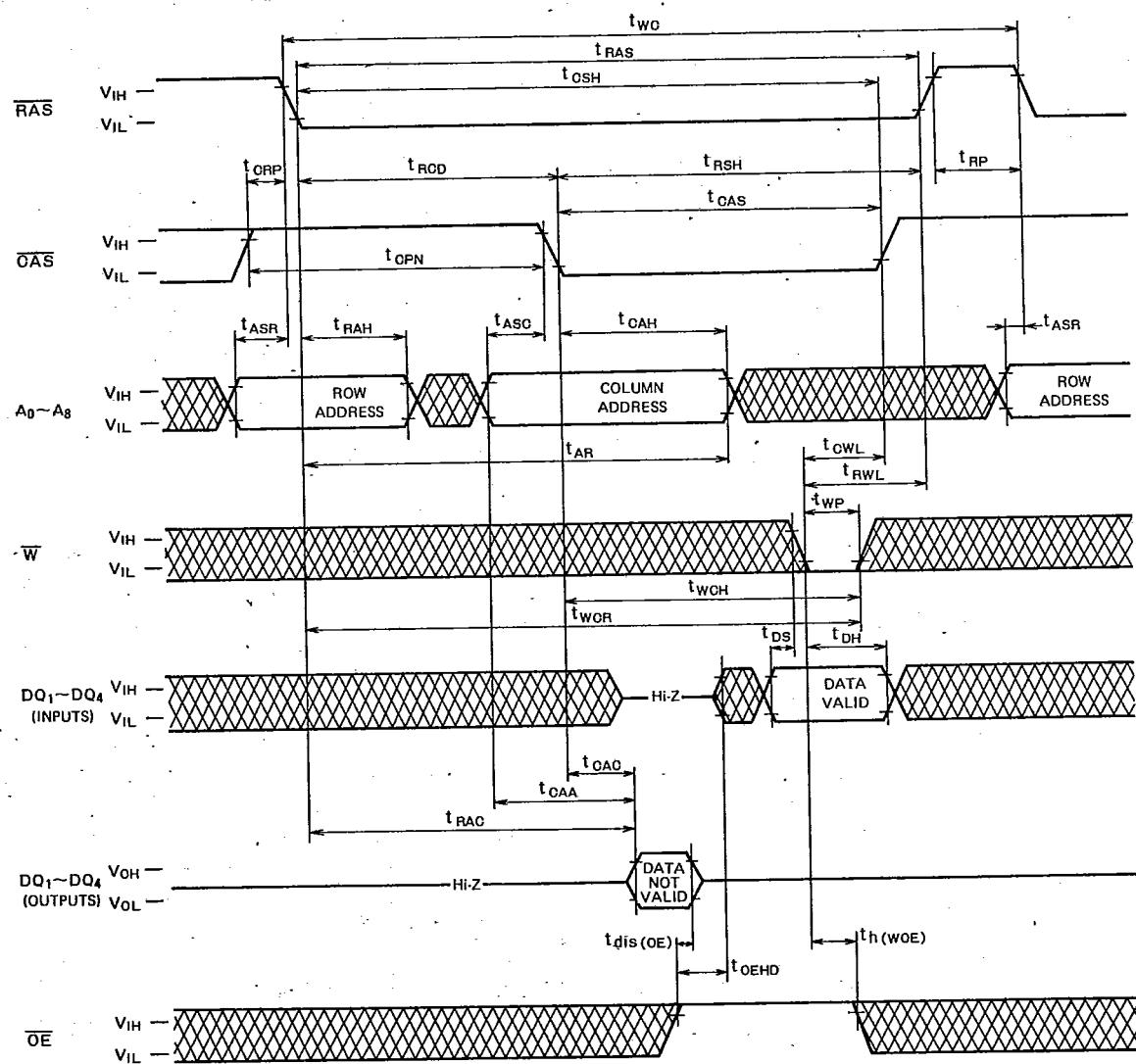
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FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

T-46-23-17

Write Cycle (Delayed Write)

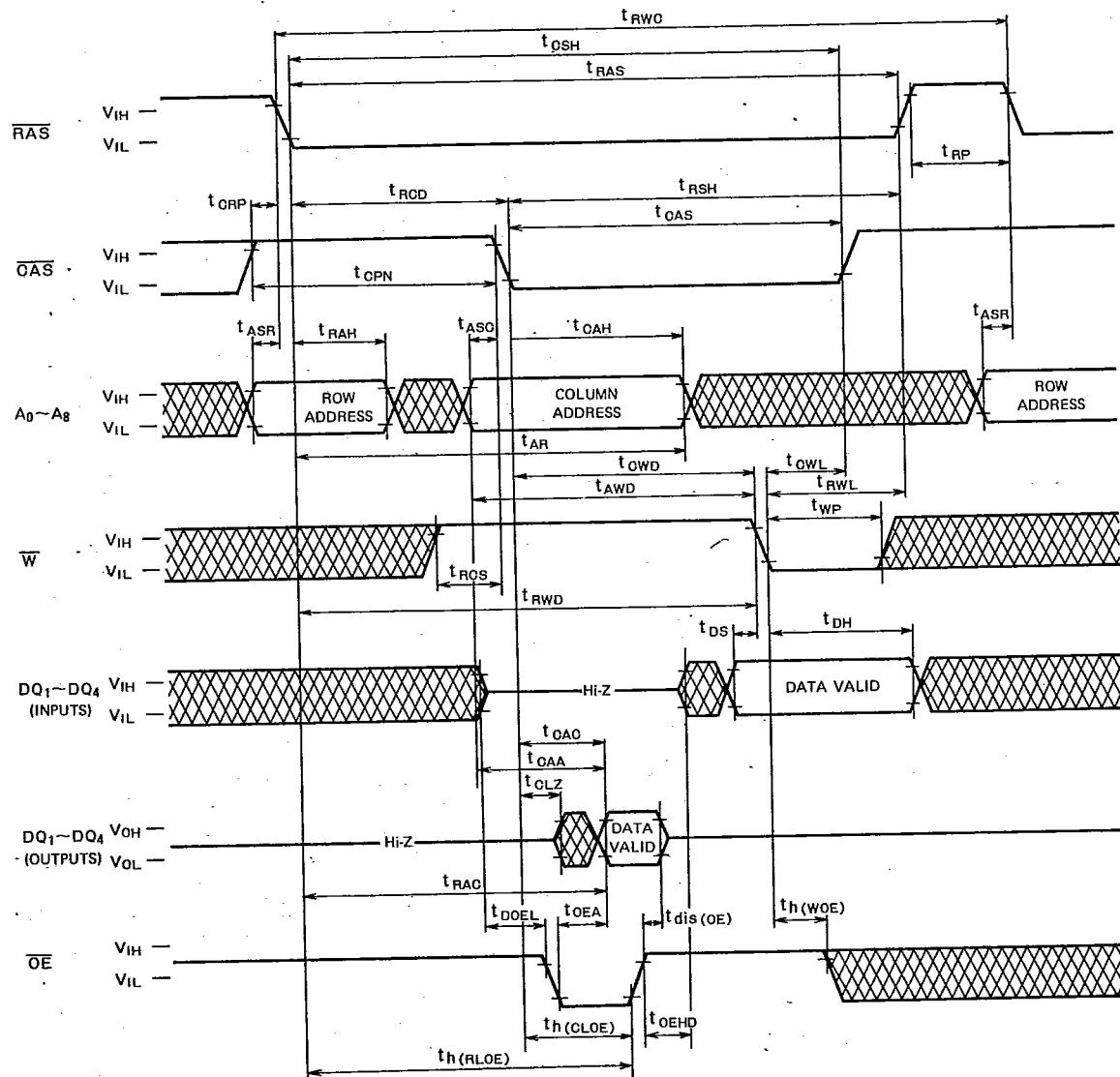
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Read-Write, Read-Modify-Write Cycle

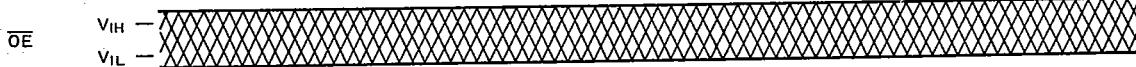
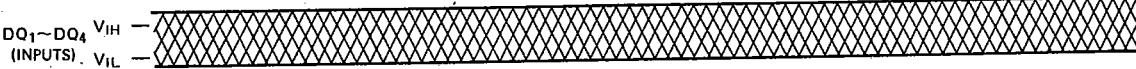
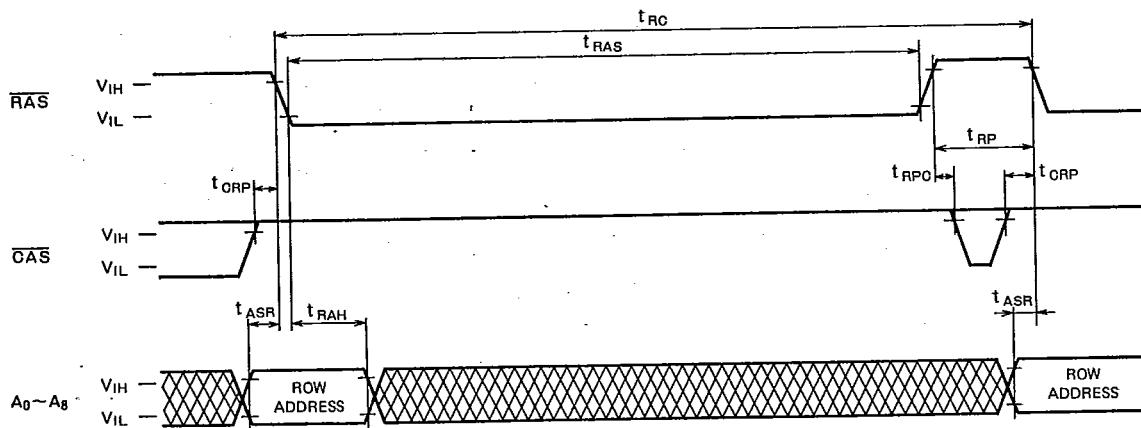
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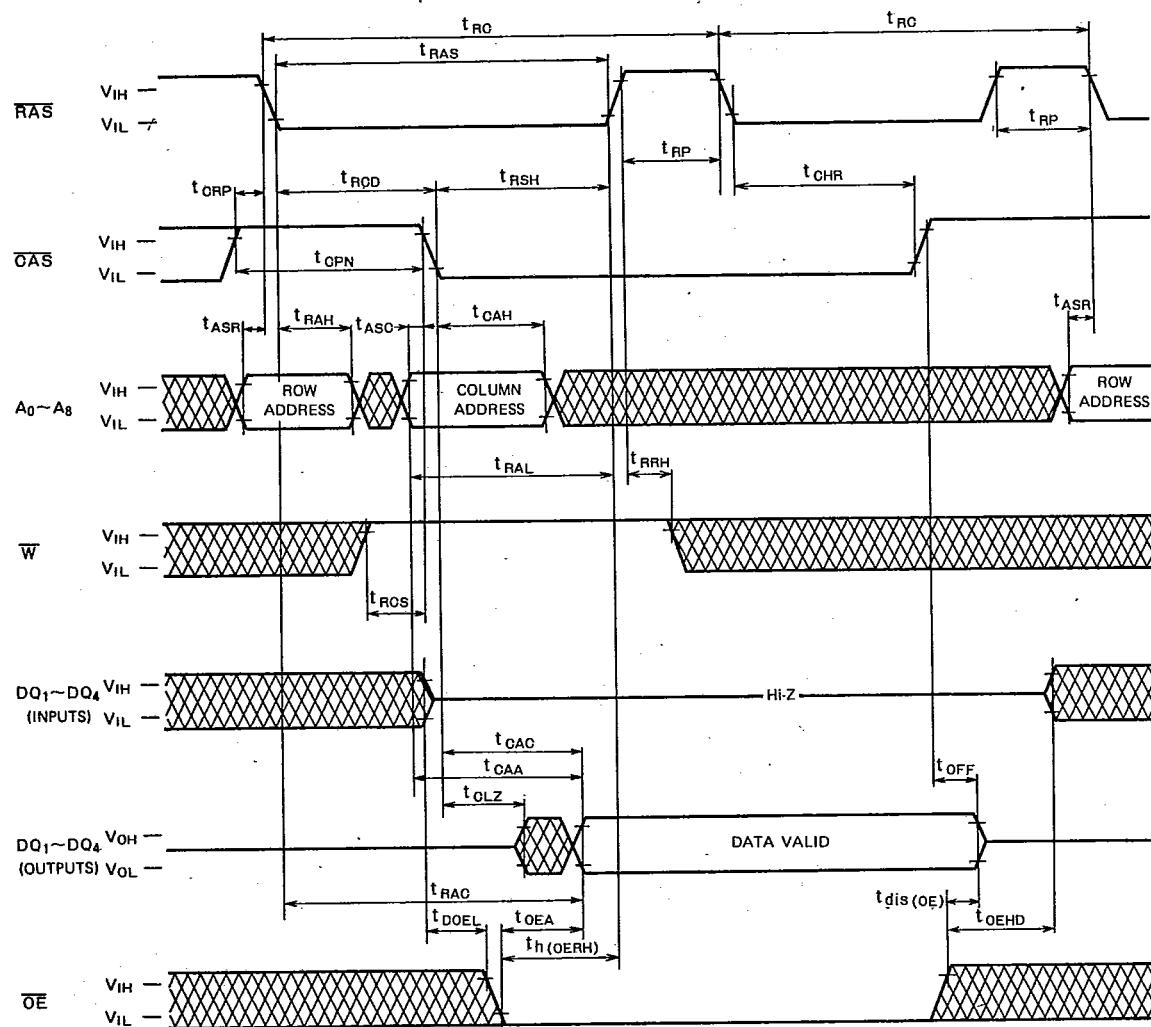
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RAS-only Refresh Cycle

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T-46-23-17

Hidden Refresh Cycle

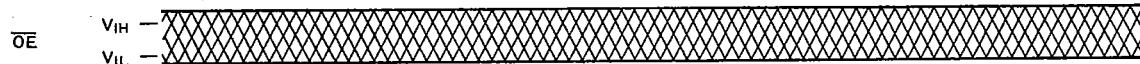
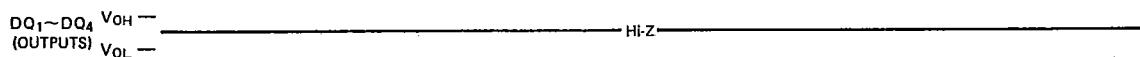
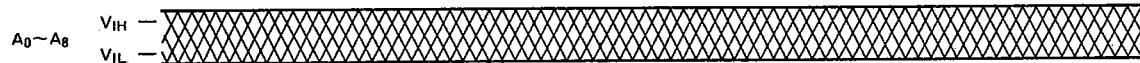
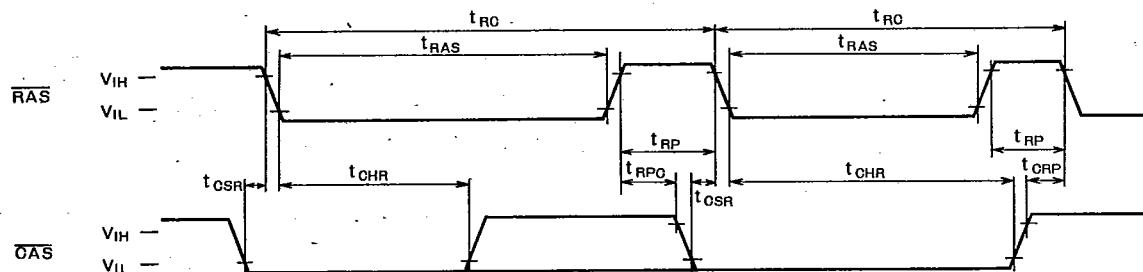
M5M44C256P, J, L-10, -12, -15

6249825 MITSUBISHI ELECTRONICS

91D 10456 D

FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

T-46-23-17

CAS before RAS Refresh Cycle

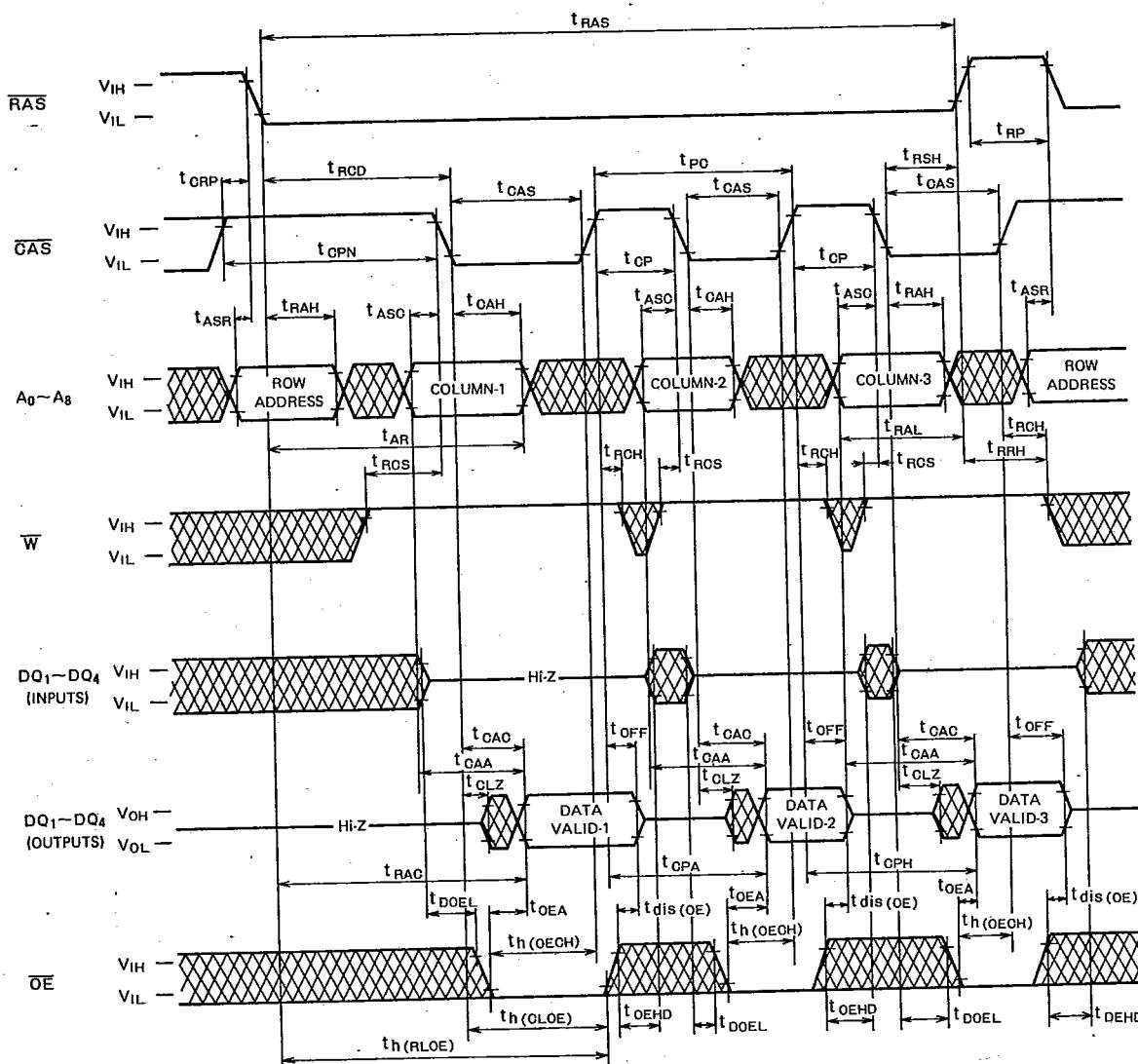
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6249825 MITSUBISHI ELECTRONICS

91D 10457 D

FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

T-46-23-17

Fast Page Mode Read Cycle

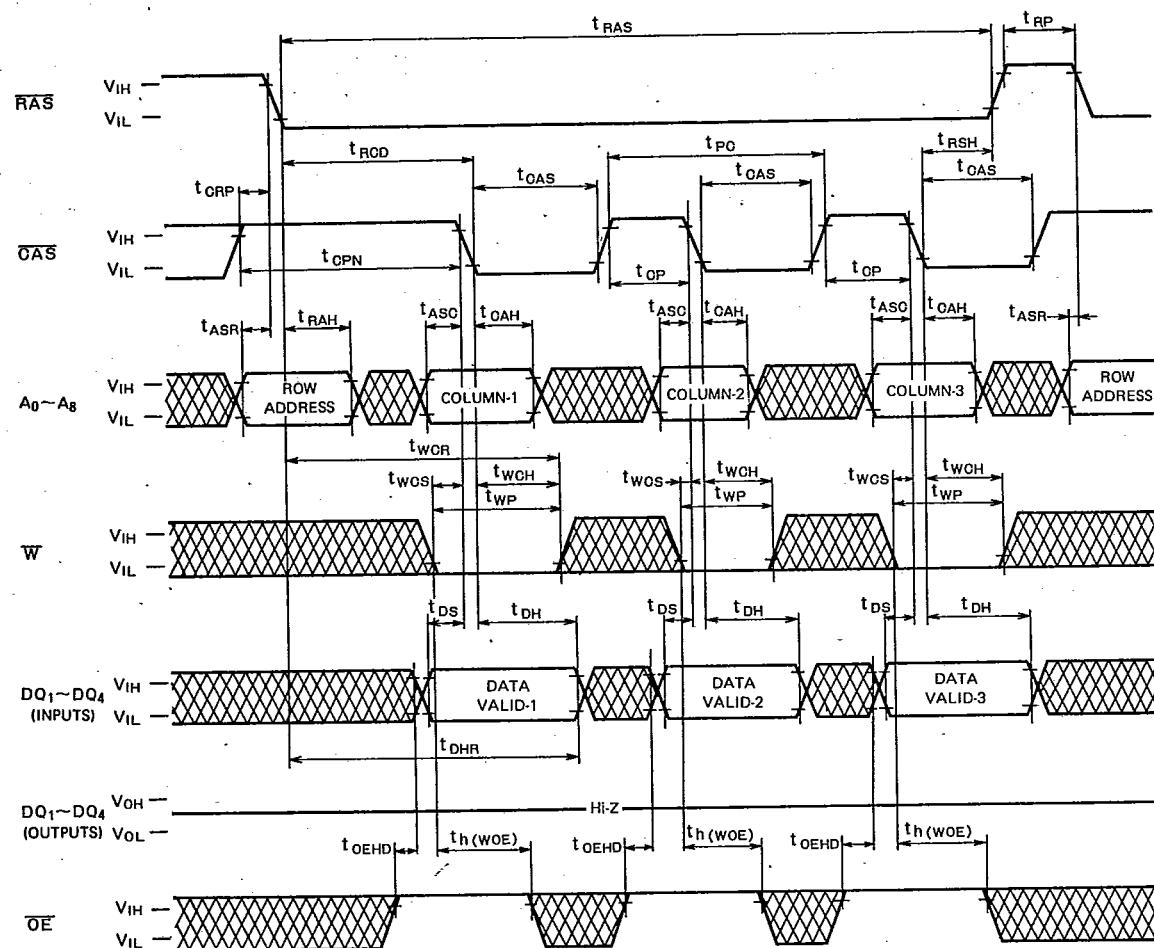
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6249825 MITSUBISHI ELECTRONICS

91D 10458 D

FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

T-46-23-17

Fast Page Mode Write Cycle

FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

T-46-23-17

Fast Page Mode Read-Write, Read-Modify-Write Cycle