gDDR3 SDRAM Graphics Addendum

MT41J256M16 – 32 Meg x 16 x 8 Banks

Features

- $V_{DD} = V_{DDQ}$ = +1.5V (1.425–1.575V)
- $V_{DD} = V_{DDQ}$ = +1.35V (1.283–1.45V) capable at down clocked speeds
- Differential bidirectional data strobe
- 8*n*-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS READ latency (CL)
- Posted CAS additive latency (AL): 0, CL - 1, CL - 2
- Programmable CAS WRITE latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of 0°C to 95°C
  - 64ms, 8192 cycle refresh at 0°C to 85°C
  - 32ms at 85°C to 115°C
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Write leveling
- Multipurpose register
- Output driver calibration

Options	Marking
• Configuration	
– 256 Meg x 16	256M16
• FBGA package (Pb-free) – x16	
– 96-ball (9mm x 14mm) Rev. E	HA
• Timing – cycle time	
– 1.0ns @ CL = 14 (gDDR3-2000)	-093G
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ 95°C)	None
• Revision	:E

Note: 1. For complete device functionality and specifications, refer to the standard 4Gb DDR3 SDRAM data sheet found at www.micron.com. The information in this data sheet supersedes the standard data sheet.

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-093G[1]	2000	14-14-14	14	14	14
-107G[2]	1800	13-13-13	14.3	14.3	14.3
-125G[2]	1600	11-11-11	13.75	13.75	13.75

Notes: 1. Requires $V_{DD} = V_{DDQ}$ = +1.5V_{NOM}
2. $V_{DD} = V_{DDQ}$ = +1.35V_{NOM} capable

Table 2: Addressing

Parameter	256 Meg x 16
Configuration	32 Meg x 16 x 8 banks
Refresh count	8K
Row addressing	32K (A[14:0])
Bank addressing	8 (BA[2:0])
Column addressing	1K (A[9:0])

Table 3: Part Number Cross Reference

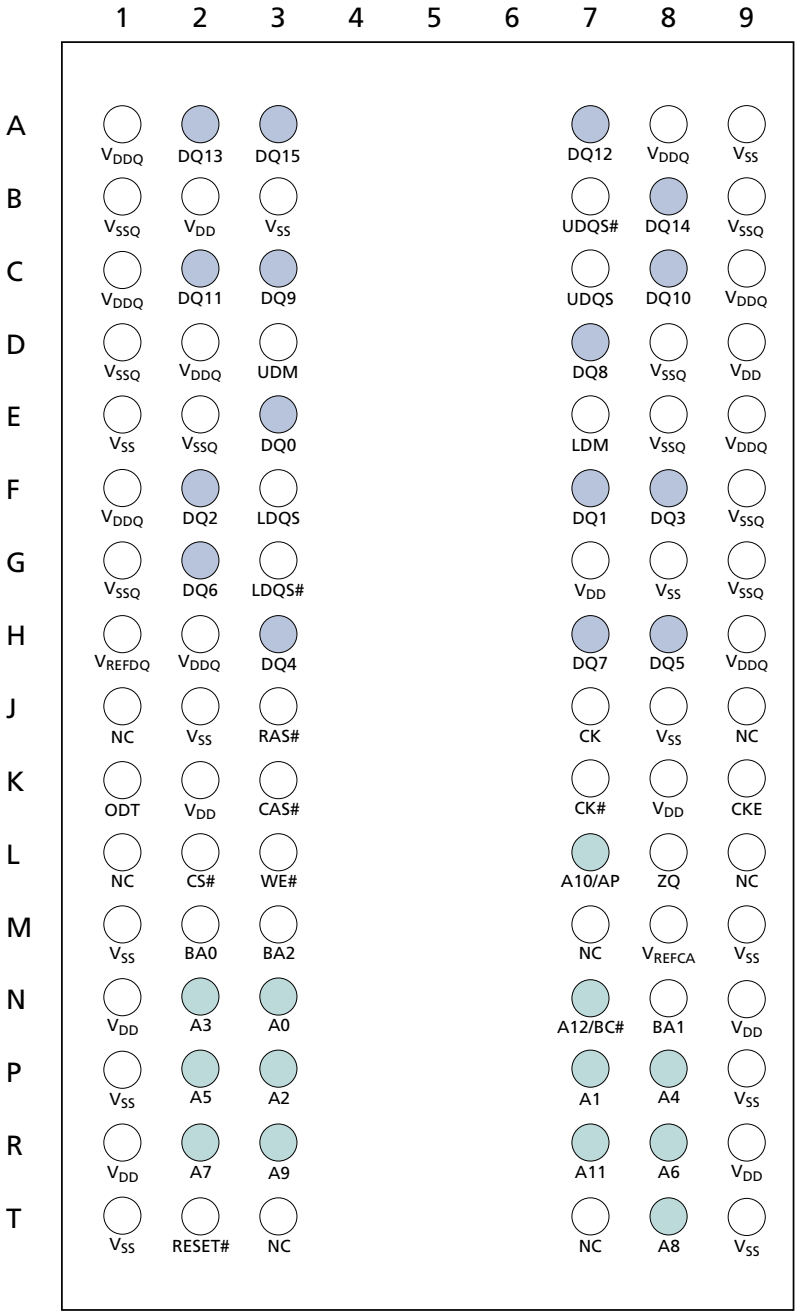
Micron Part Number	FBGA Code
MT41J256M16HA-093G:E	D9PZM

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

Ball Assignments

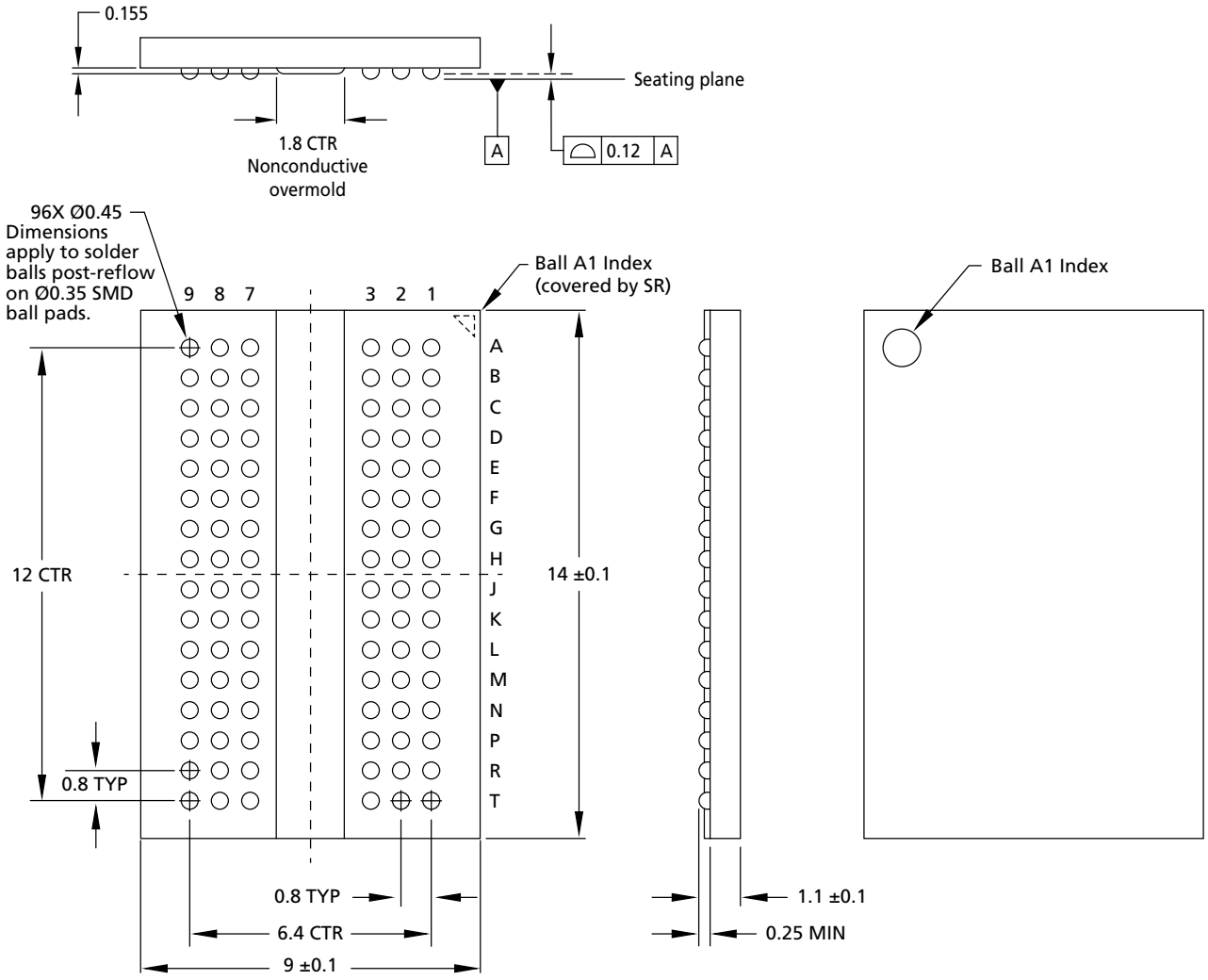
Figure 1: 96-Ball FBGA – x16 (Top View)



Notes:
1. Ball descriptions are listed in the main 4Gb DDR3 data sheet.
2. A comma separates the configuration; a slash defines a selectable function. Example D7 = NF, NF/TDQS# is selectable between NF or TDQS# via MRS.

Package Dimensions

Figure 2: 96-Ball FBGA – x16 (HA)



Note: 1. All dimensions are in millimeters.

Electrical Specifications

Table 4: DC Electrical Characteristics and Operating Conditions

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Unit	Notes
Supply voltage	V_{DD}	1.425	1.5	1.575	V	1, 2, 3
I/O supply voltage	V_{DDQ}	1.425	1.5	1.575	V	1, 2, 3
Supply voltage	V_{DD}	1.283	1.35	1.45	V	1, 2, 4
I/O supply voltage	V_{DDQ}	1.283	1.35	1.45	V	1, 2, 4

Notes:
1. V_{DD} and V_{DDQ} must track one another. V_{DDQ} must be ≤ V_{DD}. $V_{SS} = V_{SSQ}$.
2. V_{DD} and V_{DDQ} may include AC noise of ±50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. V_{DD} and V_{DDQ} must be at same level for valid AC timing parameters.
3. Valid with all speed bins.
4. Not for use with -093 speed bin.

Table 5: Input/Output Capacitance

Note 1 applies to the entire table

Capacitance Parameters	Symbol	gDDR3-1600		gDDR3-1800		gDDR3-2000		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CK and CK#	C_{CK}	0.8	1.4	0.8	1.3	0.8	1.3	pF	
ΔC: CK to CK#	C_{DCK}	0	0.15	0	0.15	0	0.15	pF	
Single-end I/O: DQ, DM	C_{IO}	1.5	2.3	1.5	2.2	1.5	2.1	pF	2
Differential I/O: DQS, DQS#, TDQS, TDQS#	C_{IO}	1.5	2.3	1.5	2.2	1.5	2.1	pF	3
ΔC: DQS to DQS#, TDQS, TDQS#	C_{DDQS}	0	0.15	0	0.15	0	0.15	pF	3
ΔC: DQ to DQS	C_{DIO}	–0.5	0.3	–0.5	0.3	–0.5	0.3	pF	4
Inputs (CTRL, CMD, ADDR)	C_I	0.75	1.3	0.75	1.2	0.75	1.2	pF	5
ΔC: CTRL to CK	C_{DI_CTRL}	–0.4	0.2	–0.4	0.2	–0.4	0.2	pF	6
ΔC: CMD_ADDR to CK	$C_{DI\_CMD\_ADDR}$	–0.4	0.4	–0.4	0.4	–0.4	0.4	pF	7
ZQ pin capacitance	C_{ZO}	–	3.0	–	3.0	–	3.0	pF	
Reset pin capacitance	C_{RE}	–	3.0	–	3.0	–	3.0	pF	

Notes:
1. V_{DD} = +1.5V ±0.075mV, $V_{DDQ} = V_{DD}$, $V_{REF} = V_{SS}$, f = 100 MHz, T_C = 25°C. $V_{OUT(DC)}$ = 0.5 × V_{DDQ}, V_{OUT} = 0.1V (peak-to-peak).
2. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
3. Includes TDQS, TDQS#. C_{DDQS} is for DQS vs. DQS# and TDQS vs. TDQS# separately.
4. $C_{DIO} = C_{IO(DQ)} - 0.5 \times (C_{IO(DQS)} + C_{IO(DQS\#)})$.
5. Excludes CK, CK#; CTRL = ODT, CS#, and CKE; CMD = RAS#, CAS#, and WE#; ADDR = A[*n*:0], BA[2:0].
6. $C_{DI\_CTRL} = C_{I(CTRL)} - 0.5 \times (C_{CK(CK)} + C_{CK(CK\#)})$.
7. $C_{DI\_CMD\_ADDR} = C_{I(CMD\_ADDR)} - 0.5 \times (C_{CK(CK)} + C_{CK(CK\#)})$.

Electrical Characteristics – I_{DD} Specifications

I_{DD} values are for full operating range of voltage and temperature unless otherwise noted.

Table 6: I_{DD} Maximum Limits - Die Rev. E

Speed Bin / I_{DD}	gDDR3-1600	gDDR3-1800	gDDR3-2000	Units	Notes
I_{DD0}	66	73	82	mA	1, 2
I_{DD1}	87	91	96	mA	1, 2
I_{DD2P0} (slow)	18	18	18	mA	1, 2
I_{DD2P1} (fast)	32	35	43	mA	1, 2
I_{DD2Q}	32	30	37	mA	1, 2
I_{DD2N}	32	35	37	mA	1, 2
I_{DD2NT}	42	45	49	mA	1, 2
I_{DD3P}	38	41	44	mA	1, 2
I_{DD3N}	47	49	52	mA	1, 2
I_{DD4R}	235	252	285	mA	1, 2
I_{DD4W}	171	190	200	mA	1, 2
I_{DD5B}	235	242	250	mA	1, 2
I_{DD6}	20	20	20	mA	1, 2, 3
I_{DD6ET}	25	25	25	mA	2, 4
I_{DD7}	243	274	305	mA	1, 2
I_{DD8}	I_{DD2P0} + 2mA	I_{DD2P0} + 2mA	I_{DD2P0} + 2mA	mA	1, 2

Notes:
1. T_C = 85°C; SRT and ASR are disabled.
2. Enabling ASR could increase I_{DDx} by up to an additional 2mA.
3. Restricted to T_C (MAX) = 85°C.
4. T_C = 85°C; ASR and ODT are disabled; SRT is enabled.
5. The I_{DD} values must be derated (increased) on IT-option devices when operated outside of the range 0°C ≤ T_C ≤ 85°C:
   - When T_C < 0°C: I_{DD2P} and I_{DD3P} must be derated by 4%; I_{DD4R} and I_{DD5W} must be derated by 2%; and I_{DD6} and I_{DD7} must be derated by 7%.
   - When T_C > 85°C: I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, I_{DD4W}, and I_{DD5W} must be derated by 2%; I_{DD2Px} must be derated by 30%.

Speed Bin Tables

Table 7: gDDR3-1600 Speed Bins

gDDR3-1600 Speed Bin			-125G			
CL-tRCD-tRP			11-11-11			
Parameter		Symbol	Min	Max	Unit	Notes
ACTIVATE to internal READ or WRITE delay time		tRCD	13.75	–	ns	
PRECHARGE command period		tRP	13.75	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		tRC	48.75	–	ns	
ACTIVATE-to-PRECHARGE command period		tRAS	35	9 x tREF	ns	1
CL = 5	CWL = 5	tCK (AVG)	3.0	3.3	ns	2
	CWL = 6, 7, 8	tCK (AVG)	Reserved		ns	3
CL = 6	CWL = 5	tCK (AVG)	2.5	3.3	ns	2
	CWL = 6, 7, 8	tCK (AVG)	Reserved		ns	3
CL = 7	CWL = 5	tCK (AVG)	Reserved		ns	3
	CWL = 6	tCK (AVG)	1.875	<2.5	ns	2
	CWL = 7, 8	tCK (AVG)	Reserved		ns	3
CL = 8	CWL = 5	tCK (AVG)	Reserved		ns	3
	CWL = 6	tCK (AVG)	1.875	<2.5	ns	2
	CWL = 7, 8	tCK (AVG)	Reserved		ns	3
CL = 9	CWL = 5, 6	tCK (AVG)	Reserved		ns	3
	CWL = 7	tCK (AVG)	1.5	<1.875	ns	2
	CWL = 8	tCK (AVG)	Reserved		ns	3
CL = 10	CWL = 5, 6	tCK (AVG)	Reserved		ns	3
	CWL = 7	tCK (AVG)	1.5	<1.875	ns	2
	CWL = 8	tCK (AVG)	Reserved		ns	3
CL = 11	CWL = 5, 6, 7	tCK (AVG)	Reserved		ns	3
	CWL = 8	tCK (AVG)	1.25	<1.5	ns	2
Supported CL settings			5, 6, 7, 8, 9, 10, 11		CK	
Supported CWL settings			5, 6, 7, 8		CK	

Notes:
1. tREFI depends on T_{OPER}.
2. The CL and CWL settings result in tCK requirements. When making a selection of tCK, both CL and CWL requirement settings need to be fulfilled.
3. Reserved settings are not allowed.

Table 8: gDDR3-1800 Speed Bins

gDDR3-1800 Speed Bin			-107G			
CL-^{t}RCD-^{t}RP			13-13-13			
Parameter		**Symbol**	**Min**	**Max**	**Unit**	**Notes**
ACTIVATE to internal READ or WRITE delay time		^{t}RCD	14.3	–	ns	
PRECHARGE command period		^{t}RP	14.3	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		^{t}RC	48.91	–	ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	35	9 x ^{t}REFI	ns	1
CL = 5	CWL = 5	^{t}CK (AVG)	3.0	3.3	ns	3
	CWL = 6, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	3
CL = 6	CWL = 5	^{t}CK (AVG)	2.5	3.3	ns	2
	CWL = 6, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	3
CL = 7	CWL = 5, 7, 8, 9	^{t}CK (AVG)	2.5	3.3	ns	3
	CWL = 6	^{t}CK (AVG)	Reserved		ns	3
CL = 8	CWL = 5, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	3
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	ns	2
CL = 9	CWL = 5, 6, 8, 9	^{t}CK (AVG)	Reserved		ns	3
	CWL = 7	^{t}CK (AVG)	1.875	<2.5	ns	3
CL = 10	CWL = 5, 6, 9	^{t}CK (AVG)	Reserved		ns	3
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	ns	2
	CWL = 8	^{t}CK (AVG)	Reserved		ns	3
CL = 11	CWL = 5, 6, 7	^{t}CK (AVG)	Reserved		ns	3
	CWL = 8	^{t}CK (AVG)	1.5	<1.875	ns	3
	CWL = 9	^{t}CK (AVG)	Reserved		ns	3
CL - 12	CWL = 5, 6, 7, 8	^{t}CK (AVG)	Reserved		ns	3
	CWL = 9	^{t}CK (AVG)	Reserved		ns	3
CL = 13	CWL = 5, 6, 7, 8	^{t}CK (AVG)	Reserved		ns	3
	CWL = 9	^{t}CK (AVG)	1.1	<1.25	ns	2
Supported CL settings			5, 6, 7, 8, 9, 10, 11, 13		CK	
Supported CWL settings			5, 6, 7, 8, 9		CK	

Notes:
1. ^{t}REFI depends on T_{OPER}.
2. The CL and CWL settings result in ^{t}CK requirements. When making a selection of ^{t}CK, both CL and CWL requirement settings need to be fulfilled.
3. Reserved settings are not allowed.

Table 9: gDDR3-2000 Speed Bins

gDDR3-2000 Speed Bin			-093G			
CL-^{t}RCD-^{t}RP			14-14-14			
Parameter		**Symbol**	**Min**	**Max**	**Unit**	**Notes**
ACTIVATE to internal READ or WRITE delay time		^{t}RCD	14	–	ns	
PRECHARGE command period		^{t}RP	14	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		^{t}RC	50	–	ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	36	9 x ^{t}REFI	ns	1
CL = 5	CWL = 5	^{t}CK (AVG)	3.0	3.3	ns	3
	CWL = 6, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	3
CL = 6	CWL = 5	^{t}CK (AVG)	2.5	3.3	ns	2
	CWL = 6, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	3
CL = 7	CWL = 5, 7, 8, 9	^{t}CK (AVG)	2.5	3.3	ns	3
	CWL = 6	^{t}CK (AVG)	Reserved		ns	3
CL = 8	CWL = 5, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	3
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	ns	2
CL = 9	CWL = 5, 6, 8, 9	^{t}CK (AVG)	Reserved		ns	3
	CWL = 7	^{t}CK (AVG)	1.875	<2.5	ns	3
CL = 10	CWL = 5, 6, 9	^{t}CK (AVG)	Reserved		ns	3
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	ns	2
	CWL = 8	^{t}CK (AVG)	Reserved		ns	3
CL = 11	CWL = 5, 6, 7	^{t}CK (AVG)	Reserved		ns	3
	CWL = 8	^{t}CK (AVG)	1.5	<1.875	ns	3
	CWL = 9	^{t}CK (AVG)	Reserved		ns	3
CL - 12	CWL = 5, 6, 7, 8	^{t}CK (AVG)	Reserved		ns	3
	CWL = 9	^{t}CK (AVG)	Reserved		ns	3
CL = 13	CWL = 5, 6, 7, 8	^{t}CK (AVG)	Reserved		ns	3
	CWL = 9	^{t}CK (AVG)	1.1	<1.25	ns	2
CL = 14	CWL = 5, 6, 7, 8, 9	^{t}CK (AVG)	1	<1.1	ns	2
	CWL = 10					
Supported CL settings			5, 6, 7, 8, 9, 10, 11, 13, 14		CK	
Supported CWL settings			5, 6, 7, 8, 9, 10		CK	

Notes:
1. ^{t}REFI depends on T_{OPER}.
2. The CL and CWL settings result in ^{t}CK requirements. When making a selection of ^{t}CK, both CL and CWL requirement settings need to be fulfilled.
3. Reserved settings are not allowed.

Electrical Characteristics and AC Operating Conditions

Table 10: Electrical Characteristics and AC Operating Conditions for Speed Extensions

Notes 1–8 apply to the entire table

Parameter		Symbol	gDDR3-1600		gDDR3-1800		gDDR3-2000		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Clock Timing										
Clock period average: DLL disable mode	T_C = 0°C to 85°C	^tCK (DLL_DIS)	8	7800	8	7800	8	7800	ns	9, 42
	T_C = >85°C to 95°C		8	3900	8	3900	8	3900	ns	42
Clock period average: DLL enable mode		^tCK (AVG)	See corresonding speed bin table for ^tCK range allowed						ns	10, 11
High pulse width average		^tCH (AVG)	0.47	0.53	0.47	0.53	0.47	0.53	CK	12
Low pulse width average		^tCL (AVG)	0.47	0.53	0.47	0.53	0.47	0.53	CK	12
Clock period jitter	DLL locked	$^tJIT_{PER}$	–80	80	–70	70	-60	60	ps	13
	DLL locking	$^tJIT_{PER}$,lck	–70	70	–60	60	-50	50	ps	13
Clock absolute period		^tCK (ABS)	MIN = ^tCK (AVG) MIN + $^tJIT_{PER}$ MIN; MAX = ^tCK (AVG) MAX + $^tJIT_{PER}$ MAX						ps	
Clock absolute high pulse width		^tCH (ABS)	0.43	–	0.43	–	0.43	–	^tCK (AVG)	14
Clock absolute low pulse width		^tCL (ABS)	0.43	–	0.43	–	0.43	–	^tCK (AVG)	15
Cycle-to-cycle jitter	DLL locked	$^tJIT_{CC}$	160		140		120		ps	16
	DLL locking	$^tJIT_{CC}$,lck	140		120		100		ps	16
Cumulative error across	2 cycles	$^tERR2_{PER}$	–118	118	–103	103	–88	88	ps	17
	3 cycles	$^tERR3_{PER}$	–140	140	–122	122	–105	105	ps	17
	4 cycles	$^tERR4_{PER}$	–155	155	–136	136	–117	117	ps	17
	5 cycles	$^tERR5_{PER}$	–168	168	–147	147	–126	126	ps	17
	6 cycles	$^tERR6_{PER}$	–177	177	–155	155	–133	133	ps	17
	7 cycles	$^tERR7_{PER}$	–186	186	–163	163	–139	139	ps	17
	8 cycles	$^tERR8_{PER}$	–193	193	–169	169	–145	145	ps	17
	9 cycles	$^tERR9_{PER}$	–200	200	–175	175	–150	150	ps	17
	10 cycles	$^tERR10_{PER}$	–205	205	–180	180	–154	154	ps	17
	11 cycles	$^tERR11_{PER}$	–210	210	–184	184	–158	158	ps	17
	12 cycles	$^tERR12_{PER}$	–215	215	–188	188	–161	161	ps	17
	n = 13, 14 . . .49, 50 cycles	$^tERRnper$	$^tERRn_{PER}$ MIN = (1 + 0.68in[*n*]) × $^tJIT_{PER}$ MIN; $^tERRn_{PER}$ MAX = (1 + 0.68in[*n*]) × $^tJIT_{PER}$ MAX						ps	17
DQ Input Timing										
Data setup time to DQS, DQS#	Base (specification)	^tDS (AC175)	–	–	–	–	–	–	ps	18, 19
	V_{REF} @ 1 V/ns		–	–	–	–	–	–	ps	19, 20

Table 10: Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	gDDR3-1600		gDDR3-1800		gDDR3-2000		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Data setup time to DQS, DQS#	Base (specification)	tDS (AC150)	30	–	10	–	–	–	ps	18, 19
	V_{REF} @ 1 V/ns		180	–	160	–	–	–	ps	19, 20
Data setup time to DQS, DQS#	Base (specification)@ 2 V/ns	tDS (AC135)	–	–	–	–	68	–	ps	19, 20
	V_{REF} @ 2 V/ns		–	–	–	–	135	–		19, 20
Data hold time from DQS, DQS#	Base (specification)	tDH (DC100)	65	–	45	–	70	–	ps	18, 19
	V_{REF} @ 1 V/ns		165	–	145	–	120	–	ps	19, 20
Minimum data pulse width		tDIPW	400	–	360	–	320	–	ps	41
DQ Output Timing										
DQS, DQS# to DQ skew, per access		tDQSQ	–	125	–	100	–	85	ps	
DQ output hold time from DQS, DQS#		tQH	0.38	–	0.38	–	0.38	–	tCK (AVG)	21
DQ Low-Z time from CK, CK#		tLZ (DQ)	–500	250	–450	225	–390	195	ps	22, 23
DQ High-Z time from CK, CK#		tHZ (DQ)	–	250	–	225	–	195	ps	22, 23
DQ Strobe Input Timing										
DQS, DQS# rising to CK, CK# rising		tDQSS	–0.25	0.25	–0.27	0.27	–0.27	0.27	CK	25
DQS, DQS# differential input low pulse width		tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	CK	
DQS, DQS# differential input high pulse width		tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	CK	
DQS, DQS# falling setup to CK, CK# rising		tDSS	0.2	–	0.18	–	0.18	–	CK	25
DQS, DQS# falling hold from CK, CK# rising		tDSH	0.2	–	0.18	–	0.18	–	CK	25
DQS, DQS# differential WRITE preamble		tWPRE	0.9	–	0.9	–	0.9	–	CK	
DQS, DQS# differential WRITE postamble		tWPST	0.3	–	0.3	–	0.3	–	CK	
DQ Strobe Output Timing										
DQS, DQS# rising to/from rising CK, CK#		tDQSCK	–255	255	–225	225	–195	195	ps	23
DQS, DQS# rising to/from rising CK, CK# when DLL is disabled		tDQSCK (DLL_DIS)	1	10	1	10	1	10	ns	26
DQS, DQS# differential output high time		tQSH	0.40	–	0.40	–	0.40	–	CK	21
DQS, DQS# differential output low time		tQSL	0.40	–	0.40	–	0.40	–	CK	21
DQS, DQS# Low-Z time (RL - 1)		tLZ (DQS)	–500	250	–450	225	–390	195	ps	22, 23
DQS, DQS# High-Z time (RL + BL/2)		tHZ (DQS)	–	250	–	225	–	195	ps	22, 23

Table 10: Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	gDDR3-1600		gDDR3-1800		gDDR3-2000		Unit	Notes
			Min	Max	Min	Max	Min	Max		
DQS, DQS# differential READ preamble		tRPRE	0.9	Note 24	0.9	Note 24	0.9	Note 24	CK	23, 24
DQS, DQS# differential READ postamble		tRPST	0.3	Note 27	0.3	Note 27	0.3	Note 27	CK	23, 27
Command and Address Timing										
DLL locking time		tDLLK	512	–	512	–	512	–	CK	28
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	tIS (AC175)	65	–	45	–	–	–	ps	29, 30
	V_{REF} @ 1 V/ns		240	–	220	–	–	–	ps	20, 30
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	tIS (AC150)	190	–	170	–	–	–	ps	29, 30
	V_{REF} @ 1 V/ns		340	–	320	–	–	–	ps	20, 30
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	tIS (AC135)	–	–	–	–	65	–	ps	
	V_{REF} @ 1 V/ns		–	–	–	–	200	–	ps	
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	tIS (AC125)	–	–	–	–	150	–	ps	
	V_{REF} @ 1 V/ns		–	–	–	–	275	–	ps	
CTRL, CMD, ADDR hold from CK,CK#	Base (specification)	tIH (DC100)	140	–	120	–	100	–	ps	29, 30
	V_{REF} @ 1 V/ns		240	–	220	–	200	–	ps	20, 30
Minimum CTRL, CMD, ADDR pulse width		tIPW	620	–	560	–	535	–	ps	41
ACTIVATE to internal READ or WRITE delay		tRCD	See corresponding speed bin table for tRCD						ns	31
PRECHARGE command period		tRP	See corresponding speed bin table for tRP						ns	31
ACTIVATE-to-PRECHARGE command period		tRAS	See corresponding speed bin table for tRAS						ns	31, 32
ACTIVATE-to-ACTIVATE command period		tRC	See corresponding speed bin table for tRC						ns	31
ACTIVATE-to-ACTIVATE minimum command period		tRRD	MIN = greater of 4CK or 7.5ns		MIN = greater of 4CK or 7.5ns		MIN = greater of 4CK or 6ns		CK	31
Four ACTIVATE windows		tFAW	45	–	40	–	35	–	ns	31
Write recovery time		tWR	15	N/A	15	N/A	15	N/A	ns	31, 32, 33
Delay from start of internal WRITE transaction to internal READ command		tWTR	MIN = greater of 4CK or 7.5ns; MAX = N/A						CK	31, 34
READ-to-PRECHARGE time		tRTP	MIN = greater of 4CK or 7.5ns; MAX = N/A						CK	31, 32

Table 10: Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	gDDR3-1600		gDDR3-1800		gDDR3-2000		Unit	Notes
			Min	Max	Min	Max	Min	Max		
CAS#-to-CAS# command delay		^{t}CCD	MIN = 4CK; MAX = N/A						CK	
Auto precharge write recovery + precharge time		^{t}DAL	MIN = WR + ^{t}RP/^{t}CK (AVG); MAX = N/A						CK	
MODE REGISTER SET command cycle time		^{t}MRD	MIN = 4CK; MAX = N/A						CK	
MODE REGISTER SET command update delay		^{t}MOD	MIN = greater of 12CK or 15ns; MAX = N/A						CK	
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		^{t}MPRR	MIN = 1CK; MAX = N/A						CK	
Calibration Timing										
ZQCL command: Long calibration time	POWER-UP and RESET operation	$^{t}ZQ_{INIT}$	512	–	512	–	512	–	CK	
	Normal operation	$^{t}ZQ_{OPER}$	256	–	256	–	256	–	CK	
ZQCS command: Short calibration time		^{t}ZQCS	64	–	64	–	64	–	CK	
Initialization and Reset Timing										
Exit reset from CKE HIGH to a valid command		^{t}XPR	MIN = greater of 5CK or ^{t}RFC + 10ns; MAX = N/A						CK	
Begin power supply ramp to power supplies stable		^{t}VDDPR	MIN = N/A; MAX = 200						ms	
RESET# LOW to power supplies stable		^{t}RPS	MIN = 0; MAX = 200						ms	
RESET# LOW to I/O and R_{TT} High-Z		^{t}IOZ	MIN = N/A; MAX = 20						ns	35
Refresh Timing										
REFRESH-to-ACTIVATE or REFRESH command period		^{t}RFC	MIN = 260; MAX = 70,200						ns	
Maximum refresh period	$T_C \leq 85°C$	–	64 (1X)						ms	36
	$T_C > 85°C$		32 (2X)						ms	36
Maximum average periodic refresh	$T_C \leq 85°C$	^{t}REFI	7.8 (64ms/8192)						µs	36
	$T_C > 85°C$		3.9 (32ms/8192)						µs	36
Self Refresh Timing										
Exit self refresh to commands not requiring a locked DLL		^{t}XS	MIN = greater of 5CK or ^{t}RFC + 10ns; MAX = N/A						CK	
Exit self refresh to commands requiring a locked DLL		^{t}XSDLL	MIN = ^{t}DLLK (MIN); MAX = N/A						CK	28
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		^{t}CKESR	MIN = ^{t}CKE (MIN) + CK; MAX = N/A						CK	
Valid clocks after self refresh entry or power-down entry		^{t}CKSRE	MIN = greater of 5CK or 10ns; MAX = N/A						CK	

Table 10: Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	gDDR3-1600		gDDR3-1800		gDDR3-2000		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Valid clocks before self refresh exit, power-down exit, or reset exit		^{t}CKSRX	MIN = greater of 5CK or 10ns; MAX = N/A						CK	
Power-Down Timing										
CKE MIN pulse width		^{t}CKE (MIN)	Greater of 3CK or 5.625ns		Greater of 3CK or 5ns		Greater of 3CK or 5ns		CK	
Command pass disable delay		^{t}CPDED	MIN = 1; MAX = N/A				MIN = 2; MAX = N/A		CK	
Power-down entry to power-down exit timing		^{t}PD	MIN = ^{t}CKE (MIN); MAX = 9 × ^{t}REFI						CK	
Begin power-down period prior to CKE registered HIGH		^{t}ANPD	WL - 1CK						CK	
Power-down entry period: ODT either synchronous or asynchronous		PDE	Greater of ^{t}ANPD or ^{t}RFC - REFRESH command to CKE LOW time						CK	
Power-down exit period: ODT either synchronous or asynchronous		PDX	^{t}ANPD + ^{t}XPDLL						CK	
Power-Down Entry Minimum Timing										
ACTIVATE command to power-down entry		^{t}ACTPDEN	MIN = 1				MIN = 2		CK	
PRECHARGE/PRECHARGE ALL command to power-down entry		^{t}PRPDEN	MIN = 1				MIN = 2		CK	
REFRESH command to power-down entry		^{t}REFPDEN	MIN = 1				MIN = 2		CK	37
MRS command to power-down entry		^{t}MRSPDEN	MIN = ^{t}MOD (MIN)						CK	
READ/READ with auto precharge command to power-down entry		^{t}RDPDEN	MIN = RL + 4 + 1						CK	
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRPDEN	MIN = WL + 4 + ^{t}WR/^{t}CK (AVG)						CK	
	BC4MRS	^{t}WRPDEN	MIN = WL + 2 + ^{t}WR/^{t}CK (AVG)						CK	
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRAPDEN	MIN = WL + 4 + WR + 1						CK	
	BC4MRS	^{t}WRAPDEN	MIN = WL + 2 + WR + 1						CK	
Power-Down Exit Timing										
DLL on, any valid command, or DLL off to commands not requiring locked DLL		^{t}XP	MIN = greater of 3CK or 6ns; MAX = N/A						CK	
Precharge power-down with DLL off to commands requiring a locked DLL		^{t}XPDLL	MIN = greater of 10CK or 24ns; MAX = N/A						CK	28
ODT Timing										
R_{TT} synchronous turn-on delay		ODTL on	CWL + AL - 2CK						CK	38
R_{TT} synchronous turn-off delay		ODTL off	CWL + AL - 2CK						CK	40

Table 10: Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter	Symbol	gDDR3-1600		gDDR3-1800		gDDR3-2000		Unit	Notes
		Min	Max	Min	Max	Min	Max		
R_{TT} turn-on from ODTL on reference	^{t}AON	–250	250	–225	225	-195	195	ps	23, 38
R_{TT} turn-off from ODTL off reference	^{t}AOF	0.3	0.7	0.3	0.7	0.3	.07	CK	39, 40
Asynchronous R_{TT} turn-on delay (power-down with DLL off)	^{t}AONPD	MIN = 2; MAX = 8.5						ns	38
Asynchronous R_{TT} turn-off delay (power-down with DLL off)	^{t}AOFPD	MIN = 2; MAX = 8.5						ns	40
ODT HIGH time with WRITE command and BL8	ODTH8	MIN = 6; MAX = N/A						CK	
ODT HIGH time without WRITE command or with WRITE command and BC4	ODTH4	MIN = 4; MAX = N/A						CK	
Dynamic ODT Timing									
$R_{TT,nom}$-to-$R_{TT(WR)}$ change skew	ODTLcnw	WL - 2CK						CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BC4	ODTLcnw4	4CK + ODTLoff						CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BL8	ODTLcnw8	6CK + ODTLoff						CK	
R_{TT} dynamic change skew	^{t}ADC	0.3	0.7	0.3	0.7	0.3	0.7	CK	39
Write Leveling Timing									
First DQS, DQS# rising edge	^{t}WLMRD	40	–	40	–	40	–	CK	
DQS, DQS# delay	^{t}WLDQSEN	25	–	25	–	25	–	CK	
Write leveling setup from rising CK, CK# crossing to rising DQS, DQS# crossing	^{t}WLS	195	–	165	–	140	–	ps	
Write leveling hold from rising DQS, DQS# crossing to rising CK, CK# crossing	^{t}WLH	195	–	165	–	140	–	ps	
Write leveling output delay	^{t}WLO	0	9	0	7.5	0	7.5	ns	
Write leveling output error	^{t}WLOE	0	2	0	2	0	2	ns	

Notes:
1. Parameters are applicable with 0°C ≤ T_C ≤ 95°C and V_{DD}/V_{DDQ} = 1.5V ±0.075V.
2. All voltages are referenced to V_{SS}.
3. Output timings are only valid for R_{ON34} output buffer selection.
4. The unit ^{t}CK (AVG) represents the actual ^{t}CK (AVG) of the input clock under operation. The unit CK represents one clock cycle of the input clock, counting the actual clock edges.
5. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 900mV in the test environment, but input timing is still referenced to V_{REF} (except ^{t}IS, ^{t}IH, ^{t}DS, and ^{t}DH use the AC/DC trip points, and CK, CK# and DQS, DQS# use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single-ended inputs and 2 V/ns for differential inputs in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
6. All timings that use time-based values (ns, µs, ms) should use ^{t}CK (AVG) to determine the correct number of clocks (this table uses CK or ^{t}CK [AVG] interchangeably). In the case of noninteger results, all minimum limits are to be rounded up to the nearest whole integer, and all maximum limits are to be rounded down to the nearest whole integer.

7. Strobe or DQSdiff refers to the DQS and DQS# differential crossing point when DQS is the rising edge. Clock or CK refers to the CK and CK# differential crossing point when CK is the rising edge.
8. This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different. The output signal voltage reference point is $V_{DDQ}/2$ for single-ended signals and the crossing point for differential signals.
9. When operating in DLL disable mode, Micron does not warrant compliance with normal mode timings or functionality.
10. The clock's ^{t}CK (AVG) is the average clock over any 200 consecutive clocks and ^{t}CK (AVG) MIN is the smallest clock rate allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
11. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of ^{t}CK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below ^{t}CK (AVG) MIN.
12. The clock's ^{t}CH (AVG) and ^{t}CL (AVG) are the average half clock period over any 200 consecutive clocks and is the smallest clock half period allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
13. The period jitter ($^{t}JIT_{PER}$) is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.
14. ^{t}CH (ABS) is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.
15. ^{t}CL (ABS) is the absolute instantaneous clock low pulse width as measured from one falling edge to the following rising edge.
16. The cycle-to-cycle jitter $^{t}JIT_{CC}$ is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.
17. The cumulative jitter error ^{t}ERR*n*PER, where *n* is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over *n* number of clock cycles.
18. ^{t}DS (base) and ^{t}DH (base) values are for a single-ended 1 V/ns DQ slew rate and 2 V/ns differential DQS, DQS# slew rate.
19. These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transition edge to its respective data strobe signal (DQS, DQS#) crossing.
20. The setup and hold times are listed converting the base specification values (to which derating tables apply) to V_{REF} when the slew rate is 1 V/ns. These values, with a slew rate of 1 V/ns, are for reference only.
21. When the device is operated with input clock jitter, this parameter needs to be derated by the actual $^{t}JIT_{PER}$ (larger of $^{t}JIT_{PER}$ (MIN) or $^{t}JIT_{PER}$ (MAX) of the input clock (output deratings are relative to the SDRAM input clock).
22. Single-ended signal parameter.
23. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The following parameters are required to be derated by subtracting $^{t}ERR_{10PER}$ (MAX): ^{t}DQSCK (MIN), ^{t}LZ(DQS) MIN, ^{t}LZ(DQ) MIN, and ^{t}AON (MIN). The following parameters are required to be derated by subtracting $^{t}ERR_{10PER}$ (MIN): ^{t}DQSCK (MAX), ^{t}HZ (MAX), ^{t}LZ (DQS) MAX, ^{t}LZ (DQ) MAX, and ^{t}AON (MAX). The parameter ^{t}RPRE (MIN) is derated by subtracting $^{t}JIT_{PER}$ (MAX), while ^{t}RPRE (MAX) is derated by subtracting $^{t}JIT_{PER}$ (MIN).
24. The maximum preamble is bound by ^{t}LZDQS (MAX).
25. These parameters are measured from a data strobe signal (DQS, DQS#) crossing to its respective clock signal (CK, CK#) crossing. The specification values are not affected by the

amount of clock jitter applied because these are relative to the clock signal crossing. These parameters should be met whether clock jitter is present.

26. The ^{t}DQSCK (DLL_DIS) parameter begins CL + AL - 1 cycles after the READ command.
27. The maximum postamble is bound by ^{t}HZDQS (MAX).
28. Commands requiring a locked DLL are READ (and RDAP) and synchronous ODT commands. In addition, after any change of latency ^{t}XPDLL, timing must be met.
29. ^{t}IS (base) and ^{t}IH (base) values are for a single-ended 1 V/ns control/command/address slew rate and 2 V/ns CK, CK# differential slew rate.
30. These parameters are measured from a command/address signal transition edge to its respective clock (CK, CK#) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present.
31. For these parameters, the DDR3 SDRAM device supports ^{t}nPARAM (nCK) = RU(^{t}PARAM [ns]/^{t}CK[AVG] [ns]), assuming all input clock jitter specifications are satisfied. For example, the device will support ^{t}nRP (nCK) = RU(^{t}RP/^{t}CK[AVG]) if all input clock jitter specifications are met. This means that for DDR3-800 6-6-6, of which ^{t}RP = 15ns, the device will support ^{t}nRP = RU(^{t}RP/^{t}CK[AVG]) = 6 as long as the input clock jitter specifications are met. That is, the PRECHARGE command at T0 and the ACTIVATE command at T0 + 6 are valid even if six clocks are less than 15ns due to input clock jitter.
32. During READs and WRITEs with auto precharge, the DDR3 SDRAM will hold off the internal PRECHARGE command until ^{t}RAS (MIN) has been satisfied.
33. When operating in DLL disable mode, the greater of 4CK or 15ns is satisfied for ^{t}WR.
34. The start of the write recovery time is defined as follows:
    - For BL8 (fixed by MRS and OTF): Rising clock edge four clock cycles after WL
    - For BC4 (OTF): Rising clock edge four clock cycles after WL
    - For BC4 (fixed by MRS): Rising clock edge two clock cycles after WL
35. RESET# should be LOW as soon as power starts to ramp to ensure the outputs are in High-Z. Until RESET# is LOW, the outputs are at risk of driving and could result in excessive current, depending on bus activity.
36. The refresh period is 64ms when T_C is less than or equal to 85°C. This equates to an average refresh rate of 7.8125µs. However, nine REFRESH commands should be asserted at least once every 70.3µs. When T_C is greater than 85°C, the refresh period is 32ms.
37. Although CKE is allowed to be registered LOW after a REFRESH command when ^{t}REFPDEN (MIN) is satisfied, there are cases where additional time such as ^{t}XPDLL (MIN) is required.
38. ODT turn-on time MIN is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time maximum is when the ODT resistance is fully on.
39. Half-clock output parameters must be derated by the actual $^{t}ERR_{10PER}$ and $^{t}JIT_{DTY}$ when input clock jitter is present. This results in each parameter becoming larger. The parameters ^{t}ADC (MIN) and ^{t}AOF (MIN) are each required to be derated by subtracting both $^{t}ERR_{10PER}$ (MAX) and $^{t}JIT_{DTY}$ (MAX). The parameters ^{t}ADC (MAX) and ^{t}AOF (MAX) are required to be derated by subtracting both $^{t}ERR_{10PER}$ (MAX) and $^{t}JIT_{DTY}$ (MAX).
40. ODT turn-off time minimum is when the device starts to turn off ODT resistance. ODT turn-off time maximum is when the DRAM buffer is in High-Z.
41. Pulse width of an input signal is defined as the width between the first crossing of $V_{REF(DC)}$ and the consecutive crossing of $V_{REF(DC)}$.
42. Should the clock rate be larger than ^{t}RFC (MIN), an AUTO REFRESH command should have at least one NOP command between it and another AUTO REFRESH command. Additionally, if the clock rate is slower than 40ns (25 MHz), all REFRESH commands should be followed by an AUTO PRECHARGE command.

Command and Address Setup, Hold, and Derating

The total ^{t}IS (setup time) and ^{t}IH (hold time) required is calculated by adding the data sheet ^{t}IS (base) and ^{t}IH (base) values to the Δ^{t}IS and Δ^{t}IH derating values, respectively. Example: ^{t}IS (total setup time) = ^{t}IS (base) + Δ^{t}IS. For a valid transition, the input signal has to remain above/below $V_{IH(AC)}/V_{IL(AC)}$ for some time ^{t}VAC.

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached $V_{IH(AC)}/V_{IL(AC)}$ at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach $V_{IH(AC)}/V_{IL(AC)}$.

Setup (^{t}IS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. Setup (^{t}IS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is always earlier than the nominal slew rate line between the shaded $V_{REF(DC)}$-to-AC region, use the nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between the shaded $V_{REF(DC)}$-to-AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for derating value.

Hold (^{t}IH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. Hold (^{t}IH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between the shaded DC-to-$V_{REF(DC)}$ region, use the nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between the shaded DC-to-$V_{REF(DC)}$ region, the slew rate of a tangent line to the actual signal from the DC level to the $V_{REF(DC)}$ level is used for derating value.

Table 11: Command and Address Setup and Hold Values Referenced at 1 V/ns – AC/DC-Based

Symbol	gDDR3-1600	gDDR3-1800	gDDR3-2000	Unit	Reference
^{t}IS (base) AC175	65	45	–	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}IS (base) AC150	190	170	–	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}IS (base) AC135	–	–	65	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}IS (base) AC125	–	–	150	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}IH (base) DC100	140	120	100	ps	$V_{IH(DC)}/V_{IL(DC)}$

Data Setup, Hold, and Derating

The total ^{t}DS (setup time) and ^{t}DH (hold time) required is calculated by adding the data sheet ^{t}DS (base) and ^{t}DH (base) values to the Δ^{t}DS and Δ^{t}DH derating values, respectively. Example: ^{t}DS (total setup time) = ^{t}DS (base) + Δ^{t}DS. For a valid transition, the input signal has to remain above/below $V_{IH(AC)}/V_{IL(AC)}$ for some time ^{t}VAC.

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached $V_{IH(AC)}/V_{IL(AC)}$) at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach $V_{IH}/V_{IL(AC)}$.

Setup (^{t}DS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. Setup (^{t}DS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is always earlier than the nominal slew rate line between the shaded $V_{REF(DC)}$-to-AC region, use the nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between the shaded $V_{REF(DC)}$-to-AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for derating value.

Hold (^{t}DH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. Hold (^{t}DH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between the shaded DC-to-$V_{REF(DC)}$ region, use the nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between the shaded DC-to-$V_{REF(DC)}$ region, the slew rate of a tangent line to the actual signal from the DC-to-$V_{REF(DC)}$ region is used for derating value.

Table 12: Data Setup and Hold Values at 1 V/ns (DQS, DQS# at 2 V/ns) – AC/DC-Based

Symbol	gDDR3-1600	gDDR3-1800	gDDR3-2000	Unit	Reference
^{t}DS (base) AC175	–	–	–	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}DS (base) AC150	30	10	–	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}DS (base) AC135	60	40	68	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}DH (base) DC100	65	45	70	ps	$V_{IH(DC)}/V_{IL(DC)}$