Mobile SDRAM

MT48H16M16LF – 4 Meg x 16 x 4 banks
MT48H8M32LF – 2 Meg x 32 x 4 banks

For the latest data sheet, refer to Micron's Web site: http://www.micron.com/products/dram/mobile

Features

- Fully synchronous; all signals registered on positive edge of system clock
- V_{DD} = +1.8V ±0.1V, V_{DDQ} = +1.8V ±0.1V
- Internal, pipelined operation; column address can be changed every clock cycle
- Four internal banks for concurrent operation
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge
- Auto refresh and self refresh modes
- LVTTL-compatible inputs and outputs
- On-chip temperature sensor to control refresh rate
- Partial array self refresh (PASR)
- Deep power-down (DPD)
- Selectable output drive (DS)
- 64ms refresh period (8,192 rows)

Options	Marking
• V_{DD}/V_{DDQ}	
• 1.8V/1.8V	H
• Configuration	
• 16 Meg x 16 (4 Meg x 16 x 4 banks)	16M16
• 8 Meg x 32 (2 Meg x 32 x 4 banks)	8M32
• Plastic Package	
• 54-Ball VFBGA (8mm x 9mm)[1]	BF
• 90-Ball VFBGA (8mm x 13mm)[2]	B5
• Timing – Cycle Time	
• 7.5ns @ CL = 3	-75
• 8ns @ CL = 3	-8
• 10ns @ CL = 3	-10
• Operating Temperature Range	
• Commercial (0° to +70°C)	None
• Industrial (-40°C to +85°C)	IT

Notes: 1. Only available for x16 configuration.
2. Only available for x32 configuration.

Table 1: Addressing

	16 Meg x 16	8 Meg x 32
Configuration	4 Meg x 16 x 4 banks	2 Meg x 32 x 4 banks
Refresh Count	8K	8K
Row Addressing	8K (A0-A12)	8K (A0-A12)
Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)
Column Addressing	512K (A0-A8)	256 (A0-A7)

Table 2: Key Timing Parameters

Speed Grade	Clock Rate			Access Time at CL3	Data Setup Time	Data Hold Time
	CL = 1	CL = 2	CL = 3			
-75	-	111	133 MHz	6ns	1.5ns	1ns
-8	50	111	125 MHz	7ns	2.5ns	1ns
-10	40	83	104 MHz	7ns	2.5ns	1ns

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Table 1: 256Mb Mobile SDRAM Part Numbers
xx = -75, -8, or -10

Part Number	Configuration	I/O Drive Level	Temperature Option
MT48H16M16LFBF-xx	16 Meg x 16	Programmable Drive	0°C to +70°C
MT48H16M16LFBF-xxIT	16 Meg x 16	Programmable Drive	-40°C to +85°C
MT48H8M32LFB5-xx	8 Meg x 32	Programmable Drive	0°C to +70°C
MT48H8M32LFB5-xxIT	8 Meg x 32	Programmable Drive	-40°C to +85°C

General Description

The Micron® 256Mb Mobile SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456-bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 67,108,864-bit banks is organized as 8,192 rows by 512K columns by 16 bits. Each of the x32's 67,108,864-bit banks is organized as 8,192 rows by 256 columns by 32 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable read or write burst lengths of 1, 2, 4, 8, or 16 locations, or full page, with a read burst terminate option. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 256 Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless high-speed, random-access operation.

The 256Mb SDRAM is designed to operate in 1.8V low-power memory systems. An auto refresh mode is provided, along with a power-saving deep power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

Figure 1: Functional Block Diagram: 16 Meg x 16 SDRAM

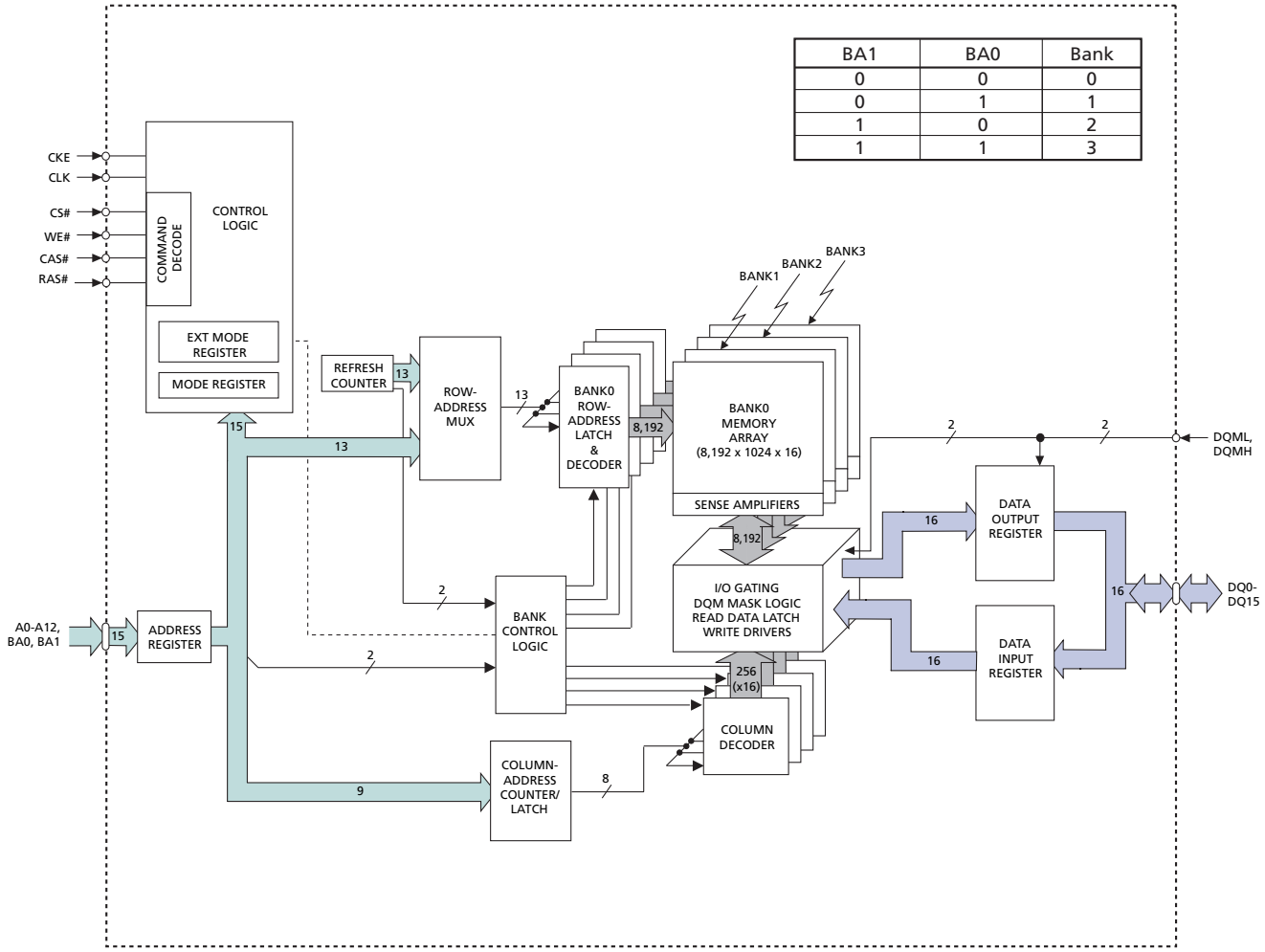
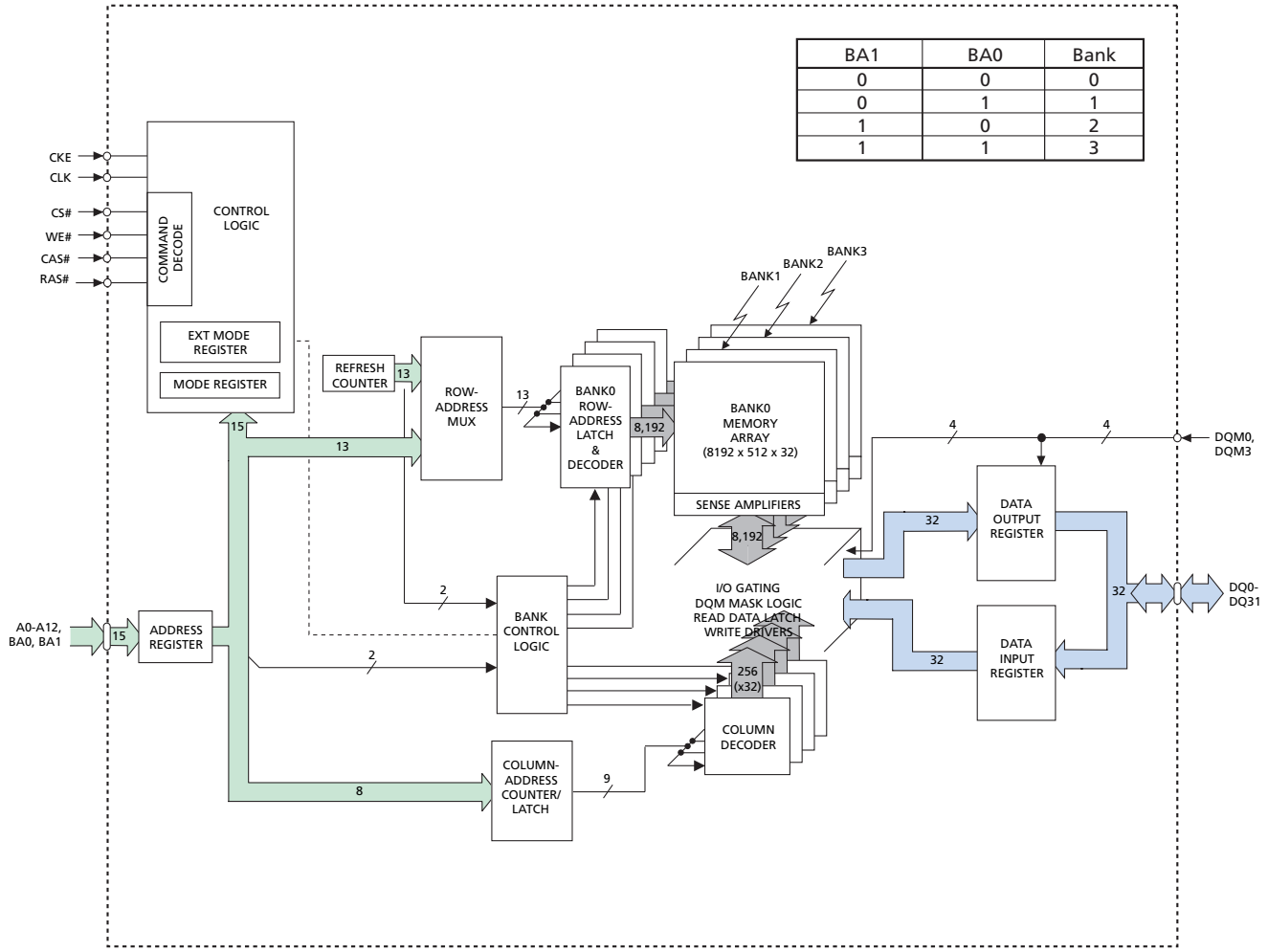


Figure 2: Functional Block Diagram: 8 Meg x 32 SDRAM



Ball Assignment

Figure 3: 54-Ball FBGA (Top View) – 8mm x 9mm

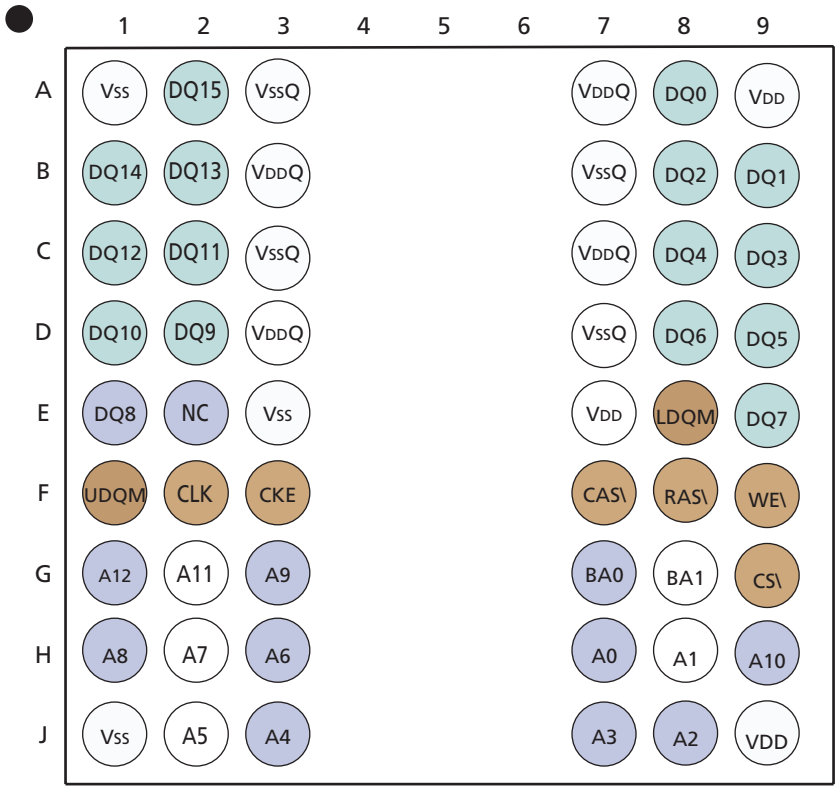
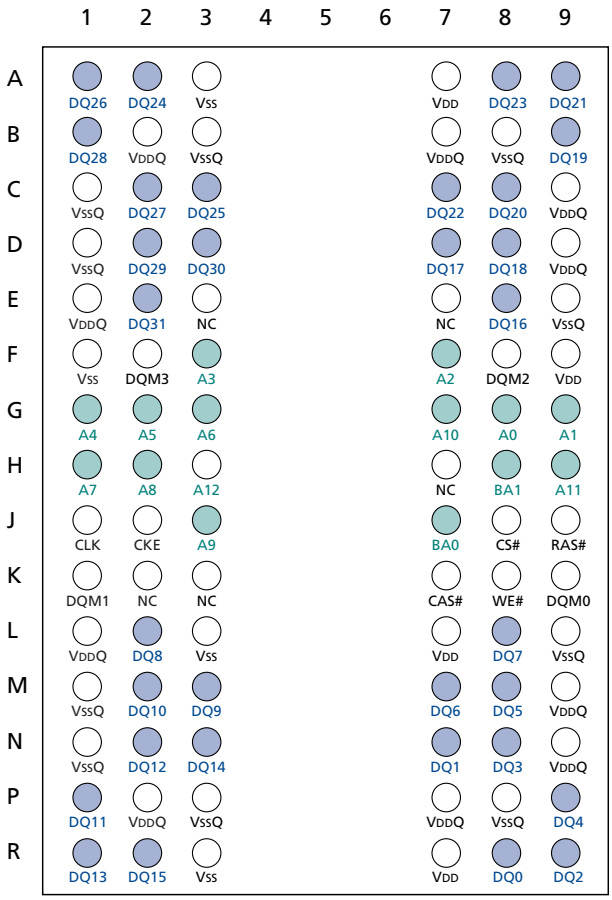


Figure 4: 90-Ball VFBGA (Top View) – 8mm x 13mm



Ball Descriptions

Table 2: VFBGA Ball Descriptions

54-Ball VFBGA	90-Ball VFBGA	Symbol	Type	Description
F2	J1	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
F3	J2	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row active in any bank), DEEP POWER-DOWN (all banks idle), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power.
G9	J8	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
F7, F8, F9	J9, K7, K8	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
E8, F1	K9, K1, F8, F2	DQM0–DQM3, LDQM, UDQM	Input	Input/Output Mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when during a READ cycle. For the x16, LDQM corresponds to DQ0-DQ7 and UDQM corresponds to DQ8-DQ16. For the x32, DQM0 corresponds to DQ0-DQ7, DQM1 corresponds to DQ8-DQ15, DQM2 corresponds to DQ16-DQ23, and DQM3 corresponds to DQ24-DQ31. DQM0-3 (or LDQM and UDQM if x16) are considered same state when referenced as DQM.
G7, G8	J7, H8	BA0, BA1	Input	Bank Address Input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. These balls also provide the op-code during a LOAD MODE REGISTER command. BA0 and BA1 become “don’t care” when registering an ALL-BANK PRECHARGE (A10 high).
H7, H8, J8, J7, J3, J2, H3, H2, H1, G3, H9, G2, G1	G8, G9, F3, F7, G1, G2, G3, H1, H2, H3, J3, G7, H9, F3, A12	A0–A12	Input	Address Inputs: A0–A12 are sampled during the ACTIVE command (row-address A0–A12) and READ/WRITE command [column-address A0–A8 (x32); column-address A0–A9 (x16); with A10 defining auto precharge] to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1. The address inputs also provide the op-code during a LOAD MODE REGISTER command.

Table 2: VFBGA Ball Descriptions (Continued)

54-Ball VFBGA	90-Ball VFBGA	Symbol	Type	Description
A8, B9, B8, C9, C8, D9, D8, E9, E1, D2, D1, C2, C1, B2, B1, A2	R8, N7, R9, N8, P9, M8, M7, L8, L2, M3, M2, P1, N2, R1, N3, R2, E8, D7, D8, B9, C8, A9, C7, A8, A2, C3, A1, C2, B1, D2, D3, E2	DQ0–DQ31	I/O	Data Input/Output: Data bus.
E2	E3, E7, H7, K2, K3	NC	–	Internally Not Connected: These could be left unconnected, but it is recommended they be connected to Vss.
A7, B3, C7, D3	B2, B7, C9, D9, E1, L1, M9, N9, P2, P7	VDDQ	Supply	DQ Power: Provide isolated power to DQ for improved noise immunity.
A3, B7, C3, D7	B8, B3, C1, D1, E9, L9, M1, N1, P3, P8	VSSQ	Supply	DQ Ground: Provide isolated ground to DQ for improved noise immunity.
A9, E7, J9	A7, F9, L7, R7	VDD	Supply	Core Power Supply.
A1, E3, J1	A3, F1, L3, R3	VSS	Supply	Ground.

Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 3: Absolute Maximum Ratings

Voltage/Temperature	Min	Max	Units
Voltage on V_{DD}/$V_{DD}Q$ supply			
Relative to V_{SS} (1.8V)	-0.35	+2.8	V
Voltage on inputs, NC, or I/O balls			
Relative to V_{SS} (1.8V)	-0.35	+2.8	V
Operating temperature			
T_A (Commercial)	0°	+70°	C
T_A (Industrial)	-40°	+85°	C
Storage temperature			
Plastic	-55°	+150°	C

Table 4: DC Electrical Characteristics and Operating Conditions

Note 1, 5, 6 apply to the following parameters; notes appear on page 19.

Parameter/Condition	Symbol	Min	Max	Units	Notes
Supply voltage	V_{DD}	1.7	1.9	V	
I/O supply voltage	$V_{DD}Q$	1.7	1.9	V	
Input high voltage: Logic 1; All inputs	V_{IH}	0.8 x $V_{DD}Q$	$V_{DD}Q$ + 0.3	V	22
Input low voltage: Logic 0; All inputs	V_{IL}	-0.3	+0.3	V	22
Output high voltage: All inputs: Iout = -4mA	V_{OH}	0.9 x $V_{DD}Q$	–	V	
Output low voltage: All inputs: Iout = 4mA	V_{OL}	–	0.2	V	
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	I_I	-1.0	1.0	µA	
Output leakage current: DQ are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$	I_{OZ}	5	5	µA	

Table 5: Electrical Characteristics and Recommended AC Operating Conditions

Notes 5, 6, 8, 9, 11 apply to the following parameters; notes appear on page 19

AC Characteristics			-75		-8		-10			
Parameter		**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Access time from CLK (pos. edge)	CL = 3	^{t}AC (3)		5.4		7		7	ns	9
	CL = 2	^{t}AC (2)		6		8		8	ns	9
	CL = 1	^{t}AC (1)	-	-		19		22	ns	9
Address hold time		^{t}AH	0.8		1		1		ns	
Address setup time		^{t}AS	1.5		2.0		2.5		ns	
CLK high-level width		^{t}CH	3		3		3		ns	
CLK low-level width		^{t}CL	3		3		3		ns	
Clock cycle time	CL = 3	^{t}CK (3)	7.5		8		9.6		ns	23
	CL = 2	^{t}CK (2)	TBD	-	TBD	-	TBD	-	ns	23
	CL = 1	^{t}CK (1)	-	-	-	-	TBD	-	ns	
CKE hold time		^{t}CKH	0.8		1		1		ns	
CKE setup time		^{t}CKS	1.5		2.5		2.5		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^{t}CMH	0.8		1		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^{t}CMS	1.5		2.5		2.5		ns	
Data-in hold time		^{t}DH	0.8		1		1		ns	
Data-in setup time		^{t}DS	1.5		2.5		2.5		ns	
Data-out high impedance time	CL = 3	^{t}HZ (3)		5.4		7		7	ns	10
	CL = 2	^{t}HZ (2)		6.5		8		8	ns	10
	CL = 1	^{t}HZ (1)		-		-19		22	ns	10
Data-out low impedance time		^{t}LZ	1		1		1		ns	
Data-out hold time (load)		^{t}OH	2.5		2.5		2.5		ns	
Data-out hold time (no load)		^{t}OHN	1.8		1.8		1.8		ns	27
ACTIVE to PRECHARGE command		^{t}RAS	45	120,000	48	120,000	50	120,000	ns	
ACTIVE to ACTIVE command period		^{t}RC	75		80		100		ns	
ACTIVE to READ or WRITE delay		^{t}RCD	22.5		24		30		ns	
Refresh period (8,192 rows)		^{t}REF		64		64		64	ms	
AUTO REFRESH period		^{t}RFC	75		80		100		ns	
PRECHARGE command period		^{t}RP	22.5		24		30		ns	
ACTIVE bank *a* to ACTIVE bank *b* command		^{t}RRD	15		16		20		ns	
Transition time		^{t}T	0.3	1.2	0.5	1.2	0.5	1.2	ns	7
WRITE recovery time		^{t}WR (a)	1 CLK + 7.5ns		1 CLK +7ns		1 CLK +5ns		–	24
		^{t}WR (m)	15		15		15		ns	25
Exit SELF REFRESH to ACTIVE command		^{t}XSR	75		80		100		ns	20

Table 6: AC Functional Characteristics

Notes 5, 6, 7, 8, 9, 11 apply to the following parameters; notes appear on page 19

Parameter		Symbol	-75	-8	-10	Units	Notes
READ/WRITE command to READ/WRITE command		tCCD	1	1	1	tCK	17
CKE to clock disable or power-down entry mode		tCKED	1	1	1	tCK	14
CKE to clock enable or power-down exit setup mode		tPED	1	1	1	tCK	14
DQM to input data delay		tDQD	0	0	0	tCK	17
DQM to data mask during WRITEs		tDQM	0	0	0	tCK	17
DQM to data high impedance during READs		tDQZ	2	2	2	tCK	17
WRITE command to input data delay		tDWD	0	0	0	tCK	17
Data-in to ACTIVE command		tDAL	5	5	5	tCK	15, 21
Data-in to PRECHARGE command		tDPL	2	2	2	tCK	16, 21
Last data-in to burst STOP command		tBDL	1	1	1	tCK	17
Last data-in to new READ/WRITE command		tCDL	1	1	1	tCK	17
Last data-in to PRECHARGE command		tRDL	2	2	2	tCK	16, 21
LOAD MODE REGISTER command to ACTIVE or REFRESH command		tMRD	2	2	2	tCK	26
Data-out to high impedance from PRECHARGE command	CL = 3	tROH(3)	3	3	3	tCK	17
	CL = 2	tROH(2)	2	2	2	tCK	17
	CL = 1	tROH(2)	-	1	1	tCK	17

Table 7: IDD Specifications and Conditions (x16)

Notes 1, 5, 6, 11, 13 apply to the following parameters; notes appear on page 19

Parameter/Condition		Symbol	Max			Unit	Notes
			-75	-8	-10		
Operating one bank active-precharge current: $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN);CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching; Data bus inputs are stable		IDD1	65	60	55	mA	3, 18, 19, 28
Precharge power-down standby current: All banks idle, CKE is LOW; CS is HIGH, $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		IDD2P	500	500	500	µA	
Precharge power-down standby current with clock stopped: All banks idle; CKE is LOW; CS is HIGH, CK = LOW; Address and control inputs are switching; Data bus inputs are stable		IDD2PS	500	500	500	µA	
Precharge non power-down standby current: All banks idle CKE = HIGH; CS = HIGH; $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		IDD2N	15	10	10	mA	28
Precharge non power-down standby current: clock stopped All banks idle, CKE = HIGH; CS = HIGH; CK = LOW; Address and control inputs are switching; Data bus inputs are stable		IDD2NS	5	5	5	mA	
Active power-down standby current: One bank active, CKE = LOW; CS = HIGH; $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		IDD3P	5	5	5	mA	
Active power-down standby current: clock stopped One bank active, CKE = LOW; CS = HIGH; CK = LOW; Address and control inputs are switching; Data bus inputs are stable		IDD3PS	3	3	3	mA	
Active non power-down standby: One bank active, CKE = HIGH; CS = HIGH; $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		IDD3N	20	15	15	mA	
Active non-power-down standby: clock stopped One bank active, CKE = HIGH; CS = HIGH; CK = LOW; Address and control inputs are switching; Data bus inputs are stable		IDD3NS	10	10	10	mA	3, 12, 19, 28
Operating burst read: One bank active; BL = 4; CL = 3; $^{t}CK = {}^{t}CK$ (MIN); Continuous read bursts; IOUT = 0mA; Address inputs are switching; 50% data changing each burst		IDD4R	95	90	90	mA	3, 18, 19, 28
Operating burst write: One bank active; BL = 4; $^{t}CK = {}^{t}CK$ (MIN); continuous WRITE bursts; Address inputs are switching; 50% data changing each burst		IDD4W	100	90	90	mA	3, 18, 19, 28
Auto refresh: Burst refresh; CKE = HIGH Address and control inputs are switching; Data bus inputs are stable	$^{t}RCF = {}^{t}RCF$ (MIN)	IDD5	55	50	45	mA	3, 12, 18, 19, 28, 29
	^{t}RCF = 7.8125µs	IDD5a	3	3	3	mA	
Deep power-down		Izz	10	10	10	µA	

Table 8: IDD7 - Self Refresh Current Options (x16)
Note 4 applies to the following parameters; notes appear on page 19

Parameter/Condition		Symbol	Max			Unit	Notes
			-75	-8	-10		
Self refresh CKE = LOW; tCK = tCK (MIN); Address and control inputs are stable; Data bus inputs are stable	Full Array, 85°C	IDD7	TBD			µA	4
	Full Array, 70°C	IDD7	TBD			µA	4
	Full Array, 45°C	IDD7	TBD			µA	4
	Full Array, 15°C	IDD7	TBD			µA	4
	Half Array, 85°C	IDD7	TBD			µA	4
	Half Array, 70°C	IDD7	TBD			µA	4
	Half Array, 45°C	IDD7	TBD			µA	4
	Half Array, 15°C	IDD7	TBD			µA	4
	1/4 Array, 85°C	IDD7	TBD			µA	4
	1/4 Array, 70°C	IDD7	TBD			µA	4
	1/4 Array, 45°C	IDD7	TBD			µA	4
	1/4 Array, 15°C	IDD7	TBD			µA	4
	1/8 Array, 85°C	IDD7	TBD			µA	4
	1/8 Array, 70°C	IDD7	TBD			µA	4
	1/8 Array, 45°C	IDD7	TBD			µA	4
	1/8 Array, 15°C	IDD7	TBD			µA	4
	1/16 Array, 85°C	IDD7	TBD			µA	4
	1/16 Array, 70°C	IDD7	TBD			µA	4
	1/16 Array, 45°C	IDD7	TBD			µA	4
	1/16 Array, 15°C	IDD7	TBD			µA	4

Table 9: IDD Specifications and Conditions (x32)
Notes: 3, 4, 12, 18, 19, 28, 29; notes appear on pages 19

Parameter/Condition		Symbol	Max -75	Max -8	Max -10	Unit	Notes
Operating one bank active-precharge current: ^{t}RFC = ^{t}RFC (MIN); ^{t}CK = ^{t}CK (MIN);CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching; Data bus inputs are stable		IDD1	65	60	55	mA mA	3, 18, 19, 28
Precharge power-down standby current: All banks idle, CKE is LOW; CS is HIGH, ^{t}CK = ^{t}CK (MIN); Address and control inputs are switching; Data bus inputs are stable		IDD2P	500	500	500	µA	
Precharge power-down standby current with clock stopped: All banks idle; CKE is LOW; CS is HIGH, CK = LOW; Address and control inputs are switching; Data bus inputs are stable		IDD2PS	500	500	500	µA	
Precharge non-power-down standby current: All banks idle CKE = HIGH; CS = HIGH; ^{t}CK = ^{t}CK (MIN); Address and control inputs are switching; Data bus inputs are stable		IDD2N	15	10	10	mA	28
Precharge non-power-down standby current: clock stopped All banks idle, CKE = HIGH; CS = HIGH; CK = LOW; Address and control inputs are switching; Data bus inputs are stable		IDD2NS	5	5	5	mA	
Active power-down standby current: One bank active, CKE = LOW; CS = HIGH; ^{t}CK = ^{t}CK (MIN); Address and control inputs are switching; Data bus inputs are stable		IDD3P	5	5	5	mA	
Active power-down standby current: clock stopped One bank active, CKE = LOW; CS = HIGH; CK = LOW; Address and control inputs are switching; Data bus inputs are stable		IDD3PS	3	3	3	mA	
Active non-power-down standby: One bank active, CKE = HIGH; CS = HIGH; ^{t}CK = ^{t}CK (MIN); Address and control inputs are switching; Data bus inputs are stable		IDD3N	20	15	15	mA	
Active non-power-down standby: clock stopped One bank active, CKE = HIGH; CS = HIGH; CK = LOW; Address and control inputs are switching; Data bus inputs are stable		IDD3NS	10	10	10	mA	3, 12, 19, 28
Operating burst read: One bank active; BL = 4; CL = 3; ^{t}CK = ^{t}CK (MIN); Continuous read bursts; IOUT = 0mA; Address inputs are switching; 50% data changing each burst		IDD4R	120	115	110	mA	3, 18, 19, 28
Operating burst write: One bank active; BL = 4; ^{t}CK = ^{t}CK (MIN); continuous WRITE bursts; Address inputs are switching; 50% data changing each burst		IDD4W	120	115	110	mA	3, 18, 19, 28
Auto refresh: Burst refresh; CKE = HIGH Address and control inputs are switching; Data bus inputs are stable	^{t}RFC = ^{t}RFC (MIN)	IDD5	55	50	45	mA	3, 12, 18, 19, 28, 29
	^{t}RFC = 7.8125µs	IDD5a	3	3	3	mA	
Deep power-down		Izz	10	10	10	µA	

Table 10: IDD7 - Self Refresh Current Options (x32)
Note 4 applies to the following parameters; notes appear on pages 19

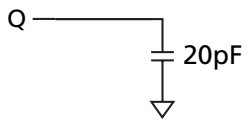
Parameter/Condition		Symbol	Max			Unit	Notes
			-75	-8	-10		
Self refresh CKE = LOW; tCK = tCK (MIN); Address and control inputs are stable; Data bus inputs are stable	Full Array, 85°C	IDD7	TBD			µA	4
	Full Array, 70°C	IDD7	TBD			µA	4
	Full Array, 45°C	IDD7	TBD			µA	4
	Full Array, 15°C	IDD7	TBD			µA	4
	Half Array, 85°C	IDD7	TBD			µA	4
	Half Array, 70°C	IDD7	TBD			µA	4
	Half Array, 45°C	IDD7	TBD			µA	4
	Half Array, 15°C	IDD7	TBD			µA	4
	1/4 Array, 85°C	IDD7	TBD			µA	4
	1/4 Array, 70°C	IDD7	TBD			µA	4
	1/4 Array, 45°C	IDD7	TBD			µA	4
	1/4 Array, 15°C	IDD7	TBD			µA	4
	1/8 Array, 85°C	IDD7	TBD			µA	4
	1/8 Array, 70°C	IDD7	TBD			µA	4
	1/8 Array, 45°C	IDD7	TBD			µA	4
	1/8 Array, 15°C	IDD7	TBD			µA	4
	1/16 Array, 85°C	IDD7	TBD			µA	4
	1/16 Array, 70°C	IDD7	TBD			µA	4
	1/16 Array, 45°C	IDD7	TBD			µA	4
	1/16 Array, 15°C	IDD7	TBD			µA	4

Table 11: Capacitance
Note 2 applies to the following parameters; otes appear on page 19

Parameter	Symbol	Min	Max	Units
Input capacitance: CLK	CI1	1.5	3.0	pF
Input capacitance: All other input-only balls	CI2	1.5	3.5	pF
Input/Output capacitance: DQ	CIO	2.0	4.5	pF

Notes

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD}, $V_{DD}Q$ = +1.8V; T_A = 25°C; pin under test biased at 1.4V; f = 1 MHz.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-40°C ≤ T_A ≤ +85°C for T_A on IT parts) is ensured.
6. An initial pause of 100µs is required after power-up, followed by one ALL-BANK PRECHARGE and two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and $V_{DD}Q$ must be powered up simultaneously. V_{SS} and $V_{SS}Q$ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
9. Outputs measured for 1.8V at 0.9V with equivalent load:



10. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^{t}OH before going High-Z.
11. AC timing and I_{DD} tests have V_{IL} and V_{IH}, with timing referenced to V_{IH}/2 = crossover point. If the input transition time is longer than ^{t}T (MAX), then the timing is referenced at V_{IL} (MAX) and V_{IH} (MIN) and no longer at the V_{IH}/2 crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{DD} specifications are tested after the device is properly initialized.
14. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by ^{t}WR plus ^{t}RP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^{t}WR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on ^{t}CK = 7.5ns for -75, ^{t}CK = 8ns for -8, and ^{t}CK = 10ns for -10.
22. V_{IH} overshoot: V_{IH} (MAX) = $V_{DD}Q$ + 2V for a pulse width ≤3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤3ns.

23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including ^{t}WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget (^{t}RP) begins at 7ns for -8 after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
25. Precharge mode only.
26. JEDEC specifies three clocks.
27. Parameter guaranteed by design.
28. For -10, CL = 3 and ^{t}CK =10ns.
29. CKE is HIGH during refresh command period ^{t}RFC (MIN) else CKE is LOW. The IDD6 limit is actually a nominal value and does not result in a fail value.