SDRAM

MT48LC16M32S2 – 4 Meg x 32 x 4 Banks

Features

- PC100 functionality
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge, and auto refresh modes
- Self refresh mode; standard and low power
- 64ms, 8,192-cycle refresh
- LVTTL-compatible inputs and outputs
- Operating temperature range
- Standard (0°C to +70°C)
- Industrial (-40°C to +85°C)
- Supports CAS latency of 1, 2, 3

Options — Marking

- VDD/VDDQ
  - 3.3V/3.3V — LC
- Configuration
  - 16M32 stacked die — S2
- Package/ballout
  - Plastic package 90-ball FBGA (8mm x 13mm)(standard) — F5
  - Plastic package 90-ball FBGA (8mm x 13mm) (lead-Free) — B5
- Timing (cycle time)
  - 6ns at CL3 (166 MHz) — -6
  - 7ns at CL3 (143 MHz) — -7
- Temperature
  - Commercial (0°C to +70°C) — No Marking
  - Industrial (-40°C to +85°C) — IT

Addendum Changes

The standard 256Mb SDRAM x32 data sheets should be referenced for a complete description of SDRAM functionality and operating modes. This addendum data sheet will concentrate on the key differences required to support the enhanced options of the TwinDie configuration.

The Micron 256Mb X32 data sheet provides full specifications and functionality unless specified herein.

Table 1: Configuration

Architecture	16 Meg x 32
Configuration	4 Meg x 32 x 4 banks
Refresh Count	8K
Row Addressing	8K (A0–A12)
Bank Addressing	4 (BA0, BA1)
Column Addressing	512 (A0–A8)

General Description

The 512Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured by stacking two 256Mb, 8 Meg x 32 devices. Each of these 256Mb devices is configured as a quad bank DRAM with a synchronous interface. They are organized with 32 DQs with 4 banks of 67,108,864 bits, comprising of 8,192 rows by 512 columns by 32 bits wide.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 512Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2n rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

The 512Mb SDRAM is designed to operate in 3.3V memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering die intitialization, register definition, command descriptions, and device operation on a per die basis unless otherwise noted.

This addendum documents any variances for the 512Mb: x32 SDRAM from the 256Mb: x32 SDRAM specification. Please refer to the 256Mb: x32 SDRAM data sheet on Micron's Web site for additional details on the part functionality.

Commands

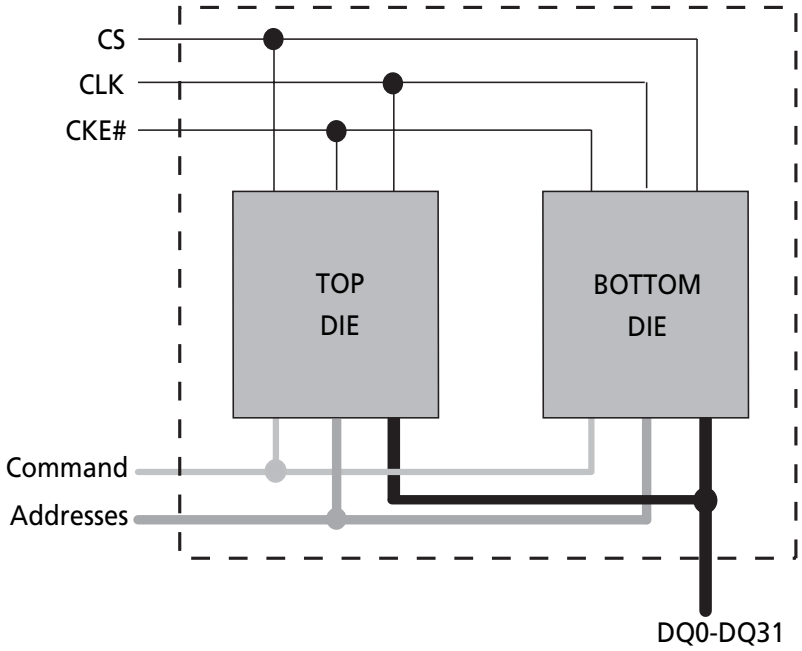
AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in conventional DRAMs. This command is non-persistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing a AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum ^{t}RP has been met after the PRECHARGE command as shown in the operations section.

The addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. The 512Mb TwinDie™ SDRAM requires 8,192 AUTO REFRESH cycles every 64ms (^{t}REF). Providing a distributed AUTO

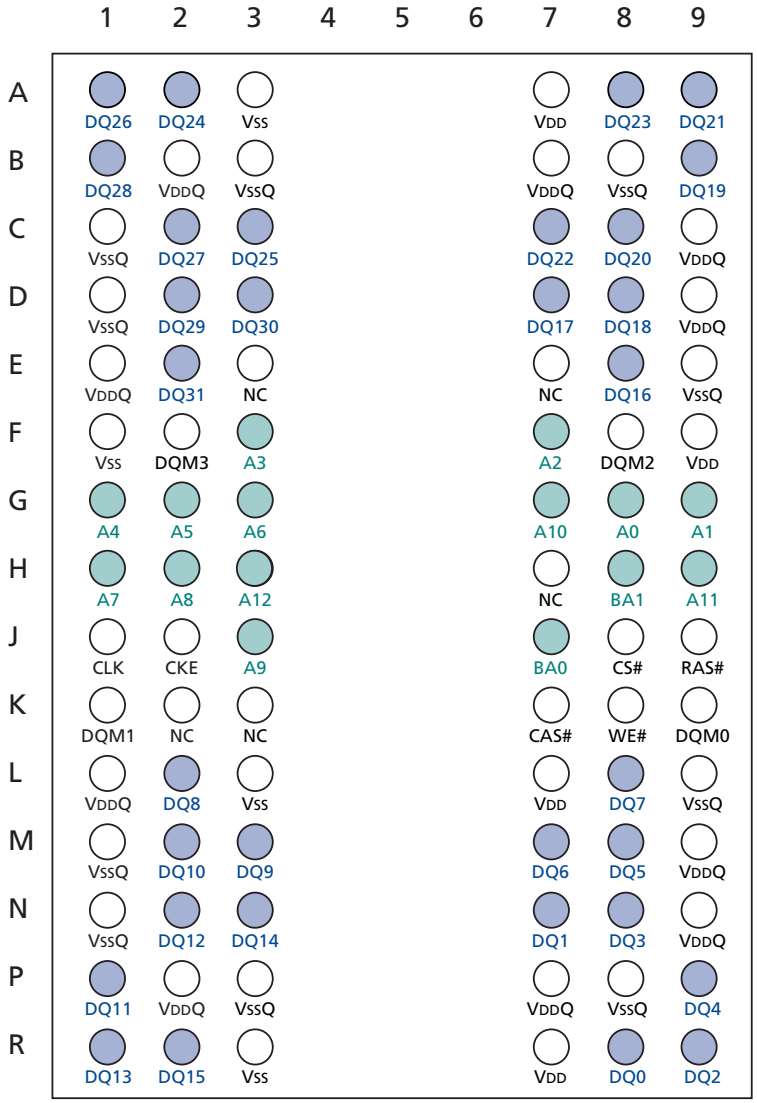
REFRESH command every 7.81µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 8,192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (^{t}RC), once every 64ms.

Figure 1: Functional Block Diagram



Ball Assignment

Figure 2: 90-Ball FBGA



Ball and Array

Electrical Specifications

Table 2: DC Electrical Characteristics and Operating Conditions

$V_{DD}/V_{DD}Q$ = +3.3V ±0.3V
Please refer to the 256Mb: x32 SDRAM data sheet for all notes.

Parameter/Condition	Symbol	MIN	MAX	Units	Notes
Supply Voltage	$V_{DD}/V_{DD}Q$	3	3.6	V	
Input High Voltage: Logic 1; All inputs	V_{IH}	2	V_{DD} + 0.3	V	22
Input Low Voltage: Logic 0; All inputs	V_{IL}	-0.3	0.8	V	22
Input Leakage Current: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other balls not under test = 0V)	I_I	-5	5	µA	
Output Leakage Current: DQs are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$	I_{OZ}	-5	5	µA	
Output Levels: Output High Voltage (I_{OUT} = -4mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OUT} = 4mA)	V_{OL}	–	0.4	V	

Table 3: I_{DD} Specifications and Conditions

V_{DD} = +3.3V ±0.3V, $V_{DD}Q$ = +3.3V ±0.3V
Please refer to the 256Mb: x32 SDRAM data sheet for all notes.

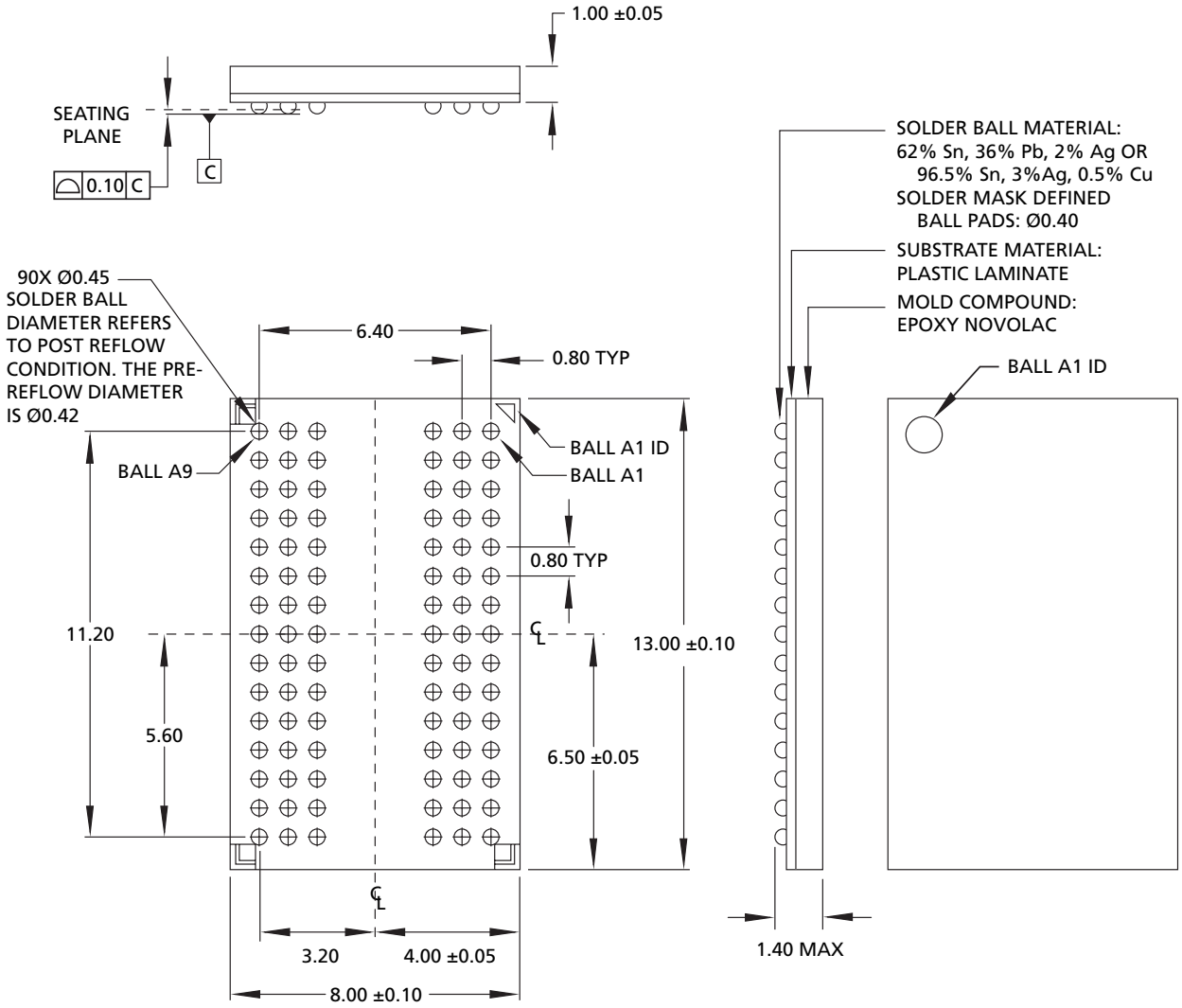
			MAX			
Parameter/Condition		Symbol	-6	-7	Units	Notes
Operating Current: Active Mode; Burst = 2; READ or WRITE; $^{t}RC = {}^{t}RC$ (MIN)		I_{DD1}	250	230	mA	3, 18, 19, 26
Standby Current: Power-Down Mode; All banks idle; CKE = LOW		I_{DD2}	2.4	2.4	mA	26
Standby Current: Active Mode; CKE = HIGH; CS# = HIGH; All banks active after ^{t}RCD met; No accesses in progress		I_{DD3}	80	80	mA	3, 12, 19, 26
Operating Current: Burst Mode; Continuous burst; READ or WRITE; All banks active, half DQs toggling every cycle.		I_{DD4}	205	185	mA	3, 18, 19, 26
Auto Refresh Current CKE = HIGH; CS# = HIGH	$^{t}RFC = {}^{t}RFC$ (MIN)	I_{DD5}	375	335	mA	3, 12, 18, 19, 26,
Self Refresh Current		I_{DD6}	4	4	mA	

Table 4: Capacitance

Parameter – FBGA "S2" Package	Symbol	MIN	MAX	Units
Input Capacitance: CLK	C_{I1}	5	8	pF
Input Capacitance: All other input-only balls	C_{I2}	5	9	pF
Input/Output Capacitance: DQs	C_{IO}	8	12	pF

Package Dimensions

Figure 3: 90-Ball FBGA (8mm x 13mm)



Notes: 1. All dimensions in millimeters.
2. Recommended pad size for PCB is 0.4mm ±0.025mm.

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