

Async/Page/Burst CellularRAM™ 1.0 Memory

MT45W2MW16BGB

Features

- Single device supports asynchronous, page, and burst operations
- Random access time: 70ns
- VCC, VCCQ voltages
 - 1.7–1.95V VCC
 - 1.7–3.6V VCCQ
- Page mode read access
 - 16-word page size
 - Interpage read access: 70ns
 - Intrapage read access: 20ns
- Burst mode write access: continuous burst
- Burst mode read access
 - 4, 8, or 16 words, or continuous burst
 - MAX clock rate: 104 MHz ($t_{CLK} = 9.62ns$)
 - Burst initial latency: 38.5ns (4 clocks) at 104 MHz
 - t_{CLK} : 7ns at 104 MHz
- Low power consumption
 - Asynchronous read: <20mA
 - Intrapage read: <15mA
 - Intrapage read initial access, burst read: (38.5ns [4 clocks] at 104 MHz) < 40mA
 - Continuous burst read: <25mA
 - Standby: <110μA
 - Deep power-down: <10μA (TYP at 25°C)
- Low-power features
 - Temperature-compensated refresh (TCR)
 - On-chip temperature sensor
 - Partial-array refresh (PAR)
 - Deep power-down (DPD) mode

Options

- Configuration
 - 2 Meg x 16
- Package
 - 54-ball VFBGA (“green”)
- Access time
 - 70ns access
- Frequency
 - 80 MHz
 - 104 MHz

Designator

MT45W2MW16B

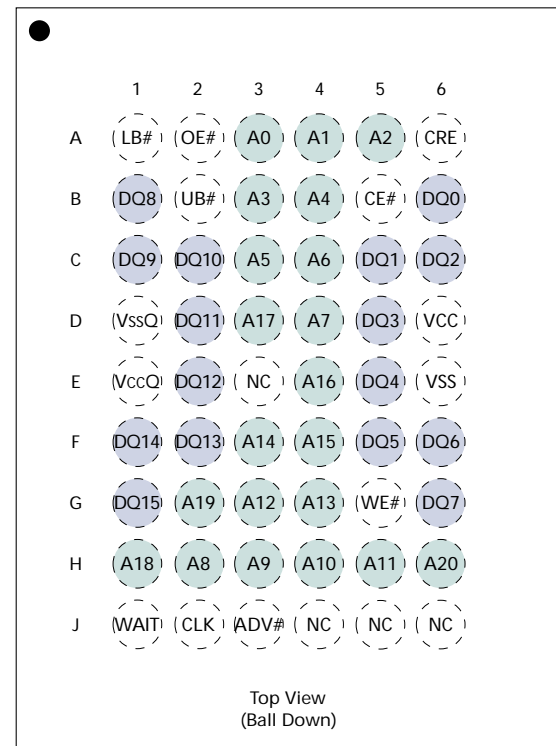
GB

-70

8

1

Figure 1: 54-Ball VFBGA Ball Assignment



Options (Continued)

Designator

- Standby power
 - Standard
- Operating temperature range
 - Wireless (–30°C to +85°C)
 - Industrial (–40°C to +85°C)

None

WT¹

IT

Notes: 1. –30°C exceeds the CellularRAM Workgroup 1.0 specification of –25°C.

Part Number Example:

MT45W2MW16BGB-701WT



Table of Contents

| | |
|--|----|
| Features | 1 |
| Options | 1 |
| General Description | 5 |
| Functional Block Diagrams | 6 |
| Ball Descriptions | 7 |
| Bus Operations | 8 |
| Part Numbering Information | 10 |
| Valid Part Number Combinations | 10 |
| Device Marking | 10 |
| Functional Description | 11 |
| Power-Up Initialization | 11 |
| Bus Operating Modes | 11 |
| Asynchronous Mode | 11 |
| Page Mode READ Operation | 12 |
| Burst Mode Operation | 13 |
| Mixed-Mode Operation | 16 |
| WAIT Operation | 16 |
| LB#/UB# Operation | 16 |
| Low-Power Operation | 19 |
| Standby Mode Operation | 19 |
| Temperature-Compensated Refresh | 19 |
| Partial-Array Refresh | 19 |
| Deep Power-Down Operation | 19 |
| Configuration Registers | 20 |
| Access Using CRE | 20 |
| Software Access to the Configuration Register | 24 |
| Bus Configuration Register | 26 |
| Burst Length (BCR[2:0]) Default = Continuous Burst | 27 |
| Burst Wrap (BCR[3]) Default = Burst No Wrap (Within Burst Length) | 27 |
| Output Impedance (BCR[5]) Default = Outputs Use Full Drive Strength | 28 |
| WAIT Configuration (BCR[8]) Default = WAIT Transitions One Clock Before Data Valid/Invalid | 28 |
| WAIT Polarity (BCR[10]) Default = WAIT Active HIGH | 29 |
| Latency Counter (BCR[13:11]) Default = Three-Clock Latency | 29 |
| Operating Mode (BCR[15]) Default = Asynchronous Operation | 29 |
| Refresh Configuration Register | 31 |
| Partial-Array Refresh (RCR[2:0]) Default = Full Array Refresh | 31 |
| Deep Power-Down (RCR[4]) Default = DPD Disabled | 32 |
| Page Mode Operation (RCR[7]) Default = Disabled | 32 |
| Electrical Characteristics | 32 |
| Maximum and Typical Standby Currents | 34 |
| Timing Requirements | 36 |
| Timing Diagrams | 40 |
| Package Dimensions | 60 |
| Revision History | 61 |

List of Figures

| | | |
|------------|---|----|
| Figure 1: | 54-Ball VFBGA Ball Assignment | 1 |
| Figure 2: | Functional Block Diagram – 2 Meg x 16 | 6 |
| Figure 3: | Part Number Chart | 10 |
| Figure 4: | Power-Up Initialization Timing | 11 |
| Figure 5: | READ Operation (ADV = LOW) | 12 |
| Figure 6: | WRITE Operation (ADV = LOW) | 12 |
| Figure 7: | Page Mode READ Operation (ADV = LOW) | 13 |
| Figure 8: | Burst Mode READ (4-Word Burst) | 14 |
| Figure 9: | Burst Mode WRITE (4-Word Burst) | 15 |
| Figure 10: | Wired-OR WAIT Configuration | 16 |
| Figure 11: | Refresh Collision During READ Operation | 17 |
| Figure 12: | Refresh Collision During WRITE Operation | 18 |
| Figure 13: | Asynchronous Mode Configuration Register WRITE followed by READ ARRAY Operation | 20 |
| Figure 14: | Synchronous Mode Configuration Register WRITE followed by READ ARRAY Operation | 21 |
| Figure 15: | Asynchronous Mode Configuration Register READ followed by READ ARRAY Operation | 22 |
| Figure 16: | Synchronous Mode Configuration Register READ followed by READ ARRAY Operation | 23 |
| Figure 17: | Load Configuration Register | 24 |
| Figure 18: | Read Configuration Register | 25 |
| Figure 19: | Bus Configuration Register Definition | 26 |
| Figure 20: | WAIT Configuration (BCR[8] = 0) | 28 |
| Figure 21: | WAIT Configuration (BCR[8] = 1) | 28 |
| Figure 22: | WAIT Configuration During Burst Operation | 29 |
| Figure 23: | Latency Counter | 30 |
| Figure 24: | Refresh Configuration Register Mapping | 31 |
| Figure 25: | Typical Refresh Current vs. Temperature | 34 |
| Figure 26: | AC Input/Output Reference Waveform | 35 |
| Figure 27: | Output Load Circuit | 35 |
| Figure 28: | Initialization Period | 39 |
| Figure 29: | Asynchronous READ | 40 |
| Figure 30: | Asynchronous READ Using ADV# | 41 |
| Figure 31: | Page Mode READ | 42 |
| Figure 32: | Single-Access Burst READ Operation | 43 |
| Figure 33: | 4-Word Burst READ Operation | 44 |
| Figure 34: | READ Burst Suspend | 45 |
| Figure 35: | Output Delay in Continuous Burst READ with BCR[8] = 0 for End-of-Row Condition | 46 |
| Figure 36: | CE#-Controlled Asynchronous WRITE | 47 |
| Figure 37: | LB#/UB#-Controlled Asynchronous WRITE | 48 |
| Figure 38: | WE#-Controlled Asynchronous WRITE | 49 |
| Figure 39: | Asynchronous WRITE Using ADV# | 50 |
| Figure 40: | Burst WRITE Operation | 51 |
| Figure 41: | Output Delay in Continuous Burst WRITE with BCR[8] = 0 for End-of-Row Condition | 52 |
| Figure 42: | Burst WRITE Followed by Burst READ | 53 |
| Figure 43: | Asynchronous WRITE Followed by Burst READ | 54 |
| Figure 44: | Asynchronous WRITE Followed by Burst READ with ADV# LOW | 55 |
| Figure 45: | Burst READ followed by Asynchronous WRITE (WE#-Controlled) | 56 |
| Figure 46: | Burst READ followed by Asynchronous WRITE Using ADV# | 57 |
| Figure 47: | Asynchronous WRITE followed by Asynchronous READ with ADV# LOW | 58 |
| Figure 48: | Asynchronous WRITE followed by Asynchronous READ | 59 |
| Figure 49: | 54-Ball VFBGA | 60 |

List of Tables

| | | |
|-----------|---|----|
| Table 1: | VFBGA Ball Descriptions | 7 |
| Table 2: | Bus Operations: Asynchronous Mode | 8 |
| Table 3: | Bus Operations: Burst Mode | 9 |
| Table 4: | Sequence and Burst Length | 27 |
| Table 5: | Latency Configuration | 29 |
| Table 6: | 32Mb Address Patterns for PAR (RCR[4] = 1) | 32 |
| Table 7: | Absolute Maximum Ratings | 32 |
| Table 8: | Electrical Characteristics and Operating Conditions | 33 |
| Table 9: | Partial-Array Refresh Specifications and Conditions | 34 |
| Table 10: | Deep Power-Down Specifications | 35 |
| Table 11: | Capacitance | 35 |
| Table 12: | Asynchronous READ Cycle Timing Requirements | 36 |
| Table 13: | Burst READ Cycle Timing Requirements | 37 |
| Table 14: | Asynchronous WRITE Cycle Timing Requirements | 38 |
| Table 15: | Burst WRITE Cycle Timing Requirements | 39 |
| Table 16: | Initialization Timing Parameters | 39 |

General Description

Micron® CellularRAM™ is a high-speed, CMOS PSRAM memory developed for low-power, portable applications. The MT45W2MW16BGB is a 32Mb DRAM core device organized as 2 Meg x 16 bits. This device includes an industry-standard burst mode Flash interface that dramatically increases READ/WRITE bandwidth compared with other low-power SRAM or Pseudo SRAM offerings.

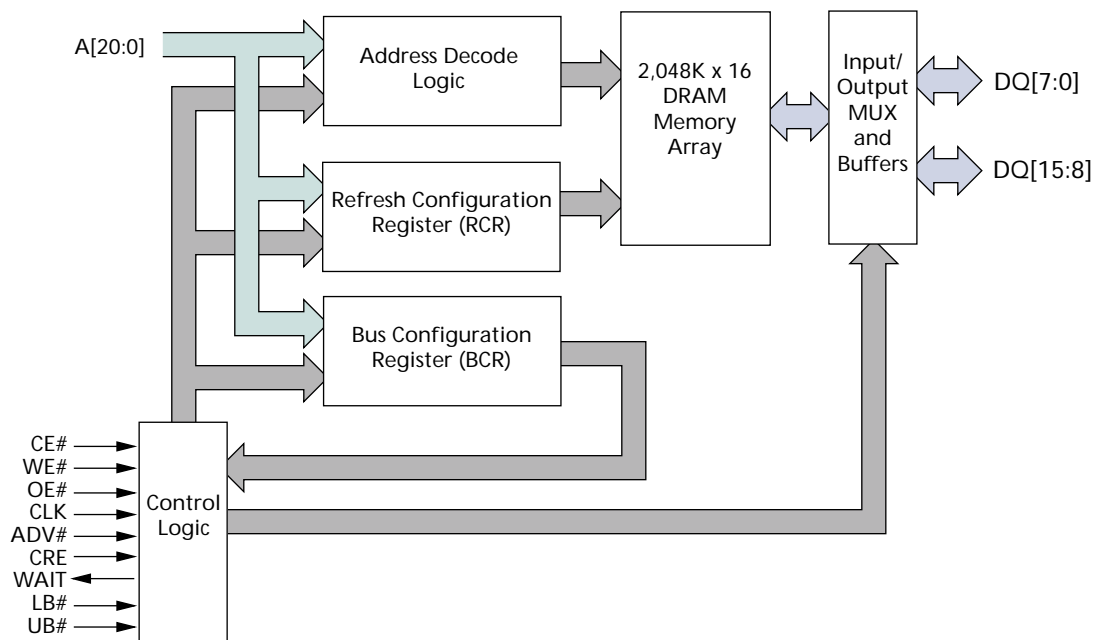
For seamless operation on a burst Flash bus, CellularRAM products incorporate a transparent self-refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device READ/WRITE performance.

Two user-accessible control registers define device operation. The bus configuration register (BCR) defines how the CellularRAM device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation.

Special attention has been focused on standby current consumption during self refresh. CellularRAM products include three system-accessible mechanisms to minimize standby current. Partial-array refresh (PAR) limits refresh to only that part of the DRAM array that contains essential data. Temperature-compensated refresh (TCR) uses an on-chip sensor to adjust the refresh rate to match the device temperature. The refresh rate decreases at lower temperatures to minimize current consumption during standby. Deep power-down (DPD) halts the REFRESH operation altogether and is used when no vital information is stored in the device. These three refresh mechanisms are accessed through the RCR.

Functional Block Diagrams

Figure 2: Functional Block Diagram – 2 Meg x 16



Note: Functional block diagrams illustrate simplified device operation. See ball description table, bus operations tables, and timing diagrams for detailed information.

Ball Descriptions

Table 1: VFBGA Ball Descriptions

| VFBGA Assignment | Symbol | Type | Description |
|--|----------|--------------|---|
| H6, G2, H1, D3, E4, F4, F3, G4, G3, H5, H4, H3, H2, D4, C4, C3, B4, B3, A5, A4, A3 | A[20:0] | Input | Address inputs: Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. The address lines are also used to define the value to be loaded into the BCR or the RCR. |
| J3 | ADV# | Input | Address valid: Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV# during asynchronous READ and WRITE operations. ADV# can be held LOW during asynchronous READ and WRITE operations. |
| B5 | CE# | Input | Chip enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby or deep power-down mode. |
| J2 | CLK | Input | Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV# is active. CLK must be static LOW or HIGH during asynchronous access READ and WRITE operations and during PAGE READ ACCESS operations. |
| A6 | CRE | Input | Configuration register enable: When CRE is HIGH, WRITE operations load the RCR or BCR, and READ operations access either the RCR or the BCR. |
| A1 | LB# | Input | Lower byte enable: DQ[7:0]. |
| A2 | OE# | Input | Output enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled. |
| B2 | UB# | Input | Upper byte enable: DQ[15:8]. |
| G5 | WE# | Input | WRITE enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is a WRITE to either a configuration register or the memory array. |
| G1, F1, F2, E2, D2, C2, C1, B1, G6, F6, F5, E5, D5, C6, C5, B6 | DQ[15:0] | Input/Output | Data inputs/outputs. |
| J1 | WAIT | Output | Wait: Provides data-valid feedback during burst READ and WRITE operations. The signal is gated by CE#. WAIT is used to arbitrate collisions between REFRESH and READ/WRITE operations. WAIT is asserted when a burst crosses a row boundary. WAIT is also used to mask the delay associated with opening a new internal page. WAIT is asserted and should be ignored during asynchronous and page mode operations. WAIT is High-Z when CE# is HIGH. |
| E3, J4, J5, J6 | NC | – | Not internally connected. |
| D6 | Vcc | Supply | Device power supply (1.7–1.95V): Power supply for device core operation. |
| E1 | VccQ | Supply | I/O power supply (1.7–3.6V): Power supply for input/output buffers. |
| E6 | Vss | Supply | Vss must be connected to ground. |
| D1 | VssQ | Supply | VssQ must be connected to ground. |

Note: The CLK and ADV# inputs can be tied to Vss if the device is always operating in asynchronous or page mode. WAIT will be asserted but should be ignored during asynchronous and page mode operations.






Bus Operations

Table 2: Bus Operations: Asynchronous Mode

| Mode | Power | CLK ¹ | ADV# | CE# | OE# | WE# | CRE | LB#/UB# | WAIT ² | DQ[15:0] ³ | Notes |
|------------------------------|-----------------|------------------|------|-----|-----|-----|-----|---------|-------------------|-----------------------|-------|
| READ | Active | L | L | L | L | H | L | L | Low-Z | Data-Out | 4 |
| WRITE | Active | L | L | L | X | L | L | L | Low-Z | Data-In | 4 |
| Standby | Standby | L | X | H | X | X | L | X | High-Z | High-Z | 5, 6 |
| No operation | Idle | L | X | L | X | X | L | X | Low-Z | X | 4, 6 |
| Configuration register WRITE | Active | L | L | L | H | L | H | X | Low-Z | High-Z | |
| Configuration register READ | Active | L | L | L | H | H | H | X | Low-Z | Config. reg. out | 8 |
| DPD | Deep power-down | L | X | H | X | X | X | X | High-Z | High-Z | 7 |

- Notes:
1. CLK must be LOW during asynchronous READ and asynchronous WRITE modes, and to achieve standby power during standby and DPD modes. CLK must be static (HIGH or LOW) during burst suspend.
 2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
 3. When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.
 4. The device will consume active power in this mode whenever addresses are changed.
 5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
 6. VIN = VccQ or 0V; all device balls must be static (unswitched) in order to achieve standby current.
 7. DPD is maintained until RCR is reconfigured.
 8. CRE-controlled reading of the configuration register is supported for this device, though it is not an official CellularRAM 1.0 feature.

Table 3: Bus Operations: Burst Mode

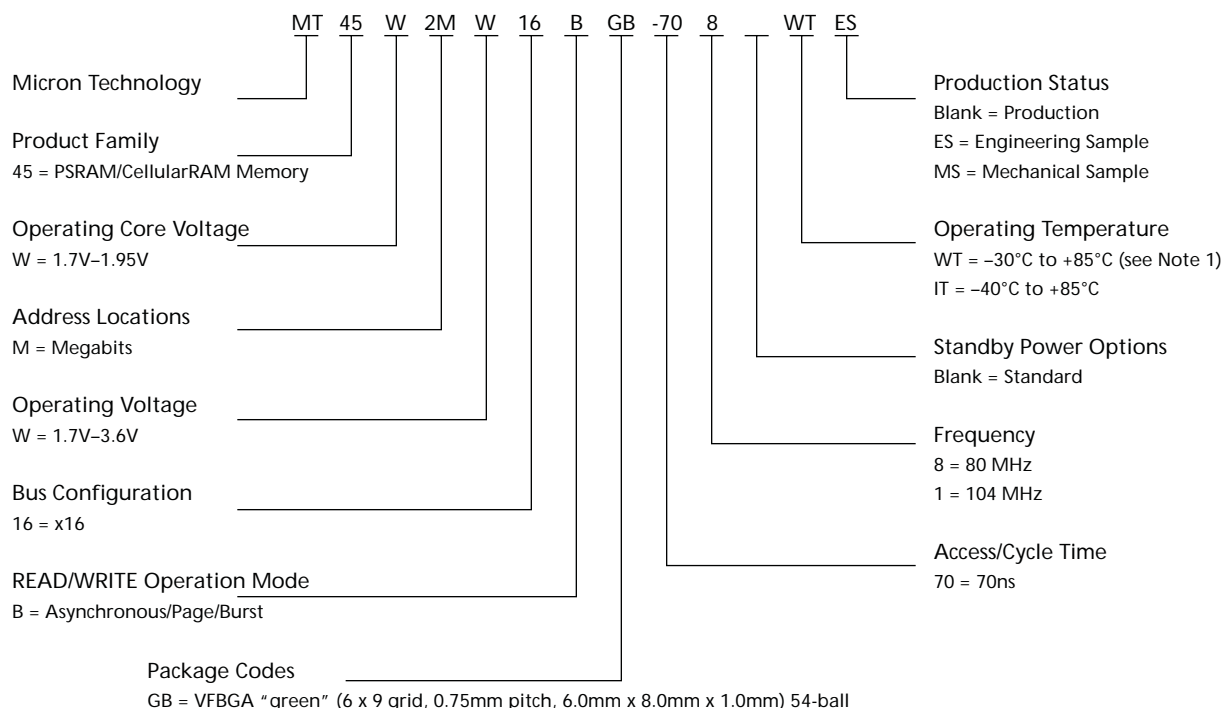
| Mode | Power | CLK ¹ | ADV# | CE# | OE# | WE# | CRE | LB#/ UB# | WAIT ² | DQ[15:0] ³ | Notes |
|------------------------------|-----------------|---|------|-----|-----|-----|-----|-------------|-------------------|-----------------------|-------|
| Asynchronous READ | Active | L | L | L | L | H | L | L | Low-Z | Data-Out | 4 |
| Asynchronous WRITE | Active | L | L | L | X | L | L | L | Low-Z | Data-In | 4 |
| Standby | Standby | L | X | H | X | X | L | X | High-Z | High-Z | 5, 6 |
| No operation | Idle | L | X | L | X | X | L | X | Low-Z | X | 4, 6 |
| Initial burst READ | Active |  | L | L | X | H | L | L | Low-Z | X | 4, 8 |
| Initial burst WRITE | Active |  | L | L | H | L | L | X | Low-Z | X | 4, 8 |
| Burst continue | Active |  | H | L | X | X | X | L | Low-Z | Data-In or Data-Out | 4, 8 |
| Burst suspend | Active | X | X | L | H | X | L | X | Low-Z | High-Z | 4, 8 |
| Configuration register WRITE | Active |  | L | L | H | L | H | X | Low-Z | High-Z | 8 |
| Configuration register READ | Active |  | L | L | H | H | H | X | Low-Z | Config. reg. out Z | 8, 9 |
| DPD | Deep power-down | L | X | H | X | X | X | X | High-Z | High-Z | 7 |

- Notes:
1. CLK must be LOW during asynchronous READ and asynchronous WRITE modes, and to achieve standby power during standby and DPD modes. CLK must be static (HIGH or LOW) during burst suspend.
 2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
 3. When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.
 4. The device will consume active power in this mode whenever addresses are changed.
 5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
 6. VIN = VccQ or 0V; all device balls must be static (unswitched) in order to achieve standby current.
 7. DPD is maintained until RCR is reconfigured.
 8. Burst mode operation is initialized through the bus configuration register (BCR[15]).
 9. This device supports CRE-controlled configuration register READS. This feature is not an official CellularRAM 1.0 feature.

Part Numbering Information

Micron CellularRAM devices are available in several different configurations and densities (see Figure 3).

Figure 3: Part Number Chart



Notes: 1. -30°C exceeds the CellularRAM Workgroup 1.0 specification of -25°C.

Valid Part Number Combinations

After building the part number from the part numbering chart, visit the Micron Web site at www.micron.com/psram to verify that the part number is offered and valid. If the device required is not on this list, contact the factory.

Device Marking

Due to the size of the package, the Micron standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a five-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site, <http://www.micron.com/decoder>. To view the location of the abbreviated mark on the device, refer to customer service note, CSN-11, "Product Mark/Label," at www.micron.com/csn.

Functional Description

In general, the MT45W2MW16BGB devices are high-density alternatives to SRAM and Pseudo SRAM products, popular in low-power, portable applications.

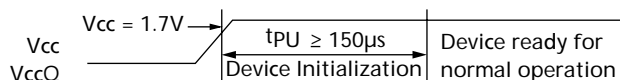
The MT45W2MW16BGB contains a 33,554,432-bit DRAM core organized as 2,097,152 addresses by 16 bits. This device implements the same high-speed bus interface found on burst mode Flash products.

The CellularRAM bus interface supports both asynchronous and burst mode transfers. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous READ protocol.

Power-Up Initialization

CellularRAM products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the BCR and the RCR with their default settings (see Figure 19 on page 26 and Figure 24 on page 31). VCC and VCCQ must be applied simultaneously. When they reach a stable level at or above 1.7V, the device will require 150 μ s to complete its self-initialization process. During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

Figure 4: Power-Up Initialization Timing



Bus Operating Modes

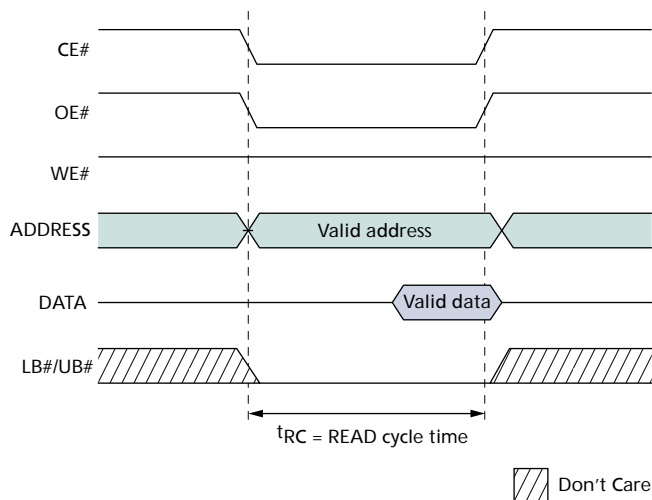
The MT45W2MW16BGB CellularRAM products incorporate a burst mode interface found on Flash products targeting low-power, wireless applications. This bus interface supports asynchronous, page mode, and burst mode READ and WRITE transfers. The specific interface supported is defined by the value loaded into the bus configuration register. Page mode is controlled by the refresh configuration register (RCR[7]).

Asynchronous Mode

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry-standard SRAM control bus (CE#, OE#, WE#, LB#/UB#). READ operations are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH (see Figure 5 on page 12). Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations occur when CE#, WE#, and LB#/UB# are driven LOW (see Figure 6 on page 12). During asynchronous WRITE operations, the OE# level is a "Don't Care," and WE# will override OE#. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB#, whichever occurs first. Asynchronous operations (page mode disabled) can either use the ADV input to latch the address, or ADV can be driven LOW during the entire READ/WRITE operation.

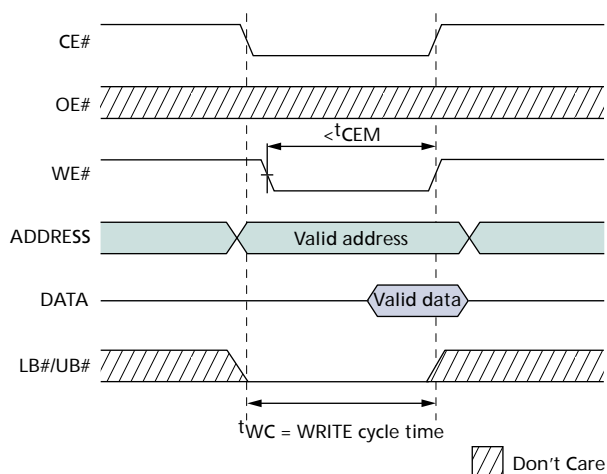
During asynchronous operation, the CLK input must be held static LOW or HIGH. WAIT will be driven while the device is enabled and its state should be ignored. WE# LOW time must be limited to t_{CEM} .

Figure 5: READ Operation (ADV = LOW)



Note: ADV must remain LOW for page mode operation.

Figure 6: WRITE Operation (ADV = LOW)



Page Mode READ Operation

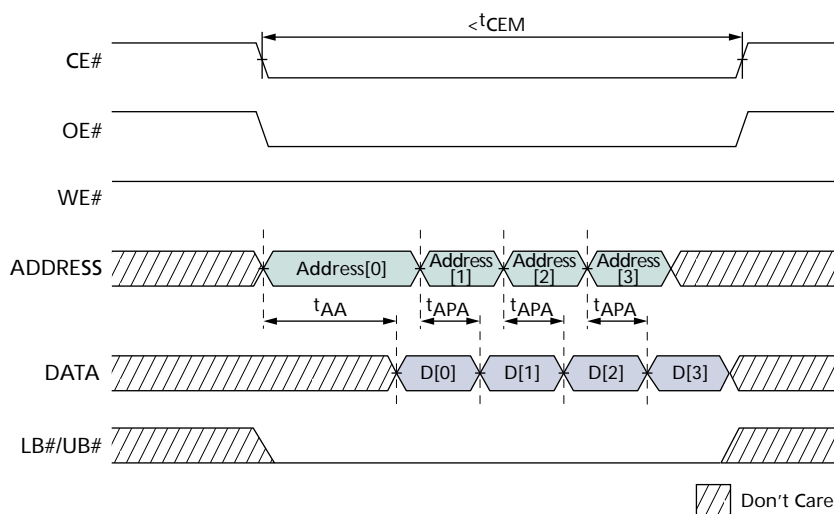
Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous READ access is performed, then adjacent addresses can be read quickly by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Any change in addresses A[4] or higher will initiate a new t_{AA} access time. Figure 7 on page 13 shows the timing for a page mode access.

Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality.

During asynchronous page mode operation, the CLK input must be held static LOW or HIGH. CE# must be driven HIGH upon completion of a page mode access. WAIT will be driven while the device is enabled and its state should be ignored. Page mode is enabled by setting RCR[7] to HIGH. ADV must be driven LOW during all page mode READ accesses.

The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than t_{CEM} .

Figure 7: Page Mode READ Operation (ADV = LOW)



Burst Mode Operation

Burst mode operations enable high-speed synchronous READ and WRITE operations. Burst operations consist of a multi-clock sequence that must be performed in an ordered fashion. After CE# goes LOW, the address to access is latched on the next rising edge of CLK that ADV# is LOW. During this first clock rising edge, WE# indicates whether the operation is going to be a READ (WE# = HIGH, Figure 8 on page 14) or WRITE (WE# = LOW, Figure 9 on page 15).

The size of a burst can be specified in the BCR as either fixed-length or continuous. Fixed-length bursts consist of 4, 8, or 16 words. Continuous bursts have the ability to start at a specified address and burst through the entire memory. The latency count stored in the BCR defines the number of clock cycles that elapse before the initial data value is transferred between the processor and CellularRAM device.

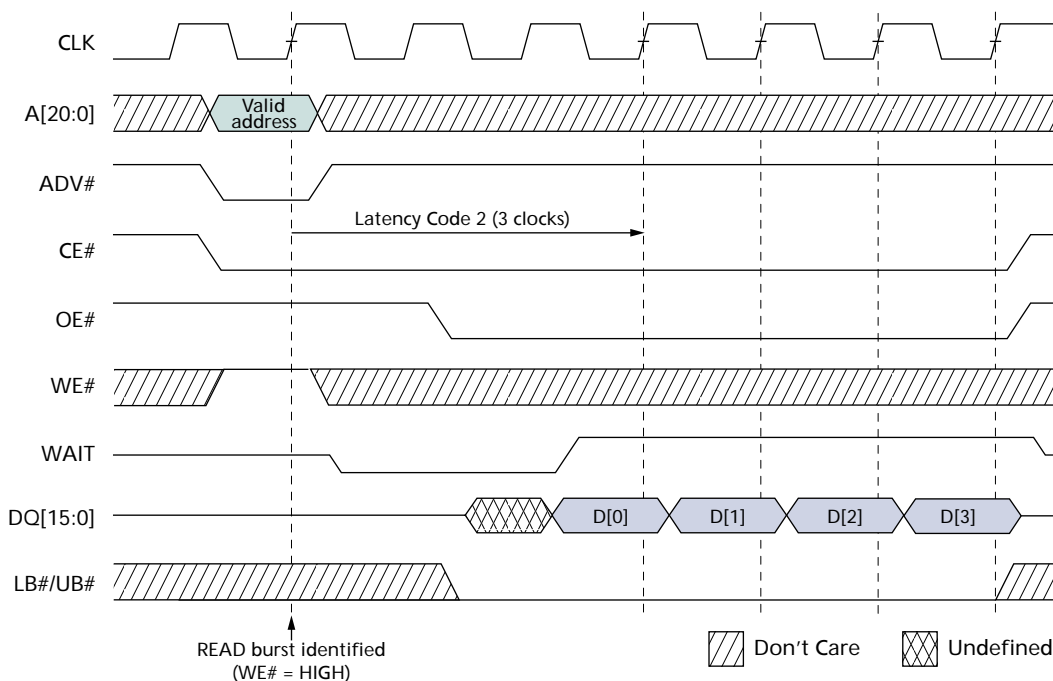
The WAIT output will be asserted as soon as CE# goes LOW and will be de-asserted to indicate when data is to be transferred into (or out of) the memory. WAIT will again be asserted if the burst crosses the boundary between 128-word rows. Once the CellularRAM device has restored the previous row's data and accessed the next row, WAIT will be de-asserted and the burst can continue (see Figure 35 on page 46).

The processor can access other devices without incurring the timing penalty of the initial latency for a new burst by suspending burst mode. Bursts are suspended by stopping CLK. CLK can be stopped HIGH or LOW. If another device will use the data bus while the burst is suspended, OE# should be taken HIGH to disable the CellularRAM outputs; otherwise, OE# can remain LOW. Note that the WAIT output will continue to be

active, and as a result no other devices should directly share the WAIT connection to the controller. To continue the burst sequence, OE# is taken LOW, then CLK is restarted after valid data is available on the bus.

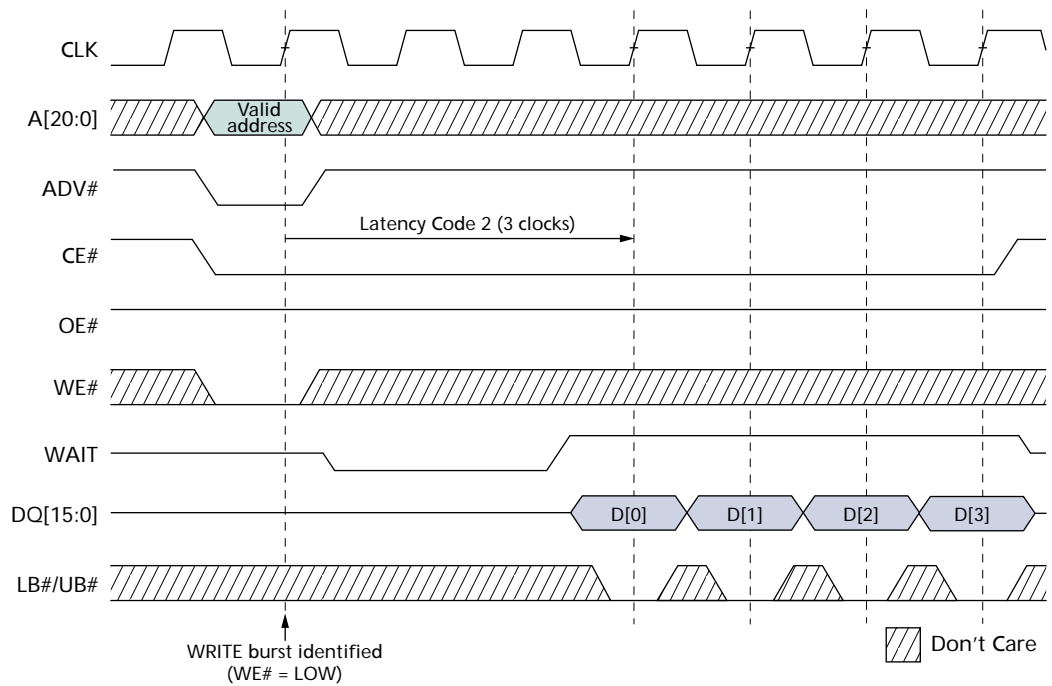
The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than t_{CEM} unless row boundaries are crossed at least every t_{CEM} . If a burst suspension will cause CE# to remain LOW for longer than t_{CEM} , CE# should be taken HIGH and the burst restarted with a new CE# LOW/ADV# LOW cycle.

Figure 8: Burst Mode READ (4-Word Burst)



Note: Non-default BCR settings: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

Figure 9: Burst Mode WRITE (4-Word Burst)



Note: Non-default BCR settings: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

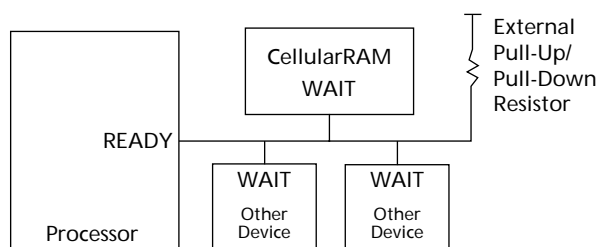
Mixed-Mode Operation

The device can support a combination of synchronous READ and asynchronous WRITE operations when the BCR is configured for synchronous operation. The asynchronous WRITE operation requires that the clock (CLK) be held static LOW or HIGH during the entire sequence. The ADV# signal can be used to latch the target address, or it can remain LOW during the entire WRITE operation. CE# must return HIGH when transitioning between mixed-mode operations. Note that the t_{CKA} period is the same as a READ or WRITE cycle. This time is required to ensure adequate refresh. Mixed-mode operation facilitates a seamless interface to legacy burst mode Flash memory controllers (see Figure 43 on page 54).

WAIT Operation

The WAIT output on a CellularRAM device is typically connected to a shared, system-level WAIT signal (see Figure 10). The shared WAIT signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus.

Figure 10: Wired-OR WAIT Configuration



After a READ or WRITE operation has been initiated, WAIT goes active to indicate that the CellularRAM device requires additional time before data can be transferred. For READ operations, WAIT will remain active until valid data is output from the device. For WRITE operations, WAIT will indicate to the memory controller when data will be accepted into the CellularRAM device. When WAIT transitions to an inactive state, the data burst will progress on successive clock edges.

During a burst cycle, CE# must remain asserted until the first data is valid. Bringing CE# HIGH during this initial latency may cause data corruption.

The WAIT output also performs an arbitration role when a READ or WRITE operation is launched while an on-chip refresh is in progress. If a collision occurs, WAIT is asserted for additional clock cycles until the refresh has completed (see Figures 11 and 12 on page 18). When the REFRESH operation has completed, the READ or WRITE operation will continue normally.

WAIT is also asserted when a continuous READ or WRITE burst crosses a row boundary. The WAIT assertion allows time for the new row to be accessed and permits any pending REFRESH operations to be performed.

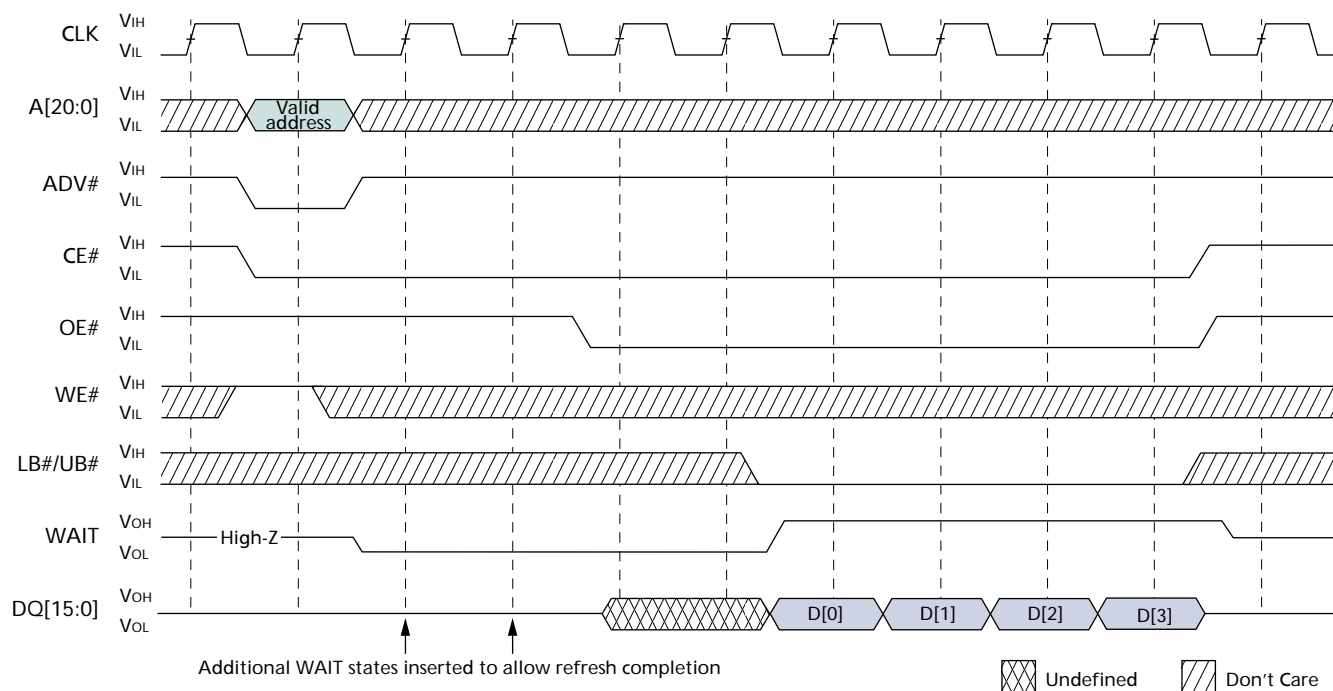
LB#/UB# Operation

The LB# enable and UB# enable signals support byte-wide data transfers. During READ operations, the enabled byte(s) are driven onto the DQ. The DQ associated with a disabled byte are put into a High-Z state during a READ operation. During WRITE opera-

tions, any disabled bytes will not be transferred to the RAM array and the internal value will remain unchanged. During an asynchronous WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first.

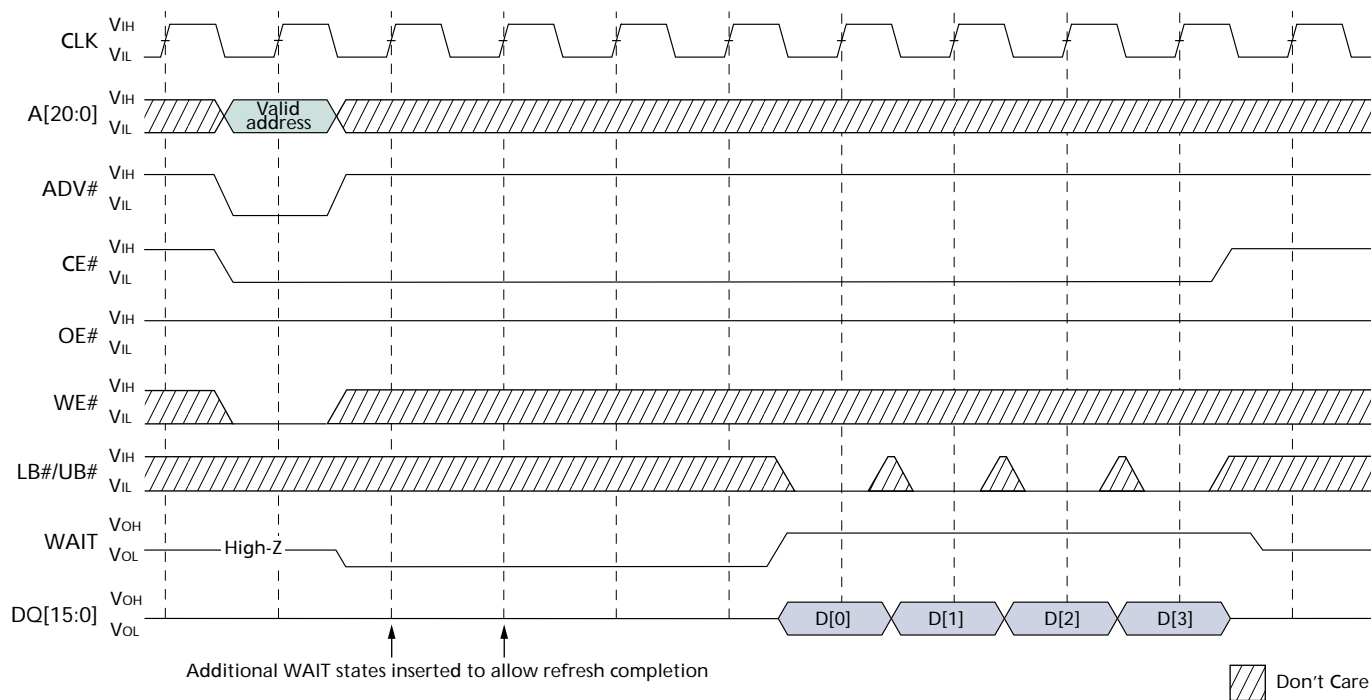
When both the LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as CE# remains LOW.

Figure 11: Refresh Collision During READ Operation



Note: Non-default BCR settings: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

Figure 12: Refresh Collision During WRITE Operation



Note: Non-default BCR settings: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

Low-Power Operation

Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM REFRESH operation. Standby operation occurs when CE# is HIGH.

The device will enter a reduced power state upon completion of a READ or WRITE operation or when the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

Temperature-Compensated Refresh

Temperature-compensated refresh (TCR) allows for adequate refresh at different temperatures. This CellularRAM device includes an on-chip temperature sensor that continually adjusts the refresh rate according to the operating temperature.

Partial-Array Refresh

Partial-array refresh (PAR) restricts REFRESH operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Table 6 on page 32). READ and WRITE operations to address ranges receiving refresh will not be affected. Data stored in addresses not receiving refresh will become corrupted. When re-enabling additional portions of the array, the new portions are available immediately upon writing to the RCR.

Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled by rewriting the RCR, the CellularRAM device will require 150 μ s to perform an initialization procedure before normal operations can resume. During this 150 μ s period, the current consumption will be higher than the specified standby levels, but considerably lower than the active current specification.

DPD cannot be enabled or disabled by writing to the RCR using the software access sequence; the RCR should be accessed using CRE instead.

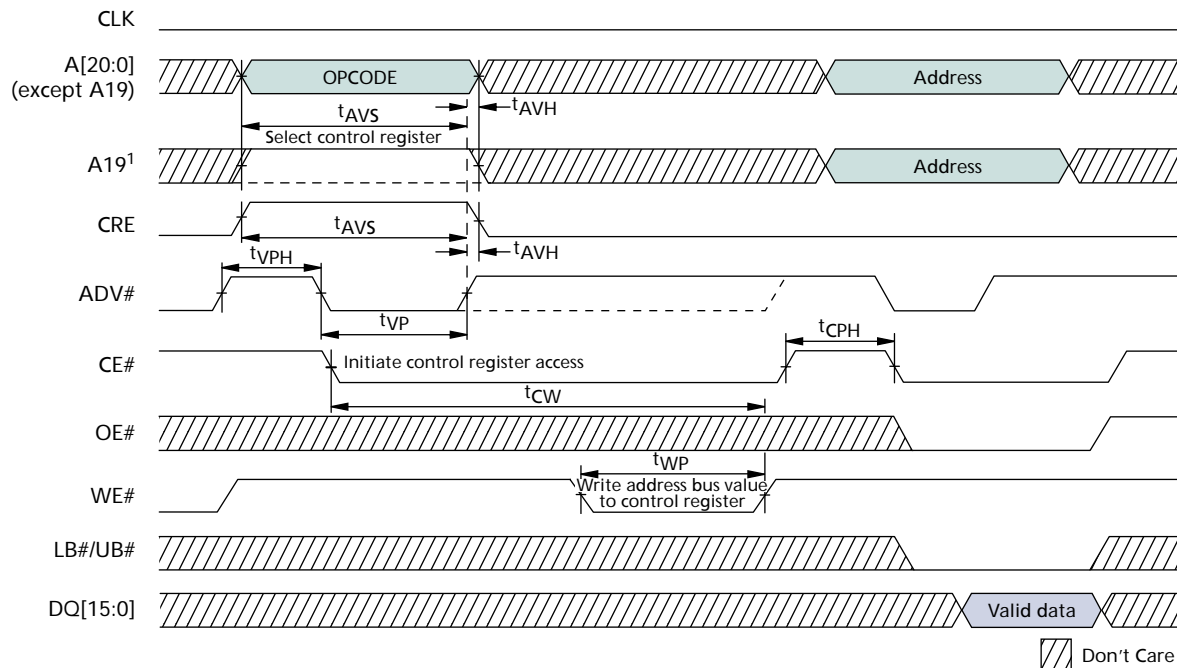
Configuration Registers

Two user-accessible configuration registers define the device operation. The bus configuration register (BCR) defines how the CellularRAM interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated any time the devices are operating in a standby state.

Access Using CRE

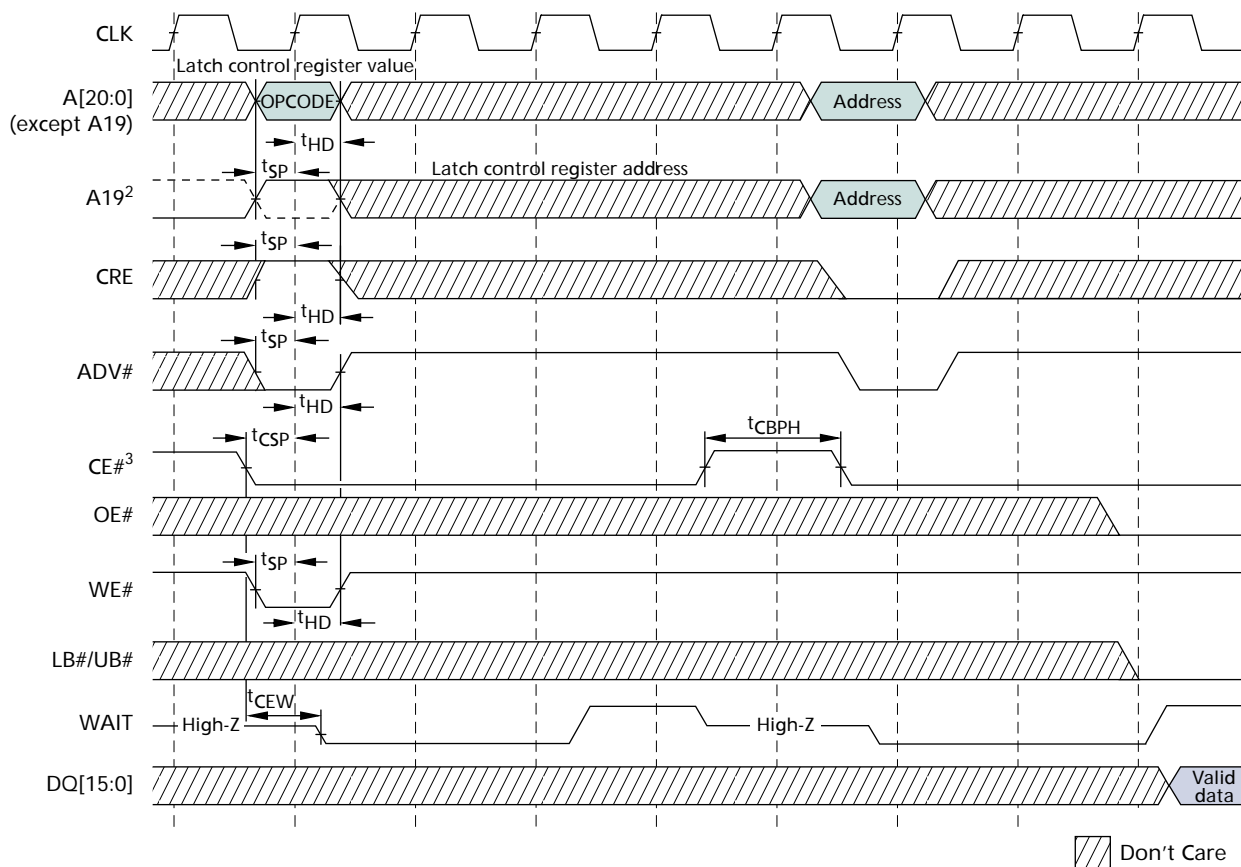
The configuration registers are loaded using either a synchronous or an asynchronous WRITE operation when the configuration register enable (CRE) input is HIGH (see Figure 13, and Figure 14 on page 21). When CRE is LOW, a READ or WRITE operation will access the memory array. The register values are placed on address pins A[19:0]. In an asynchronous WRITE, the values are latched into the configuration register on the rising edge of ADV#, CE#, or WE#, whichever occurs first; LB# and UB# are "Don't Care." The BCR is accessed when A[19] is HIGH; the RCR is accessed when A[19] is LOW. For READs, address inputs other than A19 are "Don't Care," and register bits 15:0 are output on DQ[15:0].

Figure 13: Asynchronous Mode Configuration Register WRITE followed by READ ARRAY Operation



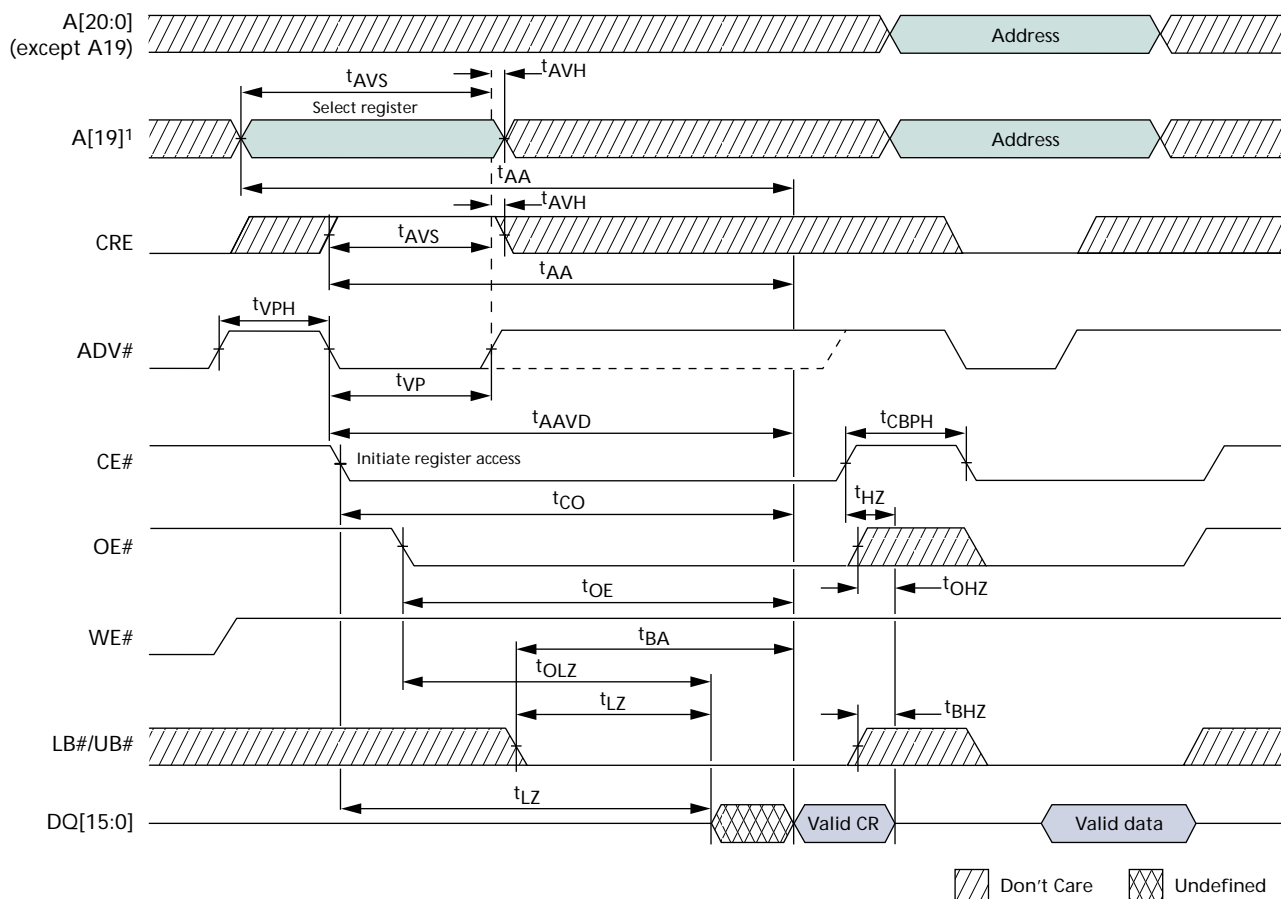
Notes: 1. A[19] = LOW to load RCR, HIGH to load BCR.

Figure 14: Synchronous Mode Configuration Register WRITE followed by READ ARRAY Operation



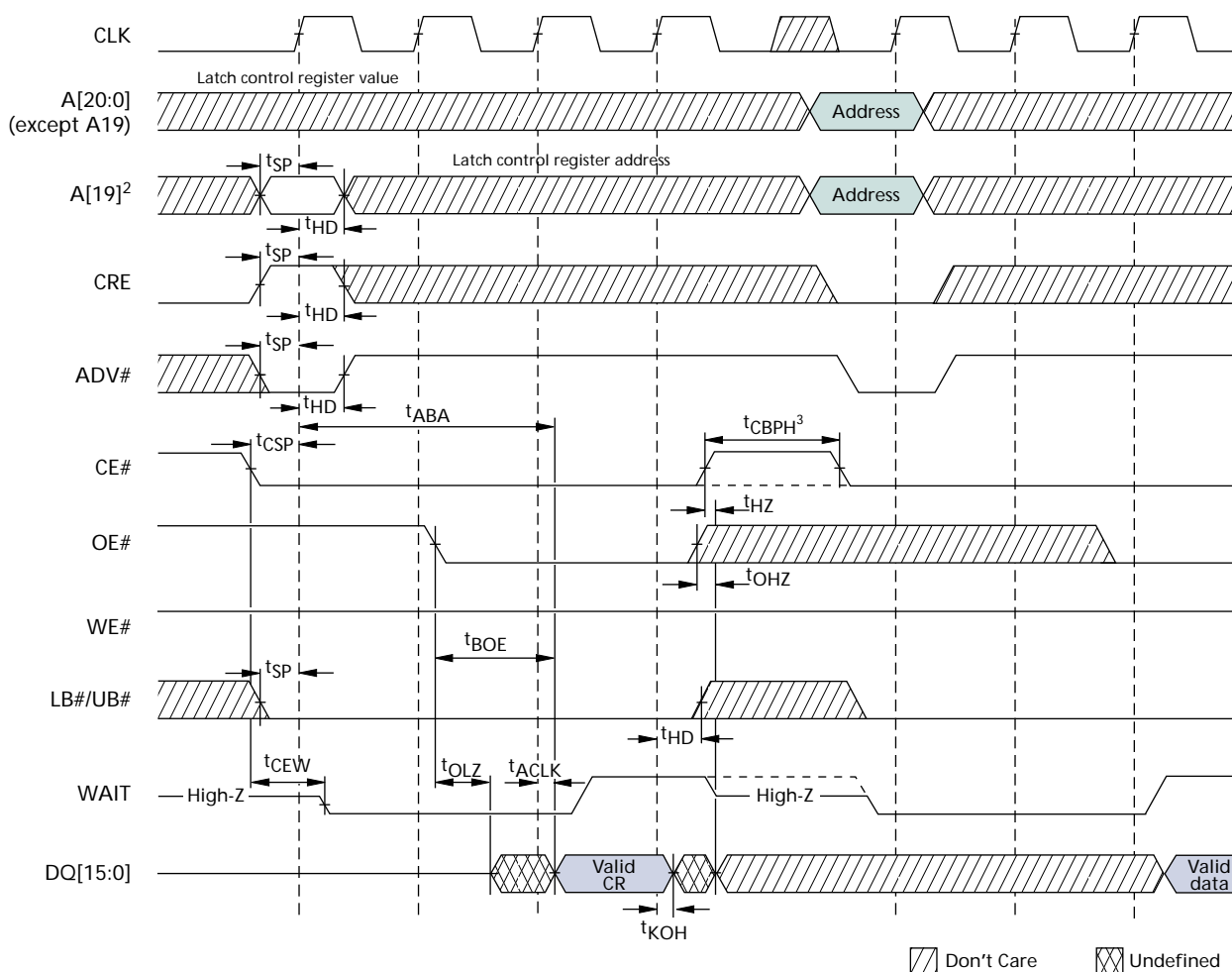
- Notes:
1. Non-default BCR settings for CR WRITE in synchronous mode followed by READ ARRAY operation: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.
 2. A[19] = LOW to load RCR, HIGH to load BCR.
 3. CE# must remain LOW to complete a burst-of-one WRITE. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

Figure 15: Asynchronous Mode Configuration Register READ followed by READ ARRAY Operation



Notes: 1. A[19] = LOW to read RCR, HIGH to read BCR.

Figure 16: Synchronous Mode Configuration Register READ followed by READ ARRAY Operation



- Notes:
1. Non-default BCR settings for synchronous mode register READ followed by READ ARRAY operation: latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.
 2. A[19] = LOW to read RCR, HIGH to read BCR.
 3. CE# must remain LOW to complete a burst-of-one READ. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

Software Access to the Configuration Register

Software access of the configuration registers uses a sequence of asynchronous READ and asynchronous WRITE operations. The contents of the configuration registers can be read or modified using the software sequence.

The configuration registers are loaded using a four-step sequence consisting of two asynchronous READ operations followed by two asynchronous WRITE operations (see Figure 17). The READ sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure 18 on page 25). Note that a third READ cycle of the highest address will cancel the access sequence until a different address is read.

The address used during all READ and WRITE operations is the highest address of the CellularRAM device being accessed (1FFFFFFh for 32Mb); the content at this address is not changed by using this sequence.

The data value presented during the third operation (WRITE) in the sequence defines whether the BCR or the RCR is to be accessed. If the data is 0000h, the sequence will access the RCR; if the data is 0001h, the sequence will access the BCR. During the fourth operation, DQ[15:0] transfer data into or out of bits 15–0 of the configuration registers.

The use of the software sequence does not affect the ability to perform the standard (CRE-controlled) method of loading the configuration registers. However, the software nature of this access mechanism eliminates the need for the control register enable (CRE) pin. If the software mechanism is used, the CRE pin can simply be tied to VSS. The port line often used for CRE control purposes is no longer required.

Software access of the RCR should not be used to enter or exit DPD.

Figure 17: Load Configuration Register

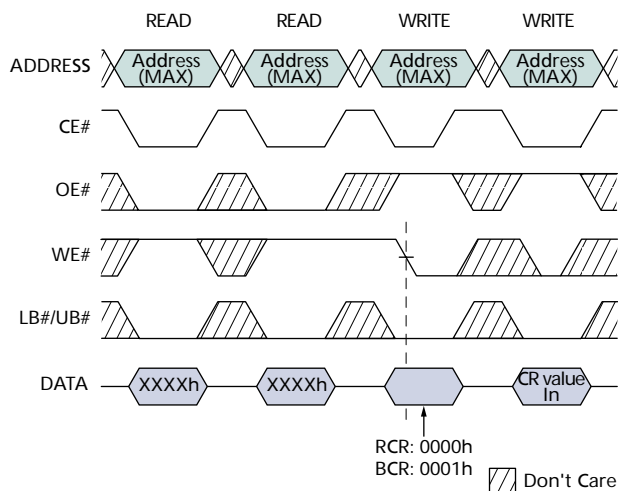
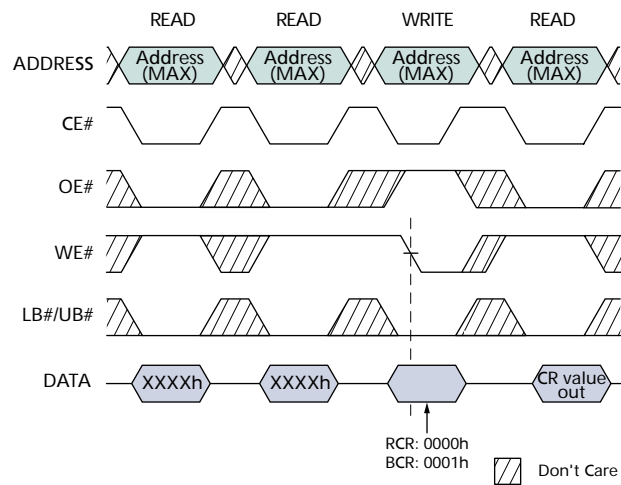


Figure 18: Read Configuration Register

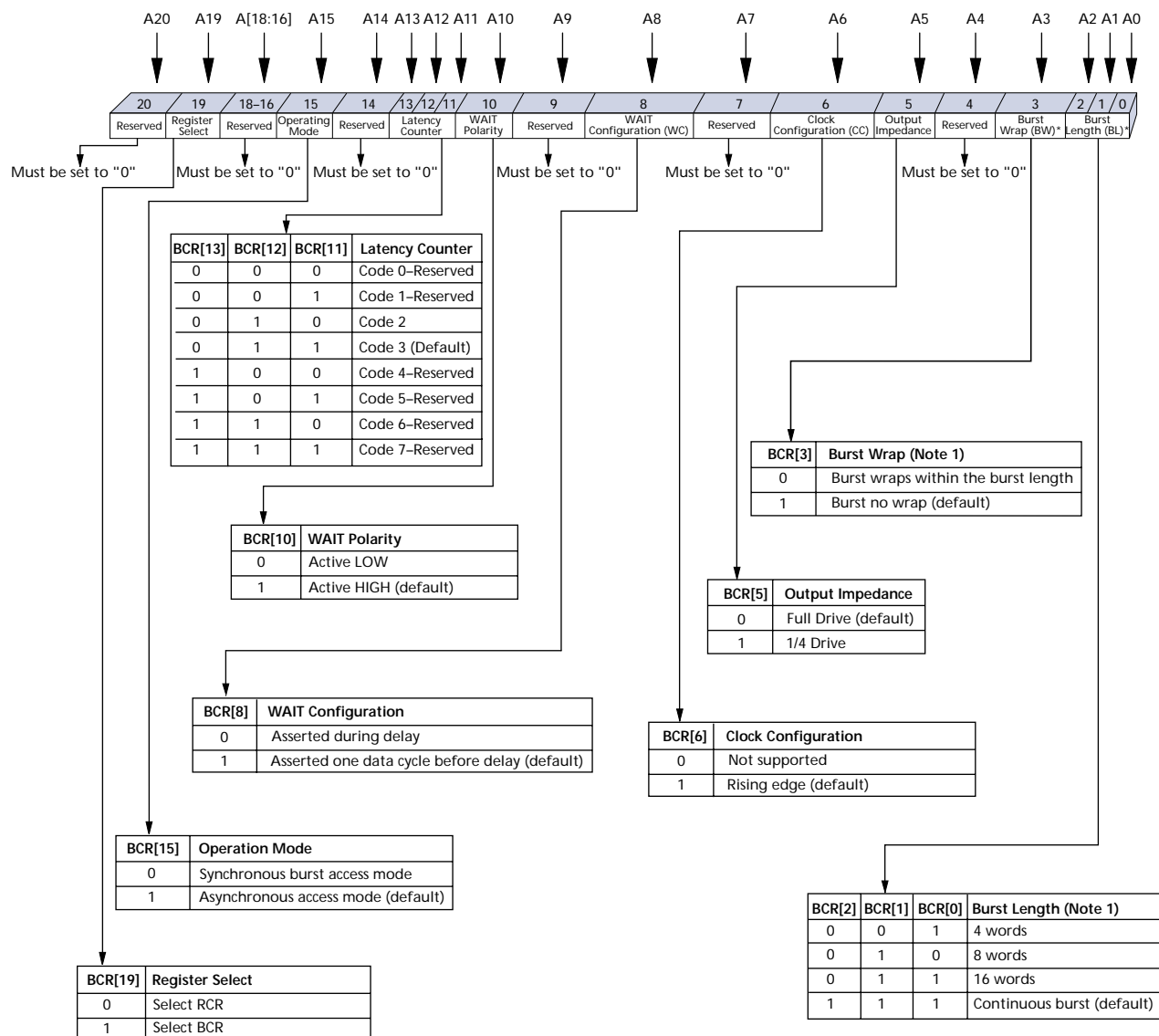


Bus Configuration Register

The BCR defines how the CellularRAM device interacts with the system memory bus. Page mode operation is enabled by a bit contained in the RCR. Figure 19 describes the control bits in the BCR. At power-up, the BCR is set to 9D4Fh.

The BCR is accessed using CRE and A[19] HIGH or through the configuration register software sequence with DQ = 0001h on the third cycle.

Figure 19: Bus Configuration Register Definition



Note: All burst WRITES are continuous.

Table 4: Sequence and Burst Length

| Burst Wrap | | Starting Address | 4-Word Burst Length | 8-Word Burst Length | 16-Word Burst length | Continuous Burst |
|------------|------|------------------|---------------------|----------------------|---|--------------------------|
| BCR[3] | Wrap | (Decimal) | Linear | Linear | Linear | Linear |
| 0 | Yes | 0 | 0-1-2-3 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15 | 0-1-2-3-4-5-6-... |
| | | 1 | 1-2-3-0 | 1-2-3-4-5-6-7-0 | 1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0 | 1-2-3-4-5-6-7-... |
| | | 2 | 2-3-0-1 | 2-3-4-5-6-7-0-1 | 2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1 | 2-3-4-5-6-7-8-... |
| | | 3 | 3-0-1-2 | 3-4-5-6-7-0-1-2 | 3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2 | 3-4-5-6-7-8-9-... |
| | | 4 | | 4-5-6-7-0-1-2-3 | 4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3 | 4-5-6-7-8-9-10-... |
| | | 5 | | 5-6-7-0-1-2-3-4 | 5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4 | 5-6-7-8-9-10-11-... |
| | | 6 | | 6-7-0-1-2-3-4-5 | 6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5 | 6-7-8-9-10-11-12-... |
| | | 7 | | 7-0-1-2-3-4-5-6 | 7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6 | 7-8-9-10-11-12-13-... |
| | | ... | | | ... | ... |
| | | 14 | | | 14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13 | 14-15-16-17-18-19-20-... |
| 1 | No | 0 | 0-1-2-3 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15 | 0-1-2-3-4-5-6-... |
| | | 1 | 1-2-3-4 | 1-2-3-4-5-6-7-8 | 1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-16 | 1-2-3-4-5-6-7-... |
| | | 2 | 2-3-4-5 | 2-3-4-5-6-7-8-9 | 2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17 | 2-3-4-5-6-7-8-... |
| | | 3 | 3-4-5-6 | 3-4-5-6-7-8-9-10 | 3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18 | 3-4-5-6-7-8-9-... |
| | | 4 | | 4-5-6-7-8-9-10-11 | 4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19 | 4-5-6-7-8-9-10-... |
| | | 5 | | 5-6-7-8-9-10-11-12 | 5-6-7-8-9-10-11-12-13-14-15-16-17-18-19-20 | 5-6-7-8-9-10-11-... |
| | | 6 | | 6-7-8-9-10-11-12-13 | 6-7-8-9-10-11-12-13-14-15-16-17-18-19-20-21 | 6-7-8-9-10-11-12-... |
| | | 7 | | 7-8-9-10-11-12-13-14 | 7-8-9-10-11-12-13-14-15-16-17-18-19-20-21-22 | 7-8-9-10-11-12-13-... |
| | | ... | | | ... | ... |
| | | 14 | | | 14-15-16-17-18-19-20-21-22-23-24-25-26-27-28-29 | 14-15-16-17-18-19-20-... |
| | | 15 | | | 15-16-17-18-19-20-21-22-23-24-25-26-27-28-29-30 | 15-16-17-18-19-20-21-... |

Burst Length (BCR[2:0]) Default = Continuous Burst

Burst lengths define the number of words the device outputs during a burst READ operation. The device supports a burst length of 4, 8, or 16 words. The device can also be set in continuous burst mode where data is output sequentially without regard to address boundaries; the internal address wraps to 000000h if the device is read past the last address. WRITE bursts are always performed using continuous burst mode.

Burst Wrap (BCR[3]) Default = Burst No Wrap (Within Burst Length)

The burst wrap option determines if a 4-, 8-, or 16-word burst READ wraps within the burst length or steps through sequential addresses. If the wrap option is not enabled, the device outputs data from sequential addresses without regard to burst boundaries; the internal address wraps to 000000h if the device is read past the last address.

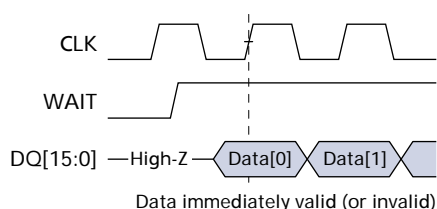
Output Impedance (BCR[5]) Default = Outputs Use Full Drive Strength

The output driver strength can be altered to adjust for different data bus loading scenarios. The reduced-strength option should be more than adequate in stacked chip (Flash + CellularRAM) environments when there is a dedicated memory bus. The reduced-drive-strength option is included to minimize noise generated on the data bus during READ operations. Normal output impedance should be selected when using a discrete CellularRAM device in a more heavily loaded data bus environment. Partial drive is approximately one-quarter full drive strength. Outputs are configured at full drive strength during testing.

WAIT Configuration (BCR[8]) Default = WAIT Transitions One Clock Before Data Valid/Invalid

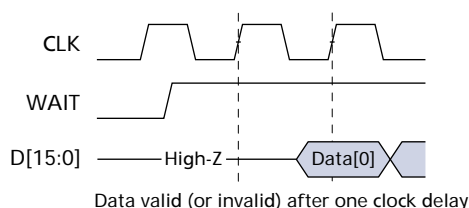
The WAIT configuration bit is used to determine when WAIT transitions between the asserted and the de-asserted state with respect to valid data presented on the data bus. The memory controller will use the WAIT signal to coordinate data transfer during synchronous READ and WRITE operations. When BCR[8] = 0, data will be valid or invalid on the clock edge immediately after WAIT transitions to the de-asserted or asserted state, respectively (see Figures 20 and 22). When BCR[8] = 1, the WAIT signal transitions one clock period prior to the data bus going valid or invalid (see Figures 21 and 22).

Figure 20: WAIT Configuration (BCR[8] = 0)



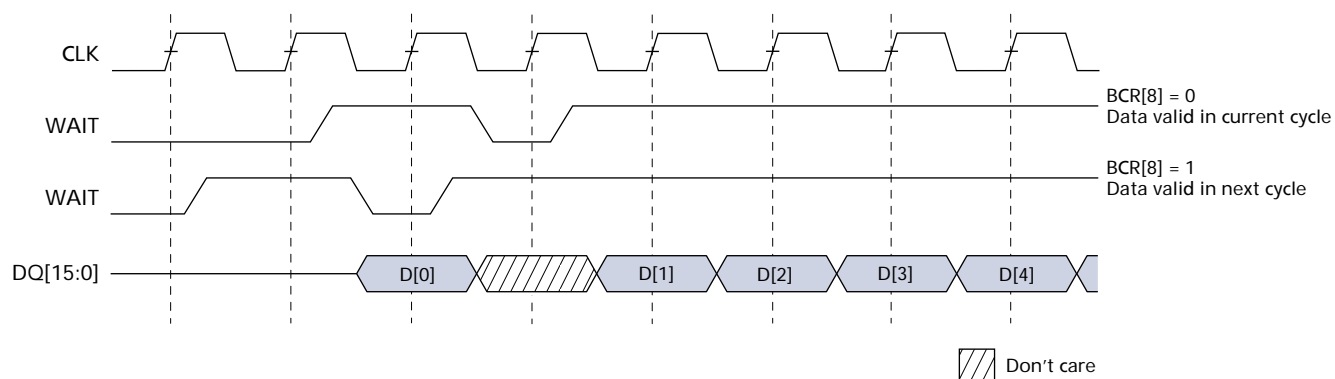
Note: Data valid/invalid immediately after WAIT transitions (BCR[8] = 0). See Figure 22 on page 29.

Figure 21: WAIT Configuration (BCR[8] = 1)



Note: Valid/invalid data delayed for one clock after WAIT transitions (BCR[8] = 1). See Figure 22 on page 29.

Figure 22: WAIT Configuration During Burst Operation



Note: Non-default BCR setting for WAIT during BURST operation: WAIT active LOW.

WAIT Polarity (BCR[10]) Default = WAIT Active HIGH

The WAIT polarity bit indicates whether an asserted WAIT output should be HIGH or LOW. This bit will determine whether the WAIT signal requires a pull-up or pull-down resistor to maintain the de-asserted state.

Latency Counter (BCR[13:11]) Default = Three-Clock Latency

The latency counter bits determine how many clocks occur between the beginning of a READ or WRITE operation and the first data value transferred. Only latency code 2 (3 clocks) or latency code 3 (4 clocks) is allowed (see Table 5 and Figure 23).

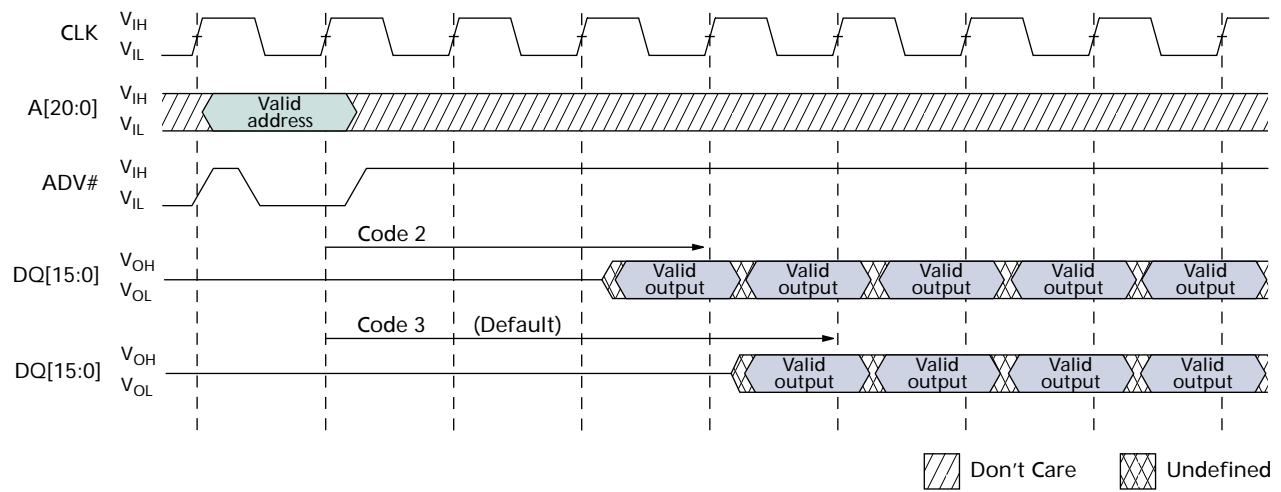
Operating Mode (BCR[15]) Default = Asynchronous Operation

The operating mode bit selects either synchronous burst operation or the default asynchronous mode of operation.

Table 5: Latency Configuration

| Latency Configuration Code | Max Input CLK Frequency (MHz) | |
|----------------------------|-------------------------------|--------------|
| | 104 MHz | 80 MHz |
| 2 (3 clocks) | 66 (15ns) | 53 (18.75ns) |
| 3 (4 clocks) – default | 104 (9.62ns) | 80 (12.50ns) |

Figure 23: Latency Counter



Refresh Configuration Register

The refresh configuration register (RCR) defines how the CellularRAM device performs its transparent self refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Page mode control is also embedded into the RCR. Figure 24 describes the control bits used in the RCR. At power-up, the RCR is set to 0010h.

The RCR is accessed using CRE and A[19] LOW; or through the configuration register software access sequence with DQ = 0000h on the third cycle (see “Configuration Registers” on page 20.)

Partial-Array Refresh (RCR[2:0]) Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Table 6 on page 32).

Figure 24: Refresh Configuration Register Mapping

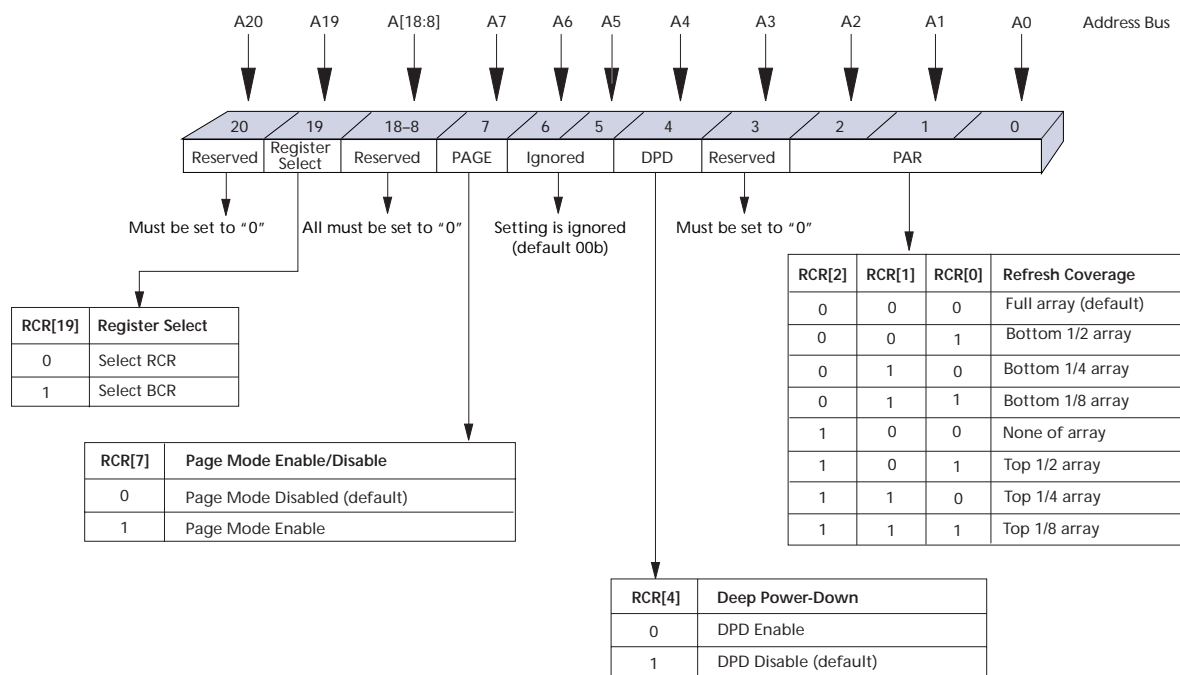


Table 6: 32Mb Address Patterns for PAR (RCR[4] = 1)

| RCR[2] | RCR[1] | RCR[0] | Active Section | Address Space | Size | Density |
|--------|--------|--------|--------------------|------------------|------------|---------|
| 0 | 0 | 0 | Full die | 000000h–1FFFFFFh | 2 Meg x 16 | 32Mb |
| 0 | 0 | 1 | One-half of die | 000000h–0FFFFFFh | 1 Meg x 16 | 16Mb |
| 0 | 1 | 0 | One-quarter of die | 000000h–07FFFFh | 512K x 16 | 8Mb |
| 0 | 1 | 1 | One-eighth of die | 000000h–03FFFFh | 256K x 16 | 4Mb |
| 1 | 0 | 0 | None of die | 0 | 0 Meg x 16 | 0Mb |
| 1 | 0 | 1 | One-half of die | 100000h–1FFFFFFh | 1 Meg x 16 | 16Mb |
| 1 | 1 | 0 | One-quarter of die | 180000h–1FFFFFFh | 512K x 16 | 8Mb |
| 1 | 1 | 1 | One-eighth of die | 1C0000h–1FFFFFFh | 256K x 16 | 4Mb |

Deep Power-Down (RCR[4]) Default = DPD Disabled

The deep power-down bit enables and disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume.

Deep power-down is enabled when RCR[4] = 0, and remains enabled until RCR[4] is set to “1.” DPD should not be enabled or disabled with the software access sequence; instead, use CRE to access the RCR.

Page Mode Operation (RCR[7]) Default = Disabled

The page mode operation bit determines whether page mode is enabled for asynchronous READ operations. In the power-up default state, page mode is disabled.

Electrical Characteristics

Table 7: Absolute Maximum Ratings

| Parameter | Rating |
|---|---|
| Voltage to any ball except Vcc, VccQ relative to Vss | –0.5V to (4.0V or VccQ + 0.3V, whichever is less) |
| Voltage on Vcc supply relative to Vss | –0.2V to +2.45V |
| Voltage on VccQ supply relative to Vss | –0.2V to +4.0V |
| Storage temperature (plastic) | –55°C to +150°C |
| Operating temperature (case) | |
| Wireless ¹ | –30°C to +85°C |
| Industrial | –40°C to +85°C |
| Soldering temperature and time 10 seconds (solder ball only) | +260°C |

Notes: 1. –30°C exceeds the CellularRAM Workgroup 1.0 specification of –25°C.

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 8: Electrical Characteristics and Operating Conditions

Wireless temperature¹ ($-30^{\circ}\text{C} < T_C < +85^{\circ}\text{C}$); Industrial temperature ($-40^{\circ}\text{C} < T_C < +85^{\circ}\text{C}$)

| Description | Conditions | Symbol | | Min | Max | Units | Notes |
|----------------------------------|---|-------------------|----------|----------------------|------------------------|-------|-------|
| Supply voltage | | V _{CC} | | 1.7 | 1.95 | V | |
| I/O supply voltage | | V _{CCQ} | | 1.7 | 3.6 | V | |
| Input high voltage | | V _{IH} | | 1.4 | V _{CCQ} + 0.2 | V | 2, 3 |
| Input low voltage | | V _{IL} | | −0.2 | 0.4 | V | 4 |
| Output high voltage | I _{OH} = −0.2mA | V _{OH} | | 0.8 V _{CCQ} | | V | 5 |
| Output low voltage | I _{OL} = +0.2mA | V _{OL} | | | 0.2 V _{CCQ} | V | 5 |
| Input leakage current | V _{IN} = 0 to V _{CCQ} | I _{LI} | | | 1 | μA | |
| Output leakage current | OE# = V _{IH} or chip disabled | I _{LO} | | | 1 | μA | |
| Operating Current | | | | | | | |
| Asynchronous random READ/ WRITE | V _{IN} = V _{CCQ} or 0V Chip enabled; I _{OUT} = 0 | I _{CC1} | −70 | | 20 | mA | 6 |
| | | | | | | | |
| Asynchronous page READ | | I _{CC1P} | −70 | | 15 | mA | 6 |
| | | | | | | | |
| Initial access, burst READ/WRITE | | I _{CC2} | 104 MHz | | 40 | mA | 6 |
| | | | 80 MHz | | 35 | | |
| Continuous burst READ | | I _{CC3R} | 104 MHz | | 25 | mA | 6 |
| | | | 80 MHz | | 18 | | |
| Continuous burst WRITE | | I _{CC3W} | 104 MHz | | 40 | mA | 6 |
| | | | 80 MHz | | 35 | | |
| Standby current | V _{IN} = V _{CCQ} or 0V CE# = V _{CCQ} | I _{SB} | Standard | | 110 | μA | 7 |

- Notes:
1. -30°C exceeds the CellularRAM Workgroup 1.0 specification of -25°C .
 2. Input signals may overshoot to V_{CCQ} + 1.0V for periods less than 2ns during transitions.
 3. V_{IH} (MIN) value is not aligned with CellularRAM work group 1.0 specification of V_{CCQ} - 0.4V.
 4. Input signals may undershoot to V_{SS} - 1.0V for periods less than 2ns during transitions.
 5. BCR[5] = 0b.
 6. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.
 7. I_{SB} (MAX) values measured with PAR set to FULL ARRAY. In order to achieve low standby current, all inputs must be driven to either V_{CCQ} or V_{SS}. I_{SB} might be slightly higher for up to 500ms after power-up, after changes to the PAR array partition, or when entering standby mode.

Maximum and Typical Standby Currents

The following table and figure refer to the maximum and typical standby currents for the MT45W2MW16BGB device. The typical values shown in Figure 25 are measured with the default on-chip temperature sensor control enabled.

Table 9: Partial-Array Refresh Specifications and Conditions

| Description | Conditions | Symbol | | Array Partition | Max | Unit |
|---------------------------------------|---------------------------------|--------|------------------------------------|-----------------|-----|---------------|
| Partial-array refresh standby current | VIN = VccQ or 0V; CE# = VccQ | IPAR | Standard power (no designation) | Full | 110 | μA |
| | | | | 1/2 | 105 | |
| | | | | 1/4 | 95 | |
| | | | | 1/8 | 95 | |
| | | | | 0 | 70 | |

Notes: 1. IPAR (MAX) values measured at 85°C. IPAR might be slightly higher for up to 500ms after changes to the PAR array partition or when entering standby mode. In order to achieve low standby current, all inputs must be driven to either VccQ or Vss.

Figure 25: Typical Refresh Current vs. Temperature

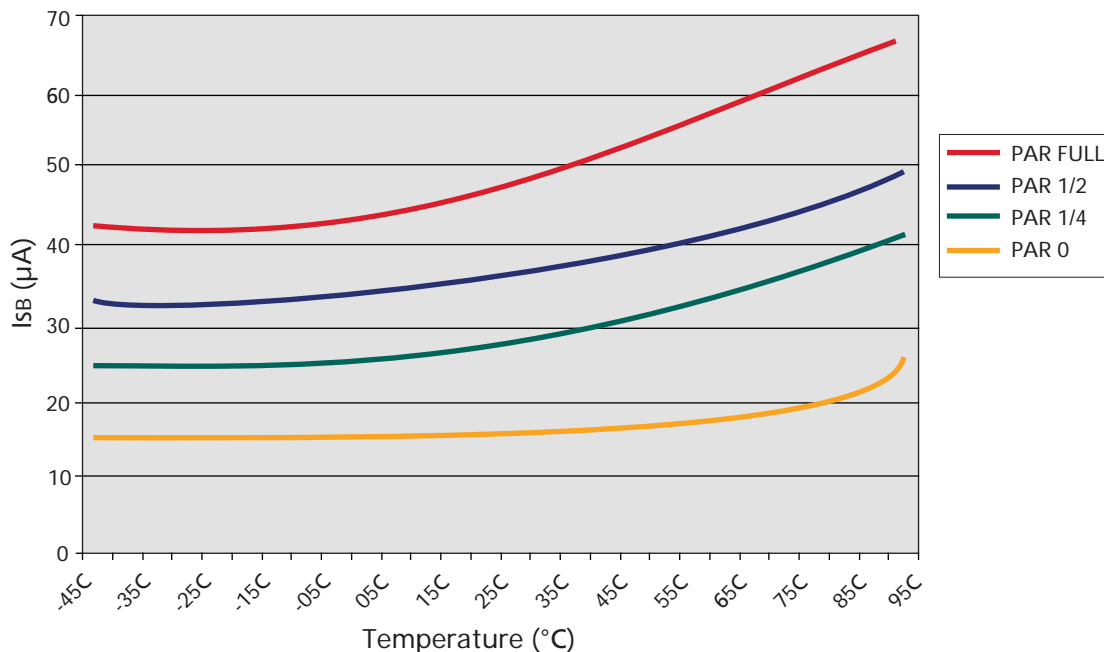


Table 10: Deep Power-Down Specifications

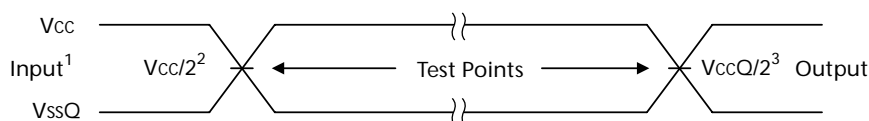
| Description | Conditions | Symbol | Typ | Units |
|-----------------|---|----------|-----|---------|
| Deep power-down | $V_{IN} = V_{CCQ}$ or $0V$; $+25^{\circ}C$ | I_{ZZ} | 10 | μA |

Table 11: Capacitance

| Description | Conditions | Symbol | Min | Max | Units | Notes |
|-------------------------------|--|----------|-----|-----|-------|-------|
| Input capacitance | $T_C = +25^{\circ}C$; $f = 1\text{ MHz}$; $V_{IN} = 0V$ | C_{IN} | 2.0 | 6.5 | pF | [1] |
| Input/output capacitance (DQ) | | C_{IO} | 3.0 | 6.5 | pF | [1] |

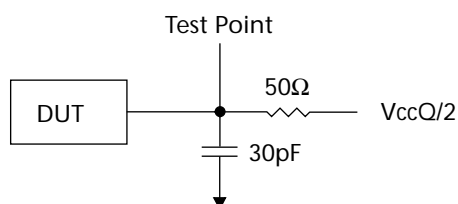
Notes: 1. These parameters are verified in device characterization and are not 100 percent tested.

Figure 26: AC Input/Output Reference Waveform



- Notes:
1. AC test inputs are driven at V_{CCQ} for a logic 1 and V_{SSQ} for a logic 0. Input rise and fall times (10 percent to 90 percent) $< 1.6\text{ ns}$.
 2. Input timing begins at $V_{CC}/2$. Due to the possibility of a difference between V_{CC} and V_{CCQ} , the input test point may not be shown to scale.
 3. Output timing ends at $V_{CCQ}/2$.

Figure 27: Output Load Circuit



Note: All tests are performed with the outputs configured for full drive strength ($BCR[5] = 0b$).

Timing Requirements

Table 12: Asynchronous READ Cycle Timing Requirements

| Parameter ¹ | Symbol | 70ns | | Units | Notes |
|---|------------|------|-----|---------|-------|
| | | Min | Max | | |
| Address access time | t_{AA} | | 70 | ns | |
| ADV# access time | t_{AADV} | | 70 | ns | |
| Page access time | t_{APA} | | 20 | ns | |
| Address hold from ADV# HIGH | t_{AVH} | 5 | | ns | |
| Address setup to ADV# HIGH | t_{AVS} | 5 | | ns | |
| LB#/UB# access time | t_{BA} | | 70 | ns | |
| LB#/UB# disable to DQ High-Z output | t_{BHZ} | | 8 | ns | [2] |
| LB#/UB# enable to Low-Z output | t_{BLZ} | 10 | | ns | [3] |
| Maximum CE# pulse width | t_{CEM} | | 8 | μ s | [4] |
| CE# LOW to WAIT valid | t_{CEW} | 1 | 7.5 | ns | |
| Chip select access time | t_{CO} | | 70 | ns | |
| CE# LOW to ADV# HIGH | t_{CVS} | 10 | | ns | |
| Chip disable to DQ and WAIT High-Z output | t_{HZ} | | 8 | ns | [2] |
| Chip enable to Low-Z output | t_{LZ} | 10 | | ns | [3] |
| Output enable to valid output | t_{OE} | | 20 | ns | |
| Output hold from address change | t_{OH} | 5 | | ns | |
| Output disable to DQ High-Z output | t_{OHZ} | | 8 | ns | [2] |
| Output enable to Low-Z output | t_{OLZ} | 3 | | ns | [3] |
| Page cycle time | t_{PC} | 20 | | ns | |
| READ cycle time | t_{RC} | 70 | | ns | |
| ADV# pulse width LOW | t_{VP} | 10 | | ns | |
| ADV# pulse width HIGH | t_{VPH} | 10 | | ns | |

- Notes:
1. All tests are performed with the outputs configured for full drive strength (BCR[5] = 0b).
 2. Low-Z to High-Z timings are tested with the circuit shown in Figure 27 on page 35. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CCQ}/2$.
 3. High-Z to Low-Z timings are tested with the circuit shown in Figure 27 on page 35. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CCQ}/2$) level toward either V_{OH} or V_{OL} .
 4. Page mode enabled only.

Table 13: Burst READ Cycle Timing Requirements

| Parameter ¹ | Symbol | 104 MHz | | 80 MHz | | Units | Notes |
|---|-------------------|---------|------|--------|------|-------|-------|
| | | Min | Max | Min | Max | | |
| Burst to READ access time | ^t ABA | | 35.9 | | 46.5 | ns | |
| CLK to output delay | ^t ACLK | | 7 | | 9 | ns | |
| Burst OE# LOW to output delay | ^t BOE | | 20 | | 20 | ns | |
| CE# HIGH between subsequent burst and mixed-mode operations | ^t CBPH | 5 | | 5 | | ns | 2 |
| Maximum CE# pulse width | ^t CEM | | 8 | | 8 | μs | |
| CE# LOW to WAIT valid | ^t CEW | 1 | 7.5 | 1 | 7.5 | ns | |
| CLK period | ^t CLK | 9.62 | | 12.5 | | ns | |
| CE# setup time to active CLK edge | ^t CSP | 3 | | 4.5 | | ns | |
| Hold time from active CLK edge | ^t HD | 2 | | 2 | | ns | |
| Chip disable to DQ and WAIT High-Z output | ^t HZ | | 8 | | 8 | ns | 3 |
| CLK rise or fall time | ^t KHKL | | 1.6 | | 1.8 | ns | |
| CLK to WAIT valid | ^t KHTL | | 7 | | 9 | ns | |
| Output HOLD from CLK | ^t KOH | 2 | | 2 | | ns | |
| CLK HIGH or LOW time | ^t KP | 3 | | 4 | | ns | |
| Output disable to DQ High-Z output | ^t OHZ | | 8 | | 8 | ns | 3 |
| Output enable to Low-Z output | ^t OLZ | 3 | | 3 | | ns | 4 |
| Setup time to active CLK edge | ^t SP | 3 | | 3 | | ns | |

- Notes:
1. All tests are performed with the outputs configured for full drive strength (BCR[5] = 0b).
 2. When configured for synchronous mode (BCR[15] = 0), a refresh opportunity must be provided every ^tCEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for greater than 15ns.
 3. Low-Z to High-Z timings are tested with the circuit shown in Figure 27 on page 35. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward V_{CCQ}/2.
 4. High-Z to Low-Z timings are tested with the circuit shown in Figure 27 on page 35. The Low-Z timings measure a 100mV transition away from the High-Z (V_{CCQ}/2) level toward either V_{OH} or V_{OL}.

Table 14: Asynchronous WRITE Cycle Timing Requirements

| Parameter | Symbol | 70ns | | Units | Notes |
|---|-----------|------|-----|-------|-------|
| | | Min | Max | | |
| Address and ADV# LOW setup time | t_{AS} | 0 | | ns | |
| Address hold from ADV# going HIGH | t_{AVH} | 5 | | ns | |
| Address setup to ADV# going HIGH | t_{AVS} | 5 | | ns | |
| Address valid to end of WRITE | t_{AW} | 70 | | ns | |
| LB#/UB# select to end of WRITE | t_{BW} | 70 | | ns | |
| CE# LOW to WAIT valid | t_{CEW} | 1 | 7.5 | ns | |
| Asynchronous address-to-burst transition time | t_{CKA} | 70 | | ns | |
| CE# HIGH between subsequent asynchronous operations | t_{CPH} | 5 | | ns | |
| CE# LOW to ADV# HIGH | t_{CVS} | 10 | | ns | |
| Chip enable to end of WRITE | t_{CW} | 70 | | ns | |
| Data hold from WRITE time | t_{DH} | 0 | | ns | |
| Data WRITE setup time | t_{DW} | 23 | | ns | |
| Chip disable to WAIT High-Z output | t_{HZ} | | 8 | ns | |
| Chip enable to Low-Z output | t_{LZ} | 10 | | ns | 2 |
| End WRITE to Low-Z output | t_{OW} | 5 | | ns | 1 |
| ADV# pulse width | t_{VP} | 10 | | ns | |
| ADV# pulse width HIGH | t_{VPH} | 10 | | ns | |
| ADV# setup to end of WRITE | t_{VS} | 70 | | ns | |
| WRITE cycle time | t_{WC} | 70 | | ns | |
| WRITE to DQ High-Z output | t_{WHZ} | | 8 | ns | 2 |
| WRITE pulse width | t_{WP} | 46 | | ns | 3 |
| WRITE pulse width HIGH | t_{WPH} | 10 | | ns | |
| WRITE recovery time | t_{WR} | 0 | | ns | |

- Notes:
1. High-Z to Low-Z timings are tested with the circuit shown in Figure 27 on page 35. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CCQ/2}$) level toward either V_{OH} or V_{OL} .
 2. Low-Z to High-Z timings are tested with the circuit shown in Figure 27 on page 35. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CCQ/2}$.
 3. WE# LOW time must be limited to t_{CEM} (8 μ s).

Table 15: Burst WRITE Cycle Timing Requirements

| Parameter | Symbol | 104 MHz | | 80 MHz | | Units | Notes |
|---|------------|---------|-----|--------|-----|---------|-------|
| | | Min | Max | Min | Max | | |
| CE# HIGH between subsequent burst and mixed-mode operations | t_{CBPH} | 5 | | 5 | | ns | 1 |
| Maximum CE# pulse width | t_{CEM} | | 8 | | 8 | μs | 1 |
| CE# LOW to WAIT valid | t_{CEW} | 1 | 7.5 | 1 | 7.5 | ns | |
| Clock period | t_{CLK} | 9.62 | | 12.5 | | ns | |
| CE# setup to CLK active edge | t_{CSP} | 3 | | 4.5 | | ns | |
| Hold time from active CLK edge | t_{HD} | 2 | | 2 | | ns | |
| Chip disable to WAIT High-Z output | t_{HZ} | | 8 | | 8 | ns | |
| CLK rise or fall time | t_{KHKL} | | 1.6 | | 1.8 | ns | |
| Clock to WAIT valid | t_{KHTL} | | 7 | | 9 | ns | |
| CLK HIGH or LOW time | t_{KP} | 3 | | 4 | | ns | |
| Setup time to active CLK edge | t_{SP} | 3 | | 3 | | ns | |

Notes: 1. When configured for synchronous mode (BCR[15] = 0), a refresh opportunity must be provided every t_{CEM} . A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for greater than 15ns.

Figure 28: Initialization Period

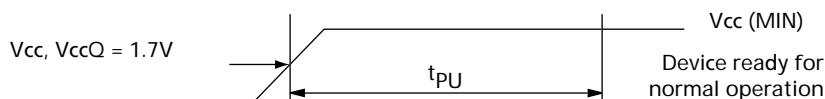


Table 16: Initialization Timing Parameters

| Parameter | Symbol | -70 | | Units |
|--|----------|-----|-----|---------|
| | | Min | Max | |
| Initialization period (required before normal operations) | t_{PU} | 150 | | μs |

Timing Diagrams

Figure 29: Asynchronous READ

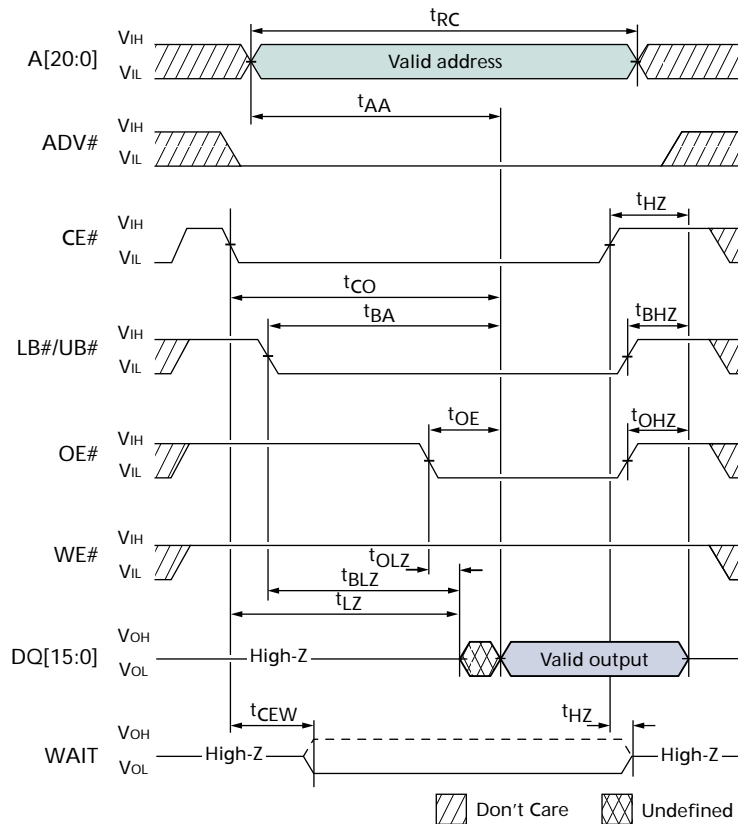


Figure 30: Asynchronous READ Using ADV#

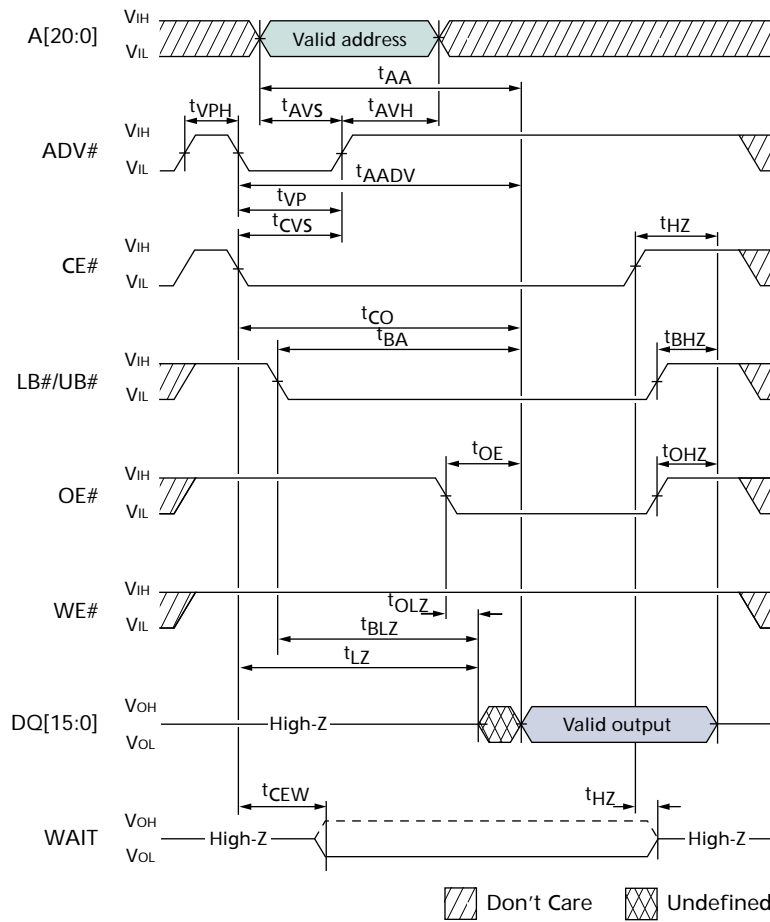


Figure 31: Page Mode READ

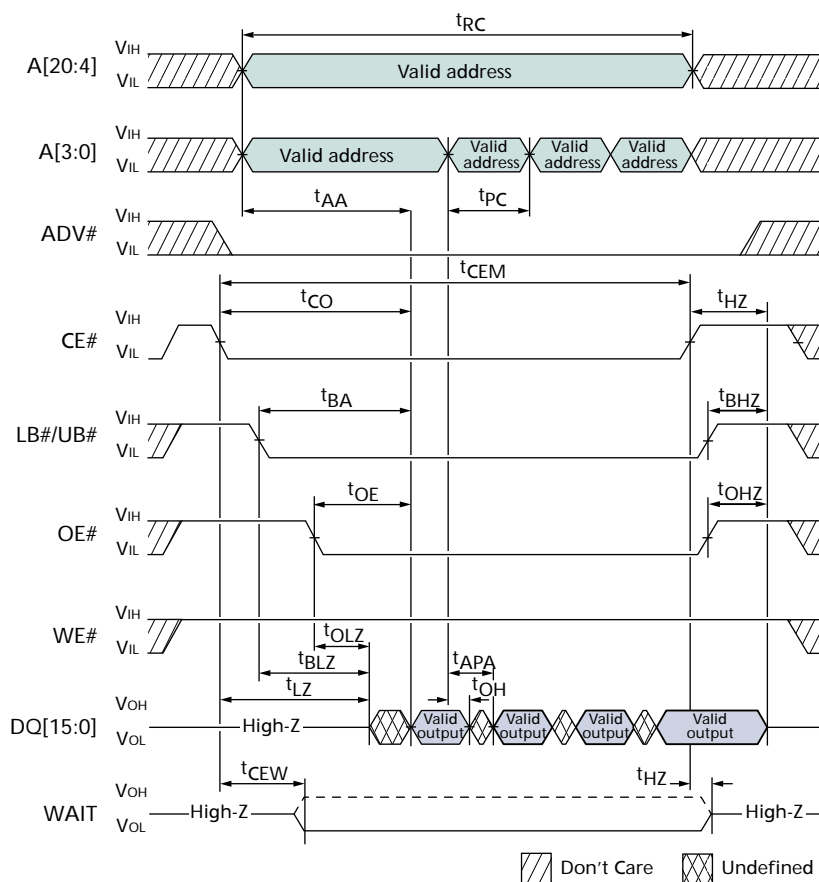
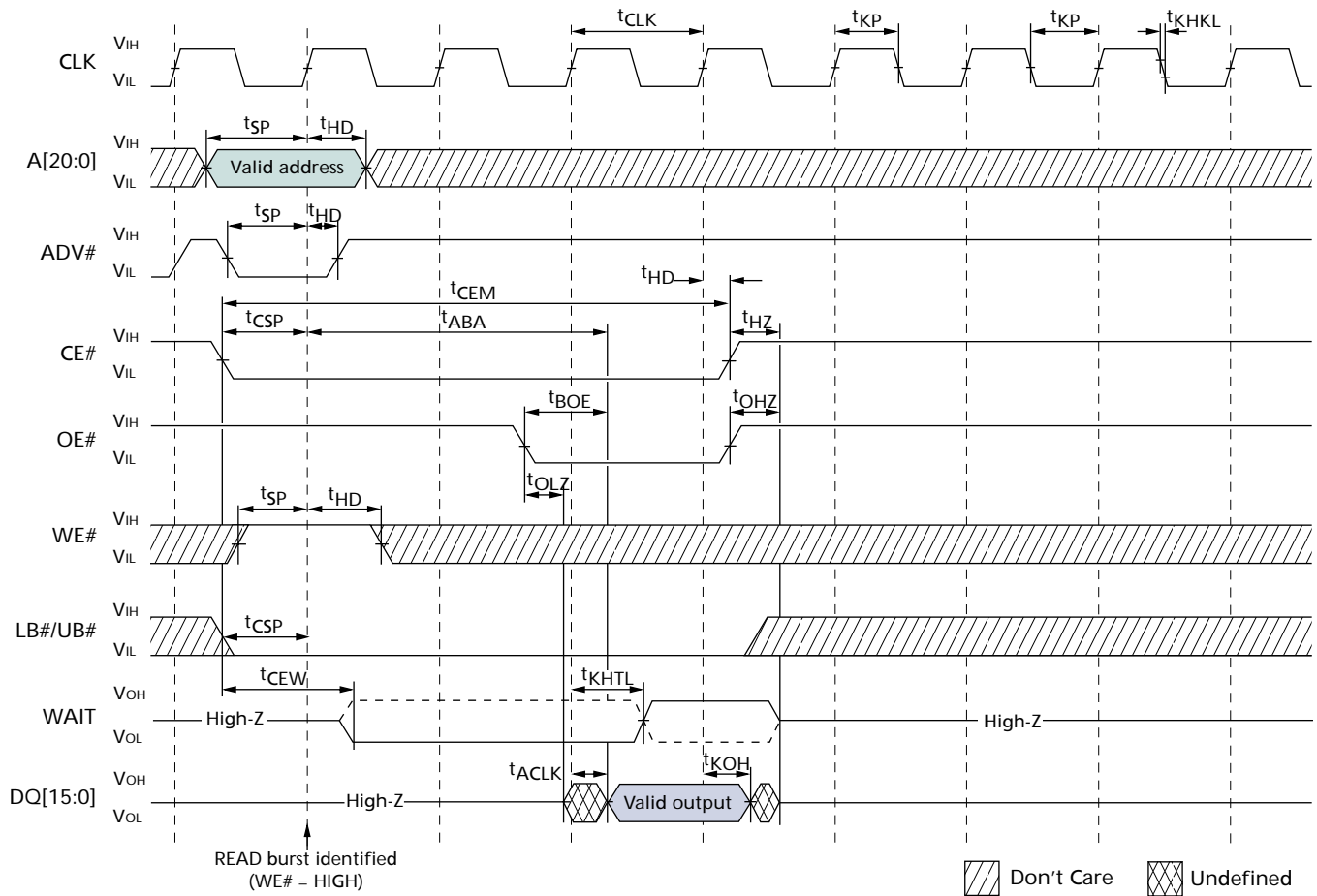
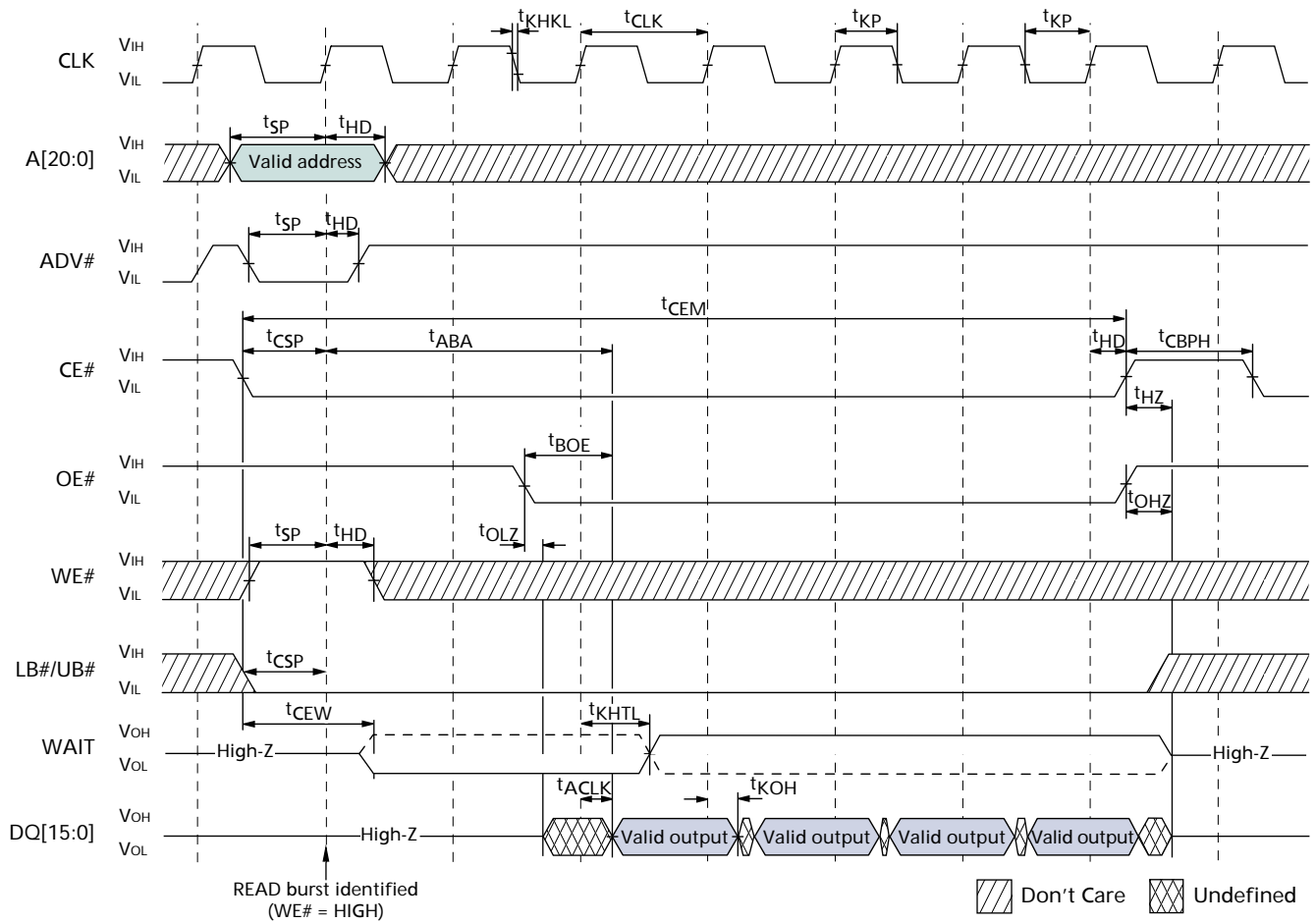


Figure 32: Single-Access Burst READ Operation



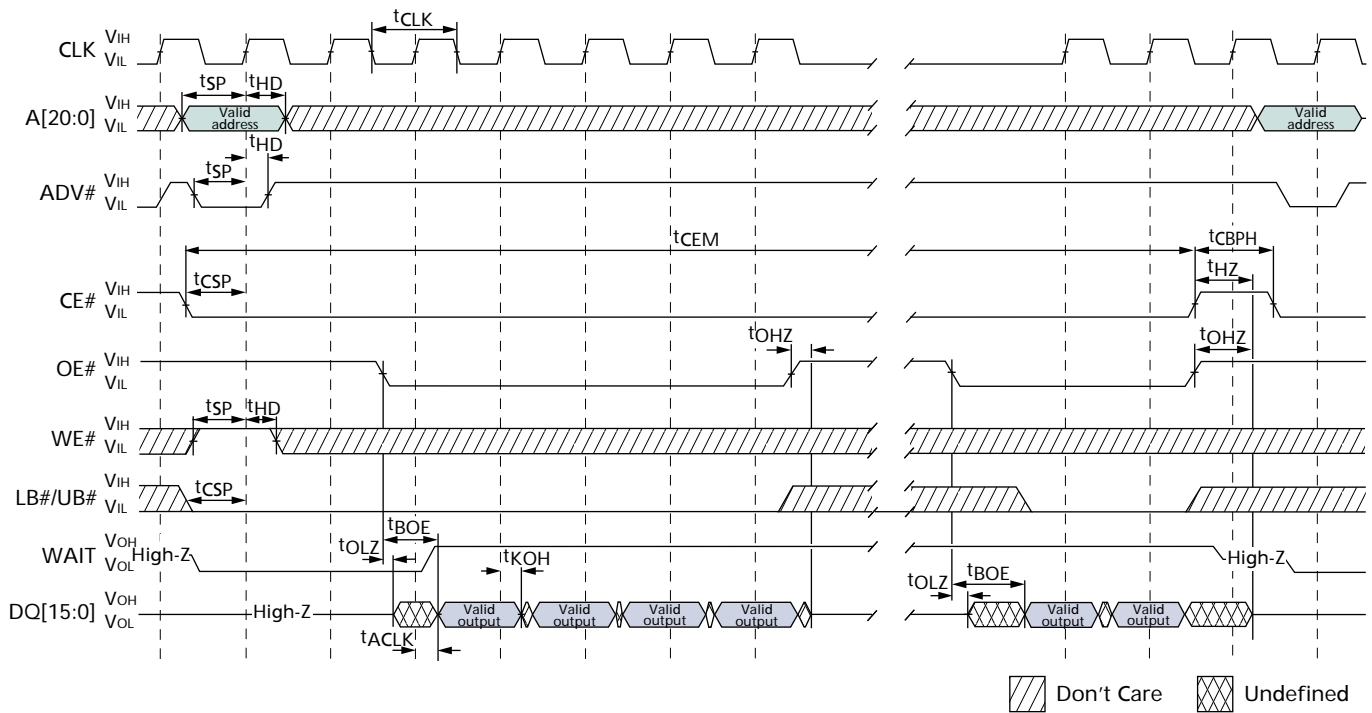
Notes: 1. Non-default BCR settings for single-access burst READ operation: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

Figure 33: 4-Word Burst READ Operation



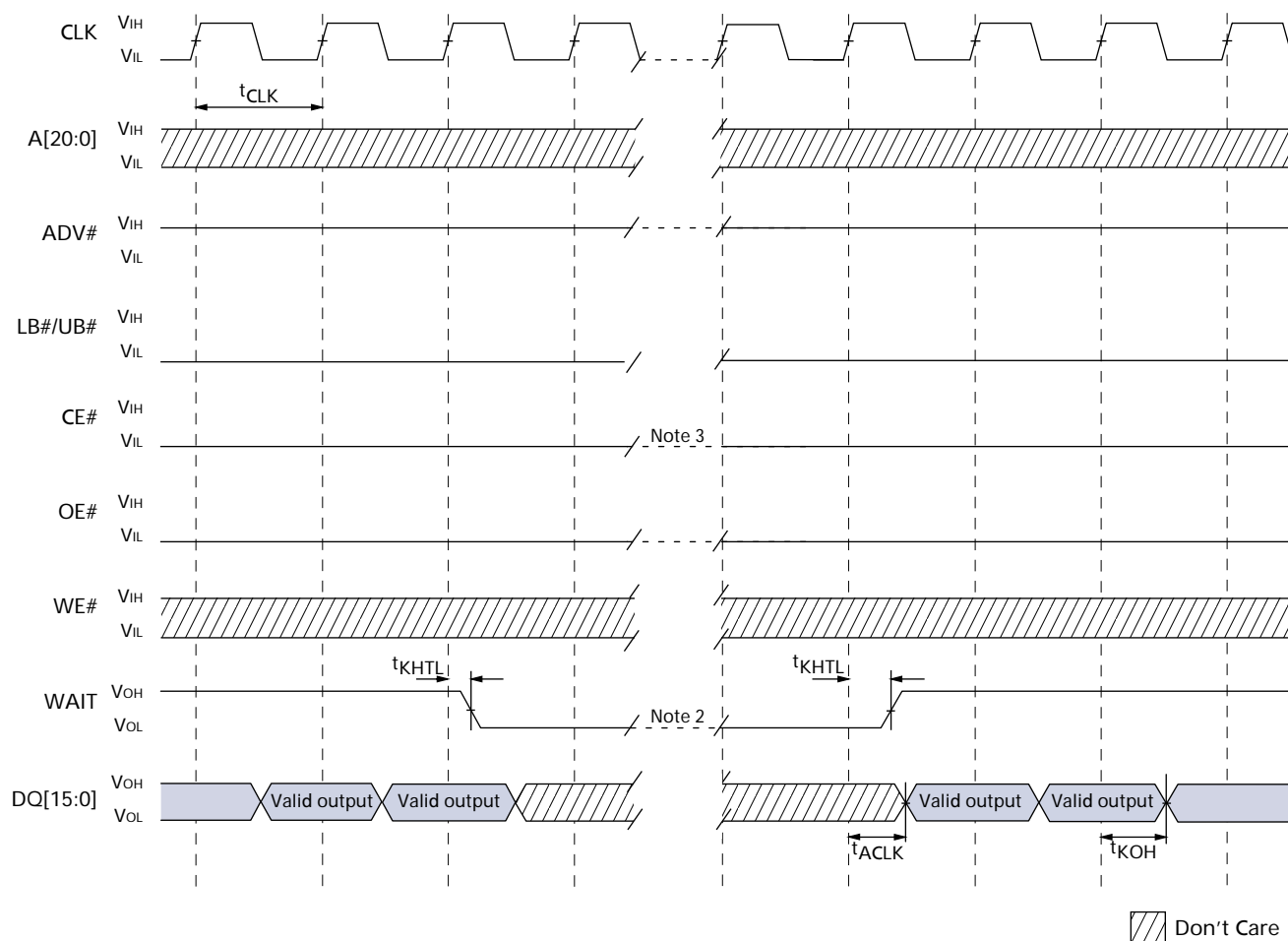
Note: Non-default BCR settings for 4-word burst READ operation: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

Figure 34: READ Burst Suspend



Note: Non-default BCR settings for READ burst suspend: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

Figure 35: Output Delay in Continuous Burst READ with BCR[8] = 0 for End-of-Row Condition



- Notes:
1. Non-default BCR settings for continuous burst READ showing an output delay, BCR[8] = 0 for end-of-row condition: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.
 2. WAIT will be asserted a maximum of $(2 \times LC)$ cycles (BCR[8] = 0; WAIT asserted during delay). LC = latency code (BCR[13:11]).
 3. CE# must not remain LOW longer than t_{CEM} .

Figure 36: CE#-Controlled Asynchronous WRITE

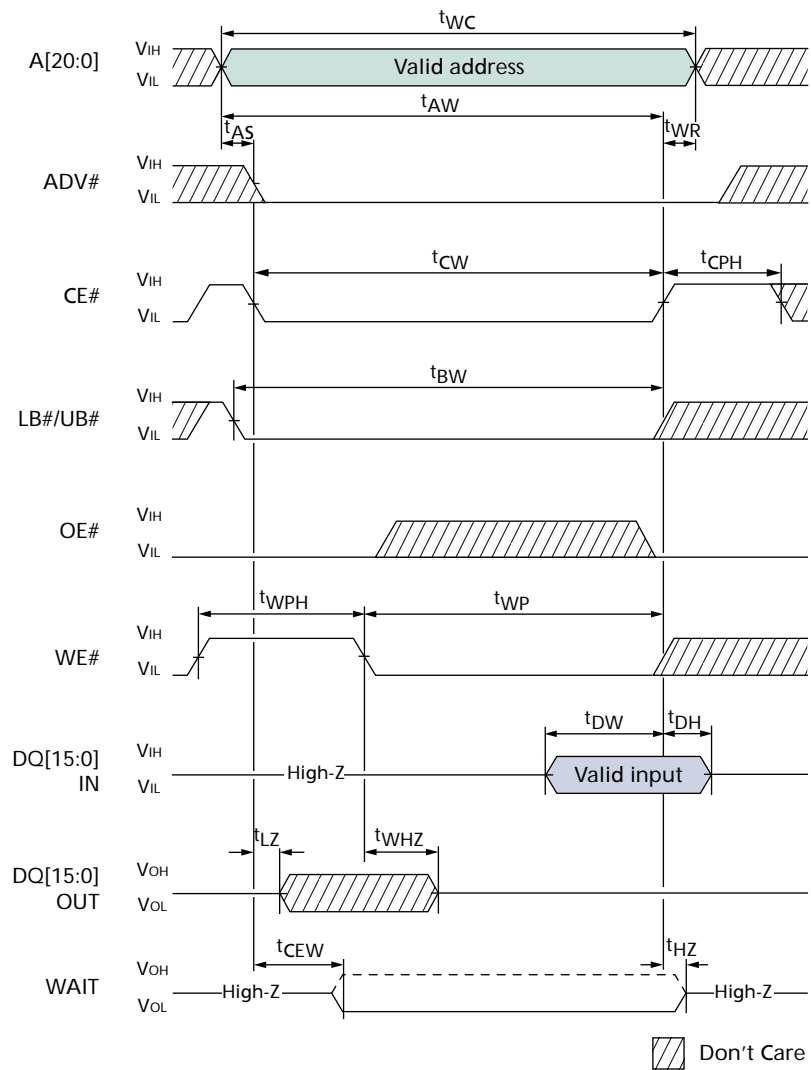


Figure 37: LB#/UB#-Controlled Asynchronous WRITE

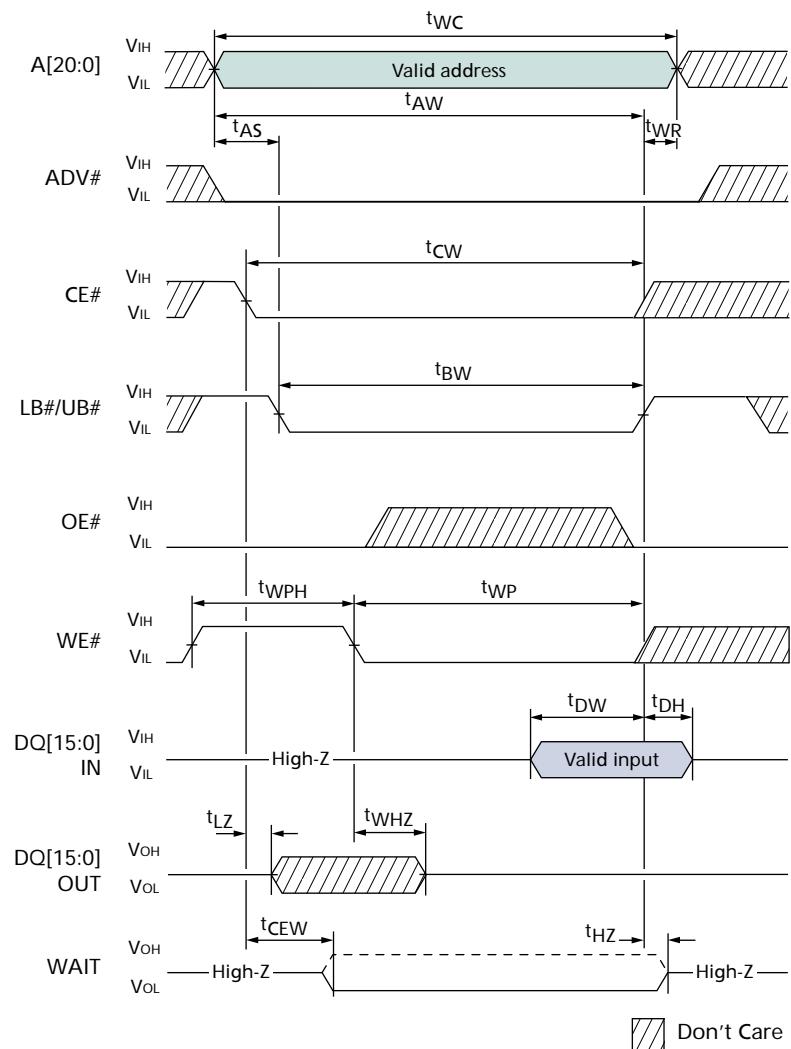


Figure 38: WE#-Controlled Asynchronous WRITE

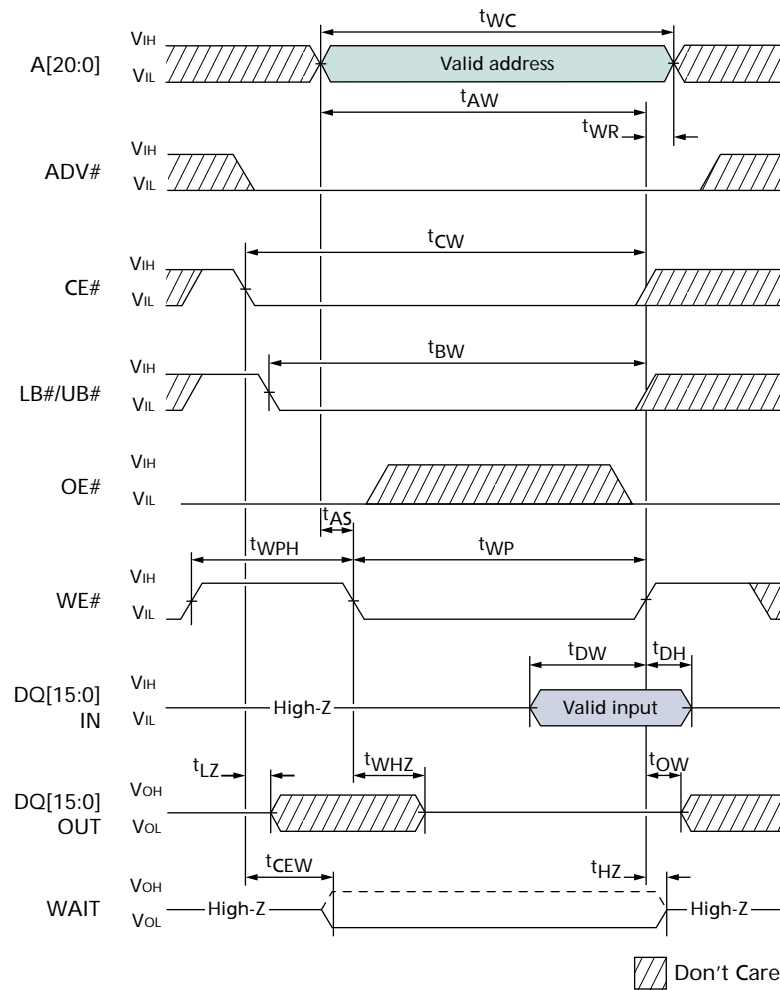


Figure 39: Asynchronous WRITE Using ADV#

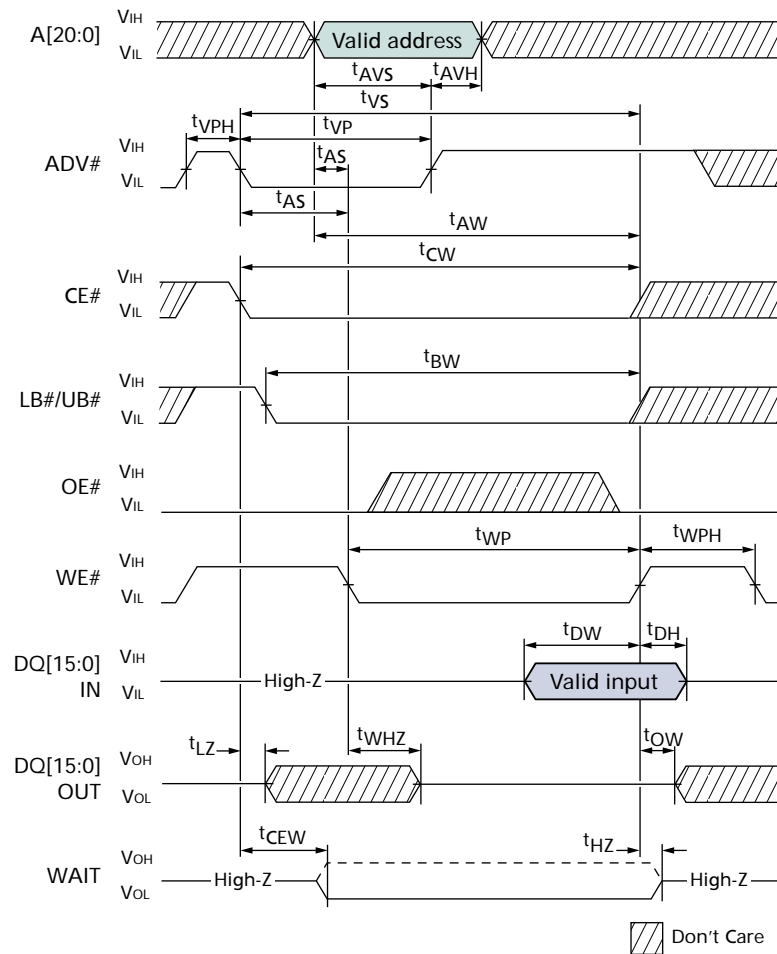
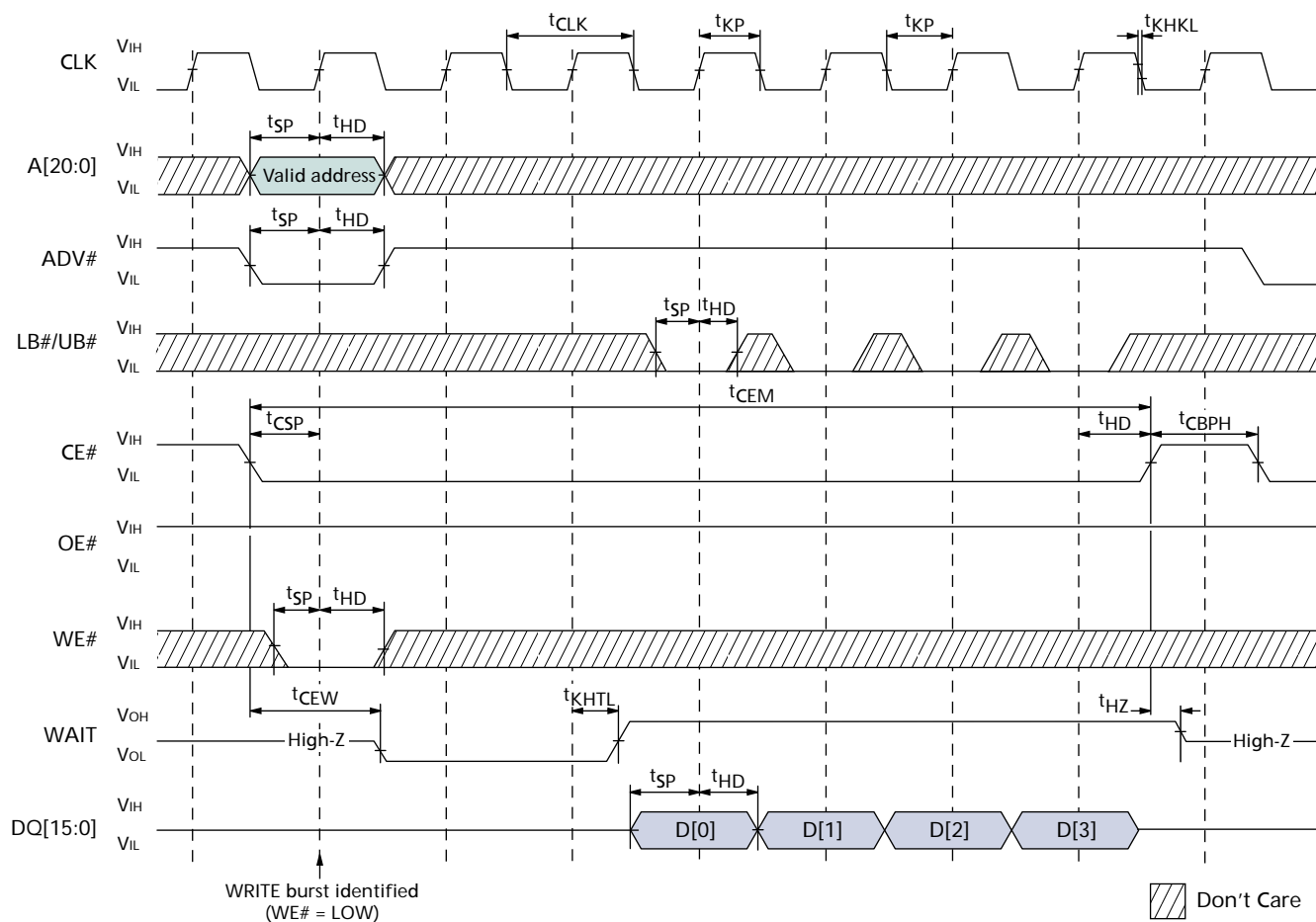
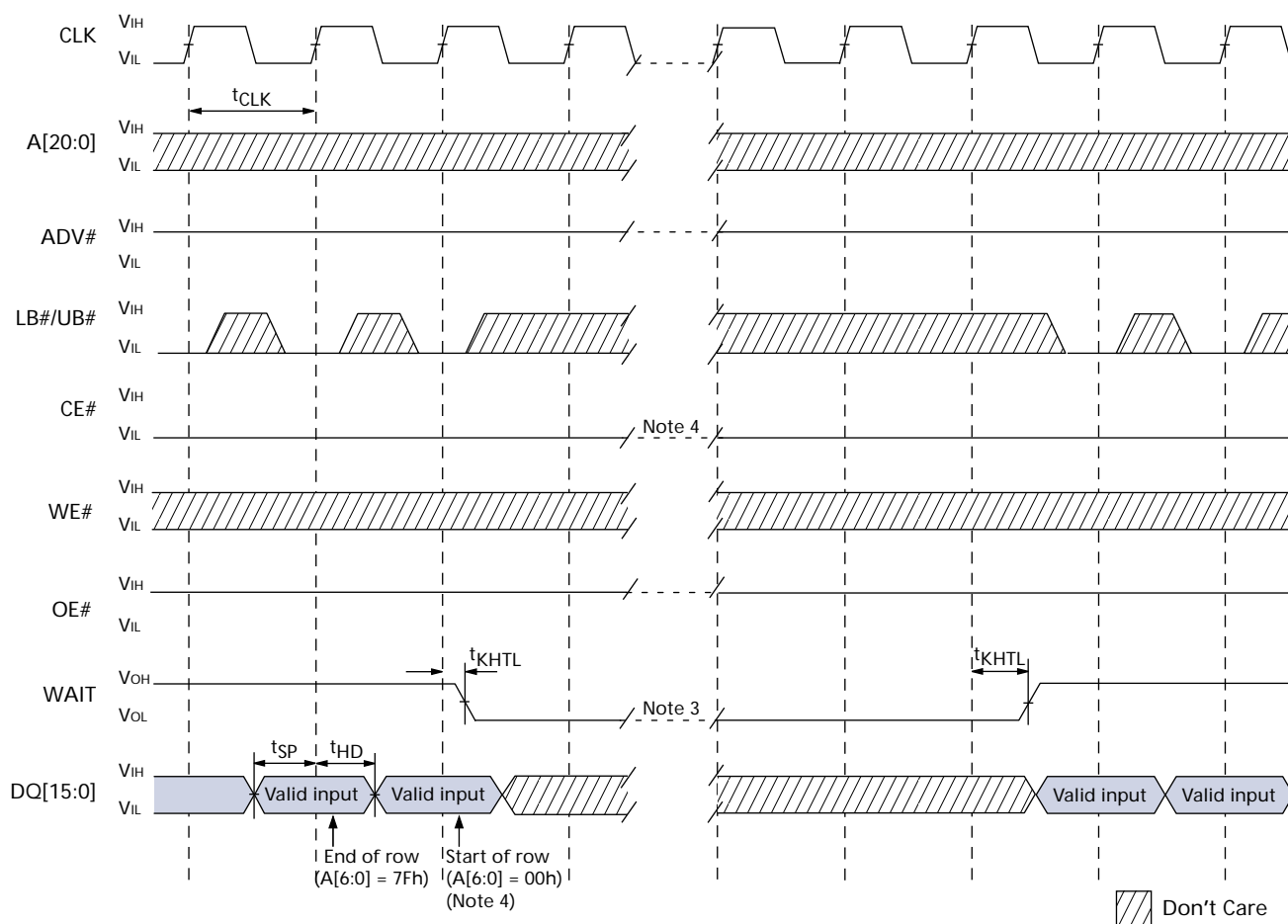


Figure 40: Burst WRITE Operation



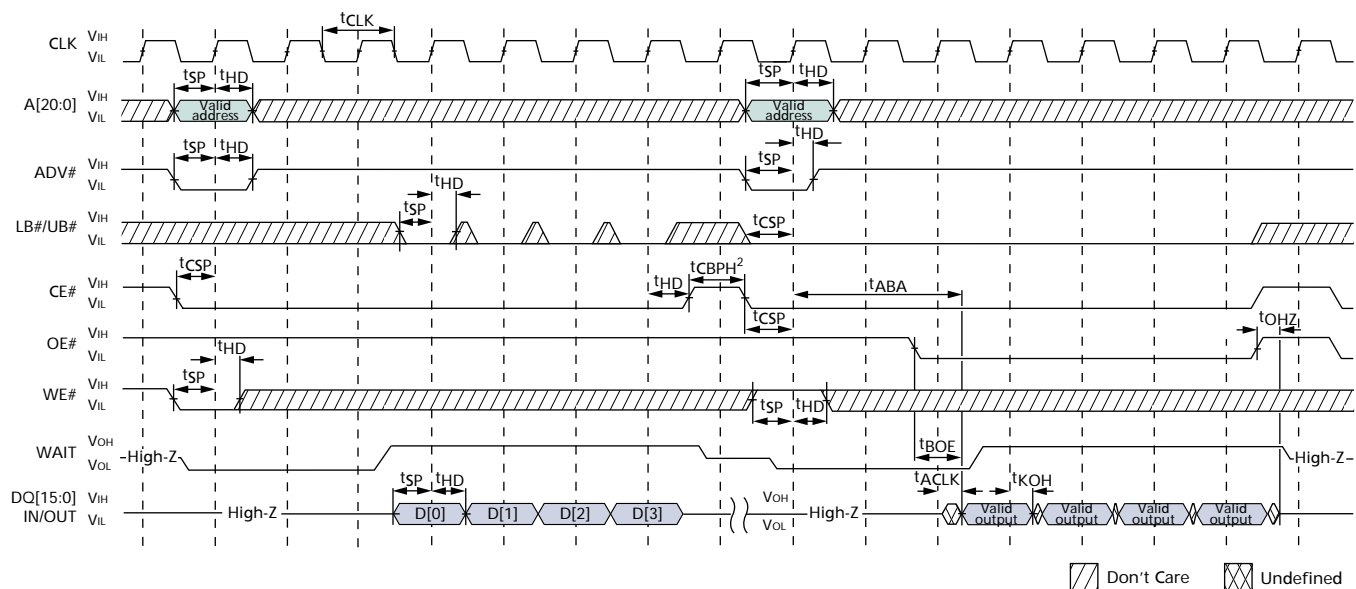
Note: Non-default BCR settings for burst WRITE operation: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted.

Figure 41: Output Delay in Continuous Burst WRITE with BCR[8] = 0 for End-of-Row Condition



- Notes:
1. Non-default BCR settings for continuous burst WRITE, BCR[8] = 0; WAIT active LOW; WAIT asserted during delay. Do not cross row boundaries with fixed latency.
 2. CE# must not remain LOW longer than t_{CEM} .
 3. WAIT asserts for anywhere from LC to 2LC cycles. LC = latency code (BCR[13:11]).
 4. Taking CE# HIGH or ADV# LOW on the start-of-row cycle will abort the burst and not write the start-of-row data. Devices from different CellularRAM vendors can assert WAIT so that the start-of-row data is input just before (as shown), or just after WAIT asserts. This difference in behavior will not be noticed by controllers that monitor WAIT, or that use WAIT to abort on the start-of-row input cycle.

Figure 42: Burst WRITE Followed by Burst READ

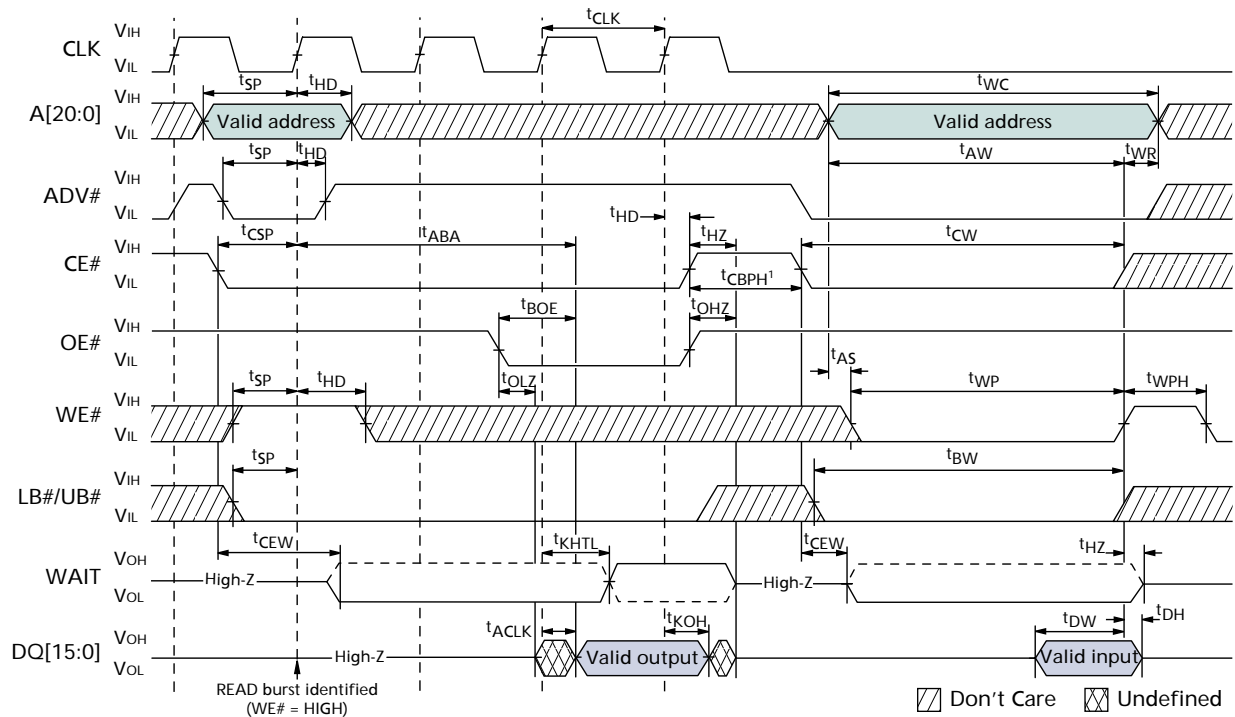


- Notes:
1. Non-default BCR settings for burst WRITE followed by burst READ: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.
 2. When configured for synchronous mode (BCR[15] = 0), a refresh opportunity must be provided every t_{CEM} . A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for greater than 15ns. Note that the CellularRAM Workgroup 1.0 specification requires CE# to be clocked HIGH to terminate the burst.

- Notes:
1. Non-default BCR settings for asynchronous WRITE followed by burst READ: latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.
 2. When configured for synchronous mode (BCR[15] = 0), a refresh opportunity must be provided every ^tCEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for greater than 15ns. Note that the CellularRAM Workgroup 1.0 specification requires CE# to be clocked HIGH to terminate the burst.

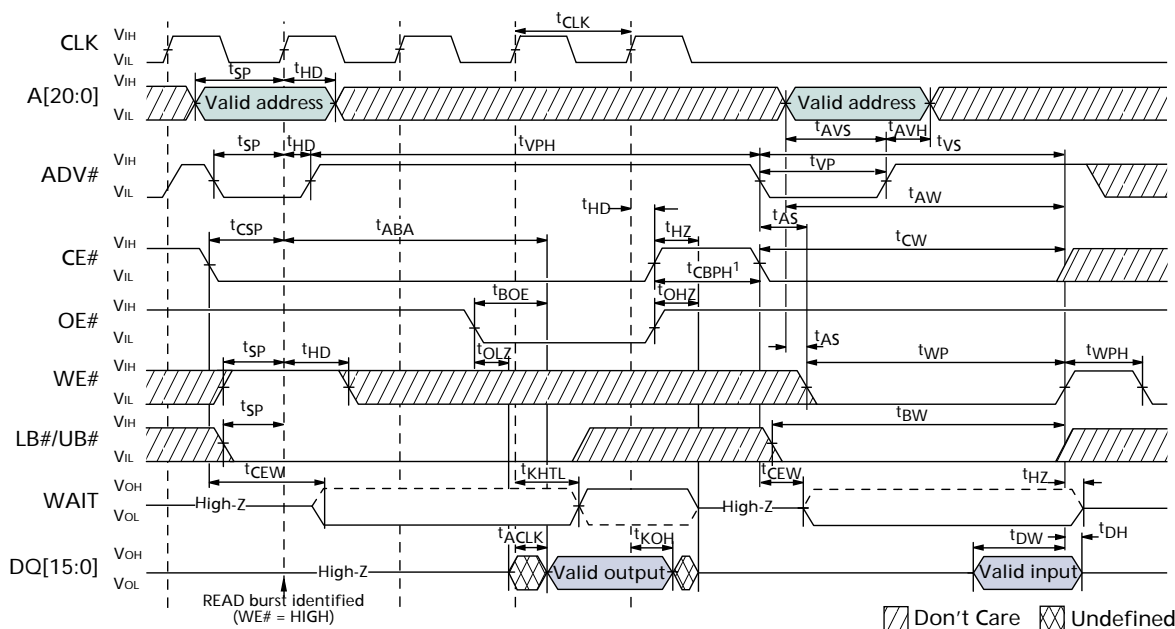
- Notes:
1. Non-default BCR settings for asynchronous WRITE followed by burst READ: latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.
 2. When configured for synchronous mode (BCR[15] = 0), a refresh opportunity must be provided every ^tCEM. A refresh opportunity is satisfied by either of these conditions: a) clocked CE# HIGH, or b) CE# HIGH for greater than 15ns. Note that the CellularRAM Workgroup 1.0 specification requires CE# to be clocked HIGH to terminate the burst.

Figure 45: Burst READ followed by Asynchronous WRITE (WE#-Controlled)



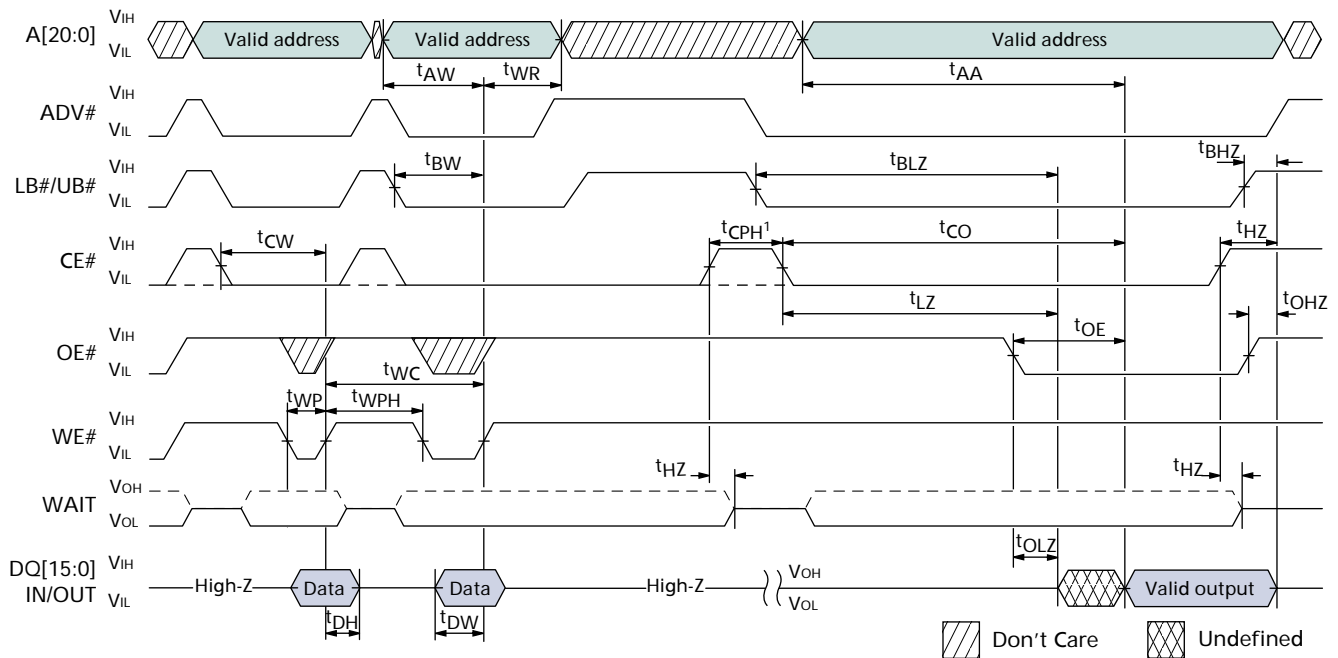
- Notes: 1. When configured for synchronous mode ($BCR[15] = 0$), a refresh opportunity must be provided every t_{CEM} . A refresh opportunity is satisfied by either of the following two conditions: a) clocked $CE\#$ HIGH, or b) $CE\#$ HIGH for greater than 15ns. Note that CellularRAM Workgroup specification 1.0 requires $CE\#$ to be clocked HIGH to terminate the burst.

Figure 46: Burst READ followed by Asynchronous WRITE Using ADV#



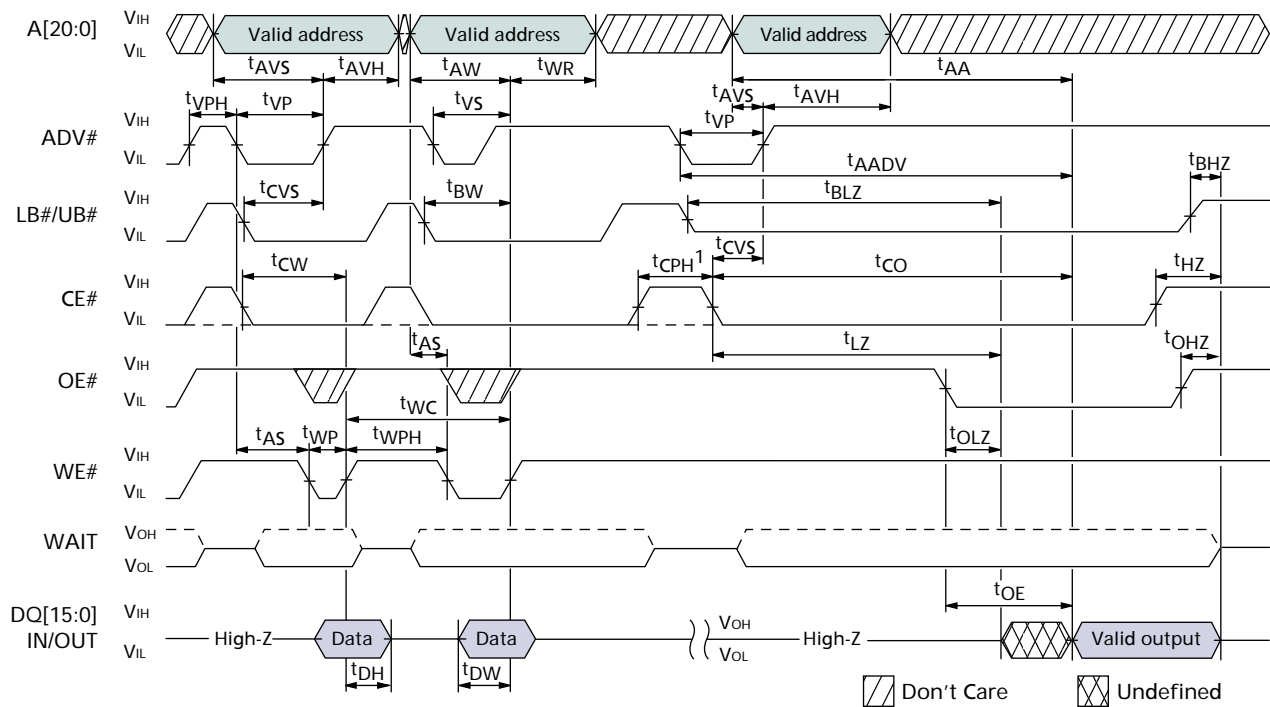
- Notes: 1. When configured for synchronous mode ($BCR[15] = 0$), a refresh opportunity must be provided every t_{CEM} . A refresh opportunity is satisfied by either of the following two conditions: a) clocked $CE\#$ HIGH, or b) $CE\#$ HIGH for greater than 15ns. Note that CellularRAM Workgroup specification 1.0 requires $CE\#$ to be clocked HIGH to terminate the burst.

Figure 47: Asynchronous WRITE followed by Asynchronous READ with ADV# LOW



- Notes: 1. When configured for synchronous mode (BCR[15] = 0), CE# must remain HIGH for at least 5ns (t_{CPH}) to schedule the appropriate internal refresh operation. Otherwise, t_{CPH} is only required after CE#-controlled WRITES.

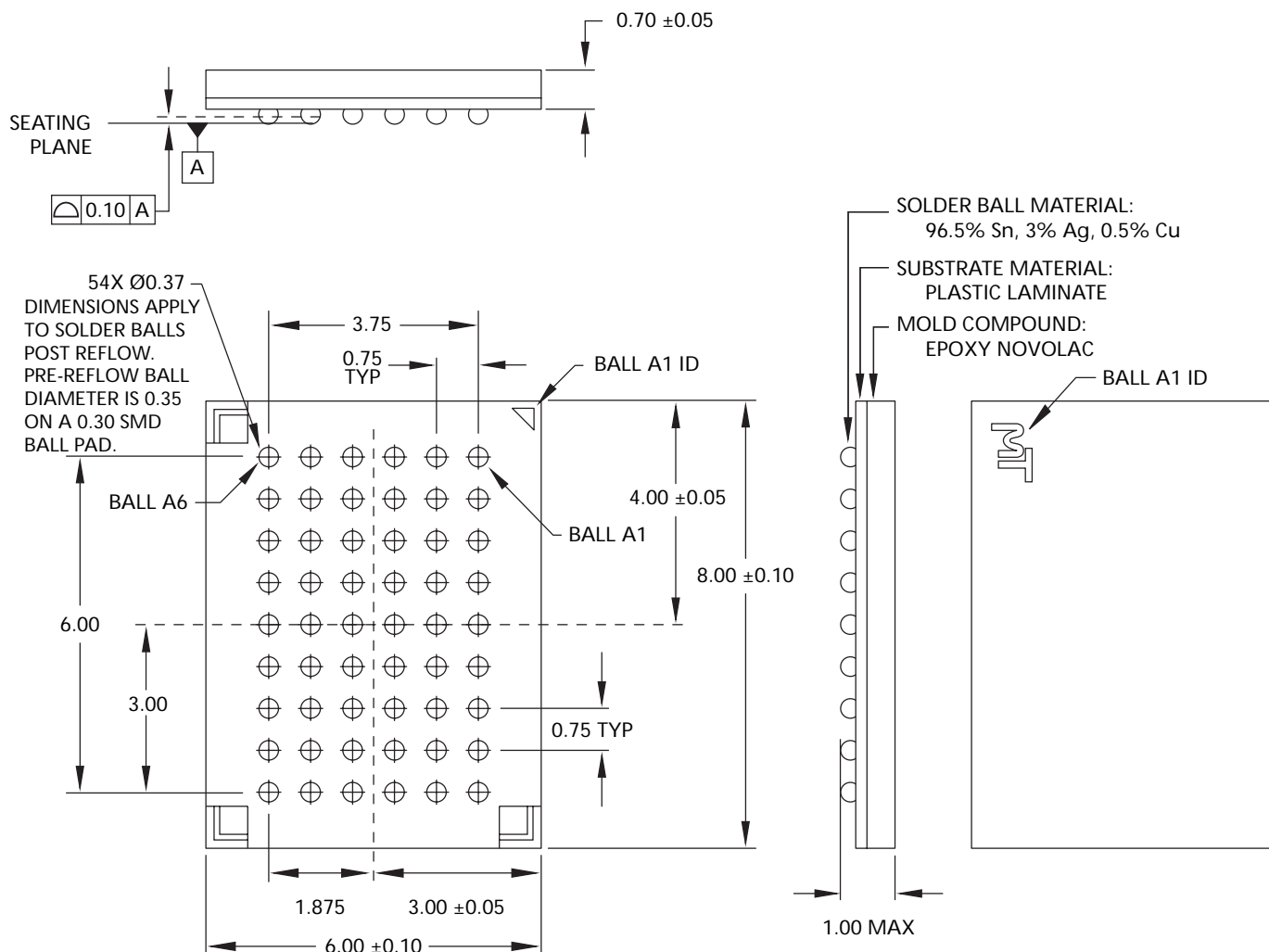
Figure 48: Asynchronous WRITE followed by Asynchronous READ



Notes: 1. When configured for synchronous mode (BCR[15] = 0), CE# must remain HIGH for at least 5ns (t_{CPH}) to schedule the appropriate internal refresh operation. Otherwise, t_{CPH} is only required after CE#-controlled WRITES.

Package Dimensions

Figure 49: 54-Ball VFBGA



- Notes:
1. All dimensions are in millimeters.
 2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.
 3. The MT45W2MW16BGB uses "green" packaging.



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900

prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992

Micron, the M logo, and the Micron logo are trademarks of Micron Technology, Inc. CellularRAM is a trademark of Micron Technology, Inc., inside the U.S. and a trademark of Qimonda AG outside the U.S. All other trademarks are the property of their respective owners. This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

Revision History

| | |
|--|--------------|
| Rev. D, Production | 11/07 |
| <ul style="list-style-type: none">Table 15, "Burst WRITE Cycle Timing Requirements," on page 39: Corrected ^tCEM parameter label from minimum to maximum. | |
| Rev. C, Production | 7/07 |
| <ul style="list-style-type: none">Renumbered the notes in Table 12 on page 36.Replaced "" with "2" in the "Notes" column in Table 12 on page 36. | |
| Rev. B, Production | 5/07 |
| <ul style="list-style-type: none">Changed revision status to Production.Removed "Contact factory" note from the "Options" section on page 1.Changed burst initial latency from "39ns" to "38.5ns" in the "Features" section on page 1.Removed "... (contact factory)" from Figure 3 on page 10.Moved the "WAIT Polarity (BCR[10]) Default = WAIT Active HIGH" section to page 29.Changed A6 and A5 to "Ignored" and added the following text in Figure 24 on page 31: "Setting is ignored (default 00b)." | |
| Rev. A, Preliminary | 2/07 |
| <ul style="list-style-type: none">Initial release. | |