



Automotive LPDDR5X SDRAM

MT62F1G32D2, MT62F2G32D4, MT62F4G32D8

Features

- **Architecture**
 - 19.2 GB/s maximum bandwidth per channel
 - Frequency range: 1200–5 MHz (data rate range per pin: 9600–40 Mb/s with WCK:CK = 4:1)
 - Selectable CKR (WCK:CK = 2:1 or 4:1)
- **LPDDR5X/LPDDR5 data interface**
 - Single x16 channel/die
 - Double-data-rate command/address entry
 - Differential command clocks (CK_t/CK_c) for high-speed operation
 - Differential data clocks (WCK_t/WCK_c)
 - Optional differential read strobe (RDQS_t/RDQS_c)
 - 16n-bit or 32n-bit prefetch architecture
 - Bank Architecture: Bank Group (BG) mode, and 16-bank (16B) mode supported
 - Command-selectable burst lengths (BL = 16 or 32) in bank group or 16-bank modes
 - Background ZQ cal/Cmd-based ZQ calibration
 - Optional link protection (link ECC)
 - Partial-array self refresh (PASR) and partial-array auto refresh (PAAR) with segment mask
- **Ultra-low-voltage core and I/O power supplies**
 - V_{DD1} = 1.70–1.95V; 1.80V TYP
 - V_{DD2H} = 1.01–1.12V; 1.05V TYP
 - V_{DD2L} = V_{DD2H} or 0.87–0.97V; 0.90V TYP
 - V_{DDQ} = 0.50V or 0.45V¹ TYP; 0.30V TYP (ODT off only)
- **I/O characteristics**
 - Interface-LVSTL 0.5/0.3
 - I/O type: Low-swing single-ended, V_{SS} terminated
 - V_{OH}-compensated output drive
 - Programmable V_{SS} on-die termination (ODT)
 - Non target ODT support
 - DVFSQ support
 - Per byte and per pin DFE support
- **Low power features**
 - Enhanced DVFSC: Enhanced dynamic voltage frequency scaling core
 - Single-ended (CK, WCK, RDQS)
 - Data copy
 - Write X

Options

- **Operating Voltage**
 - V_{DD1}/V_{DD2H}/V_{DD2L}/V_{DDQ}/V_{DDQ} (ODT off only): 1.80V/1.05V/V_{DD2H} or 0.90V/0.50V or 0.45V¹/0.30V
- **Array Configuration**

- 1Gb x 32 (1Gbx16 x 1Die x 2Ch x 1R)	1G32
- 2Gb x 32 (1Gbx16 x 1Die x 2Ch x 2R)	2G32
- 4Gb x 32 (2Gbx8 x 2 Die x 2Ch x 2R)	4G32
- **Device configuration**

- 2 die in package (1Gb16 x 2 die)	D2
- 4 die in package (1Gb16 x 4 die)	D4
- 8 die in package (2Gb8 x 8 die)	D8
- **FBGA RoHS-compliant “green” package**

- 315-ball TFBGA 12.4mm x 15.0mm (TYP), seated height 1.1mm (MAX)	DS
- 315-ball LFBGA 12.4mm x 15.0mm (TYP), seated height 1.3mm (MAX)	DV
- **Speed grade, cycle time (^tWCK)**

- 9600 Mb/s	-020
- 8533 Mb/s	-023
- 7500 Mb/s	-026
- **Functional safety, DLEP & RAS**

- ISO 26262 ASIL D compliant	F ²
- ASIL D systematic fault coverage	
- Suitable for meeting random HW metrics up to ASIL D	
- Micron safety documentation	
- Micron safety features enabled	
- Direct Link ECC Protocol (DLEP)	
- Improved RAS	
- **Automotive**

- AEC-Q100	A
- PPAP	
- **Operating temperature:**

- -40°C ≤ T _C ≤ +95°C	IT
- -40°C ≤ T _C ≤ +105°C	AT
- -40°C ≤ T _C ≤ +125°C	UT ³
- **Revision**

	:F
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Notes: 1. V_{DDQ} = 0.45V (TYP) support on all packages up to 7500 Mb/s.

2. For functional safety documentation to aid in ISO 26262 functional safety system design, contact Micron sales representative.



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3. Based on automotive usage model. Contact Micron sales representative with questions.

Part Number Ordering Information

Figure 1: Part Number Chart

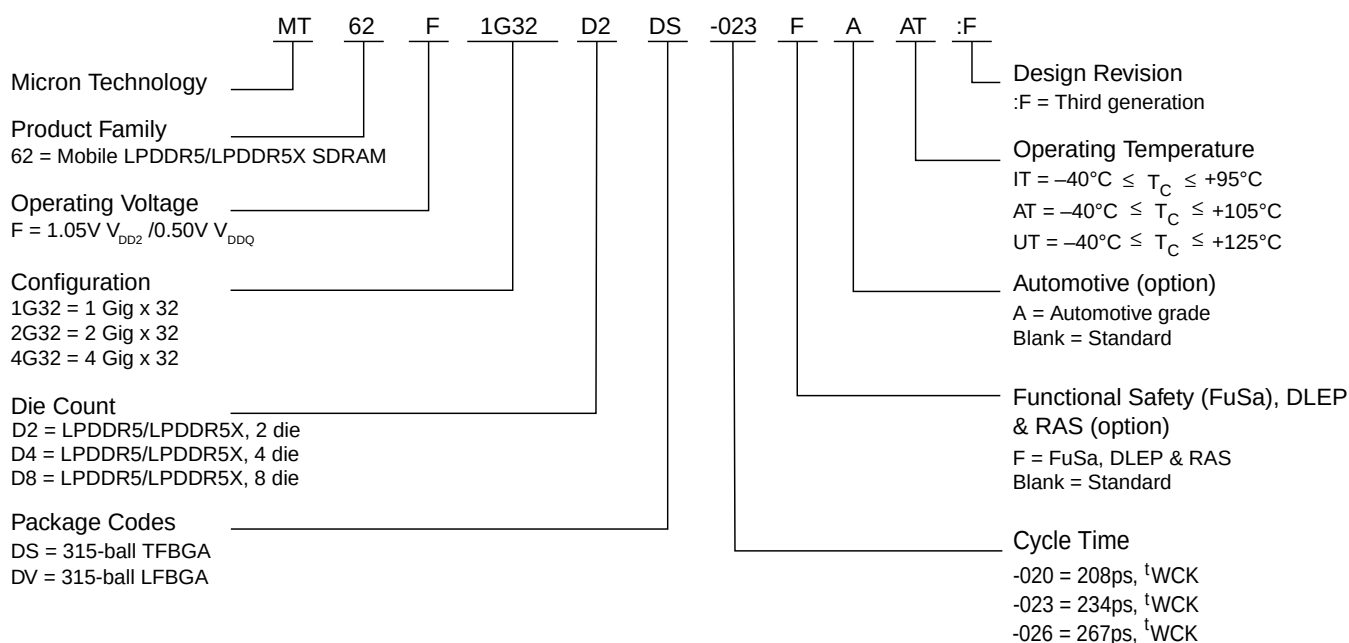


Table 1: Part Number List

Part Number	Total Density	Data Rate per Pin
MT62F1G32D2DS-020 AIT:F	4GB (32Gb)	9600 Mb/s
MT62F1G32D2DS-020 AAT:F		
MT62F1G32D2DS-020 AUT:F		
MT62F1G32D2DS-020 FAAT:F		
MT62F1G32D2DS-020 FAUT:F		
MT62F1G32D2DS-020 FAIT:F		
MT62F2G32D4DS-020 AIT:F	8GB (64Gb)	
MT62F2G32D4DS-020 AAT:F		
MT62F2G32D4DS-020 AUT:F		
MT62F2G32D4DS-020 FAAT:F		
MT62F2G32D4DS-020 FAUT:F		
MT62F2G32D4DS-020 FAIT:F		
MT62F4G32D8DV-020 AIT:F	16GB (128Gb)	
MT62F4G32D8DV-020 AAT:F		
MT62F4G32D8DV-020 AUT:F		
MT62F4G32D8DV-020 FAAT:F		
MT62F4G32D8DV-020 FAIT:F		
MT62F4G32D8DV-020 FAUT:F		


**315b: x32 Automotive LPDDR5X SDRAM
Features**
Table 1: Part Number List (Continued)

Part Number	Total Density	Data Rate per Pin
MT62F1G32D2DS-023 AIT:F	4GB (32Gb)	8533 Mb/s
MT62F1G32D2DS-023 AAT:F		
MT62F1G32D2DS-023 AUT:F		
MT62F1G32D2DS-023 FAAT:F		
MT62F1G32D2DS-023 FAUT:F		
MT62F1G32D2DS-023 FAIT:F		
MT62F2G32D4DS-023 AIT:F	8GB (64Gb)	
MT62F2G32D4DS-023 AAT:F		
MT62F2G32D4DS-023 AUT:F		
MT62F2G32D4DS-023 FAAT:F		
MT62F2G32D4DS-023 FAUT:F		
MT62F2G32D4DS-023 FAIT:F		
MT62F4G32D8DV-023 AIT:F	16GB (128Gb)	
MT62F4G32D8DV-023 AAT:F		
MT62F4G32D8DV-023 AUT:F		
MT62F4G32D8DV-023 FAAT:F		
MT62F4G32D8DV-023 FAUT:F		
MT62F4G32D8DV-023 FAIT:F		
MT62F2G32D4DS-026 AIT:F	8GB (64Gb)	7500 Mb/s
MT62F2G32D4DS-026 AAT:F		
MT62F4G32D8DV-026 AIT:F	16GB (128Gb)	
MT62F4G32D8DV-026 AAT:F		

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

LPDDR5/LPDDR5X Data Sheet List

For general LPDDR5/LPDDR5X specifications, please refer to the data sheets below.

- General LPDDR5/LPDDR5X Specifications 1: Mode Registers
- General LPDDR5/LPDDR5X Specifications 2: AC/DC and Interface Specifications
- General LPDDR5/LPDDR5X Specifications 3: Features and Functionalities



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Important Notes and Warnings

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System Design and Implementation. This product has been developed for multiple applications based on assumed use cases and requirements (including assumed functional safety requirements and constraints). It is the customer's sole responsibility to evaluate and confirm the validity and suitability of Micron's product datasheet, assumed use cases and requirements, and evaluation results by verifying Micron's assumptions against actual use cases and requirements in the intended end system and application. The customer must ensure compliance with all applicable requirements and standards (including industry, product, security, privacy, safety, etc.) to its system and applications. The customer must protect against death, personal injury, and severe property and environmental damage by ensuring that adequate design and redundancy (as needed), manufacturing and operating safeguards are included into customer's applications to ensure that failure of the Micron component will not result in such harms.

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Limited Warranty. In no event shall Micron be liable for any indirect, incidental, punitive, special or consequential damages (including without limitation lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort, warranty, breach of contract or other legal theory, unless explicitly stated in a written agreement executed by Micron's duly authorized representative.



General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQs collectively, unless specifically stated otherwise.

RDQS, CK, and WCK should be interpreted as RDQS_t, RDQS_c, CK_t, CK_c, and WCK_t, WCK_c respectively unless specifically stated otherwise. CA includes all CA pins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[6:0].

V_{REF} indicates $V_{REF(CA)}$ and $V_{REF(DQ)}$.

Complete functionality is described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any content defined in this device ID specific data sheet document takes precedence over similar content defined in the general core LPDDR5/LPDDR5X SDRAM data sheet document(s).

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.



Automotive Product Notes

The automotive LPDDR5/LPDDR5X DRAM Product family ("A" parts - see Part Number Ordering Information) are not intended for use in functional safety (ASIL rated) applications. Should customer or distributor purchase, use, or sell any Micron "A" component for any functional safety (ASIL rated) application, customer and distributor shall indemnify and hold harmless Micron and its subsidiaries, subcontractors, and affiliates and the directors, officers, and employees of each against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, or death arising in any way out of such functional safety (ASIL rated) application, whether or not Micron or its subsidiaries, subcontractors, or affiliates were negligent in the design, manufacture, or warning of the Micron product.



Functional Safety, DLEP & RAS Notes

This automotive functional safety, DLEP and improved RAS LPDDR5/LPDDR5X DRAM product family ("F" parts - see Part Numbering Ordering Information). This product has been developed according to ISO 26262:2018 requirements for use in functional safety systems targeting up to ASIL D compliance.

The automotive functional safety, DLEP and improved RAS LPDDR5/LPDDR5X DRAM product family contains several new features that operate within the JEDEC LPDDR5/LPDDR5X protocols (commands, timings, and so forth) and are made available to the integrator on "F" parts. The specification addendum governing these functional safety, DLEP and improved RAS features is available under NDA. This LPDDR5/LPDDR5X DRAM may operate as a standard JEDEC LPDDR5/LPDDR5X DRAM only, or as a standard JEDEC LPDDR5/LPDDR5X DRAM specifically designed with functional safety, DLEP and improved RAS features (only available on "F" parts).

Additional support is available to customers who need to integrate Micron's products in their functional safety-related applications. This support may include Safety Analysis Report, reporting FMEDA results and metrics, Safety Manual and Pin FMEA Report, providing guidelines and instructions for using Micron products in safety-related applications.

Contact a Micron sales representative to initiate the process required to obtain the functional safety documentation.


**315b: x32 Automotive LPDDR5X SDRAM
Device Configuration**

Device Configuration

Table 2: Die Organization in the Package (x32)

Die Organization	1G32 (32 Gb/package)	2G32 (64 Gb/package)	4G32 (128 Gb/package)
Channel A	x16 mode × 1 die	–	–
Channel B	x16 mode × 1 die	–	–
Channel A, rank 0	–	x16 mode × 1 die	–
Channel B, rank 0	–	x16 mode × 1 die	–
Channel A, rank 1	–	x16 mode × 1 die	–
Channel B, rank 1	–	x16 mode × 1 die	–
Channel A, rank 0 DQ[7:0]	–	–	x8 mode × 1 die
Channel A, rank 1 DQ[7:0]	–	–	x8 mode × 1 die
Channel B, rank 0 DQ[7:0]	–	–	x8 mode × 1 die
Channel B, rank 1 DQ[7:0]	–	–	x8 mode × 1 die
Channel A, rank 0 DQ[15:8]	–	–	x8 mode × 1 die
Channel A, rank 1 DQ[15:8]	–	–	x8 mode × 1 die
Channel B, rank 0 DQ[15:8]	–	–	x8 mode × 1 die
Channel B, rank 1 DQ[15:8]	–	–	x8 mode × 1 die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 3: Die Addressing

Description	1G32 (32 Gb/package), 2G32 (64 Gb/package)		4G32 (128 Gb/package)	
Density per die	16Gb		16Gb	
Bits	17,179,869,184		17,179,869,184	
Bank mode	BG mode	16B mode	BG mode	16B mode
Configuration	64Mb × 16 DQ × 4 Banks × 4BG	64Mb × 16 DQ × 16 Banks	128Mb × 8 DQ × 4 Banks × 4BG	128Mb × 8 DQ × 16 Banks
Number of banks	4	16	4	16
Number of bank groups	4	1	4	1
Array prefetch bits	256	256	128	128
Rows per bank	65,536		131,072	
Columns	64		64	
Page size (bytes)	2048	2048	1024	1024
Native burst length	16	16	16	16
Number of I/Os	16		8	
Bank address	BA[1:0]	BA[3:0]	BA[1:0]	BA[3:0]
Bank group address	BG[1:0]	–	BG[1:0]	–
Row address	R[15:0]		R[16:0]	
Column address	C[5:0]		C[5:0]	
Burst address	B[3:0]	B[3:0]	B[3:0]	B[3:0]
Burst starting address boundary	128-bit		128-bit	

Note: 1. Refer to the SDRAM Addressing section in General LPDDR5/LPDDR5X Specifications 3.



315b: x32 Automotive LPDDR5X SDRAM Refresh Requirement Parameters

Refresh Requirement Parameters

Table 4: Refresh Requirement Parameters

Parameter	Symbol	16Gb Die	Unit
		BG and 16B Mode	
REFRESH cycle time (all banks)	t_{RFCab}	280	ns
REFRESH cycle time (per bank)	t_{RFCpb}	140	ns
Per bank refresh to per bank refresh time (different bank)	$t_{PBR2PBR}$	90	ns
Per bank refresh to ACTIVATE command time (different bank)	$t_{PBR2ACT}$	7.5	ns

Note: 1. This table only describes refresh parameters that are density dependent. Refer to Refresh Requirement section in General LPDDR5/LPDDR5X Specifications 3 for all refresh parameters.



315b: x32 Automotive LPDDR5X SDRAM DQ Rx Mask and Single Input Pulse Relaxed Specifications

CS Rx Relaxed Specification

Table 5: CS Rx Specifications

Item	Symbol	Min/ Max	CK Frequency (MHz)												Unit	Note
			67 ⁶	133	200	266	344	400	467	533	600	688	750	800		
Rx mask																
CS Rx mask height	vCSIVW	Min	155												mV	2, 7
CS Rx mask width at V _{REF} CS	^t CSIVW1	Min	0.3												UI	1
CS Rx mask width at vCSIVW	^t CSIVW2	Min	0.22												UI	1
Rx single pulse																
CS Rx pulse amplitude	vCSIHL_AC	Min	240												mV	3
CS reference voltage	vREFCS		V _{DD2H} /3												mV	
CS Rx pulse width	^t CSIPW	Min	0.6												UI	
Power down																
CS V _{IL} during power down/ deep sleep	V _{ILPD}	Max	130												mV	4
CS V _{IH} during power down/ deep sleep	V _{IHPD}	Min	550												mV	5
		Max	V _{DD2H} + 200													

- Notes: 1. CS Rx mask voltage and timing parameters at the pin include temperature drift and voltage AC noise impact based on Z(f) specification at a fixed temperature on the package. The voltage supply noise must comply to the component min/max DC operating conditions.
2. CS single-pulse signal amplitude into the receiver must meet or exceed vCSIHL_AC at any point over the total UI; No timing requirement above a certain level. vCSIHL_AC is the peak-to-peak voltage centered around V_{REF} CS such that vCSIHL_AC/2 min has to be met both above and below V_{REF} CS.
3. vCSIHL_AC does not have to be met when no transitions are occurring.
4. The input voltage presented to the CS Rx pin during power down should be 0V nominally to minimize leakage current.
5. V_{IHPD} is only applied for POWER DOWN and DEEP SLEEP EXIT operations.
6. The Rx voltage and absolute timing requirements apply for all CS operating frequencies at or below 67 for all speed bins. For example, ^tCSIVW1 (ns) = 4.477ns at or below 67 MHz CK frequency.
7. Measured at die pad.

DQ Rx Mask and Single Input Pulse Relaxed Specifications

Table 6: DQ Rx Mask and Single Input Pulse Specifications

Item	Symbol	Min/ Max	WCK Frequency (MHz)			Unit	Notes
			3750	4266	4800		
DQ Rx mask height	vDIVW	Min	70			mV	1, 2, 3
DQ Rx mask width at V _{REF} (DQ)	^t DIVW1	Min	0.35			UI	1, 3
DQ Rx mask width at vDIVW	^t DIVW2	Min	0.18			UI	1, 3
DQ Rx pulse width at V _{REF} (DQ)	^t DIPW1	Min	0.51			UI	4
DQ Rx pulse reference	^t DIPW2	Min	0.26			UI	4
DQ Rx pulse width at V _{REF} (DQ) ± vDIVW/2	^t DIHL	Min	0.24			UI	4
DQ Rx pulse amplitude from programmed V _{REF} (DQ)	vDIHP1	Min	70			mV	
	vDILP1	Max	-70			mV	



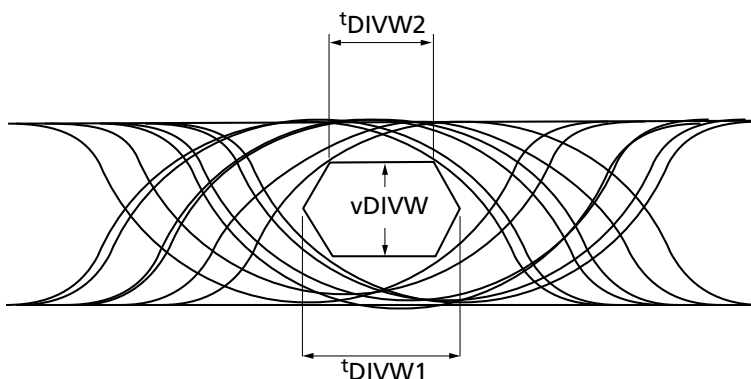
315b: x32 Automotive LPDDR5X SDRAM DQ Rx Mask and Single Input Pulse Relaxed Specifications

Table 6: DQ Rx Mask and Single Input Pulse Specifications (Continued)

Item	Symbol	Min/ Max	WCK Frequency (MHz)			Unit	Notes
			3750	4266	4800		
DQ Rx early pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP2	Min	55			mV	
	vDILP2	Max	-55			mV	
DQ Vref	VrefDQ	Max	180			mV	
		Min	75			mV	
DQ to DQ Offset	tDQ2DQ	Max	30			ps	5

- Notes: 1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies greater than TBD MHz and maximum voltage of TBD mV peak-to-peak from DC-TBD MHz at a fixed temperature on the package. The voltage supply noise must comply with the component min/max DC operating conditions.
2. Rx mask voltage vDIVW must be centered around $V_{REF(DQ)}$.
3. Mask specifications (t_{DIVW1} , t_{DIVW2} , and vDIVW) are the same regardless DFE enabled or disabled. DFE co-efficient can be included as part of input waveform amplitude when DFE is enabled.
4. UI = $t_{WCK}/2$, programed V_{REF} , is defined as a percentage of MR14/15 code x V_{DDQ} .
5. DQ to DQ offset defined within byte from DRAM pin to internal latch for a given component.

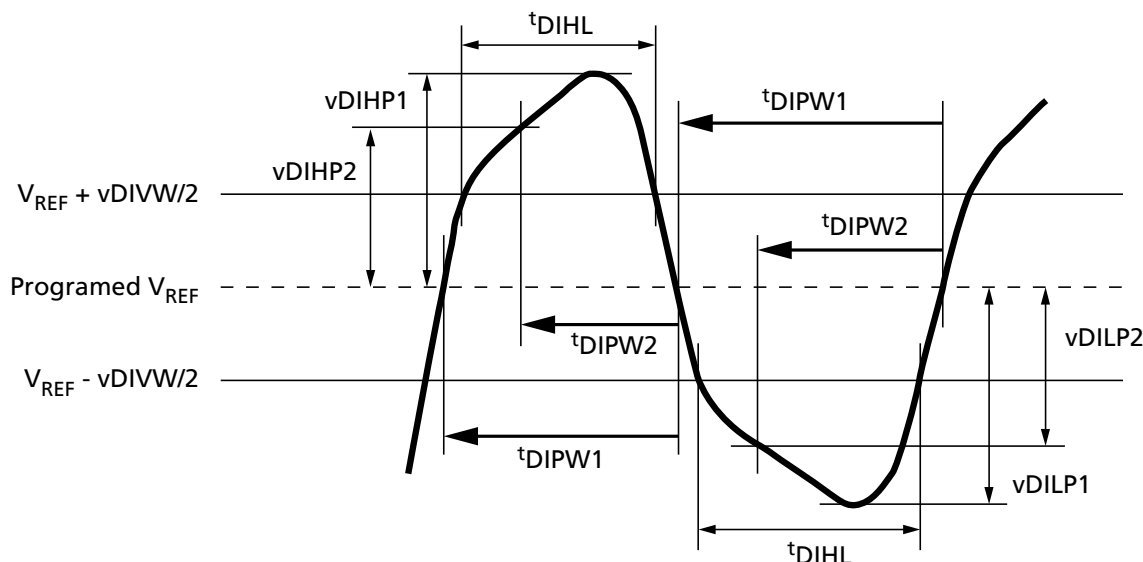
Figure 2: DQ Rx Mask Definition





315b: x32 Automotive LPDDR5X SDRAM DQ Rx Mask and Single Input Pulse Relaxed Specifications 3200 MHz

Figure 3: LPDDR5X DQ Single Pulse Definition



Note: 1. $vDIHL_AC/2 = vDIHP1 = vDILP1$. Programmed $V_{REF(DQ)}$ is defined as percentage of MR14/15 code * V_{DDQ} .

DQ Rx Mask and Single Input Pulse Relaxed Specifications 3200 MHz

Table 7: DQ, DMI, Parity and DBI Rx Mask and Single Input Pulse Specifications

Item	Symbol	Min/Max	WCK Frequency (MHz)	Unit	Notes
			3200		
DQ Rx mask height	vDIVW	Min	70	mV	1, 2, 3, 6
DQ Rx mask width at $V_{REF(DQ)}$	t_{DIVW1}	Min	0.35	UI	1, 3
DQ Rx mask width at vDIVW	t_{DIVW2}	Min	0.18	UI	1, 3
DQ Rx pulse width at $V_{REF(DQ)}$	t_{DIPW1}	Min	0.51	UI	4, 6
DQ Rx pulse reference	t_{DIPW2}	Min	0.26	UI	4
DQ Rx pulse width at $V_{REF(DQ)} \pm vDIVW/2$	t_{DIHL}	Min	0.24	UI	4, 6
DQ Rx pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP1	Min	70	mV	
	vDILP1	Max	-70	mV	
DQ Rx early pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP2	Min	55	mV	
	vDILP2	Max	-55	mV	
DQ V_{REF}	$V_{REF(DQ)}$	Min	75	mV	6
		Max	180	mV	6
DQ to DQ offset	t_{DQ2DQ}	Max	30	ps	5

Notes: 1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies greater than TBD MHz and maximum voltage of TBD mV peak-to-peak from DC-TBD MHz at a fixed temperature on the package. The voltage supply noise must comply with the component min/max DC operating conditions.

2. Rx mask voltage vDIVW must be centered around $V_{REF(DQ)}$.

3. Mask specifications (t_{DIVW1} , t_{DIVW2} , and vDIVW) are the same regardless DFE enabled or disabled. DFE coefficient can be included as part of input waveform amplitude when DFE is enabled.

4. UI = $t_{WCK}/2$, programed V_{REF} , is defined as a percentage of MR14/15 code x V_{DDQ} .



315b: x32 Automotive LPDDR5X SDRAM 16-Bank Extended Frequency

5. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
6. When vDIVV is 70mV or more and less than 80mV.

16-Bank Extended Frequency

16-Bank Extended Frequency Description

Micron's LPDDR5 SDRAM device which are marked with 8533 Mb/s per-pin (-023) capability can support frequency set points using 2:1 WCK to CK ratio and above the 1600 MHz limit. Shown in the table below is specification requirements when considering 1867 MHz and 2133 MHz frequencies. This support is not available on 1-alpha process node and earlier Device ID's, this feature can expand capabilities of your system.

Table 8: 16-Bank Operation¹ @ 4.3 Gb/s

Parameter	3733 Mb/s per-pin	Comments	4267 Mb/s per-pin	Comments
RL Set 1/2/3	20/22/24	MR2[3:0] = 1100	23/25/26	MR2[3:0] = 1101
nRBTP	6		6	
WL Set A/B	11/19	MR1[7:4] = 1100	12/22	MR1[7:4] = 1101
nWR x16/x8	32/34	MR2[7:4] = 1100	37/39	MR2[7:4] = 1101
^t WCKPRE_static ²	5	Follows 7500 data rate	6	Follows 8533 data rate
^t WCKPRE_WR_toggle	4	Follows 3200 data rate	4	Follows 3200 data rate
^t WCKPRE_RD_toggle	10	Follows 3200 data rate	10	Follows 3200 data rate
^t WCKENL_FS	2	Follows 3200 data rate	2	Follows 3200 data rate
^t WCKPRE_toggle_FS ³	14	Minimum	16	Minimum
ODTLon	WL - 4	Follows 3200 data rate	WL - 4	Follows 3200 data rate
ODTLoff ⁴	WL + 5 (BL16), WL + 9 (BL32)	Follows 3200	WL + 5 (BL16), WL + 9 (BL32)	Follows 3200 data rate
ODTLoff_RD_DQ	RL - 4	Follows 3200 data rate	RL - 4	Follows 3200 data rate
ODTLoff_RD_RDQS	RL - 6	MR10 OP[1, 5:4] = 000, 001, 010	RL - 6	MR10 OP[1, 5:4] = 000, 001, 010
	RL - 8	MR10 OP[1, 5:4] = 011, 1XX	RL - 8	MR10 OP[1, 5:4] = 011, 1XX
ODTLon_RD_DQ ⁵	RL + 6 (BL16), RL + 10 (BL32)		RL + 6 (BL16), RL + 10 (BL32)	
ODTLon_RD_RDQS ⁶	RL + 8 (BL16), RL + 12 (BL32)		RL + 8 (BL16), RL + 12 (BL32)	

Notes: 1. Restricted to WCK:CK 2:1 ratio, WCK:CK 4:1 ratio not supported; Link ECC is disabled, and DVFSC/E-DVFSC is disabled.

2. Common for WR/RD/FS.

3. Minimum 1 + RL - (^tWCKENL_FS + ^tWCKPRE_Static) when CAS to RD is 1CK.

4. (WL + BL/n_min + RU(^tWCK2DQI(max)/^tCK)).

5. (RL + BL/n_min + RU(^tWCK2DQO(max)/^tCK)).

6. (RL + BL/n_min + RU(^tWCK2DQO(max)/^tCK)) + 2.

7. 8533 MT/s or higher data rated parts support 16-bank mode up to 4267 MT/s with restrictions, all other speed rated parts greater than 3200 MT/s per-pin and less than 8533 MT/s per-pin are restricted from the extended 16B



315b: x32 Automotive LPDDR5X SDRAM 16-Bank Extended Frequency

mode capabilities. Refer to the above table for constraints for operating in 16-bank mode when data rate is greater than 3200 MT/s per-pin and equal to or less than 4267 MT/s per-pin.

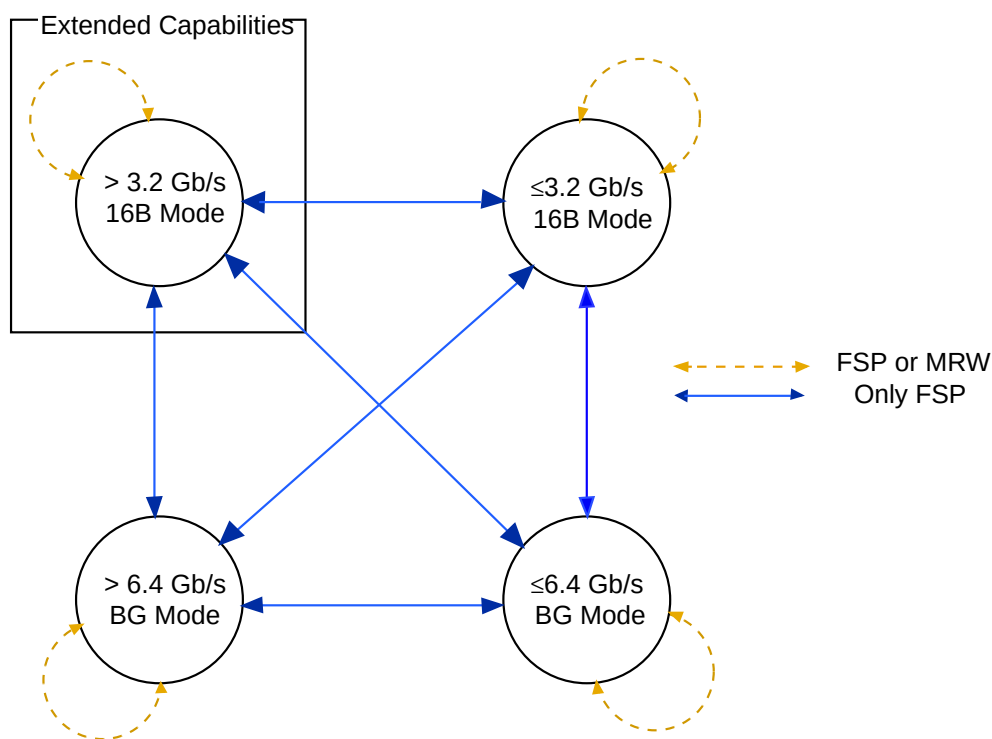
- When operating in the 16-bank mode, the FSP procedure must be used when setting the data rate above 3.2 Gb/s per-pin even when setting for the first time. For example, if the device is powered-up and initialized for 4266 Gb/s per-pin timing at the initial operation start, the FSP procedure must still be used. See Figure 4: 16B and BG Data Rate Change Flow Chart Showing Extended Capabilities on page 17 for details of FSP usage.

16B/BG Data Rate Change Diagram With FSP Requirements

The following flow chart diagram shows the needed 16-bank (16B) and bank group (BG) data rate change details and how the frequency set protocol (FSP) supports the extended frequency range.

The diagram below represents the device extended capabilities which are extended to 4267 Mb/s per-pin data rate in 16B mode.

Figure 4: 16B and BG Data Rate Change Flow Chart Showing Extended Capabilities

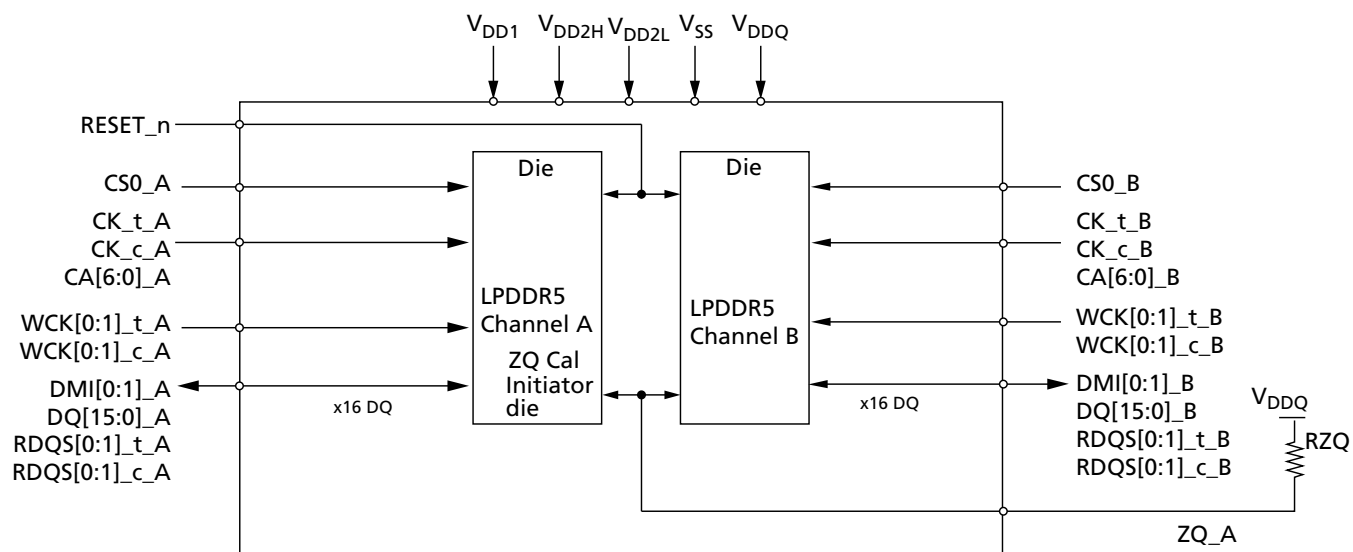




Package Block Diagrams

Dual Die, Dual Channel, Single Rank

Figure 5: Dual-Die, Dual-Channel, Single-Rank Package Block Diagram

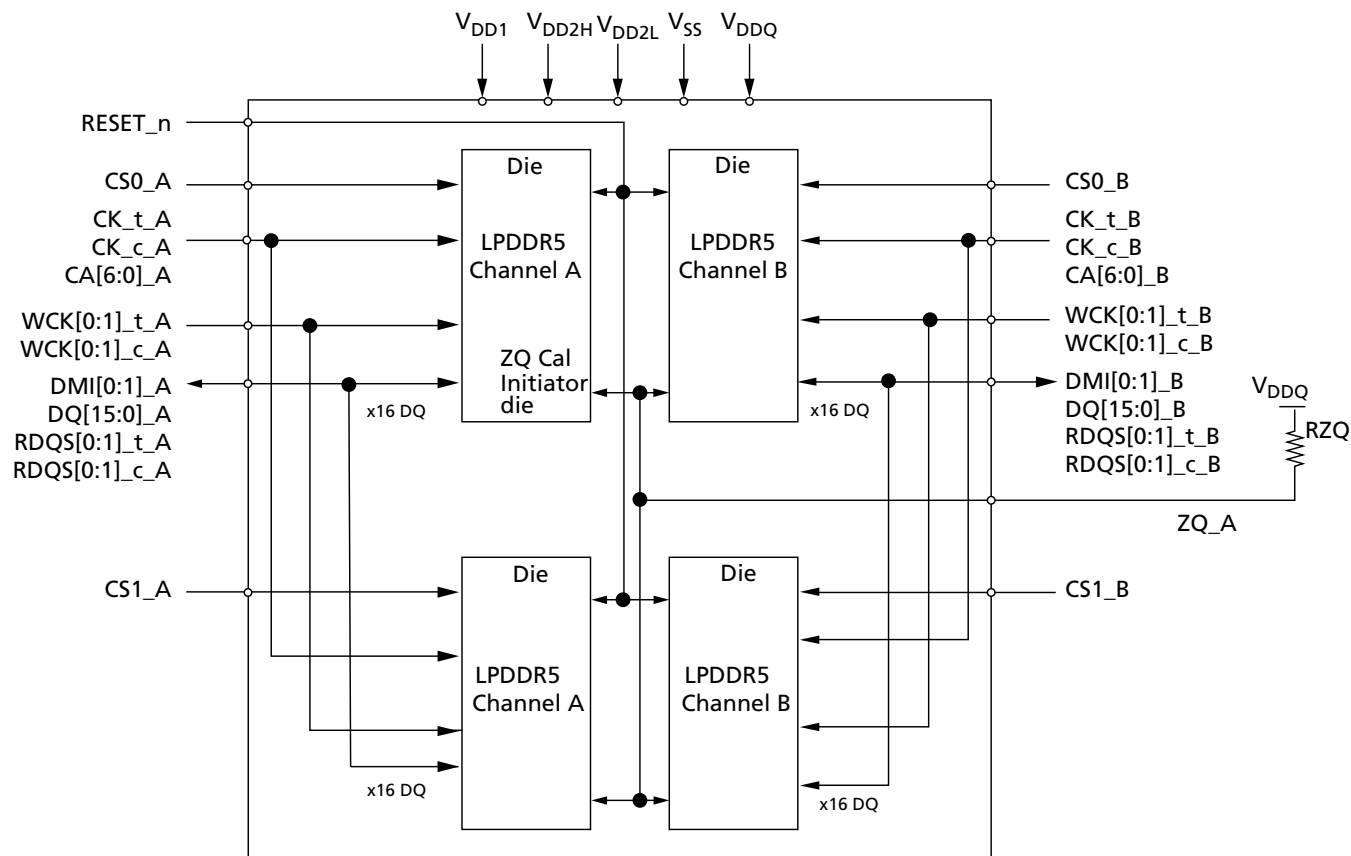




315b: x32 Automotive LPDDR5X SDRAM Package Block Diagrams

Quad Die, Dual Channel, Dual Rank

Figure 6: Quad-Die, Dual-Channel, Dual-Rank Package Block Diagram

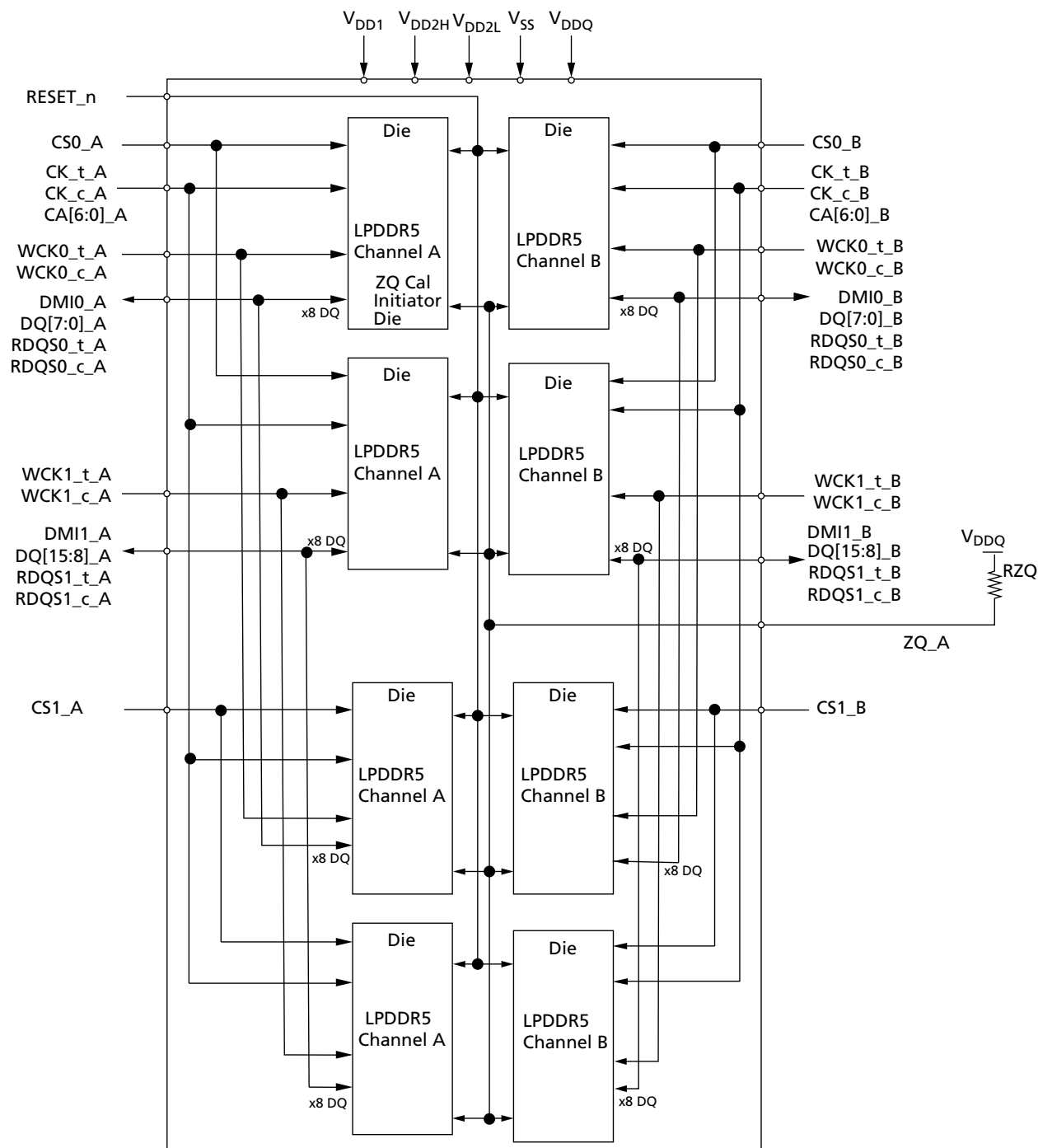




315b: x32 Automotive LPDDR5X SDRAM Package Block Diagrams

Eight Die, Dual Channel, Dual Rank

Figure 7: Eight-Die, Dual-Channel, Dual-Rank Package Block Diagram





315b: x32 Automotive LPDDR5X SDRAM Ball Assignments and Descriptions

Ball Assignments and Descriptions

315b Dual Channel, 1 Rank, 2 Rank

Table 9: 315-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:B], CK_c_[A:B]	Input	Clock: CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:B], CS1_[A:B]	Input	Chip select: CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] become NC pins in a single-rank package.
CA[6:0]_[A:B]	Input	Command/address inputs: Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:B], WCK[1:0]_c_[A:B]	Input	Data clock: WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_[A:B]	I/O	Data input/output: Bidirectional data bus.
RDQS[1:0]_t_[A:B], RDQS[1:0]_c_[A:B]	I/O Output	Read data strobe: RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:B]	I/O	Data mask inversion: DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A	Reference	ZQ calibration reference: Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V _{DDQ} through a 240 ohm ±1% resistor.
V _{DDQ} , V _{DD1} , V _{DD2H} , V _{DD2L}	Supply	Power supplies: Isolated on the die for improved noise immunity.
V _{SS}	Supply	Ground reference: Power supply ground reference.
RESET_n	Input	Reset: When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	No connect: Not internally connected.
RFU	–	Reserved Future Use: Not internally connected.



315b: x32 Automotive LPDDR5X SDRAM Ball Assignments and Descriptions

Figure 8: 315-Ball Dual-Channel Discrete FBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	NC	NC	V _{DDQ}	DMI0_A	V _{SS}	V _{DD2L}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2L}	V _{SS}	DMI1_A	V _{DDQ}	NC	NC	A
B	NC	V _{DDQ}	RDQS0_t_A	V _{SS}	DQ4_A	V _{DD2L}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2L}	DQ12_A	V _{SS}	RDQS1_t_A	V _{DDQ}	NC	B
C	V _{DD1}	DQ1_A	V _{DDQ}	RDQS0_c_A	V _{SS}	DQ5_A	V _{DD2H}	V _{SS}	V _{DD2H}	DQ13_A	V _{SS}	RDQS1_c_A	V _{DDQ}	DQ9_A	V _{DD1}	C
D	DQ0_A	V _{SS}	DQ3_A	V _{DDQ}	WCK0_c_A	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	WCK1_c_A	V _{DDQ}	DQ11_A	V _{SS}	DQ8_A	D
E	V _{SS}	DQ2_A	V _{SS}	WCK0_t_A	V _{DDQ}	DQ6_A	V _{DD2H}	V _{SS}	V _{DD2H}	DQ14_A	V _{DDQ}	WCK1_t_A	V _{SS}	DQ10_A	V _{SS}	E
F	V _{DDQ}	V _{SS}	V _{DDQ}	V _{DDQ}	DQ7_A	V _{DD2H}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2H}	DQ15_A	V _{DDQ}	V _{DDQ}	V _{SS}	V _{DDQ}	F
G	V _{DDQ}	V _{DDQ}	V _{SS}	CA0_A	V _{SS}	CS1_A	V _{SS}	CA2_A	V _{SS}	CA4_A	V _{SS}	CA6_A	V _{SS}	V _{DDQ}	V _{DDQ}	G
H	RESET_N	V _{DD2L}	V _{SS}	V _{SS}	CA1_A	V _{SS}	CS0_A	V _{SS}	CK_t_A	V _{SS}	CA3_A	V _{SS}	CA5_A	V _{DD2L}	ZQ_A	H
J	V _{SS}	V _{DD2L}	V _{SS}	RFU	V _{DD2H}	RFU	V _{SS}	V _{SS}	CK_c_A	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	V _{DD2L}	V _{SS}	J
K	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	K
L	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	L
M	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	M
N	V _{SS}	V _{DD2L}	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	CK_c_B	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	V _{DD2L}	V _{SS}	N
P	RFU	V _{DD2L}	CA5_B	V _{SS}	CA3_B	V _{SS}	CK_t_B	V _{SS}	CS0_B	V _{SS}	CA1_B	V _{SS}	V _{SS}	V _{DD2L}	RFU	P
R	V _{DDQ}	V _{DDQ}	V _{SS}	CA6_B	V _{SS}	CA4_B	V _{SS}	CA2_B	V _{SS}	CS1_B	V _{SS}	CA0_B	V _{SS}	V _{DDQ}	V _{DDQ}	R
T	V _{DDQ}	V _{SS}	V _{DDQ}	V _{DDQ}	DQ15_B	V _{DD2H}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2H}	DQ7_B	V _{DDQ}	V _{DDQ}	V _{SS}	V _{DDQ}	T
U	V _{SS}	DQ10_B	V _{SS}	WCK1_t_B	V _{DDQ}	DQ14_B	V _{DD2H}	V _{SS}	V _{DD2H}	DQ6_B	V _{DDQ}	WCK0_t_B	V _{SS}	DQ2_B	V _{SS}	U
V	DQ8_B	V _{SS}	DQ11_B	V _{DDQ}	WCK1_c_B	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	WCK0_c_B	V _{DDQ}	DQ3_B	V _{SS}	DQ0_B	V
W	V _{DD1}	DQ9_B	V _{DDQ}	RDQS1_c_B	V _{SS}	DQ13_B	V _{DD2H}	V _{SS}	V _{DD2H}	DQ5_B	V _{SS}	RDQS0_c_B	V _{DDQ}	DQ1_B	V _{DD1}	W
Y	NC	V _{DDQ}	RDQS1_t_B	V _{SS}	DQ12_B	V _{DD2L}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2L}	DQ4_B	V _{SS}	RDQS0_t_B	V _{DDQ}	NC	Y
AA	NC	NC	V _{DDQ}	DMI1_B	V _{SS}	V _{DD2L}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2L}	V _{SS}	DMI0_B	V _{DDQ}	NC	NC	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Top View (ball down)

V_{SS}
 V_{DD1}
 V_{DD2H}
 V_{DD2L}
 V_{DDQ}
 CK
 RDQS
 WCK
 DQ,DMI
 CA, CS, ZQ, RESET
 NC, RFU

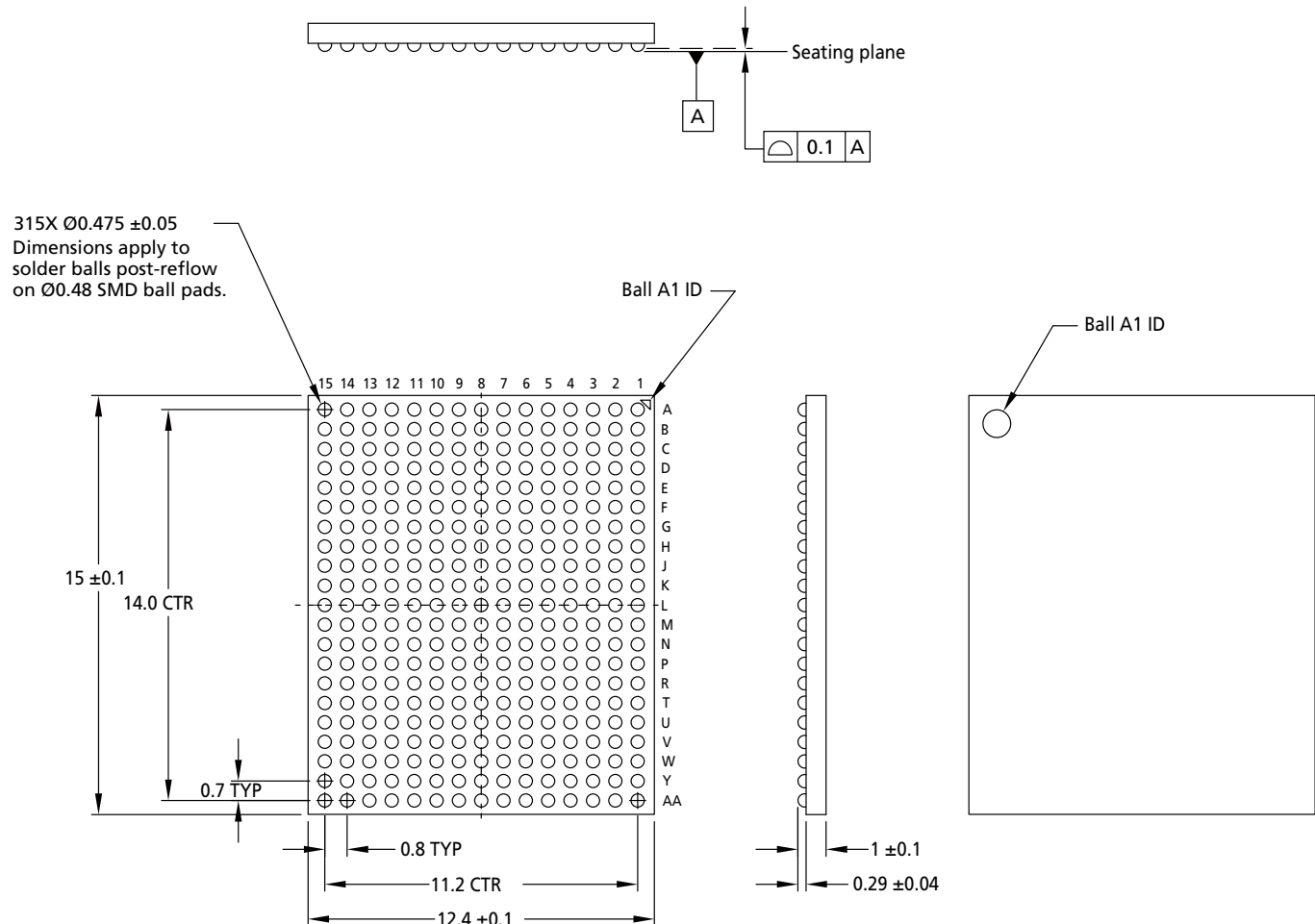


315b: x32 Automotive LPDDR5X SDRAM Package Dimensions

Package Dimensions

315-Ball Package (Package Code: DS)

Figure 9: 315-Ball TFBGA – 12.4mm (TYP) × 15.0mm (TYP) × 1.1mm (MAX) (Package Code: DS)



Notes: 1. All dimensions are in millimeters.

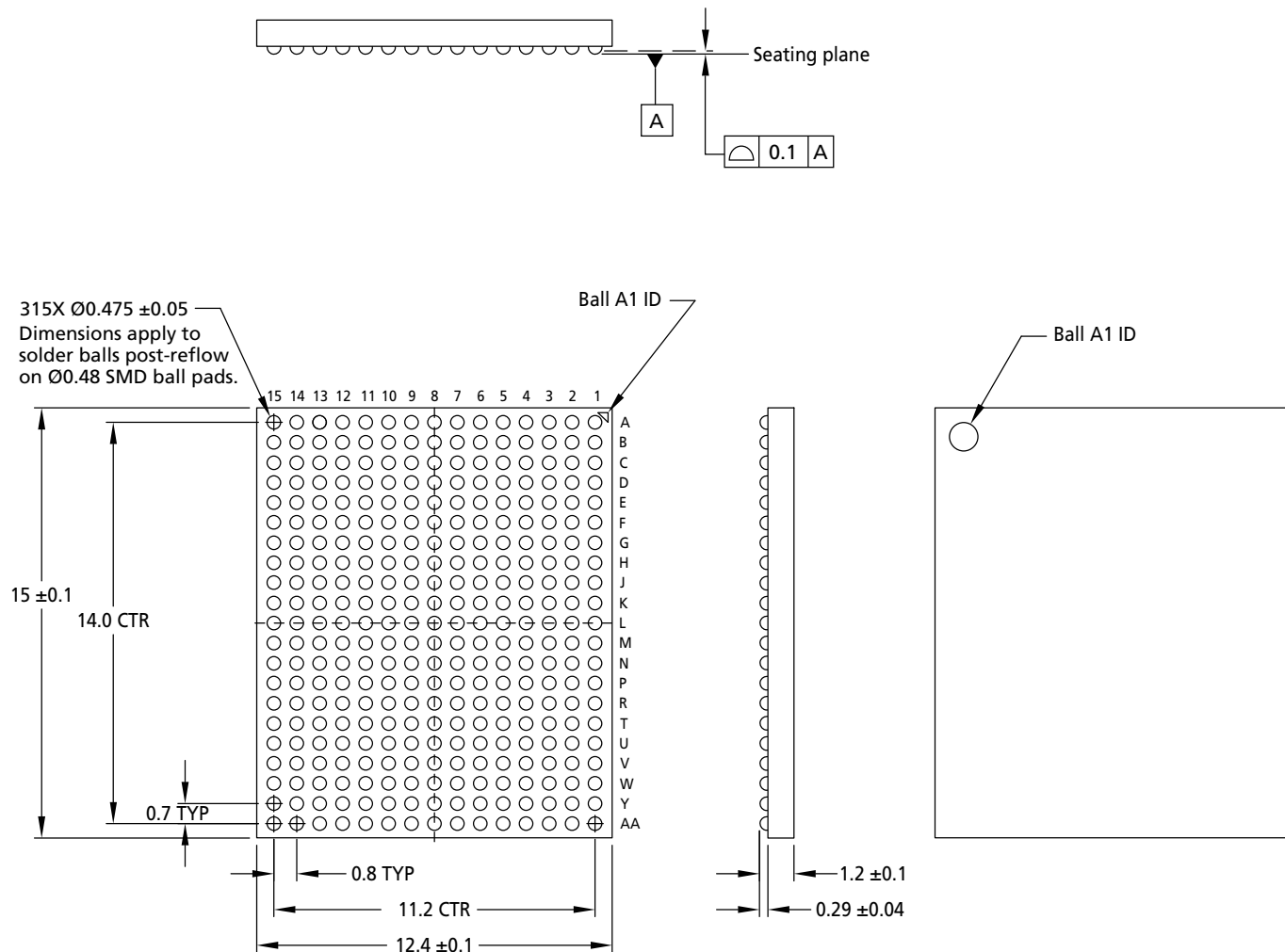
2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni)



315b: x32 Automotive LPDDR5X SDRAM Package Dimensions

315-Ball Package (Package Code: DV)

Figure 10: 315-Ball LFBGA – 12.4mm (TYP) × 15.0mm (TYP) × 1.3mm (MAX) (Package Code: DV)



Notes: 1. All dimensions are in millimeters.

2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni)


**315b: x32 Automotive LPDDR5X SDRAM
Package Dimensions**
Package Thermal Impedance
Table 10: Package Thermal Impedance Characteristics

Die Revision	Package	Parameter	Symbol	Value	Unit
Rev F	315-ball, DDP, package code DS	Junction-to-case (TOP)	Θ_{JC}	4.8	°C/W
		Junction-to-board	Θ_{JB}	12.5	°C/W
	315-ball, QDP, package code DS	Junction-to-case (TOP)	Θ_{JC}	4.1	°C/W
		Junction-to-board	Θ_{JB}	14.5	°C/W
	315-ball, 8DP, package code DV	Junction-to-case (TOP)	Θ_{JC}	4.4	°C/W
		Junction-to-board	Θ_{JB}	15.6	°C/W

Note: 1. Thermal impedance values provided are for reference only. These values are based on a model and represent a maximum characteristic.


**315b: x32 Automotive LPDDR5X SDRAM
Product-Specific Mode Register Definition**
Product-Specific Mode Register Definition
Table 11: Mode Register Contents

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0	Per-pin DFE	Pre Emphasis	Unified NT ODT behavior mode	DMI output behavior mode	Optimized refresh mode	Enhanced WCK always-on mode	Latency mode	NT ODT timing mode
	OP[0] = 1b: Device supports different NT ODT latency for DQ and RDQS							
	OP[1] = 0b: Device supports x16 mode latency for 1G32, 2G32 OP[1] = 1b: Device supports x8 mode latency for 4G32							
	OP[2] = 1b: Device supports enhanced WCK always-on mode							
	OP[3] = 1b: Device supports optimized refresh mode							
	OP[4] = 1b: Device supports both DMI behavior mode 1 and 2 and mode selection							
	OP[5] = 1b: The NT ODT behavior follows the unified NT ODT behavior							
	OP[6] = 1b: Device supports Pre Emphasis mode							
	OP[7] = 1b: Device supports Per Pin DFE							
MR1						DRFM support ³	ARFM support ³	CS ODT OP support
	OP[0] = 1b: Device supports CS ODT behavior OP							
	OP[1] = 1b: Device supports ARFM							
	OP[2] = 0b: Device does not support DRFM							
MR3				BK/BG ORG				
	OP[4:3] = 00b: BG mode supported							
	01b: 8B mode not supported							
	10b: 16B Mode supported							
	11b: RFU							
MR4				Refresh Multiplier (Note 7, 8)				
	OP[4:0]: Refer to General LPDDR5/LPDDR5X Specification 1 for mode register definitions.							
MR5	Manufacturer ID							
	1111 1111b: Micron							
MR6	Revision ID1							
	0010 1000b							
MR8	I/O width		Density				Device Type ⁶	
	OP[7:6] = 00b: x16 for 1G32, 2G32 OP[7:6] = 01b: x8 for 4G32		OP[5:2] = 0110b: 16Gb				OP[1:0] = 01b: LPDDR5X SDRAM (up to 8533 Mb/s) OP[1:0] = 10b: LPDDR5X SDRAM (up to 9600 Mb/s)	
MR13						VRO		
	OP[2] = 0b: Normal operation (default) 1b: Output the V _{REF(CA)} value on DQ7 and V _{REF(DQ)} value on DQ6							


**315b: x32 Automotive LPDDR5X SDRAM
Product-Specific Mode Register Definition**
Table 11: Mode Register Contents (Continued)

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR19			WCK2DQ OSC FM					
	OP[5] = 1b: WCK2DQ OSC FM supported							
MR21	WXS				ODTD- CSFS	WXFS	RDCFS	WDCFS
	OP[0] = 1b: WRITE DATA COPY function supported							
	OP[1] = 1b: READ DATA COPY function supported							
	OP[2] = 1b: WRITE X function supported							
	OP[3] = 1b: Device ODTD-CS is supported							
	OP[7] = 1b: Data to be written can be selected with 0 and 1							
MR22	RECC		WECC					
	OP[5:4] = 00b: Write link ECC disabled (default) 01b: Write link ECC enabled (See Note 4)							
	OP[7:6] = 00b: Read link ECC disabled (default) 01b: Read link ECC enabled (See Note 4)							
MR24	DFES				Read DCA			
	OP[3] = 1b: Device supports Read DCA							
	OP[7] = 1b: Device supports DFE (See Note 5)							
MR26		RDQSTFS						
	OP[6] = 1b: Read/write-based RDQS_t TRAINING function supported							
MR27	RAAMULT		RAAIMT					RFM
	OP[0] = 1b: RFM is required							
	OP[5:1] = 00101b: 40							
	OP[7:6] = 01b: 4X							
MR41					E-DVFSC ODT	DVFSC/ E-DVFSC Support		
	OP[2:1] = 10b: Both DVFSC and Enhanced DVFSC Mode supported							
	OP[3] = 0b: Enhanced DVFSC ODT option not supported							
MR43		SBEC rule						
	OP[6] = 1b: Simultaneous SBE on each DQ byte and DMI are independently counted							
MR57	ARFM ³		RFMSB		RFMSB		RAADEC	
	OP[1:0] = 10b: 2 × RAAIMT							
	OP[3:2] = 00b: Single Bank Mode not supported							
	OP[5:4] = 00b: One RAA counter per two banks (1 of 8)							
	OP[7:6] = 00b: default (00101b: 40), 01b: Level A, 10b: Level B, 11b: Level C							

Notes: 1. The contents of mode registers described here reflect information specific to each die in these packages.

2. Refer to General LPDDR5/LPDDR5X Specification 1 for mode registers not described here.

3. Refer to General LPDDR5/LPDDR5X Specification 3 for feature description not described here.

4. Write link ECC and read link ECC are supported.

5. Device supports 7-step DFE.

6. Device type only supports Bank Group and 16B modes.

**315b: x32 Automotive LPDDR5X SDRAM
Product-Specific Mode Register Definition**

-
7. MR4:OP[4:0] output from each die in a defined package shall be used to determine the required package level refresh rate. Any other method used to determine a valid refresh rate, places ownership and responsibility of the correct refresh rate on the system developer or end user. TOPER (case surface temperature) shall be used to determine whether operating temperature requirements are being met. Any other method used to determine operating temperature, places ownership and responsibility of the correct operating temperature on the system developer or end user.
 8. The intent of a MR4 OP[4:0] output of <01111> is to not to support a refresh rate of 0.125xd; rather a method to inform the host the die temperature is most likely being operated beyond its supported upper maximum limit and the host should immediately place the DRAM in to a refresh only state at 0.125xd refresh rate until the MR4 readout of <01111> no longer exists. No other operation other than refresh should be conducted.


315b: x32 Automotive LPDDR5X SDRAM
I_{DD} Parameters
I_{DD} Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section in General LPDDR5/LPDDR5X Specifications 2 for detailed conditions.

Table 12: I_{DD} Parameters at 7500 Mb/s – Single Die

Symbol	Supply	x8 Mode			x16 Mode			Unit	Note
		UT	AT	IT	UT	AT	IT		
I _{DD01}	V _{DD1}	4.4	4.1	4.1	4.4	4.1	4.1	mA	
I _{DD02H}	V _{DD2H}	86	63	63	91	66	66		
I _{DD02L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD0Q}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2P1}	V _{DD1}	2.4	1.6	1.6	2.4	1.6	1.6	mA	
I _{DD2P2H}	V _{DD2H}	8.5	5.5	5.5	8.5	5.5	5.5		
I _{DD2P2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2PQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2PS1}	V _{DD1}	2.4	1.6	1.6	2.4	1.6	1.6	mA	
I _{DD2PS2H}	V _{DD2H}	8.5	5.5	5.5	8.5	5.5	5.5		
I _{DD2PS2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2PSQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2N1}	V _{DD1}	2.4	1.6	1.6	2.4	1.6	1.6	mA	
I _{DD2N2H}	V _{DD2H}	61	43	43	66	46	46		
I _{DD2N2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2NQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2NS1}	V _{DD1}	2.4	1.6	1.6	2.4	1.6	1.6	mA	
I _{DD2NS2H}	V _{DD2H}	61	43	43	66	46	46		
I _{DD2NS2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2NSQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD3P1}	V _{DD1}	3.5	2.8	2.8	3.6	2.9	2.9	mA	
I _{DD3P2H}	V _{DD2H}	23.5	15.5	15.5	23.5	15.5	15.5		
I _{DD3P2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD3PQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD3PS1}	V _{DD1}	3.5	2.8	2.8	3.6	2.9	2.9	mA	
I _{DD3PS2H}	V _{DD2H}	23.5	15.5	15.5	23.5	15.5	15.5		
I _{DD3PS2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD3PSQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD3N1}	V _{DD1}	4	3.1	3.1	4	3.1	3.1	mA	
I _{DD3N2H}	V _{DD2H}	76.5	53.5	53.5	81.5	56.5	56.5		
I _{DD3N2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD3NQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		


315b: x32 Automotive LPDDR5X SDRAM
I_{DD} Parameters
Table 12: I_{DD} Parameters at 7500 Mb/s – Single Die (Continued)

Symbol	Supply	x8 Mode			x16 Mode			Unit	Note
		UT	AT	IT	UT	AT	IT		
I _{DD4R1}	V _{DD1}	18.5	17.5	17.5	20	19	19	mA	3, 4, 6
I _{DD4R2H}	V _{DD2H}	305	275	275	455	420	420		
I _{DD4R2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD4RQ}	V _{DDQ}	61	61	61	122	122	122		
I _{DD4W1}	V _{DD1}	17	16	16	18	17	17	mA	3, 6
I _{DD4W2H}	V _{DD2H}	220	195	195	325	295	295		
I _{DD4W2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD4WQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD51}	V _{DD1}	25	24	24	25	24	24	mA	
I _{DD52H}	V _{DD2H}	285	235	235	285	235	235		
I _{DD52L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD5Q}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD5AB1}	V _{DD1}	4	3.6	3.6	4	3.6	3.6	mA	
I _{DD5AB2H}	V _{DD2H}	76	55	55	81	56	56		
I _{DD5AB2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD5ABQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD5PB1}	V _{DD1}	4	3.6	3.6	4	3.6	3.6	mA	
I _{DD5PB2H}	V _{DD2H}	76	55	55	81	56	56		
I _{DD5PB2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD5PBQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		

- Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode enabled. Enhanced DVFSQ and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V (DVFSQ disabled)/0.27–0.37V (DVFSQ enabled)
6. IDD4R2 and IDD4W2 have implemented a more stringent pattern than required by JEDEC and therefore these IDD values are slightly higher than if the JEDEC pattern was used.
7. Notes 1, 2, and 5 apply to entire table.


315b: x32 Automotive LPDDR5X SDRAM
I_{DD} Parameters
Table 13: I_{DD} Parameters at 8533 Mb/s – Single Die

Symbol	Supply	x8 Mode			x16 Mode			Unit	Note
		UT	AT	IT	UT	AT	IT		
I _{DD01}	V _{DD1}	4.4	4.1	4.1	4.4	4.1	4.1	mA	
I _{DD02H}	V _{DD2H}	86	63	63	91	66	66		
I _{DD02L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD0Q}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2P1}	V _{DD1}	2.4	1.6	1.6	2.4	1.6	1.6	mA	
I _{DD2P2H}	V _{DD2H}	8.5	5.5	5.5	8.5	5.5	5.5		
I _{DD2P2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2PQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2PS1}	V _{DD1}	2.4	1.6	1.6	2.4	1.6	1.6	mA	
I _{DD2PS2H}	V _{DD2H}	8.5	5.5	5.5	8.5	5.5	5.5		
I _{DD2PS2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2PSQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2N1}	V _{DD1}	2.4	1.6	1.6	2.4	1.6	1.6	mA	
I _{DD2N2H}	V _{DD2H}	61	43	43	66	46	46		
I _{DD2N2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2NQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2NS1}	V _{DD1}	2.4	1.6	1.6	2.4	1.6	1.6	mA	
I _{DD2NS2H}	V _{DD2H}	61	43	43	66	46	46		
I _{DD2NS2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2NSQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD3P1}	V _{DD1}	3.5	2.8	2.8	3.6	2.9	2.9	mA	
I _{DD3P2H}	V _{DD2H}	23.5	15.5	15.5	23.5	15.5	15.5		
I _{DD3P2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD3PQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD3PS1}	V _{DD1}	3.5	2.8	2.8	3.6	2.9	2.9	mA	
I _{DD3PS2H}	V _{DD2H}	23.5	15.5	15.5	23.5	15.5	15.5		
I _{DD3PS2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD3PSQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD3N1}	V _{DD1}	4	3.1	3.1	4	3.1	3.1	mA	
I _{DD3N2H}	V _{DD2H}	76.5	53.5	53.5	81.5	56.5	56.5		
I _{DD3N2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD3NQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD4R1}	V _{DD1}	20.5	19.5	19.5	22	21	21	mA	3, 4, 6
I _{DD4R2H}	V _{DD2H}	325	295	295	495	455	455		
I _{DD4R2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD4RQ}	V _{DDQ}	66	66	66	131	131	131		


315b: x32 Automotive LPDDR5X SDRAM
I_{DD} Parameters
Table 13: I_{DD} Parameters at 8533 Mb/s – Single Die (Continued)

Symbol	Supply	x8 Mode			x16 Mode			Unit	Note
		UT	AT	IT	UT	AT	IT		
I _{DD4W1}	V _{DD1}	19	18	18	20	19	19	mA	3, 6
I _{DD4W2H}	V _{DD2H}	235	210	210	30	320	320		
I _{DD4W2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD4WQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD51}	V _{DD1}	25	24	24	25	24	24	mA	
I _{DD52H}	V _{DD2H}	285	235	235	285	235	235		
I _{DD52L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD5Q}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD5AB1}	V _{DD1}	4	3.6	3.6	4	3.6	3.6	mA	
I _{DD5AB2H}	V _{DD2H}	76	55	55	81	56	56		
I _{DD5AB2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD5ABQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD5PB1}	V _{DD1}	4	3.6	3.6	4	3.6	3.6	mA	
I _{DD5PB2H}	V _{DD2H}	76	55	55	81	56	56		
I _{DD5PB2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD5PBQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		

- Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode enabled. Enhanced DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V (DVFSQ disabled)/0.27–0.37V (DVFSQ enabled)
6. IDD4R2 and IDD4W2 have implemented a more stringent pattern than required by JEDEC and therefore these IDD values are slightly higher than if the JEDEC pattern was used.
7. Notes 1, 2, and 5 apply to entire table.


315b: x32 Automotive LPDDR5X SDRAM
I_{DD} Parameters
Table 14: I_{DD} Parameters at 9600 Mb/s – Single Die

Symbol	Supply	x8 Mode			x16 Mode			Unit	Note
		UT	AT	IT	UT	AT	IT		
I _{DD01}	V _{DD1}	4.4	4.1	4.1	4.4	4.1	4.1	mA	
I _{DD02H}	V _{DD2H}	86	63	63	91	66	66		
I _{DD02L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD0Q}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2P1}	V _{DD1}	2.4	1.6	1.6	2.4	1.6	1.6	mA	
I _{DD2P2H}	V _{DD2H}	8.5	5.5	5.5	8.5	5.5	5.5		
I _{DD2P2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2PQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2PS1}	V _{DD1}	2.4	1.6	1.6	2.4	1.6	1.6	mA	
I _{DD2PS2H}	V _{DD2H}	8.5	5.5	5.5	8.5	5.5	5.5		
I _{DD2PS2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2PSQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2N1}	V _{DD1}	2.4	1.6	1.6	2.4	1.6	1.6	mA	
I _{DD2N2H}	V _{DD2H}	61	43	43	66	46	46		
I _{DD2N2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2NQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2NS1}	V _{DD1}	2.4	1.6	1.6	2.4	1.6	1.6	mA	
I _{DD2NS2H}	V _{DD2H}	61	43	43	66	46	46		
I _{DD2NS2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2NSQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD3P1}	V _{DD1}	3.5	2.8	2.8	3.6	2.9	2.9	mA	
I _{DD3P2H}	V _{DD2H}	23.5	15.5	15.5	23.5	15.5	15.5		
I _{DD3P2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD3PQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD3PS1}	V _{DD1}	3.5	2.8	2.8	3.6	2.9	2.9	mA	
I _{DD3PS2H}	V _{DD2H}	23.5	15.5	15.5	23.5	15.5	15.5		
I _{DD3PS2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD3PSQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD3N1}	V _{DD1}	4	3.1	3.1	4	3.1	3.1	mA	
I _{DD3N2H}	V _{DD2H}	76.5	53.5	53.5	81.5	56.5	56.5		
I _{DD3N2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD3NQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD4R1}	V _{DD1}	22.5	21.5	21.5	24	23	23	mA	3, 4, 6
I _{DD4R2H}	V _{DD2H}	345	315	315	530	495	495		
I _{DD4R2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD4RQ}	V _{DDQ}	70	70	70	139	139	139		


315b: x32 Automotive LPDDR5X SDRAM
I_{DD} Parameters
Table 14: I_{DD} Parameters at 9600 Mb/s – Single Die (Continued)

Symbol	Supply	x8 Mode			x16 Mode			Unit	Note
		UT	AT	IT	UT	AT	IT		
I _{DD4W1}	V _{DD1}	21	20	20	22	21	21	mA	3, 6
I _{DD4W2H}	V _{DD2H}	250	225	225	380	350	350		
I _{DD4W2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD4WQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD51}	V _{DD1}	25	24	24	25	24	24	mA	
I _{DD52H}	V _{DD2H}	285	235	235	285	235	235		
I _{DD52L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD5Q}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD5AB1}	V _{DD1}	4	3.6	3.6	4	3.6	3.6	mA	
I _{DD5AB2H}	V _{DD2H}	76	55	55	81	56	56		
I _{DD5AB2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD5ABQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD5PB1}	V _{DD1}	4	3.6	3.6	4	3.6	3.6	mA	
I _{DD5PB2H}	V _{DD2H}	76	55	55	81	56	56		
I _{DD5PB2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD5PBQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		

- Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode enabled. Enhanced DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V (DVFSQ disabled)/0.27–0.37V (DVFSQ enabled)
6. IDD4R2 and IDD4W2 have implemented a more stringent pattern than required by JEDEC and therefore these IDD values are slightly higher than if the JEDEC pattern was used.
7. Notes 1, 2, and 5 apply to entire table.


315b: x32 Automotive LPDDR5X SDRAM
I_{DD} Parameters
Table 15: I_{DD} Parameters at 3200 Mb/s – With Enhanced DVFS Enabled - Single Die

Symbol	Supply	x8 Mode			x16 Mode			Unit	Note
		UT	AT	IT	UT	AT	IT		
I _{DD4R-DVFS} C1	V _{DD1}	11	10	10	12	11	11	mA	3, 4, 6
I _{DD4R-DVFS} C2H	V _{DD2H}	40	31	31	42	33	33		
I _{DD4R-DVFS} C2L	V _{DD2L}	86	73	73	140	120	120		
I _{DD4R-DVFS} CQ	V _{DDQ}	44	44	44	88	88	88		
I _{DD4W-DVFS} C1	V _{DD1}	10	9	9	10.5	9.5	9.5	mA	3, 6
I _{DD4W-DVFS} C2H	V _{DD2H}	37	28	28	40	30	30		
I _{DD4W-DVFS} C2L	V _{DD2L}	71	57	57	110	95	95		
I _{DD4W-DVFS} CQ	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD5ED} 1	V _{DD1}	22	21	21	22	21	21	mA	
I _{DD5ED} 2H	V _{DD2H}	245	195	195	245	195	195		
I _{DD5ED} 2L	V _{DD2L}	39	26.5	26.5	39	26.5	26.5		
I _{DD5ED} Q	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD5ABED} 1	V _{DD1}	3.8	3.4	3.4	3.8	3.4	3.4	mA	
I _{DD5ABED} 2H	V _{DD2H}	36	28	28	37	28	28		
I _{DD5ABED} 2L	V _{DD2L}	31	22	22	35	26	26		
I _{DD5ABED} Q	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD5PBED} 1	V _{DD1}	3.8	3.4	3.4	3.8	3.4	3.4	mA	
I _{DD5PBED} 2H	V _{DD2H}	36	28	28	37	28	28		
I _{DD5PBED} 2L	V _{DD2L}	31	22	22	35	26	26		
I _{DD5PBED} Q	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		

- Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. Enhanced DVFS enabled, DVFSQ enabled, 3200 Mb/s, 16B mode
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V (DVFSQ disabled)/0.27–0.37V (DVFSQ enabled)
6. IDD4R2 and IDD4W2 have implemented a more stringent pattern than required by JEDEC and therefore these IDD values are slightly higher than if the JEDEC pattern was used.
7. Notes 1, 2, and 5 apply to entire table.


315b: x32 Automotive LPDDR5X SDRAM
I_{DD} Parameters
Table 16: Full-Array Power-Down Self Refresh Current – Single Die

Temperature	Symbol	Supply	Value	Unit	Notes
25°C	I _{DD61}	V _{DD1}	0.25	mA	
	I _{DD62H}	V _{DD2H}	0.6		
	I _{DD62L}	V _{DD2L}	2.0	uA	4
	I _{DD6Q}	V _{DDQ}	30.0		
	I _{DD6DS1}	V _{DD1}	0.25	mA	
	I _{DD6DS2H}	V _{DD2H}	0.6		
	I _{DD6DS2L}	V _{DD2L}	2.0	uA	4
	I _{DD6DSQ}	V _{DDQ}	30.0		
45°C	I _{DD61}	V _{DD1}	0.32	mA	
	I _{DD62H}	V _{DD2H}	1.1		
	I _{DD62L}	V _{DD2L}	2.0	uA	4
	I _{DD6Q}	V _{DDQ}	30.0		
	I _{DD6DS1}	V _{DD1}	0.32	mA	
	I _{DD6DS2H}	V _{DD2H}	1.1		
	I _{DD6DS2L}	V _{DD2L}	2.0	uA	4
	I _{DD6DSQ}	V _{DDQ}	30.0		
65°C	I _{DD61}	V _{DD1}	0.58	mA	
	I _{DD62H}	V _{DD2H}	2.7		
	I _{DD62L}	V _{DD2L}	2.0	uA	4
	I _{DD6Q}	V _{DDQ}	30.0		
	I _{DD6DS1}	V _{DD1}	0.58	mA	
	I _{DD6DS2H}	V _{DD2H}	2.7		
	I _{DD6DS2L}	V _{DD2L}	2.0	uA	4
	I _{DD6DSQ}	V _{DDQ}	30.0		
85°C	I _{DD61}	V _{DD1}	3.5	mA	
	I _{DD62H}	V _{DD2H}	20.8		
	I _{DD62L}	V _{DD2L}	0.2	mA	4
	I _{DD6Q}	V _{DDQ}	0.6		
	I _{DD6DS1}	V _{DD1}	3.5	mA	
	I _{DD6DS2H}	V _{DD2H}	20.8		
	I _{DD6DS2L}	V _{DD2L}	0.2	mA	4
	I _{DD6DSQ}	V _{DDQ}	0.6		

- Notes: 1. I_{DD625/45/65°C} is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD685°C} is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. DVFS_C and DVFS_Q disabled.
3. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V
4. While entering and exiting Self-Refresh modes, all defined/used supply rails (V_{DD1}, V_{DD2H}, V_{DD2L}, V_{DDQ}) are required to be at valid levels. After the Self-Refresh with Power down mode entrance commands are completed and t_{ESPD} timing requirement has been satisfied, the V_{DDQ} power rail may be turned off by the controller.



Revision History

Rev. G – 05/2025

- Updated Features page
- Updated Part Number Ordering Information page
- Updated Important Notes and Warnings page
- Added Automotive Product Notes Page
- Updated Functional Safety, DLEP & RAS Notes page
- Updated Mode Register settings
- Updated note on thermal impedance page

Rev. F – 11/2024

- Added "F" MPNs to Part Number List table

Rev. E – 10/2024

- Updated IDD tables
- Updated mode register settings to show support for both LDVFS and EDVFS

Rev. D – 08/2024

- Added RxMask adjusted spec for 9600Mbps data rate.
- Added IDD4W2 and IDD4R2 related note to the datasheet

Rev. C – 05/2024

- Updated legal status to Preliminary
- Updated Mode Register Contents table to show no DRFM support
- Changed Thermal Resistance to Thermal Impedance

Rev. B – 12/2023

- Updated timing parameters for 9600Mbps
- Corrected IDD6 labels which were missing the “DS” for Deep Sleep Mode
- Updated important notes and warnings section
- Updated General Notes to highlight precedence between core data sheet and specific data sheet
- Added adjustments to CS Rx and DQ Rx mask parameters
- Updated MR1: Added DRFM support bit definition
- Updated MR24: Added DFE support bit setting
- Added DVFS enabled I_{DD} parameters to I_{DD} tables. Parameters affected = I_{DD4R} , I_{DD4W}
- Updated I_{DD6} Note 4 to align with core data sheet description
- Added I_{DD6} table entries for 45°C and 65°C, adjusted I_{DD6IT} limits to align with WT
- Removed I_{DD3NS} from I_{DD} tables
- Added table for DQ Rx adjustments at 3200Mhz
- Added clarification to IDD table notes

Rev. A – 10/2023

- Initial data sheet release

**315b: x32 Automotive LPDDR5X SDRAM**
Revision History

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