LPDDR5X SDRAM

MT62F1G16D1, MT62F1G32D2, MT62F2G32D4, MT62F4G32D8, MT62F1G64D4, MT62F2G64D8

Features

- **Architecture**
  - 17.1 GB/s maximum bandwidth per channel
  - Frequency range: 1067–5 MHz (data rate range per pin: 8533–40 Mb/s with WCK:CK = 4:1)
  - Selectable CKR (WCK:CK = 2:1 or 4:1)
- **LPDDR5X/LPDDR5 data interface**
  - Single x16 channel/die
  - Double-data-rate command/address entry
  - Differential command clocks (CK_t/CK_c) for high-speed operation
  - Differential data clocks (WCK_t/WCK_c)
  - Optional differential read strobe (RDQS_t/RDQS_c)
  - 16*n*-bit or 32*n*-bit prefetch architecture
  - Bank Architecture: Bank Group (BG) mode, and 16-bank (16B) mode supported
  - Command-selectable burst lengths (BL = 16 or 32) in bank group or 16-bank modes
  - Background ZQ calibration/command-based ZQ calibration
  - Optional link protection (link ECC)
  - Partial-array self refresh (PASR) and partial-array auto refresh (PAAR) with segment mask
- **Ultra-low-voltage core and I/O power supplies**
  - V_{DD1} = 1.70–1.95V; 1.80V TYP
  - V_{DD2H} = 1.01–1.12V; 1.05V TYP
  - V_{DD2L} = V_{DD2H} or 0.87–0.97V; 0.90V TYP
  - V_{DDQ} = 0.50V or 0.45V[1] TYP; 0.30V TYP (ODT off only)
- **I/O characteristics**
  - Interface-LVSTL 0.5/0.3
  - I/O type: Low-swing single-ended, V_{SS} terminated
  - V_{OH}-compensated output drive
  - Programmable V_{SS} on-die termination (ODT)
  - Non target ODT support
  - DVFSQ support
  - Per byte and per pin DFE support
- **Low power features**
  - Enhanced DVFSC: Enhanced dynamic voltage frequency scaling core
  - Single-ended CK, single-ended WCK and single-ended RDQS
  - Data copy
  - Write X

Options	Marking
Operating Voltage	F
– V_{DD1}/V_{DD2H}/V_{DD2L}/V_{DDQ}/V_{DDQ} (ODT off only):1.80V/1.05V/V_{DD2H} or 0.90V/0.50V or 0.45V[1]/0.30V	
Array Configuration	
– 1Gb x 16 (1Gbx16 x 1 Die x 1Ch x 1R)	1G16
– 1Gb x 32 (1Gbx16 x 1 Die x 2Ch x 1R)	1G32
– 2Gb x 32 (1Gbx16 x 1 Die x 2Ch x 2R)	2G32
– 4Gb x 32 (2Gbx8 x 2 Die x 2Ch x 2R)	4G32
– 1Gb x 64 (1Gbx16 x 1 Die x 4Ch x 1R)	1G64
– 2Gb x 64 (1Gbx16 x 1 Die x 4Ch x 2R)	2G64
Device configuration	
– 1 die in package (1Gb16 x 1 die)	D1
– 2 die in package (1Gb16 x 2 die)	D2
– 4 die in package (1Gb16 x 4 die)	D4
– 8 die in package (2Gb8 x 8 die, 1Gb16 x 8 die)	D8
FBGA RoHS-compliant "green" package	
– 315-ball TFBGA: 12.4mm x 15.0mm (TYP), seated height 1.1mm (MAX)	DS
– 315-ball LFBGA 12.4mm x 15.0mm (TYP), seated height 1.3mm (MAX)	DV
– 441-ball TFBGA 14.0mm x 14.0mm (TYP), seated height 1.1mm (MAX)	EK
– 561-ball TFBGA 8.0mm x 12.4mm (TYP), seated height 1.2mm (MAX)	CZ
– 563-ball WFBGA 7.0mm x 12.4mm (TYP), seated height 0.675mm (MAX)	AH
– 563-ball VFBGA 7.0mm x 12.4mm (TYP), seated height 0.915mm (MAX)	AJ
Speed grade, cycle time (^{t}WCK)	
– 8533 Mb/s	-023
– 7500 Mb/s	-026

Options	Marking
• Operating Temperature:	
– –25°C ≤ T_C ≤ +85°C	WT
– –40°C ≤ T_C ≤ +95°C	IT
• Revision	:C

Note: 1. V_{DDQ} = 0.45V (TYP) support on all packages up to 7500 Mb/s.

Part Number Ordering Information

Figure 1: Part Number Chart

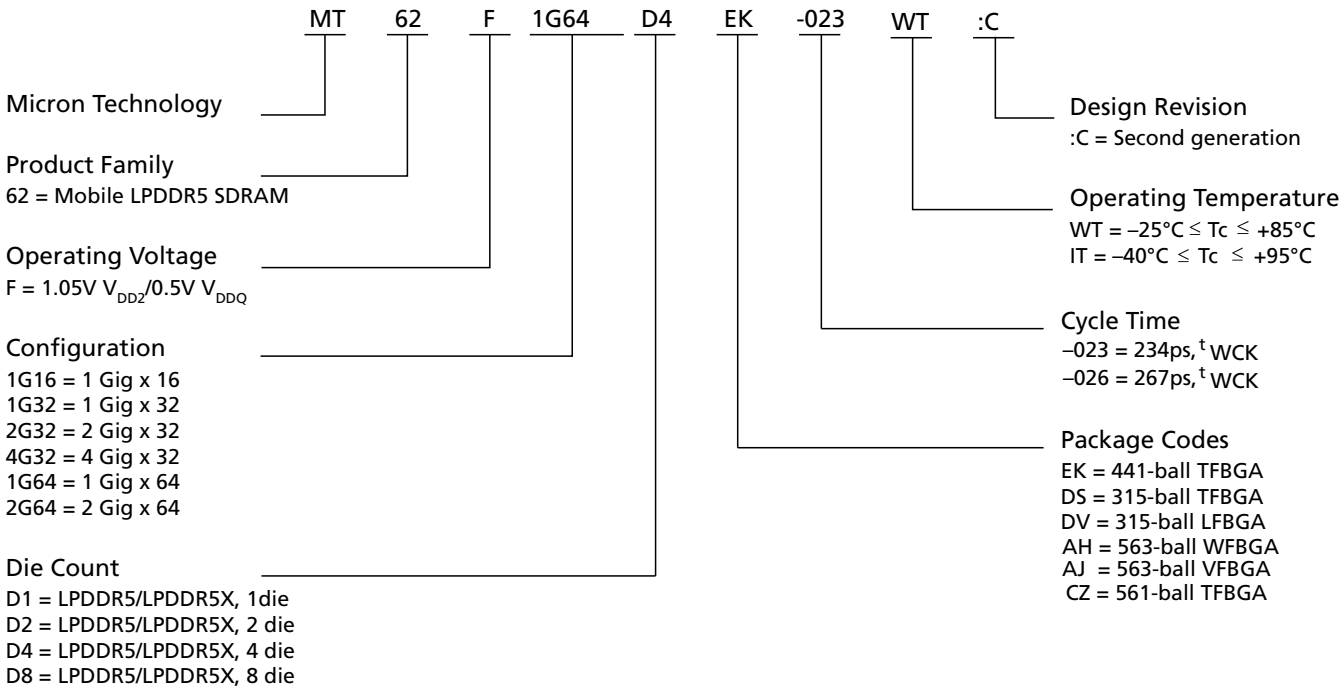

Table 1: Part Number List

Part Number	Total Density	Data Rate per Pin
MT62F1G16D1DS-023 IT:C	2GB (16Gb)	8533 Mb/s
MT62F1G32D2DS-023 IT:C	4GB (32Gb)	
MT62F1G32D2DS-023 WT:C		
MT62F2G32D4DS-023 IT:C	8GB (64Gb)	
MT62F2G32D4DS-023 WT:C		
MT62F4G32D8DV-023 WT:C	16GB (128Gb)	
MT62F1G64D4EK-023 IT:C	8GB (64Gb)	
MT62F1G64D4EK-023 WT:C		
MT62F2G64D8EK-023 WT:C	16GB (128Gb)	
MT62F1G64D4CZ-023 WT:C	8GB (64Gb)	
MT62F2G64D8CZ-023 WT:C	16GB (128Gb)	
MT62F1G64D4AH-023 WT:C	8GB (64Gb)	
MT62F2G64D8AJ-023 WT:C	16GB (128Gb)	
MT62F1G32D2DS-026 WT:C	4GB (32Gb)	7500 Mb/s
MT62F2G32D4DS-026 WT:C	8GB (64Gb)	
MT62F4G32D8DV-026 WT:C	16GB (128Gb)	
MT62F1G64D4EK-026 WT:C	8GB (64Gb)	
MT62F2G64D8EK-026 WT:C	16GB (128Gb)	
MT62F1G64D4CZ-026 WT:C	8GB (64Gb)	
MT62F2G64D8CZ-026 WT:C	16GB (128Gb)	

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

LPDDR5/LPDDR5X Data Sheet List

For general LPDDR5/LPDDR5X specifications, please refer to the data sheets below.

- General LPDDR5/LPDDR5X Specifications 1: Mode Registers
- General LPDDR5/LPDDR5X Specifications 2: AC/DC and Interface Specifications
- General LPDDR5/LPDDR5X Specifications 3: Features and Functionalities

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General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQs collectively, unless specifically stated otherwise.

RDQS, CK, and WCK should be interpreted as RDQS_t, RDQS_c, CK_t, CK_c, and WCK_t, WCK_c respectively unless specifically stated otherwise. CA includes all CA pins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[6:0].

V_{REF} indicates $V_{REF(CA)}$ and $V_{REF(DQ)}$.

Complete functionality is described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any content defined in this device ID specific data sheet document takes precedence over similar content defined in the general core LPDDR5/LPDDR5X SDRAM data sheet document(s).

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

Device Configuration

Table 2: Die Organization in the Package (x16)

Die Organization	1G16 (16 Gb/package)
Channel A	x16 mode × 1 die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 3: Die Organization in the Package (x32)

Die Organization	1G32 (32 Gb/package)	2G32 (64 Gb/package)	4G32 (128 Gb/package)
Channel A	x16 mode × 1 die	–	–
Channel B	x16 mode × 1 die	–	–
Channel A, rank 0	–	x16 mode × 1 die	–
Channel B, rank 0	–	x16 mode × 1 die	–
Channel A, rank 1	–	x16 mode × 1 die	–
Channel B, rank 1	–	x16 mode × 1 die	–
Channel A, rank 0 DQ[7:0]	–	–	x8 mode × 1 die
Channel A, rank 1 DQ[7:0]	–	–	x8 mode × 1 die
Channel B, rank 0 DQ[7:0]	–	–	x8 mode × 1 die
Channel B, rank 1 DQ[7:0]	–	–	x8 mode × 1 die
Channel A, rank 0 DQ[15:8]	–	–	x8 mode × 1 die
Channel A, rank 1 DQ[15:8]	–	–	x8 mode × 1 die
Channel B, rank 0 DQ[15:8]	–	–	x8 mode × 1 die
Channel B, rank 1 DQ[15:8]	–	–	x8 mode × 1 die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 4: Die Organization in the Package (x64)

Die Organization	1G64 (64 Gb/package)	2G64 (128 Gb/package)
Channel A, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel B, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel C, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel D, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel A, rank 1	–	x16 mode × 1 die
Channel B, rank 1	–	x16 mode × 1 die
Channel C, rank 1	–	x16 mode × 1 die
Channel D, rank 1	–	x16 mode × 1 die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 5: Die Addressing

Description	1G16 (16 Gb/package), 1G32 (32 Gb/package), 2G32 (64 Gb/package), 1G64 (64 Gb/package), 2G64 (128 Gb/package)		4G32 (128 Gb/package)	
Density per die	16Gb		16Gb	
Bits	17,179,869,184		17,179,869,184	
Bank mode	BG mode	16B mode	BG mode	16B mode
Configuration	64Mb × 16 DQ × 4 Banks × 4BG	64Mb × 16 DQ × 16 Banks	128Mb × 8 DQ × 4 Banks × 4BG	128Mb × 8 DQ × 16 Banks
Number of banks	4	16	4	16
Number of bank groups	4	1	4	1
Array prefetch bits	256	256	128	128
Rows per bank	65,536		131,072	
Columns	64		64	
Page size (bytes)	2048	2048	1024	1024
Native burst length	16	16	16	16
Number of I/Os	16		8	
Bank address	BA[1:0]	BA[3:0]	BA[1:0]	BA[3:0]
Bank group address	BG[1:0]	–	BG[1:0]	–
Row address	R[15:0]		R[16:0]	
Column address	C[5:0]		C[5:0]	
Burst address	B[3:0]	B[3:0]	B[3:0]	B[3:0]
Burst starting address boundary	128-bit		128-bit	

Note: 1. Refer to the SDRAM Addressing section in General LPDDR5/LPDDR5X Specifications 3.

Refresh Requirement Parameters

Table 6: Refresh Requirement Parameters

Parameter	Symbol	16Gb Die	Unit
		BG and 16B Mode	
REFRESH cycle time (all banks)	^{t}RFCab	280	ns
REFRESH cycle time (per bank)	^{t}RFCpb	140	ns
Per bank refresh to per bank refresh time (different bank)	^{t}PBR2PBR	90	ns
Per bank refresh to ACTIVATE command time (different bank)	^{t}PBR2ACT	7.5	ns

Note: 1. This table only describes refresh parameters that are density dependent. Refer to Refresh Requirement section in General LPDDR5/LPDDR5X Specifications 3 for all refresh parameters.

CS Rx Relaxed Specification

Table 7: CS Rx Specifications

Item	Symbol	Min/ Max	CK Frequency (MHz)													Unit	Note
			67[6]	133	200	266	344	400	467	533	600	688	750	800	937.5	1066.5		
Rx mask																		
CS Rx mask height	vCSIVW	Min	155														mV	2, 7
CS Rx mask width at V_{REF} CS	^{t}CSIVW1	Min	0.3														UI	1
CS Rx mask width at vCSIVW	^{t}CSIVW2	Min	0.22														UI	1
Rx single pulse																		
CS Rx pulse amplitude	vCSIHL_AC	Min	240														mV	3
CS reference voltage	vREFCS		V_{DD2H}/3														mV	
CS Rx pulse width	^{t}CSIPW	Min	0.6														UI	
Power down																		
CS V_{IL} during power down/deep sleep	V_{ILPD}	Max	130														mV	4
CS V_{IH} during power down/deep sleep	V_{IHPD}	Min	550														mV	5
		Max	V_{DD2H} + 200															

Notes: 1. CS Rx mask voltage and timing parameters at the pin include temperature drift and voltage AC noise impact based on Z(f) specification at a fixed temperature on the package. The voltage supply noise must comply to the component min/max DC operating conditions.
2. CS single-pulse signal amplitude into the receiver must meet or exceed vCSIHL_AC at any point over the total UI; No timing requirement above a certain level. vCSIIHL_AC is the peak-to-peak voltage centered around V_{REF} CS such that vCSIHL_AC/2 min has to be met both above and below V_{REF} CS.
3. vCSIHL_AC does not have to be met when no transitions are occurring.
4. The input voltage presented to the CS Rx pin during power down should be 0V nominally to minimize leakage current.
5. V_{IHPD} is only applied for POWER DOWN and DEEP SLEEP EXIT operations.
6. The Rx voltage and absolute timing requirements apply for all CS operating frequencies at or below 67 for all speed bins. For example, ^{t}CSIVW1 (ns) = 4.477ns at or below 67 MHz CK frequency.
7. Measured at die pad.

DQ Rx Mask and Single Input Pulse Relaxed Specifications

Table 8: DQ Rx Mask and Single Input Pulse Specifications

Item	Symbol	Min/ Max	WCK Frequency (MHz)		Unit	Notes
			3750	4266		
DQ Rx mask height	vDIVW	Min	70		mV	1, 2, 3
DQ Rx mask width at $V_{REF(DQ)}$	^{t}DIVW1	Min	0.35		UI	1, 3
DQ Rx mask width at vDIVW	^{t}DIVW2	Min	0.18		UI	1, 3
DQ Rx pulse width at $V_{REF(DQ)}$	^{t}DIPW1	Min	0.51		UI	4
DQ Rx pulse reference	^{t}DIPW2	Min	0.26		UI	4
DQ Rx pulse width at $V_{REF(DQ)}$ ± vDIVW/2	^{t}DIHL	Min	0.24		UI	4
DQ Rx pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP1	Min	70		mV	
	vDILP1	Max	–70		mV	

Table 8: DQ Rx Mask and Single Input Pulse Specifications (Continued)

Item	Symbol	Min/ Max	WCK Frequency (MHz)		Unit	Notes
			3750	4266		
DQ Rx early pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP2	Min	55		mV	
	vDILP2	Max	–55		mV	

Notes: 1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies greater than TBD MHz and maximum voltage of TBD mV peak-to-peak from DC-TBD MHz at a fixed temperature on the package. The voltage supply noise must comply with the component min/max DC operating conditions.
2. Rx mask voltage vDIVW must be centered around $V_{REF(DQ)}$.
3. Mask specifications (^{t}DIVW1, ^{t}DIVW2, and vDIVW) are the same regardless DFE enabled or disabled. DFE co-efficient can be included as part of input waveform amplitude when DFE is enabled.
4. UI = ^{t}WCK/2, programed V_{REF}, is defined as a percentage of MR14/15 code x V_{DDQ}.

Figure 2: DQ Rx Mask Definition

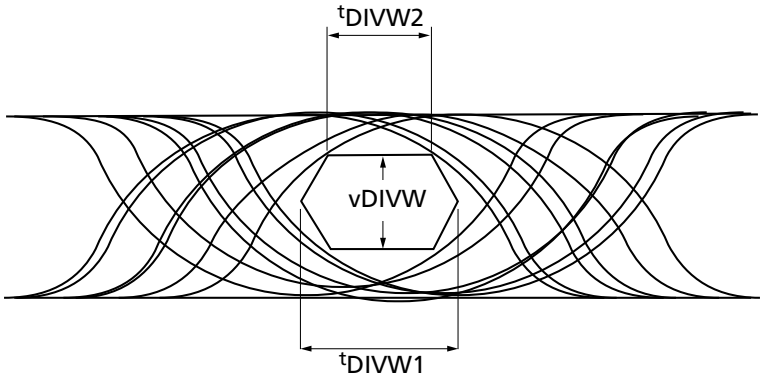
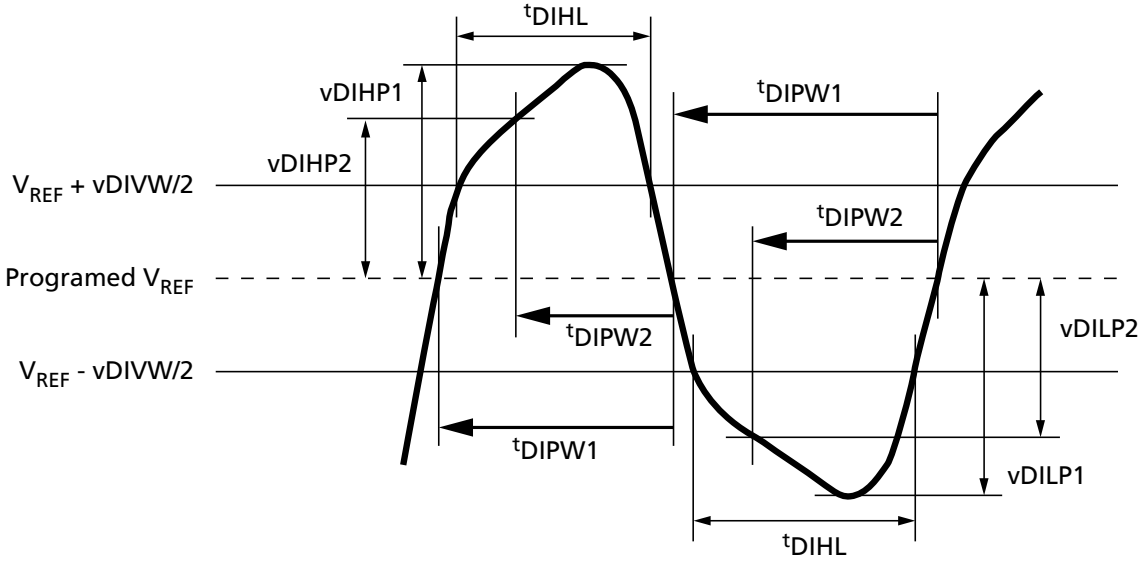


Figure 3: LPDDR5X DQ Single Pulse Definition



Note: 1. vDIHL_AC/2 = vDIHP1 = vDILP1. Programmed $V_{REF(DQ)}$ is defined as percentage of MR14/15 code * V_{DDQ}.

DQ Rx Mask and Single Input Pulse Relaxed Specifications 3200 MHz

Table 9: DQ, DMI, Parity and DBI Rx Mask and Single Input Pulse Specifications

Item	Symbol	Min/Max	WCK Frequency (MHz)	Unit	Notes
			3200		
DQ Rx mask height	vDIVW	Min	70	mV	1, 2, 3, 6
DQ Rx mask width at $V_{REF(DQ)}$	^{t}DIVW1	Min	0.35	UI	1, 3
DQ Rx mask width at vDIVW	^{t}DIVW2	Min	0.18	UI	1, 3
DQ Rx pulse width at $V_{REF(DQ)}$	^{t}DIPW1	Min	0.51	UI	4, 6
DQ Rx pulse reference	^{t}DIPW2	Min	0.26	UI	4
DQ Rx pulse width at $V_{REF(DQ)}$ ± vDIVW/2	^{t}DIHL	Min	0.24	UI	4, 6
DQ Rx pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP1	Min	70	mV	
	vDILP1	Max	–70	mV	
DQ Rx early pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP2	Min	55	mV	
	vDILP2	Max	–55	mV	
DQ V_{REF}	VREF(DQ)	Min	75	mV	6
		Max	180	mV	6
DQ to DQ offset	^{t}DQ2DQ	Max	30	ps	5

Notes: 1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies greater than TBD MHz and maximum voltage of TBD mV peak-to-peak from DC-TBD MHz at a fixed temperature on the package. The voltage supply noise must comply with the component min/max DC operating conditions.
2. Rx mask voltage vDIVW must be centered around $V_{REF(DQ)}$.
3. Mask specifications (^{t}DIVW1, ^{t}DIVW2, and vDIVW) are the same regardless DFE enabled or disabled. DFE co-efficient can be included as part of input waveform amplitude when DFE is enabled.
4. UI = ^{t}WCK/2, programed V_{REF}, is defined as a percentage of MR14/15 code x V_{DDQ}.
5. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
6. When vDIVW is 70mV or more and less than 80mV.

16-Bank Extended Frequency

16-Bank Extended Frequency Description

Micron's LPDDR5 SDRAM device which are marked with 8533 Mb/s per-pin (-023) capability can support frequency set points using 2:1 WCK to CK ratio and above the 1600 MHz limit. Shown in the table below is specification requirements when considering 1867 MHz and 2133 MHz frequencies. This support is not available on 1-alpha process node and earlier Device ID's, this feature can expand capabilities of your system.

Table 10: 16-Bank Operation[1] @ 4.3 Gb/s

Parameter	3733 Mb/s per-pin	Comments	4267 Mb/s per-pin	Comments
RL Set 1/2/3	20/22/24	MR2[3:0] = 1100	23/25/26	MR2[3:0] = 1101
*n*RBTP	6		6	
WL Set A/B	11/19	MR1[7:4] = 1100	12/22	MR1[7:4] = 1101
*n*WR x16/x8	32/34	MR2[7:4] = 1100	37/39	MR2[7:4] = 1101
^{t}WCKPRE_static[2]	5	Follows 7500 data rate	6	Follows 8533 data rate

Table 10: 16-Bank Operation[1] @ 4.3 Gb/s (Continued)

Parameter	3733 Mb/s per-pin	Comments	4267 Mb/s per-pin	Comments
^{t}WCKPRE_WR_toggle	4	Follows 3200 datarate	4	Follows 3200 data rate
^{t}WCKPRE_RD_toggle	10	Follows 3200 datarate	10	Follows 3200 data rate
^{t}WCKENL_FS	2	Follows 3200 data rate	2	Follows 3200 data rate
^{t}WCKPRE_toggle_FS[3]	14	Minimum	16	Minimum
ODTLon	WL - 4	Follows 3200 data rate	WL - 4	Follows 3200 data rate
ODTLoff[4]	WL + 5 (BL16), WL + 9 (BL32)	Follows 3200	WL + 5 (BL16), WL + 9 (BL32)	Follows 3200 data rate
ODTLoff_RD_DQ	RL - 4	Follows 3200 data rate	RL - 4	Follows 3200 data rate
ODTLoff_RD_RDQS	RL - 6	MR10 OP[1, 5:4] = 000, 001, 010	RL - 6	MR10 OP[1, 5:4] = 000, 001, 010
	RL - 8	MR10 OP[1, 5:4] = 011, 1XX	RL - 8	MR10 OP[1, 5:4] = 011, 1XX
ODTLon_RD_DQ[5]	RL + 6 (BL16), RL + 10 (BL32)		RL + 6 (BL16), RL + 10 (BL32)	
ODTLon_RD_RDQS[6]	RL + 8 (BL16), RL + 12 (BL32)		RL + 8 (BL16), RL + 12 (BL32)	

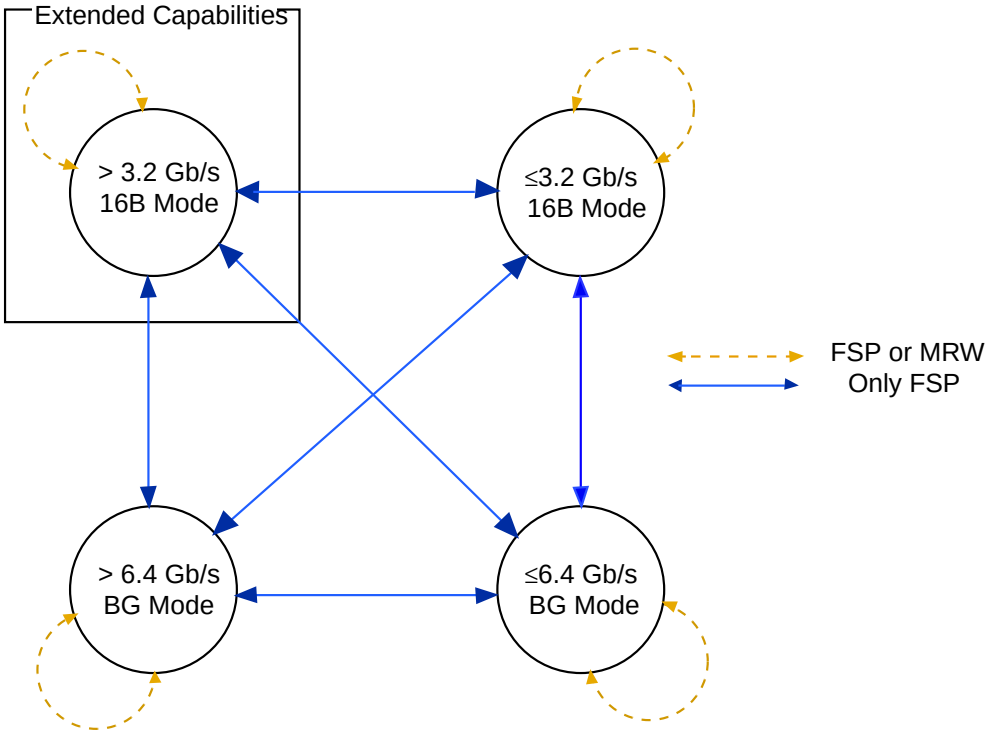
Notes: 1. Restricted to WCK:CK 2:1 ratio, WCK:CK 4:1 ratio not supported; Link ECC is disabled, and DVFSC/E-DVFSC is disabled.
2. Common for WR/RD/FS.
3. Minimum 1 + RL - (^{t}WCKENL_FS + ^{t}WCKPRE_Static) when CAS to RD is 1CK.
4. (WL + BL/n_min + RU(^{t}WCK2DQI(max)/^{t}CK)).
5. (RL + BL/n_min + RU(^{t}WCK2DQO(max)/^{t}CK)).
6. (RL + BL/n_min + RU(^{t}WCK2DQO(max)/^{t}CK)) + 2.
7. 8533 MT/s or higher data rated parts support 16-bank mode up to 4267 MT/s with restrictions, all other speed rated parts greater than 3200 MT/s per-pin and less than 8533 MT/s per-pin are restricted from the extended 16B mode capabilities. Refer to the above table for constraints for operating in 16-bank mode when data rate is greater than 3200 MT/s per-pin and equal to or less than 4267 MT/s per-pin.
8. When operating in the 16-bank mode, the FSP procedure must be used when setting the data rate above 3.2 Gb/s per-pin even when setting for the first time. For example, if the device is powered-up and initialized for 4266 Gb/s per-pin timing at the initial operation start, the FSP procedure must still be used. See Figure 4: 16B and BG Data Rate Change Flow Chart Showing Extended Capabilities on page 16 for details of FSP usage.

16B/BG Data Rate Change Diagram With FSP Requirements

The following flow chart diagram shows the needed 16-bank (16B) and bank group (BG) data rate change details and how the frequency set protocol (FSP) supports the extended frequency range.

The diagram below represents the device extended capabilities which are extended to 4267 Mb/s per-pin data rate in 16B mode.

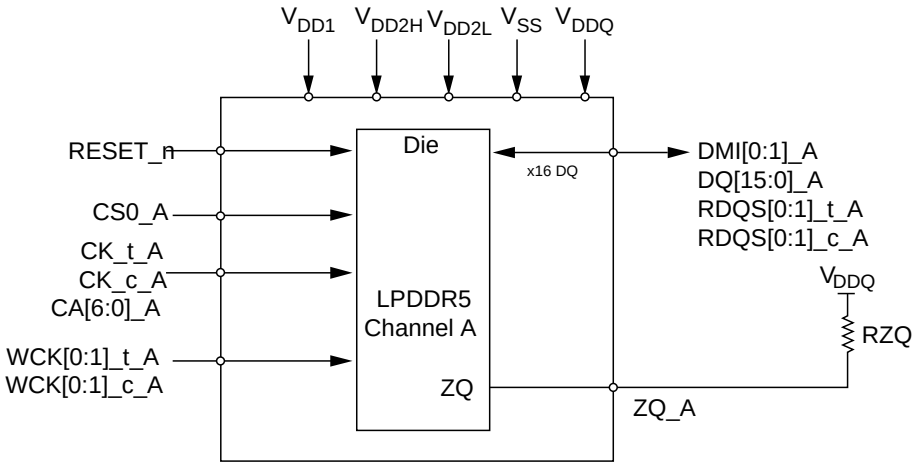
Figure 4: 16B and BG Data Rate Change Flow Chart Showing Extended Capabilities



Package Block Diagrams

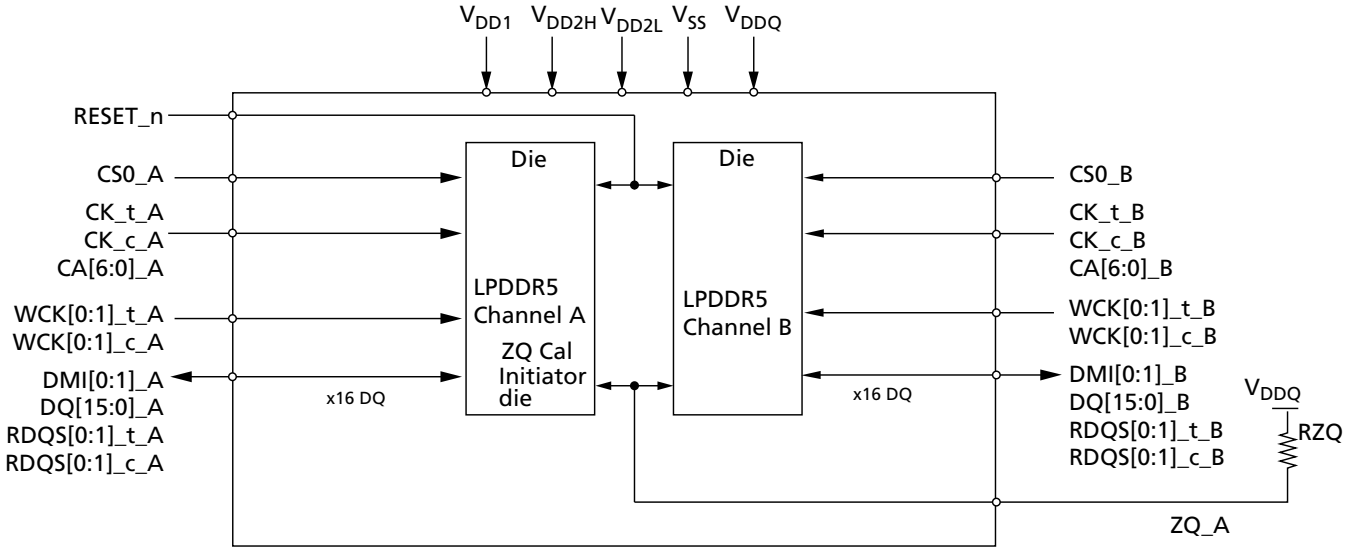
Single Die, Single Channel, Single Rank

Figure 5: Single-Die, Single-Channel, Single-Rank Package Block Diagram



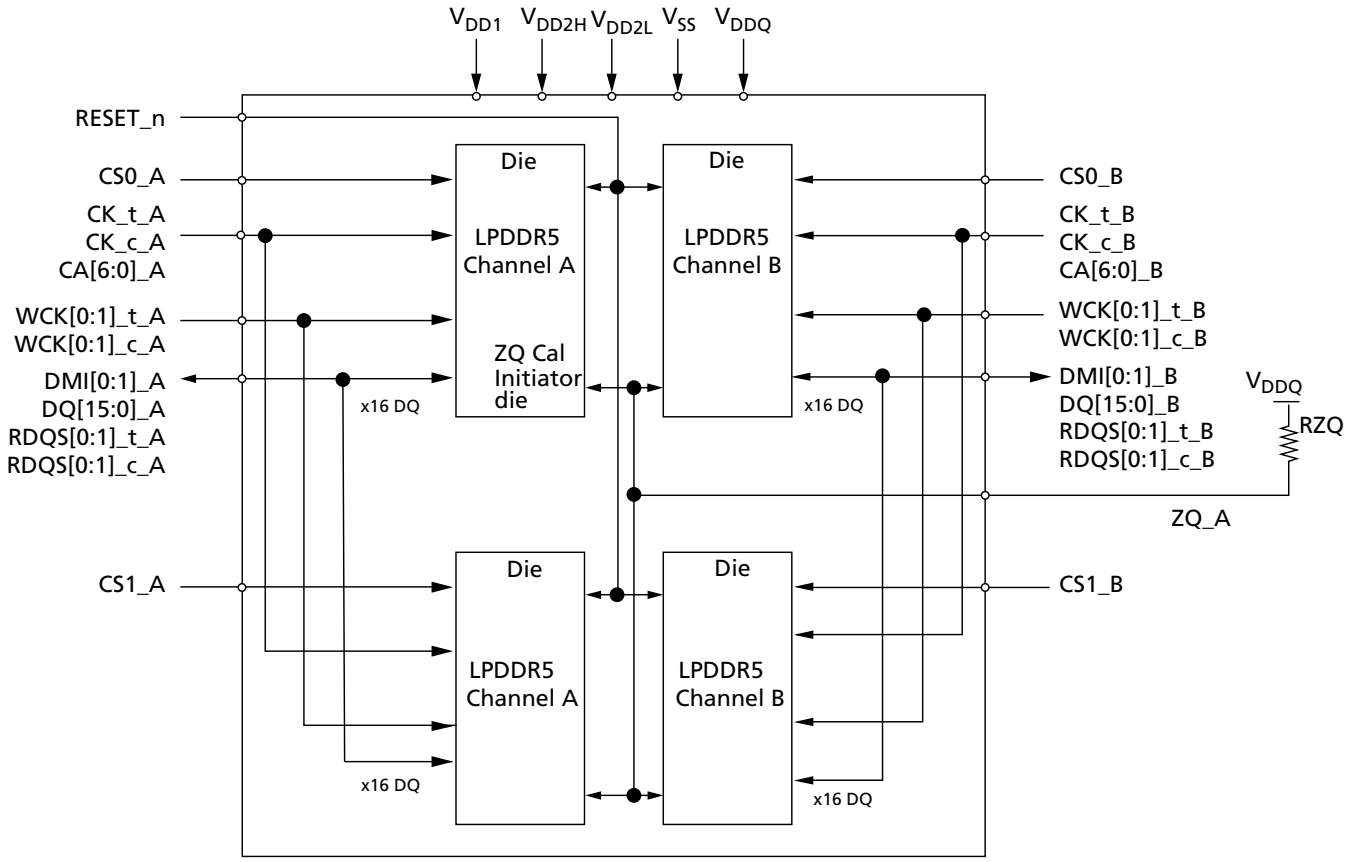
Dual Die, Dual Channel, Single Rank

Figure 6: Dual-Die, Dual-Channel, Single-Rank Package Block Diagram



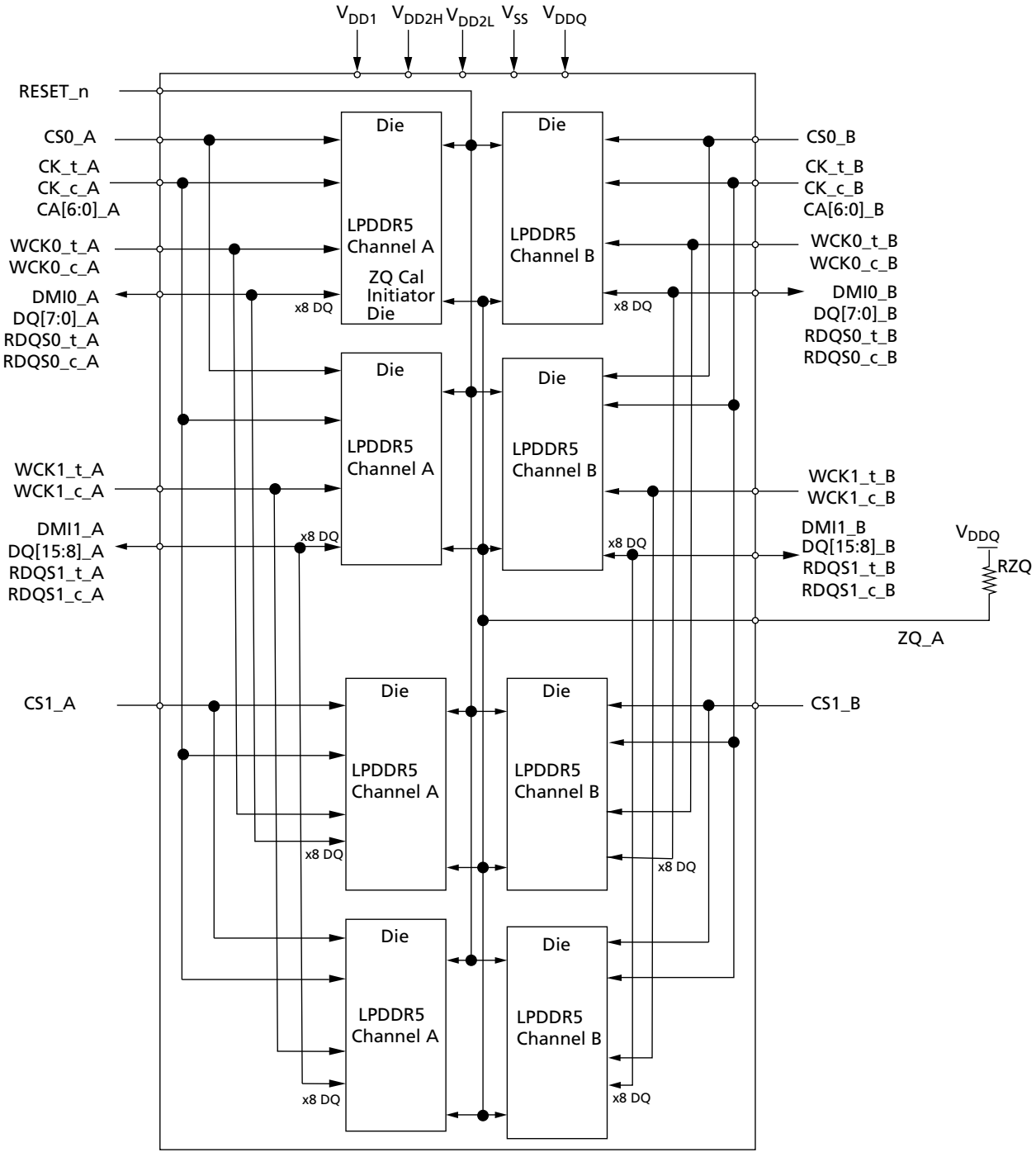
Quad Die, Dual Channel, Dual Rank

Figure 7: Quad-Die, Dual-Channel, Dual-Rank Package Block Diagram



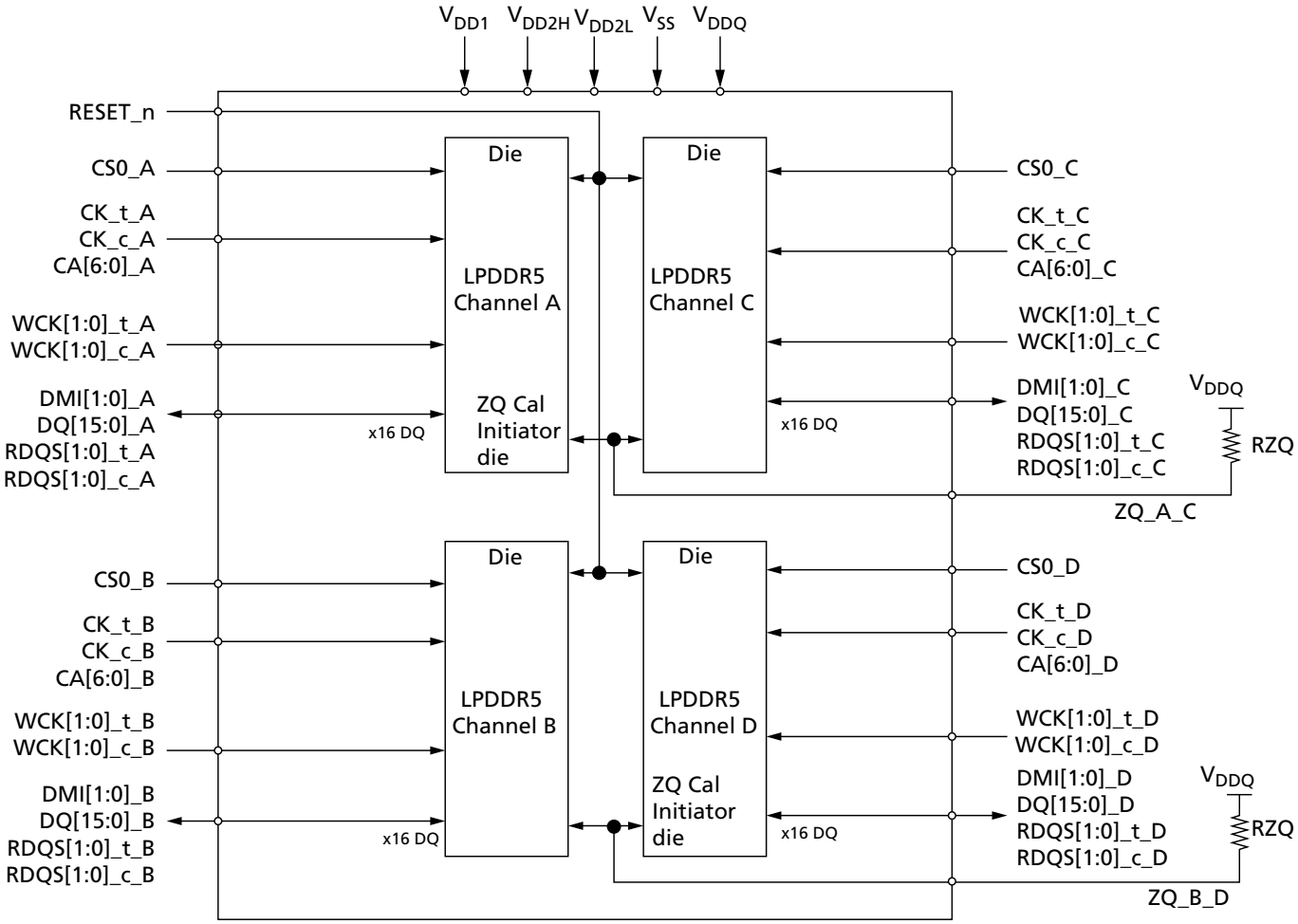
Eight Die, Dual Channel, Dual Rank

Figure 8: Eight-Die, Dual-Channel, Dual-Rank Package Block Diagram



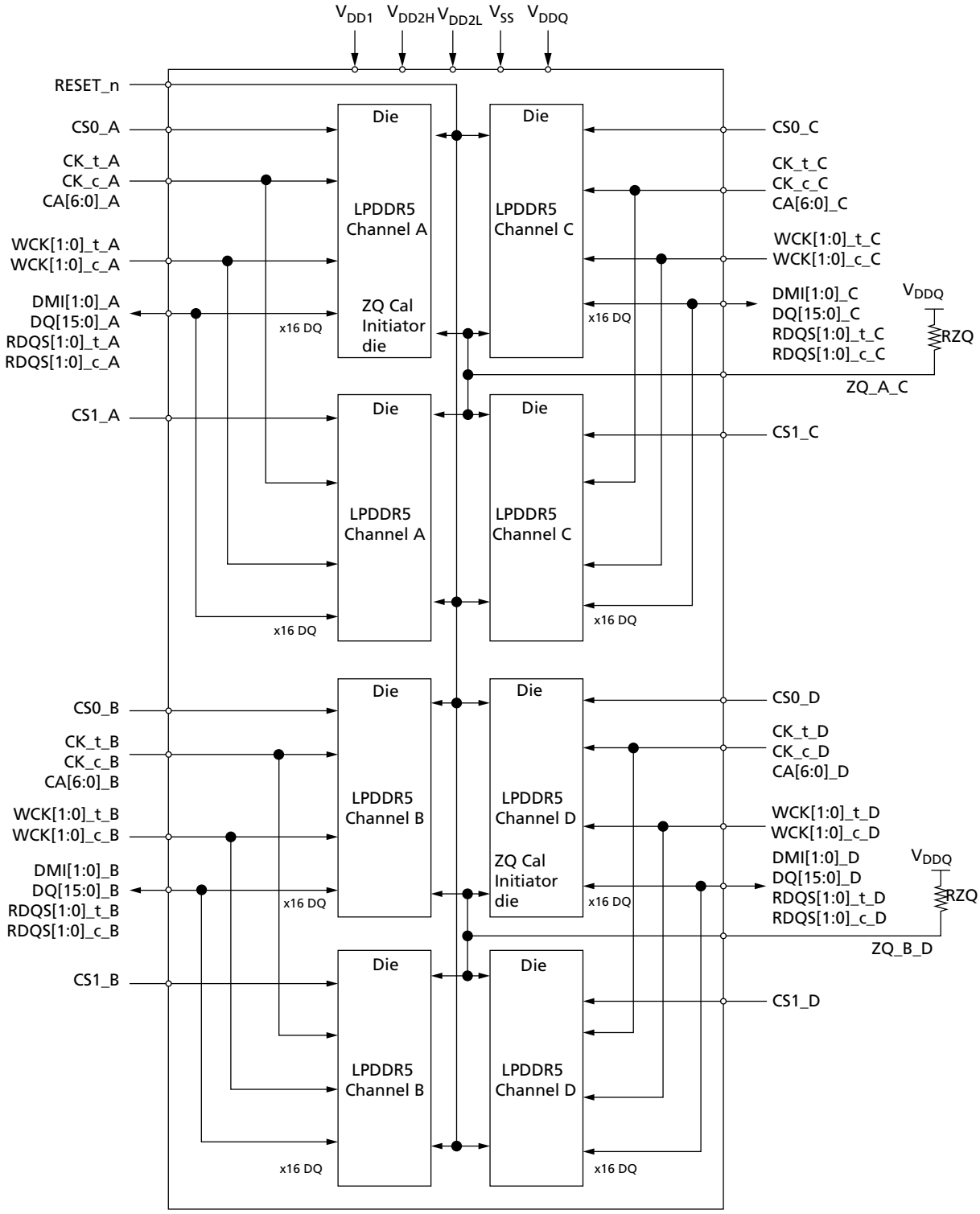
Quad-Die, Quad-Channel, Single-Rank

Figure 9: Quad-Die, Quad-Channel, Single-Rank Package Block Diagram



Eight-Die, Quad-Channel, Dual-Rank

Figure 10: Eight-Die, Quad-Channel, Dual-Rank Package Block Diagram



Ball Assignments and Descriptions

315b Single Die, Single Channel, 1 Rank, 2 Rank

Table 11: Single Channel 315-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A], CK_c_[A]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A], CS1_[A]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] become NC pins in a single-rank package.
CA[6:0]_[A]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A], WCK[1:0]_c_[A]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_[A]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A], RDQS[1:0]_c_[A]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240 ohm ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.
RFU	–	**Reserved Future Use:** Not internally connected

Figure 11: 315-Ball Single-Channel Discrete FBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	NC	NC	V_{DDQ}	DMI0_A	V_{SS}	V_{DD2L}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2L}	V_{SS}	DMI1_A	V_{DDQ}	NC	NC	A
B	NC	V_{DDQ}	RDQS0_t_A	V_{SS}	DQ4_A	V_{DD2L}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2L}	DQ12_A	V_{SS}	RDQS1_t_A	V_{DDQ}	NC	B
C	V_{DD1}	DQ1_A	V_{DDQ}	RDQS0_c_A	V_{SS}	DQ5_A	V_{DD2H}	V_{SS}	V_{DD2H}	DQ13_A	V_{SS}	RDQS1_c_A	V_{DDQ}	DQ9_A	V_{DD1}	C
D	DQ0_A	V_{SS}	DQ3_A	V_{DDQ}	WCK0_c_A	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	WCK1_c_A	V_{DDQ}	DQ11_A	V_{SS}	DQ8_A	D
E	V_{SS}	DQ2_A	V_{SS}	WCK0_t_A	V_{DDQ}	DQ6_A	V_{DD2H}	V_{SS}	V_{DD2H}	DQ14_A	V_{DDQ}	WCK1_t_A	V_{SS}	DQ10_A	V_{SS}	E
F	V_{DDQ}	V_{SS}	V_{DDQ}	V_{DDQ}	DQ7_A	V_{DD2H}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2H}	DQ15_A	V_{DDQ}	V_{DDQ}	V_{SS}	V_{DDQ}	F
G	V_{DDQ}	V_{DDQ}	V_{SS}	CA0_A	V_{SS}	CS1 _A	V_{SS}	CA2_A	V_{SS}	CA4_A	V_{SS}	CA6_A	V_{SS}	V_{DDQ}	V_{DDQ}	G
H	RESET_N	V_{DD2L}	V_{SS}	V_{SS}	CA1_A	V_{SS}	CS0 _A	V_{SS}	CK_t_A	V_{SS}	CA3_A	V_{SS}	CA5_A	V_{DD2L}	ZQ_A	H
J	V_{SS}	V_{DD2L}	V_{SS}	RFU	V_{DD2H}	RFU	V_{SS}	V_{SS}	CK_c_A	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	V_{DD2L}	V_{SS}	J
K	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	K
L	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	L
M	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	M
N	V_{SS}	V_{DD2L}	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	V_{DD2L}	V_{SS}	N
P	RFU	V_{DD2L}	NC	V_{SS}	NC	V_{SS}	NC	V_{SS}	NC	V_{SS}	NC	V_{SS}	V_{SS}	V_{DD2L}	RFU	P
R	V_{DDQ}	V_{DDQ}	V_{SS}	NC	V_{SS}	NC	V_{SS}	NC	V_{SS}	NC	V_{SS}	NC	V_{SS}	V_{DDQ}	V_{DDQ}	R
T	V_{DDQ}	V_{SS}	V_{DDQ}	V_{DDQ}	NC	V_{DD2H}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2H}	NC	V_{DDQ}	V_{DDQ}	V_{SS}	V_{DDQ}	T
U	V_{SS}	NC	V_{SS}	NC	V_{DDQ}	NC	V_{DD2H}	V_{SS}	V_{DD2H}	NC	V_{DDQ}	NC	V_{SS}	NC	V_{SS}	U
V	NC	V_{SS}	NC	V_{DDQ}	NC	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	NC	V_{DDQ}	NC	V_{SS}	NC	V
W	V_{DD1}	NC	V_{DDQ}	NC	V_{SS}	NC	V_{DD2H}	V_{SS}	V_{DD2H}	NC	V_{SS}	NC	V_{DDQ}	NC	V_{DD1}	W
Y	NC	V_{DDQ}	NC	V_{SS}	NC	V_{DD2L}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2L}	NC	V_{SS}	NC	V_{DDQ}	NC	Y
AA	NC	NC	V_{DDQ}	NC	V_{SS}	V_{DD2L}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2L}	V_{SS}	NC	V_{DDQ}	NC	NC	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Top View (ball down)

VSS | V_{DD1} | V_{DD2H} | V_{DD2L} | V_{DDQ} | CK | RDQS | WCK | DQ,DMI | CA, CS, ZQ, RESET | NC, RFU

315b Dual Channel, 1 Rank, 2 Rank

Table 12: 315-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:B], CK_c_[A:B]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:B], CS1_[A:B]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] become NC pins in a single-rank package.
CA[6:0]_[A:B]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:B], WCK[1:0]_c_[A:B]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_[A:B]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A:B], RDQS[1:0]_c_[A:B]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:B]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240 ohm ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.
RFU	–	**Reserved Future Use:** Not internally connected.

Figure 12: 315-Ball Dual-Channel Discrete FBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	NC	NC	V_{DDQ}	DMI0_A	V_{SS}	V_{DD2L}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2L}	V_{SS}	DMI1_A	V_{DDQ}	NC	NC	A
B	NC	V_{DDQ}	RDQS0t_A	V_{SS}	DQ4_A	V_{DD2L}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2L}	DQ12_A	V_{SS}	RDQS1t_A	V_{DDQ}	NC	B
C	V_{DD1}	DQ1_A	V_{DDQ}	RDQS0c_A	V_{SS}	DQ5_A	V_{DD2H}	V_{SS}	V_{DD2H}	DQ13_A	V_{SS}	RDQS1c_A	V_{DDQ}	DQ9_A	V_{DD1}	C
D	DQ0_A	V_{SS}	DQ3_A	V_{DDQ}	WCK0_c_A	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	WCK1_c_A	V_{DDQ}	DQ11_A	V_{SS}	DQ8_A	D
E	V_{SS}	DQ2_A	V_{SS}	WCK0_t_A	V_{DDQ}	DQ6_A	V_{DD2H}	V_{SS}	V_{DD2H}	DQ14_A	V_{DDQ}	WCK1_t_A	V_{SS}	DQ10_A	V_{SS}	E
F	V_{DDQ}	V_{SS}	V_{DDQ}	V_{DDQ}	DQ7_A	V_{DD2H}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2H}	DQ15_A	V_{DDQ}	V_{DDQ}	V_{SS}	V_{DDQ}	F
G	V_{DDQ}	V_{DDQ}	V_{SS}	CA0_A	V_{SS}	CS1_A	V_{SS}	CA2_A	V_{SS}	CA4_A	V_{SS}	CA6_A	V_{SS}	V_{DDQ}	V_{DDQ}	G
H	RESET_N	V_{DD2L}	V_{SS}	V_{SS}	CA1_A	V_{SS}	CS0_A	V_{SS}	CK_t_A	V_{SS}	CA3_A	V_{SS}	CA5_A	V_{DD2L}	ZQ_A	H
J	V_{SS}	V_{DD2L}	V_{SS}	RFU	V_{DD2H}	RFU	V_{SS}	V_{SS}	CK_c_A	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	V_{DD2L}	V_{SS}	J
K	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	K
L	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	L
M	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	M
N	V_{SS}	V_{DD2L}	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	CK_c_B	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	V_{DD2L}	V_{SS}	N
P	RFU	V_{DD2L}	CA5_B	V_{SS}	CA3_B	V_{SS}	CK_t_B	V_{SS}	CS0_B	V_{SS}	CA1 _B	V_{SS}	V_{SS}	V_{DD2L}	RFU	P
R	V_{DDQ}	V_{DDQ}	V_{SS}	CA6_B	V_{SS}	CA4_B	V_{SS}	CA2 _B	V_{SS}	CS1_B	V_{SS}	CA0 _B	V_{SS}	V_{DDQ}	V_{DDQ}	R
T	V_{DDQ}	V_{SS}	V_{DDQ}	V_{DDQ}	DQ15_B	V_{DD2H}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2H}	DQ7_B	V_{DDQ}	V_{DDQ}	V_{SS}	V_{DDQ}	T
U	V_{SS}	DQ10_B	V_{SS}	WCK1_t_B	V_{DDQ}	DQ14_B	V_{DD2H}	V_{SS}	V_{DD2H}	DQ6_B	V_{DDQ}	WCK0_t_B	V_{SS}	DQ2_B	V_{SS}	U
V	DQ8_B	V_{SS}	DQ11_B	V_{DDQ}	WCK1_c_B	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	WCK0_c_B	V_{DDQ}	DQ3_B	V_{SS}	DQ0_B	V
W	V_{DD1}	DQ9_B	V_{DDQ}	RDQS1c_B	V_{SS}	DQ13_B	V_{DD2H}	V_{SS}	V_{DD2H}	DQ5_B	V_{SS}	RDQS0c_B	V_{DDQ}	DQ1_B	V_{DD1}	W
Y	NC	V_{DDQ}	RDQS1t_B	V_{SS}	DQ12_B	V_{DD2L}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2L}	DQ4_B	V_{SS}	RDQS0t_B	V_{DDQ}	NC	Y
AA	NC	NC	V_{DDQ}	DMI1_B	V_{SS}	V_{DD2L}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2L}	V_{SS}	DMI0_B	V_{DDQ}	NC	NC	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Top View (ball down)

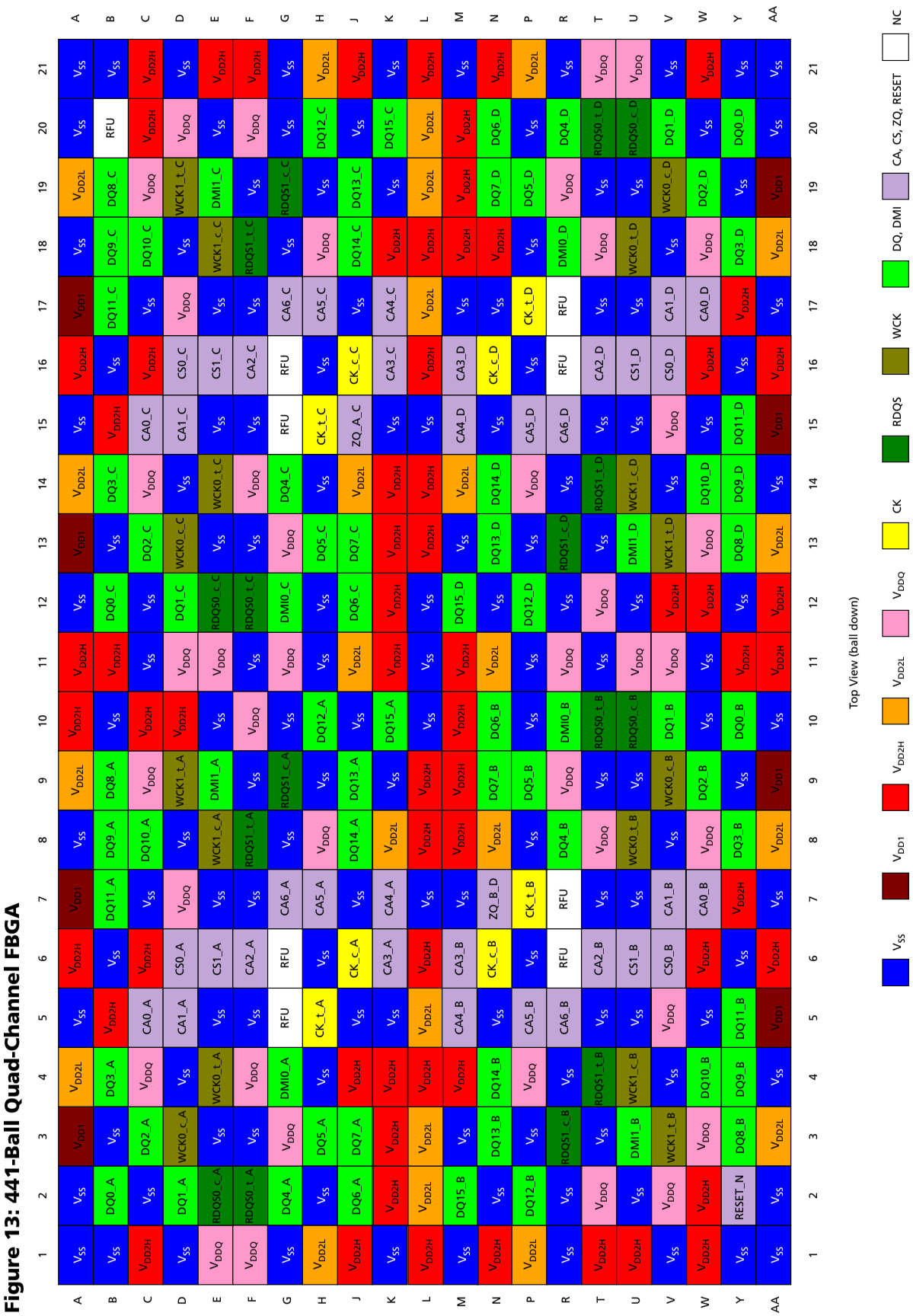
VSS | V_{DD1} | V_{DD2H} | V_{DD2L} | V_{DDQ} | CK | RDQS | WCK | DQ,DMI | CA, CS, ZQ, RESET | NC, RFU

441-Ball Quad-Channel, 1-Rank, 2-Rank

Table 13: 441-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:D], CK_c_[A:D]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:D], CS1_[A:D]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:D] become NC pins in a single-rank package.
CA[6:0]_[A:D]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:D], WCK[1:0]_c_[A:D]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for WRITE data capture and READ data output.
DQ[15:0]_[A:D]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A:D], RDQS[1:0]_c_[A:D]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:D]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A_C, ZQ_B_D	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240 ohm ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.
RFU	–	**Reserved Future Use:** Not internally connected

Figure 13: 441-Ball Quad-Channel FBGA



563b Quad Channel, 1 Rank, 2 Rank

Table 14: 563-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:D] CK_c_[A:D]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:D], CS1_[A:D]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:D] become NC pins in a single-rank package.
CA[6:0]_[A:D]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:D] WCK[1:0]_c_[A:D]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for WRITE data capture and READ data output.
DQ[15:0]_[A:D]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A:D] RDQS[1:0]_c_[A:D]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:D]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A_C, ZQ_B_D	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240 ohm ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.

Figure 14: 563-Ball Quad-Channel FBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
A		NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	A
B	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	B
C	V_{SS}	V_{SS}	DQ0_A	V_{DDQ}	V_{SS}	DMI0_A	DQ5_A	V_{SS}	CS0_A	CS1_A	CA3_A	V_{SS}	DQ13_A	DMI1_A	V_{SS}	V_{DDQ}	DQ8_A	V_{SS}	V_{SS}	C
D	V_{SS}	V_{DD1}	V_{SS}	DQ3_A	WCK0_C_A	V_{DDQ}	V_{SS}	CA0_A	V_{SS}	V_{SS}	V_{SS}	CA6_A	V_{SS}	V_{DDQ}	WCK1_C_A	DQ11_A	V_{SS}	V_{DD1}	V_{SS}	D
E	V_{SS}	V_{DD2H}	DQ1_A	V_{SS}	WCK0_T_A	V_{SS}	DQ6_A	V_{DDQ}	CA1_A	CK_T_A	CA4_A	V_{DDQ}	DQ14_A	V_{SS}	WCK1_T_A	V_{SS}	DQ9_A	V_{DD2H}	V_{SS}	E
F	V_{SS}	V_{SS}	V_{DDQ}	RDQS0_T_A	V_{DD2H}	DQ4_A	V_{DDQ}	V_{SS}	V_{SS}	CK_C_A	V_{SS}	V_{SS}	V_{DDQ}	DQ12_A	V_{DD2H}	RDQS1_T_A	V_{DDQ}	V_{SS}	V_{SS}	F
G	V_{SS}	V_{DD2L}	DQ2_A	RDQS0_C_A	V_{SS}	V_{DD2H}	DQ7_A	V_{DD2H}	CA2_A	V_{DD2L}	CA5_A	V_{DD2H}	DQ15_A	V_{DD2H}	V_{SS}	RDQS1_C_A	DQ10_A	ZQ_A_C	V_{SS}	G
H	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD2L}	V_{SS}	H
J	V_{SS}	V_{DD2L}	DQ2_C	RDQS0_C_C	V_{SS}	V_{DD2H}	DQ7_C	V_{DD2H}	CA2_C	V_{DD2L}	CA5_C	V_{DD2H}	DQ15_C	V_{DD2H}	V_{SS}	RDQS1_C_C	DQ10_C	RESET_N	V_{SS}	J
K	V_{SS}	V_{SS}	V_{DDQ}	RDQS0_T_C	V_{DD2H}	DQ4_C	V_{DDQ}	V_{SS}	V_{SS}	CK_C_C	V_{SS}	V_{SS}	V_{DDQ}	DQ12_C	V_{DD2H}	RDQS1_T_C	V_{DDQ}	V_{SS}	V_{SS}	K
L	V_{SS}	V_{DD2H}	DQ1_C	V_{SS}	WCK0_T_C	V_{SS}	DQ6_C	V_{DDQ}	CA1_C	CK_T_C	CA4_C	V_{DDQ}	DQ14_C	V_{SS}	WCK1_T_C	V_{SS}	DQ9_C	V_{DD2H}	V_{SS}	L
M	V_{SS}	V_{SS}	V_{SS}	DQ3_C	WCK0_C_C	V_{DDQ}	V_{SS}	CA0_C	V_{SS}	V_{SS}	V_{SS}	CA6_C	V_{SS}	V_{DDQ}	WCK1_C_C	DQ11_C	V_{SS}	VSS	V_{SS}	M
N	V_{SS}	V_{DD1}	DQ0_C	V_{DDQ}	V_{SS}	DMI0_C	DQ5_C	V_{SS}	CS0_C	CS1_C	CA3_C	V_{SS}	DQ13_C	DMI1_C	V_{SS}	V_{DDQ}	DQ8_C	V_{DD1}	V_{SS}	N
P	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	P
R	V_{SS}	V_{SS}				V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	R
T	V_{SS}	V_{SS}				V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	T
U	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	U
V	V_{SS}	V_{DD1}	DQ8_D	V_{DDQ}	V_{SS}	DMI1_D	DQ13_D	V_{SS}	CA3_D	CS1_D	CS0_D	V_{SS}	DQ5_D	DMI0_D	V_{SS}	V_{DDQ}	DQ0_D	V_{DD1}	V_{SS}	V
W	V_{SS}	V_{SS}	V_{SS}	DQ11_D	WCK1_C_D	V_{DDQ}	V_{SS}	CA6_D	V_{SS}	V_{SS}	V_{SS}	CA0_D	V_{SS}	V_{DDQ}	WCK0_C_D	DQ3_D	V_{SS}	V_{SS}	V_{SS}	W
Y	V_{SS}	V_{DD2H}	DQ9_D	V_{SS}	WCK1_T_D	V_{SS}	DQ14_D	V_{DDQ}	CA4_D	CK_T_D	CA1_D	V_{DDQ}	DQ6_D	V_{SS}	WCK0_T_D	V_{SS}	DQ1_D	V_{DD2H}	V_{SS}	Y
AA	V_{SS}	V_{SS}	V_{DDQ}	RDQS1_T_D	V_{DD2H}	DQ12_D	V_{DDQ}	V_{SS}	V_{SS}	CK_C_D	V_{SS}	V_{SS}	V_{DDQ}	DQ4_D	V_{DD2H}	RDQS0_T_D	V_{DDQ}	V_{SS}	V_{SS}	AA
AB	V_{SS}	V_{DD2L}	DQ10_D	RDQS1_C_D	V_{SS}	V_{DD2H}	DQ15_D	V_{DD2H}	CA5_D	V_{DD2L}	CA2_D	V_{DD2H}	DQ7_D	V_{DD2H}	V_{SS}	RDQS0_C_D	DQ2_D	V_{SS}	V_{SS}	AB
AC	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD2L}	V_{SS}	AC
AD	V_{SS}	V_{DD2L}	DQ10_B	RDQS1_C_B	V_{SS}	V_{DD2H}	DQ15_B	V_{DD2H}	CA5_B	V_{DD2L}	CA2_B	V_{DD2H}	DQ7_B	V_{DD2H}	V_{SS}	RDQS0_C_B	DQ2_B	ZQ_B_D	V_{SS}	AD
AE	V_{SS}	V_{SS}	V_{DDQ}	RDQS1_T_B	V_{DD2H}	DQ12_B	V_{DDQ}	V_{SS}	V_{SS}	CK_C_B	V_{SS}	V_{SS}	V_{DDQ}	DQ4_B	V_{DD2H}	RDQS0_T_B	V_{DDQ}	V_{SS}	V_{SS}	AE
AF	V_{SS}	V_{DD2H}	DQ9_B	V_{SS}	WCK1_T_B	V_{SS}	DQ14_B	V_{DDQ}	CA4_B	CK_T_B	CA1_B	V_{DDQ}	DQ6_B	V_{SS}	WCK0_T_B	V_{SS}	DQ1_B	V_{DD2H}	V_{SS}	AF
AG	V_{SS}	V_{DD1}	V_{SS}	DQ11_B	WCK1_C_B	V_{DDQ}	V_{SS}	CA6_B	V_{SS}	V_{SS}	V_{SS}	CA0_B	V_{SS}	V_{DDQ}	WCK0_C_B	DQ3_B	V_{SS}	V_{DD1}	V_{SS}	AG
AH	V_{SS}	V_{SS}	DQ8_B	V_{DDQ}	V_{SS}	DMI1_B	DQ13_B	V_{SS}	CA3_B	CS1_B	CS0_B	V_{SS}	DQ5_B	DMI0_B	V_{SS}	V_{DDQ}	DQ0_B	V_{SS}	V_{SS}	AH
AJ	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	AJ
AK	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	AK
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	

Top View (ball down)

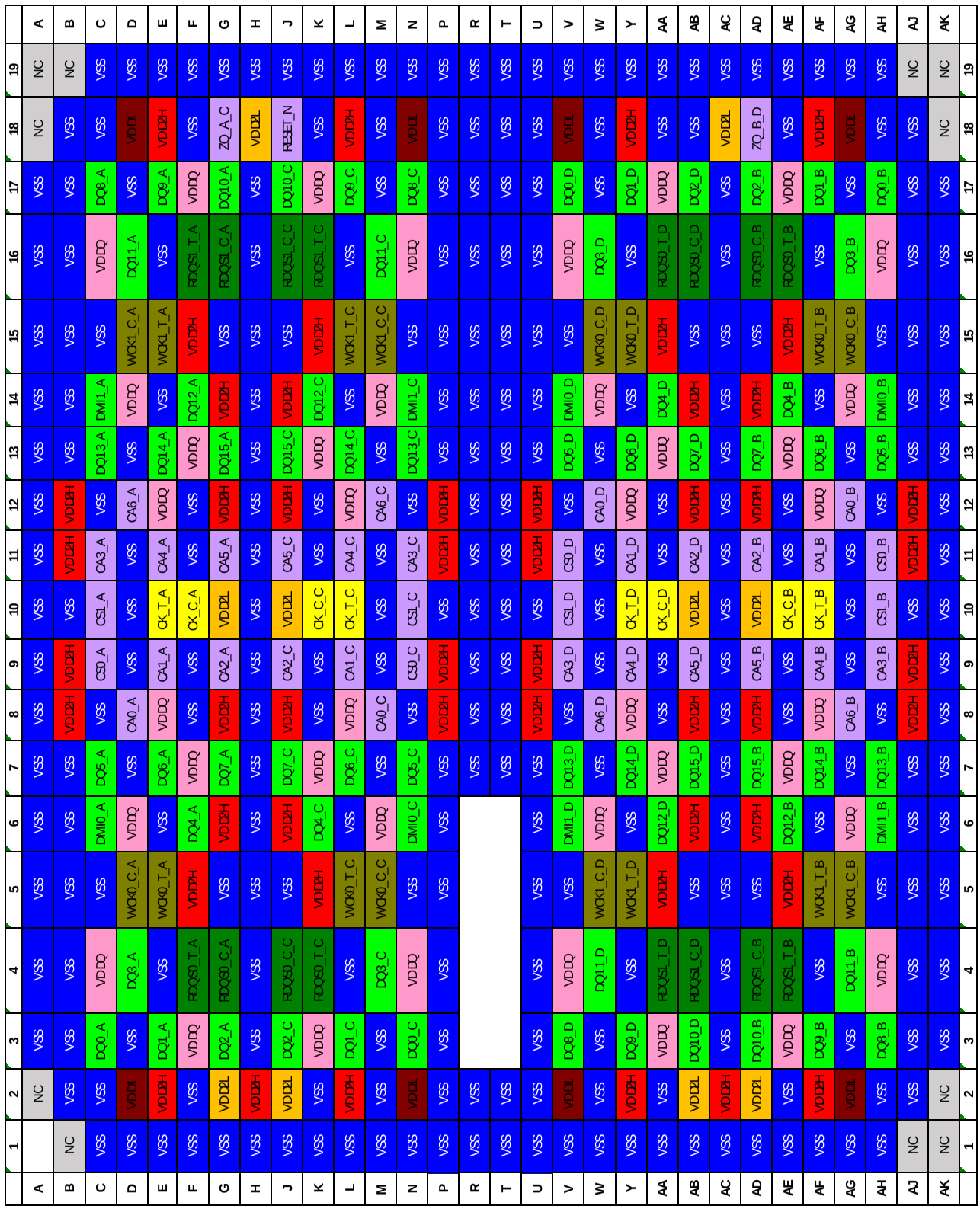
V_{SS} | V_{DD1} | V_{DD2H} | V_{DD2HQ} | V_{DD2L} | V_{DDQ} | CK | DQS, RDQS | DQ, DMI | WCK | CA, CS, ZQ, RESET | NC, RFU, DNU

561-Ball Quad-Channel, 1-Rank, 2-Rank

Table 15: Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:D] CK_c_[A:D]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:D], CS1_[A:D]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:D] become NC pins in a single-rank package.
CA[6:0]_[A:D]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:D] WCK[1:0]_c_[A:D]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for WRITE data capture and READ data output.
DQ[15:0]_[A:D]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A:D] RDQS[1:0]_c_[A:D]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:D]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A_C, ZQ_B_D	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240 ohm ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.

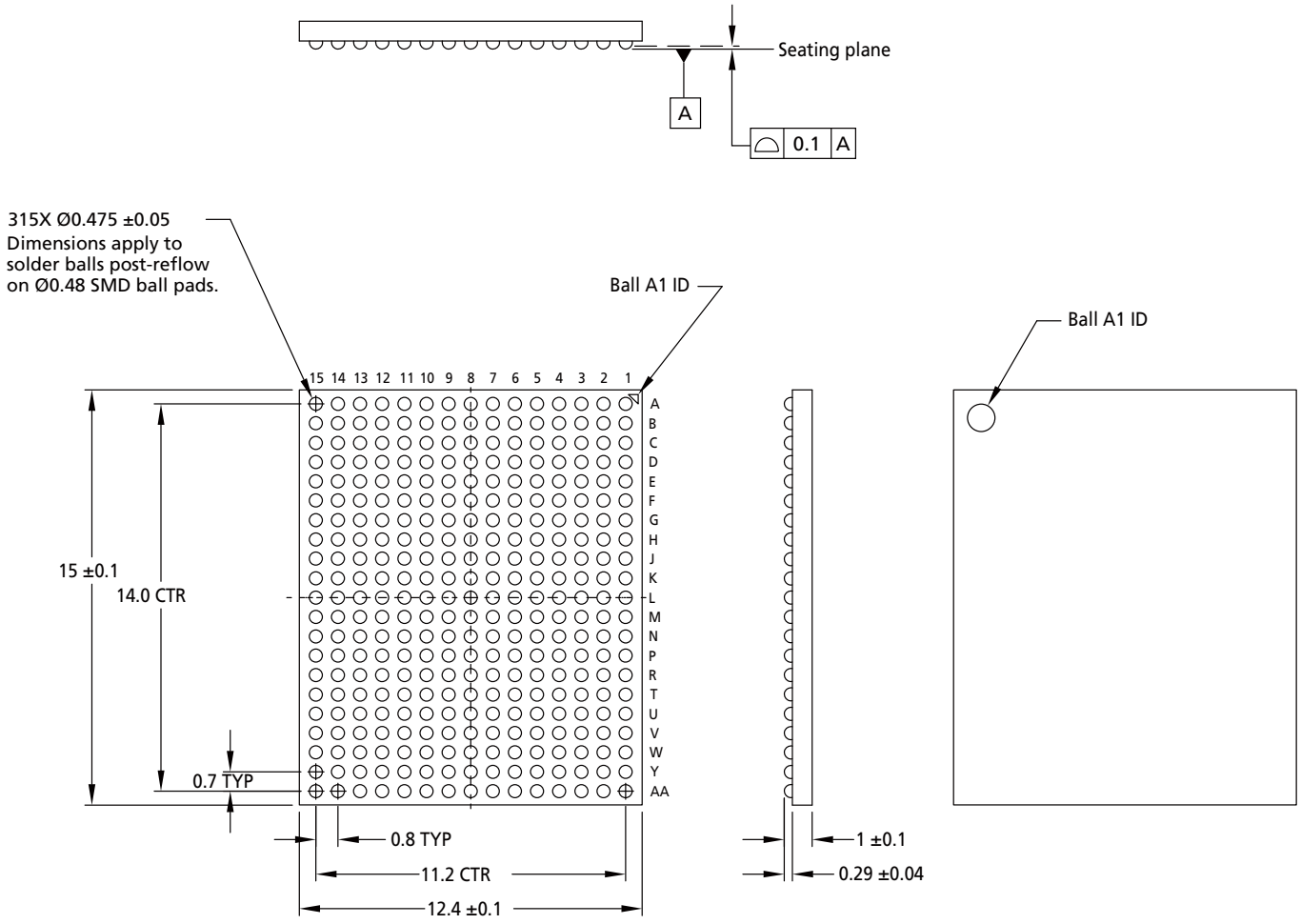
Figure 15: 561-Ball Quad-Channel FBGA



Package Dimensions

315-Ball Package (Package Code: DS)

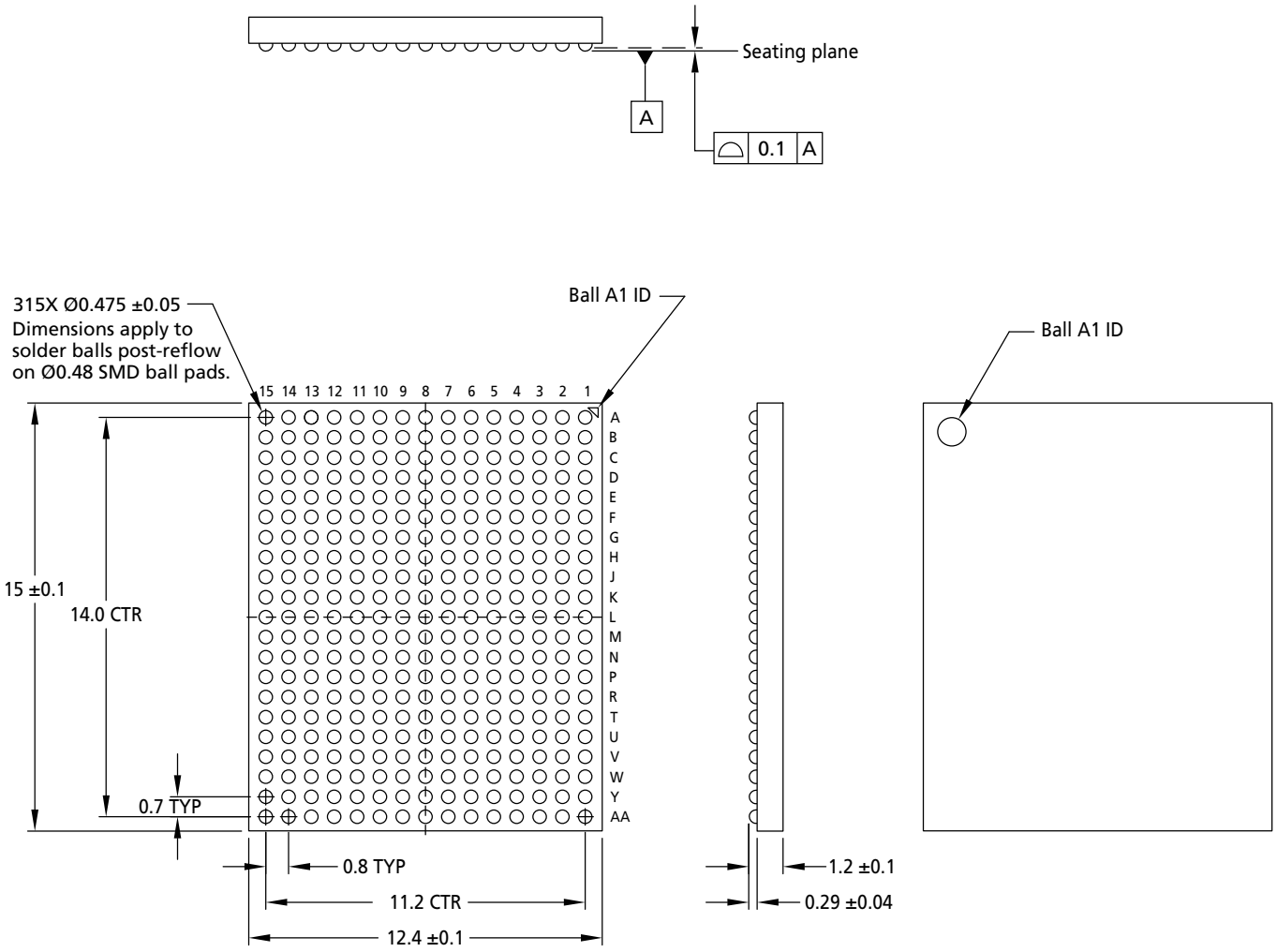
Figure 16: 315-Ball TFBGA – 12.4mm (TYP) × 15.0mm (TYP) × 1.1mm (MAX) (Package Code: DS)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni)

315-Ball Package (Package Code: DV)

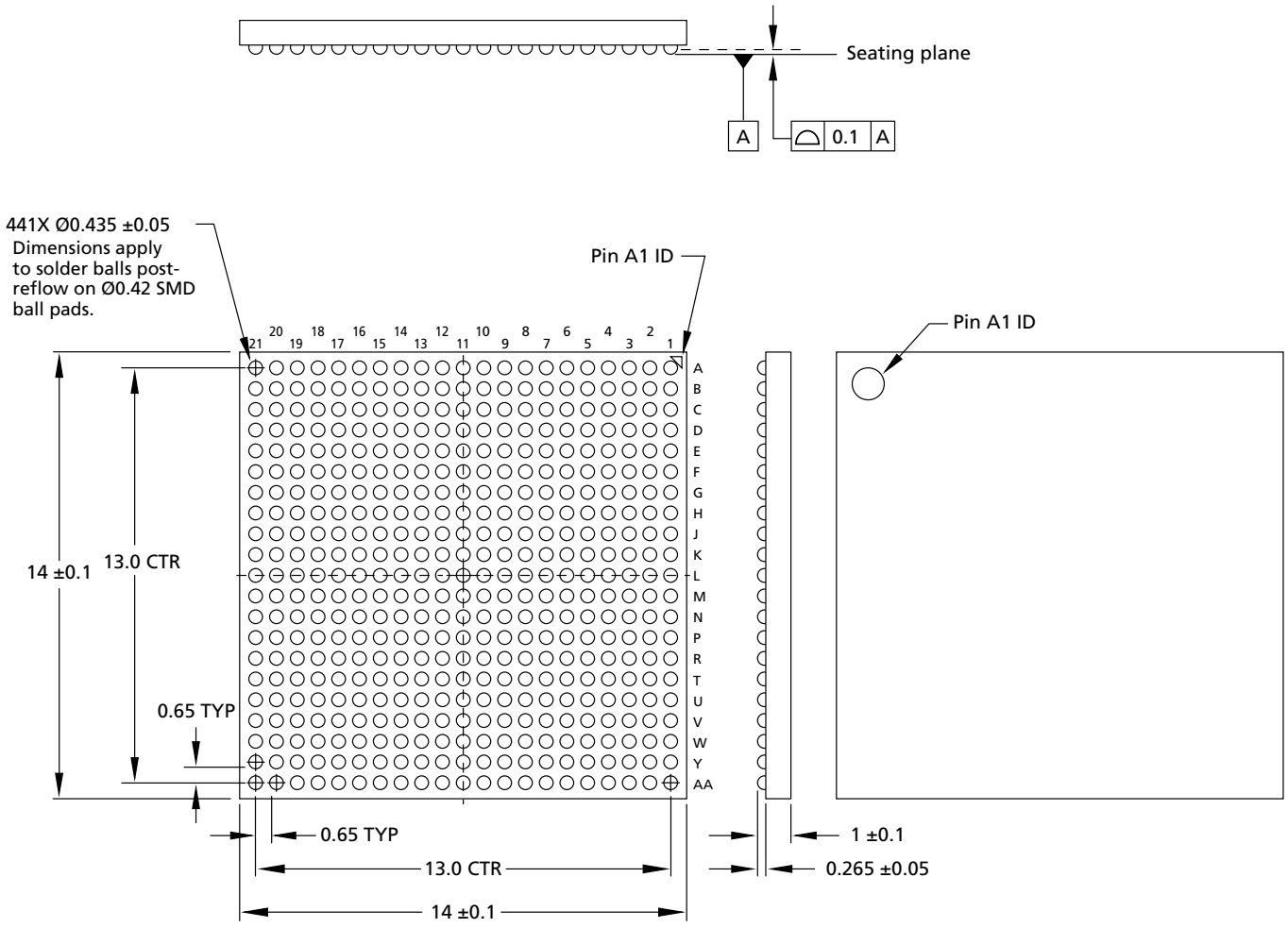
Figure 17: 315-Ball LFBGA – 12.4mm (TYP) × 15.0mm (TYP) × 1.3mm (MAX) (Package Code: DV)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni)

441-Ball Package (Package Code: EK)

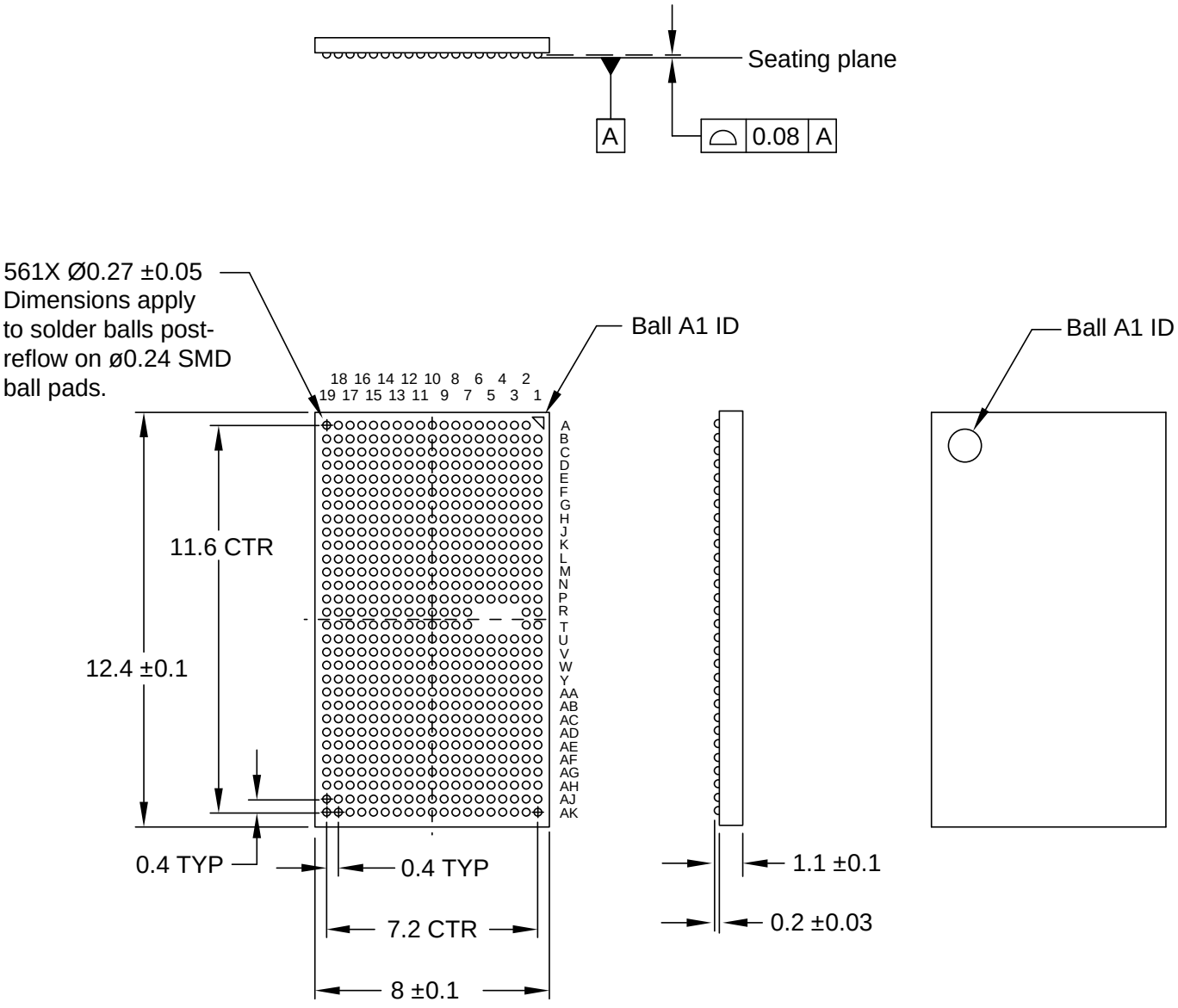
Figure 18: 441-Ball TFBGA – 14.0mm (TYP) x 14.0mm (TYP) x 1.1mm (MAX) (Package Code: EK)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni).

561-Ball Package (Package Code: CZ)

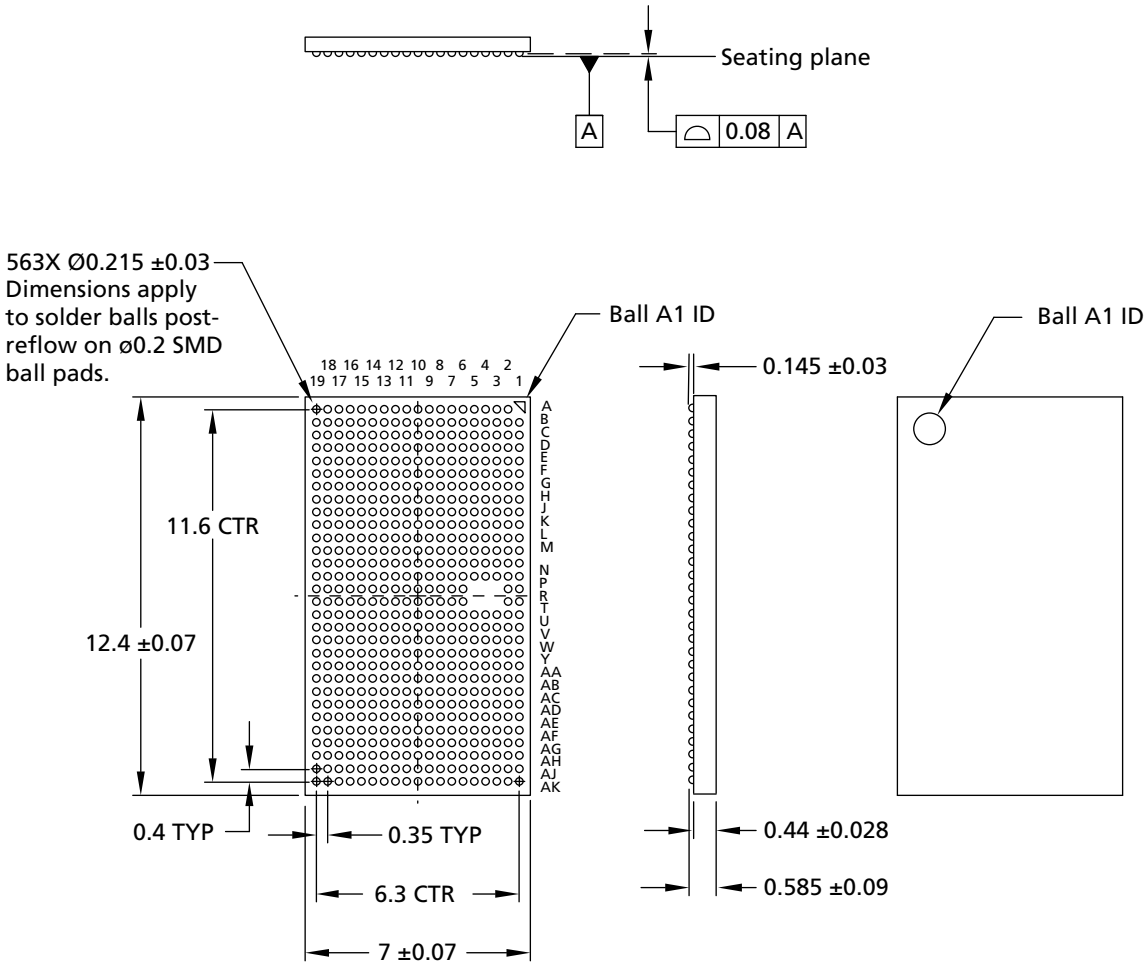
Figure 19: 561-Ball TFBGA – 8.0mm (TYP) × 12.4mm (TYP) × 1.2mm (MAX) (Package Code: CZ)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn- 4Ag-0.5Cu-3Bi-0.05Ni)

563-Ball Package (Package Code: AH)

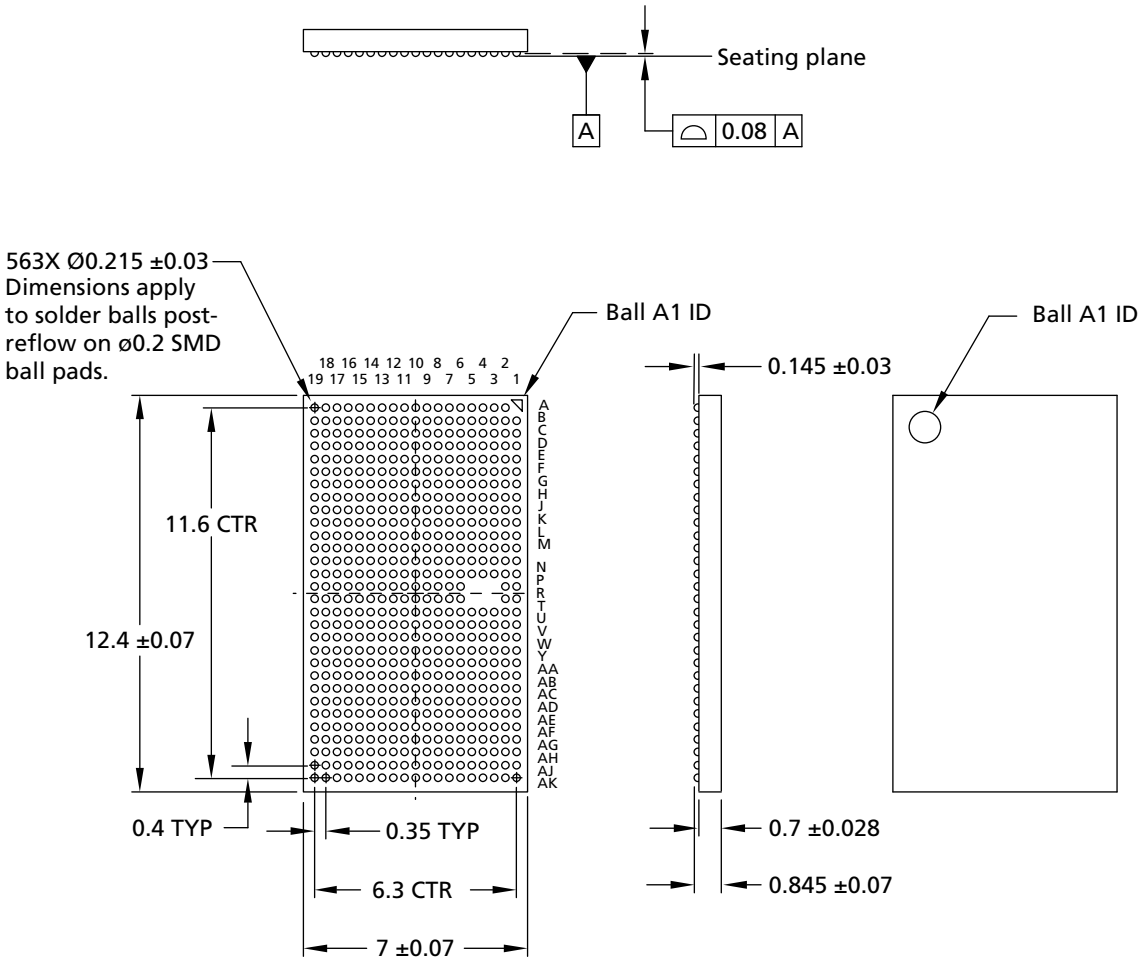
Figure 20: 563-Ball WFBGA – 7.0mm (TYP) x 12.4mm (TYP) x 0.675mm (MAX) (Package Code: AH)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SAC302 with Ni/Au pads (Sn-3Ag-0.2Cu).

563-Ball Package (Package Code: AJ)

Figure 21: 563-Ball VFBGA – 7.0mm (TYP) x 12.4mm (TYP) x 0.915mm (MAX) (Package Code: AJ)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SAC302 with Ni/Au pads (Sn-3Ag-0.2Cu).

Package Thermal Impedance

Table 16: Package Thermal Impedance Characteristics

Die Revision	Package	Parameter	Symbol	Value	Unit
Rev C	315-ball, DDP, package code DS	Junction-to-case (TOP)	Θ_{JC}	4.7	°C/W
		Junction-to-board	Θ_{JB}	13.9	°C/W
	315-ball, QDP, package code DS	Junction-to-case (TOP)	Θ_{JC}	4.1	°C/W
		Junction-to-board	Θ_{JB}	14.5	°C/W
	315-ball, 8DP, package code DV	Junction-to-case (TOP)	Θ_{JC}	4.4	°C/W
		Junction-to-board	Θ_{JB}	15.6	°C/W
	441-ball, QDP, package code EK	Junction-to-case (TOP)	Θ_{JC}	3.0	°C/W
		Junction-to-board	Θ_{JB}	9.5	°C/W
	441-ball, 8DP, package code EK	Junction-to-case (TOP)	Θ_{JC}	2.6	°C/W
		Junction-to-board	Θ_{JB}	9.0	°C/W
	561-ball, QDP, package code CZ	Junction-to-case (TOP)	Θ_{JC}	4.6	°C/W
		Junction-to-board	Θ_{JB}	14.7	°C/W
	561-ball, 8DP, package code CZ	Junction-to-case (TOP)	Θ_{JC}	5.0	°C/W
		Junction-to-board	Θ_{JB}	16.3	°C/W
	563-ball, QDP, package code AH	Junction-to-case (TOP)	Θ_{JC}	3.3	°C/W
		Junction-to-board	Θ_{JB}	9.1	°C/W
	563-ball, 8DP, package code AJ	Junction-to-case (TOP)	Θ_{JC}	4.1	°C/W
		Junction-to-board	Θ_{JB}	10.1	°C/W

Product-Specific Mode Register Definition

Table 17: Mode Register Contents

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0	**Per-pin DFE**	**Pre Emphasis**	**Unified NT ODT behavior mode**	**DMI output behavior mode**	**Optimized refresh mode**	**Enhanced WCK always-on mode**	**Latency mode**	**NT ODT timing mode**
	OP[0] = 1b: Device supports different NT ODT latency for DQ and RDQS							
	OP[1] = 0b: Device supports x16 mode latency for 1G16, 1G32, 2G32, 1G64, 2G64 OP[1] = 1b: Device supports x8 mode latency for 4G32							
	OP[2] = 1b: Device supports enhanced WCK always-on mode							
	OP[3] = 1b: Device supports optimized refresh mode							
	OP[4] = 1b: Device supports both DMI behavior mode 1 and 2 and mode selection							
	OP[5] = 1b: The NT ODT behavior follows the unified NT ODT behavior							
	OP[6] = 1b: Device supports Pre Emphasis mode							
	OP[7] = 1b: Device supports Per Pin DFE							
MR1						**DRFM support[3]**	**ARFM support[3]**	**CS ODT OP support**
	OP[0] = 1b: Device supports CS ODT behavior OP							
	OP[1] = 1b: Device supports ARFM							
	OP[2] = 0b: Device does not support DRFM							
MR3				**BK/BG ORG**				
	OP[4:3] = 00b: BG, 10b: 16B Mode support							
MR4				**Refresh Multiplier** (Note 7)				
	OP[4:0]: Refer to General LPDDR5/LPDDR5X Specification 1 for mode register definitions.							
MR5	**Manufacturer ID**							
	1111 1111b: Micron							
MR6	**Revision ID1**							
	0000 1000b							
MR8	**I/O width**		**Density**				**Device Type[6]**	
	OP[7:6] = 00b: x16 for 1G16, 1G32, 2G32, 1G64, 2G64 OP[7:6] = 01b: x8 for 4G32		OP[5:2] = 0110b: 16Gb				OP[1:0] = 01b: LPDDR5X SDRAM	
MR13						**VRO**		
	OP[2] = 0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6							
MR19			**WCK2DQ OSC FM**					
	OP[5] = 1b: WCK2DQ OSC FM supported							

Table 17: Mode Register Contents (Continued)

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR21	**WXS**				**ODTD-CSFS**	**WXFS**	**RDCFS**	**WDCFS**
	OP[0] = 1b: WRITE DATA COPY function supported							
	OP[1] = 1b: READ DATA COPY function supported							
	OP[2] = 1b: WRITE X function supported							
	OP[3] = 1b: Device ODTD-CS is supported							
	OP[7] = 1b: Data to be written can be selected with 0 and 1							
MR22	**RECC**		**WECC**					
	OP[5:4] = 00b: Write link ECC disabled (default) 01b: Write link ECC enabled (See Note 4)							
	OP[7:6] = 00b: Read link ECC disabled (default) 01b: Read link ECC enabled (See Note 4)							
MR24	**DFES**				**Read DCA**			
	OP[3] = 1b: Device supports Read DCA							
	OP[7] = 1b: Device supports DFE (See Note 5)							
MR26		**RDQSTFS**						
	OP[6] = 1b: Read/write-based RDQS_t TRAINING function supported							
MR27	**RAAMULT**		**RAAIMT**					**RFM**
	OP[0] = 1b: RFM is required							
	OP[5:1] = 00101b: 40							
	OP[7:6] = 01b: 4X							
MR41					**E-DVFSC ODT**	**DVFSC/E-DVFSC Support**		
	OP[2:1] = 01b: Only Enhanced DVFSC Mode supported							
	OP[3] = 0b: Enhanced DVFSC ODT option not supported							
MR43		**SBEC rule**						
	OP[6] = 1b: Simultaneous SBE on each DQ byte and DMI are independently counted							
MR57	**ARFM**[3]		**RFMSBC**		**RFMSB**		**RAADEC**	
	OP[1:0] = 10b: 2 × RAAIMT							
	OP[3:2] = 00b: Single Bank Mode not supported							
	OP[5:4] = 00b: One RAA counter per two banks (1 of 8)							
	OP[7:6] = 00b: default (00101b: 40), 01b: Level A, 10b: Level B, 11b: Level C							

Notes: 1. The contents of mode registers described here reflect information specific to each die in these packages.
2. Refer to General LPDDR5/LPDDR5X Specification 1 for mode registers not described here.
3. Refer to General LPDDR5/LPDDR5X Specification 3 for feature description not described here.
4. Write link ECC and read link ECC are supported.
5. Device supports 7-step DFE.
6. Device type only supports Bank Group and 16B modes.
7. MR4:OP[4:0] output from each die in a defined package shall be used to determine the required package level refresh rate. Any other method used to determine a valid refresh rate, places ownership and responsibility of the correct refresh rate on the system developer or end user. T_{OPER} (case surface temperature) shall be used to determine whether operating temperature requirements are being met. Any other method used to determine

operating temperature, places ownership and responsibility of the correct operating temperature on the system developer or end user.

I_{DD} Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section in General LPDDR5/LPDDR5X Specifications 2 for detailed conditions.

Table 18: WT I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade				Unit	Note
		x8 Mode		x16 Mode			
		7500 Mb/s	8533 Mb/s	7500 Mb/s	8533 Mb/s		
I_{DD01}	V_{DD1}	3.80	3.80	3.80	3.80	mA	
I_{DD02H}	V_{DD2H}	51.00	51.00	53.00	53.00		
I_{DD02L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD0Q}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD2P1}	V_{DD1}	1.50	1.50	1.50	1.50	mA	
I_{DD2P2H}	V_{DD2H}	3.90	3.90	3.90	3.90		
I_{DD2P2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD2PQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD2PS1}	V_{DD1}	1.50	1.50	1.50	1.50	mA	
$I_{DD2PS2H}$	V_{DD2H}	3.90	3.90	3.90	3.90		
$I_{DD2PS2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD2PSQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD2N1}	V_{DD1}	1.50	1.50	1.50	1.50	mA	
I_{DD2N2H}	V_{DD2H}	31.00	31.00	32.50	32.50		
I_{DD2N2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD2NQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD2NS1}	V_{DD1}	1.50	1.50	1.50	1.50	mA	
$I_{DD2NS2H}$	V_{DD2H}	31.00	31.00	32.50	32.50		
$I_{DD2NS2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD2NSQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD3P1}	V_{DD1}	2.40	2.40	2.50	2.50	mA	
I_{DD3P2H}	V_{DD2H}	12.50	12.50	12.50	12.50		
I_{DD3P2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD3PQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD3PS1}	V_{DD1}	2.40	2.40	2.50	2.50	mA	
$I_{DD3PS2H}$	V_{DD2H}	12.50	12.50	12.50	12.50		
$I_{DD3PS2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD3PSQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD3N1}	V_{DD1}	2.80	2.80	2.80	2.80	mA	
I_{DD3N2H}	V_{DD2H}	38.00	38.00	40.00	40.00		
I_{DD3N2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD3NQ}	V_{DDQ}	0.60	0.60	0.60	0.60		

Table 18: WT I_{DD} Parameters – Single Die (Continued)

Symbol	Supply	Speed Grade				Unit	Note
		x8 Mode		x16 Mode			
		7500 Mb/s	8533 Mb/s	7500 Mb/s	8533 Mb/s		
I_{DD4R1}	V_{DD1}	16.50	18.50	18.00	20.50	mA	3, 4, 6
I_{DD4R2H}	V_{DD2H}	235.00	260.00	390.00	430.00		
I_{DD4R2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD4RQ}	V_{DDQ}	56.00	60.50	111.90	121.00		
I_{DD4W1}	V_{DD1}	15.50	17.50	16.50	18.50	mA	3, 6
I_{DD4W2H}	V_{DD2H}	170.00	180.00	265.00	280.00		
I_{DD4W2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD4WQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD51}	V_{DD1}	23.50	23.50	24.00	24.00	mA	
I_{DD52H}	V_{DD2H}	205.00	205.00	205.00	205.00		
I_{DD52L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD5Q}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD5AB1}	V_{DD1}	3.60	3.60	3.60	3.60	mA	
$I_{DD5AB2H}$	V_{DD2H}	46.00	46.00	47.00	47.00		
$I_{DD5AB2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD5ABQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD5PB1}	V_{DD1}	3.60	3.60	3.60	3.60	mA	
$I_{DD5PB2H}$	V_{DD2H}	46.00	46.00	47.00	47.00		
$I_{DD5PB2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD5PBQ}	V_{DDQ}	0.60	0.60	0.60	0.60		

Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode enabled. DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V (DVFSQ disabled)/0.27-0.37V (DVFSQ enabled); T_C = –25°C to +85°C
6. IDD4R2 and IDD4W2 have implemented a more stringent pattern than required by JEDEC and therefore these IDD values are slightly higher than if the JEDEC pattern was used.
7. Notes 1, 2, and 5 apply to entire table.

Table 19: WT I_{DD} Parameters – With Enhanced DVFSC Enabled - Single Die

Symbol	Supply	Speed Grade		Unit	Note
		x8 Mode	x16 Mode		
		3200 Mb/s	3200 Mb/s		
$I_{DD4R-DVFSC1}$	V_{DD1}	9.0	10.0	mA	3, 4, 6
$I_{DD4R-DVFSC2H}$	V_{DD2H}	30.0	32.0		
$I_{DD4R-DVFSC2L}$	V_{DD2L}	70.0	115.0		
$I_{DD4R-DVFSCQ}$	V_{DDQ}	37.4	74.7		
$I_{DD4W-DVFSC1}$	V_{DD1}	8.5	9.0	mA	3, 6
$I_{DD4W-DVFSC2H}$	V_{DD2H}	27.0	29.0		
$I_{DD4W-DVFSC2L}$	V_{DD2L}	45.0	80.0		
$I_{DD4W-DVFSCQ}$	V_{DDQ}	0.6	0.6		
I_{DD5ED1}	V_{DD1}	20.5	21.0	mA	
$I_{DD5ED2H}$	V_{DD2H}	160.0	160.0		
$I_{DD5ED2L}$	V_{DD2L}	26.5	26.5		
I_{DD5EDQ}	V_{DDQ}	0.6	0.6		
$I_{DD5ABED1}$	V_{DD1}	3.4	3.4	mA	
$I_{DD5ABED2H}$	V_{DD2H}	24.0	24.0		
$I_{DD5ABED2L}$	V_{DD2L}	18.5	22.0		
$I_{DD5ABEDQ}$	V_{DDQ}	0.6	0.6		
$I_{DD5PBED1}$	V_{DD1}	3.4	3.4	mA	
$I_{DD5PBED2H}$	V_{DD2H}	24.0	24.0		
$I_{DD5PBED2L}$	V_{DD2L}	18.5	22.0		
$I_{DD5PBEDQ}$	V_{DDQ}	0.6	0.6		

Notes:
1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. Enhanced DVFSC enabled, DVFSQ enabled, 3200 Mb/s, 16B mode
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V (DVFSQ disabled)/0.27-0.37V (DVFSQ enabled); T_C = –25°C to +85°C
6. IDD4R2 and IDD4W2 have implemented a more stringent pattern than required by JEDEC and therefore these IDD values are slightly higher than if the JEDEC pattern was used.
7. Notes 1, 2, and 5 apply to entire table.

Table 20: WT Full-Array Power-Down Self Refresh Current – Single Die

Temperature	Symbol	Supply	Value	Unit	Notes
25°C	I_{DD61}	V_{DD1}	0.27	mA	
	I_{DD62H}	V_{DD2H}	1.00		
	I_{DD62L}	V_{DD2L}	2.00	uA	4
	I_{DD6Q}	V_{DDQ}	30.00		
	I_{DD6DS1}	V_{DD1}	0.27	mA	
	$I_{DD6DS2H}$	V_{DD2H}	1.00		
	$I_{DD6DS2L}$	V_{DD2L}	2.00	uA	4
	I_{DD6DSQ}	V_{DDQ}	30.00		
45°C	I_{DD61}	V_{DD1}	0.4	mA	
	I_{DD62H}	V_{DD2H}	1.4		
	I_{DD62L}	V_{DD2L}	2.00	uA	4
	I_{DD6Q}	V_{DDQ}	30.00		
	I_{DD6DS1}	V_{DD1}	0.4	mA	
	$I_{DD6DS2H}$	V_{DD2H}	1.4		
	$I_{DD6DS2L}$	V_{DD2L}	2.00	uA	4
	I_{DD6DSQ}	V_{DDQ}	30.00		
65°C	I_{DD61}	V_{DD1}	0.85	mA	
	I_{DD62H}	V_{DD2H}	3.2		
	I_{DD62L}	V_{DD2L}	2.00	uA	4
	I_{DD6Q}	V_{DDQ}	30.00		
	I_{DD6DS1}	V_{DD1}	0.85	mA	
	$I_{DD6DS2H}$	V_{DD2H}	3.2		
	$I_{DD6DS2L}$	V_{DD2L}	2.00	uA	4
	I_{DD6DSQ}	V_{DDQ}	30.00		
85°C	I_{DD61}	V_{DD1}	3.70	mA	
	I_{DD62H}	V_{DD2H}	21.00		
	I_{DD62L}	V_{DD2L}	0.20	mA	4
	I_{DD6Q}	V_{DDQ}	0.60		
	I_{DD6DS1}	V_{DD1}	3.70	mA	
	$I_{DD6DS2H}$	V_{DD2H}	21.00		
	$I_{DD6DS2L}$	V_{DD2L}	0.20	mA	4
	I_{DD6DSQ}	V_{DDQ}	0.60		

Notes: 1. I_{DD6}25/45/65°C is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD6}85°C is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. DVFSC and DVFSQ disabled.
3. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –25°C to +85°C
4. While entering and exiting self-refresh modes, all defined/used supply rails (V_{DD1}, V_{DD2H}, V_{DD2L}, V_{DDQ}) are required to be at valid levels. After the self-refresh with power down mode entrance commands are completed and ^{t}ESPD timing requirement has been satisfied, the V_{DDQ} power rail may be turned off by the controller.

Table 21: IT I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade				Unit	Note
		x8 Mode		x16 Mode			
		7500 Mb/s	8533 Mb/s	7500 Mb/s	8533 Mb/s		
I_{DD01}	V_{DD1}	4.10	4.10	4.10	4.10	mA	
I_{DD02H}	V_{DD2H}	63.00	63.00	66.00	66.00		
I_{DD02L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD0Q}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD2P1}	V_{DD1}	1.80	1.80	1.80	1.80	mA	
I_{DD2P2H}	V_{DD2H}	5.80	5.80	5.80	5.80		
I_{DD2P2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD2PQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD2PS1}	V_{DD1}	1.80	1.80	1.80	1.80	mA	
$I_{DD2PS2H}$	V_{DD2H}	5.80	5.80	5.80	5.80		
$I_{DD2PS2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD2PSQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD2N1}	V_{DD1}	1.70	1.70	1.70	1.70	mA	
I_{DD2N2H}	V_{DD2H}	43.00	43.00	46.00	46.00		
I_{DD2N2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD2NQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD2NS1}	V_{DD1}	1.70	1.70	1.70	1.70	mA	
$I_{DD2NS2H}$	V_{DD2H}	43.00	43.00	46.00	46.00		
$I_{DD2NS2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD2NSQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD3P1}	V_{DD1}	2.80	2.80	2.90	2.90	mA	
I_{DD3P2H}	V_{DD2H}	15.50	15.50	15.50	15.50		
I_{DD3P2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD3PQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD3PS1}	V_{DD1}	2.80	2.80	2.90	2.90	mA	
$I_{DD3PS2H}$	V_{DD2H}	15.50	15.50	15.50	15.50		
$I_{DD3PS2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD3PSQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD3N1}	V_{DD1}	3.10	3.10	3.10	3.10	mA	
I_{DD3N2H}	V_{DD2H}	53.50	53.50	56.50	56.50		
I_{DD3N2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD3NQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD4R1}	V_{DD1}	16.50	18.50	18.00	20.50	mA	3, 4, 6
I_{DD4R2H}	V_{DD2H}	260.00	280.00	410.00	450.00		
I_{DD4R2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD4RQ}	V_{DDQ}	56.00	60.50	111.90	121.00		

Table 21: IT I_{DD} Parameters – Single Die (Continued)

Symbol	Supply	Speed Grade				Unit	Note
		x8 Mode		x16 Mode			
		7500 Mb/s	8533 Mb/s	7500 Mb/s	8533 Mb/s		
I_{DD4W1}	V_{DD1}	15.50	17.50	16.50	18.50	mA	3, 6
I_{DD4W2H}	V_{DD2H}	185.00	195.00	280.00	295.00		
I_{DD4W2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD4WQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD51}	V_{DD1}	23.50	23.50	24.00	24.00	mA	
I_{DD52H}	V_{DD2H}	205.00	205.00	205.00	205.00		
I_{DD52L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD5Q}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD5AB1}	V_{DD1}	3.60	3.60	3.60	3.60	mA	
$I_{DD5AB2H}$	V_{DD2H}	55.00	55.00	56.00	56.00		
$I_{DD5AB2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD5ABQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD5PB1}	V_{DD1}	3.60	3.60	3.60	3.60	mA	
$I_{DD5PB2H}$	V_{DD2H}	55.00	55.00	56.00	56.00		
$I_{DD5PB2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD5PBQ}	V_{DDQ}	0.60	0.60	0.60	0.60		

Notes:
1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode enabled. DVFSC, Enhanced DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V (DVFSQ disabled)/0.27-0.37V (DVFSQ enabled); T_C = –40°C to +95°C
6. IDD4R2 and IDD4W2 have implemented a more stringent pattern than required by JEDEC and therefore these IDD values are slightly higher than if the JEDEC pattern was used.
7. Notes 1, 2, and 5 apply to entire table.

Table 22: IT I_{DD} Parameters – With Enhanced DVFSC Enabled - Single Die

Symbol	Supply	Speed Grade		Unit	Note
		x8 Mode	x16 Mode		
		3200 Mb/s	3200 Mb/s		
$I_{DD4R-DVFSC1}$	V_{DD1}	9.0	10.0	mA	3, 4, 6
$I_{DD4R-DVFSC2H}$	V_{DD2H}	31.0	33.0		
$I_{DD4R-DVFSC2L}$	V_{DD2L}	73.0	120.0		
$I_{DD4R-DVFSCQ}$	V_{DDQ}	37.4	74.7		
$I_{DD4W-DVFSC1}$	V_{DD1}	8.5	9.0	mA	3, 6
$I_{DD4W-DVFSC2H}$	V_{DD2H}	28.0	30.0		
$I_{DD4W-DVFSC2L}$	V_{DD2L}	57.0	95.0		
$I_{DD4W-DVFSCQ}$	V_{DDQ}	0.6	0.6		
I_{DD5ED1}	V_{DD1}	20.5	21.0	mA	
$I_{DD5ED2H}$	V_{DD2H}	160.0	160.0		
$I_{DD5ED2L}$	V_{DD2L}	26.5	26.5		
I_{DD5EDQ}	V_{DDQ}	0.6	0.6		
$I_{DD5ABED1}$	V_{DD1}	3.4	3.4	mA	
$I_{DD5ABED2H}$	V_{DD2H}	28.0	28.0		
$I_{DD5ABED2L}$	V_{DD2L}	22.0	26.0		
$I_{DD5ABEDQ}$	V_{DDQ}	0.6	0.6		
$I_{DD5PBED1}$	V_{DD1}	3.4	3.4	mA	
$I_{DD5PBED2H}$	V_{DD2H}	28.0	28.0		
$I_{DD5PBED2L}$	V_{DD2L}	22.0	26.0		
$I_{DD5PBEDQ}$	V_{DDQ}	0.6	0.6		

Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. Enhanced DVFSC enabled, DVFSQ enabled, 3200 Mb/s, 16B mode
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V (DVFSQ disabled)/0.27-0.37V (DVFSQ enabled); T_C = –40°C to +95°C
6. IDD4R2 and IDD4W2 have implemented a more stringent pattern than required by JEDEC and therefore these IDD values are slightly higher than if the JEDEC pattern was used.
7. Notes 1, 2, and 5 apply to entire table.

Table 23: IT Full-Array Power-Down Self Refresh Current – Single Die

Temperature	Symbol	Supply	Value	Unit	Notes
25°C	I_{DD61}	V_{DD1}	0.27	mA	
	I_{DD62H}	V_{DD2H}	1.00		
	I_{DD62L}	V_{DD2L}	2.00	uA	4
	I_{DD6Q}	V_{DDQ}	30.00		
	I_{DD6DS1}	V_{DD1}	0.27	mA	
	$I_{DD6DS2H}$	V_{DD2H}	1.00		
	$I_{DD6DS2L}$	V_{DD2L}	2.00	uA	4
	I_{DD6DSQ}	V_{DDQ}	30.00		
45°C	I_{DD61}	V_{DD1}	0.4	mA	
	I_{DD62H}	V_{DD2H}	1.4		
	I_{DD62L}	V_{DD2L}	2.00	uA	4
	I_{DD6Q}	V_{DDQ}	30.00		
	I_{DD6DS1}	V_{DD1}	0.4	mA	
	$I_{DD6DS2H}$	V_{DD2H}	1.4		
	$I_{DD6DS2L}$	V_{DD2L}	2.00	uA	4
	I_{DD6DSQ}	V_{DDQ}	30.00		
65°C	I_{DD61}	V_{DD1}	0.85	mA	
	I_{DD62H}	V_{DD2H}	3.2		
	I_{DD62L}	V_{DD2L}	2.00	uA	4
	I_{DD6Q}	V_{DDQ}	30.00		
	I_{DD6DS1}	V_{DD1}	0.85	mA	
	$I_{DD6DS2H}$	V_{DD2H}	3.2		
	$I_{DD6DS2L}$	V_{DD2L}	2.00	uA	4
	I_{DD6DSQ}	V_{DDQ}	30.00		
85°C	I_{DD61}	V_{DD1}	3.70	mA	
	I_{DD62H}	V_{DD2H}	21.00		
	I_{DD62L}	V_{DD2L}	0.20	mA	4
	I_{DD6Q}	V_{DDQ}	0.60		
	I_{DD6DS1}	V_{DD1}	3.70	mA	
	$I_{DD6DS2H}$	V_{DD2H}	21.00		
	$I_{DD6DS2L}$	V_{DD2L}	0.20	mA	4
	I_{DD6DSQ}	V_{DDQ}	0.60		

Notes: 1. I_{DD6}25/45/65°C is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD6}85°C is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. DVFSC and DVFSQ disabled.
3. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –40°C to +95°C
4. While entering and exiting self-refresh modes, all defined/used supply rails (V_{DD1}, V_{DD2H}, V_{DD2L}, V_{DDQ}) are required to be at valid levels. After the self-refresh with power down mode entrance commands are completed and ^{t}ESPD timing requirement has been satisfied, the V_{DDQ} power rail may be turned off by the controller.

Revision History

Rev. G – 09/2024

- Added missing IDD6 and DVFSC related IDD values
- Added IDD4R and IDD4W notes to the datasheet

Rev. F – 05/2024

- Updated Note 1 on the Features page to expand to 7500 Mb/s
- Changed Thermal Resistance to Thermal Impedance

Rev. E – 12/2023

- Updated Important Notes and Warnings section
- Updated General Notes to highlight precedence between core data sheet and specific data sheet
- Added adjustments to CS Rx and DQ Rx mask parameters
- Added table for DQ Rx adjustments at 3200 MHz
- Updated Mode Register Contents table: Added DRFM support bit to MR1; Added DFE support bit to MR24; Added E-DVFSC ODT OP support to MR41
- Removed I_{DD3NS} from I_{DD} tables
- Added clarification to I_{DD} table notes
- Added DVFSC enabled I_{DD} parameters to I_{DD} tables. Parameters affected = I_{DD4R}, I_{DD4W}
- Corrected I_{DD6} labels which were missing the DS for deep sleep mode
- Added I_{DD6} table entries for 45°C and 65°C, adjusted I_{DD6} IT limits to align with WT
- Updated I_{DD6} Note 4 to align with core data sheet description

Rev. D – 09/2023

- Updated legal status to Production
- Added the 561-ball package mechanical drawing
- Added pinout description for 561-ball package
- Added details on feature page.
- Added MR4 to the register definition section along with Note 7, to highlight how refresh rate is defined.
- Added Package Thermal impedance characteristics details

Rev. C – 06/2023

- Corrected the 563-ball package drawings to show 3 digits of precision for both the AJ package and the AH package
- Updated top page to align with the AH and AJ package z-height changes
- Added the DVFSC enabled IDD parameters to the IDD tables. Parameters affected = IDD4R, IDD4W, IDD5, IDD5AB, IDD5PB
- Corrected the ARFM support bit value from 0b to 1b
- Corrected the RAAIMT defined bits from 01110b to 00101b which is the correct value for 40

Rev. B – 02/2023

- Added E-DVFSC ODT MR41:OP[3] details for non-support
- Changed the RFM single bank support check bit to RFMSB not supported
- Updated the preliminary IDD values to align with latest data
- Corrected the 563-ball package to be the AH package

Rev. A – 10/2022

- Initial Preliminary data sheet release

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006
208-368-4000, micron.com/support

This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.