NAND Flash with Mobile LPDDR4/ LPDDR4X 149-Ball MCP

MT29GZ9A9BPMET-046AIT.265, MT29GZ9A9BPMET-046AAT.265

Features

- Micron® NAND Flash and LPDDR4/LPDDR4X components
- RoHS-compliant, "green" package
- Separate NAND Flash and LPDDR4/LPDDR4X interfaces
- Space-saving multichip package (MCP)
- Low-voltage operation
- Industrial temperature range: –40°C to +85°C
- Automotive temperature range: –40°C to +105°C
- AEC-Q100

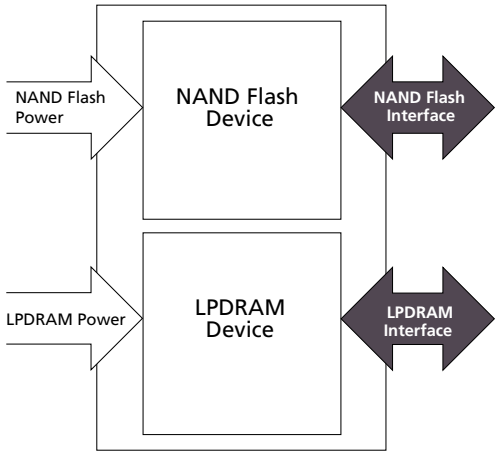
NAND Flash-Specific Features

- Organization
  - Page size x8: 4352 bytes (4096 + 256 bytes)
  - Block size: 64 pages
  - Number of planes: 1
- V_{CC} = 1.70–1.95V; 1.80V nominal

Mobile LPDDR4/LPDDR4X-Specific Features

- Ultra-low-voltage core and I/O power supply
  - V_{DD1} = 1.70–1.95V; 1.80V nominal
  - V_{DD2} = 1.06–1.17V; 1.1V nominal
  - V_{DDQ} = 1.06–1.17V; 1.10V nominal
    or Low V_{DDQ} = 0.57–0.65V; 0.60V nominal
- Frequency range
  - 2133–10 MHz (data rate range: 4266–20 Mb/s/pin)
- 16*n* prefetch DDR architecture
- 8 internal banks per channel for concurrent operation

Figure 1: MCP Block Diagram



Mobile LPDDR4/LPDDR4X-Specific Features (Continued)

- Single-data-rate CMD/ADR entry
- Bidirectional/differential data strobe per byte lane
- Programmable and on-the-fly burst lengths (BL = 16, 32)
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Programmable V_{SS} (ODT) termination

Table 1: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	WRITE Latency		READ Latency	
			Set A	Set B	DBI Disabled	DBI Enabled
-046	2133	4266	18	34	36	40

Table 2: Configuration Addressing

Architecture	16Gb single-channel die
Die configuration	128 Meg x 16 x 8 banks x1 channels
Memory density (per die)	16Gb
Memory density (per channel)	16Gb
Row addressing	32K (A[16:0])
Column addressing	1K (A[9:0])
Number of die	1
Die per rank	1
Ranks per channel[1]	1

Note: 1. A channel is a complete LPDRAM interface, including command/address and data pins.

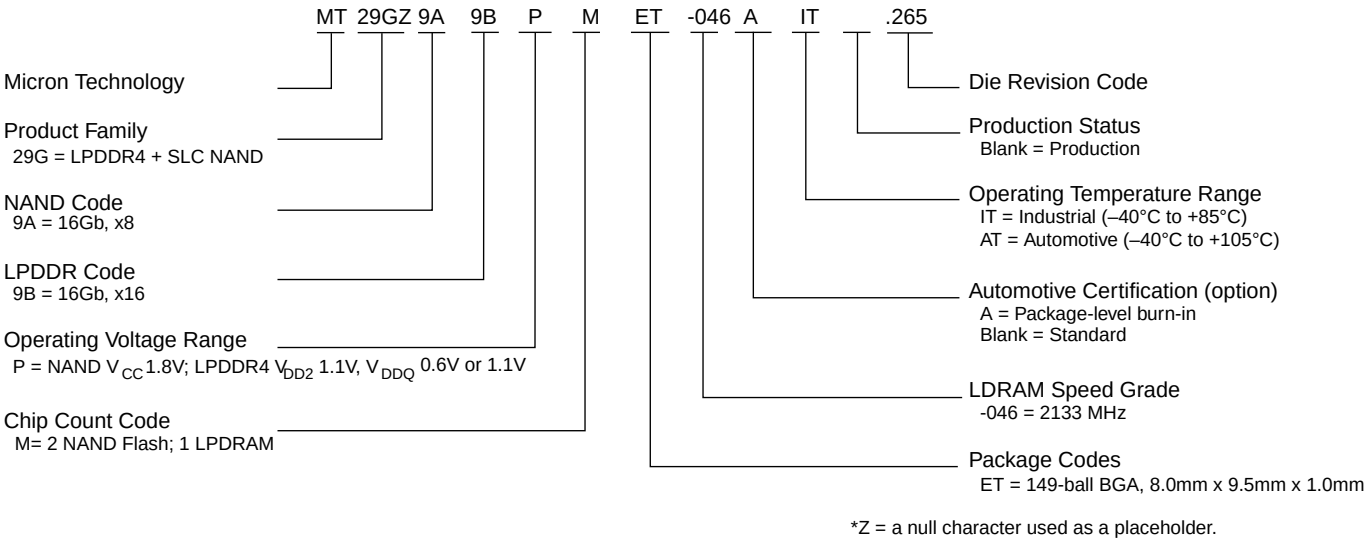
Table 3: Part Number References

MCP	NAND Discrete	NAND READ ID Parameter
MT29GZ9A9BPMET-046AIT.265, MT29GZ9A9BPMET-046AAT.265	MT29F8G08	MT29F8G08ADBFA 8Gb, x8, 1.8V

Part Numbering Information

Micron NAND Flash and LPDRAM devices are available in different configurations and densities. The MCP/PoP part numbering guide is available at www.micron.com/numbering.

Figure 2: Part Number Chart



*Z = a null character used as a placeholder.

Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: www.micron.com/decoder. To view the location of the abbreviated mark on the device, refer to customer service note CSN-11, "Product Mark/Label," at www.micron.com/csn.

Contents

List of Figures

List of Tables

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MCP General Description

Micron MCP products combine NAND Flash and Mobile LPDRAM devices in a single MCP. These products target mobile applications with low-power, high-performance, and minimal package-footprint design requirements. The NAND Flash and Mobile LPDRAM devices are also members of the Micron discrete memory products portfolio.

The NAND Flash and Mobile LPDRAM devices are packaged with separate interfaces (no shared address, control, data, or power balls). This bus architecture supports an optimized interface to processors with separate NAND Flash and Mobile LPDRAM buses. The NAND Flash and Mobile LPDRAM devices have separate core power connections and share a common ground (that is, V_{SS} is tied together on the two devices).

The bus architecture of this device also supports separate NAND Flash and Mobile LPDRAM functionality without concern for device interaction.

Ball Assignments and Descriptions

Figure 3: 149-Ball FBGA (x16 LPDDR) Ball Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	DNU	DNU											DNU	DNU
B	DNU	NC	NC	NC	NC	NC	NC			NC	NC	VCC	NC	DNU
C	NC	NC	NC	WP#	R/B#	VSSm	WE#			VSSm	IO7	IO6	VCC	NC
D	NC	NC	NC	NC	CE#	VSSm	RE#			ALE	VSSm	VSSm	IO1	IO4
E					VDD2	VDD2	VDD2			VSSm	IO2	IO5	VCC	VCC
F	DQ10	VDD2	DQ8	DQ9	VSS	VSS	DQS1_t			CLE	VSSm	VSSm	IO3	IO0
G	DQ11	VDDQ	VDDQ	VSS	DQ12	VDDQ	DQS1_c				ODT_ca	NC	NC	NC
H	DMI1	VSS	VDDQ	DQ14	VSS	DQ15	VDDQ				VSS	NC	VSS	CLK_t
J	DQ13	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0	VSS	CLK_c
K											CA1	VSS	CS1	CKE1
L											CA4	VSS	CS0	CKE0
M	DQ3	VSS	DMI0	VSS	DQ6	VSS	DQS0_c				CA3	VSS	VSS	RESET_
N	DQ2	VSS	VSS	DQ5	VSS	DQ7	DQS0_t				CA2	VSS	CA5	RFU
P	DQ1	DQ0	VDDQ	VSS	DQ4	VSS	VDD2				VDD2	VDD2	VDD1	ZQ0
R	DNU	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	DNU
T	DNU	DNU											DNU	DNU

Top View (ball down)

NAND | DDR4_A (Channel A) | ZQ, ODT_CA, RESET | Supply | Ground

Table 4: x8 NAND Ball Descriptions

Symbol	Type	Description
ALE	Input	**Address latch enable:** When ALE is HIGH, addresses can be transferred to the on-chip address register.
CE#	Input	**Chip enable:** Gates transfers between the host system and the NAND device.
CLE	Input	**Command latch enable:** When CLE is HIGH, commands can be transferred to the on-chip command register.
RE#	Input	**Read enable:** Gates information from the NAND device to the host system.
WE#	Input	**Write enable:** Gates information from the host system to the NAND device.
WP#	Input	**Write protect:** Driving WP# LOW blocks ERASE and PROGRAM operations.
I/O[7:0] (x8)	Input/ output	**Data inputs/outputs:** The bidirectional I/Os transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/Os are inputs. for NAND x8 devices.
R/B#	Output	**Ready/busy:** Open-drain, active-LOW output that indicates when an internal operation is in progress.
V_{CC}	Supply	**V_{CC}:** NAND power supply.

Note: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

Table 5: x16 LPDDR Ball Descriptions

Symbol	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock. Each channel (A, B, C, and D) has its own clock pair.
CKE0, CKE1	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK.
CS0, CS1	Input	**Chip select:** Each channel (A, B, C, and D) has its own CS signals.
CA[5:0]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table. Each channel (A, B, C, and D) has its own CA signals.
ODT_ca	Input	**CA ODT control:** The ODT_CA pin is ignored by LPDDR4X devices. CA ODT is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to a valid logic level.
DQ0[15:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS0_t, DQS0_c, DQS1_t, DQS1_c	I/O	**Data strobe:** DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B, C, and D) has its own DQS_t and DQS_c strobes.

Table 5: x16 LPDDR Ball Descriptions (Continued)

Symbol	Type	Description
DMI[1:0]	I/O	**Data mask/Data bus inversion:** DMI is a dual use bi-directional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion (DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its own DMI signals.
ZQ0, ZQ1	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin shall be connected to V_{DDQ} through a 240Ω ±1% resistor.
V_{DD1}, V_{DD2}, V_{DDQ}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets all channels of the die.
NC	–	**No connect:** Not internally connected.

Note: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

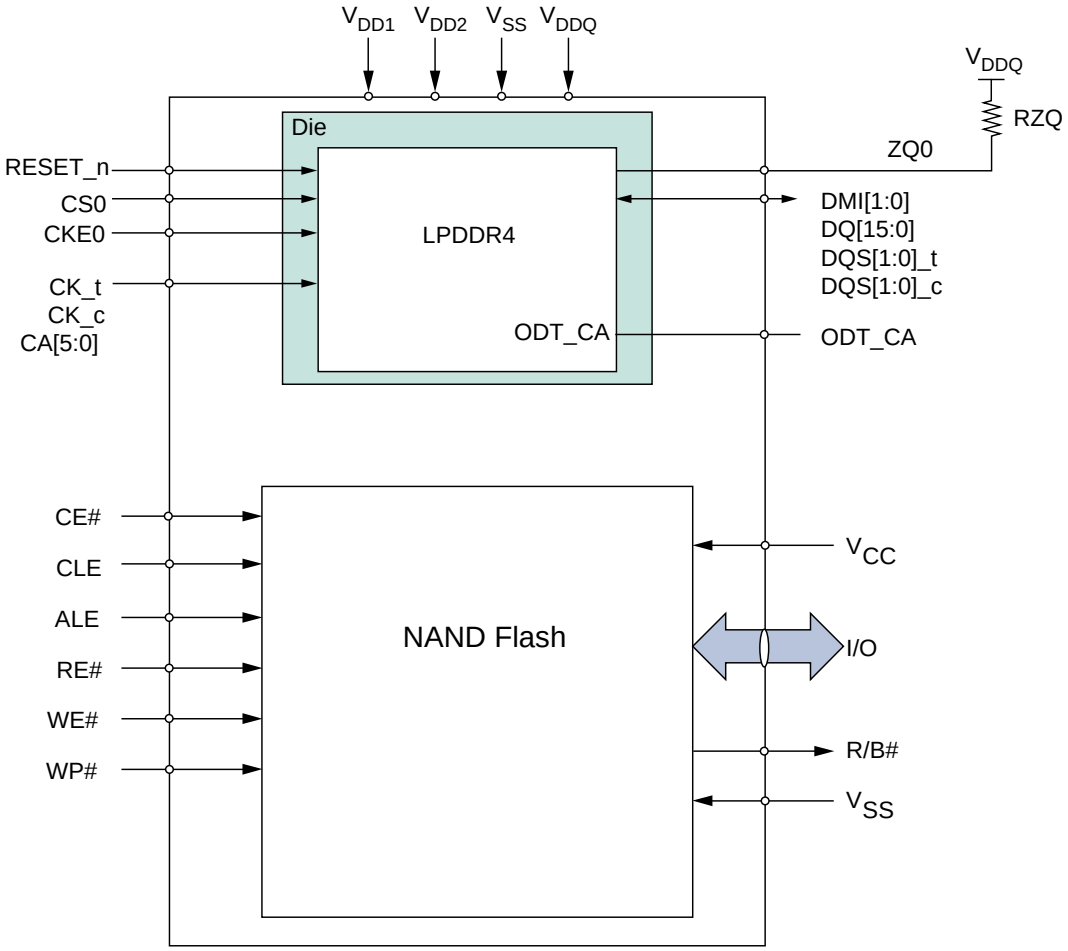
Table 6: Non-Device-Specific Descriptions

Symbol	Type	Description
V_{SS}	Supply	**V_{SS}:** Shared ground.
Symbol	**Type**	**Description**
DNU	–	**Do not use:** Must be grounded or left floating.
NC	–	**No connect:** Not internally connected.
RFU[1]	–	Reserved for future use.

Note: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

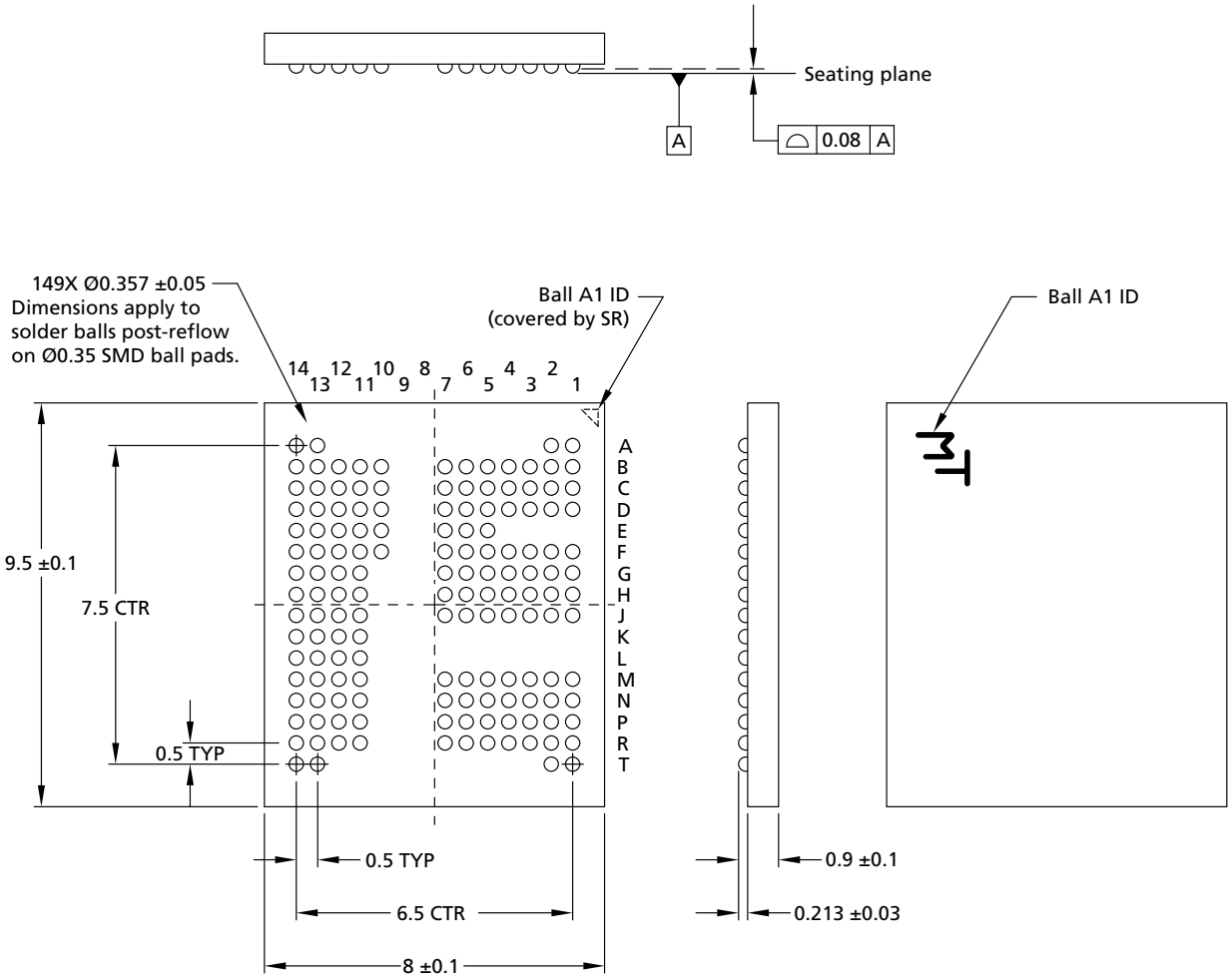
Device Diagrams

Figure 4: 149-Ball Functional Block Diagram



Package Dimensions

Figure 5: 149-Ball WFBGA



Notes: 1. All dimensions are in millimeters.
2. Package height does not include room temperature warpage.

8Gb,16Gb: x8, x16 NAND Flash Memory

- Open NAND Flash Interface (ONFI) 1.0-compliant[1]
- Single-level cell (SLC) technology
- Organization
  - Page size x8: 4320 bytes (4096 + 224 bytes)
  - Page size x16: 2160 words (2048 + 112 words)
  - Block size: 64 pages (256K + 14K bytes)
  - Plane size: 2 planes x 2048 blocks per plane
  - Device size: 8Gb: 4096 blocks
  - Device size: 16Gb: 8192 blocks
- Asynchronous I/O performance
  - ^{t}RC/^{t}WC: 20ns (3.3V), 30ns (1.8V)
- Array performance
  - Read page: 25µs
  - Program page: 200µs (TYP)
  - Erase block: 2ms (TYP)
- Command set: ONFI NAND Flash Protocol
- Advanced command set
  - Program page cache mode
  - Read page cache mode
  - One-time programmable (OTP) mode
  - Block lock (1.8V only)
  - Programmable drive strength
  - Two-plane commands
  - Multi-die (LUN) operations
  - Read unique ID
  - Internal data move
- Operation status byte provides software method for detecting
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Ready/Busy# (R/B#) signal provides a hardware method of detecting operation completion
- WP# signal: Write protect entire device
- First block (block address 00h) is valid when shipped from factory with ECC. For minimum required ECC, see Error Management.
- RESET (FFh) required as first command after power-on
- Alternate method of device initialization after power-up (contact factory)
- Internal data move operations supported within the plane from which data is read
- Quality and reliability
  - Data retention: JESD47G-compliant; see qualification report
  - Endurance: 100,000 PROGRAM/ERASE cycles
- Operating voltage range
  - V_{CC}: 2.7–3.6V
  - V_{CC}: 1.7–1.95V
- Operating temperature
  - Commercial: 0°C to +70°C
  - Extended (ET): –40°C to +85°C

Note: 1. The ONFI 1.0 specification is available at www.onfi.org.

General Description

Micron NAND Flash devices include an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (I/Ox) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection and monitor device status (R/B#).

This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign.

A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). There is at least one NAND Flash die per chip enable signal. For further details, see Device and Array Organization.

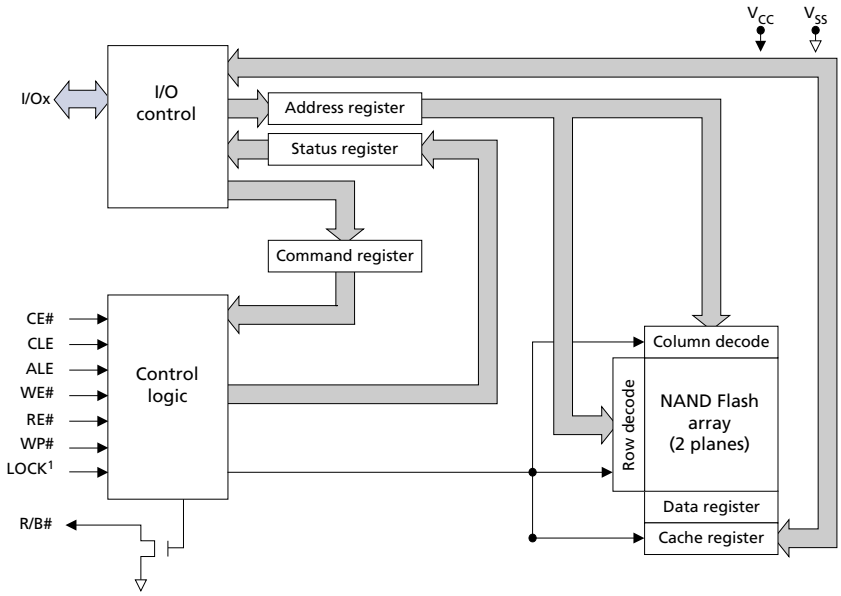
Architecture

These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder to select a row address, or to a column decoder to select a column address.

Data is transferred to or from the NAND Flash memory array, byte by byte (x8) or word by word (x16), through a data register and a cache register.

The NAND Flash memory array is programmed and read using page-based operations and is erased using block-based operations. During normal page operations, the data and cache registers act as a single register. During cache operations, the data and cache registers operate independently to increase data throughput. The status register reports the status of die operations.

Figure 6: NAND Flash Die (LUN) Functional Block Diagram



Note: 1. The LOCK pin is used on the 1.8V device.

Device and Array Organization

Figure 7: Array Organization – 8Gb x 8

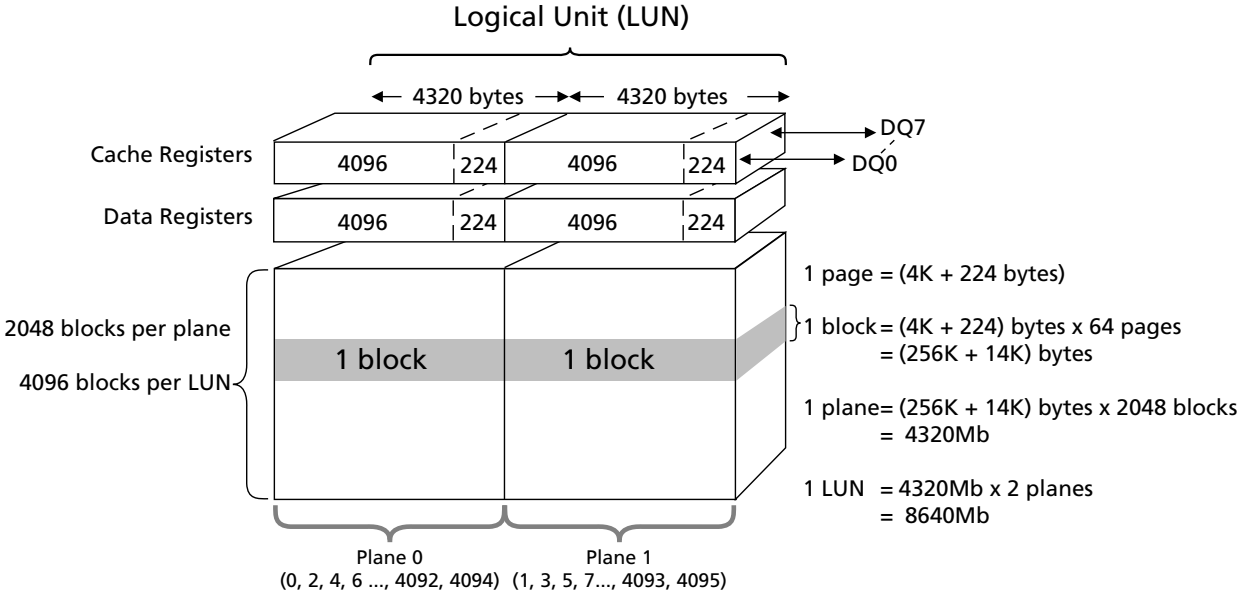


Table 7: Array Addressing (8Gb x 8)

Cycle	I/07	I/06	I/05	I/04	I/03	I/02	I/01	I/00
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	CA12	CA11	CA10	CA9	CA8
Third	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	BA17	BA16

Notes: 1. Block address concatenated with page address = actual page address. CAx = column address; PAx = page address; BAx = block address.
2. If CA12 is 1, then CA[11:8] must be 0.
3. BA6 controls plane selection.

Figure 8: Array Organization – 8Gb x 16

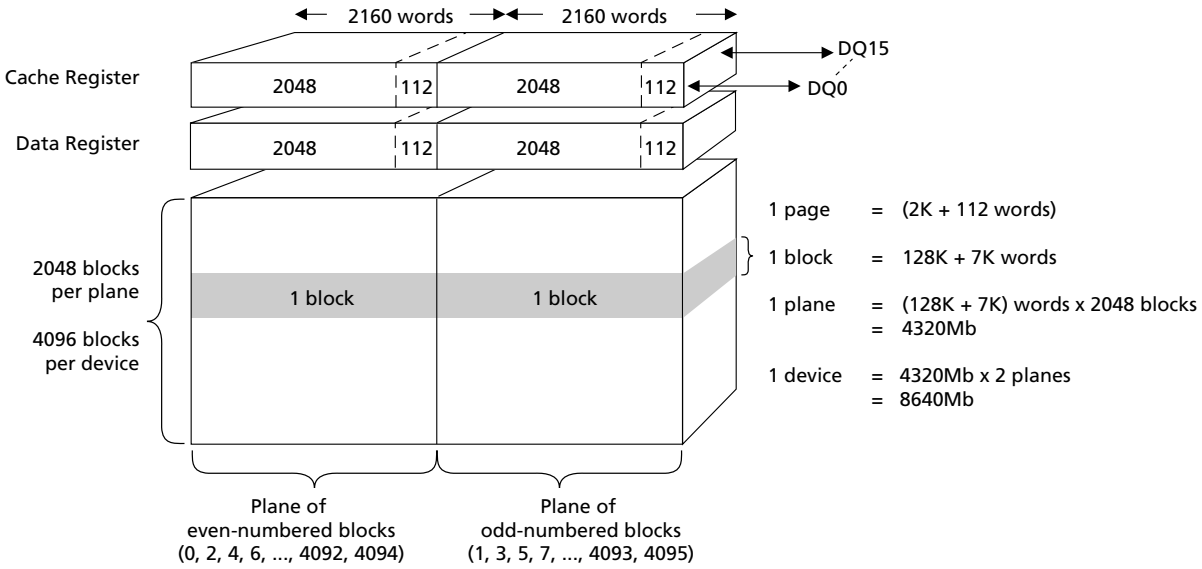


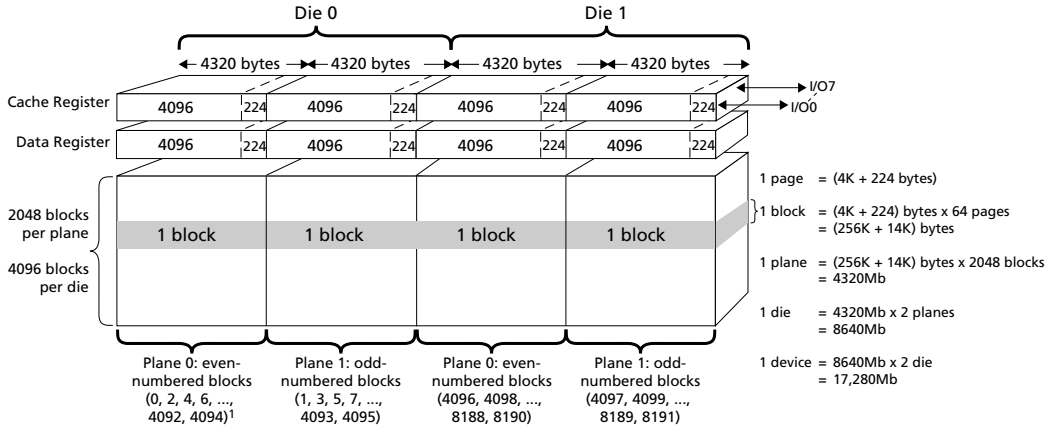
Table 8: Array Addressing (8Gb x 16)

Cycle	I/O[15:8]	I/07	I/06	I/05	I/04	I/03	I/02	I/01	I/00
First	LOW	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	LOW	CA11	CA10	CA9	CA8
Third	LOW	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	LOW	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	BA17	BA16

Notes: 1. Block address concatenated with page address = actual page address. CAx = column address; PAx = page address; BAx = block address.
2. If CA11 = 1, then CA[10:7] must be 0.
3. BA6 controls plane selection.

Bare Die Array Organization

Figure 9: Array Organization – 16Gb x 8, Dual-Die, Single-CE# Bare Die Configuration



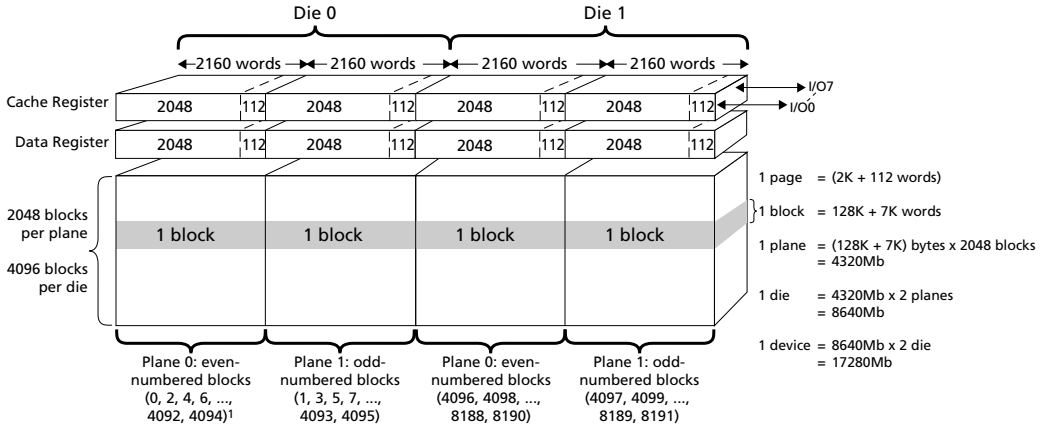
Note: 1. Die 0, Plane 0: BA18 = 0; BA6 = 0. Die 0, Plane 1: BA18 = 0; BA6 = 1.
Die 1, Plane 0: BA18 = 1; BA6 = 0. Die 1, Plane 1: BA18 = 1; BA6 = 1.

Table 9: Array Addressing (16Gb x 8, Dual-Die, Single-CE# Bare Die Configuration)

Cycle	I/07	I/06	I/05	I/04	I/03	I/02	I/01	I/00
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	CA12	CA11	CA10	CA9	CA8
Third	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	BA18	BA17	BA16

Notes: 1. CAx = column address; PAx = page address; BAx = block address.
2. If CA11 is 1, then CA[10:7] must be 0.
3. Die address boundary: 0 = 0–8Gb; 1 = 8Gb–16Gb.

Figure 10: Array Organization – 16Gb x 16, Dual-Die, Single-CE# Bare Die Configuration



Note: 1. Die 0, Plane 0: BA18 = 0; BA6 = 0. Die 0, Plane 1: BA18 = 0; BA6 = 1.
Die 1, Plane 0: BA18 = 1; BA6 = 0. Die 1, Plane 1: BA18 = 1; BA6 = 1.

Table 10: Array Addressing (16Gb x 16, Dual-Die, Single-CE# Bare Die Configuration)

Cycle	I/O[15:8]	I/07	I/06	I/05	I/04	I/03	I/02	I/01	I/O0
First	LOW	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	LOW	CA11	CA10	CA9	CA8
Third	LOW	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	LOW	BA15	BA14	BA13	BA12	BA11	BA10	BA9	PA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	BA18	BA17	BA16

Notes: 1. Block address concatenated with page address = actual page address. CAx = column address; PAx = page address; BAx = block address.
2. If CA11 = 1, then CA[10:7] must be 0.
3. Die address boundary: 0 = 0–8Gb; 1 = 8Gb–16Gb.

Asynchronous Interface Bus Operation

The bus on the device is multiplexed. Data I/O, addresses, and commands all share the same pins. I/O[15:8] are used only for data in the x16 configuration. Addresses and commands are always supplied on I/O[7:0].

The command sequence typically consists of a COMMAND LATCH cycle, address input cycles, and one or more data cycles, either READ or WRITE.

Table 11: Asynchronous Interface Mode Selection

Mode[1]	CE#	CLE	ALE	WE#	RE#	I/Ox	WP#
Standby[2]	H	X	X	X	X	X	0V/V_{CC}
Command input	L	H	L	⎍	H	X	H
Address input	L	L	H	⎍	H	X	H
Data input	L	L	L	⎍	H	X	H
Data output	L	L	L	H	⎎	X	X
Write protect	X	X	X	X	X	X	L

Notes: 1. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.
2. WP# should be biased to CMOS LOW or HIGH for standby.

Asynchronous Enable/Standby

When the device is not performing an operation, the CE# pin is typically driven HIGH and the device enters standby mode. The memory will enter standby if CE# goes HIGH while data is being transferred and the device is not busy. This helps reduce power consumption.

The CE# "Don't Care" operation enables the NAND Flash to reside on the same asynchronous memory bus as other Flash or SRAM devices. Other devices on the memory bus can then be accessed while the NAND Flash is busy with internal operations. This capability is important for designs that require multiple NAND Flash devices on the same bus.

A HIGH CLE signal indicates that a command cycle is taking place. A HIGH ALE signal signifies that an ADDRESS INPUT cycle is occurring.

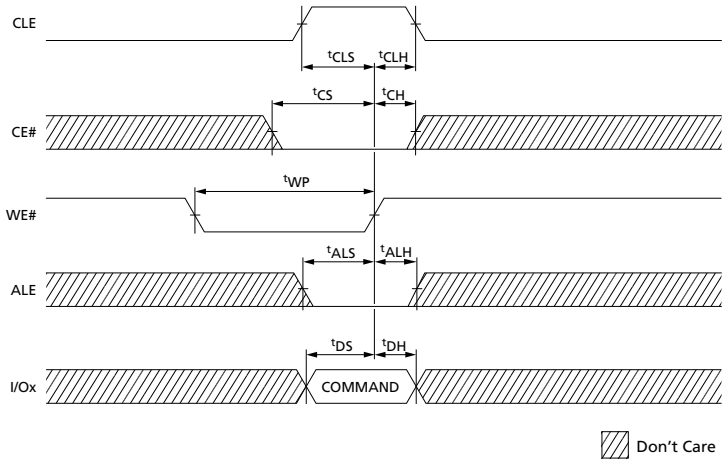
Asynchronous Commands

An asynchronous command is written from I/O[7:0] to the command register on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is HIGH, and RE# is HIGH.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, including READ STATUS (70h) and READ STATUS ENHANCED (78h), are accepted by die (LUNs) even when they are busy.

For devices with a x16 interface, I/O[15:8] must be written with zeros when a command is issued.

Figure 11: Asynchronous Command Latch Cycle



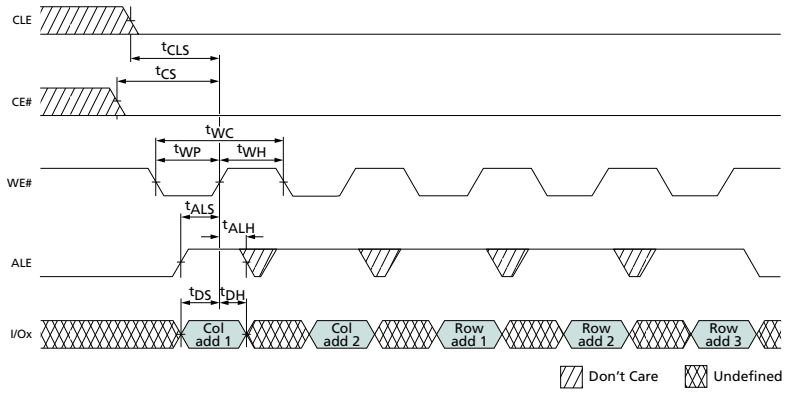
Asynchronous Addresses

An asynchronous address is written from I/O[7:0] to the address register on the rising edge of WE# when CE# is LOW, ALE is HIGH, CLE is LOW, and RE# is HIGH.

Bits that are not part of the address space must be LOW (see Device and Array Organization). The number of cycles required for each command varies. Refer to the command descriptions to determine addressing requirements.

Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses are accepted by die (LUNs) even when they are busy; for example, like address cycles that follow the READ STATUS ENHANCED (78h) command.

Figure 12: Asynchronous Address Latch Cycle



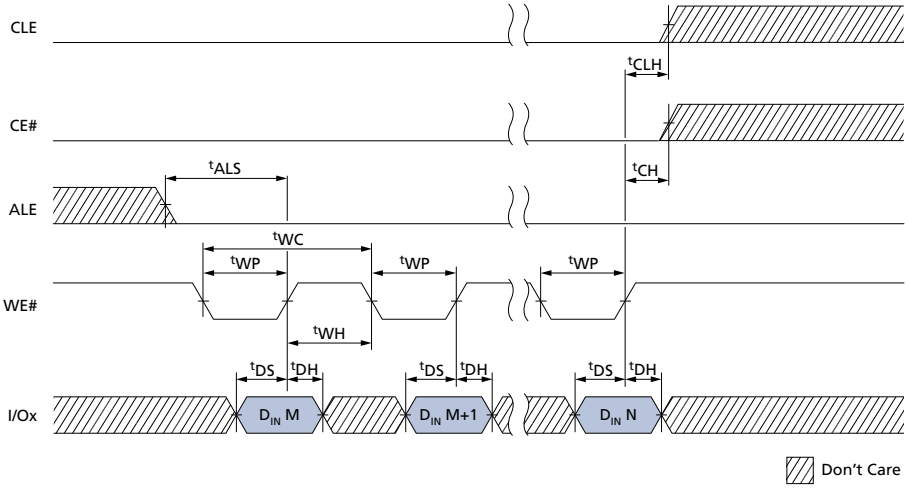
Asynchronous Data Input

Data is written from I/O[7:0] to the cache register of the selected die (LUN) on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is LOW, and RE# is HIGH.

Data input is ignored by die (LUNs) that are not selected or are busy (RDY = 0). Data is written to the data register on the rising edge of WE# when CE#, CLE, and ALE are LOW, and the device is not busy.

Data is input on I/O[7:0] on x8 devices and on I/O[15:0] on x16 devices.

Figure 13: Asynchronous Data Input Cycles



Asynchronous Data Output

Data can be output from a die (LUN) if it is in a READY state. Data output is supported following a READ operation from the NAND Flash array. Data is output from the cache register of the selected die (LUN) to I/O[7:0] on the falling edge of RE# when CE# is LOW, ALE is LOW, CLE is LOW, and WE# is HIGH.

If the host controller is using a ^{t}RC of 30ns or greater, the host can latch the data on the rising edge of RE# (see the figure below for proper timing). If the host controller is using a ^{t}RC of less than 30ns, the host can latch the data on the next falling edge of RE#.

Using the READ STATUS ENHANCED (78h) command prevents data contention following an interleaved die (multi-LUN) operation. After issuing the READ STATUS ENHANCED (78h) command, to enable data output, issue the READ MODE (00h) command.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by first issuing the READ STATUS or READ STATUS ENHANCED (78h) command.

Figure 14: Asynchronous Data Output Cycles

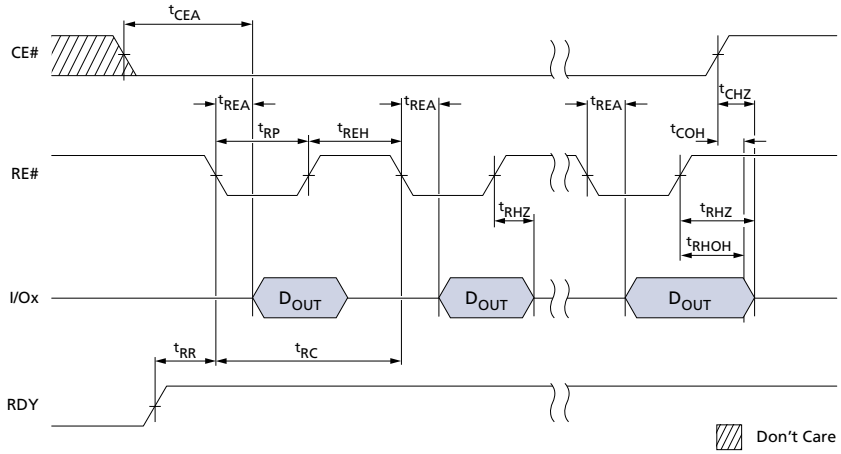
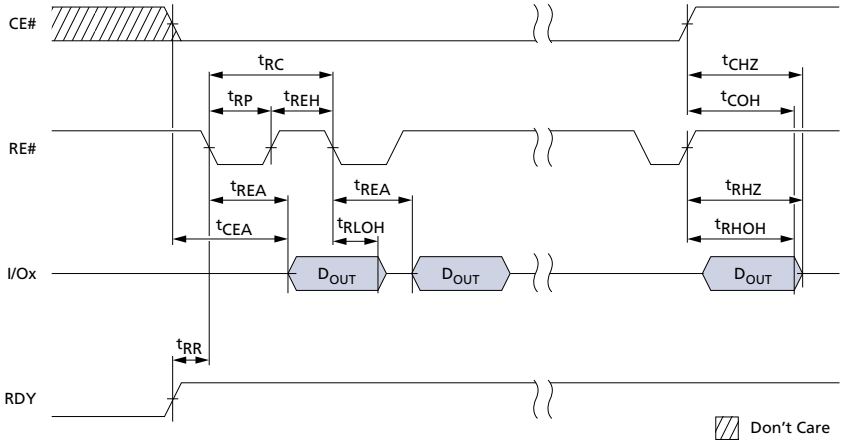


Figure 15: Asynchronous Data Output Cycles (EDO Mode)



Write Protect#

The write protect# (WP#) signal enables or disables PROGRAM and ERASE operations to a target. When WP# is LOW, PROGRAM and ERASE operations are disabled. When WP# is HIGH, PROGRAM and ERASE operations are enabled. When WP# is LOW or toggled LOW during a READ operation, read

will be performed as normal. It is recommended that the host drive WP# LOW during power-on until V_{CC} is stable to prevent inadvertent PROGRAM and ERASE operations (see Device Initialization for additional details).

If WP# is toggled during PROGRAM or ERASE (while RB# is LOW), then the following will occur:

- The PROGRAM or ERASE operation is aborted
- In asynchronous mode, toggling WP# LOW during a NAND PROGRAM or ERASE operation will act like a RESET (FFh) command. In synchronous mode, it will act like a SYNCHRONOUS RESET (FCh) command
- The data that was being programmed or erased (targeted page or block) is not valid anymore
- The status register will be set to 60h until a RESET, new operation, or new power up command is given

After a command sequence is complete and the target is ready, WP# can be transitioned. After WP# is transitioned, the host must wait ^{t}WW before issuing a new command.

The WP# signal is always an active input, even when CE# is HIGH. This signal should not be multiplexed with other signals.

Ready/Busy#

The ready/busy# (R/B#) signal provides a hardware method of indicating whether a target is ready or busy. A target is busy when one or more of its die (LUNs) are busy (RDY = 0). A target is ready when all of its die (LUNs) are ready (RDY = 1). Because each die (LUN) contains a status register, it is possible to determine the independent status of each die (LUN) by polling its status register instead of using the R/B# signal (see Status Operations for details regarding die (LUN) status).

This signal requires a pull-up resistor, Rp, for proper operation. R/B# is HIGH when the target is ready, and transitions LOW when the target is busy. The signal's open-drain driver enables multiple R/B# outputs to be OR-tied. Typically, R/B# is connected to an interrupt pin on the system controller.

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# signal. The actual value used for Rp depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. Between the 10% and 90% points on the R/B# waveform, the rise time is approximately two time constants (TC).

$$T_C = R \times C$$

Where R = Rp (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# signal and the total load capacitance. Approximate Rp values using a circuit load of 100pF are provided in Figure 21: TC vs. Rp on page 38.

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and V_{CC}.

$$Rp = \frac{V_{CC}\,(MAX) - V_{OL}\,(MAX)}{I_{OL} + \Sigma_{IL}}$$

Where Σ_{IL} is the sum of the input currents of all devices tied to the R/B# pin.

Figure 16: READ/BUSY# Open Drain

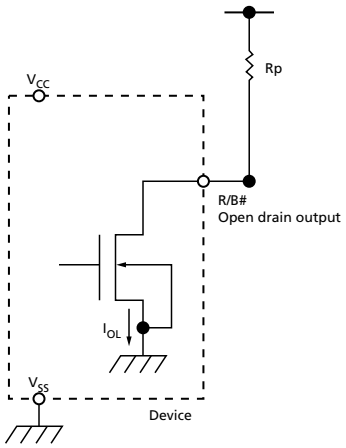
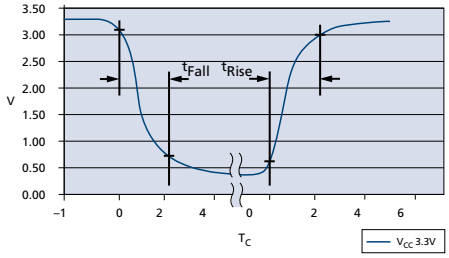
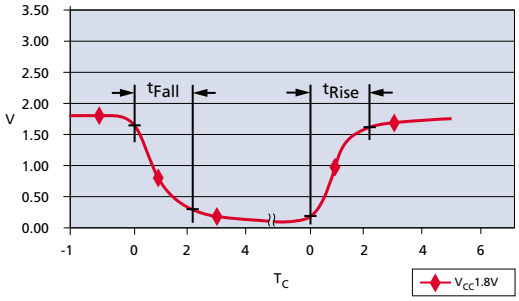


Figure 17: ^{t}Fall and ^{t}Rise (3.3V V_{CC})



Notes: 1. ^{t}Fall and ^{t}Rise calculated at 10% and 90% points.
2. ^{t}Rise dependent on external capacitance and resistive loading and output transistor impedance.
3. ^{t}Rise primarily dependent on external pull-up resistor and external capacitive loading.
4. ^{t}Fall = 10ns at 3.3V.
5. See TC values in Figure 21: TC vs. Rp on page 38 for approximate Rp value and TC.

Figure 18: ^{t}Fall and ^{t}Rise (1.8V V_{CC})



Notes: 1. ^{t}Fall and ^{t}Rise are calculated at 10% and 90% points.
2. ^{t}Rise is primarily dependent on external pull-up resistor and external capacitive loading.
3. ^{t}Fall ≈ 7ns at 1.8V.
4. See TC values in Figure 21: TC vs. Rp on page 38 for TC and approximate Rp value.

Figure 19: I_{OL} vs. Rp (V_{CC} = 3.3V V_{CC})

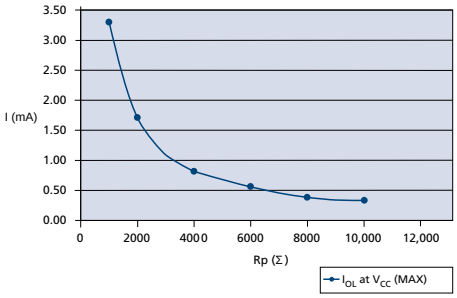


Figure 20: I_{OL} vs. Rp (1.8V V_{CC})

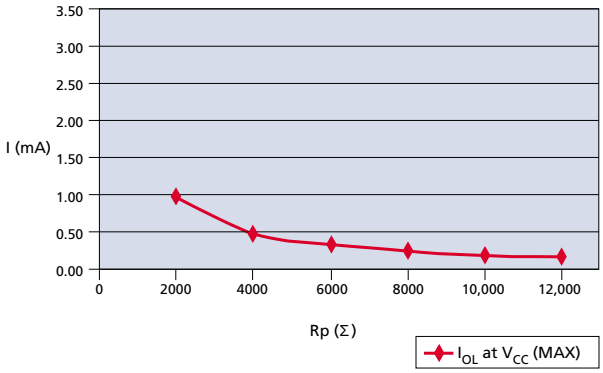
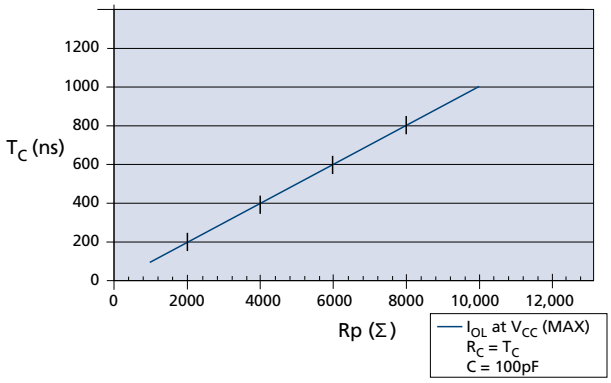


Figure 21: TC vs. Rp

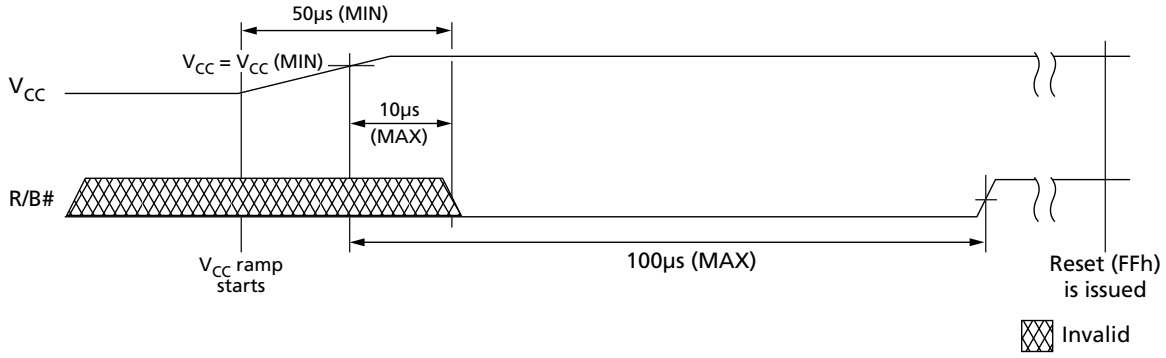


Device Initialization

Micron NAND Flash devices are designed to prevent data corruption during power transitions. V_{CC} is internally monitored. (The WP# signal supports additional hardware protection during power transitions.) When ramping V_{CC}, use the following procedure to initialize the device:

1. Ramp V_{CC}.
2. The host must wait for R/B# to be valid and HIGH before issuing RESET (FFh) to any target. The R/B# signal becomes valid when 50µs has elapsed since the beginning the V_{CC} ramp, and 10µs has elapsed since V_{CC} reaches $V_{CC,min}$.
3. If not monitoring R/B#, the host must wait at least 100µs after V_{CC} reaches $V_{CC,min}$. If monitoring R/B#, the host must wait until R/B# is HIGH.
4. The asynchronous interface is active by default for each target. Each LUN draws less than an average of 10mA (I_{ST}) measured over intervals of 1ms until the RESET (FFh) command is issued.
5. The RESET (FFh) command must be the first command issued to all targets (CE#s) after the NAND Flash device is powered on. Each target will be busy for 1ms after a RESET command is issued. The RESET busy time can be monitored by polling R/B# or issuing the READ STATUS (70h) command to poll the status register.
6. The device is now initialized and ready for normal operation.

Figure 22: R/B# Power-On Behavior



Power Cycle Requirements

Upon power-down the NAND device requires a maximum voltage and minimum time that the host must hold V_{CC} and V_{CCQ} below the voltage prior to power-on.

Table 12: Power Cycle Requirements

Parameter	Value	Unit
Maximum V_{CC}/V_{CCQ}	100	mV
Minimum time below maximum voltage	100	ns

Command Definitions

Table 13: Command Set

Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Valid While Selected LUN is Busy[1]	Valid While Other LUNs are Busy[2]	Notes
Reset Operations							
RESET	FFh	0	–	–	Yes	Yes	
Identification Operation							
READ ID	90h	1	–	–	No	No	
READ PARAMETER PAGE	ECh	1	–	–	No	No	
READ UNIQUE ID	EDh	1	–	–	No	No	
Feature Operations							
GET FEATURES	EEh	1	–	–	No	No	
SET FEATURES	EFh	1	4	–	No	No	
Status Operations							
READ STATUS	70h	0	–	–	Yes		
READ STATUS ENHANCED	78h	3	–	–	Yes	Yes	
Column Address Operations							
RANDOM DATA READ	05h	2	–	E0h	No	Yes	
RANDOM DATA READ TWO-PLANE	06h	5	–	E0h	No	Yes	
RANDOM DATA INPUT	85h	2	Optional	–	No	Yes	
PROGRAM FOR INTERNAL DATA MOVE	85h	5	Optional	–	No	Yes	3
READ OPERATIONS							
READ MODE	00h	0	–	–	No	Yes	
READ PAGE	00h	5	–	30h	No	Yes	
READ PAGE CACHE SEQUENTIAL	31h	0	–	–	No	Yes	4
READ PAGE CACHE RANDOM	00h	5	–	31h	No	Yes	4
READ PAGE CACHE LAST	3Fh	0	–	–	No	Yes	4
Program Operations							
PROGRAM PAGE	80h	5	Yes	10h	No	Yes	
PROGRAM PAGE CACHE	80h	5	Yes	15h	No	Yes	5
Erase Operations							
ERASE BLOCK	60h	3	–	D0h	No	Yes	
Internal Data Move Operations							
READ FOR INTERNAL DATA MOVE	00h	5	–	35h	No	Yes	3
PROGRAM FOR INTERNAL DATA MOVE	85h	5	Optional	10h	No	Yes	

Table 13: Command Set (Continued)

Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Valid While Selected LUN is Busy[1]	Valid While Other LUNs are Busy[2]	Notes
Block Lock Operations							
BLOCK UNLOCK LOW	23h	3	–	–	No	Yes	
BLOCK UNLOCK HIGH	24h	3	–	–	No	Yes	
BLOCK LOCK	2Ah	–	–	–	No	Yes	
BLOCK LOCK TIGHT	2Ch	–	–	–	No	Yes	
BLOCK LOCK READ STATUS	7Ah	3	–	–	No	Yes	
One-Time Programmable (OTP) Operations							
OTP DATA LOCK BY BLOCK (ONFI)	80h	5	No	10h	No	No	6
OTP DATA PROGRAM (ONFI)	80h	5	Yes	10h	No	No	6
OTP DATA READ (ONFI)	00h	5	No	30h	No	No	6

Notes: 1. Busy means RDY = 0.
2. These commands can be used for interleaved die (multi-LUN) operations (see Interleaved Die Multi-LUN Operations).
3. Do not cross plane address boundaries when using READ for INTERNAL DATA MOVE and PROGRAM for INTERNAL DATA MOVE.
4. Issuing a READ PAGE CACHE series (31h, 00h-31h, 00h-32h, 3Fh) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a READ PAGE (00h-30h) or READ PAGE CACHE series command; otherwise, it is prohibited.
5. Issuing a PROGRAM PAGE CACHE (80h-15h) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a PROGRAM PAGE CACHE (80h-15h) command; otherwise, it is prohibited.
6. OTP commands can be entered only after issuing the SET FEATURES command with the feature address.

Table 14: Two-Plane Command Set

Command	Command Cycle #1	Number of Valid Address Cycles	Command Cycle #2	Number of Valid Address Cycles	Command Cycle #3	Valid While Selected LUN is Busy	Valid While Other LUNs are Busy	Notes
READ PAGE TWO-PLANE	00h	5	00h	5	30h	No	Yes	
READ FOR TWO-PLANE INTERNAL DATA MOVE	00h	5	00h	5	35h	No	Yes	1
RANDOM DATA READ TWO-PLANE	06h	5	E0h	–	–	No	Yes	2
PROGRAM PAGE TWO-PLANE	80h	5	11h-80h	5	10h	No	Yes	
PROGRAM PAGE CACHE MODE TWO-PLANE	80h	5	11h-80h	5	15h	No	Yes	

Table 14: Two-Plane Command Set (Continued)

Command	Command Cycle #1	Number of Valid Address Cycles	Command Cycle #2	Number of Valid Address Cycles	Command Cycle #3	Valid While Selected LUN is Busy	Valid While Other LUNs are Busy	Notes
PROGRAM FOR TWO-PLANE INTERNAL DATA MOVE	85h	5	11h-85h	5	10h	No	Yes	1
BLOCK ERASE TWO-PLANE	60h	3	D1h-60h	–	D0h	No	Yes	3

Notes: 1. Do not cross plane boundaries when using READ FOR INTERNAL DATA MOVE TWO-PLANE or PROGRAM FOR TWO-PLANE INTERNAL DATA MOVE.
2. The RANDOM DATA READ TWO-PLANE command is limited to use with the PAGE READ TWO-PLANE command.
3. D1h command can be omitted.

Reset Operations

RESET (FFh)

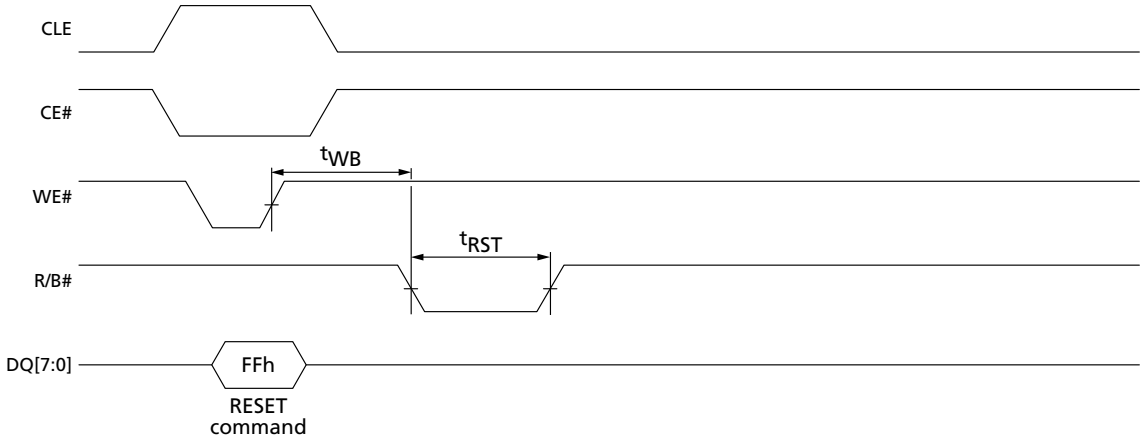
The RESET command is used to put the memory device into a known condition and to abort the command sequence in progress.

READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. The contents of the memory location being programmed or the block being erased are no longer valid. The data may be partially erased or programmed, and is invalid. The command register is cleared and is ready for the next command. The data register and cache register contents are marked invalid.

The status register contains the value E0h when WP# is HIGH; otherwise, it is written with a 60h value. R/B# goes LOW for ^{t}RST after the RESET command is written to the command register.

The RESET command must be issued to all CE#s as the first command after power-on. The device will be busy for a maximum of 1ms.

Figure 23: RESET (FFh) Operation



Identification Operations

READ ID (90h)

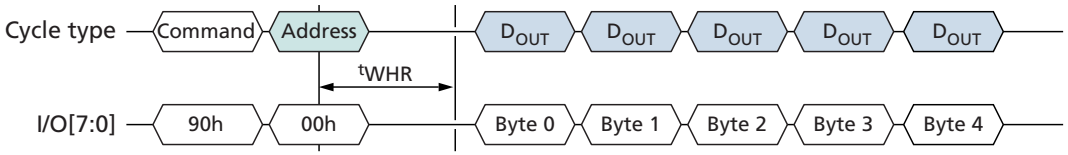
The READ ID (90h) command is used to read identifier codes programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing 90h to the command register puts the target in read ID mode. The target stays in this mode until another valid command is issued.

When the 90h command is followed by an 00h address cycle, the target returns a 5-byte identifier code that includes the manufacturer ID, device configuration, and part-specific information.

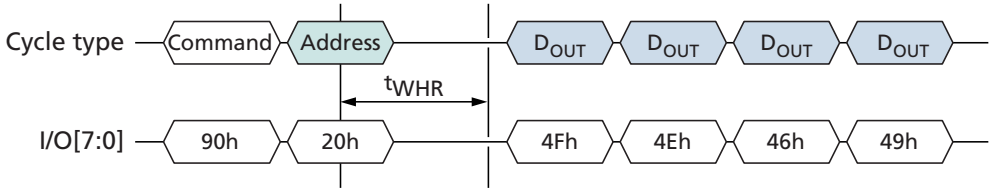
When the 90h command is followed by a 20h address cycle, the target returns the 4-byte ONFI identifier code.

Figure 24: READ ID (90h) with 00h Address Operation



Note: 1. See READ ID Parameter tables for byte definitions.

Figure 25: READ ID (90h) with 20h Address Operation



Note: 1. See READ ID Parameter tables for byte definitions.

READ ID Parameter Tables

Table 15: READ ID Parameters for Address 00h

b = binary; h = hexadecimal

		Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value
Byte 0 – Manufacturer ID											
Manufacturer		Micron	0	0	1	0	1	1	0	0	2Ch
Byte 1 – Device ID											
MT29F8G08ABBCA		8Gb, x8, 1.8V	1	0	1	0	0	0	1	1	A3h
MT29F8G16ABBCA		8Gb, x16, 1.8V	1	0	1	1	0	0	1	1	B3h
MT29F8G08ABACA		8Gb, x8, 3.3V	1	1	0	1	0	0	1	1	D3h
MT29F8G16ABACA		8Gb, x16, 3.3V	1	1	0	0	0	0	1	1	C3h
MT29F16G08ADACA		16Gb, x8, 3.3V	1	1	0	1	0	1	0	1	D5h
MT29F16G16ADACA		16Gb, x16, 3.3V	1	1	0	0	0	1	0	1	C5h
MT29F16G08ADBCA		16Gb, x8, 1.8V	1	0	1	0	0	1	0	1	A5h
MT29F16G16ADBCA		16Gb, x16, 1.8V	1	0	1	1	0	1	0	1	B5h
Byte 2											
Number of die per CE		1							0	0	00b
Number of die per CE		2							0	1	01b
Cell type		SLC					0	0			00b
Number of simultaneously programmed pages		2			0	1					01b
Interleaved operations between multiple die		Supported		1							1b
		Not supported		0							0b
Cache programming		Supported	1								1b
Byte value		MT29F8G	1	0	0	1	0	0	0	0	90h
		MT29F16G	1	1	0	1	0	0	0	1	D1h
Byte 3											
Page size		4KB							1	0	10b
Spare area size (bytes)		224B						1			1b
Block size (w/o spare)		256KB			1	0					10b
Organization		x8		0							0b
		x16		1							
Serial access (MIN)	1.8V	30ns	0				0				0xxx0b
	3.3V	20ns	1				0				1xxx0b
Byte value		MT29F8G08ABBCA	0	0	1	0	0	1	1	0	26h
		MT29F8G16ABBCA	0	1	1	0	0	1	1	0	66h
		MT29F8G08ABACA	1	0	1	0	0	1	1	0	A6h
		MT29F8G16ABACA	1	1	1	0	0	1	1	0	E6h
		MT29F16G08ADACA	1	0	1	0	0	1	1	0	A6h
		MT29F16G16ADACA	1	1	1	0	0	1	1	0	E6h
		MT29F16G08ADBCA	0	0	1	0	0	1	1	0	26h
		MT29F16G16ADBCA	0	1	1	0	0	1	1	0	66h

Table 15: READ ID Parameters for Address 00h (Continued)

	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value
Byte 4										
Reserved								0	0	00b
Planes per CE#	2					0	1			01b
	4					1	0			10b
Plane size	4Gb		1	1	0					110b
Reserved		0								0b
Byte value	MT29F8G	0	1	1	0	0	1	0	0	64h
	MT29F16G	0	1	1	0	1	0	0	0	68h

Table 16: READ ID Parameters for Address 20h

h = hexadecimal

Byte	Options	I/07	I/06	I/05	I/04	I/03	I/02	I/01	I/00	Value
0	“O”	0	1	0	0	1	1	1	1	4Fh
1	“N”	0	1	0	0	1	1	1	0	4Eh
2	“F”	0	1	0	0	0	1	1	0	46h
3	“I”	0	1	0	0	1	0	0	1	49h
4	Undefined	X	X	X	X	X	X	X	X	XXh

READ PARAMETER PAGE (ECh)

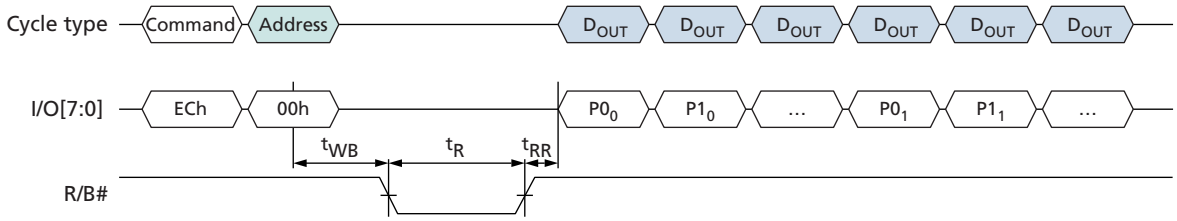
The READ PARAMETER PAGE (ECh) command is used to read the ONFI parameter page programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing ECh to the command register puts the target in read parameter page mode. The target stays in this mode until another valid command is issued.

When the ECh command is followed by an 00h address cycle, the target goes busy for ^{t}R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. Use of the READ STATUS ENHANCED (78h) command is prohibited while the target is busy and during data output.

A minimum of three copies of the parameter page are stored in the device. Each parameter page is 256 bytes. If desired, the RANDOM DATA READ (05h-E0h) command can be used to change the location of data output.

Figure 26: READ PARAMETER (ECh) Operation



Parameter Page Data Structure Tables

Table 17: Parameter Page Data Structure

Byte	Description		Value
0–3	Parameter page signature		4Fh, 4Eh, 46h, 49h
4–5	Revision number		02h, 00h
6–7	Features supported	MT29F8G08ABBCA3W	18h, 00h
		MT29F8G16ABBCA3W	19h, 00h
		MT29F8G08ABACA3W	18h, 00h
		MT29F8G16ABACA3W	19h, 00h
		MT29F8G08ABBCAH4	18h, 00h
		MT29F8G16ABBCAH4	19h, 00h
		MT29F16G08ADBCAH4	1Ah, 00h
		MT29F16G16ADBCAH4	1Bh, 00h
		MT29F8G08ABACAWP	18h, 00h
		MT29F8G16ABACAWP	19h, 00h
		MT29F8G08ABACAH4	18h, 00h
		MT29F8G16ABACAH4	19h, 00h
		MT29F16G08ADACAH4	1Ah, 00h
		MT29F16G16ADACAH4	1Bh, 00h
8–9	Optional commands supported		3Fh, 00h
10–31	Reserved		00h
32–43	Device manufacturer		4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h

Table 17: Parameter Page Data Structure (Continued)

Byte	Description		Value
44–63	Device model	MT29F8G08ABBCA3W	4Dh, 54h, 32h, 39h, 46h, 38h, 47h, 30h, 38h, 41h, 42h, 42h, 43h, 41h, 33h, 57h, 20h, 20h, 20h, 20h
		MT29F8G16ABBCA3W	4Dh, 54h, 32h, 39h, 46h, 38h, 47h, 31h, 36h, 41h, 42h, 42h, 43h, 41h, 33h, 57h, 20h, 20h, 20h, 20h
		MT29F8G08ABACA3W	4Dh, 54h, 32h, 39h, 46h, 38h, 47h, 30h, 38h, 41h, 42h, 41h, 43h, 41h, 33h, 57h, 20h, 20h, 20h, 20h
		MT29F8G16ABACA3W	4Dh, 54h, 32h, 39h, 46h, 38h, 47h, 31h, 36h, 41h, 42h, 41h, 43h, 41h, 33h, 57h, 20h, 20h, 20h, 20h
		MT29F8G08ABBCAH4	4Dh, 54h, 32h, 39h, 46h, 38h, 47h, 30h, 38h, 41h, 42h, 42h, 43h, 41h, 48h, 34h, 20h, 20h, 20h, 20h
		MT29F8G16ABBCAH4	4Dh, 54h, 32h, 39h, 46h, 38h, 47h, 31h, 36h, 41h, 42h, 42h, 43h, 41h, 48h, 34h, 20h, 20h, 20h, 20h
		MT29F16G08ADBCAH4	4Dh, 54h, 32h, 39h, 46h, 31h, 36h, 47h, 30h, 38h, 41h, 44h, 42h, 43h, 41h, 48h, 34h, 20h, 20h, 20h
		MT29F16G16ADBCAH4	4Dh, 54h, 32h, 39h, 46h, 31h, 36h, 47h, 31h, 36h, 41h, 44h, 42h, 43h, 41h, 48h, 34h, 20h, 20h, 20h
		MT29F8G08ABACAWP	4Dh, 54h, 32h, 39h, 46h, 38h, 47h, 30h, 38h, 41h, 42h, 41h, 43h, 41h, 57h, 50h, 20h, 20h, 20h, 20h
		MT29F8G16ABACAWP	4Dh, 54h, 32h, 39h, 46h, 38h, 47h, 31h, 36h, 41h, 42h, 41h, 43h, 41h, 57h, 50h, 20h, 20h, 20h, 20 h
		MT29F8G08ABACAH4	4Dh, 54h, 32h, 39h, 46h, 38h, 47h, 30h, 38h, 41h, 42h, 41h, 43h, 41h, 48h, 34h, 20h, 20h, 20h, 20h
		MT29F8G16ABACAH4	4Dh, 54h, 32h, 39h, 46h, 38h, 47h, 31h, 36h, 41h, 42h, 41h, 43h, 41h, 48h, 34h, 20h, 20h, 20h, 20h
		MT29F16G08ADACAH4	4Dh, 54h, 32h, 39h, 46h, 31h, 36h, 47h, 30h, 38h, 41h, 44h, 41h, 43h, 41h, 48h, 34h, 20h, 20h, 20h
		MT29F16G16ADACAH4	4Dh, 54h, 32h, 39h, 46h, 31h, 36h, 47h, 31h, 36h, 41h, 44h, 41h, 43h, 41h, 48h, 34h, 20h, 20, 20h
64	Manufacturer ID		2Ch
65–66	Date code		00h
67–79	Reserved		00h
80–83	Number of data bytes per page		00h, 10h, 00h, 00h
84–85	Number of spare bytes per page		E0h, 00h
86–89	Number of data bytes per partial page		00h, 04h, 00h, 00h
90–91	Number of spare bytes per partial page		38h, 00h
92–95	Number of pages per block		40h, 00h, 00h, 00h
96–99	Number of blocks per unit		00h, 10h, 00h, 00h

Table 17: Parameter Page Data Structure (Continued)

Byte	Description		Value
100	Number of logical units	MT29F8G08ABBCA3W	01h
		MT29F8G16ABBCA3W	01h
		MT29F8G08ABACA3W	01h
		MT29F8G16ABACA3W	01h
		MT29F8G08ABBCAH4	01h
		MT29F8G16ABBCAH4	01h
		MT29F16G08ADBCAH4	02h
		MT29F16G16ADBCAH4	02h
		MT29F8G08ABACAWP	01h
		MT29F8G16ABACAWP	01h
		MT29F8G08ABACAH4	01h
		MT29F8G16ABACAH4	01h
		MT29F16G08ADACAH4	02h
		MT29F16G16ADACAH4	02h
101	Number of address cycles		23h
102	Number of bits per cell		01h
103–104	Bad blocks maximum per unit		50h, 00h
105–106	Block endurance		06h, 04h
107	Guaranteed valid blocks at beginning of target		01h
108–109	Block endurance for guaranteed valid blocks		00h, 00h
110	Number of programs per page		04h
111	Partial programming attributes		00h
112	Number of bits ECC bits		08h
113	Number of interleaved address bits		01h
114	Interleaved operation attributes		0Eh
115–127	Reserved		00h

Table 17: Parameter Page Data Structure (Continued)

Byte	Description		Value
128	I/O pin capacitance	MT29F8G08ABBCA3W	0Ah
		MT29F8G16ABBCA3W	0Ah
		MT29F8G08ABACA3W	0Ah
		MT29F8G16ABACA3W	0Ah
		MT29F8G08ABBCAH4	0Ah
		MT29F8G16ABBCAH4	0Ah
		MT29F16G08ADBCAH4	14h
		MT29F16G16ADBCAH4	14h
		MT29F8G08ABACAWP	0Ah
		MT29F8G16ABACAWP	0Ah
		MT29F8G08ABACAH4	0Ah
		MT29F8G16ABACAH4	0Ah
		MT29F16G08ADACAH4	14h
		MT29F16G16ADACAH4	14h
129–130	Timing mode support	MT29F8G08ABBCA3W	0Fh, 00h
		MT29F8G16ABBCA3W	0Fh, 00h
		MT29F8G08ABACA3W	3Fh, 00h
		MT29F8G16ABACA3W	3Fh, 00h
		MT29F8G08ABBCAH4	0Fh, 00h
		MT29F8G16ABBCAH4	0Fh, 00h
		MT29F16G08ADBCAH4	0Fh, 00h
		MT29F16G16ADBCAH4	0Fh, 00h
		MT29F8G08ABACAWP	3Fh, 00h
		MT29F8G16ABACAWP	3Fh, 00h
		MT29F8G08ABACAH4	3Fh, 00h
		MT29F8G16ABACAH4	3Fh, 00h
		MT29F16G08ADACAH4	3Fh, 00h
		MT29F16G16ADACAH4	3Fh, 00h

Table 17: Parameter Page Data Structure (Continued)

Byte	Description		Value
131–132	Program cache timing mode support	MT29F8G08ABBCA3W	0Fh, 00h
		MT29F8G16ABBCA3W	0Fh, 00h
		MT29F8G08ABACA3W	3Fh, 00h
		MT29F8G16ABACA3W	3Fh, 00h
		MT29F8G08ABBCAH4	0Fh, 00h
		MT29F8G16ABBCAH4	0Fh, 00h
		MT29F16G08ADBCAH4	0Fh, 00h
		MT29F16G16ADBCAH4	0Fh, 00h
		MT29F8G08ABACAWP	3Fh, 00h
		MT29F8G16ABACAWP	3Fh, 00h
		MT29F8G08ABACAH4	3Fh, 00h
		MT29F8G16ABACAH4	3Fh, 00h
		MT29F16G08ADACAH4	3Fh, 00h
		MT29F16G16ADACAH4	3Fh, 00h
133–134	^{t}PROG maximum page program time		58h, 02h
135–136	^{t}BERS maximum block erase time		10h, 27h
137–138	^{t}R maximum page read time		19h, 00h
139–140	^{t}CCS minimum		64h, 00h
141–163	Reserved		00h
164–165	Vendor-specific revision number		01h, 00h
166–253	Vendor-specific		01h, 00h, 00h, 02h, 04h, 80h, 01h, 81h, 04h, 01h, 02h, 01h, 0Ah, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
254–255	Integrity CRC		Set at test
256–511	Value of bytes 0–255		
512–767	Value of bytes 0–255		
768+	Additional redundant parameter pages		

READ UNIQUE ID (EDh)

The READ UNIQUE ID (EDh) command is used to read a unique identifier programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EDh to the command register puts the target in read unique ID mode. The target stays in this mode until another valid command is issued.

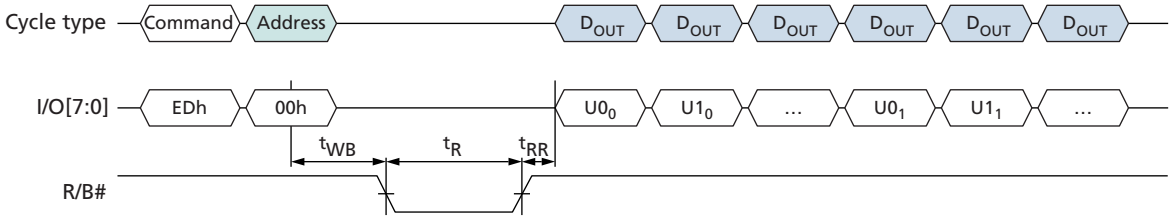
When the EDh command is followed by an 00h address cycle, the target goes busy for ^{t}R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode.

After ^{t}R completes, the host enables data output mode to read the unique ID. When the asynchronous interface is active, one data byte is output per RE# toggle.

Sixteen copies of the unique ID data are stored in the device. Each copy is 32 bytes. The first 16 bytes of a 32-byte copy are unique data, and the second 16 bytes are the complement of the first 16 bytes. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, then that copy of the unique ID data is correct. In the event that a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data. If desired, the RANDOM DATA READ (05h-E0h) command can be used to change the data output location.

The upper eight I/Os on a x16 device are not used and are a “Don’t Care” for x16 devices.

Figure 27: READ UNIQUE ID (EDh) Operation



Feature Operations

The SET FEATURES (EFh) and GET FEATURES (EEh) commands are used to modify the target's default power-on behavior. These commands use a one-byte feature address to determine which subfeature parameters will be read or modified. Each feature address (in the 00h to FFh range) is defined in below. The SET FEATURES (EFh) command writes subfeature parameters (P1–P4) to the specified feature address. The GET FEATURES command reads the subfeature parameters (P1–P4) at the specified feature address.

Table 18: Feature Address Definitions

Feature Address	Definition
00h	Reserved
01h	Timing mode
02h–7Fh	Reserved
80h	Programmable output drive strength
81h	Programmable RB# pull-down strength
82h–FFh	Reserved
90h	Array operation mode

Table 19: Feature Address 90h – Array Operation Mode

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
Operation mode option	Normal	Reserved (0)							0	00h	1
	OTP operation	Reserved (0)							1	01h	1
	OTP protection	Reserved (0)						1	1	03h	
		Reserved (0)								00h	
		Reserved (0)								00h	
P2											
Reserved		Reserved (0)								00h	
P3											
Reserved		Reserved (0)								00h	
P4											
Reserved		Reserved (0)								00h	

Note: 1. These bits are reset to 00h on power cycle.

SET FEATURES (EFh)

The SET FEATURES (EFh) command writes the subfeature parameters (P1–P4) to the specified feature address to enable or disable target-specific features. This command is accepted by the target only when all die (LUNs) on the target are idle.

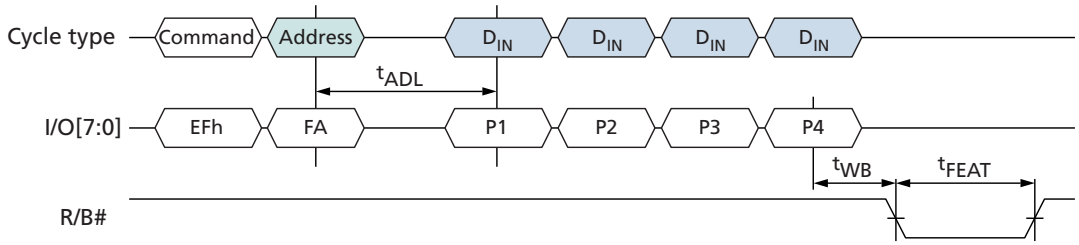
Writing EFh to the command register puts the target in the set features mode. The target stays in this mode until another command is issued.

The EFh command is followed by a valid feature address. The host waits for ^{t}ADL before the subfeature parameters are input. When the asynchronous interface is active, one subfeature parameter is latched per rising edge of WE#.

After all four subfeature parameters are input, the target goes busy for ^{t}FEAT. The READ STATUS (70h) command can be used to monitor for command completion.

Feature address 01h (timing mode) operation is unique. If SET FEATURES is used to modify the interface type, the target will be busy for ^{t}ITC.

Figure 28: SET FEATURES (EFh) Operation



GET FEATURES (EEh)

The GET FEATURES (EEh) command reads the subfeature parameters (P1–P4) from the specified feature address. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EEh to the command register puts the target in get features mode. The target stays in this mode until another valid command is issued.

When the EEh command is followed by a feature address, the target goes busy for ^{t}FEAT. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. During and prior to data output, use of the READ STATUS ENHANCED (78h) command is prohibited prior to and during data output.

After ^{t}FEAT completes, the host enables data output mode to read the subfeature parameters.

Figure 29: GET FEATURES (EEh) Operation

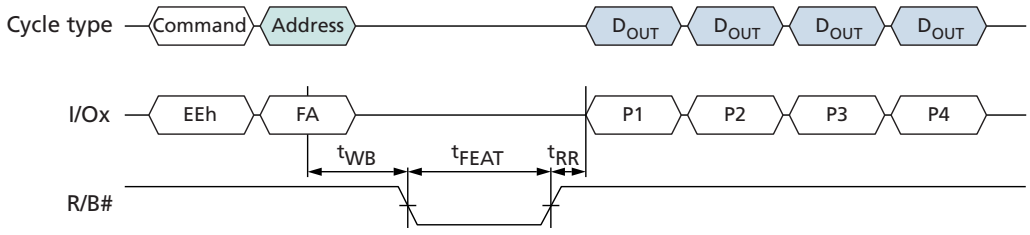


Table 20: Feature Addresses 01h: Timing Mode

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
Timing mode	Mode 0 (default)	Reserved (0)					0	0	0	00h	1, 2
	Mode 1	Reserved (0)					0	0	1	01h	2
	Mode 2	Reserved (0)					0	1	0	02h	2, 4
	Mode 3	Reserved (0)					0	1	1	03h	2
	Mode 4	Reserved (0)					1	0	0	04h	3
	Mode 5	Reserved (0)					1	0	1	05h	3
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Notes: 1. The timing mode feature address is used to change the default timing mode. The timing mode should be selected to indicate the maximum speed at which the device will receive commands, addresses, and data cycles. The five supported settings for the timing mode are shown. The default timing mode is mode 0. The device returns to mode 0 when the device is power cycled. Supported timing modes are reported in the parameter page.

2. Supported for both 1.8V and 3.3V.
3. Supported for 3.3V only.
4. Supported for 1.8V only.^{t}WHR, ^{t}REA, ^{t}CEA, and^{t}RHZ per timing mode 2. (See AC Characteristics: Normal Operation (1.8V) table for details.)

Table 21: Feature Addresses 80h: Programmable I/O Drive Strength

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
I/O drive strength	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarters	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Note: 1. The programmable drive strength feature address is used to change the default I/O drive strength. Drive strength should be selected based on expected loading of the memory bus. This table shows the four supported output drive strength settings. The default drive strength is full strength. The device returns to the default drive strength mode when the device is power cycled. AC timing parameters may need to be relaxed if I/O drive strength is not set to full.

Table 22: Feature Addresses 81h: Programmable R/B# Pull-Down Strength

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
R/B# pull-down strength	Full (default)							0	0	00h	1
	Three-quarters							0	1	01h	
	One-half							1	0	02h	
	One-quarter							1	1	03h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Note: 1. This feature address is used to change the default R/B# pull-down strength. Its strength should be selected based on the expected loading of R/B#. Full strength is the default, power-on value.

Status Operations

Each die (LUN) provides its status independently of other die (LUNs) on the same target through its 8-bit status register.

After the READ STATUS (70h) or READ STATUS ENHANCED (78h) command is issued, status register output is enabled. The contents of the status register are returned on I/O[7:0] for each data output request.

When the asynchronous interface is active and status register output is enabled, changes in the status register are seen on I/O[7:0] as long as CE# and RE# are LOW; it is not necessary to toggle RE# to see the status register update.

While monitoring the status register to determine when a data transfer from the Flash array to the data register (^{t}R) is complete, the host must issue the READ MODE (00h) command to disable the status register and enable data output (see Read Operations).

The READ STATUS (70h) command returns the status of the most recently selected die (LUN). To prevent data contention during or following an interleaved die (multi-LUN) operation, the host must enable only one die (LUN) for status output by using the READ STATUS ENHANCED (78h) command (see Interleaved Die (Multi-LUN) Operations).

Table 23: Status Register Definition

SR Bit	Program Page	Program Page Cache Mode	Page Read	Page Read Cache Mode	Block Erase	Description
7	Write protect	Write protect	Write protect	Write protect	Write protect	0 = Protected 1 = Not protected
6	RDY	RDY[2] cache	RDY	RDY[2] cache	RDY	0 = Busy 1 = Ready
5	ARDY	ARDY[1]	ARDY	ARDY[1]	ARDY	0 = Busy 1 = Ready
4	–	–	–	–	–	Reserved (0)
3	–	–	–	–	–	Reserved (0)
2	–	–	–	–	–	Reserved (0)
1	–	FAILC (N - 1)	–	–	–	0 = Pass 1 = Fail
0	FAIL	FAIL (N)	–	–	FAIL	0 = Pass 1 = Fail

Notes: 1. Status register bit 5 is 0 during the actual programming operation. If cache mode is used, this bit will be 1 when all internal operations are complete.
2. Status register bit 6 is 1 when the cache is ready to accept new data. R/B# follows bit 6.

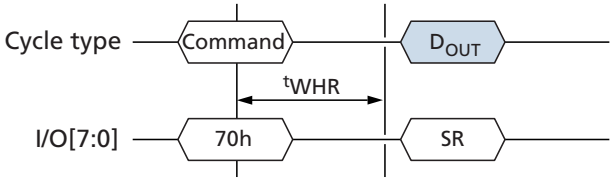
READ STATUS (70h)

The READ STATUS (70h) command returns the status of the last-selected die (LUN) on a target. This command is accepted by the last-selected die (LUN) even when it is busy (RDY = 0).

If there is only one die (LUN) per target, the READ STATUS (70h) command can be used to return status following any NAND command.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select the die (LUN) that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as two or more die (LUNs) could respond until the next operation is issued. The READ STATUS (70h) command can be used following all single-die (LUN) operations.

Figure 30: READ STATUS (70h) Operation



READ STATUS ENHANCED (78h)

The READ STATUS ENHANCED (78h) command returns the status of the addressed die (LUN) on a target even when it is busy (RDY = 0). This command is accepted by all die (LUNs), even when they are BUSY (RDY = 0).

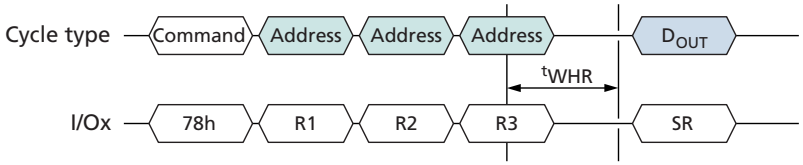
Writing 78h to the command register, followed by three row address cycles containing the page, block, and LUN addresses, puts the selected die (LUN) into read status mode. The selected die (LUN) stays in this mode until another valid command is issued. Die (LUNs) that are not addressed are deselected to avoid bus contention.

The selected LUN's status is returned when the host requests data output. The RDY and ARDY bits of the status register are shared for all planes on the selected die (LUN). The FAILC and FAIL bits are specific to the plane specified in the row address.

The READ STATUS ENHANCED (78h) command also enables the selected die (LUN) for data output. To begin data output following a READ-series operation after the selected die (LUN) is ready (RDY = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the cache register that will output data, use the RANDOM DATA READ TWO-PLANE (06h-E0h) command after the die (LUN) is ready.

Use of the READ STATUS ENHANCED (78h) command is prohibited during the power-on RESET (FFh) command and when OTP mode is enabled. It is also prohibited following some of the other reset, identification, and configuration operations. See individual operations for specific details.

Figure 31: READ STATUS ENHANCED (78h) Operation



Column Address Operations

The column address operations affect how data is input to and output from the cache registers within the selected die (LUNs). These features provide host flexibility for managing data, especially when the host internal buffer is smaller than the number of data bytes or words in the cache register.

When the asynchronous interface is active, column address operations can address any byte in the selected cache register.

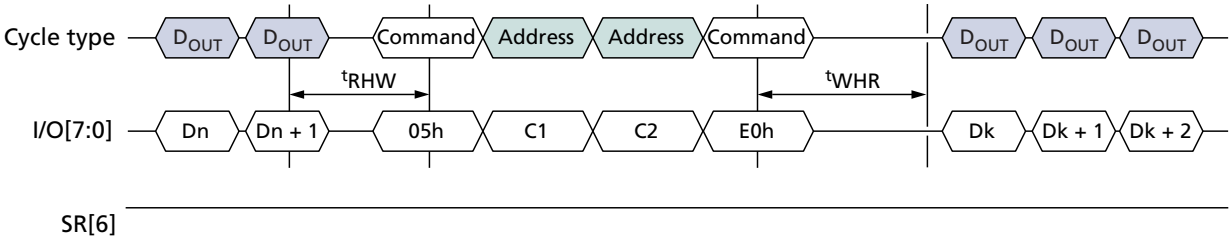
RANDOM DATA READ (05h-E0h)

The RANDOM DATA READ (05h-E0h) command changes the column address of the selected cache register and enables data output from the last selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during CACHE READ operations (RDY = 1; ARDY = 0).

Writing 05h to the command register, followed by two column address cycles containing the column address, followed by the E0h command, puts the selected die (LUN) into data output mode. After the E0h command cycle is issued, the host must wait at least ^{t}WHR before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be issued prior to issuing the RANDOM DATA READ (05h-E0h). In this situation, using the RANDOM DATA READ (05h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention because two or more die (LUNs) could output data.

Figure 32: RANDOM DATA READ (05h-E0h) Operation



RANDOM DATA READ TWO-PLANE (06h-E0h)

The RANDOM DATA READ TWO-PLANE (06h-E0h) command enables data output on the addressed die's (LUN's) cache register at the specified column address. This command is accepted by a die (LUN) when it is ready (RDY = 1; ARDY = 1).

Writing 06h to the command register, followed by two column address cycles and three row address cycles, followed by E0h, enables data output mode on the address LUN's cache register at the specified column address. After the E0h command cycle is issued, the host must wait at least ^{t}WHR before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

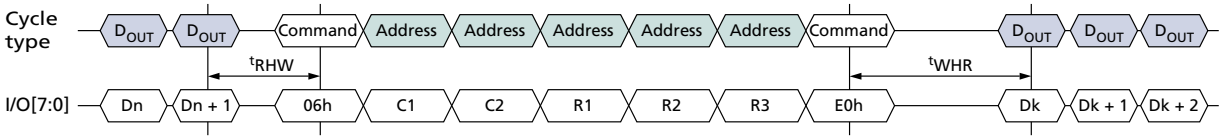
Following a two-plane read page operation, the RANDOM DATA READ TWO-PLANE (06h-E0h) command is used to select the cache register to be enabled for data output. After data output is complete on the selected plane, the command can be issued again to begin data output on another plane.

In devices with more than one die (LUN) per target, after all of the die (LUNs) on the target are ready (RDY = 1), the RANDOM DATA READ TWO-PLANE (06h-E0h) command can be used following an interleaved die (multi-LUN) read operation. Die (LUNs) that are not addressed are deselected to avoid bus contention.

In devices with more than one die (LUN) per target, during interleaved die (multi-LUN) operations where more than one or more die (LUNs) are busy (RDY = 1; ARDY = 0 or RDY = 0; ARDY = 0), the READ STATUS ENHANCED (78h) command must be issued to the die (LUN) to be selected prior to issuing the RANDOM DATA READ TWO-PLANE (06h-E0h). In this situation, using the RANDOM DATA READ TWO-PLANE (06h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention, as two or more die (LUNs) could output data.

If there is a need to update the column address without selecting a new cache register or LUN, the RANDOM DATA READ (05h-E0h) command can be used instead.

Figure 33: RANDOM DATA READ TWO-PLANE (06h-E0h) Operation



RANDOM DATA INPUT (85h)

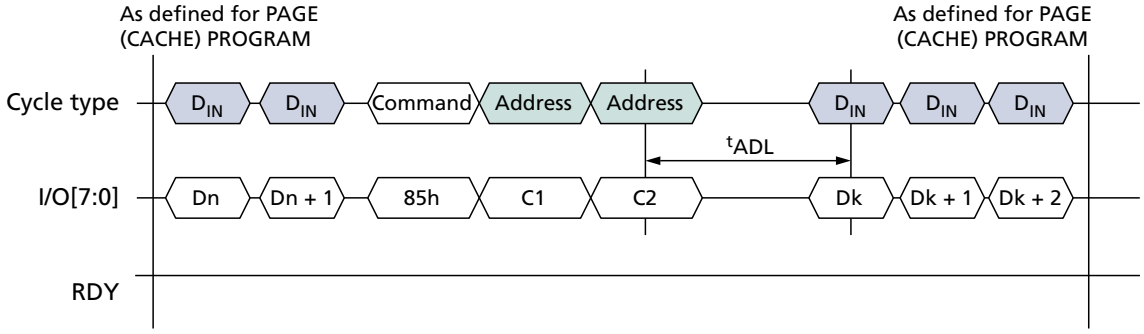
The RANDOM DATA INPUT (85h) command changes the column address of the selected cache register and enables data input on the last-selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during cache program operations
(RDY = 1; ARDY = 0).

Writing 85h to the command register, followed by two column address cycles containing the column address, puts the selected die (LUN) into data input mode. After the second address cycle is issued, the host must wait at least ^{t}ADL before inputting data. The selected die (LUN) stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The RANDOM DATA INPUT (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE CACHE (80h-15h), PROGRAM FOR INTERNAL DATA MOVE (85h-10h), and PROGRAM FOR TWO-PLANE INTERNAL DATA MOVE (85h-11h).

In devices that have more than one die (LUN) per target, the RANDOM DATA INPUT (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

Figure 34: RANDOM DATA INPUT (85h) Operation



PROGRAM FOR INTERNAL DATA INPUT (85h)

The PROGRAM FOR INTERNAL DATA INPUT (85h) command changes the row address (block and page) where the cache register contents will be programmed in the NAND Flash array. It also changes the column address of the selected cache register and enables data input on the specified die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during cache programming operations (RDY = 1; ARDY = 0).

Write 85h to the command register. Then write two column address cycles and three row address cycles. This updates the page and block destination of the selected device for the addressed LUN and puts the cache register into data input mode. After the fifth address cycle is issued the host must wait at least ^{t}ADL before inputting data. The selected LUN stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The PROGRAM FOR INTERNAL DATA INPUT (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE TWO-PLANE (80h-11h), PROGRAM PAGE CACHE (80h-15h), PROGRAM FOR INTERNAL DATA MOVE (85h-10h), and PROGRAM FOR TWO-PLANE INTERNAL DATA MOVE (85h-11h). When used with these commands, the LUN address and plane select bits are required to be identical to the LUN address and plane select bits originally specified.

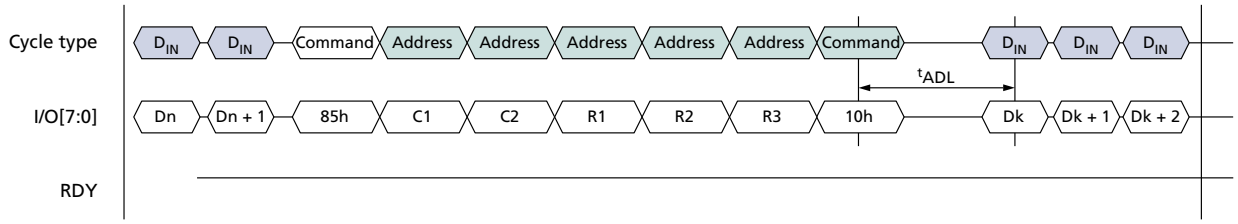
The PROGRAM FOR INTERNAL DATA INPUT (85h) command enables the host to modify the original page and block address for the data in the cache register to a new page and block address.

In devices that have more than one die (LUN) per target, the PROGRAM FOR INTERNAL DATA INPUT (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

The PROGRAM FOR INTERNAL DATA INPUT (85h) command can be used with the RANDOM DATA READ (05h-E0h) or RANDOM DATA READ TWO-PLANE (06h-E0h) commands to read and modify cache register contents in small sections prior to programming cache register contents to the NAND Flash array. This capability can reduce the amount of buffer memory used in the host controller.

The RANDOM DATA INPUT (85h) command can be used during the PROGRAM FOR INTERNAL DATA MOVE command sequence to modify one or more bytes of the original data. First, data is copied into the cache register using the 00h-35h command sequence, then the RANDOM DATA INPUT (85h) command is written along with the address of the data to be modified next. New data is input on the external data pins. This copies the new data into the cache register.

Figure 35: PROGRAM FOR INTERNAL DATA INPUT (85h) Operation



Read Operations

The READ PAGE (00h-30h) command, when issued by itself, reads one page from the NAND Flash array to its cache register and enables data output for that cache register.

During data output the following commands can be used to read and modify the data in the cache registers: RANDOM DATA READ (05h-E0h) and RANDOM DATA INPUT (85h).

Read Cache Operations

To increase data throughput, the READ PAGE CACHE series (31h, 00h-31h) commands can be used to output data from the cache register while concurrently copying a page from the NAND Flash array to the data register.

To begin a read page cache sequence, begin by reading a page from the NAND Flash array to its corresponding cache register using the READ PAGE (00h-30h) command. R/B# goes LOW during ^{t}R and the selected die (LUN) is busy (RDY = 0, ARDY = 0). After ^{t}R (R/B# is HIGH and RDY = 1, ARDY = 1), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h) – copies the next sequential page from the NAND Flash array to the data register
- READ PAGE CACHE RANDOM (00h-31h) – copies the page specified in this command from the NAND Flash array to its corresponding data register

After the READ PAGE CACHE series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the next page begins copying data from the array to the data register. After ^{t}RCBSY,
R/B# goes HIGH and the die's (LUN's) status register bits indicate the device is busy with a cache operation (RDY = 1, ARDY = 0). The cache register becomes available and the page requested in the READ PAGE CACHE operation is transferred to the data register. At this point, data can be output from the cache register, beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data output by the die (LUN).

After outputting the desired number of bytes from the cache register, either an additional READ PAGE CACHE series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the data register is copied into the cache register. After ^{t}RCBSY, R/B# goes HIGH and RDY = 1 and ARDY = 1, indicating that the cache register is available and that the die (LUN) is ready. Data can then be output from the cache register, beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output.

For READ PAGE CACHE series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, ^{t}RCBSY, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and RESET (FFh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE series (31h, 00h-31h) operations are status operations (70h, 78h), READ MODE (00h), READ PAGE CACHE series (31h, 00h-31h), RANDOM DATA READ (05h-E0h), and RESET (FFh).

Two-Plane Read Operations

Two-plane read page operations improve data throughput by copying data from more than one plane simultaneously to the specified cache registers. This is done by prepending one or more READ PAGE TWO-PLANE (00h-00h-30h) commands in front of the READ PAGE (00h-30h) command.

When the die (LUN) is ready, the RANDOM DATA READ TWO-PLANE (06h-E0h) command determines which plane outputs data. During data output, the following commands can be used to read and modify the data in the cache registers: RANDOM DATA READ (05h-E0h) and RANDOM DATA INPUT (85h).

Two-Plane Read Cache Operations

Two-plane read cache operations can be used to output data from more than one cache register while concurrently copying one or more pages from the NAND Flash array to the data register. This is done by prepending READ PAGE TWO-PLANE (00h-00h-30h) commands in front of the PAGE READ CACHE RANDOM (00h-31h) command.

To begin a two-plane read page cache sequence, begin by issuing a READ PAGE TWO-PLANE operation using the READ PAGE TWO-PLANE (00h-00h-30h) and READ PAGE (00h-30h) commands. R/B# goes LOW during ^{t}R and the selected die (LUN) is busy (RDY = 0, ARDY = 0). After ^{t}R (R/B# is HIGH and RDY = 1, ARDY = 1), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h) – copies the next sequential pages from the previously addressed planes from the NAND Flash array to the data registers.
- READ PAGE TWO-PLANE (00h-00h-30h) [in some cases, followed by READ PAGE CACHE RANDOM (00h-31h)] – copies the pages specified from the NAND Flash array to the corresponding data registers.

After the READ PAGE CACHE series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the next pages begin copying data from the array to the data registers. After ^{t}RCBSY, R/B# goes HIGH and the LUN's status register bits indicate the device is busy with a cache operation (RDY = 1, ARDY = 0). The cache registers become available and the pages requested in the READ PAGE CACHE operation are transferred to the data registers. Issue the RANDOM DATA READ TWO-PLANE (06h-E0h) command to determine which cache register will output data. After data is output, the RANDOM DATA READ TWO-PLANE (06h-E0h) command can be used to output data from other cache registers. After a cache register has been selected, the RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data output.

After outputting data from the cache registers, either an additional TWO-PLANE READ CACHE series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the data registers are copied into the cache registers. After ^{t}RCBSY, R/B# goes HIGH and RDY = 1 and ARDY = 1, indicating that the cache registers are available and that the die (LUN) is ready. Issue the RANDOM DATA READ TWO-PLANE (06h-E0h) command to determine which cache register will output data. After data is output, the RANDOM DATA READ TWO-PLANE (06h-E0h) command can be used to output data from other cache registers. After a cache register has been selected, the RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data output.

For READ PAGE CACHE series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, ^{t}RCBSY, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and RESET (FFh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE series (31h, 00h-31h) operations are status operations (70h, 78h), READ MODE (00h), two-plane read cache series (31h, 00h-00h-30h, 00h-31h), RANDOM DATA READ (06h-E0h, 05h-E0h), and RESET (FFh).

READ MODE (00h)

The READ MODE (00h) command disables status output and enables data output for the last-selected die (LUN) and cache register after a READ operation (00h-30h, 00h-3Ah, 00h-35h) has been monitored with a status operation (70h, 78h). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to issuing the READ MODE (00h) command. This prevents bus contention.

READ PAGE (00h-30h)

The READ PAGE (00h–30h) command copies a page from the NAND Flash array to its respective cache register and enables data output. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To read a page from the NAND Flash array, write the 00h command to the command register, then write *n* address cycles to the address registers, and conclude with the 30h command. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}R as data is transferred.

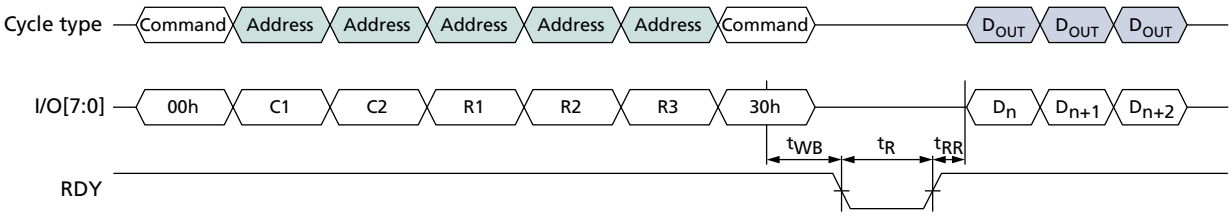
To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. If the status operations are used to monitor the LUN's status, when the die (LUN) is ready (RDY = 1, ARDY = 1), the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, output begins at the column address specified.

During data output the RANDOM DATA READ (05h-E0h) command can be issued.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to the issue of the READ MODE (00h) command. This prevents bus contention.

The READ PAGE (00h-30h) command is used as the final command of a two-plane read operation. It is preceded by one or more READ PAGE TWO-PLANE (00h-00h-30h) commands. Data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the die (LUN) is ready (RDY = 1, ARDY = 1), data output is enabled for the cache register linked to the plane addressed in the READ PAGE (00h-30h) command. When the host requests data output, output begins at the column address last specified in the READ PAGE (00h-30h) command. The RANDOM DATA READ TWO-PLANE (06h-E0h) command is used to enable data output in the other cache registers.

Figure 36: READ PAGE (00h-30h) Operation



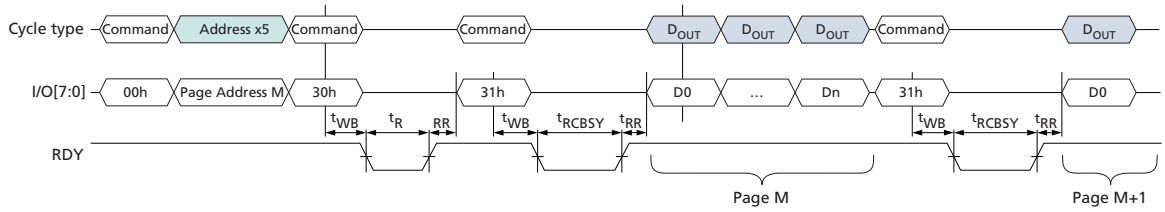
READ PAGE CACHE SEQUENTIAL (31h)

The READ PAGE CACHE SEQUENTIAL (31h) command reads the next sequential page within a block into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue this command, write 31h to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output from the cache register.

The READ PAGE CACHE SEQUENTIAL (31h) command can be used to cross block boundaries. If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after the last page of a block is read into the data register, the next page read will be the next logical block in which the 31h command was issued. Do not issue the READ PAGE CACHE SEQUENTIAL (31h) to cross die (LUN) boundaries. Instead, issue the READ PAGE CACHE LAST (3Fh) command.

Figure 37: READ PAGE CACHE SEQUENTIAL (31h) Operation



READ PAGE CACHE RANDOM (00h-31h)

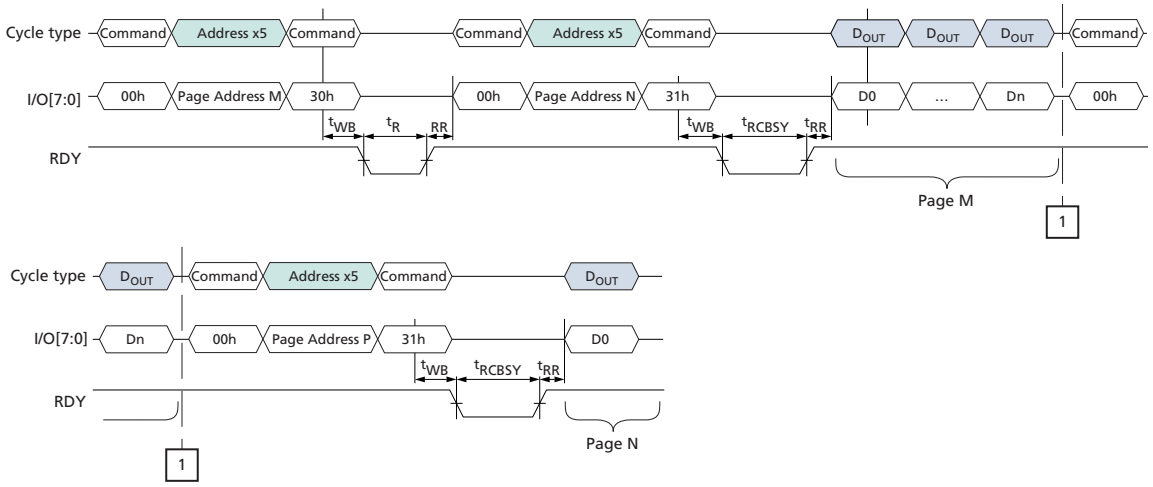
The READ PAGE CACHE RANDOM (00h-31h) command reads the specified block and page into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue this command, write 00h to the command register, then write *n* address cycles to the address register, and conclude by writing 31h to the command register. The column address in the address specified is ignored. The die (LUN) address must match the same die (LUN) address as the previous READ PAGE (00h-30h) command or, if applicable, the previous READ PAGE CACHE RANDOM (00h-31h) command.

After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command followed by the READ MODE (00h) command must be used to select only one die (LUN) and prevent bus contention.

Figure 38: READ PAGE CACHE RANDOM (00h-31h) Operation



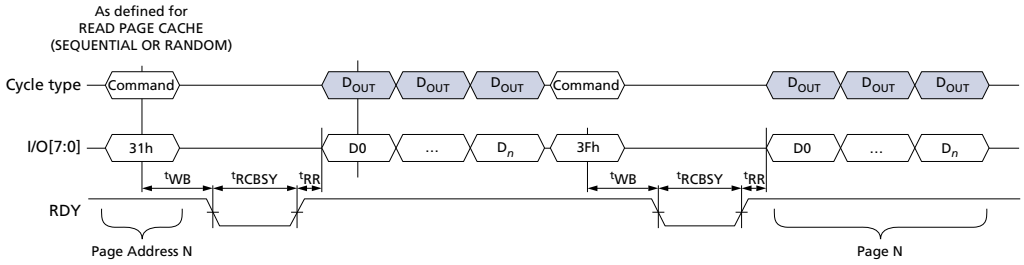
READ PAGE CACHE LAST (3Fh)

The READ PAGE CACHE LAST (3Fh) command ends the read page cache sequence and copies a page from the data register to the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue the READ PAGE CACHE LAST (3Fh) command, write 3Fh to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and the die (LUN) is ready (RDY = 1, ARDY = 1). At this point, data can be output from the cache register, beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one LUN per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command followed by the READ MODE (00h) command must be used to select only one die (LUN) and prevent bus contention.

Figure 39: READ PAGE CACHE LAST (3Fh) Operation



READ PAGE TWO-PLANE 00h-00h-30h

The READ PAGE TWO-PLANE (00h-00h-30h) operation is similar to the PAGE READ (00h-30h) operation. It transfers two pages of data from the NAND Flash array to the data registers. Each page must be from a different plane on the same die.

To enter the READ PAGE TWO-PLANE mode, write the 00h command to the command register, and then write five address cycles for plane 0 (BA6 = 0). Next, write the 00h command to the command register, and five address cycles for plane 1 (BA6 = 1). Finally, issue the 30h command. The first-plane

and second-plane addresses must meet the two-plane addressing requirements, and, in addition, they must have identical column addresses.

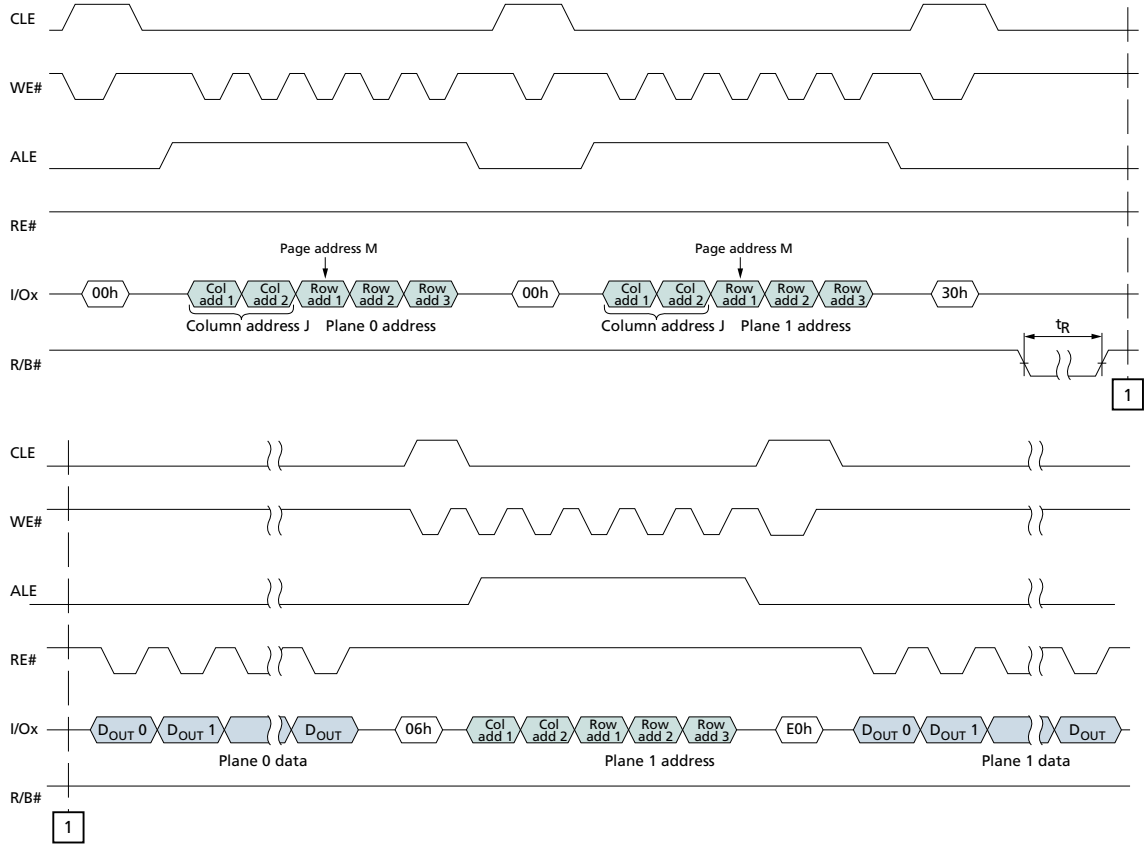
After the 30h command is written, page data is transferred from both planes to their respective data registers in ^{t}R. During these transfers, R/B# goes LOW. When the transfers are complete, R/B# goes HIGH. To read out the data from the plane 0 data register, pulse RE# repeatedly. After the data cycle from the plane 0 address completes, issue a RANDOM DATA READ TWO-PLANE (06h-E0h) command to select the plane 1 address, then repeatedly pulse RE# to read out the data from the plane 1 data register.

Alternatively, the READ STATUS (70h) command can monitor data transfers. When the transfers are complete, status register bit 6 is set to 1. To read data from the first of the two planes, the user must first issue the RANDOM DATA READ TWO-PLANE (06h-E0h) command and pulse RE# repeatedly.

When the data cycle is complete, issue a RANDOM DATA READ TWO-PLANE (06h-E0h) command to select the other plane. To output the data beginning at the specified column address, pulse RE# repeatedly.

Use of the READ STATUS ENHANCED (78h) command is prohibited during and following a PAGE READ TWO-PLANE operation.

Figure 40: READ PAGE TWO-PLANE (00h-00h-30h) Operation



Program Operations

Program operations are used to move data from the cache or data registers to the NAND array. During a program operation the contents of the cache and/or data registers are modified by the internal control logic.

Within a block, pages must be programmed sequentially from the least significant page address to the most significant page address (0, 1, 2, ….., 63). During a program operation, the contents of the cache and/or data registers are modified by the internal control logic.

Program Operations

The PROGRAM PAGE (80h-10h) command, when not preceded by the PROGRAM PAGE TWO-PLANE (80h-11h) command, programs one page from the cache register to the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that the operation has completed successfully.

Program Cache Operations

The PROGRAM PAGE CACHE (80h-15h) command can be used to improve program operation system performance. When this command is issued, the die (LUN) goes busy (RDY = 0, ARDY = 0) while the cache register contents are copied to the data register, and the die (LUN) is busy with a program cache operation (RDY = 1, ARDY = 0. While the contents of the data register are moved to the NAND Flash array, the cache register is available for an additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) command.

For PROGRAM PAGE CACHE series (80h-15h) operations, during the die (LUN) busy times, ^{t}CBSY and ^{t}LPROG, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and reset (FFh). When RDY = 1 and ARDY = 0, the only valid commands during PROGRAM PAGE CACHE series (80h-15h) operations are status operations (70h, 78h), PROGRAM PAGE CACHE (80h-15h), PROGRAM PAGE (80h-10h), RANDOM DATA INPUT (85h), PROGRAM FOR INTERNAL DATA INPUT (85h), and RESET (FFh).

Two-Plane Program Operations

The PROGRAM PAGE TWO-PLANE (80h-11h) command can be used to improve program operation system performance by enabling multiple pages to be moved from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more PROGRAM PAGE TWO-PLANE (80h-11h) commands in front of the PROGRAM PAGE (80h-10h) command.

Two-Plane Program Cache Operations

The PROGRAM PAGE TWO-PLANE (80h-11h) command can be used to improve program cache operation system performance by enabling multiple pages to be moved from the cache registers to the data registers and, while the pages are being transferred from the data registers to different planes of the NAND Flash array, free the cache registers to receive data input from the host. This is done by prepending one or more PROGRAM PAGE TWO-PLANE (80h-11h) commands in front of the PROGRAM PAGE CACHE (80h-15h) command.

PROGRAM PAGE (80h-10h)

The PROGRAM PAGE (80h-10h) command enables the host to input data to a cache register, and moves the data from the cache register to the specified block and page address in the array of the selected die (LUN). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) when it is busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

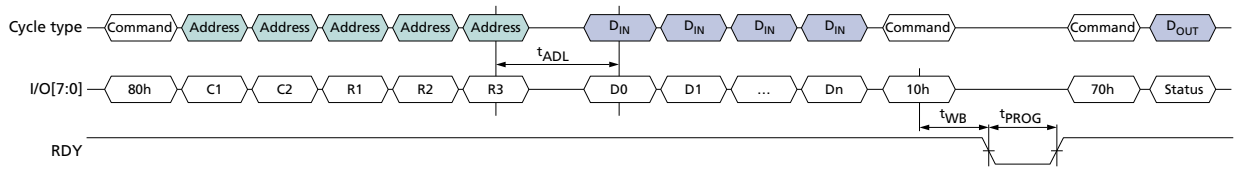
To input a page to the cache register and move it to the NAND array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE TWO-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write *n* address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the RANDOM DATA INPUT (85h) and PROGRAM FOR INTERNAL DATA INPUT (85h) commands may be issued. When data input is complete, write 10h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}PROG as data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) may be used. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The PROGRAM PAGE (80h-10h) command is used as the final command of a two-plane program operation. It is preceded by one or more PROGRAM PAGE TWO-PLANE (80h-11h) commands. Data is transferred from the cache registers for all of the addressed planes to the NAND array. The host should check the status of the operation by using the status operations (70h, 78h).

Figure 41: PROGRAM PAGE (80h-10h) Operation



PROGRAM PAGE CACHE (80h-15h)

The PROGRAM PAGE CACHE (80h-15h) command enables the host to input data to a cache register; copies the data from the cache register to the data register; then moves the data register contents to the specified block and page address in the array of the selected die (LUN). After the data is copied to the data register, the cache register is available for additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) commands. The PROGRAM PAGE CACHE (80h-15h) command is accepted by the die (LUN) when it is ready (RDY =1, ARDY = 1). It is also accepted by the die (LUN) when busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

To input a page to the cache register to move it to the NAND array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE TWO-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write *n* address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the RANDOM DATA INPUT (85h) and PROGRAM FOR INTERNAL DATA INPUT (85h) commands may be issued. When data input is complete, write 15h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}CBSY to allow the data register to become available from a previous program cache operation, to copy data from the cache register to the data register, and then to begin moving the data register contents to the specified page and block address.

To determine the progress of ^{t}CBSY, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is busy with a PROGRAM CACHE operation (RDY = 1, ARDY = 0), the host should check the status of the FAILC bit to see if a previous cache operation was successful.

If, after ^{t}CBSY, the host wants to wait for the program cache operation to complete, without issuing the PROGRAM PAGE (80h-10h) command, the host should monitor ARDY until it is 1. The host should then check the status of the FAIL and FAILC bits.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The PROGRAM PAGE CACHE (80h-15h) command is used as the final command of a two-plane program cache operation. It is preceded by one or more PROGRAM PAGE TWO-PLANE (80h-11h) commands. Data for all of the addressed planes is transferred from the cache registers to the corresponding data registers, then moved to the NAND Flash array. The host should check the status of the operation by using the status operations (70h, 78h).

Figure 42: PROGRAM PAGE CACHE (80h–15h) Operation (Start)

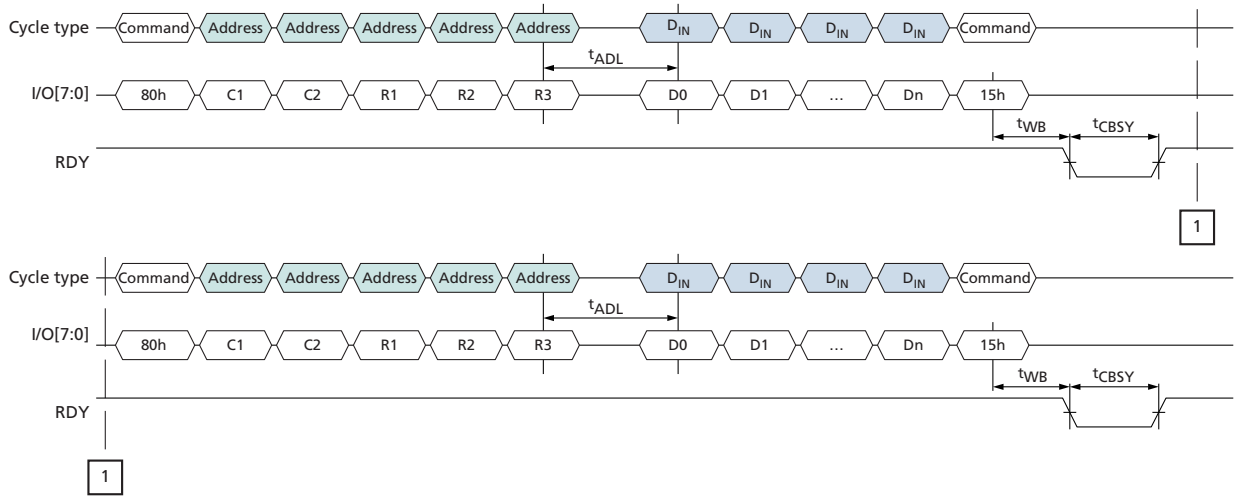
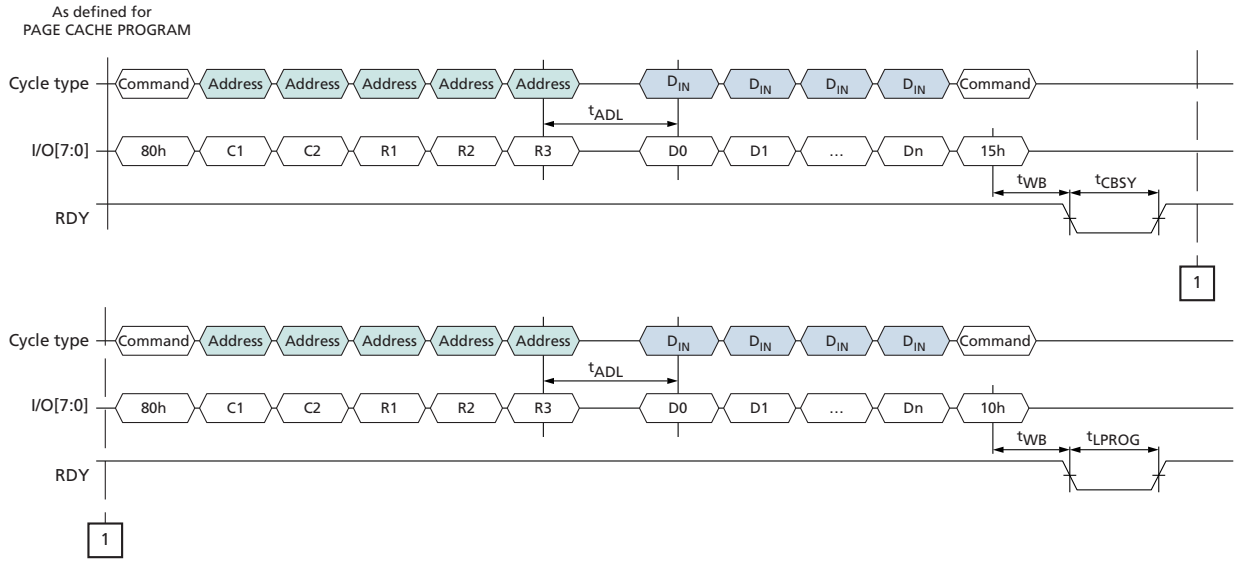


Figure 43: PROGRAM PAGE CACHE (80h–15h) Operation (End)



PROGRAM PAGE TWO-PLANE (80h-11h)

The PROGRAM PAGE TWO-PLANE (80h-11h) command enables the host to input data to the addressed plane's cache register and queue the cache register to ultimately be moved to the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified that plane is also queued for data transfer. To input data for the final plane and to begin the program operation for all previously queued planes, issue either the PROGRAM PAGE (80h-10h) command or the PROGRAM PAGE CACHE (80h-15h) command. All of the queued planes will move the data to the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1).

To input a page to the cache register and queue it to be moved to the NAND Flash array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE TWO-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Write five address cycles containing the column address and row address; data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle, the RANDOM

DATA INPUT (85h) and PROGRAM FOR INTERNAL DATA INPUT (85h) commands can be issued. When data input is complete, write 11h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}DBSY.

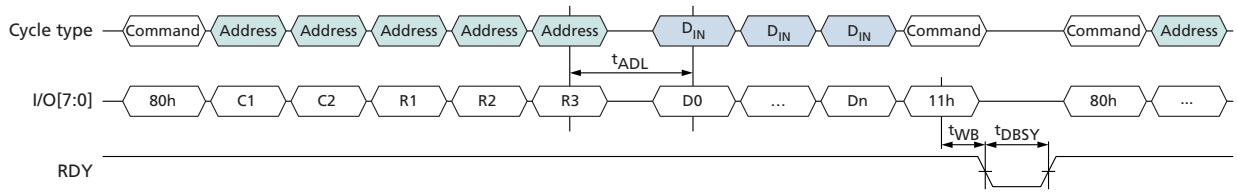
To determine the progress of ^{t}DBSY, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is ready (RDY = 1), additional PROGRAM PAGE TWO-PLANE (80h-11h) commands can be issued to queue additional planes for data transfer. Alternatively, the PROGRAM PAGE (80h-10h) or PROGRAM PAGE CACHE (80h-15h) commands can be issued.

When the PROGRAM PAGE (80h-10h) command is used as the final command of a two-plane program operation, data is transferred from the cache registers to the NAND Flash array for all of the addressed planes during ^{t}PROG. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit for each of the planes to verify that programming completed successfully.

When the PROGRAM PAGE CACHE (80h-15h) command is used as the final command of a program cache two-plane operation, data is transferred from the cache registers to the data registers after the previous array operations finish. The data is then moved from the data registers to the NAND Flash array for all of the addressed planes. This occurs during ^{t}CBSY. After ^{t}CBSY, the host should check the status of the FAILC bit for each of the planes from the previous program cache operation, if any, to verify that programming completed successfully.

For the PROGRAM PAGE TWO-PLANE (80h-11h), PROGRAM PAGE (80h-10h), and PROGRAM PAGE CACHE (80h-15h) commands, see Two-Plane Operations for two-plane addressing requirements.

Figure 44: PROGRAM PAGE TWO-PLANE (80h–11h) Operation



Erase Operations

Erase operations are used to clear the contents of a block in the NAND Flash array to prepare its pages for program operations.

Erase Operations

The ERASE BLOCK (60h-D0h) command, when not preceded by the ERASE BLOCK TWO-PLANE (60h-D1h) command, erases one block in the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

TWO-PLANE ERASE Operations

The ERASE BLOCK TWO-PLANE (60h-D1h) command can be used to further system performance of erase operations by allowing more than one block to be erased in the NAND array. This is done by prepending one or more ERASE BLOCK TWO-PLANE (60h-D1h) commands in front of the ERASE BLOCK (60h-D0h) command. See Two-Plane Operations for details.

ERASE BLOCK (60h-D0h)

The ERASE BLOCK (60h-D0h) command erases the specified block in the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

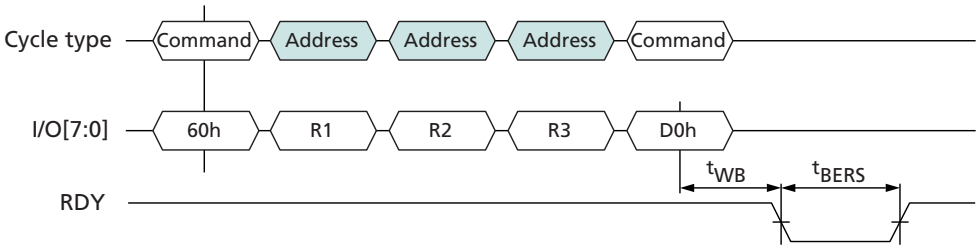
To erase a block, write 60h to the command register. Then write three address cycles containing the row address; the page address is ignored. Conclude by writing D0h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}BERS while the block is erased.

To determine the progress of an ERASE operation, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the die (LUN) is ready (RDY = 1, ARDY = 1) the host should check the status of the FAIL bit.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The ERASE BLOCK (60h-D0h) command is used as the final command of an erase two-plane operation. It is preceded by one or more ERASE BLOCK TWO-PLANE (60h-D1h) commands. All blocks in the addressed planes are erased. The host should check the status of the operation by using the status operations (70h, 78h). See Two-Plane Operations for two-plane addressing requirements.

Figure 45: ERASE BLOCK (60h-D0h) Operation



ERASE BLOCK TWO-PLANE (60h-D1h)

The ERASE BLOCK TWO-PLANE (60h-D1h) command queues a block in the specified plane to be erased in the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for a block to be erased. To specify the final block to be erased and to begin the ERASE operation for all previously queued planes, issue the ERASE

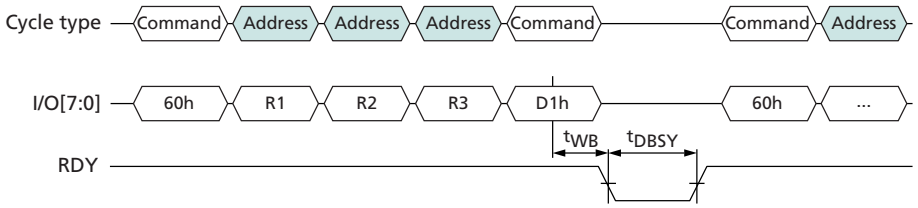
BLOCK (60h-D0h) command. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To queue a block to be erased, write 60h to the command register, then write three address cycles containing the row address; the page address is ignored. Conclude by writing D1h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}DBSY.

To determine the progress of ^{t}DBSY, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is ready (RDY = 1, ARDY = 1), additional ERASE BLOCK TWO-PLANE (60h-D1h) commands can be issued to queue additional planes for erase. Alternatively, the ERASE BLOCK (60h-D0h) command can be issued to erase all of the queued blocks.

For two-plane addressing requirements for the ERASE BLOCK TWO-PLANE (60h-D1h) and ERASE BLOCK (60h-D0h) commands, see Two-Plane Operations.

Figure 46: ERASE BLOCK TWO-PLANE (60h–D1h) Operation



Internal Data Move Operations

Internal data move operations make it possible to transfer data within a device from one page to another using the cache register. This is particularly useful for block management and wear leveling.

The INTERNAL DATA MOVE operation is a two-step process consisting of a READ FOR INTERNAL DATA MOVE (00h-35h) and a PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command. To move data from one page to another on the same plane, first issue the READ FOR INTERNAL DATA MOVE (00h-35h) command. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host can transfer the data to a new page by issuing the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command. When the die (LUN) is again ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

To prevent bit errors from accumulating over multiple INTERNAL DATA MOVE operations, it is recommended that the host read the data out of the cache register after the READ FOR INTERNAL DATA MOVE (00h-35h) completes and prior to issuing the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command. The RANDOM DATA READ (05h-E0h) command can be used to change the column address. The host should check the data for ECC errors and correct them. When the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command is issued, any corrected data can be input. The PROGRAM FOR INTERNAL DATA INPUT (85h) command can be used to change the column address.

It is not possible to use the READ FOR INTERNAL DATA MOVE operation to move data from one plane to another or from one die (LUN) to another. Instead, use a READ PAGE (00h-30h) or READ FOR INTERNAL DATA MOVE (00h-35h) command to read the data out of the NAND, and then use a PROGRAM PAGE (80h-10h) command with data input to program the data to a new plane or die (LUN).

Between the READ FOR INTERNAL DATA MOVE (00h-35h) and PROGRAM FOR INTERNAL DATA MOVE (85h-10h) commands, the following commands are supported: status operations (70h, 78h) and column address operations (05h-E0h, 06h-E0h, 85h). The RESET operation (FFh) can be issued after READ FOR INTERNAL DATA MOVE (00h-35h), but the contents of the cache registers on the target are not valid.

In devices that have more than one die (LUN) per target, once the READ FOR INTERNAL DATA MOVE (00h-35h) is issued, interleaved die (multi-LUN) operations are prohibited until after the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command is issued.

Two-Plane Read for Internal Data Move Operations

Two-plane internal data move read operations improve read data throughput by copying data simultaneously from more than one plane to the specified cache registers. This is done by issuing the READ PAGE TWO-PLANE (00h-00h-30h) command or the READ FOR INTERNAL DATA MOVE (00h-00h-35h) command.

The INTERNAL DATA MOVE PROGRAM TWO-PLANE (85h-11h) command can be used to further system performance of PROGRAM FOR INTERNAL DATA MOVE operations by enabling movement of multiple pages from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more PROGRAM FOR INTERNAL DATA MOVE (85h-11h) commands in front of the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command. See Two-Plane Operations for details.

READ FOR INTERNAL DATA MOVE (00h-35h)

The READ FOR INTERNAL DATA MOVE (00h-35h) command is functionally identical to the READ PAGE (00h-30h) command, except that 35h is written to the command register instead of 30h.

Though it is not required, it is recommended that the host read the data out of the device to verify the data prior to issuing the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command to prevent the propagation of data errors.

Figure 47: READ FOR INTERNAL DATA MOVE (00h-35h) Operation

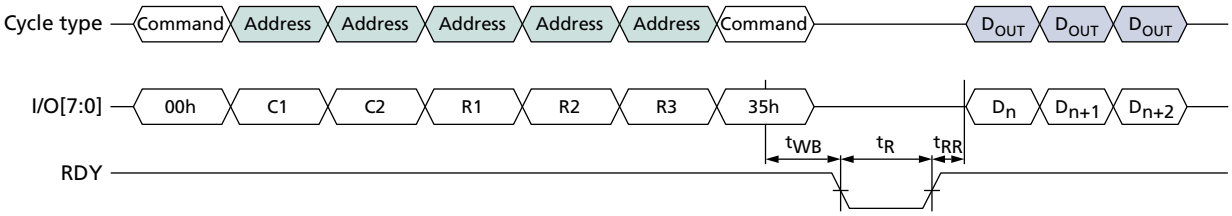
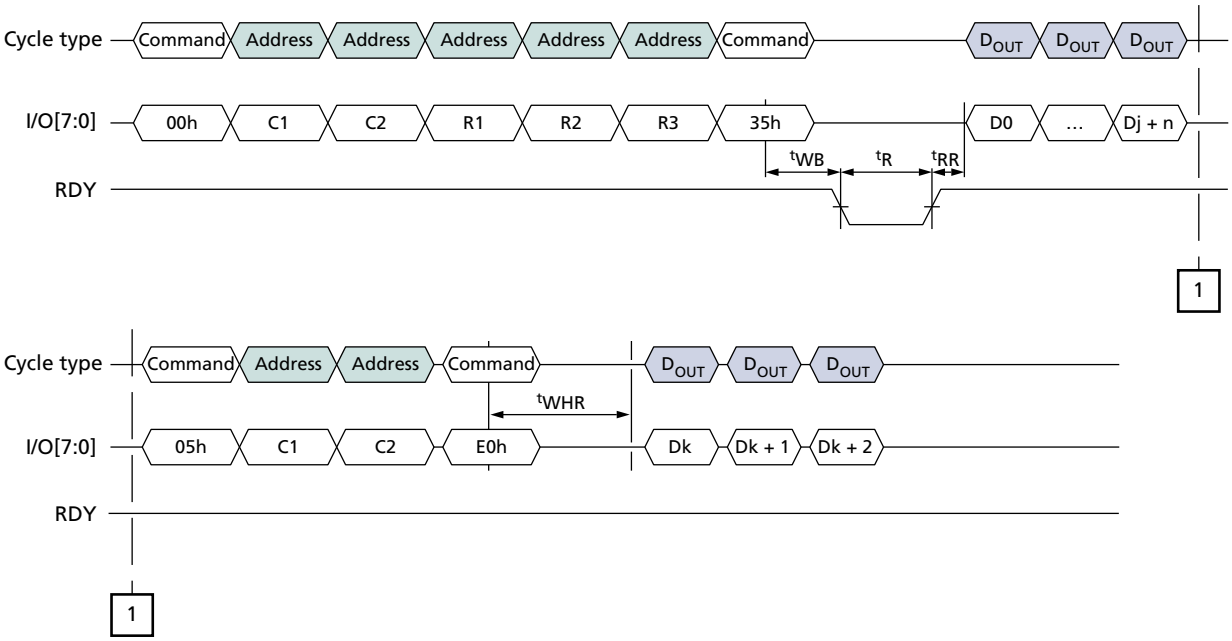


Figure 48: READ FOR INTERNAL DATA MOVE (00h–35h) with RANDOM DATA READ (05h–E0h)



PROGRAM FOR INTERNAL DATA MOVE (85h–10h)

The PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command is functionally identical to the PROGRAM PAGE (80h-10h) command, except that when 85h is written to the command register, cache register contents are not cleared.

Figure 49: PROGRAM FOR INTERNAL DATA MOVE (85h–10h) Operation

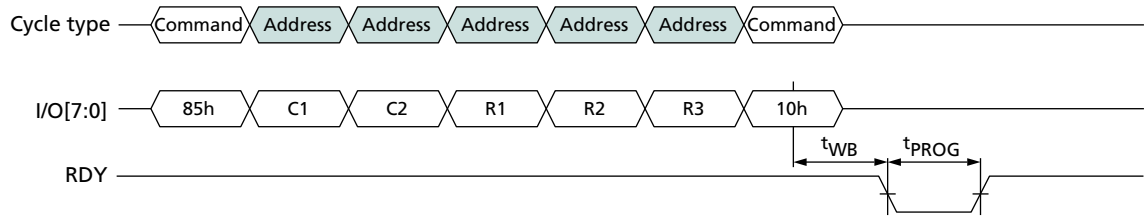
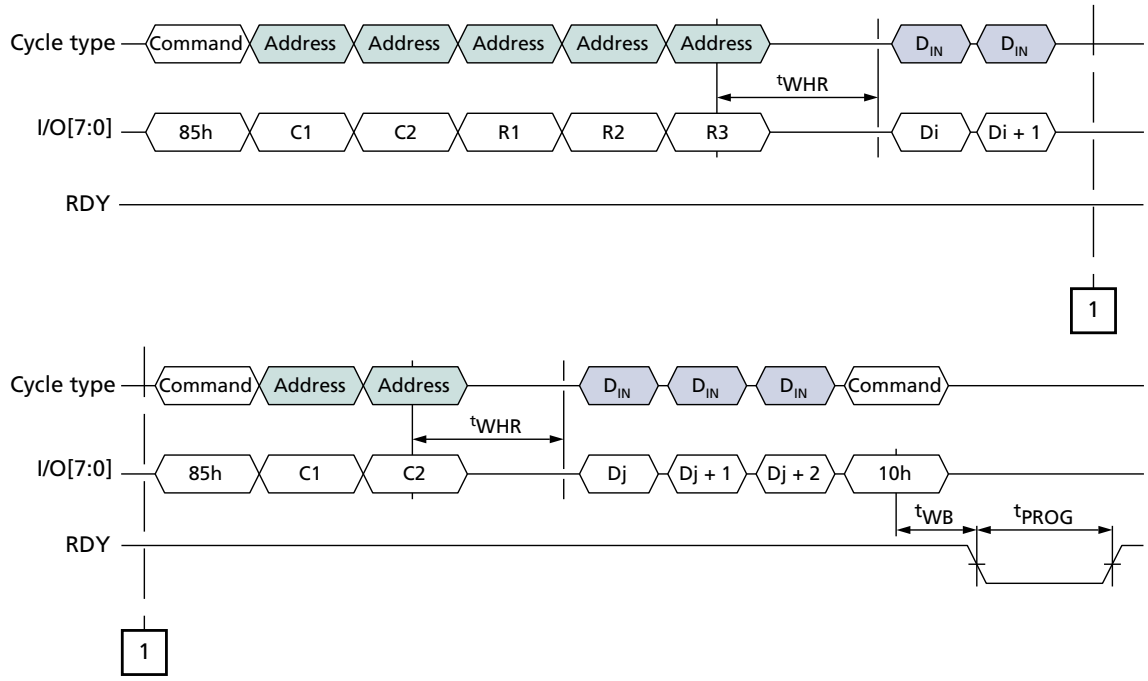


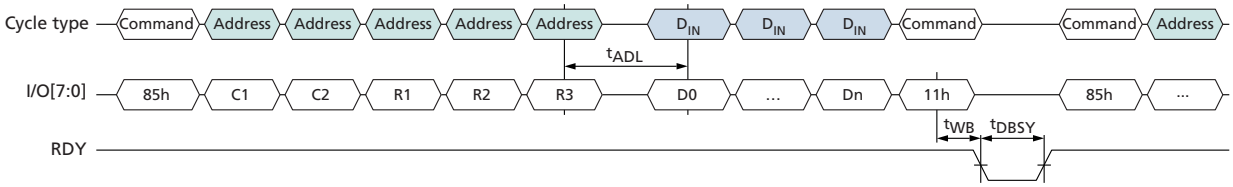
Figure 50: PROGRAM FOR INTERNAL DATA MOVE (85h-10h) with RANDOM DATA INPUT (85h)



PROGRAM FOR INTERNAL DATA MOVE TWO-PLANE (85h-11h)

The PROGRAM FOR INTERNAL DATA MOVE TWO-PLANE (85h-11h) command is functionally identical to the PROGRAM PAGE TWO-PLANE (85h-11h) command, except that when 85h is written to the command register, cache register contents are not cleared. See Program Operations for further details.

Figure 51: PROGRAM FOR INTERNAL DATA MOVE TWO-PLANE (85h-11h) Operation



Block Lock Feature

The block lock feature protects either the entire device or ranges of blocks from being programmed and erased. Using the block lock feature is preferable to using WP# to prevent PROGRAM and ERASE operations.

Block lock is enabled and disabled at power-on through the LOCK pin. At power-on, if LOCK is LOW, all BLOCK LOCK commands are disabled. However, if LOCK is HIGH at power-on, the BLOCK LOCK commands are enabled and, by default, all the blocks on the device are protected, or locked, from PROGRAM and ERASE operations, even if WP# is HIGH.

Before the contents of the device can be modified, the device must first be unlocked. Either a range of blocks or the entire device may be unlocked. PROGRAM and ERASE operations complete successfully only in the block ranges that have been unlocked. Blocks, once unlocked, can be locked again to protect them from further PROGRAM and ERASE operations.

Blocks that are locked can be protected further, or locked tight. When locked tight, the device's blocks can no longer be locked or unlocked.

WP# and Block Lock

The following is true when the block lock feature is enabled:

- Holding WP# LOW locks all blocks, provided the blocks are not locked tight.
- If WP# is held LOW to lock blocks, then returned to HIGH, a new UNLOCK command must be issued to unlock blocks.

UNLOCK (23h-24h)

By default at power-on, if LOCK is HIGH, all the blocks are locked and protected from PROGRAM and ERASE operations. The UNLOCK (23h) command is used to unlock a range of blocks. Unlocked blocks have no protection and can be programmed or erased.

The UNLOCK command uses two registers, a lower boundary block address register and an upper boundary block address register, and the invert area bit to determine what range of blocks are unlocked. When the invert area bit = 0, the range of blocks within the lower and upper boundary address registers are unlocked. When the invert area bit = 1, the range of blocks outside the boundaries of the lower and upper boundary address registers are unlocked. The lower boundary block address must be less than the upper boundary block address. The figures below show examples of how the lower and upper boundary address registers work with the invert area bit.

To unlock a range of blocks, issue the UNLOCK (23h) command followed by the appropriate address cycles that indicate the lower boundary block address. Then issue the 24h command followed by the appropriate address cycles that indicate the upper boundary block address. The least significant page address bit, PA0, should be set to 1 if setting the invert area bit; otherwise, it should be 0. The other page address bits should be 0.

Only one range of blocks can be specified in the lower and upper boundary block address registers. If after unlocking a range of blocks the UNLOCK command is again issued, the new block address range determines which blocks are unlocked. The previous unlocked block address range is not retained.

Figure 52: Flash Array Protected: Invert Area Bit = 0

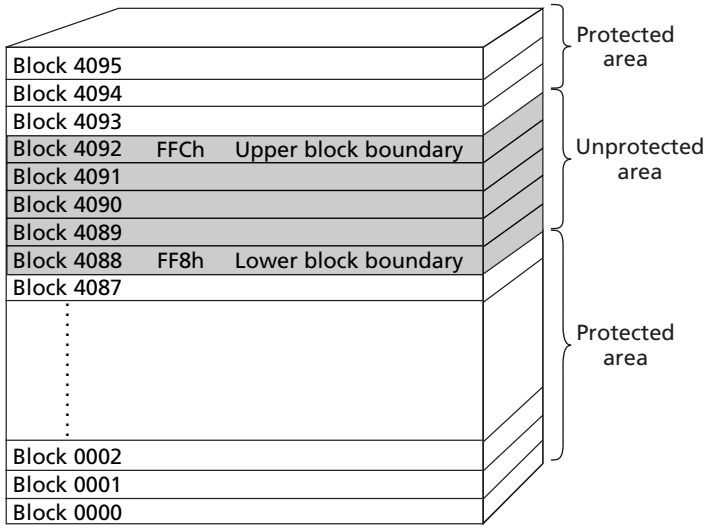


Figure 53: Flash Array Protected: Invert Area Bit = 1

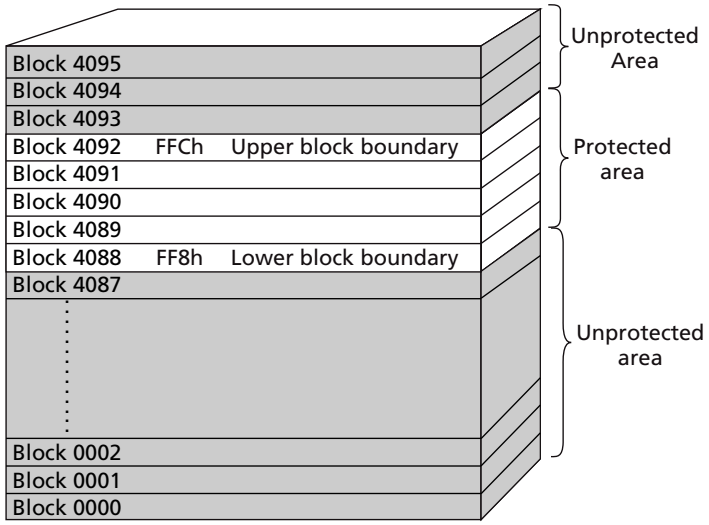
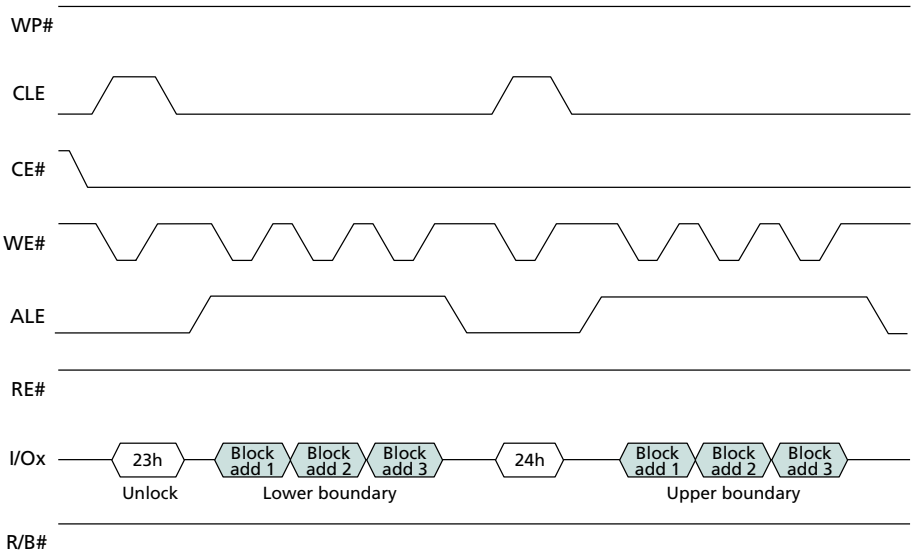


Table 24: Block Lock Address Cycle Assignments

ALE Cycle	I/O7[15:8]	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	BA7	BA6	LOW	LOW	LOW	LOW	LOW	Invert area bit[2]
Second	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Third	LOW	LOW	LOW	LOW	LOW	LOW	BA17	BA16

Notes: 1. I/O[15:8] is applicable only for x16 devices.
2. Invert area bit is applicable for 24h command; it may be LOW or HIGH for 23h command.

Figure 54: UNLOCK Operation



LOCK (2Ah)

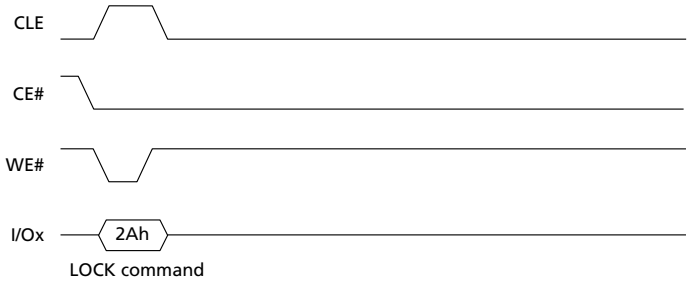
By default at power-on, if LOCK is HIGH, all the blocks are locked and protected from PROGRAM and ERASE operations. If portions of the device are unlocked using the UNLOCK (23h) command, they can be locked again using the LOCK (2Ah) command. The LOCK command locks all of the blocks in the device. Locked blocks are write-protected from PROGRAM and ERASE operations.

To lock all of the blocks in the device, issue the LOCK (2Ah) command.

When a PROGRAM or ERASE operation is issued to a locked block, R/B# goes LOW for ^{t}LBSY. The PROGRAM or ERASE operation does not complete. Any READ STATUS command reports bit 7 as 0, indicating that the block is protected.

The LOCK (2Ah) command is disabled if LOCK is LOW at power-on or if the device is locked tight.

Figure 55: LOCK Operation



LOCK TIGHT (2Ch)

The LOCK TIGHT (2Ch) command prevents locked blocks from being unlocked and also prevents unlocked blocks from being locked. When this command is issued, the UNLOCK (23h) and LOCK (2Ah) commands are disabled. This provides an additional level of protection against inadvertent PROGRAM and ERASE operations to locked blocks.

To implement LOCK TIGHT in all of the locked blocks in the device, verify that WP# is HIGH and then issue the LOCK TIGHT (2Ch) command.

When a PROGRAM or ERASE operation is issued to a locked block that has also been locked tight, R/B# goes LOW for ^{t}LBSY. The PROGRAM or ERASE operation does not complete. The READ STATUS (70h) command reports bit 7 as 0, indicating that the block is protected. PROGRAM and ERASE operations complete successfully to blocks that were not locked at the time the LOCK TIGHT command was issued.

After the LOCK TIGHT command is issued, the command cannot be disabled via a software command. Lock tight status can be disabled only by power cycling the device or toggling WP#. When the lock tight status is disabled, all of the blocks become locked, the same as if the LOCK (2Ah) command had been issued.

The LOCK TIGHT (2Ch) command is disabled if LOCK is LOW at power-on.

Figure 56: LOCK TIGHT Operation

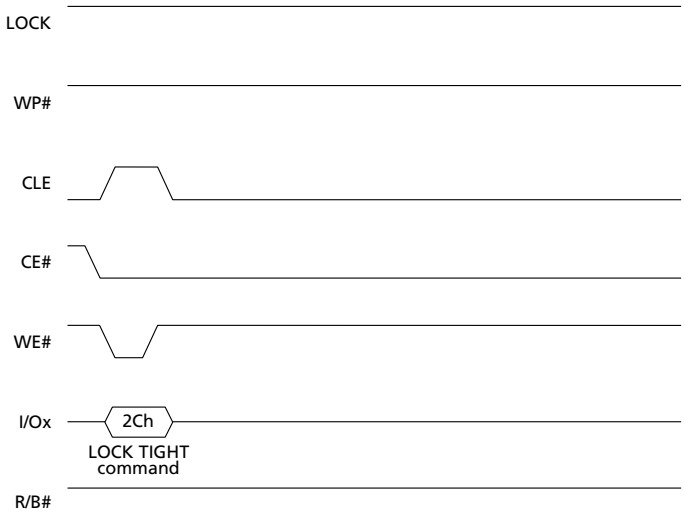
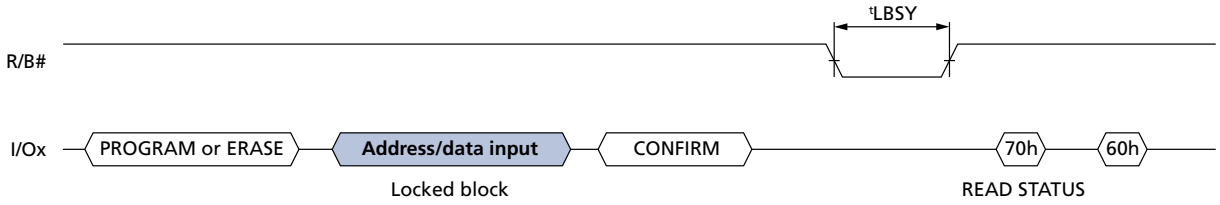


Figure 57: PROGRAM/ERASE Issued to Locked Block



BLOCK LOCK READ STATUS (7Ah)

The BLOCK LOCK READ STATUS (7Ah) command is used to determine the protection status of individual blocks. The address cycles have the same format, as shown below, and the invert area bit should be set LOW. On the falling edge of RE# the I/O pins output the block lock status register, which contains the information on the protection status of the block.

Table 25: Block Lock Status Register Bit Definitions

Block Lock Status Register Definitions	I/O[7:3]	I/O2 (Lock#)	I/O1 (LT#)	I/O0 (LT)
Block is locked tight	X	0	0	1
Block is locked	X	0	1	0
Block is unlocked, and device is locked tight	X	1	0	1
Block is unlocked, and device is not locked tight	X	1	1	0

Figure 58: BLOCK LOCK READ STATUS

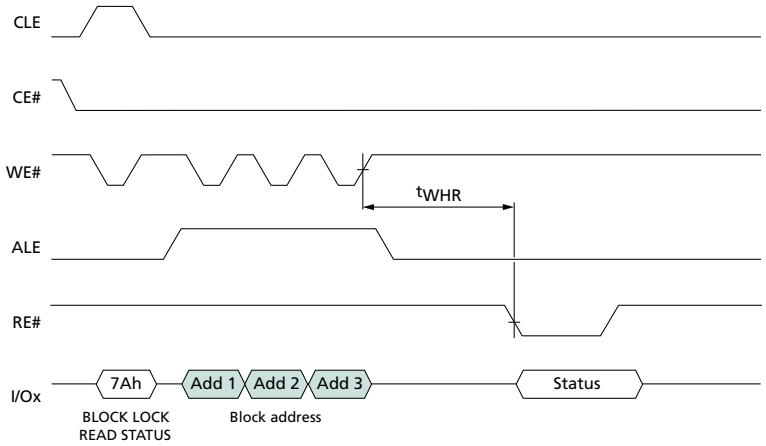
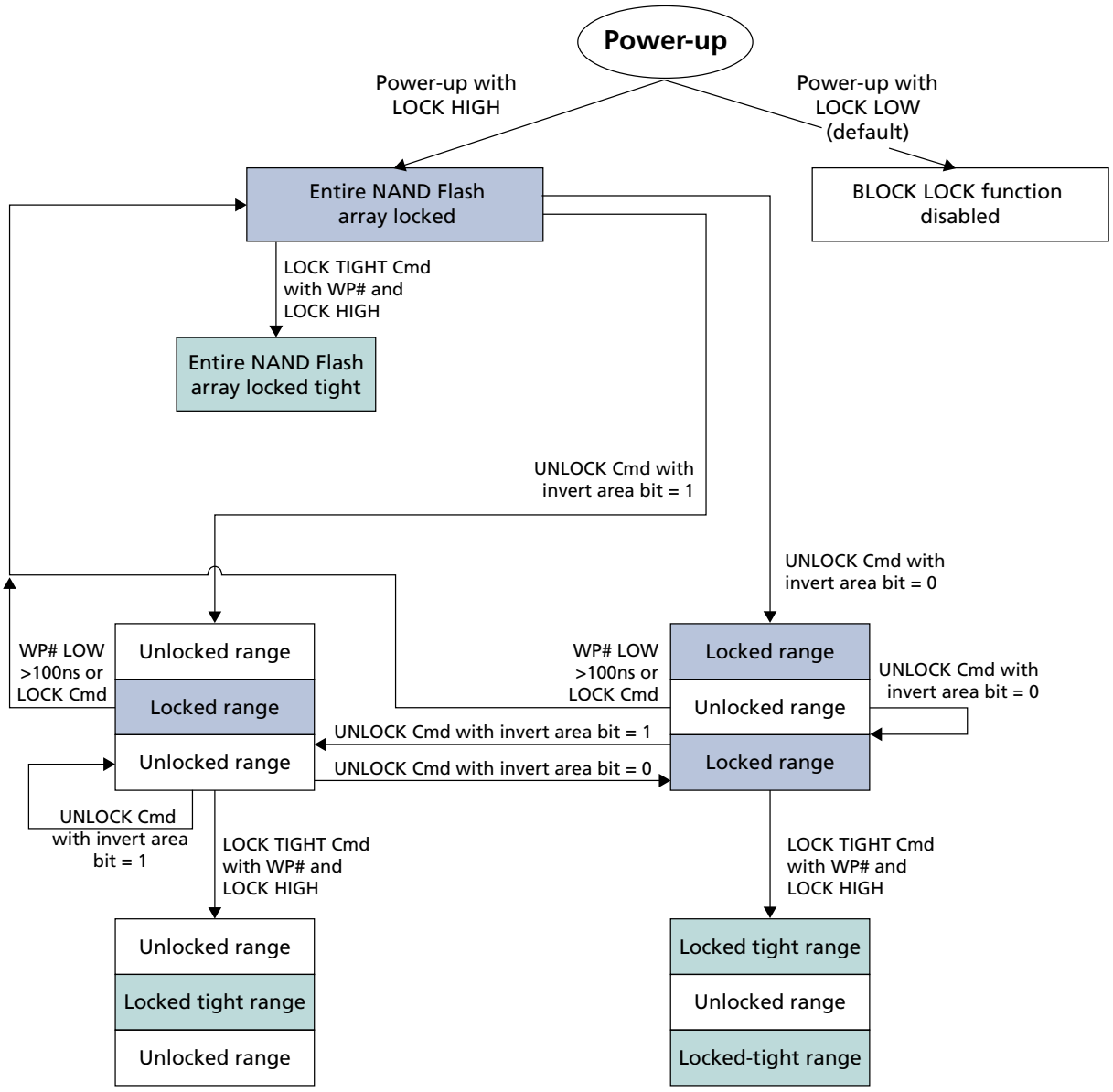


Figure 59: BLOCK LOCK Flowchart



One-Time Programmable (OTP) Operations

This Micron NAND Flash device offers a protected, one-time programmable NAND Flash memory area. Thirty full pages of OTP data are available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands. Customers can use the OTP area any way they choose; typical uses include programming serial numbers or other data for permanent storage.

The OTP area leaves the factory in an unwritten state (all bits are 1s). Programming or partial-page programming enables the user to program only 0 bits in the OTP area. The OTP area cannot be erased, whether it is protected or not. Protecting the OTP area prevents further programming of that area.

Micron provides a unique way to program and verify data before permanently protecting it and preventing future changes. The OTP area is only accessible while in OTP operation mode. To set the device to OTP operation mode, issue the SET FEATURE (EFh) command to feature address 90h and write 01h to P1, followed by three cycles of 00h to P2-P4. For parameters to enter OTP mode, see Features Operations.

When the device is in OTP operation mode, all subsequent PAGE READ (00h-30h) and PROGRAM PAGE (80h-10h) commands are applied to the OTP area. The OTP area is assigned to page addresses 02h-1Fh. To program an OTP page, issue the PROGRAM PAGE (80h-10h) command. The pages must be programmed in the ascending order. Similarly, to read an OTP page, issue the PAGE READ (00h-30h) command.

Protecting the OTP is done by entering OTP protect mode. To set the device to OTP protect mode, issue the SET FEATURE (EFh) command to feature address 90h and write 03h to P1, followed by three cycles of 00h to P2-P4.

To determine whether the device is busy during an OTP operation, either monitor R/B# or use the READ STATUS (70h) command.

To exit OTP operation or protect mode, write 00h to P1 at feature address 90h.

Legacy OTP Commands

For legacy OTP commands, OTP DATA PROGRAM (A0h-10h), OTP DATA PROTECT (A5h-10h), and OTP DATA READ (AFh-30h), refer to the MT29F4GxxAxC data sheet.

OTP DATA PROGRAM (80h-10h)

The OTP DATA PROGRAM (80h-10h) command is used to write data to the pages within the OTP area. An OTP page allows only four partial-page programs. There is no ERASE operation for OTP pages.

PROGRAM PAGE enables programming into an offset of an OTP page using two bytes of the column address (CA[12:0]). The command is compatible with the RANDOM DATA INPUT (85h) command. The PROGRAM PAGE command will not execute if the OTP area has been protected.

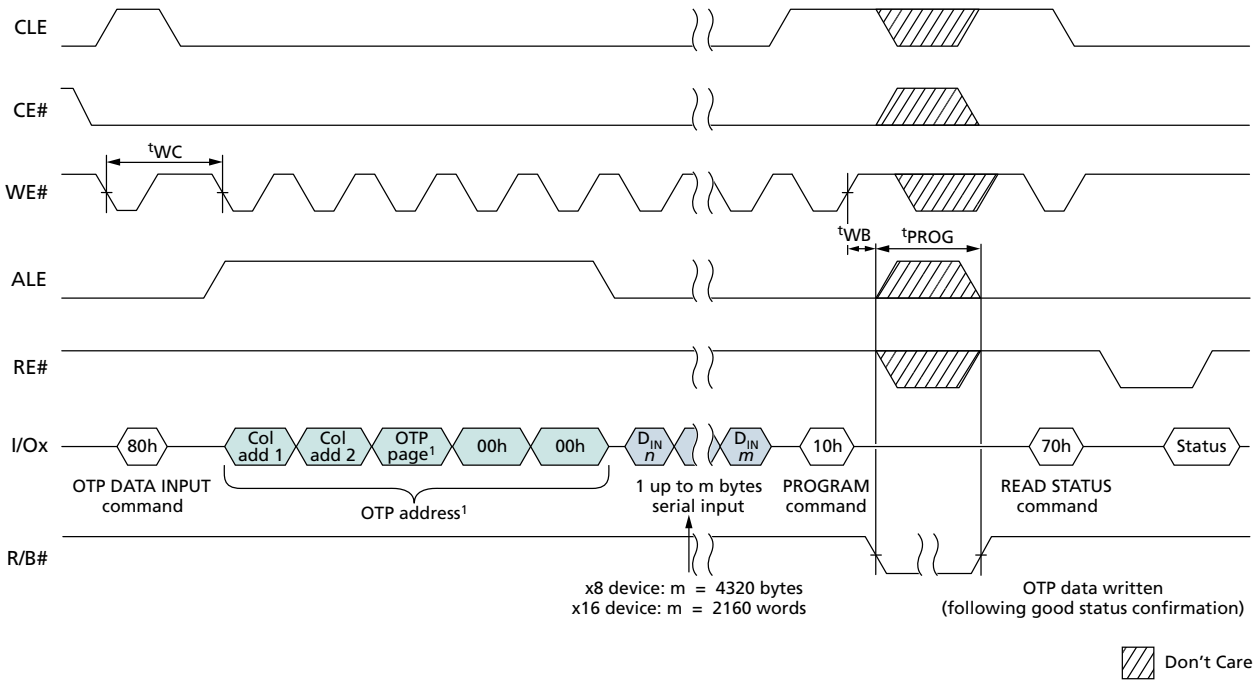
To use the PROGRAM PAGE command, issue the 80h command. Issue *n* address cycles. The first two address cycles are the column address. For the remaining cycles, select a page in the range of 02h-00h through 1Fh-00h. Next, write *n* bytes of data. After data input is complete, issue the 10h command. The internal control logic automatically executes the proper programming algorithm and controls the necessary timing for programming and verification.

R/B# goes LOW for the duration of the array programming time (^{t}PROG). The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. Bit 5 of the status register reflects the state of R/B#. When the device is ready, read bit 0 of the status register to determine whether the operation passed or failed (see Status Operations). Each OTP page can be programmed to 8 partial-page programming.

RANDOM DATA INPUT (85h)

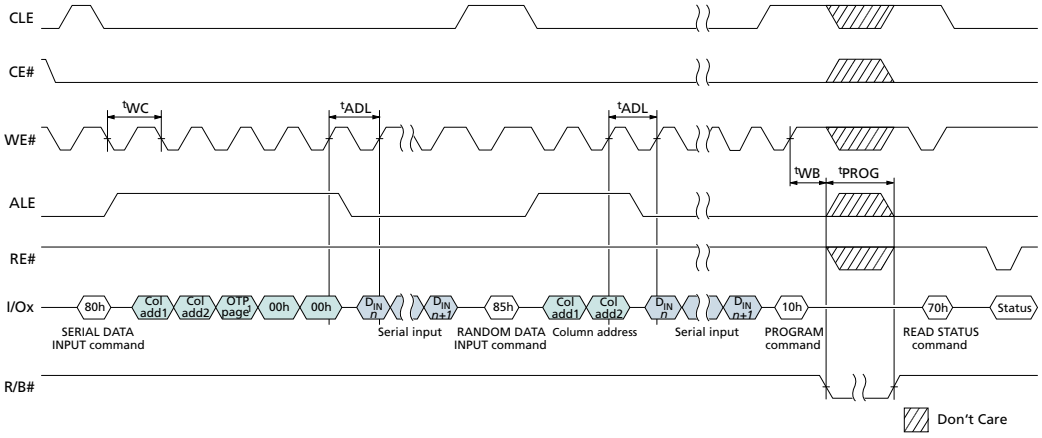
After the initial OTP data set is input, additional data can be written to a new column address with the RANDOM DATA INPUT (85h) command. The RANDOM DATA INPUT command can be used any number of times in the same page prior to the OTP PAGE WRITE (10h) command being issued.

Figure 60: OTP DATA PROGRAM (After Entering OTP Operation Mode)



Note: 1. The OTP page must be within the 02h–1Fh range.

Figure 61: OTP DATA PROGRAM Operation with RANDOM DATA INPUT (After Entering OTP Operation Mode)



OTP DATA PROTECT (80h-10)

The OTP area is protected on a block basis. To protect a block, set the device to OTP protect mode, then issue the PROGRAM PAGE (80h-10h) command and write OTP address 00h, 00h, 00h, 00h. To set the device to OTP protect mode, issue the SET FEATURE (EFh) command to 90h (feature address) and write 03h to P1, followed by three cycles of 00h to P2-P4.

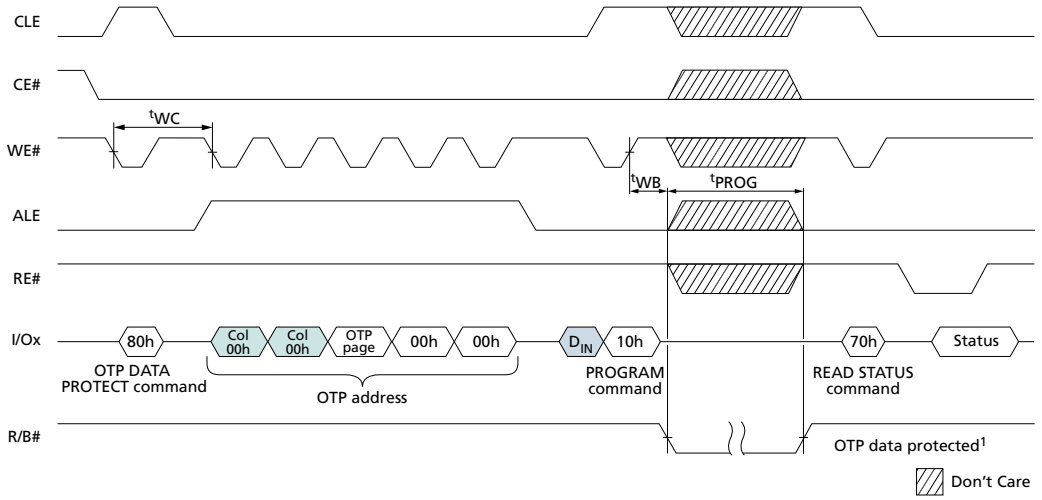
After the data is protected, it cannot be programmed further. When the OTP area is protected, the pages within the area are no longer programmable and cannot be unprotected.

To use the PROGRAM PAGE command to protect the OTP area, issue the 80h command, followed by *n* address cycles, write 00h data, data cycle of 00h, followed by the 10h command. (An example of the address sequence is shown in the following figure.) If an OTP DATA PROGRAM command is issued after the OTP area has been protected, R/B# will go LOW for tOBSY.

The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. Bit 5 of the status register reflects the state of R/B#.

When the device is ready, read bit 0 of the status register to determine whether the operation passed or failed (see Status Operations).

Figure 62: OTP DATA PROTECT Operation (After Entering OTP Protect Mode)



Note: 1. OTP data is protected following a good status confirmation.

OTP DATA READ (00h-30h)

To read data from the OTP area, set the device to OTP operation mode, then issue the PAGE READ (00h-30h) command. Data can be read from OTP pages within the OTP area whether the area is protected or not.

To use the PAGE READ command for reading data from the OTP area, issue the 00h command, and then issue five address cycles: for the first two cycles, the column address; and for the remaining address cycles, select a page in the range of 02h-00h-00h through 1Fh-00h-00h. Lastly, issue the 30h command. The PAGE READ CACHE MODE command is not supported on OTP pages.

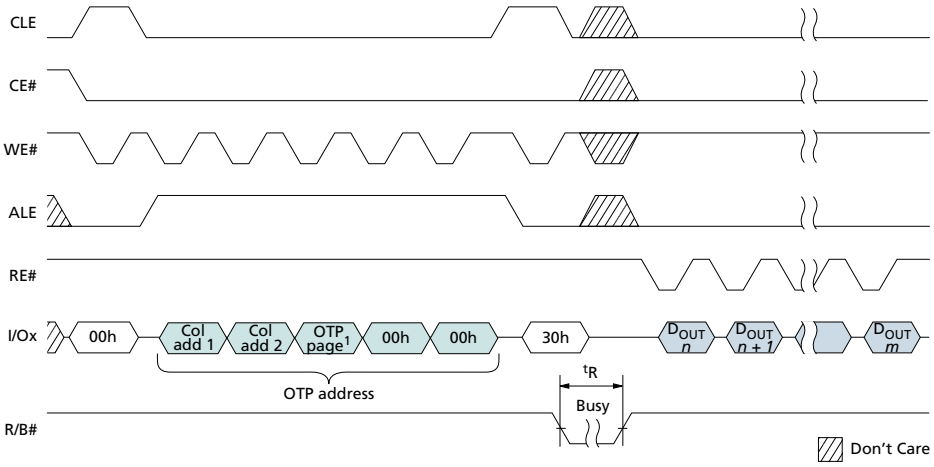
R/B# goes LOW (^{t}R) while the data is moved from the OTP page to the data register. The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. Bit 5 of the status register reflects the state of R/B# (see Status Operations).

Normal READ operation timings apply to OTP read accesses. Additional pages within the OTP area can be selected by repeating the OTP DATA READ command.

The PAGE READ command is compatible with the RANDOM DATA OUTPUT (05h-E0h) command.

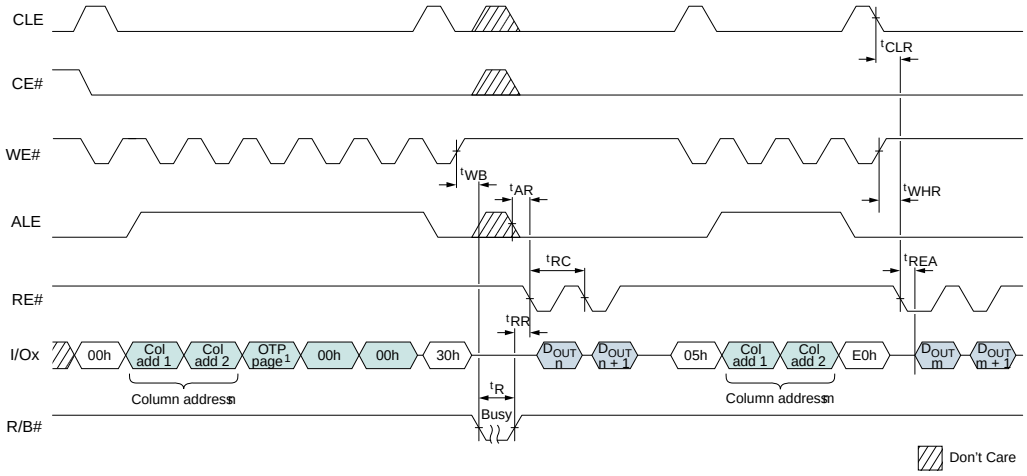
Only data on the current page can be read. Pulsing RE# outputs data sequentially.

Figure 63: OTP DATA READ



Note: 1. The OTP page must be within the 02h–1Fh range.

Figure 64: OTP DATA READ with RANDOM DATA READ Operation



Note: 1. The OTP page must be within the range 02h–1Fh.

Two-Plane Operations

Each NAND Flash logical unit (LUN) is divided into multiple physical planes. Each plane contains a cache register and a data register independent of the other planes. The planes are addressed via the low-order block address bits. Specific details are provided in Device and Array Organization.

Two-plane operations make better use of the NAND Flash arrays on these physical planes by performing concurrent READ, PROGRAM, or ERASE operations on multiple planes, significantly improving system performance. Two-plane operations must be of the same type across the planes; for example, it is not possible to perform a PROGRAM operation on one plane with an ERASE operation on another.

When issuing two-plane program or erase operations, use the READ STATUS (70h) command and check whether the previous operation(s) failed. If the READ STATUS (70h) command indicates that an error occurred (FAIL = 1 and/or FAILC = 1), use the READ STATUS ENHANCED (78h) command to determine which plane operation failed.

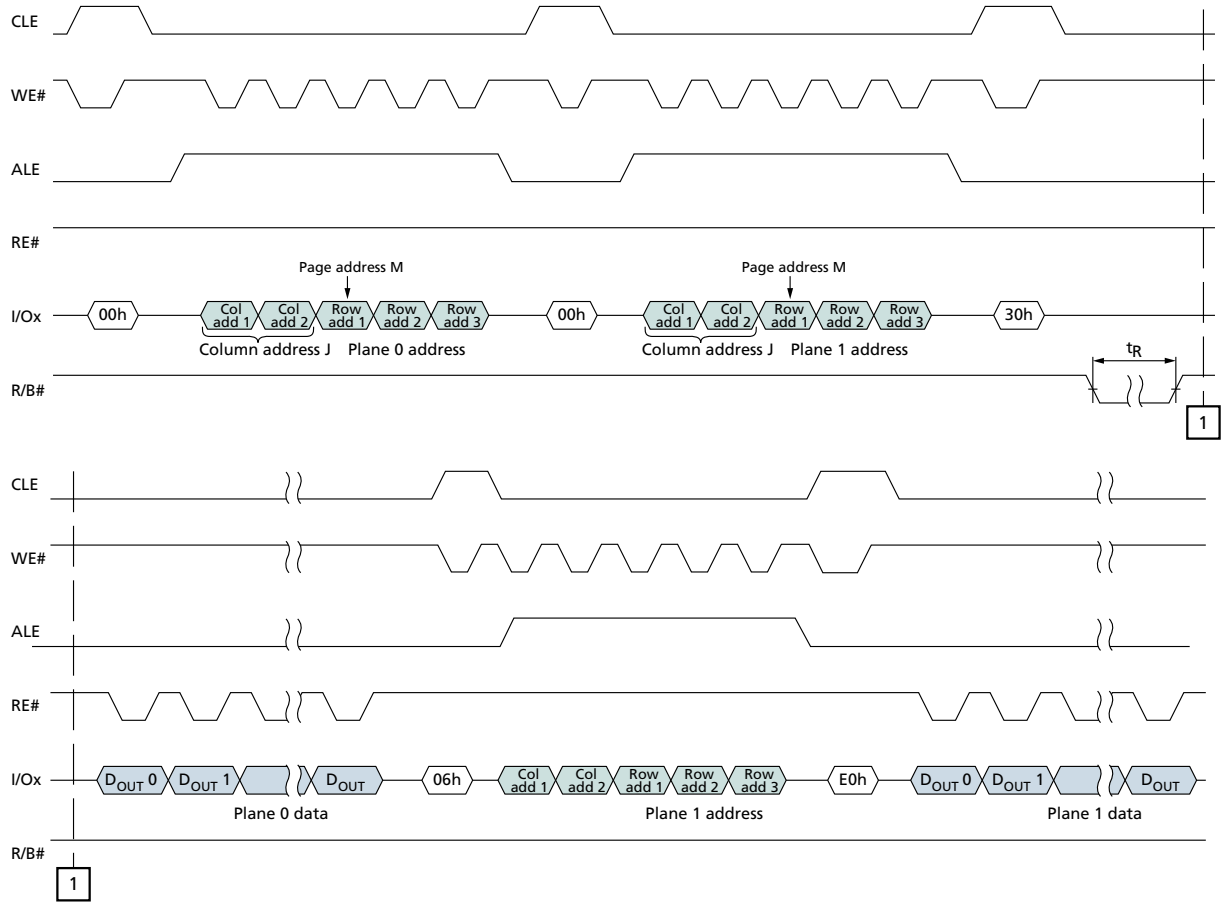
Two-Plane Addressing

Two-plane commands require multiple, five-cycle addresses, one address per operational plane. For a given two-plane operation, these addresses are subject to the following requirements:

- The LUN address bit(s) must be identical for all of the issued addresses.
- The plane select bit, BA[6], must be different for each issued address.
- The page address bits, PA[5:0], must be identical for each issued address.

The READ STATUS (70h) command should be used following two-plane program page and erase block operations on a single die (LUN).

Figure 65: TWO-PLANE PAGE READ



Notes: 1. Column and page addresses must be the same.
2. The least significant block address bit, BA6, must be different for the first- and second-plane addresses.

Figure 66: TWO-PLANE PAGE READ with RANDOM DATA READ

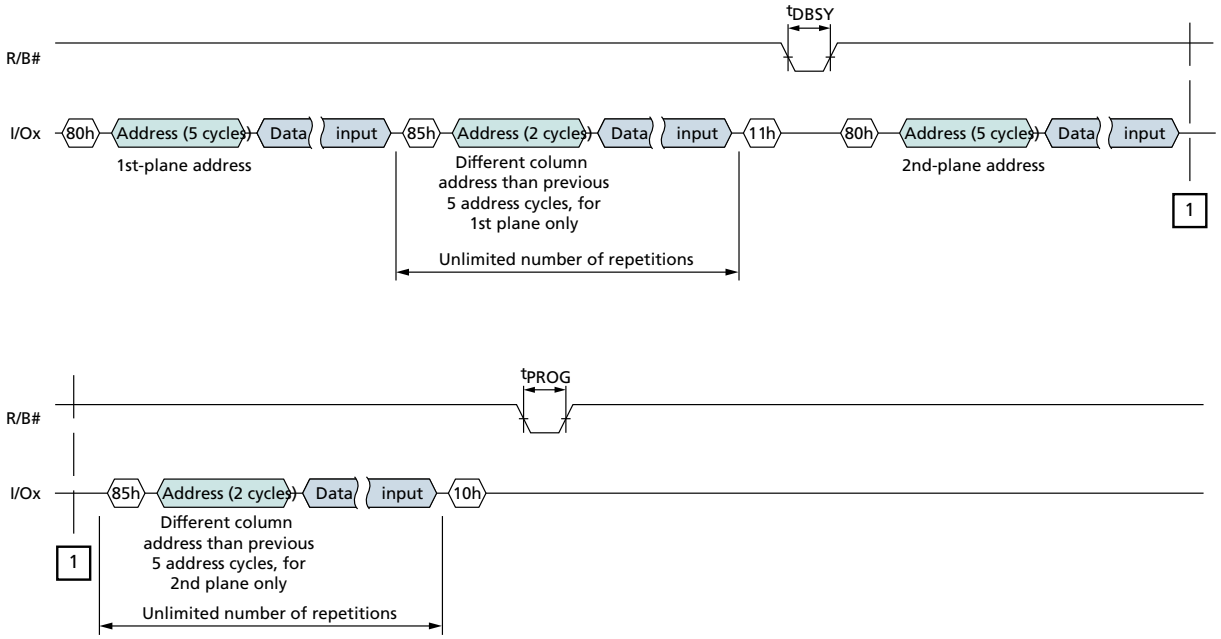


Figure 67: TWO-PLANE PROGRAM PAGE

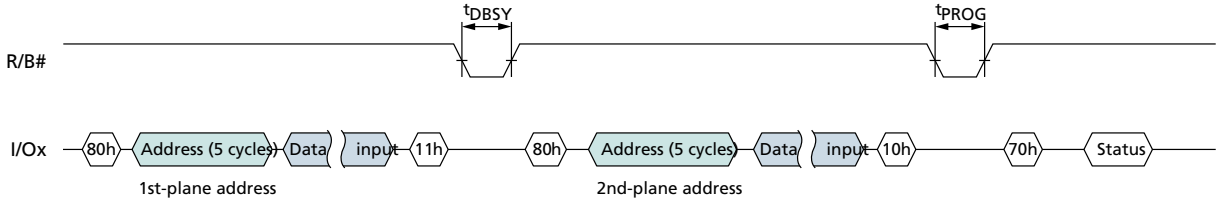


Figure 68: TWO-PLANE PROGRAM PAGE with RANDOM DATA INPUT

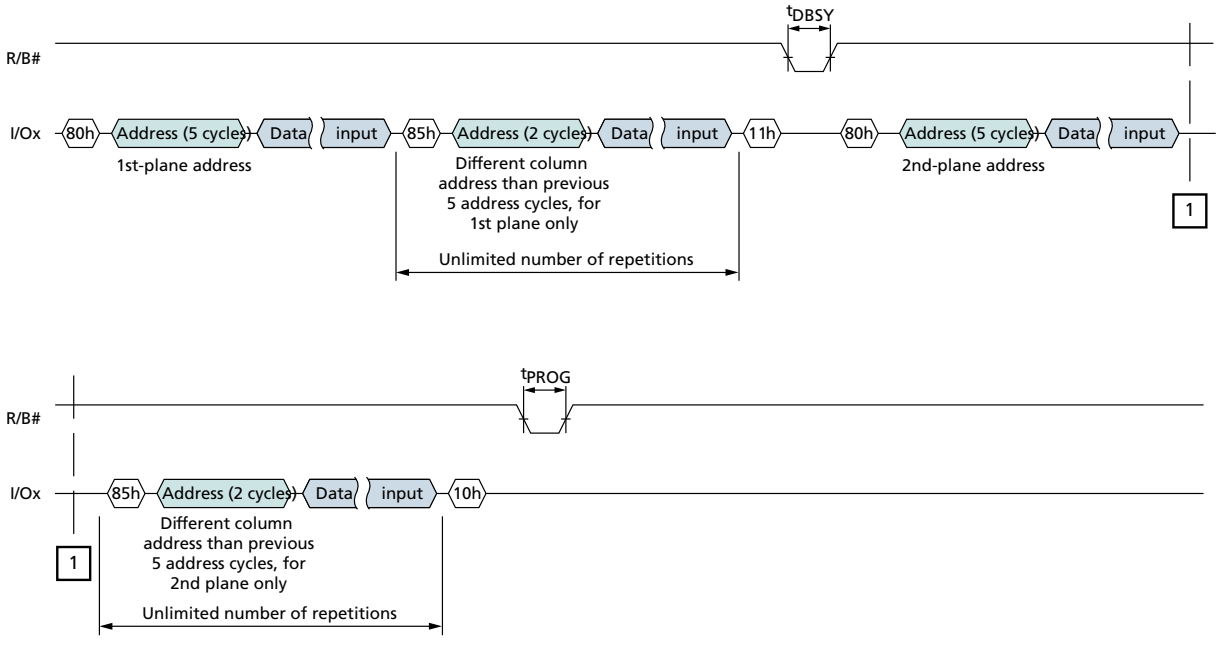


Figure 69: TWO-PLANE PROGRAM PAGE CACHE MODE

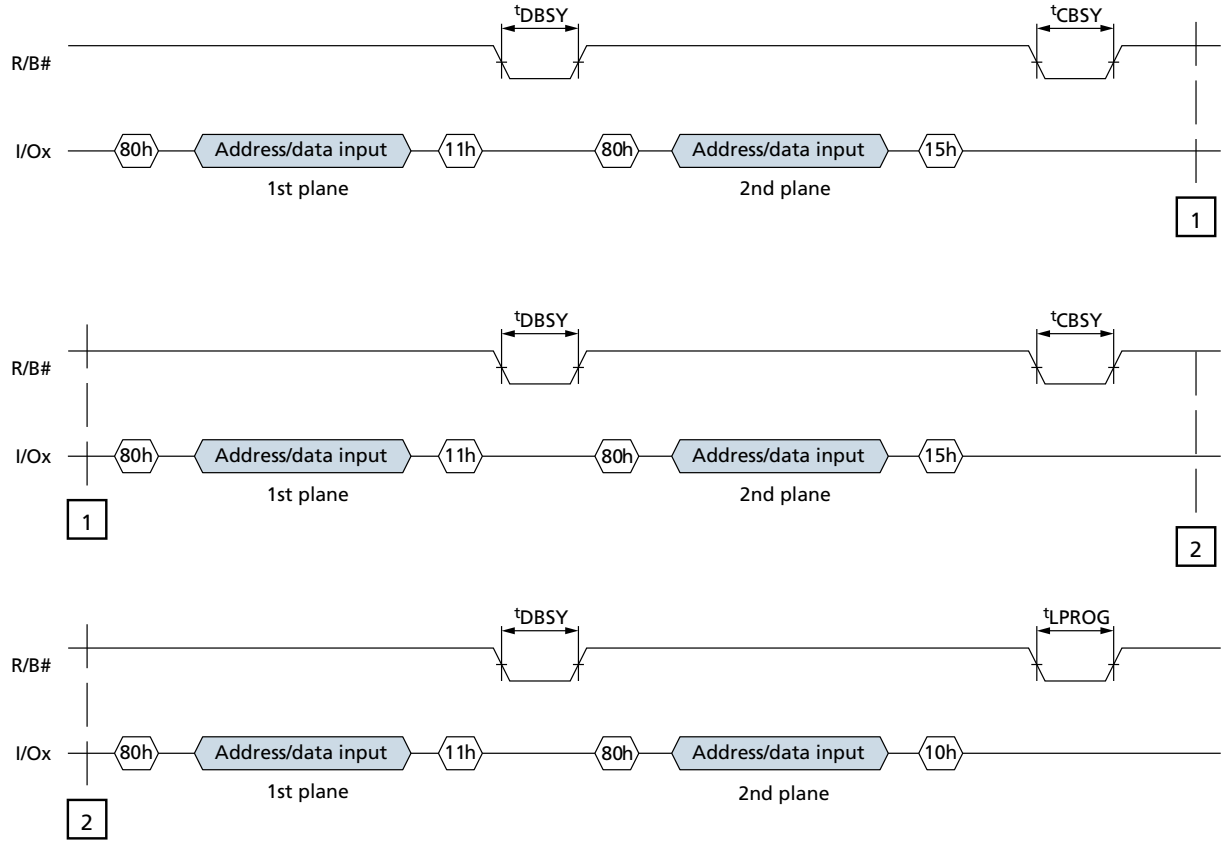


Figure 70: TWO-PLANE INTERNAL DATA MOVE

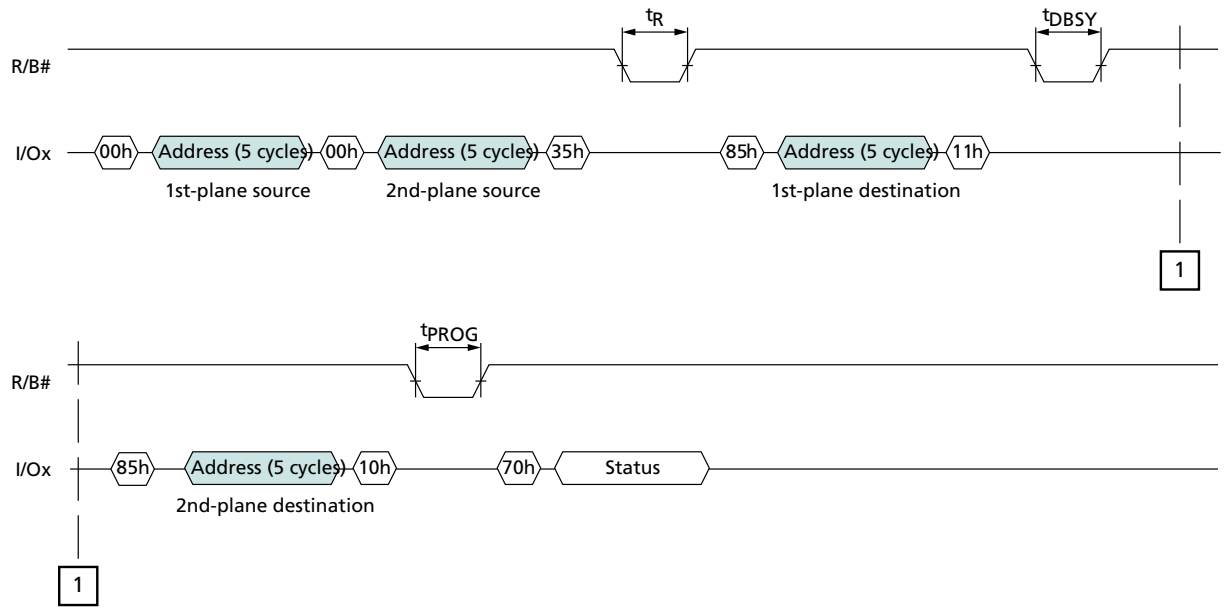


Figure 71: TWO-PLANE INTERNAL DATA MOVE with TWO-PLANE RANDOM DATA READ

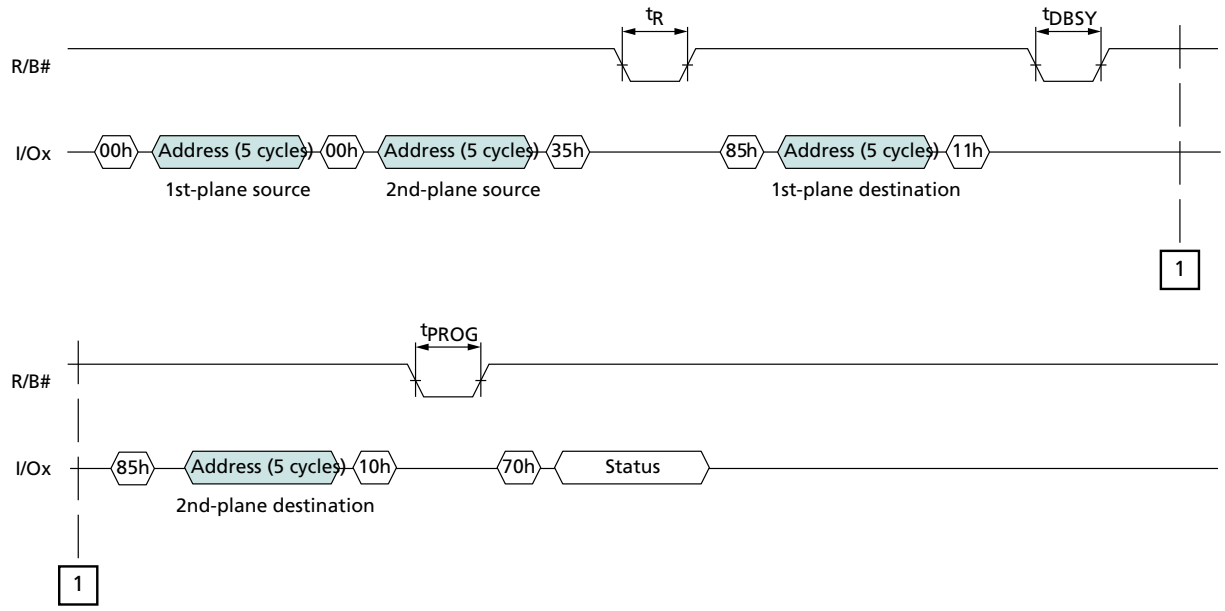


Figure 72: TWO-PLANE INTERNAL DATA MOVE with RANDOM DATA INPUT

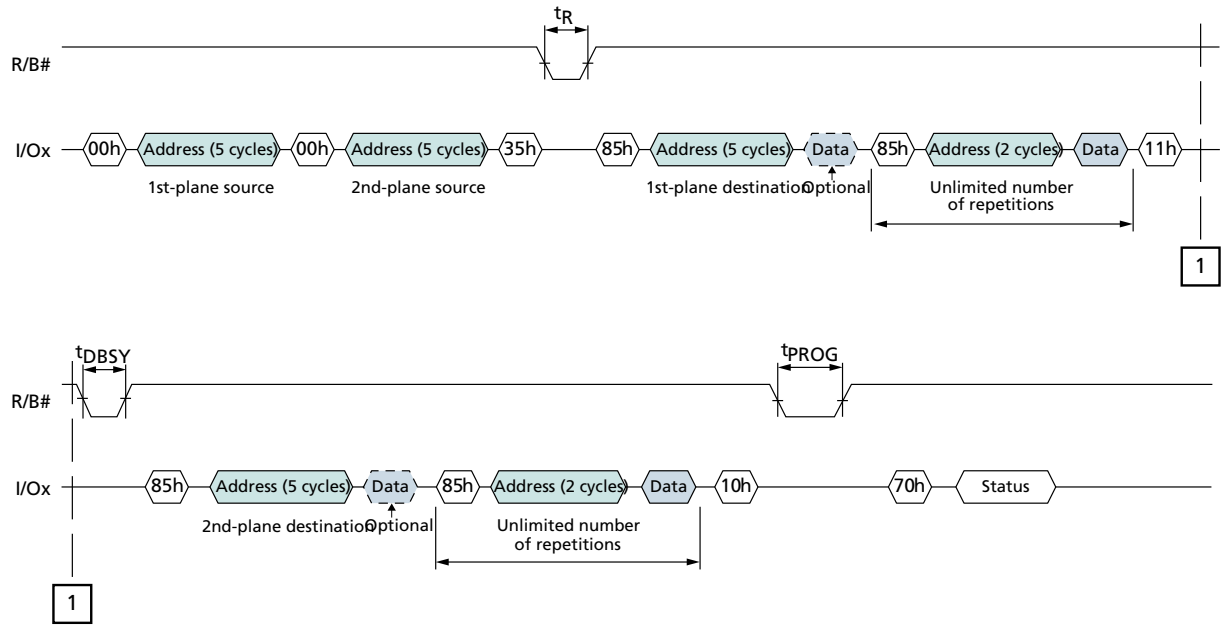


Figure 73: TWO-PLANE BLOCK ERASE

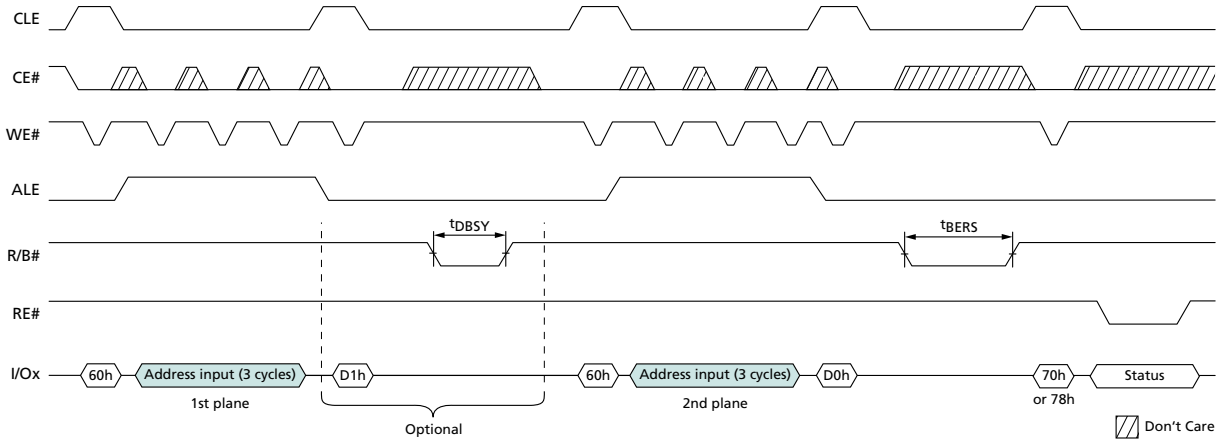
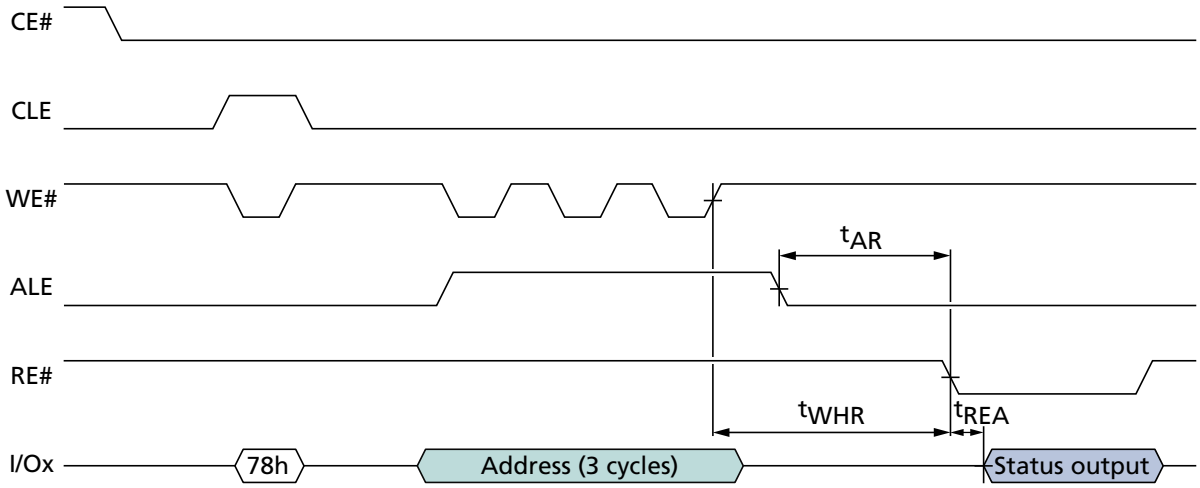


Figure 74: TWO-PLANE/MULTIPLE-DIE READ STATUS Cycle



Interleaved Die (Multi-LUN) Operations

In devices that have more than one die (LUN) per target, it is possible to improve performance by interleaving operations between the die (LUNs). An interleaved die (multi-LUN) operation is one that is issued to an idle die (LUN) (RDY = 1) while another die (LUN) is busy (RDY = 0).

Interleaved die (multi-LUN) operations are prohibited following RESET (FFh), identification (90h, ECh, EDh), and configuration (EEh, EFh) operations until ARDY =1 for all of the die (LUNs) on the target.

During an interleaved die (multi-LUN) operation, there are two methods to determine operation completion. The R/B# signal indicates when all of the die (LUNs) have finished their operations. R/B# remains LOW while any die (LUN) is busy. When R/B# goes HIGH, all of the die (LUNs) are idle and the operations are complete. Alternatively, the READ STATUS ENHANCED (78h) command can report the status of each die (LUN) individually.

If a die (LUN) is performing a cache operation, like PROGRAM PAGE CACHE (80h-15h), then the die (LUN) is able to accept the data for another cache operation when status register bit 6 is 1. All operations, including cache operations, are complete on a die when status register bit 5 is 1.

During and following interleaved die (multi-LUN) operations, the READ STATUS (70h) command is prohibited. Instead, use the READ STATUS ENHANCED (78h) command to monitor status. This command selects which die (LUN) will report status. When two-plane commands are used with interleaved die (multi-LUN) operations, the two-plane commands must also meet the requirements in Two-Plane Operations.

See Command Definitions for the list of commands that can be issued while other die (LUNs) are busy.

During an interleaved die (multi-LUN) operation that involves a PROGRAM series (80h-10h, 80h-15h) operation and a READ operation, the PROGRAM series operation must be issued before the READ series operation. The data from the READ series operation must be output to the host before the next PROGRAM series operation is issued. This is because the 80h command clears the cache register contents of all cache registers on all planes.

Error Management

Table 26: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB) per LUN	4016
Total available blocks per LUN	4096
First spare area location	x8: byte 4096 x16: word 2048
Bad block mark	x8: 00h x16: 0000h
Minimum required ECC	8-bit ECC per 540 bytes of data

Electrical Specifications

Stresses greater than those listed can cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

Table 27: Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}

Parameter/Condition		Symbol	Min	Max	Unit
Voltage input	1.8V	V_{IN}	–0.6	2.4	V
	3.3V		–0.6	4.6	V
V_{CC} supply voltage	1.8V	V_{CC}	–0.6	2.4	V
	3.3V		–0.6	4.6	V
Storage temperature		T_{STG}	–65	150	°C
Short circuit output current, I/Os		–	–	5	mA

Table 28: Recommended Operating Conditions

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	T_A	0	–	70	°C
	Extended		–40	–	85	°C
V_{CC} supply voltage	1.8V	V_{CC}	1.7	1.8	1.95	V
	3.3V		2.7	3.3	3.6	V
Ground supply voltage		V_{SS}	0	0	0	V

Table 29: Valid Blocks

Note 1 applies to all

Parameter	Symbol	Device	Min	Max	Unit	Notes
Valid block number	NVB	MT29F8G	4016	4096	Blocks	2
		MT29F16G	8032	8192	Blocks	2,3

Notes: 1. Invalid blocks are blocks that contain one or more bad bits. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid by the factory.
2. Block 00h (the first block) is guaranteed to be valid with ECC when shipped from the factory.
3. Each 8Gb section has a maximum of 80 invalid blocks.

Table 30: Capacitance

Description	Symbol	Max	Unit	Notes
Input capacitance	C_{IN}	10	pF	1,2
Input/output capacitance (I/O)	C_{IO}	10	pF	1,2

Notes: 1. These parameters are verified in device characterization and are not 100% tested.
2. Test conditions: T_C = 25°C; f = 1 MHz; Vin = 0V.

Table 31: Test Conditions

Parameter	Value	Notes
Input pulse levels	0.0V to V_{CC}	
Input rise and fall times	5ns	
Input and output timing levels	$V_{CC}/2$	
Output load	1 TTL GATE and CL = 30pF (1.8V)	1
	1 TTL GATE and CL = 50pF (3.3V)	
Output load	1 TTL GATE and CL = 30pF (1.8V)	1
	1 TTL GATE and CL = 50pF (3.3V)	

Note: 1. Verified in device characterization, not 100% tested.

Electrical Specifications – DC Characteristics and Operating Conditions

Table 32: DC Characteristics and Operating Conditions (3.3V)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Sequential READ current	$^{t}RC = {}^{t}RC$ (MIN); CE# = V_{IL}; I_{OUT} = 0mA	I_{CC1}	–	25	35	mA	
PROGRAM current	–	I_{CC2}	–	25	35	mA	
ERASE current	–	I_{CC3}	–	25	35	mA	
Standby current (TTL)	CE# = V_{IH}; WP# = 0V/V_{CC}	I_{SB1}	–	–	1	mA	
Standby current (CMOS)	CE# = V_{CC} - 0.2V; WP# = 0V/V_{CC}	I_{SB2}	–	20	100	µA	
Staggered power-up current	Rise time = 1ms Line capacitance = 0.1µF	I_{ST}	–	–	10 per die	mA	1
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	–	–	±10	µA	
Output leakage current	V_{OUT} = 0V to V_{CC}	I_{LO}	–	–	±10	µA	
Input high voltage	I/O[7:0], I/O[15:0], CE#, CLE, ALE, WE#, RE#, WP#, R/B#	V_{IH}	0.8 x V_{CC}	–	V_{CC} + 0.3	V	
Input low voltage, all inputs	–	V_{IL}	–0.3	–	0.2 x V_{CC}	V	
Output high voltage	I_{OH} = –400µA	V_{OH}	0.67 x V_{CC}	–	–	V	2
Output low voltage	I_{OL} = 2.1mA	V_{OL}	–	–	0.4	V	2
Output low current	V_{OL} = 0.4V	I_{OL} (R/B#)	8	10	–	mA	3

Notes: 1. Measurement is taken with 1ms averaging intervals and begins after V_{CC} reaches V_{CC} (MIN).
2. I_{OL} (R/B#) may need to be relaxed if R/B pull-down strength is not set to full.
3. V_{OH} and V_{OL} may need to be relaxed if I/O drive strength is not set to full.

Table 33: DC Characteristics and Operating Conditions (1.8V)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Sequential READ current	$^{t}RC = {}^{t}RC$ (MIN); CE# = V_{IL}; I_{OUT} = 0mA	I_{CC1}	–	10	20	mA	1,2
PROGRAM current	–	I_{CC2}	–	10	20	mA	1,2
ERASE current	–	I_{CC3}	–	10	20	mA	1,2
Standby current (TTL)	CE# = V_{IH}; LOCK = WP# = 0V/V_{CC}	I_{SB1}	–	–	1	mA	
Standby current (CMOS)	CE# = V_{CC} - 0.2V; LOCK = WP# = 0V/V_{CC}	I_{SB2}	–	10	50	µA	
Staggered power-up current	Rise time = 1ms Line capacitance = 0.1µF	I_{ST}	–	–	10 per die	mA	3
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	–	–	±10	µA	
Output leakage current	V_{OUT} = 0V to V_{CC}	I_{LO}	–	–	±10	µA	
Input high voltage	I/O[7:0], I/O[15:0], CE#, CLE, ALE, WE#, RE#, WP#, R/B#, LOCK	V_{IH}	0.8 x V_{CC}	–	V_{CC} + 0.3	V	
Input low voltage, all inputs	–	V_{IL}	–0.3	–	0.2 x V_{CC}	V	
Output high voltage	I_{OH} = –100µA	V_{OH}	V_{CC} - 0.1	–	–	V	4
Output low voltage	I_{OL} = 100µA	V_{OL}	–	–	0.1	V	4
Output low current	V_{OL} = 0.2V	I_{OL} (R/B#)	3	4	–	mA	5

Notes: 1. Typical and maximum values are for single-plane operation only. Dual-plane operation values are 20mA (TYP) and 40mA (MAX).
2. Values are for single die operations. Values could be higher for interleaved die operations.
3. Measurement is taken with 1ms averaging intervals and begins after V_{CC} reaches V_{CC} (MIN).
4. Test conditions for V_{OH} and V_{OL}.
5. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full.

Electrical Specifications – AC Characteristics and Operating Conditions

Table 34: AC Characteristics: Command, Data, and Address Input (3.3V)

Parameter	Symbol	Min	Max	Unit	Notes
ALE to data start	tADL	70	–	ns	1
ALE hold time	tALH	5	–	ns	
ALE setup time	tALS	10	–	ns	
CE# hold time	tCH	5	–	ns	
CLE hold time	tCLH	5	–	ns	
CLE setup time	tCLS	10	–	ns	
CE# setup time	tCS	15	–	ns	
Data hold time	tDH	5	–	ns	
Data setup time	tDS	7	–	ns	
WRITE cycle time	tWC	20	–	ns	1
WE# pulse width HIGH	tWH	7	–	ns	1
WE# pulse width	tWP	10	–	ns	1
WP# transition to WE# LOW	tWW	100	–	ns	

Note: 1. Timing for tADL begins in the address cycle, on the final rising edge of WE#, and ends with the first rising edge of WE# for data input.

Table 35: AC Characteristics: Command, Data, and Address Input (1.8V)

Parameter	Symbol	Min	Max	Unit	Notes
ALE to data start	tADL	100	–	ns	1
ALE hold time	tALH	5	–	ns	
ALE setup time	tALS	10	–	ns	
CE# hold time	tCH	5	–	ns	
CLE hold time	tCLH	5	–	ns	
CLE setup time	tCLS	10	–	ns	
CE# setup time	tCS	25	–	ns	
Data hold time	tDH	5	–	ns	
Data setup time	tDS	10	–	ns	
WRITE cycle time	tWC	30	–	ns	1
WE# pulse width HIGH	tWH	10	–	ns	1
WE# pulse width	tWP	15	–	ns	1
WP# transition to WE# LOW	tWW	100	–	ns	

Note: 1. Timing for tADL begins in the address cycle on the final rising edge of WE#, and ends with the first rising edge of WE# for data input.

Table 36: AC Characteristics: Normal Operation (1.8V)

Note 1 applies to all

Parameter	Symbol	Min	Max	Unit	Notes
ALE to RE# delay	^{t}AR	10	–	ns	
CE# access time	^{t}CEA	–	30	ns	
CE# HIGH to output High-Z	^{t}CHZ	–	50	ns	2
CLE to RE# delay	^{t}CLR	10	–	ns	
CE# HIGH to output hold	^{t}COH	15	–	ns	
Output High-Z to RE# LOW	^{t}IR	0	–	ns	
READ cycle time	^{t}RC	30	–	ns	
RE# access time	^{t}REA	–	25	ns	
RE# HIGH hold time	^{t}REH	10	–	ns	
RE# HIGH to output hold	^{t}RHOH	15	–	ns	
RE# HIGH to WE# LOW	^{t}RHW	100	–	ns	
RE# HIGH to output High-Z	^{t}RHZ	–	65	ns	2
RE# pulse width	^{t}RP	15	–	ns	
Ready to RE# LOW	^{t}RR	20	–	ns	
Reset time (READ/PROGRAM/ERASE)	^{t}RST	–	5/10/500	µs	3
WE# HIGH to busy	^{t}WB	–	100	ns	4
WE# HIGH to RE# LOW	^{t}WHR	80	–	ns	

Notes: 1. AC characteristics may need to be relaxed if I/O drive strength is not set to full.
2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100% tested.
3. The first time the RESET (FFh) command is issued while the device is idle, the device will be busy for a maximum of 1ms. Thereafter, the device is busy for a maximum of 5µs.
4. Do not issue a new command during ^{t}WB, even if R/B# is ready.

Table 37: AC Characteristics: Normal Operation (3.3V)

Note 1 applies to all

Parameter	Symbol	Min	Max	Unit	Notes
ALE to RE# delay	^{t}AR	10	–	ns	
CE# access time	^{t}CEA	–	25	ns	
CE# HIGH to output High-Z	^{t}CHZ	–	30	ns	2
CLE to RE# delay	^{t}CLR	10	–	ns	
CE# HIGH to output hold	^{t}COH	15	–	ns	
Output High-Z to RE# LOW	^{t}IR	0	–	ns	
READ cycle time	^{t}RC	20	–	ns	
RE# access time	^{t}REA	–	16	ns	
RE# HIGH hold time	^{t}REH	7	–	ns	
RE# HIGH to output hold	^{t}RHOH	15	–	ns	
RE# HIGH to WE# LOW	^{t}RHW	100	–	ns	2
RE# HIGH to output High-Z	^{t}RHZ	–	100	ns	
RE# LOW to output hold	^{t}RLOH	5	–	ns	
RE# pulse width	^{t}RP	10	–	ns	
Ready to RE# LOW	^{t}RR	20	–	ns	
Reset time (READ/PROGRAM/ERASE)	^{t}RST	–	5/10/500	µs	3
WE# HIGH to busy	^{t}WB	–	100	ns	4
WE# HIGH to RE# LOW	^{t}WHR	60	–	ns	

Notes: 1. AC characteristics may need to be relaxed if I/O drive strength is not set to “full.”
2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100% tested.
3. The first time the RESET (FFh) command is issued while the device is idle, the device will go busy for a maximum of 1ms. Thereafter, the device goes busy for a maximum of 5µs.
4. Do not issue a new command during ^{t}WB, even if R/B# is ready.

Electrical Specifications – Program/Erase Characteristics

Table 38: Program/Erase Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial-page programs	NOP	–	4	cycles	1
BLOCK ERASE operation time	^{t}BERS	2	10	ms	2
Busy time for PROGRAM CACHE operation	^{t}CBSY	3	600	µs	3
Busy time for TWO-PLANE PROGRAM PAGE or TWO-PLANE BLOCK ERASE operation	^{t}DBSY	0.5	1	µs	
Cache read busy time	^{t}RCBSY	3	25	µs	
Busy time for SET FEATURES and GET FEATURES operations	^{t}FEAT	–	1	µs	
LAST PAGE PROGRAM operation time	^{t}LPROG	–	–	–	4
Busy time for OTP DATA PROGRAM operation if OTP is protected	^{t}OBSY	–	30	µs	
Busy time for PROGRAM/ERASE on locked blocks	^{t}LBSY	–	3	µs	
PROGRAM PAGE operation time	^{t}PROG	200	600	µs	2
Power-on reset time	^{t}POR	–	1	ms	
READ PAGE operation time	^{t}R	–	25	µs	

Notes: 1. Four total partial-page programs to the same page.
2. Typical ^{t}PROG and ^{t}BERS time may increase for two-plane operations.
3. ^{t}CBSY MAX time depends on timing between internal program completion and data-in.
4. ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last - 1 page) - command load time (last page) - address load time (last page) - data load time (last page).

Asynchronous Interface Timing Diagrams

Figure 75: RESET Operation

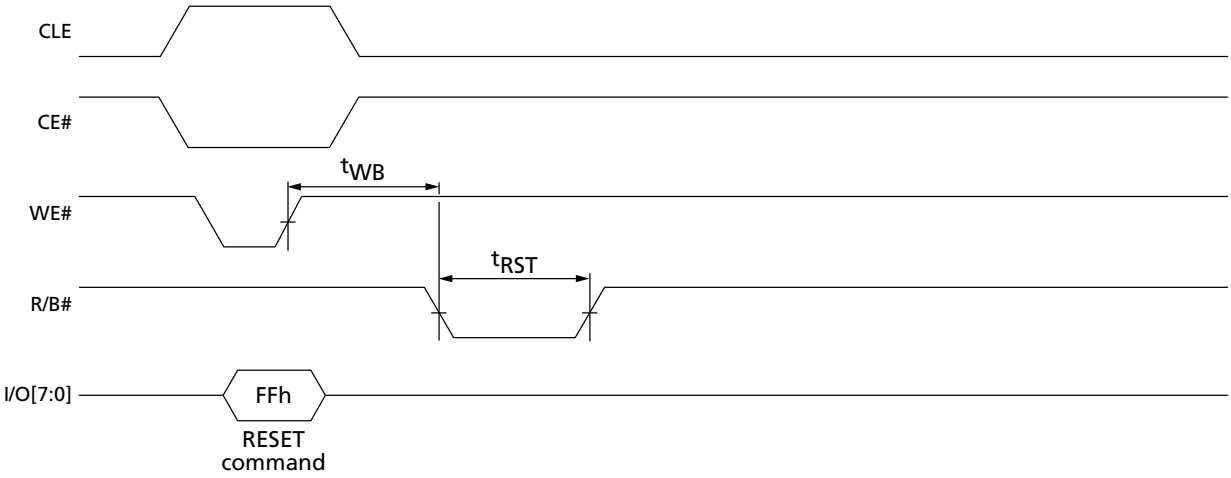


Figure 76: READ STATUS Cycle

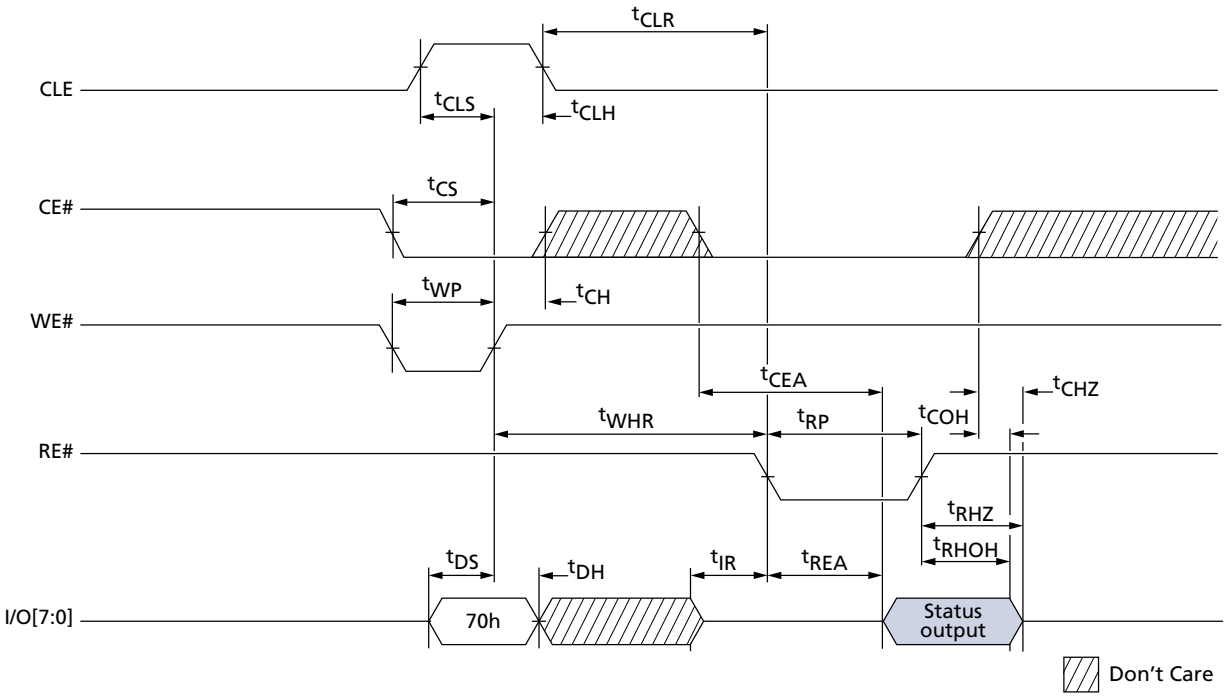


Figure 77: READ STATUS ENHANCED Cycle

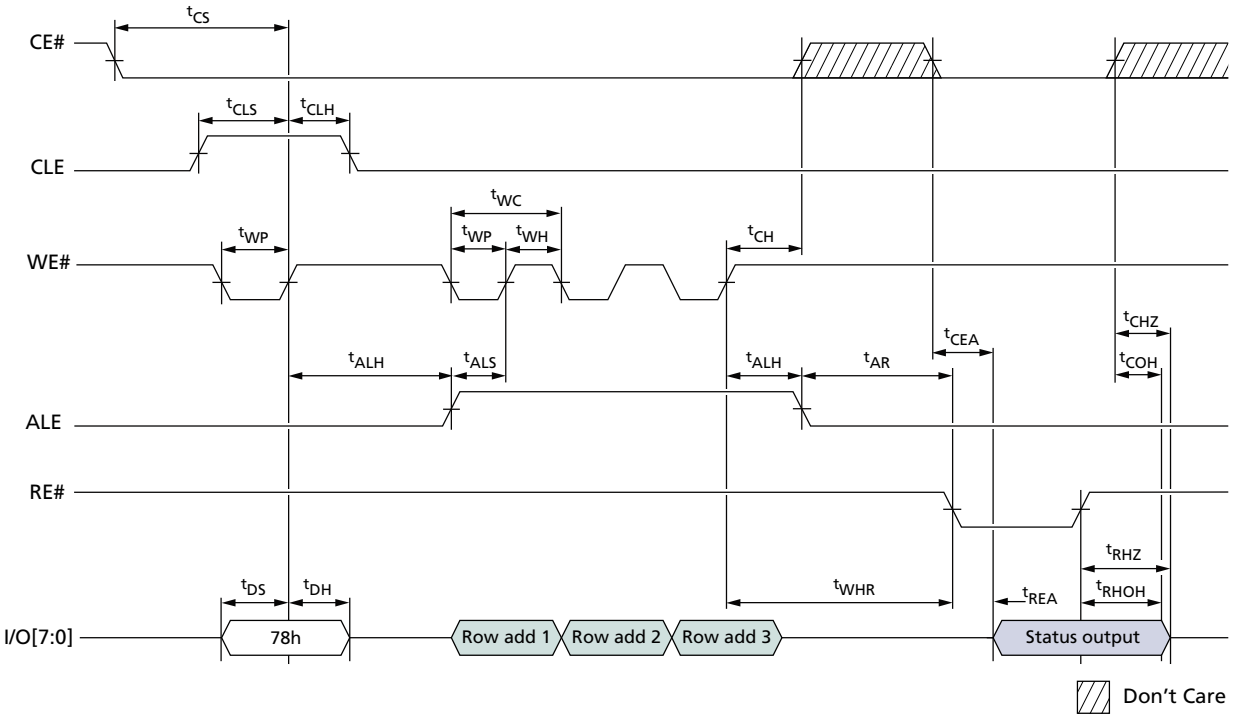


Figure 78: READ PARAMETER PAGE

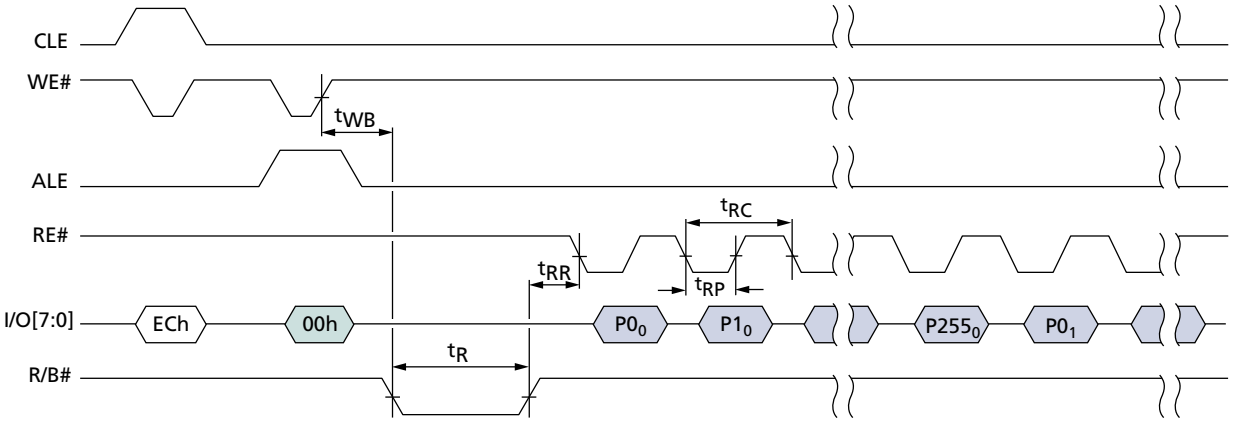


Figure 79: READ PAGE

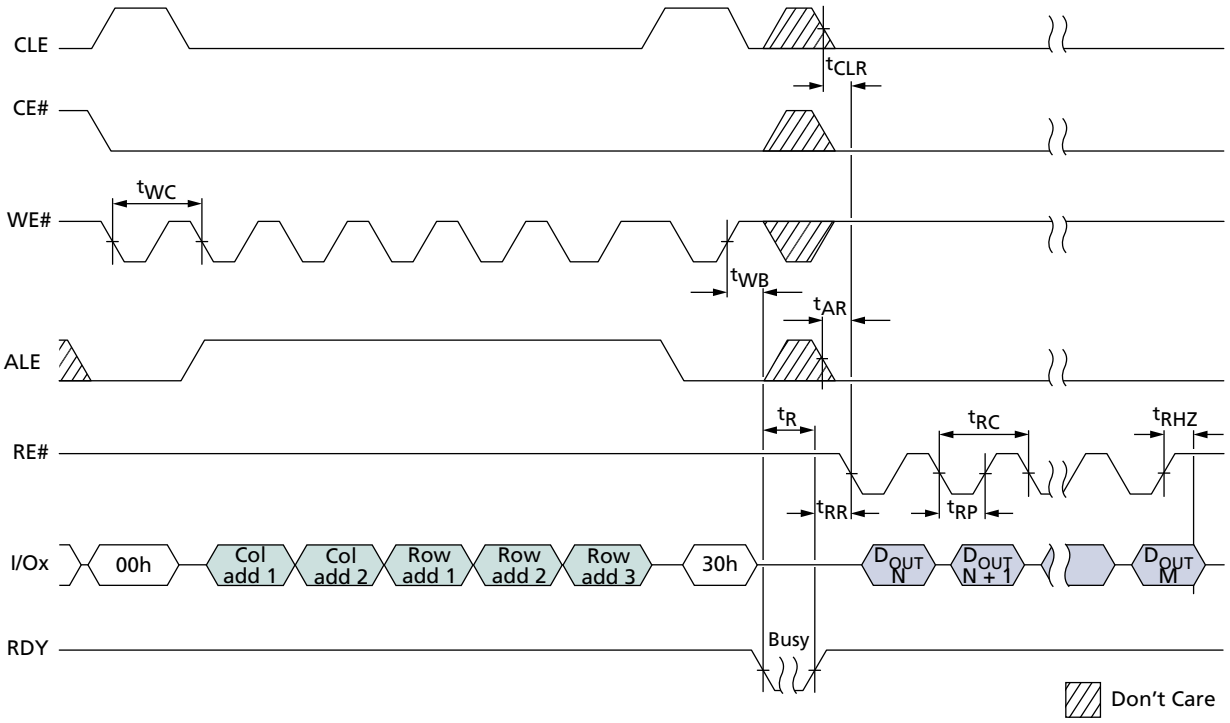


Figure 80: READ PAGE Operation with CE# "Don't Care"

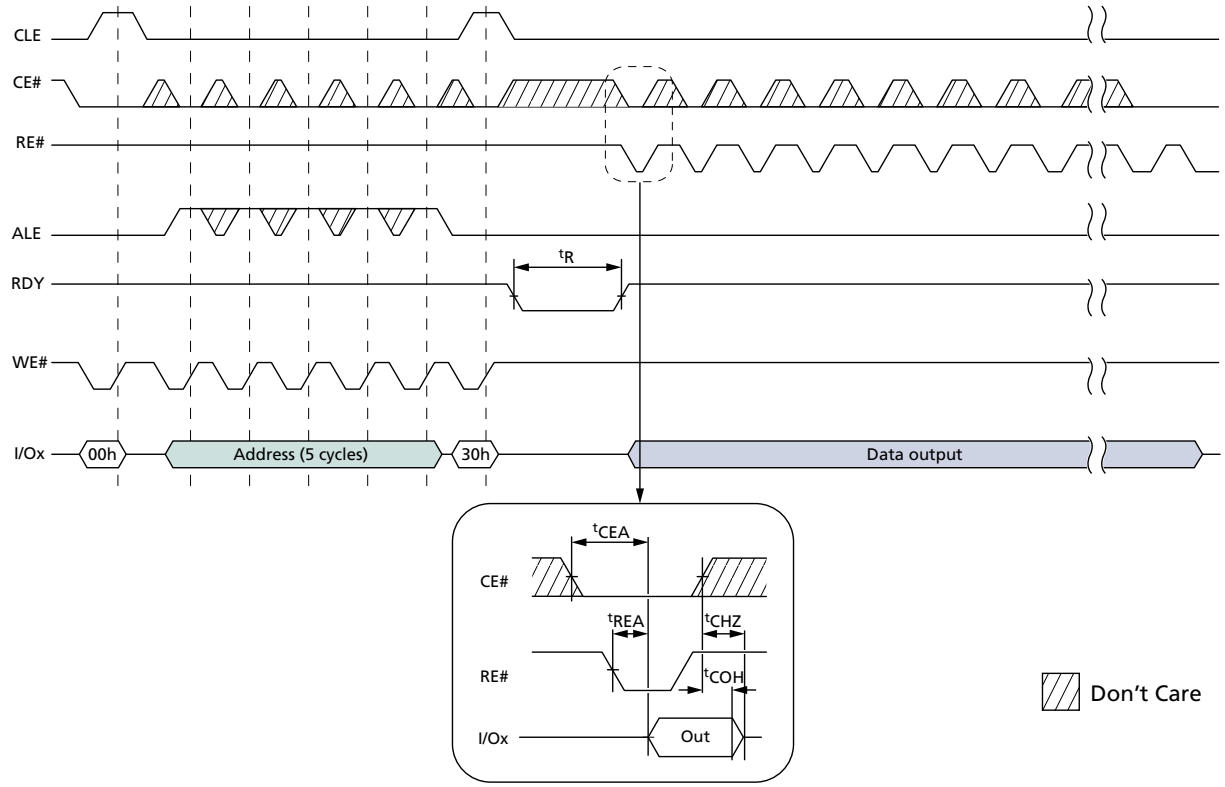


Figure 81: RANDOM DATA READ

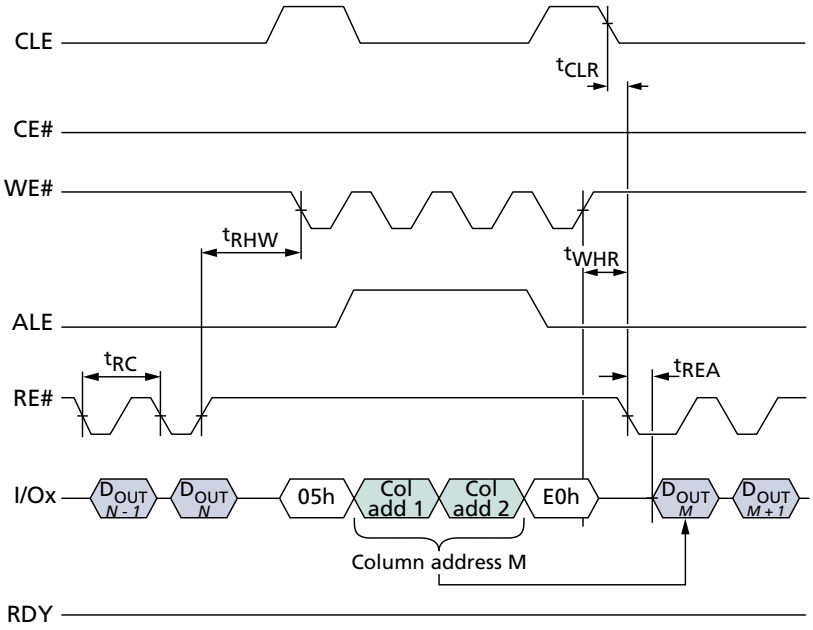


Figure 82: READ PAGE CACHE SEQUENTIAL

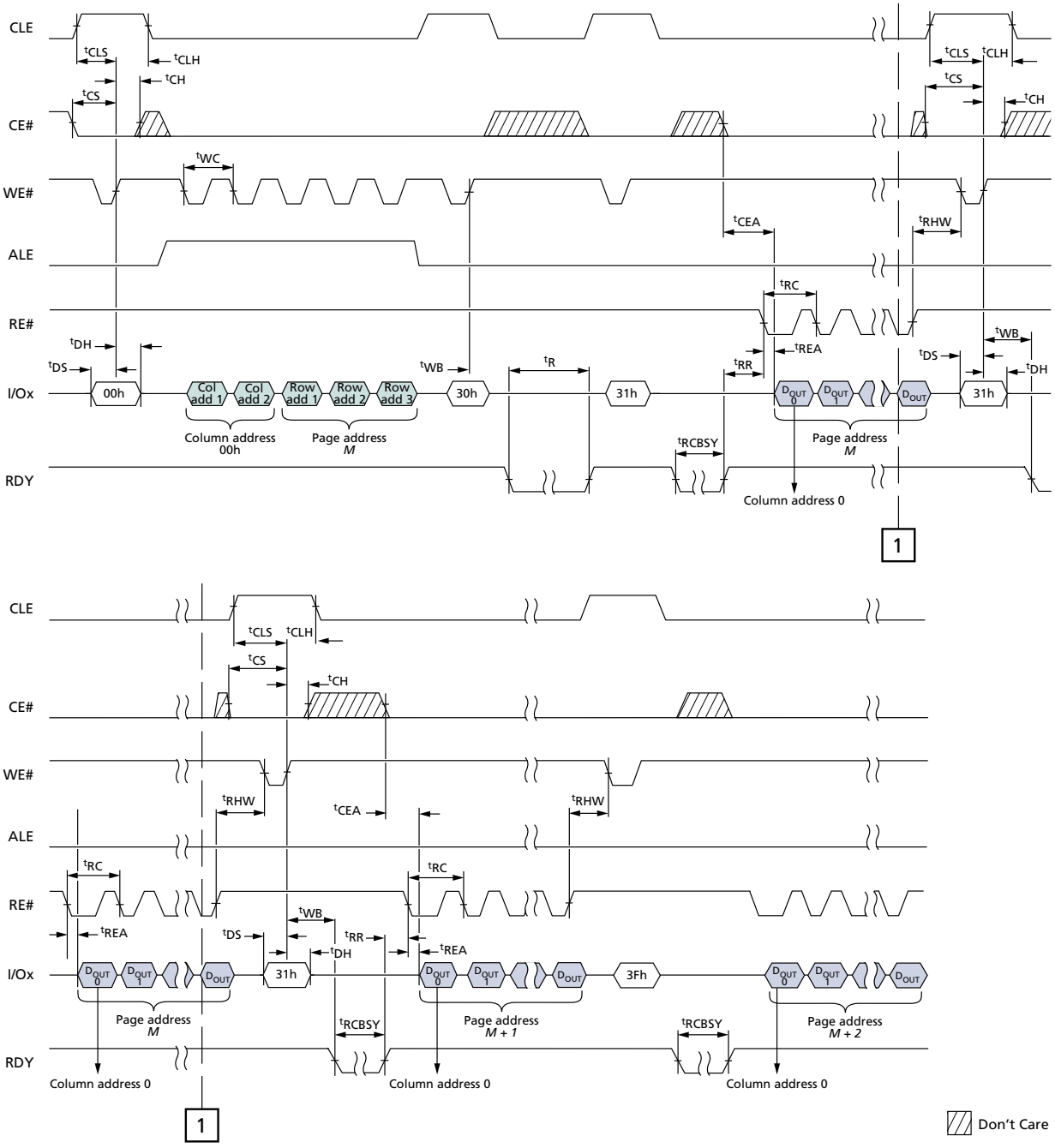


Figure 83: READ PAGE CACHE RANDOM

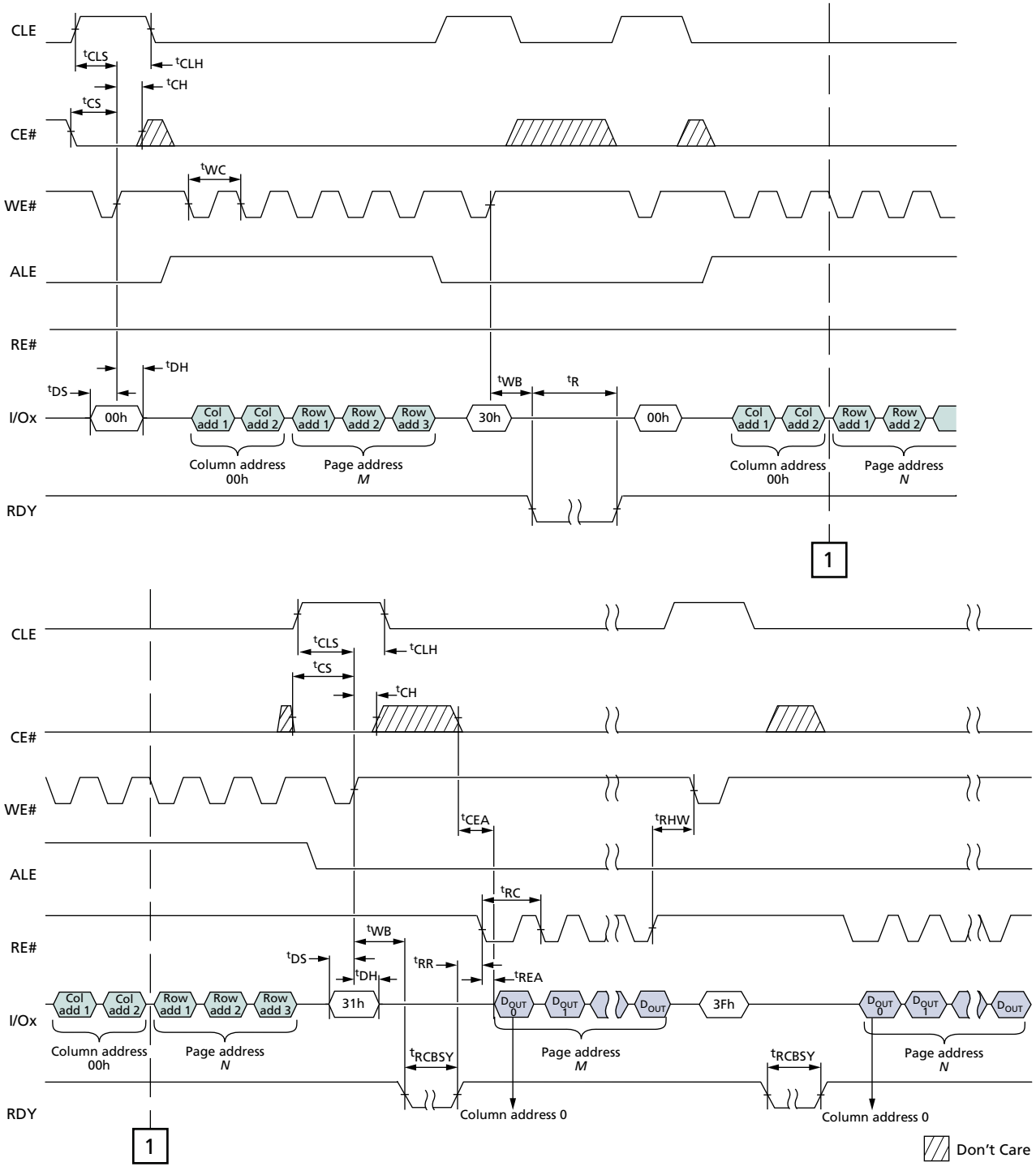


Figure 84: READ ID Operation

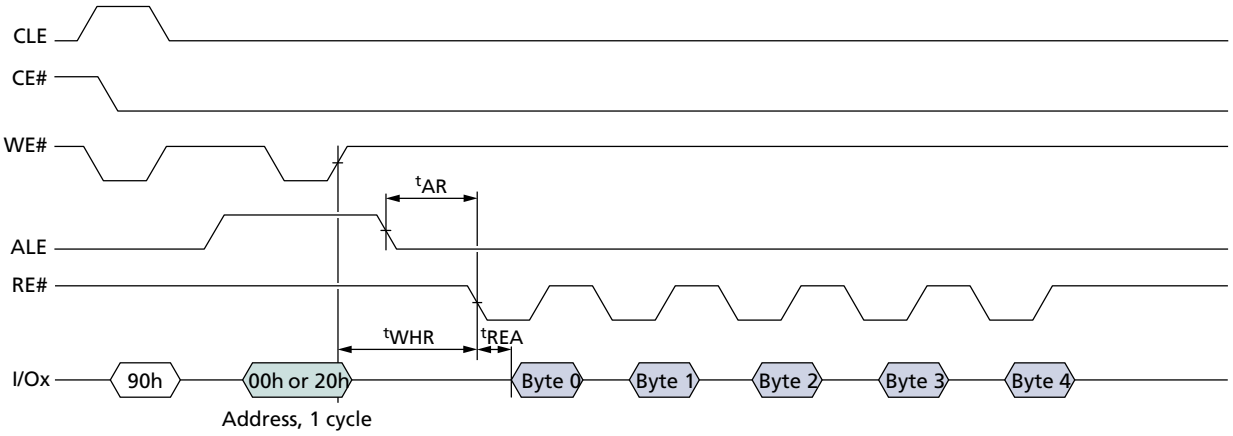


Figure 85: PROGRAM PAGE Operation

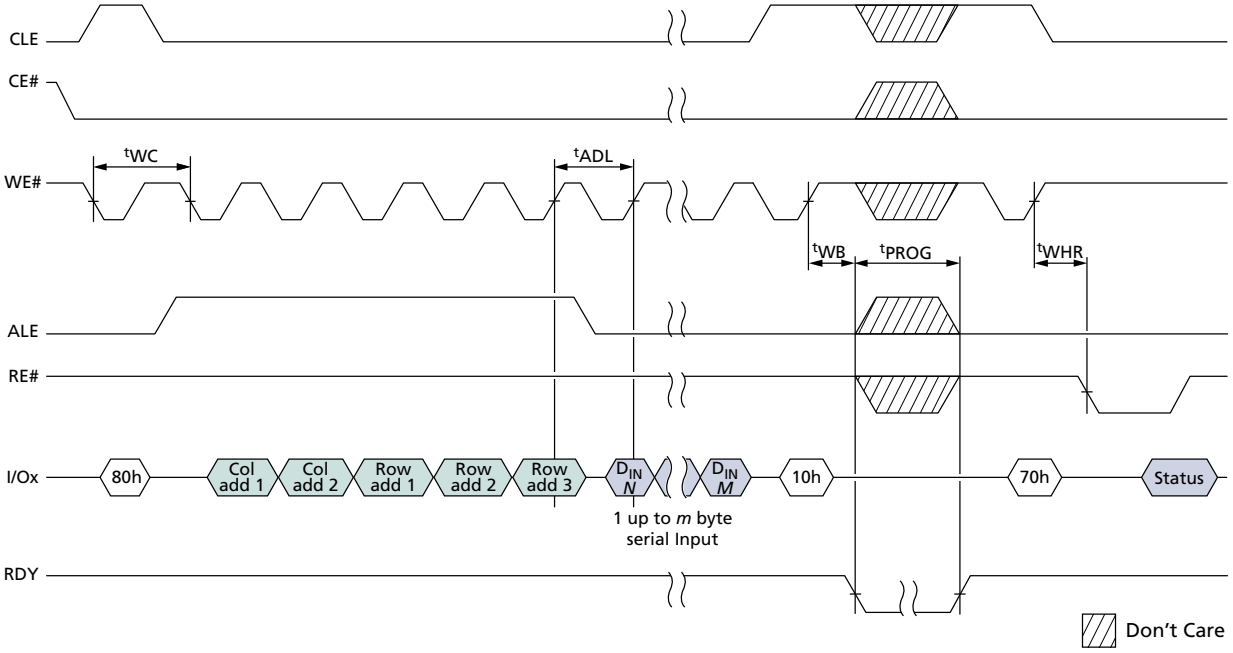


Figure 86: PROGRAM PAGE Operation with CE# "Don't Care"

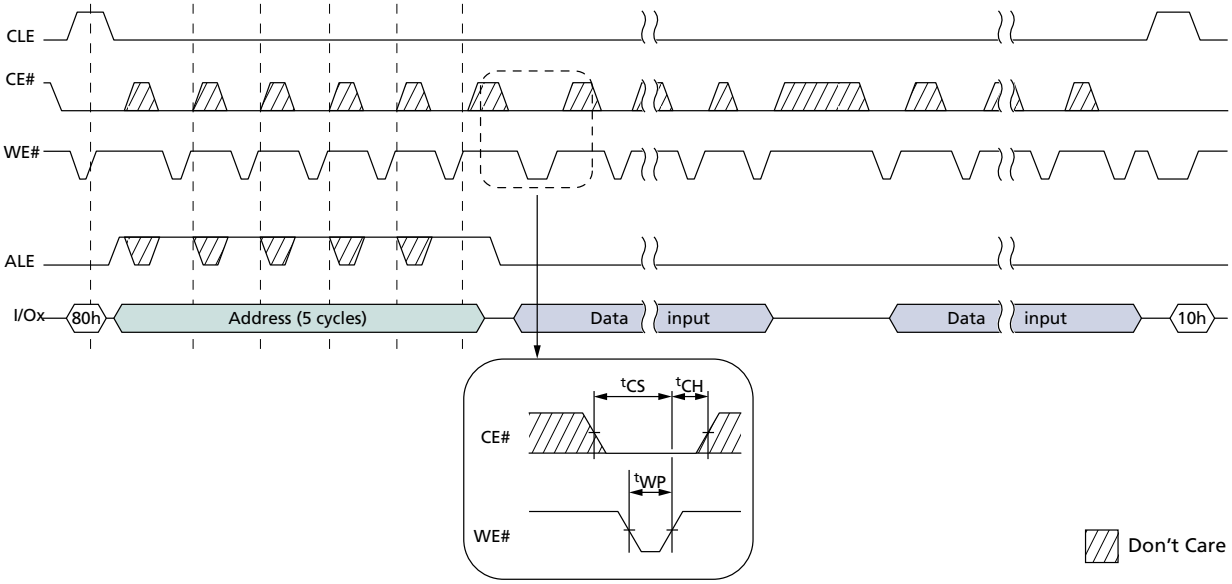


Figure 87: PROGRAM PAGE Operation with RANDOM DATA INPUT

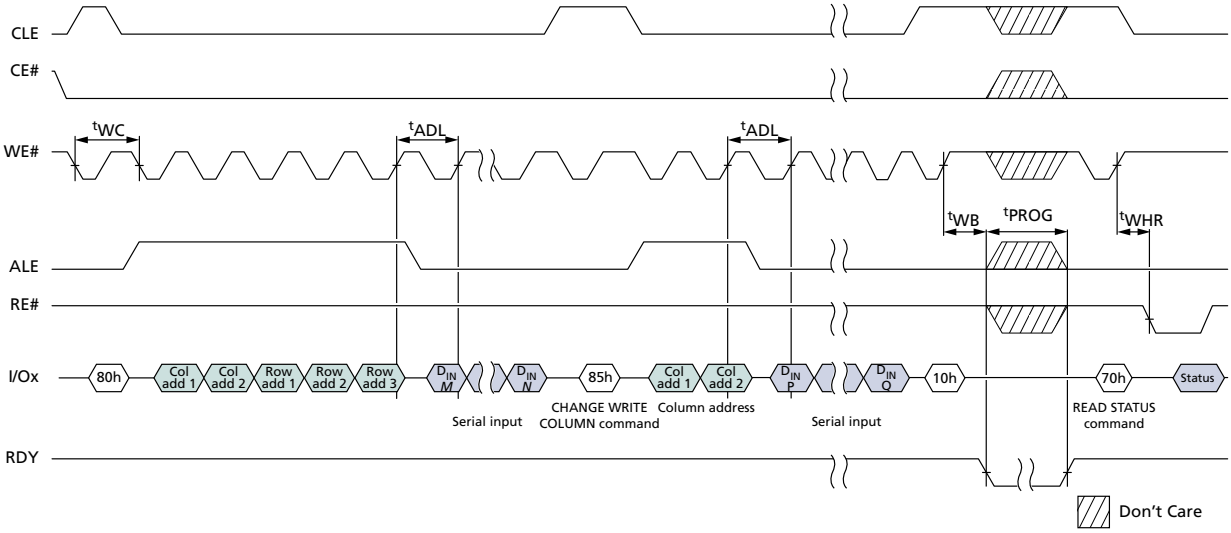


Figure 88: PROGRAM PAGE CACHE

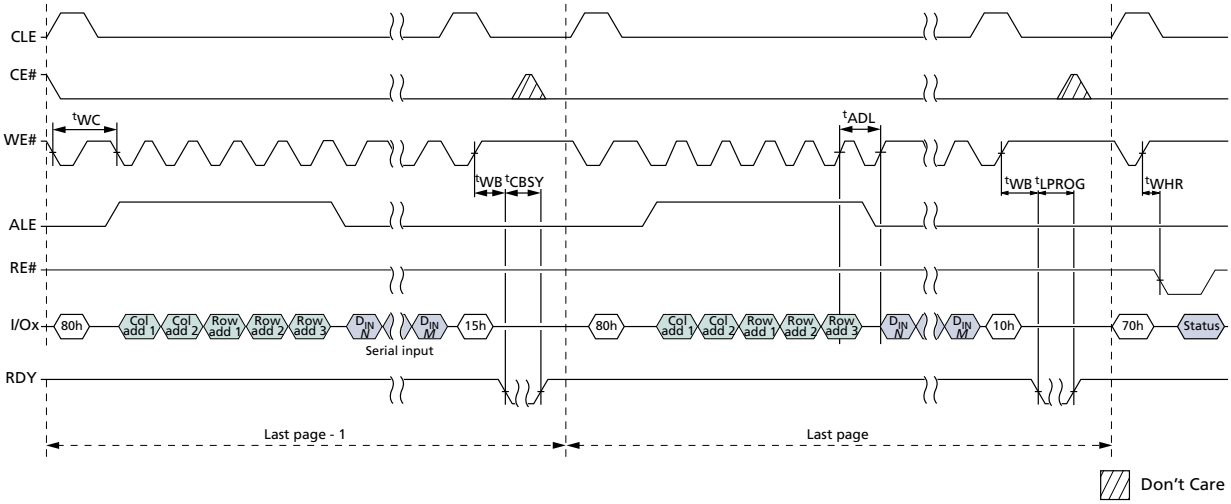


Figure 89: PROGRAM PAGE CACHE Ending on 15h

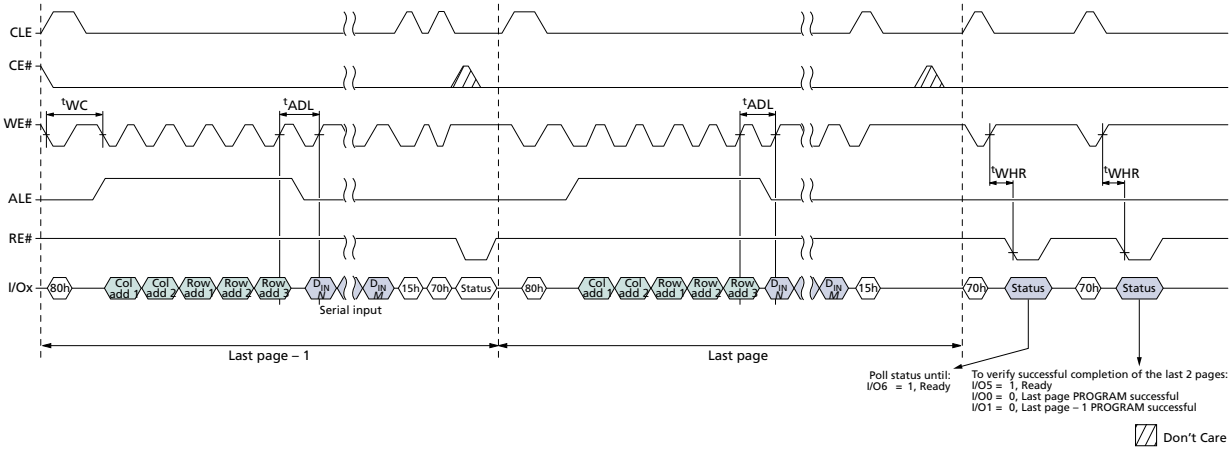


Figure 90: INTERNAL DATA MOVE

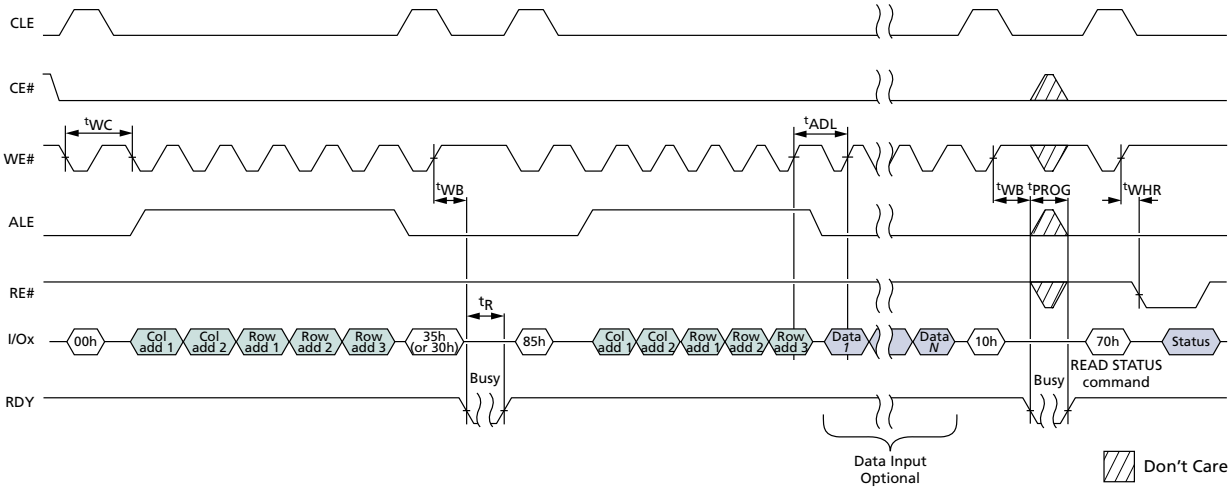
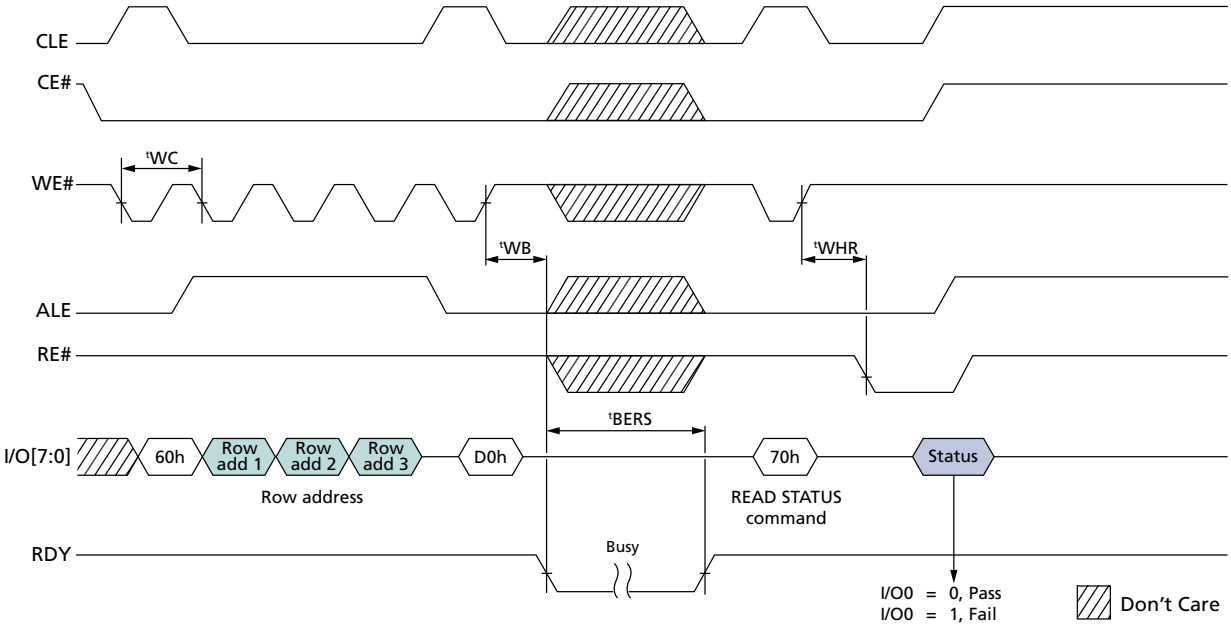


Figure 91: ERASE BLOCK Operation



16Gb: x16 LPDDR4X SDRAM

Features

- Ultra-low-voltage core and I/O power supplies
  - V_{DD1} = 1.70–1.95V; 1.80V nominal
  - V_{DD2} = 1.06–1.17V; 1.10V nominal
  - V_{DDQ} = 0.57–0.65V; 0.60V nominal
- JEDEC LPDDR4X-compliant
- Frequency range
  - 2133–10 MHz (data rate range per pin: 4266–20 Mb/s)
- Architecture
  - Up to 8.53 GB/s per channel (x16)
  - 16*n* prefetch DDR architecture
  - 8 internal banks per channel for concurrent operation
  - Single-data-rate command/address entry
  - Bidirectional/differential data strobe per byte lane
  - Programmable READ and WRITE latencies (RL/WL)
  - Programmable and on-the-fly burst lengths (BL = 16, 32)
  - Directed per-bank refresh for concurrent bank operation and ease of command scheduling
  - On-chip temperature sensor to control self refresh rate
  - Partial-array self refresh (PASR)
  - Selectable output drive strength (DS)
  - Clock-stop capability
  - RoHS-compliant, "green" packaging
  - Programmable V_{SS} (ODT) termination
  - Single-ended CK and DQS support

Table 39: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate per Pin (Mb/s)	Array Configuration	WRITE Latency		READ Latency	
				Set A	Set B	DBI Disabled	DBI Enabled
-046	2133	4266	1 Gig x 16	18	34	36	40

General Description

The 16Gb mobile low-power DDR4 SDRAM with low V_{DDQ} (LPDDR4X) is a high-speed, CMOS dynamic random-access memory device. This device is internally configured with 2 channels or 1 channel ×16 I/O, each channel having 8 banks.

General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQ collectively, unless stated otherwise.

DQS and CK should be interpreted as DQS_t, DQS_c and CK_t, CK_c respectively, unless stated otherwise. CA includes all CA pins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[5:0].

V_{REF} indicates V_{REFCA} and V_{REFDQ}.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, not supported, and will result in unknown operation.

For single-ended CK and DQS features or specifications, refer to the LPDDR4X Single-Ended CK and DQS Addendum.

Device Configuration

Table 40: Device Configuration

		1G16 (16Gb/package)
Die addressing	Dual/single Die	16Gb single-channel die
	Memory density (per die)	16Gb
	Memory density (per channel)	16Gb
	Configuration	128Mb × 16 DQ × 8 banks
	Number of channels (per die)	1
	Number of banks (per channel)	8
	Array prefetch (bits, per channel)	256
	Number of rows (per channel)	131,072
	Number of columns (fetch boundaries)	64
	Page size (bytes)	2048
	Channel density (bits per channel)	17,179,869,184
	Total density (bits per die)	17,179,869,184
	Bank address	BA[2:0]
	Row address	R[16:0]
	Column address	C[9:0]
	Burst starting address boundary	64-bit

Note: 1. Refer to Package Block Diagram section in Product Specification and SDRAM Addressing section in General LPDDR4X specification.

Refresh Requirement Parameters

Table 41: Refresh Requirement Parameters

Parameter	Symbol	16Gb Single-Channel Die	Unit
REFRESH cycle time (all banks)	^{t}RFCab	380	ns
REFRESH cycle time (per bank)	^{t}RFCpb	190	ns
Per bank refresh to per bank refresh time (different bank)	^{t}PBR2PBR	90	ns

Note: 1. This table only describes refresh parameters which are density dependent. Refer to Refresh Requirement section in General LPDDR4X specification for all the refresh parameters.

Product Specific Mode Register definition

Table 42: Mode Register Contents

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0			**Single-ended mode**			**RFM support**	**Latency mode**	**REF**
	OP[0] = 1b: Only modified refresh mode supported OP[1] = 0b: Device supports normal latency OP[2] = 0b: Device supports TRR OP[5] = 1b: Device supports single-ended mode							
MR3						**PPRP[3]**		
	OP[2] = 0b: PPR protection disabled (default) 1b: PPR protection enabled							
MR5	**Manufacturer ID**							
	1111 1111b: Micron							
MR6	**Revision ID1**							
	0000 0111b							
MR8	**I/O width**		**Density**					
	OP[7:6] = 00b: x16/channel		OP[5:2] = 0110b: 16Gb single-channel die					
MR13						**VRO**		
	OP[2] = 0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6							
MR24	**TRR mode**				**Unlimited MAC**	**MAC value**		
	OP[3:0] = 1000b: Unlimited MAC OP[7] = 0b: Disable (default) 1b: Reserved							
MR25	**PPR resources[4]**							
	Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0
	0b: PPR resource is not available 1b: PPR resource is available							

Notes: 1. The contents of Product Specific Mode Register definition will reflect information specific to each die in these packages.
2. Other bits not defined above and other mode registers are referred to Mode Register Assignments and Definitions section.
3. When not using PPR function, PPR protection should be enabled to prevent unintended PPR entry.(MR3 OP[2]=1b).
4. Before using PPR function, confirm the availability of PPR resource by reading MR25.
5. Notes 1 and 2 apply to entire table.

I_{DD} Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section for detailed conditions.

Table 43: I_{DD} Parameters – Single Die (16Gb Single-Channel Die)

V_{DD2}= 1.06–1.17V; V_{DDQ} = 0.57–0.65V; V_{DD1} = 1.70–1.95V; T_C = –25°C to +85°C

Symbol	Supply	Speed Grade	Unit	Note
		4266 Mb/s		
I_{DD01}	V_{DD1}	5.00	mA	
I_{DD02}	V_{DD2}	26.00		
I_{DD0Q}	V_{DDQ}	0.75		
I_{DD2P1}	V_{DD1}	2.40	mA	
I_{DD2P2}	V_{DD2}	3.40		
I_{DD2PQ}	V_{DDQ}	0.75		
I_{DD2PS1}	V_{DD1}	2.40	mA	
I_{DD2PS2}	V_{DD2}	3.40		
I_{DD2PSQ}	V_{DDQ}	0.75		
I_{DD2N1}	V_{DD1}	2.40	mA	
I_{DD2N2}	V_{DD2}	14.00		
I_{DD2NQ}	V_{DDQ}	0.75		
I_{DD2NS1}	V_{DD1}	2.40	mA	
I_{DD2NS2}	V_{DD2}	12.00		
I_{DD2NSQ}	V_{DDQ}	0.75		
I_{DD3P1}	V_{DD1}	2.40	mA	
I_{DD3P2}	V_{DD2}	6.20		
I_{DD3PQ}	V_{DDQ}	0.75		
I_{DD3PS1}	V_{DD1}	2.40	mA	
I_{DD3PS2}	V_{DD2}	6.20		
I_{DD3PSQ}	V_{DDQ}	0.75		
I_{DD3N1}	V_{DD1}	3.40	mA	
I_{DD3N2}	V_{DD2}	16.00		
I_{DD3NQ}	V_{DDQ}	0.75		
I_{DD3NS1}	V_{DD1}	3.40	mA	
I_{DD3NS2}	V_{DD2}	14.00		
I_{DD3NSQ}	V_{DDQ}	0.75		
I_{DD4R1}	V_{DD1}	11.00	mA	2, 3
I_{DD4R2}	V_{DD2}	205.00		
I_{DD4RQ}	V_{DDQ}	63.00		
I_{DD4W1}	V_{DD1}	11.00	mA	2
I_{DD4W2}	V_{DD2}	160.00		
I_{DD4WQ}	V_{DDQ}	0.75		

Table 43: I_{DD} Parameters – Single Die (16Gb Single-Channel Die) (Continued)

Symbol	Supply	Speed Grade	Unit	Note
		4266 Mb/s		
I_{DD51}	V_{DD1}	23.00	mA	
I_{DD52}	V_{DD2}	110.00		
I_{DD5Q}	V_{DDQ}	0.75		
I_{DD5AB1}	V_{DD1}	6.60	mA	
I_{DD5AB2}	V_{DD2}	24.00		
I_{DD5ABQ}	V_{DDQ}	0.75		
I_{DD5PB1}	V_{DD1}	4.80	mA	
I_{DD5PB2}	V_{DD2}	24.00		
I_{DD5PBQ}	V_{DDQ}	0.75		

Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BL = 16, DBI disabled.
3. I_{DD4RQ} value is reference only. Typical value. $V_{OH} = 0.5 \times V_{DDQ}$; $T_C = 25°C$

Table 44: I_{DD6} Full-Array Self Refresh Current – Single Die (16Gb Single-Channel Die)

V_{DD2}= 1.06–1.17V; V_{DDQ} = 0.57–0.65V; V_{DD1} = 1.70–1.95V

Temperature	Supply	Full-Array Self Refresh Current	Unit
25°C	V_{DD1}	0.52	mA
	V_{DD2}	1.16	
	V_{DDQ}	0.01	
85°C	V_{DD1}	4.30	mA
	V_{DD2}	9.00	
	V_{DDQ}	0.75	

Note: 1. I_{DD6} 25°C is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD6} 85°C is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.

General LPDDR4X Specification

Functional Description

The Mobile Low-Power DDR4 SDRAM (LPDDR4) is a high-speed CMOS, dynamic random-access memory internally configured with either 1 or 2 channels. Each channel is comprised of 16 DQs and 8 banks.

LPDDR4 uses a 2-tick, single-data-rate (SDR) protocol on the CA bus to reduce the number of input signals in the system. The term "2-tick" means that the command/address is decoded across two transactions, such that half of the command/address is captured with each of two consecutive rising edges of CK. The 6-bit CA bus contains command, address, and bank information. Some commands such as READ, WRITE, MASKED WRITE, and ACTIVATE require two consecutive 2-tick SDR commands to complete the instruction.

LPDDR4 uses a double-data-rate (DDR) protocol on the DQ bus to achieve high-speed operation. The DDR interface transfers two data bits to each DQ lane in one clock cycle and is matched to a 16*n*-prefetch DRAM architecture. A write/read access consists of a single 16*n*-bit-wide data transfer to/from the DRAM core and 16 corresponding *n*-bit-wide data transfers at the I/O pins.

Read and write accesses to the device are burst-oriented. Accesses start at a selected column address and continue for a programmed number of columns in a programmed sequence.

Accesses begin with the registration of an ACTIVATE command to open a row in the memory core, followed by a WRITE or READ command to access column data within the open row. The address and bank address (BA) bits registered by the ACTIVATE command are used to select the bank and row to be opened. The address and BA bits registered with the WRITE or READ command are used to select the bank and the starting column address for the burst access.

Prior to normal operation, the LPDDR4 SDRAM must be initialized. The following sections provide detailed information about device initialization, register definition, command descriptions and device operations.

SDRAM Addressing

The table below includes all SDRAM addressing options defined by JEDEC. Under the Device Configuration heading near the beginning of this data sheet are addressing details for this product data sheet.

Table 45: SDRAM Addressing – Dual-Channel Die

Memory Density (Per Die)		4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
Memory density (per channel)		2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb
Configuration		16Mb × 16DQ × 8 banks × 2 channels	24Mb × 16DQ × 8 banks × 2 channels	32Mb × 16DQ × 8 banks × 2 channels	48Mb × 16DQ × 8 banks × 2 channels	64Mb × 16DQ × 8 banks × 2 channels	96Mb × 16DQ × 8 banks × 2 channels	128Mb × 16DQ × 8 banks × 2 channels
Number of channels (per die)		2	2	2	2	2	2	2
Number of banks (per channel)		8	8	8	8	8	8	8
Array prefetch (bits, per channel)		256	256	256	256	256	256	256
Number of rows (per channel)		16,384	24,576	32,768	49,152	65,536	98,304	131,072
Number of columns (fetch boundaries)		64	64	64	64	64	64	64
Page size (bytes)		2048	2048	2048	2048	2048	2048	2048
Channel density (bits per channel)		2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184
Total density (bits per die)		4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184	25,769,803,776	34,359,738,368
Bank address		BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]
×16	Row add	R[13:0]	R[14:0] (R13 = 0 when R14 = 1)	R[14:0]	R[15:0] (R14 = 0 when R15 = 1)	R[15:0]	R[16:0] (R15 = 0 when R16 = 1)	R[16:0]
	Col. add	C[9:0]	C[9:0]	C[9:0]	C[9:0]	C[9:0]	C[9:0]	C[9:0]
Burst starting address boundary		64-bit	64-bit	64-bit	64-bit	64-bit	64-bit	64-bit

Table 46: SDRAM Addressing – Single-Channel Die

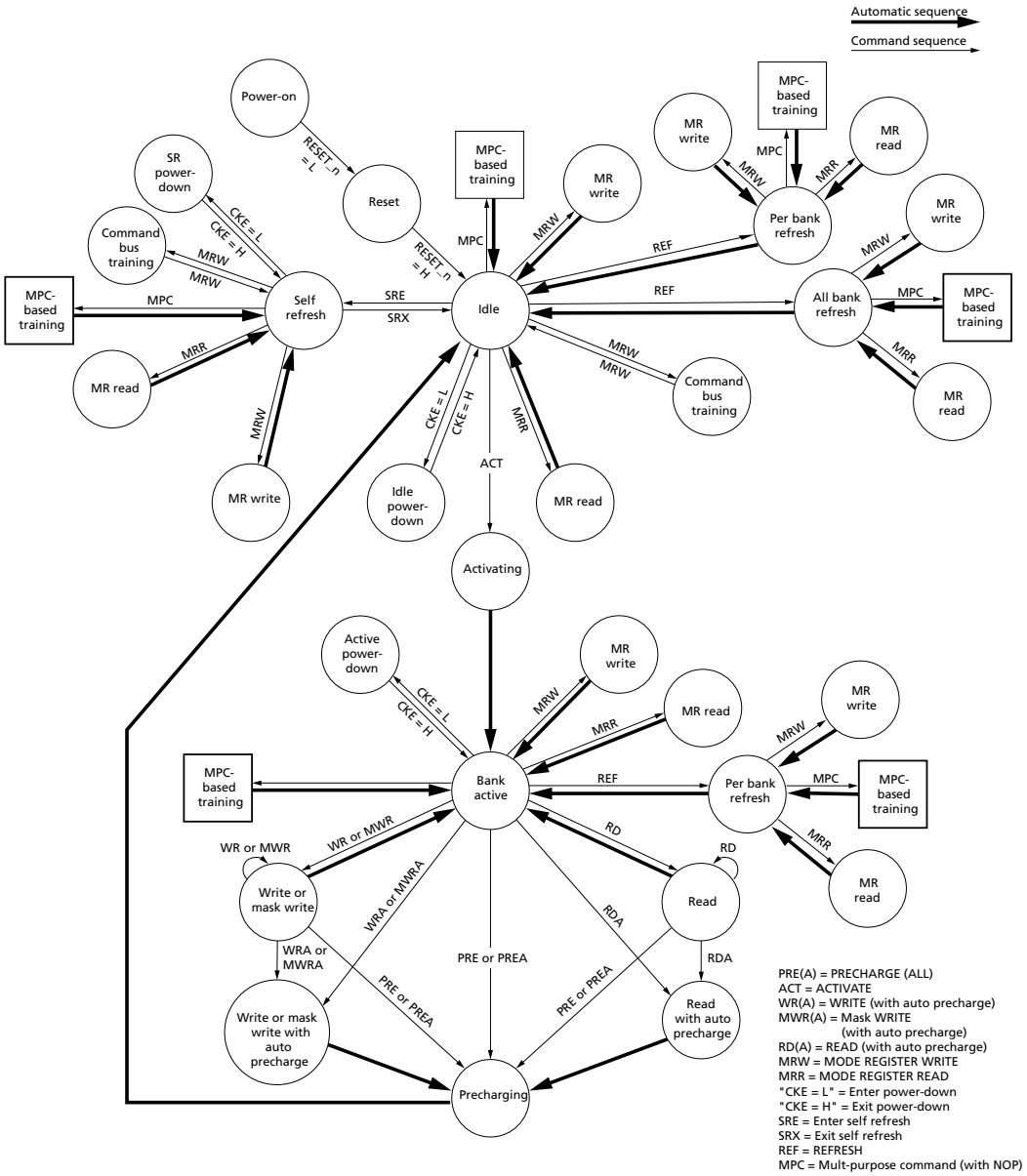
Memory Density (Per Die)		2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb
Memory density (per channel)		2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb
Configuration		16Mb × 16 DQ × 8 banks	24Mb × 16 DQ × 8 banks	32Mb × 16 DQ × 8 banks	48Mb × 16 DQ × 8 banks	64Mb × 16 DQ × 8 banks	96Mb × 16 DQ × 8 banks	128Mb × 16 DQ × 8 banks
Number of channels (per die)		1	1	1	1	1	1	1
Number of banks (per channel)		8	8	8	8	8	8	8
Array prefetch (bits, per channel)		256	256	256	256	256	256	256
Number of rows (per channel)		16,384	24,576	32,768	49,152	65,536	98,304	131,072
Number of columns (fetch boundaries)		64	64	64	64	64	64	64
Page size (bytes)		2048	2048	2048	2048	2048	2048	2048
Channel density (bits per channel)		2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184
Total density (bits per die)		2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184
Bank address		BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]
×16	Row add	R[13:0]	R[14:0] (R13 = 0 when R14 = 1)	R[14:0]	R[15:0] (R14 = 0 when R15 = 1)	R[15:0]	R[16:0] (R15 = 0 when R16 = 1)	R[16:0]
	Col. add	C[9:0]	C[9:0]	C[9:0]	C[9:0]	C[9:0]	C[9:0]	C[9:0]
Burst starting address boundary		64-bit	64-bit	64-bit	64-bit	64-bit	64-bit	64-bit

Notes: 1. The lower two column addresses (C[1:0]) are assumed to be zero and are not transmitted on the CA bus.
2. Row and column address values on the CA bus that are not used for a particular density should be at valid logic levels.
3. For non-binary memory densities, only a quarter of the row address space is invalid. When the MSB address bit is HIGH, then the MSB - 1 address bit must be LOW.

Simplified Bus Interface State Diagram

The state diagram provides a simplified illustration of the bus interface, supported state transitions, and the commands that control them. For a complete description of device behavior, use the information provided in the state diagram with the truth tables and timing specifications. The truth tables describe device behavior and applicable restrictions when considering the actual state of all banks. For command descriptions, see the Commands and Timing section.

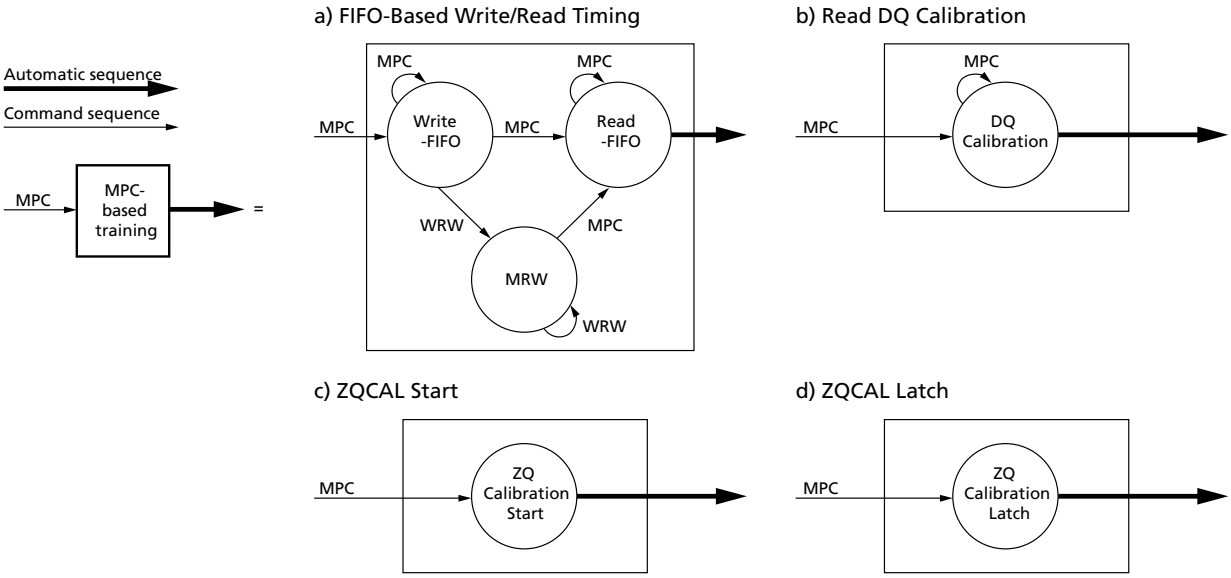
Figure 92: Simplified State Diagram



Notes: 1. From the self refresh state, the device can enter power-down, MRR, MRW, or any of the training modes initiated with the MPC command. See the Self Refresh section.
2. All banks are precharged in the idle state.
3. In the case of using an MRW command to enter a training mode, the state machine will not automatically return to the idle state at the conclusion of training. See the applicable training section for more information.
4. In the case of an MPC command to enter a training mode, the state machine may not automatically return to the idle state at the conclusion of training. See the applicable training section for more information.

5. This diagram is intended to provide an overview of the possible state transitions and commands to control them; however, it does not contain the details necessary to operate the device. In particular, situations involving more than one bank are not captured in complete detail.
6. States that have an "automatic return" and can be accessed from more than one prior state (that is, MRW from either idle or active states) will return to the state where they were initiated (that is, MRW from idle will return to idle).
7. The RESET pin can be asserted from any state and will cause the device to enter the reset state. The diagram shows RESET applied from the power-on and idle states as an example, but this should not be construed as a restriction on RESET.
8. MRW commands from the active state cannot change operating parameters of the device that affect timing. Mode register fields which may be changed via MRW from the active state include: MR1-OP[3:0], MR1-OP[7], MR3-OP[7:6], MR10-OP[7:0], MR11-OP[7:0], MR13-OP[5], MR15-OP[7:0], MR16-OP[7:0], MR17-OP[7:0], MR20-OP[7:0], and MR22-OP[4:0].

Figure 93: Simplified State Diagram



Power-Up and Initialization

To ensure proper functionality for power-up and reset initialization, default values for the MR settings are provided in the table below.

Table 47: Mode Register Default Settings

Item	Mode Register Setting	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00b	FSP-OP/WR[0] are enabled
WLS	MR2 OP[6]	0b	WRITE latency set A is selected
WL	MR2 OP[5:3]	000b	WL = 4
RL	MR2 OP[2:0]	000b	RL = 6, *n*RTP = 8
*n*WR	MR1 OP[6:4]	000b	*n*WR = 6
DBI-WR/RD	MR3 OP[7:6]	00b	Write and read DBI are disabled
CA ODT	MR11 OP[6:4]	000b	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000b	DQ ODT is disabled

Table 47: Mode Register Default Settings (Continued)

Item	Mode Register Setting	Default Setting	Description
$V_{REF(CA)}$ setting	MR12 OP[6]	1b	$V_{REF(CA)}$ range[1] is enabled
$V_{REF(CA)}$ value	MR12 OP[5:0]	011101b	Range1: 50.3% of V_{DDQ}
$V_{REF(DQ)}$ setting	MR14 OP[6]	1b	$V_{REF(DQ)}$ range[1] enabled
$V_{REF(DQ)}$ value	MR14 OP[5:0]	011101b	Range1: 50.3% of V_{DDQ}

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory. The power-up sequence of all channels must proceed simultaneously.

Voltage Ramp

1. While applying power (after Ta), RESET_n should be held LOW (≤0.2 × V_{DD2}), and all other inputs must be between $V_{IL,min}$ and $V_{IH,max}$. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in the table below. V_{DD1} must ramp at the same time or earlier than V_{DD2}. V_{DD2} must ramp at the same time or earlier than V_{DDQ}.

Table 48: Voltage Ramp Conditions

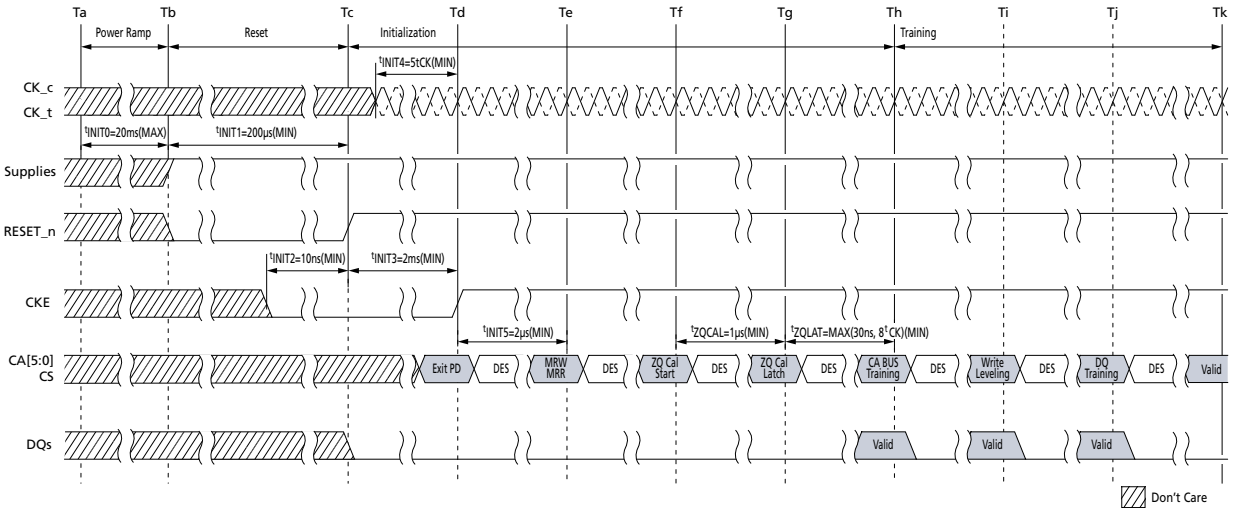
After...	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2}
	V_{DD2} must be greater than V_{DDQ} - 200mV

Notes: 1. Ta is the point when any power supply first reaches 300mV.
2. Voltage ramp conditions in above table apply between Ta and power-off (controlled or uncontrolled).
3. Tb is the point at which all supply and reference voltages are within their defined operating ranges.
4. Power ramp duration ^{t}INIT0 (Tb–Ta) must not exceed 20ms.
5. The voltage difference between any V_{SS} and V_{SSQ} must not exceed 100mV.

2. Following completion of the voltage ramp (Tb), RESET_n must be held LOW for ^{t}INIT1. DQ, DMI, DQS_t, and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latch-up. CK_t and CK_c, CS, and CA input levels must be between V_{SS} and V_{DD2} during voltage ramp to avoid latch-up. Voltage ramp power supply requirements are provided in the table below.

3. Beginning at Tb, RESET_n must remain LOW for at least ^{t}INIT1(Tc), after which RESET_n can be de-asserted to HIGH(Tc). At least 10ns before CKE de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care."

Figure 94: Voltage Ramp and Initialization Sequence



Note: 1. Training is optional and may be done at the system designer's discretion. The order of training may be different than what is shown here.

4. After RESET_n is de-asserted(Tc), wait at least ^{t}INIT3 before activating CKE. CK_t, CK_c must be started and stabilized for ^{t}INIT4 before CKE goes active(Td). CS must remain LOW when the controller activates CKE.

5. After CKE is set to HIGH, wait a minimum of ^{t}INIT5 to issue any MRR or MRW commands(Te). For MRR and MRW commands, the clock frequency must be within the range defined for ^{t}CKb. Some AC parameters (for example, ^{t}DQSCK) could have relaxed timings (such as ^{t}DQSCKb) before the system is appropriately configured.

6. After completing all MRW commands to set the pull-up, pull-down, and Rx termination values, the controller can issue the ZQCAL START command to the memory(Tf). This command is used to calibrate the V_{OH} level and the output impedance over process, voltage, and temperature. In systems where more than one device share one external ZQ resistor, the controller must not overlap the ZQ calibration sequence of each device. The ZQ calibration sequence is completed after ^{t}ZQCAL (Tg). The ZQCAL LATCH command must be issued to update the DQ drivers and DQ + CA ODT to the calibrated values.

7. After ^{t}ZQLAT is satisfied (Th), the command bus (internal $V_{REF(CA)}$, CS, and CA) should be trained for high-speed operation by issuing an MRW command (command bus training mode). This command is used to calibrate the device's internal V_{REF} and align CS/CA with CK for high-speed operation. The device will power-up with receivers configured for low-speed operations and with $V_{REF(CA)}$ set to a default factory setting. Normal device operation at clock speeds higher than ^{t}CKb may not be possible until command bus training is complete. The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and it outputs the results asynchronously on the DQ bus. See command bus training in the MRW section for information on how to enter/exit the training mode.

8. After command bus training, the controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is HIGH(Ti). See the Write Leveling section for a detailed description of the write leveling entry and exit sequence. In write leveling mode, the controller adjusts write DQS timing to the point where the device recognizes the start of write DQ data burst with desired WRITE latency.

9. After write leveling, the DQ bus (internal $V_{REF(DQ)}$, DQS, and DQ) should be trained for high-speed operation using the MPC TRAINING commands and by issuing MRW commands to adjust $V_{REF(DQ)}$. The device will power-up with receivers configured for low-speed operations and with $V_{REF(DQ)}$ set to a default factory setting. Normal device operation at clock speeds higher than ^{t}CKb should not be attempted until DQ bus training is complete. The MPC[READ DQ CALIBRATION] command is used together with MPC[READ-FIFO] or MPC[WRITE-FIFO] commands to train the DQ bus without disturbing the memory array contents. See the DQ Bus Training section for more information on the DQ bus training sequence.

10. At Tk, the device is ready for normal operation and is ready to accept any valid command. Any mode registers that have not previously been configured for normal operation should be written at this time.

Table 49: Initialization Timing Parameters

Parameter	Min	Max	Unit	Comment
^{t}INIT0	–	20	ms	Maximum voltage ramp time
^{t}INIT1	200	–	µs	Minimum RESET_n LOW time after completion of voltage ramp
^{t}INIT2	10	–	ns	Minimum CKE LOW time before RESET_n goes HIGH
^{t}INIT3	2	–	ms	Minimum CKE LOW time after RESET_n goes HIGH

Table 49: Initialization Timing Parameters (Continued)

Parameter	Min	Max	Unit	Comment
^{t}INIT4	5	–	^{t}CK	Minimum stable clock before first CKE HIGH
^{t}INIT5	2	–	µs	Minimum idle time before first MRW/MRR command
^{t}CKb	Note[1, 2]	Note[1, 2]	ns	Clock cycle time during boot

Notes: 1. Minimum ^{t}CKb guaranteed by DRAM test is 18ns.
2. The system may boot at a higher frequency than dictated by minimum ^{t}CKb. The higher boot frequency is system dependent.

Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET_n below $0.2 \times V_{DD2}$ anytime when reset is needed. RESET_n needs to be maintained for minimum ^{t}PW_RESET. CKE must be pulled LOW at least 10ns before de-asserting RESET_n.
2. Repeat steps 4–10 in Voltage Ramp section.

Table 50: Reset Timing Parameter

Parameter	Value		Unit	Comment
	Min	Max		
^{t}PW_RESET	100	–	ns	Minimum RESET_n LOW time for reset initialization with stable power

Power-Off Sequence

Controlled Power-Off

While powering off, CKE must be held LOW ($\leq 0.2 \times V_{DD2}$); all other inputs must be between $V_{IL,min}$ and $V_{IH,max}$. The device outputs remain at High-Z while CKE is held LOW.

DQ, DMI, DQS_t, and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during the power-off sequence to avoid latch-up. CK_t, CK_c, CS, and CA input levels must be between V_{SS} and V_{DD2} during the power-off sequence to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified in the minimum DC Operating Condition.

Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

Table 51: Power Supply Conditions

The voltage difference between V_{SS} and V_{SSQ} must not exceed 100mV

Between...	Applicable Conditions
Tx and Tz	V_{DD1} must be greater than V_{DD2}
	V_{DD2} must be greater than V_{DDQ} - 200mV

Uncontrolled Power-Off

When an uncontrolled power-off occurs, the following conditions must be met:

- At Tx, when the power supply drops below the minimum values specified in the Recommended DC Operating Conditions table, all power supplies must be turned off and all power supply current capacity must be at zero, except for any static charge remaining in the system.

- After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period, the relative voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than 0.5 V/µs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table 52: Power-Off Timing

Parameter	Symbol	Min	Max	Unit
Power-off ramp time	^{t}POFF	–	2	sec

Mode Registers

Mode Register Assignments and Definitions

Mode register definitions are provided in the Mode Register Assignments table. In the access column of the table, R indicates read-only; W indicates write-only; R/W indicates read- or write-capable or enabled. The MRR command is used to read from a register. The MRW command is used to write to a register.

Table 53: Mode Register Assignments

MR#	MA[5:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00h	Device info	R	RFU			RZQI		RFM support	Latency mode	REF
1	01h	Device feature 1	W	RD-PST	*n*WR (for AP)			RD-PRE	WR-PRE	BL	
2	02h	Device feature 2	W	WR Lev	WLS	WL			RL		
3	03h	I/O config-1	W	DBI-WR	DBI-RD	PDDS			PPRP	WR-PST	PU-CAL
4	04h	Refresh and training	R /W	TUF	Thermal offset		PPRE	SR abort	Refresh rate		
5	05h	Basic config-1	R	Manufacturer ID							
6	06h	Basic config-2	R	Revision ID1							
7	07h	Basic config-3	R	Revision ID2							
8	08h	Basic config-4	R	I/O width		Density				Type	
9	09h	Test mode	W	Vendor-specific test mode							
10	0Ah	I/O calibration	W	RFU							ZQ RST
11	0Bh	ODT	W	RFU	CA ODT			RFU	DQ ODT		
12	0Ch	$V_{REF(CA)}$	R/W	RFU	VR_{CA}	$V_{REF(CA)}$					
13	0Dh	Register control	W	FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT
14	0Eh	$V_{REF(DQ)}$	R/W	RFU	VR_{DQ}	$V_{REF(DQ)}$					
15	0Fh	DQI-LB	W	Lower-byte invert register for DQ calibration							
16	10h	PASR_Bank	W	PASR bank mask							
17	11h	PASR_Seg	W	PASR segment mask							
18	12h	IT-LSB	R	DQS oscillator count – LSB							
19	13h	IT-MSB	R	DQS oscillator count – MSB							
20	14h	DQI-UB	W	Upper-byte invert register for DQ calibration							
21	15h	Vendor use	W	RFU							
22	16h	ODT feature 2	W	ODTD for x8_2ch		ODTD -CA	ODTE -CS	ODTE -CK	SoC ODT		
23	17h	DQS oscillator stop	W	DQS oscillator run-time setting							
24	18h	TRR control when MR0 OP2 = 0b	R/W	TRR mode	TRR mode BAn			Unltd MAC	MAC value		
		RFM control when MR0 OP2 = 1b	R	RAAMMT		RAAIMT					RFM
25	19h	PPR resources	R	B7	B6	B5	B4	B3	B2	B1	B0
26–29	1Ah–1Dh	–	–	Reserved for future use							

Table 53: Mode Register Assignments (Continued)

MR#	MA[5:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
30	1Eh	Reserved for test	W	SDRAM will ignore							
31	1Fh	–	–	Reserved for future use							
32	20h	DQ calibration pattern A	W	See DQ calibration section							
33–35	21h–23h	Do not use	–	Do not use							
36	24h	RAADEC	R	RFU						RAADEC	
37–38	25h–26h	Do not use	-	Do not use							
39	27h	Reserved for test	W	SDRAM will ignore							
40	28h	DQ calibration pattern B	W	See DQ calibration section							
41–47	29h–2Fh	Do not use	–	Do not use							
48–63	30h–3Fh	Reserved	–	Reserved for future use							

Notes: 1. RFU bits must be set to 0 during MRW commands.
2. RFU bits are read as 0 during MRR commands.
3. All mode registers that are specified as RFU or write-only shall return undefined data when read via an MRR command.
4. RFU mode registers must not be written.
5. Writes to read-only registers will not affect the functionality of the device.
6. Notes 1–5 apply to entire table.

Table 54: MR0 Device Feature 0 (MA[5:0] = 00h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU			RZQI		RFM support	Latency mode	REF

Table 55: MR0 Op-Code Bit Definitions

Register Information	Type	OP	Definition	Notes
Refresh mode	Read-only	OP[0]	0b: Both legacy and modified refresh mode supported 1b: Only modified refresh mode supported	
Latency mode	Read-only	OP[1]	0b: Device supports normal latency	5, 6
			1b: Device supports byte mode latency	
RFM support	Read-only	OP[2]	0b: TRR is supported	
			1b: RFM is supported	
Built-in self-test for RZQ information	Read-only	OP[4:3]	00b: RZQ self-test not supported	1–4
			01b: ZQ may connect to V_{SSQ} or float	
			10b: ZQ may short to V_{DDQ}	
			11b: ZQ pin self-test completed, no error condition detected (ZQ may not connect to V_{SSQ}, float, or short to V_{DDQ})	

Notes: 1. RZQI MR value, if supported, will be valid after the following sequence:
- Completion of MPC[ZQCAL START] command to either channel
- Completion of MPC[ZQCAL LATCH] command to either channel then ^{t}ZQLAT is satisfied

RZQI value will be lost after reset.
2. If ZQ is connected to V_{SSQ} to set default calibration, OP[4:3] must be set to 01b. If ZQ is not connected to V_{SSQ}, either OP[4:3] = 01b or OP[4:3] = 10b might indicate a ZQ pin assembly error. It is recommended that the assembly error be corrected.
3. In the case of possible assembly error, the device will default to factory trim settings for R_{ON}, and will ignore ZQ CALIBRATION commands. In either case, the device may not function as intended.
4. If the ZQ pin self-test returns OP[4:3] = 11b, the device has detected a resistor connected to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor meets the specified limits (that is, 240Ω±1%).
5. See byte mode addendum spec for byte mode latency details.
6. Byte mode latency for 2Ch. x16 device is only allowed when it is stacked in a same package with byte mode device.

Table 56: MR1 Device Feature 1 (MA[5:0] = 01h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RD-PST	*n*WR (for AP)			RD-PRE	WR-PRE	BL	

Table 57: MR1 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
BL Burst length	Write-only	OP[1:0]	00b: BL = 16 sequential (default)	1
			01b: BL = 32 sequential	
			10b: BL = 16 or 32 sequential (on-the-fly)	
			11b: Reserved	
WR-PRE Write preamble length	Write-only	OP[2]	0b: Reserved	5, 6
			1b: WR preamble = 2 × ^{t}CK	
RD-PRE Read preamble type	Write-only	OP[3]	0b: RD preamble = Static (default)	3, 5, 6
			1b: RD preamble = Toggle	
*n*WR Write-recovery for AUTO PRECHARGE command	Write-only	OP[6:4]	000b: *n*WR = 6 (default)	2, 5, 6
			001b: *n*WR = 10	
			010b: *n*WR = 16	
			011b: *n*WR = 20	
			100b: *n*WR = 24	
			101b: *n*WR = 30	
			110b: *n*WR = 34	
			111b: *n*WR = 40	
RD-PST Read postamble length	Write-only	OP[7]	0b: RD postamble = 0.5 × ^{t}CK (default)	4, 5, 6
			1b: RD postamble = 1.5 × ^{t}CK	

Notes: 1. Burst length on-the-fly can be set to either BL = 16 or BL = 32 by setting the BL bit in the command operands. See the Command Truth Table.
2. The programmed value of *n*WR is the number of clock cycles the device uses to determine the starting point of an internal precharge after a write burst with auto precharge (AP) enabled. See Frequency Ranges for RL, WL, and *n*WR Settings table.
3. For READ operations, this bit must be set to select between a toggling preamble and a non-toggling preamble (see the Preamble section).

4. OP[7] provides an optional read postamble with an additional rising and falling edge of DQS_t. The optional postamble cycle is provided for the benefit of certain memory controllers.
5. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
6. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, that is, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

Table 58: Burst Sequence for Read

C4	C3	C2	C1	C0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16-Bit READ Operation																																				
V	**0**	**0**	**0**	**0**	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
V	**0**	**1**	**0**	**0**	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3																
V	**1**	**0**	**0**	**0**	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7																
V	**1**	**1**	**0**	**0**	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B																
32-Bit READ Operation																																				
0	**0**	**0**	**0**	**0**	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
0	**0**	**1**	**0**	**0**	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13
0	**1**	**0**	**0**	**0**	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17
0	**1**	**1**	**0**	**0**	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B
1	**0**	**0**	**0**	**0**	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	**0**	**1**	**0**	**0**	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
1	**1**	**0**	**0**	**0**	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1	**1**	**1**	**0**	**0**	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B

Notes: 1. C[1:0] are not present on the CA bus; they are implied to be zero.
2. The starting burst address is on 64-bit (4*n*) boundaries.

Table 59: Burst Sequence for Write

C4	C3	C2	C1	C0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16-Bit WRITE Operation																																				
V	**0**	**0**	**0**	**0**	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
32-Bit WRITE Operation																																				
0	**0**	**0**	**0**	**0**	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

Notes: 1. C[1:0] are not present on the CA bus; they are implied to be zero.
2. The starting burst address is on 256-bit (16*n*) boundaries for burst length 16.
3. The starting burst address is on 512-bit (32*n*) boundaries for burst length 32.
4. C[3:2] must be set to 0 for all WRITE operations.

Table 60: MR2 Device Feature 2 (MA[5:0] = 02h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WR Lev	WLS	WL			RL		

Table 61: MR2 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
RL READ latency	Write-only	OP[2:0]	RL and *n*RTP for DBI-RD disabled (MR3 OP[6] = 0b)	1, 3, 4
			000b: RL = 6, *n*RTP = 8 (default)	
			001b: RL = 10, *n*RTP = 8	
			010b: RL = 14, *n*RTP = 8	
			011b: RL = 20, *n*RTP = 8	
			100b: RL = 24, *n*RTP = 10	
			101b: RL = 28, *n*RTP = 12	
			110b: RL = 32, *n*RTP = 14	
			111b: RL = 36, *n*RTP = 16	
			RL and *n*RTP for DBI-RD enabled (MR3 OP[6] = 1b)	
			000b: RL = 6, *n*RTP = 8	
			001b: RL = 12,*n*RTP = 8	
			010b: RL = 16, *n*RTP = 8	
			011b: RL = 22, *n*RTP = 8	
			100b: RL = 28, *n*RTP = 10	
			101b: RL = 32, *n*RTP = 12	
			110b: RL = 36, *n*RTP = 14	
			111b: RL = 40, *n*RTP = 16	
WL WRITE latency	Write-only	OP[5:3]	WL set A (MR2 OP[6] = 0b)	1, 3, 4
			000b: WL = 4 (default)	
			001b: WL = 6	
			010b: WL = 8	
			011b: WL = 10	
			100b: WL = 12	
			101b: WL = 14	
			110b: WL = 16	
			111b: WL = 18	
			WL set B (MR2 OP[6] = 1b)	
			000b: WL = 4	
			001b: WL = 8	
			010b: WL = 12	
			011b: WL = 18	
			100b: WL = 22	
			101b: WL = 26	
			110b: WL = 30	
			111b: WL = 34	

Table 61: MR2 Op-Code Bit Definitions (Continued)

Feature	Type	OP	Definition	Notes
WLS WRITE latency set	Write-only	OP[6]	0b: Use WL set A (default)	1, 3, 4
			1b: Use WL set B	
WR Lev Write leveling	Write-only	OP[7]	0b: Disable write leveling (default)	2
			1b: Enable write leveling	

Notes: 1. See Latency Code Frequency Table for allowable frequency ranges for RL/WL/*n*WR.
2. After an MRW command to set the write leveling enable bit (OP[7] = 1b), the device remains in the MRW state until another MRW command clears the bit (OP[7] = 0b). No other commands are allowed until the write leveling enable bit is cleared.
3. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command this MR address, or read from with an MRR command to this address.
4. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, that is, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.
5. *n*RTP is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the *n*RTP value before starting a precharge.

Table 62: Frequency Ranges for RL, WL, *n*WR, and *n*RTP Settings

READ Latency		WRITE Latency							
No DBI	w/DBI	Set A	Set B	*n*WR	*n*RTP	Lower Frequency Limit (>)	Upper Frequency Limit(≤)	Units	Notes
6	6	4	4	6	8	10	266	MHz	1–6
10	12	6	8	10	8	266	533		
14	16	8	12	16	8	533	800		
20	22	10	18	20	8	800	1066		
24	28	12	22	24	10	1066	1333		
28	32	14	26	30	12	1333	1600		
32	36	16	30	34	14	1600	1866		
36	40	18	34	40	16	1866	2133		

Notes: 1. The device should not be operated at a frequency above the upper frequency limit or below the lower frequency limit shown for each RL, WL, or *n*WR value.
2. DBI for READ operations is enabled in MR3 OP[6]. When MR3 OP[6] = 0, then the "No DBI" column should be used for READ latency. When MR3 OP[6] = 1, then the "w/DBI" column should be used for READ latency.
3. WRITE latency set A and set B are determined by MR2 OP[6]. When MR2 OP[6] = 0, then WRITE latency set A should be used. When MR2 OP[6] = 1, then WRITE latency set B should be used.
4. The programmed value for *n*RTP is the number of clock cycles the device uses to determine the starting point of an internal PRECHARGE operation after a READ burst with AP (auto precharge) enabled . It is determined by RU(^{t}RTP/^{t}CK).
5. The programmed value of *n*WR is the number of clock cycles the device uses to determine the starting point of an internal PRECHARGE operation after a WRITE burst with AP (auto precharge) enabled. It is determined by RU(^{t}WR/^{t}CK).
6. *n*RTP shown in this table is valid for BL16 only. For BL32, the device will add 8 clocks to the *n*RTP value before starting a precharge.

Table 63: MR3 I/O Configuration 1 (MA[5:0] = 03h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DBI-WR	DBI-RD	PDDS			PPRP	WR-PST	PU-CAL

Table 64: MR3 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
PU-CAL (Pull-up calibration point)	Write-only	OP[0]	0b: V_{DDQ} × 0.6	1–4
			1b: V_{DDQ} × 0.5 (default)	
WR-PST (WR postamble length)		OP[1]	0b: WR postamble = 0.5 × ^{t}CK (default)	2, 3, 5
			1b: WR postamble = 1.5 × ^{t}CK	
PPRP (Post-package repair protection)		OP[2]	0b: PPR protection disabled (default)	6
			1b: PPR protection enabled	
PDDS (Pull-down drive strength)		OP[5:3]	000b: RFU	1, 2, 3
			001b: R_{ZQ}/1	
			010b: R_{ZQ}/2	
			011b: R_{ZQ}/3	
			100b: R_{ZQ}/4	
			101b: R_{ZQ}/5	
			110b: R_{ZQ}/6 (default)	
			111b: Reserved	
DBI-RD (DBI-read enable)		OP[6]	0b: Disabled (default)	2, 3
			1b: Enabled	
DBI-WR (DBI-write enable)		OP[7]	0b: Disabled (default)	2, 3
			1b: Enabled	

Notes:
1. All values are typical. The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Recalibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1.The device will operate only according to the values stored in the registers for the active set point, for example, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. For dual-channel device, PU-CAL (MR3-OP[0]) must be set the same for both channels on a die. The SDRAM will read the value of only one register (Ch.A or Ch.B); the choice is vendor-specific, so both channels must be set the same.
5. 1.5 × ^{t}CK apply > 1.6 GHz clock.
6. If MR3 OP[2] is set to 1b, PPR protection mode is enabled. The PPR protection bit is a sticky bit and can only be set to 0b by a power on reset. MR4 OP[4] controls entry to PPR mode. If PPR protection is enabled then the DRAM will not allow writing of 1b to MR4 OP[4].

Table 65: MR4 Device Temperature (MA[5:0] = 04h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	Thermal offset		PPRE	SR abort	Refresh rate		

Table 66: MR4 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
Refresh rate	Read-only	OP[2:0]	000b: SDRAM low temperature operating limit exceeded	1–4, 7–9
			001b: 4x refresh	
			010b: 2x refresh	
			011b: 1x refresh (default)	
			100b: 0.5x refresh	
			101b: 0.25x refresh, no derating	
			110b: 0.25x refresh, with derating	
			111b: SDRAM high temperature operating limit exceeded	
SR abort (Self refresh abort)	Write	OP[3]	0b: Disable (default)	9
			1b: Device dependent	
PPRE (Post-package repair entry/exit)	Write	OP[4]	0b: Exit PPR mode (default)	5, 9
			1b: Enter PPR mode (Reference MR25 OP[7:0] for available PPR resources)	
Thermal offset-controller offset to TCSR	Write	OP[6:5]	00b: No offset, 0–5°C gradient (default)	9
			01b: 5°C offset, 5–10°C gradient	
			10b: 10°C offset, 10–15°C gradient	
			11b: Reserved	
TUF (Temperature update flag)	Read-only	OP7	0b: OP[2:0] No change in OP[2:0] since last MR4 read (default)	6–8
			1b: Change in OP[2:0] since last MR4 read	

Notes: 1. The refresh rate for each MR4 OP[2:0] setting applies to ^{t}REFI, ^{t}REFIpb, and ^{t}REFW. MR4 OP[2:0] = 011b corresponds to a device temperature of 85°C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If MR4 OP[2] = 1b, the device temperature is greater than 85°C.
2. At higher temperatures (>85°C), AC timing derating may be required. If derating is required the device will set MR4 OP[2:0] = 110b. See derating timing requirements in the AC Timing section.
3. DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
4. The device may not operate properly when MR4 OP[2:0] = 000b or 111b.
5. Post-package repair can be entered or exited by writing to MR4 OP[4].
6. When MR4 OP[7] = 1b, the refresh rate reported in MR4 OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset MR4 OP[7] to 0b.
7. MR4 OP[7] = 0b at power-up. MR4 OP[2:0] bits are valid after initialization sequence (Te).
8. See the Temperature Sensor section for information on the recommended frequency of reading MR4.
9. MR4 OP[6:3] can be written in this register. All other bits will be ignored by the device during an MRW command to this register.

Table 67: MR5 Basic Configuration 1 (MA[5:0] = 05h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID							

Table 68: MR5 Op-Code Bit Definitions

Feature	Type	OP	Definition
Manufacturer ID	Read-only	OP[7:0]	1111 1111b: Micron
			All others: Reserved

Table 69: MR6 Basic Configuration 2 (MA[5:0] = 06h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Note: 1. MR6 is vendor-specific.

Table 70: MR6 Op-Code Bit Definitions

Feature	Type	OP	Definition
Revision ID1	Read-only	OP[7:0]	xxxx xxxxb: Revision ID1

Note: 1. MR6 is vendor-specific.

Table 71: MR7 Basic Configuration 3 (MA[5:0] = 07h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Table 72: MR7 Op-Code Bit Definitions

Feature	Type	OP	Definition
Revision ID2	Read-only	OP[7:0]	xxxx xxxxb: Revision ID2

Note: 1. MR7 is vendor-specific.

Table 73: MR8 Basic Configuration 4 (MA[5:0] = 08h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Table 74: MR8 Op-Code Bit Definitions

Feature	Type	OP	Definition
Type	Read-only	OP[1:0]	00b: S16 SDRAM (16*n* prefetch)
			All others: Reserved
Density	Read-only	OP[5:2]	0000b: 4Gb dual-channel die/2Gb single-channel die
			0001b: 6Gb dual-channel die/3Gb single-channel die
			0010b: 8Gb dual-channel die/4Gb single-channel die
			0011b: 12Gb dual-channel die/6Gb single-channel die
			0100b: 16Gb dual-channel die/8Gb single-channel die
			0101b: 24Gb dual-channel die/12Gb single-channel die
			0110b: 32Gb dual-channel die/16Gb single-channel die
			1100b: 2Gb dual-channel die/1Gb single-channel die
			All others: Reserved
I/O width	Read-only	OP[7:6]	00b: x16/channel
			01b: x8/channel
			All others: Reserved

Table 75: MR9 Test Mode (MA[5:0] = 09h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific test mode							

Table 76: MR9 Op-Code Definitions

Feature	Type	OP	Definition
Test mode	Write-only	OP[7:0]	0000000b; Vendor-specific test mode disabled (default)

Table 77: MR10 Calibration (MA[5:0] = 0Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU							ZQ RESET

Table 78: MR10 Op-Code Bit Definitions

Feature	Type	OP	Definition
ZQ reset	Write-only	OP[0]	0b: Normal operation (default)
			1b: ZQ reset

Notes: 1. See AC Timing table for calibration latency and timing.

2. If ZQ is connected to V_{DDQ} through R_{ZQ}, either the ZQ CALIBRATION function or default calibration (via ZQ reset) is supported. If ZQ is connected to V_{SS}, the device operates with default calibration and ZQ CALIBRATION commands are ignored. In both cases, the ZQ connection must not change after power is supplied to the device.

Table 79: MR11 ODT Control (MA[5:0] = 0Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	CA ODT			RFU	DQ ODT		

Table 80: MR11 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
DQ ODT DQ bus receiver on-die termination	Write-only	OP[2:0]	000b: Disable (default)	1, 2, 3
			001b: RZQ/1	
			010b: RZQ/2	
			011b: RZQ/3	
			100b: RZQ/4	
			101b: RZQ/5	
			110b: RZQ/6	
			111b: RFU	
CA ODT CA bus receiver on-die termination	Write-only	OP[6:4]	000b: Disable (default)	1, 2, 3
			001b: RZQ/1	
			010b: RZQ/2	
			011b: RZQ/3	
			100b: RZQ/4	
			101b: RZQ/5	
			110b: RZQ/6	
			111b: RFU	

Notes: 1. All values are typical. The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, for example, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

Table 81: MR12 Register Information (MA[5:0] = 0Ch)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	VR_{CA}	$V_{REF(CA)}$					

Table 82: MR12 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
$V_{REF(CA)}$ $V_{REF(CA)}$ settings	Read/Write	OP[5:0]	000000b–110010b: See V_{REF} Settings table	1–3, 5, 6
			All others: Reserved	
VR_{CA} $V_{REF(CA)}$ range	Read/Write	OP[6]	0b: $V_{REF(CA)}$ range[0] enabled	1, 2, 4, 5, 6
			1b: $V_{REF(CA)}$ range[1] enabled (default)	

Notes: 1. This register controls the $V_{REF(CA)}$ levels for frequency set point[1:0]. Values from either VR(ca)[0] or VR(ca)[1] may be selected by setting MR12 OP[6] appropriately.

2. A read to MR12 places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ will be set to 0. See the MRR Operation section.
3. A write to MR12 OP[5:0] sets the internal $V_{REF(CA)}$ level for FSP[0] when MR13 OP[6] = 0b or sets the internal $V_{REF(CA)}$ level for FSP[1] when MR13 OP[6] = 1b. The time required for $V_{REF(CA)}$ to reach the set level depends on the step size from the current level to the new level. See the $V_{REF(CA)}$ training section.
4. A write to MR12 OP[6] switches the device between two internal $V_{REF(CA)}$ ranges. The range (range[0] or range[1]) must be selected when setting the $V_{REF(CA)}$ register. The value, once set, will be retained until overwritten or until the next power-on or reset event.
5. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, for example, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 83: MR13 Register Control (MA[5:0] = 0Dh)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT

Table 84: MR13 Op-Code Bit Definition

Feature	Type	OP	Definition	Notes
CBT Command bus training	Write-only	OP[0]	0b: Normal operation (default)	1
			1b: Command bus training mode enabled	
RPT Read preamble training		OP[1]	0b: Disabled (default)	
			1b: Read preamble training mode enabled	
VRO V_{REF} output		OP[2]	0b: Normal operation (default)	2
			1b: Output the $V_{REF(CA)}$ and $V_{REF(DQ)}$ values on DQ bits	
VRCG V_{REF} current generator		OP[3]	0b: Normal operation (default)	3
			1b: Fast response (high current) mode	
RRO Refresh rate option		OP[4]	0b: Disable codes 001 and 010 in MR4 OP[2:0]	4, 5
			1b: Enable all codes in MR4 OP[2:0]	
DMD Data mask disable		OP[5]	0b: DATA MASK operation enabled (default)	6
			1b: DATA MASK operation disabled	
FSP-WR Frequency set point write/read		OP[6]	0b: Frequency set point[0] (default)	7
			1b: Frequency set point[1]	
FSP-OP FREQUENCY SET POINT operation mode		OP[7]	0b: Frequency set point[0] (default)	8
			1b: Frequency set point[1]	

Notes: 1. A write to set OP[0] = 1 causes the LPDDR4 SDRAM to enter the command bus training mode. When OP[0] = 1 and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0] = 0) and return to normal operation. See the Command Bus Training section for more information.
2. When set, the device will output the $V_{REF(CA)}$ and $V_{REF(DQ)}$ voltage on DQ pins. Only the "active" frequency set point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal V_{REF} levels. The DQ pins used for V_{REF} output are vendor-specific.
3. When OP[3] = 1, the V_{REF} circuit uses a high current mode to improve V_{REF} settling time.

4. MR13 OP[4] RRO bit is valid only when MR0 OP[0] = 1. For LPDDR4 SDRAM with MR0 OP[0] = 0, MR4 OP[2:0] bits are not dependent on MR13 OP[4].
5. When OP[4] = 0, only 001b and 010b in MR4 OP[2:0] are disabled. LPDDR4 SDRAM must report 011b instead of 001b or 010b in this case. Controller should follow the refresh mode reported by MR4 OP[2:0], regardless of RRO setting. TCSR function does not depend on RRO setting.
6. When enabled (OP[5] = 0b) data masking is enabled for the device. When disabled (OP[5] = 1b), the device will ignore any mask patterns issued during a MASKED WRITE command. See the Data Mask section for more information.
7. FSP-WR determines which frequency set point registers are accessed with MRW and MRR commands for the following functions such as $V_{REF(CA)}$ setting, $V_{REF(CA)}$ range, $V_{REF(DQ)}$ setting, $V_{REF(DQ)}$ range. For more information, refer to Frequency Set Point section.
8. FSP-OP determines which frequency set point register values are currently used to specify device operation for the following functions such as $V_{REF(CA)}$ setting, $V_{REF(CA)}$ range, $V_{REF(DQ)}$ setting, $V_{REF(DQ)}$ range. For more information, refer to Frequency Set Point section.

Table 85: Mode Register 14 (MA[5:0] = 0Eh)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	VR_{DQ}	$V_{REF(DQ)}$					

Table 86: MR14 Op-Code Bit Definition

Feature	Type	OP	Definition	Notes
$V_{REF(DQ)}$ $V_{REF(DQ)}$ setting	Read/Write	OP[5:0]	000000b–110010b: See V_{REF} Settings table	1–3, 5, 6
			All others: Reserved	
VR_{DQ} $V_{REF(DQ)}$ range		OP[6]	0b: $V_{REF(DQ)}$ range[0] enabled	1, 2, 4–6
			1b: $V_{REF(DQ)}$ range[1] enabled (default)	

Notes: 1. This register controls the $V_{REF(DQ)}$ levels for frequency set point[1:0]. Values from either VR_{DQ}[0] (vendor defined) or VR_{DQ}[1] (vendor defined) may be selected by setting OP[6] appropriately.
2. A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ shall be set to 0. See the MRR Operation section.
3. A write to OP[5:0] sets the internal $V_{REF(DQ)}$ level for FSP[0] when MR13 OP[6] = 0b, or sets FSP[1] when MR13 OP[6] = 1b. The time required for $V_{REF(DQ)}$ to reach the set level depends on the step size from the current level to the new level. See the $V_{REF(DQ)}$ training section.
4. A write to OP[6] switches the device between two internal $V_{REF(DQ)}$ ranges. The range (range[0] or range[1]) must be selected when setting the $V_{REF(DQ)}$ register. The value, once set, will be retained until overwritten, or until the next power-on or reset event.
5. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, for example, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 87: V_{REF} Setting for Range[0] and Range[1]

Function	OP	Range[0] Values		Range[1] Values	
		$V_{REF(CA)}$ (% of V_{DDQ}) $V_{REF(DQ)}$ (% of V_{DDQ})		$V_{REF(CA)}$ (% of V_{DDQ}) $V_{REF(DQ)}$ (% of V_{DDQ})	
V_{REF} setting for MR12 and MR14	OP[5:0]	000000b: 15.0%	011010b: 30.5%	000000b: 32.9%	011010b: 48.5%
		000001b: 15.6%	011011b: 31.1%	000001b: 33.5%	011011b: 49.1%
		000010b: 16.2%	011100b: 31.7%	000010b: 34.1%	011100b: 49.7%
		000011b: 16.8%	011101b: 32.3%	000011b: 34.7%	011101b: 50.3% (default)
		000100b: 17.4%	011110b: 32.9%	000100b: 35.3%	011110b: 50.9%
		000101b: 18.0%	011111b: 33.5%	000101b: 35.9%	011111b: 51.5%
		000110b: 18.6%	100000b: 34.1%	000110b: 36.5%	100000b: 52.1%
		000111b: 19.2%	100001b: 34.7%	000111b: 37.1%	100001b: 52.7%
		001000b: 19.8%	100010b: 35.3%	001000b: 37.7%	100010b: 53.3%
		001001b: 20.4%	100011b: 35.9%	001001b: 38.3%	100011b: 53.9%
		001010b: 21.0%	100100b: 36.5%	001010b: 38.9%	100100b: 54.5%
		001011b: 21.6%	100101b: 37.1%	001011b: 39.5%	100101b: 55.1%
		001100b: 22.2%	100110b: 37.7%	001100b: 40.1%	100110b: 55.7%
		001101b: 22.8%	100111b: 38.3%	001101b: 40.7%	100111b: 56.3%
		001110b: 23.4%	101000b: 38.9%	001110b: 41.3%	101000b: 56.9%
		001111b: 24.0%	101001b: 39.5%	001111b: 41.9%	101001b: 57.5%
		010000b: 24.6%	101010b: 40.1%	010000b: 42.5%	101010b: 58.1%
		010001b: 25.1%	101011b: 40.7%	010001b: 43.1%	101011b: 58.7%
		010010b: 25.7%	101100b: 41.3%	010010b: 43.7%	101100b: 59.3%
		010011b: 26.3%	101101b: 41.9%	010011b: 44.3%	101101b: 59.9%
		010100b: 26.9%	101110b: 42.5%	010100b: 44.9%	101110b: 60.5%
		010101b: 27.5%	101111b: 43.1%	010101b: 45.5%	101111b: 61.1%
		010110b: 28.1%	110000b: 43.7%	010110b: 46.1%	110000b: 61.7%
		010111b: 28.7%	110001b: 44.3%	010111b: 46.7%	110001b: 62.3%
		011000b: 29.3%	110010b: 44.9%	011000b: 47.3%	110010b: 62.9%
		011001b: 29.9%	All others: Reserved	011001b: 47.9%	All others: Reserved

Notes: 1. These values may be used for MR14 OP[5:0] and MR12 OP[5:0] to set the $V_{REF(CA)}$ or $V_{REF(DQ)}$ levels in the device.
2. The range may be selected in each of the MR14 or MR12 registers by setting OP[6] appropriately.
3. Each of the MR14 or MR12 registers represents either FSP[0] or FSP[1]. Two frequency set points each for CA and DQ are provided to allow for faster switching between terminated and unterminated operation or between different high-frequency settings, which may use different terminations values.
4. Notes 1–3 apply to entire table.

Table 88: MR15 Register Information (MA[5:0] = 0Fh)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Lower-byte invert register for DQ calibration							

Table 89: MR15 Op-code Bit Definition

Feature	Type	OP	Definition	Notes
Lower-byte invert for DQ calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0] and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane	1–3
			0b: Do not invert 1b: Invert the DQ calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55h	

Notes: 1. This register will invert the DQ calibration pattern found in MR32 and MR40 for any single DQ or any combination of DQ. Example: If MR15 OP[7:0] = 00010101b, then the DQ calibration patterns transmitted on DQ[7, 6, 5, 3, 1] will not be inverted, but the DQ calibration patterns transmitted on DQ[4, 2, 0] will be inverted.
2. DM[0] is not inverted and always transmits the "true" data contained in MR32 and MR40.
3. No DATA BUS INVERSION (DBI) function is enacted during read DQ calibration, even if DBI is enabled in MR3-OP[6].

Table 90: MR15 Invert Register Pin Mapping

PIN	DQ0	DQ1	DQ2	DQ3	DMIO	DQ4	DQ5	DQ6	DQ7
MR15	OP0	OP1	OP2	OP3	No invert	OP4	OP5	OP6	OP7

Table 91: MR16 PASR Bank Mask (MA[5:0] = 010h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR bank mask							

Table 92: MR16 Op-Code Bit Definitions

Feature	Type	OP	Definition
Bank[7:0] mask	Write-only	OP[7:0]	0b: Bank refresh enabled (default)
			1b: Bank refresh disabled

OP[n]	Bank Mask	8-Bank SDRAM
0	xxxxxxx1	Bank 0
1	xxxxxx1x	Bank 1
2	xxxxx1xx	Bank 2
3	xxxx1xxx	Bank 3
4	xxx1xxxx	Bank 4
5	xx1xxxxx	Bank 5
6	x1xxxxxx	Bank 6
7	1xxxxxxx	Bank 7

Notes: 1. When a mask bit is asserted (OP[*n*] = 1), refresh to that bank is disabled.
2. PASR bank masking is on a per-channel basis; the two channels on the die may have different bank masking in dual-channel devices.

Table 93: MR17 PASR Segment Mask (MA[5:0] = 11h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR segment mask							

Table 94: MR17 PASR Segment Mask Definitions

Feature	Type	OP	Definition
Segment[7:0] mask	Write-only	OP[7:0]	0b: Segment refresh enabled (default)
			1b: Segment refresh disabled

Table 95: MR17 PASR Segment Mask

Segment	OP	Segment Mask	Density (per channel)							
			1Gb	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb
			R[12:10]	R[13:11]	R[14:12]	R[14:12]	R[15:13]	R[15:13]	R[16:14]	R[16:14]
0	0	XXXXXXX1	000b							
1	1	XXXXXX1X	001b							
2	2	XXXXX1XX	010b							
3	3	XXXX1XXX	011b							
4	4	XXX1XXXX	100b							
5	5	XX1XXXXX	101b							
6	6	X1XXXXXX	110b	110b	Not allowed	110b	Not allowed	110b	Not allowed	110b
7	7	1XXXXXXX	111b	111b		111b		111b		111b

Notes: 1. This table indicates the range of row addresses in each masked segment. "X" is “Don’t Care” for a particular segment.
2. PASR segment-masking is on a per-channel basis. The two channels on the die may have different segment masking in dual-channel devices.
3. For 3Gb, 6Gb, and 12Gb density per channel, OP[7:6] must always be LOW (= 00b).

Table 96: MR18 Register Information (MA[5:0] = 12h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS oscillator count - LSB							

Table 97: MR18 LSB DQS Oscillator Count

Function	Type	OP	Definition
DQS oscillator count (WR training DQS oscillator)	Read-only	OP[7:0]	0h–FFh LSB DRAM DQS oscillator count

Notes: 1. MR18 reports the LSB bits of the DRAM DQS oscillator count. The DRAM DQS oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS oscillator count.
3. The value in this register is reset each time an MPC command is issued to start in the DQS oscillator counter.
4. Notes 1–3 apply to entire table.

Table 98: MR19 Register Information (MA[5:0] = 13h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS oscillator count – MSB							

Table 99: MR19 DQS Oscillator Count

Function	Type	OP	Definition
DQS oscillator count – MSB (WR training DQS oscillator)	Read-only	OP[7:0]	0h–FFh MSB DRAM DQS oscillator count

Notes: 1. MR19 reports the MSB bits of the DRAM DQS oscillator count. The DRAM DQS oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS oscillator count.
3. A new MPC[START DQS OSCILLATOR] should be issued to reset the contents of MR18/MR19.
4. Notes 1–3 apply to the entire table.

Table 100: MR20 Register Information (MA[5:0] = 14h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Upper-byte invert register for DQ calibration							

Table 101: MR20 Register Information

Function	Type	OP	Definition
Upper-byte invert for DQ calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0] and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane
			0b: Do not invert 1b: Invert the DQ calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55h

Notes: 1. This register will invert the DQ calibration pattern found in MR32 and MR40 for any single DQ or any combination of DQ. For example, if MR20 OP[7:0] = 00010101b, the DQ calibration patterns transmitted on DQ[15, 14, 13, 11, 9] will not be inverted, but the DQ calibration patterns transmitted on DQ[12, 10, 8] will be inverted.
2. DM[1] is not inverted and always transmits the true data contained in MR32 and MR40.
3. No DATA BUS INVERSION (DBI) function is enacted during read DQ calibration, even if DBI is enabled in MR3 OP[6].
4. Notes 1–3 apply to entire table.

Table 102: MR20 Invert Register Pin Mapping

Pin	DQ8	DQ9	DQ10	DQ11	DMI1	DQ12	DQ13	DQ14	DQ15
MR20	OP0	OP1	OP2	OP3	No invert	OP4	OP5	OP6	OP7

Table 103: MR21 Register Information (MA[5:0] = 15h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU							

Table 104: MR22 Register Information (MA[5:0] = 16h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
ODTD for x8_2ch		ODTD-CA	ODTE-CS	ODTE-CK	SOC ODT		

Table 105: MR22 Register Information

Function	Type	OP	Data	Notes
SOC ODT (controller ODT value for V_{OH} calibration)	Write-only	OP[2:0]	000b: Disable (default) 001b: R_{ZQ}/1 (Illegal if MR3 OP[0] = 0b) 010b: R_{ZQ}/2 011b: R_{ZQ}/3 (Illegal if MR3 OP[0] = 0b) 100b: R_{ZQ}/4 101b: R_{ZQ}/5 (Illegal if MR3 OP[0] = 0b) 110b: R_{ZQ}/6 (Illegal if MR3 OP[0] = 0b) 111b: RFU	1, 2, 3
ODTE-CK (CK ODT enabled for non-terminating rank)	Write-only	OP[3]	ODT bond PAD is ignored 0b: ODT-CK enable (default) 1b: ODT-CK disable	2, 3
ODTE-CS (CS ODT enabled for non-terminating rank)	Write-only	OP[4]	ODT bond PAD is ignored 0b: ODT-CS enable (default) 1b: ODT-CS disable	2, 3
ODTD-CA (CA ODT termination disable)	Write-only	OP[5]	ODT bond PAD is ignored 0b: CA ODT enable (default) 1b: CA ODT disable	2, 3
ODTD for x8_2ch (Byte) mode	Write-only	OP[7:6]	See Byte Mode section	

Notes: 1. All values are typical.
2. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, for example, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 106: MR23 Register Information (MA[5:0] = 17h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS interval timer run-time setting							

Table 107: MR23 Register Information

Function	Type	OP	Data
DQS interval timer run-time	Write-only	OP[7:0]	00000000b: Disabled (default)
			00000001b: DQS timer stops automatically at the 16th clock after timer start
			00000010b: DQS timer stops automatically at the 32nd clock after timer start
			00000011b: DQS timer stops automatically at the 48th clock after timer start
			00000100b: DQS timer stops automatically at the 64th clock after timer start
			--------- Through ---------
			00111111b: DQS timer stops automatically at the (63 × 16)th clock after timer start
			01XXXXXXb: DQS timer stops automatically at the 2048th clock after timer start
			10XXXXXXb: DQS timer stops automatically at the 4096th clock after timer start
			11XXXXXXb: DQS timer stops automatically at the 8192nd clock after timer start

Notes: 1. MPC command with OP[6:0] = 1001101b (STOP DQS INTERVAL OSCILLATOR) stops the DQS interval timer in the case of MR23 OP[7:0] = 00000000b.
2. MPC command with OP[6:0] = 1001101b (STOP DQS INTERVAL OSCILLATOR) is illegal with valid nonzero values in MR23 OP[7:0].
3. Notes 1–2 apply to entire table.

Table 108: MR24 Register Information (MA[5:0] = 18h) when MR0 OP[2] = 0b

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TRR mode	TRR mode BAn			Unlimited MAC	MAC value		

Table 109: MR24 Register Information when MR0 OP[2] = 0b

Function	Type	OP	Data	Notes
MAC value	Read	OP[2:0]	000b: Unknown (OP[3] = 0) or unlimited (OP[3] = 1)	1
			001b: 700K	
			010b: 600K	
			011b: 500K	
			100b: 400K	
			101b: 300K	
			110b: 200K	
			111b: Reserved	
Unlimited MAC	Read	OP[3]	0b: OP[2:0] defines the MAC value	2
			1b: Unlimited MAC value	

Table 109: MR24 Register Information when MR0 OP[2] = 0b (Continued)

Function	Type	OP	Data	Notes
TRR mode BAn	Write	OP[6:4]	000b: Bank 0	
			001b: Bank 1	
			010b: Bank 2	
			011b: Bank 3	
			100b: Bank 4	
			101b: Bank 5	
			110b: Bank 6	
			111b: Bank 7	
TRR mode	Write	OP[7]	0b: Disabled (default)	
			1b: Enabled	

Notes: 1. OP[2:0] = 000b Unknown means that the device is not tested for ^{t}MAC and pass/fail values are unknown. OP[2:0] = 000b Unlimited means that there is no restriction on the number of activates between refresh windows. However, specific attempts to by-pass TRR may result in data disturb.
2. When OP[3] = 1b, MR24 OP[2:0] set to 000b.

Table 110: MR24 Register Information (MA[5:0] = 18h) when MR0 OP[2] = 1b

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RAAMMT		RAAIMT					RFM

Table 111: MR24 Register Information when MR0 OP[2] = 1b

Function	Type	OP	Data	Notes
RFM(RFM required)	Read	OP[0]	0b: RFM not required	1
			1b: RFM required	
RAAIMT (Rolling accumulated ACT initial management threshold)	Read	OP[5:1]	00000b: Invalid	1
			00001b: 8	
			00010b: 16	
			.....	
			11110b: 240	
			11111b: 248	
RAAMMT (Rolling accumulated ACT maximum management threshold)	Read	OP[7:6]	00b: 2X	1
			01b: 4X	
			10b: 6X	
			11b: 8X	

Note: 1. Vendor programmed.

Table 112: MR25 Register Information (MA[5:0] = 19h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0

Table 113: MR25 Register Information

Function	Type	OP	Data
PPR resources	Read-only	OP[7:0]	0b: PPR resource is not available
			1b: PPR resource is available

Note: 1. When OP[*n*] = 0, there is no PPR resource available for that bank. When OP[*n*] = 1, there is a PPR resource available for that bank, and PPR can be initiated by the controller.

Table 114: MR26:29 Register Information (MA[5:0] = 1Ah–1Dh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved for future use							

Table 115: MR30 Register Information (MA[5:0] = 1Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid 0 or 1							

Table 116: MR30 Register Information

Function	Type	OP	Data
SDRAM will ignore	Write-only	OP[7:0]	Don't care

Note: 1. This register is reserved for testing purposes. The logical data values written to OP[7:0] will have no effect on SDRAM operation; however, timings need to be observed as for any other MR access command.

Table 117: MR31 Register Information (MA[5:0] = 1Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved for future use							

Table 118: MR32 Register Information (MA[5:0] = 20h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ calibration pattern A (default = 5Ah)							

Table 119: MR32 Register Information

Feature	Type	OP	Data	Notes
Return DQ calibration pattern MR32 + MR40	Write-only	OP[7:0]	Xb: An MPC command issued with OP[6:0] = 1000011b causes the device to return the DQ calibration pattern contained in this register and (followed by) the contents of MR40. A default pattern 5Ah is loaded at power-up or reset, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the MR32/MR40 data pattern for a given DQ (see MR15/MR20 for more information).	1, 2, 3

Notes: 1. The patterns contained in MR32 and MR40 are transmitted on DQ[15:0] and DMI[1:0] when read DQ calibration is initiated via an MPC command. The pattern is transmitted serially on each data lane and organized little endian such that the low-order bit in a byte is transmitted first. If the data pattern is 27H, the first bit transmitted is a 1 followed by 1, 1, 0, 0, 1, 0, and 0. The bit stream will be 00100111.
2. MR15 and MR20 may be used to invert the MR32/MR40 data pattern on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3 OP[6].
4. No DATA BUS INVERSION (DBI) function is enacted during read DQ calibration, even if DBI is enabled in MR3 OP[6].

Table 120: MR33:35 Register Information (MA[5:0] = 21h–23h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Do not use							

Table 121: MR36 Register Information (MA[5:0] = 24h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU						RAADEC	

Table 122: MR36 Register Information

Feature	Type	OP	Data	Notes
RAADEC (RAA count multiplier per RFM command)	Read	OP[1:0]	00b: x1 01b: x1.5 10b: x2 11b: RFU	1

Note: 1. OP[1:0] RAADEC bits are valid only when MR0 OP[2] (RFM support) = 1.

Table 123: MR37:38 Register Information (MA[5:0] = 25h–26h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Do not use							

Table 124: MR39 Register Information (MA[5:0] = 27h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid 0 or 1							

Table 125: MR39 Register Information

Function	Type	OP	Data
SDRAM will ignore	Write-only	OP[7:0]	Don't care

Note: 1. This register is reserved for testing purposes. The logical data values written to OP[7:0] will have no effect on SDRAM operation; however, timings need to be observed as for any other MR access command.

Table 126: MR40 Register Information (MA[5:0] = 28h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ calibration pattern B (default = 3Ch)							

Table 127: MR40 Register Information

Function	Type	OP	Data	Notes
Return DQ calibration pattern MR32 + MR40	Write-only	OP[7:0]	Xb: A default pattern 3Ch is loaded at power-up or reset, or the pattern may be overwritten with a MRW to this register. See MR32 for more information.	1, 2, 3

Notes: 1. The pattern contained in MR40 is concatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when read DQ calibration is initiated via an MPC command. The pattern is transmitted serially on each data lane and organized little endian such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27H, the first bit transmitted will be a 1, followed by 1, 1, 0, 0, 1, 0, and 0. The bit stream will be 00100111.
2. MR15 and MR20 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3 OP[6].
4. No DATA BUS INVERSION (DBI) function is enacted during read DQ calibration, even if DBI is enabled in MR3 OP[6].

Table 128: MR41:47 Register Information (MA[5:0] = 29h–2Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Do not use							

Table 129: MR48:63 Register Information (MA[5:0] = 30h–3Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved for future use							

Commands and Timing

Commands transmitted on the CA bus are encoded into two parts and are latched on two consecutive rising edges of the clock. This is called 2-tick CA capture because each command requires two clock edges to latch and decode the entire command.

Truth Tables

Truth tables provide complementary information to the state diagram. They also clarify device behavior and applicable restrictions when considering the actual state of the banks.

Unspecified operations and timings are illegal. To ensure proper operation after an illegal event, the device must be either reset by asserting the RESET_n command or powered down and then restarted using the specified initialization sequence before normal operation can continue.

CKE signal has to be held HIGH when the commands listed in the command truth table input.

Table 130: Command Truth Table

Command	CS	SDR CA Pins						CK Edge	Notes
		CA0	CA1	CA2	CA3	CA4	CA5		
MRW-1	H	L	H	H	L	L	OP7	↑1	1, 11
	L	MA0	MA1	MA2	MA3	MA4	MA5	↑2	
MRW-2	H	L	H	H	L	H	OP6	↑1	1, 11
	L	OP0	OP1	OP2	OP3	OP4	OP5	↑2	
MRR-1	H	L	H	H	H	L	V	↑1	1, 2, 12
	L	MA0	MA1	MA2	MA3	MA4	MA5	↑2	
REFRESH (all/per bank)	H	L	L	L	H	L	AB	↑1	1, 2, 3, 4, 14, 15
	L	BA0	BA1	BA2	RFM	V	V	↑2	
ENTER SELF REFRESH	H	L	L	L	H	H	V	↑1	1, 2
	L	V						↑2	
ACTIVATE-1	H	H	L	R12	R13	R14	R15	↑1	1, 2, 3, 10
	L	BA0	BA1	BA2	R16	R10	R11	↑2	
ACTIVATE-2	H	R17	R18	R6	R7	R8	R9	↑1	1, 10, 13
	L	R0	R1	R2	R3	R4	R5	↑2	
WRITE-1	H	L	L	H	L	L	BL	↑1	1, 2, 3, 6, 7, 9
	L	BA0	BA1	BA2	V	C9	AP	↑2	
EXIT SELF REFRESH	H	L	L	H	L	H	V	↑1	1, 2
	L	V						↑2	
MASK WRITE-1	H	L	L	H	H	L	BL	↑1	1, 2, 3, 5, 6, 7, 9
	L	BA0	BA1	BA2	V	C9	AP	↑2	
RFU	H	L	L	H	H	H	V	↑1	1, 2
	L	V						↑2	
RFU	H	L	H	L	H	L	V	↑2	1, 2
	L	V						↑2	
RFU	H	L	H	L	H	H	V	↑2	1, 2
	L	V						↑2	
READ-1	H	L	H	L	L	L	BL	↑1	1, 2, 3, 6, 7, 9
	L	BA0	BA1	BA2	V	C9	AP	↑2	
CAS-2 (WRITE-2, MASKED WRITE-2, READ-2, MRR-2, MPC (except NOP))	H	L	H	L	L	H	C8	↑1	1, 8, 9
	L	C2	C3	C4	C5	C6	C7	↑2	
PRECHARGE (all/per bank)	H	L	L	L	L	H	AB	↑1	1, 2, 3, 4
	L	BA0	BA1	BA2	V	V	V	↑2	
MPC (TRAIN, NOP)	H	L	L	L	L	L	OP6	↑1	1, 9
	L	OP0	OP1	OP2	OP3	OP4	OP5	↑2	
DESELECT	L	X						↑1	1, 2

Notes: 1. All commands except for DESELECT are two clock cycles and are defined by the current state of CS and CA[5:0] at the rising edge of the clock. DESELECT command is one clock cycle and is not latched by the device.
2. V = H or L (a defined logic level); X = "Don't Care," in which case CS, CK_t, CK_c, and CA[5:0] can be floated.
3. Bank addresses BA[2:0] determine which bank is to be operated upon.
4. AB HIGH during PRECHARGE or REFRESH commands indicate the command must be applied to all banks, and the bank addresses are "Don't Care."
5. MASK WRITE-1 command only supports BL16. For MASK WRITE-1 commands, CA5 must be driven LOW on the first rising clock cycle (R1).
6. AP HIGH during a WRITE-1, MASK WRITE-1, or READ-1 command indicates that an auto precharge will occur to the bank the command is operating on. AP LOW indicates that no auto precharge will occur and the bank will remain open upon completion of the command.
7. When enabled in the mode register, BL HIGH during a WRITE-1, MASK-WRITE-1, or READ-1 command indicates the burst length should be set on-the-fly to BL = 32; BL LOW during one of these commands indicates the burst length should be set on-the-fly to BL = 16. If on-the-fly burst length is not enabled in the mode register, this bit should be driven to a valid level and is ignored by the device.
8. For CAS-2 commands (WRITE-2, MASK WRITE-2, READ-2, MRR-2, or MPC (only WRITE-FIFO, READ-FIFO, and READ DQ CALIBRATION)), C[1:0] are not transmitted on the CA [5:0] bus and are assumed to be zero. Note that for CAS-2 WRITE-2 or CAS-2 MASK WRITE-2 command, C[3:2] must be driven LOW.
9. WRITE-1, MASK-WRITE-1, READ-1, MODE REGISTER READ-1, or MPC (only WRITE-FIFO, READ-FIFO, and READ DQ CALIBRATION) command must be immediately followed by CAS-2 command consecutively without any other command in between. WRITE-1, MASK WRITE-1, READ-1, MRR-1, or MPC (only WRITE-FIFO, READ-FIFO, and READ DQ CALIBRATION) command must be issued first before issuing CAS-2 command. MPC (only START and STOP DQS OSCILLATOR, ZQCAL START and LATCH) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.
10. The ACTIVATE-1 command must be followed by the ACTIVATE-2 command consecutively without any other command between them. The ACTIVATE-1 command must be issued prior to the ACTIVATE-2 command. When the ACTIVATE-1 command is issued, the ACTIVATE-2 command must be issued before issuing another ACTIVATE-1 command.
11. The MRW-1 command must be followed by the MRW-2 command consecutively without any other command between them. The MRW-1 command must be issued prior to the MRW-2 command.
12. The MRR-1 command must be followed by the CAS-2 command consecutively without any other commands between them. The MRR-1 command must be issued prior to the CAS-2 command.
13. For device densities not requiring R17 and R18, R17 and R18 must both be driven High for every ACT-2 command to maintain backward compatibility.

    For device densities not requiring R18, R18 must be driven High for every ACT-2 command to maintain backward compatibility.
14. CA3 R2 edge is V when RFM is not required, but becomes RFM when read-only MR24 OP[0] = 1b.
15. Issuing the RFMpb or RFMab command allows the device to use the command period for additional refresh management.
16. Commands are transmitted to the device across a six-lane interface and use CK, CKE, and CS to control the capture of transmitted data. This is applies to entire table.

ACTIVATE Command

The ACTIVATE command must be executed before a READ or WRITE command can be issued. The ACTIVATE command is issued in two parts: The bank and upper-row addresses are entered with activate-1 and the lower-row addresses are entered with ACTIVATE-2. ACTIVATE-1 and ACTIVATE-2 are executed by strobing CS HIGH while setting CA[5:0] at valid levels (see Command table) at the rising edge of CK.

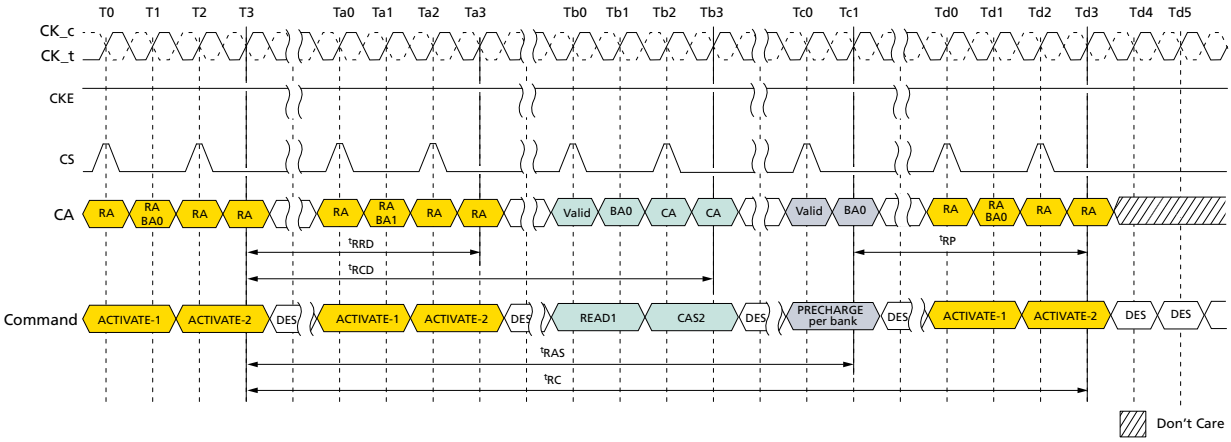
The bank addresses (BA[2:0]) are used to select the desired bank. The row addresses (R[15:0]) are used to determine which row to activate in the selected bank. The ACTIVATE-2 command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at time ^{t}RCD after the ACTIVATE-2 command is sent. After a bank has been activated, it must be precharged to close the active row before another ACTIVATE-2 command can be applied to the same bank. The bank active and precharge times are defined as ^{t}RAS and ^{t}RP, respectively. The

minimum time interval between successive ACTIVATE-2 commands to the same bank is determined by the row cycle time of the device (tRC). The minimum time interval between ACTIVATE-2 commands to different banks is tRRD.

Certain restrictions must be observed for bank ACTIVATE and REFpb operations.

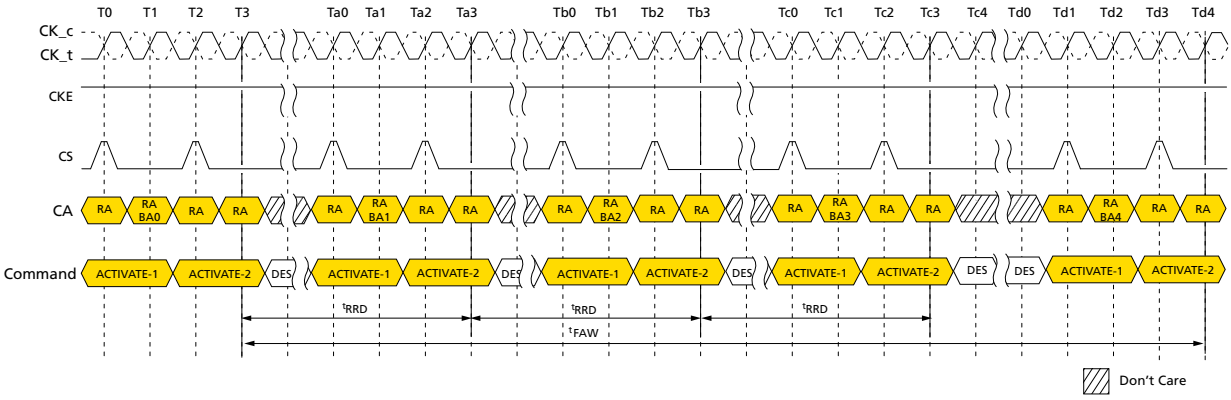
- Four-activate window (tFAW): No more than 4 banks may be activated (or refreshed, in the case of REFpb) per channel in a rolling tFAW window. Convert to clocks by dividing tFAW[ns] by tCK[ns] and rounding up to the next integer value. As an example of the rolling window, if RU[(tFAW/tCK)] is 64 clocks, and an ACTIVATE command is issued on clock N, no more than three additional ACTIVATE commands may be issued between clock N + 1 and N + 63. REFpb also counts as bank activation for the purposes of tFAW.
- 8-bank per channel, precharge all banks (AB) allowance: tRP for a PRECHARGE ALL BANKS command for an 8-bank device must equal tRPab, which is greater than tRPpb.

Figure 95: ACTIVATE Command



Note: 1. A PRECHARGE command uses tRPab timing for all-bank precharge and tRPpb timing for single-bank precharge. In this figure, tRP is used to denote either all-bank precharge or a single-bank precharge. tCCD = MIN, 1.5*n*CK postamble, 533 MHz < clock frequency ≤ 800 MHz, ODT worst timing case.

Figure 96: tFAW Timing



Note: 1. REFpb may be substituted for one of the ACTIVATE commands for the purposes of tFAW.

Read and Write Access Modes

After a bank has been activated, a READ or WRITE command can be executed. This is accomplished by asserting CKE asynchronously, with CS and CA[5:0] set to the proper state (see Command Truth Table) on the rising edge of CK.

The device provides a fast column access operation. A single READ or WRITE command will initiate a burst READ or WRITE operation, where data is transferred to/from the device on successive clock cycles. Burst interrupts are not allowed; however, the optimal burst length may be set on-the-fly (see Command Truth Table).

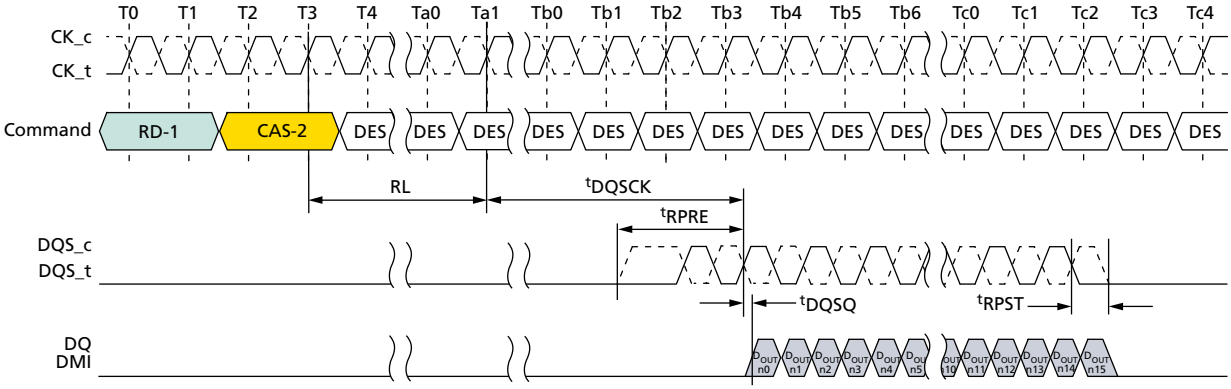
Preamble and Postamble

The DQS strobe for the device requires a preamble prior to the first latching edge (the rising edge of DQS_t with data valid), and it requires a postamble after the last latching edge. The preamble and postamble options are set via MODE REGISTER WRITE commands.

The read preamble is two ^{t}CK in length and is either static or has one clock toggle before the first latching edge. The read preamble option is enabled via MRW to MR1 OP[3] (0 = Static; 1 = Toggle).

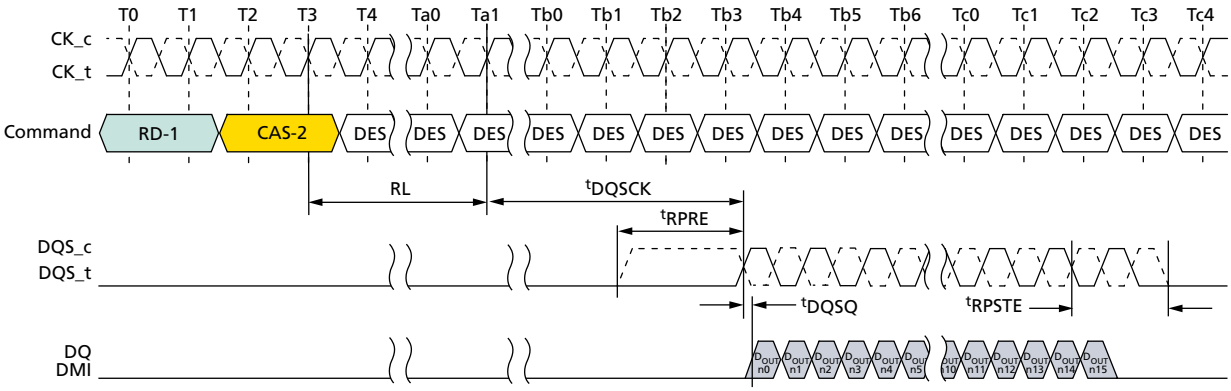
The read postamble has a programmable option to extend the postamble by 1*n*CK (^{t}RPSTE). The extended postamble option is enabled via MRW to MR1 OP[7] (0 = 0.5*n*CK; 1 = 1.5*n*CK).

Figure 97: DQS Read Preamble and Postamble – Toggling Preamble and 0.5*n*CK Postamble



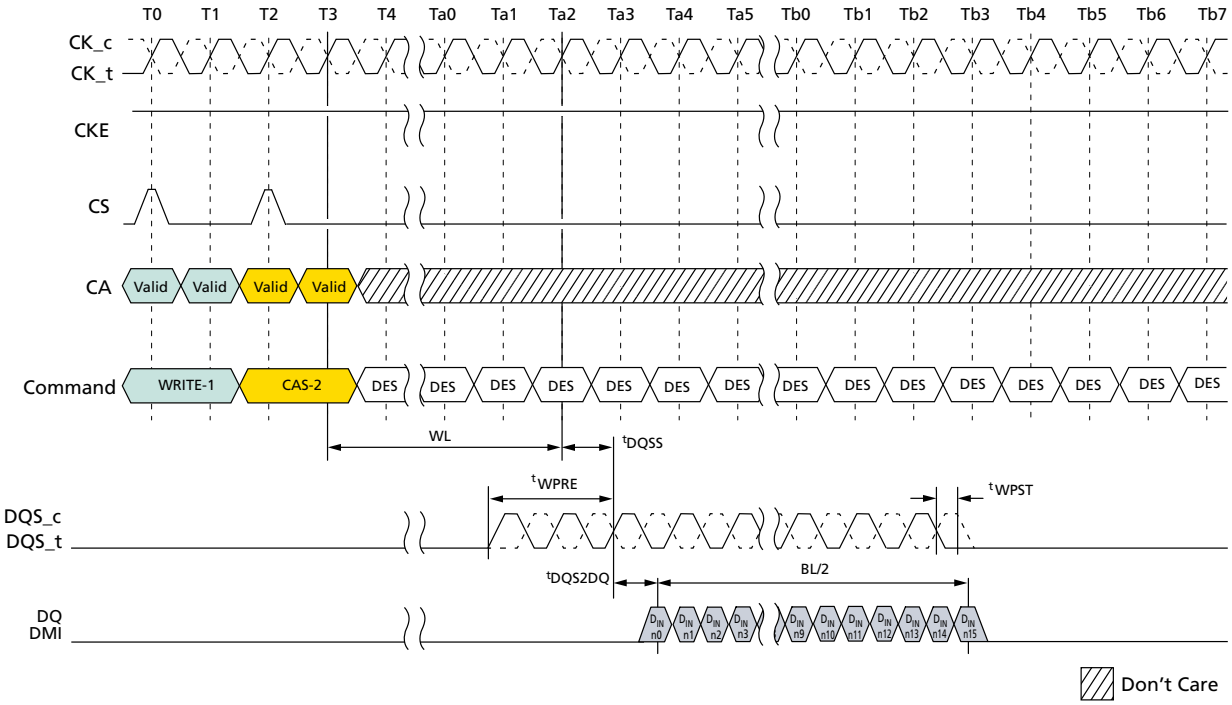
Notes: 1. BL = 16, Preamble = Toggling, Postamble = 0.5*n*CK.
2. DQS and DQ terminated V_{SSQ}.
3. DQS_t/DQS_c is "Don't Care" prior to the start of ^{t}RPRE. No transition of DQS is implied, as DQS_t/DQS_c can be HIGH, LOW, or High-Z prior to ^{t}RPRE.

Figure 98: DQS Read Preamble and Postamble – Static Preamble and 1.5*n*CK Postamble



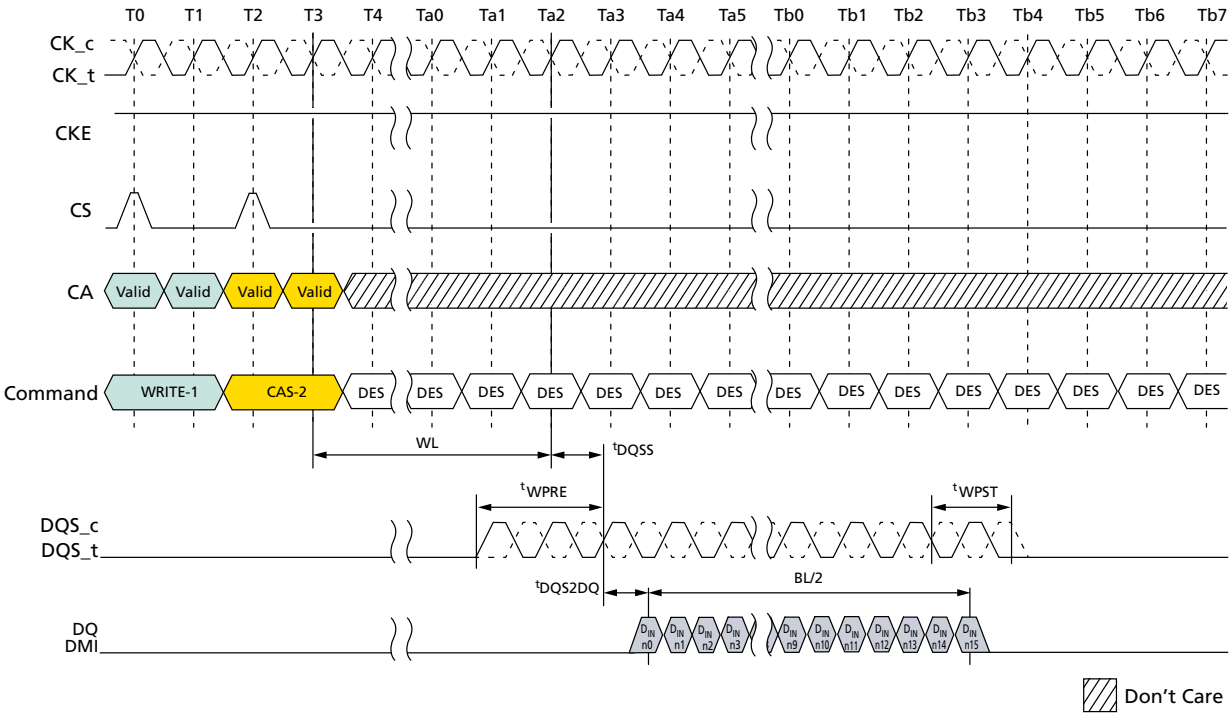
Notes: 1. BL = 16, Preamble = Static, Postamble = 1.5*n*CK (extended).
2. DQS and DQ terminated V_{SSQ}.
3. DQS_t/DQS_c is "Don't Care" prior to the start of ^{t}RPRE. No transition of DQS is implied, as DQS_t/DQS_c can be HIGH, LOW, or High-Z prior to ^{t}RPRE.

Figure 99: DQS Write Preamble and Postamble – 0.5*n*CK Postamble



Notes: 1. BL = 16, Postamble = 0.5*n*CK.
2. DQS and DQ terminated V_{SSQ}.
3. DQS_t/DQS_c is "Don't Care" prior to the start of ^{t}WPRE. No transition of DQS is implied, as DQS_t/DQS_c can be HIGH, LOW, or High-Z prior to ^{t}WPRE.

Figure 100: DQS Write Preamble and Postamble – 1.5*n*CK Postamble



Notes: 1. BL = 16, Postamble = 1.5*n*CK.
2. DQS and DQ terminated V_{SSQ}.
3. DQS_t/DQS_c is "Don't Care" prior to the start of ^{t}WPRE. No transition of DQS is implied, as DQS_t/DQS_c can be HIGH, LOW, or High-Z prior to ^{t}WPRE.

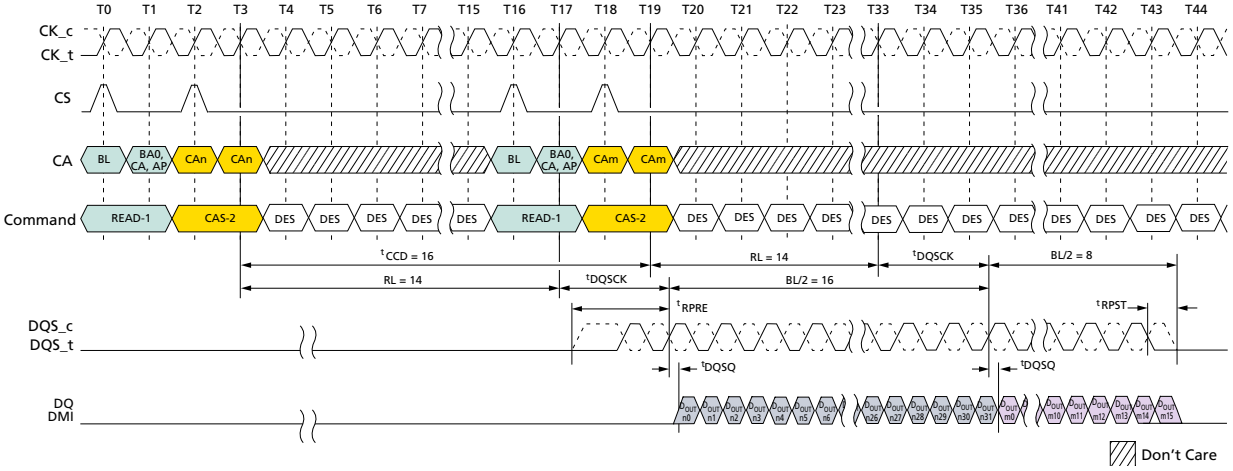
Burst READ Operation

A burst READ command is initiated with CKE, CS, and CA[5:0] asserted to the proper state on the rising edge of CK, as defined by the Command Truth Table. The command address bus inputs determine the starting column address for the burst. The two low-order address bits are not transmitted on the CA bus and are implied to be 0; therefore, the starting burst address is always a multiple of four (that is, 0x0, 0x4, 0x8, 0xC).

The READ latency (RL) is defined from the last rising edge of the clock that completes a READ command (for example, the second rising edge of the CAS-2 command) to the rising edge of the clock from which the ^{t}DQSCK delay is measured. The first valid data is available RL × ^{t}CK + ^{t}DQSCK + ^{t}DQSQ after the rising edge of clock that completes a READ command.

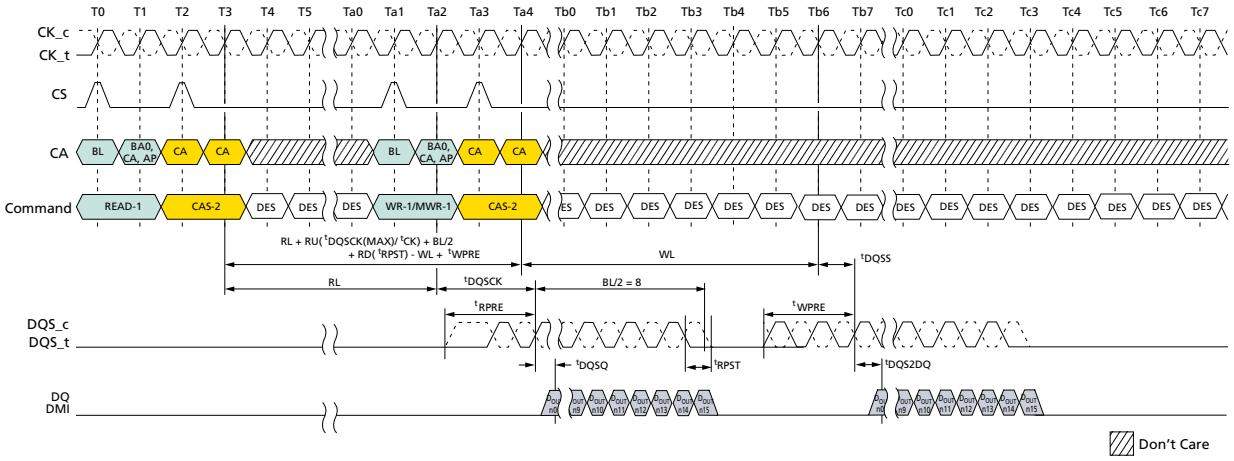
The data strobe output is driven ^{t}RPRE before the first valid rising strobe edge. The first data bit of the burst is synchronized with the first valid (post-preamble) rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edge-aligned with the data strobe. At the end of a burst, the DQS signals are driven for another half cycle postamble, or for a 1.5-cycle postamble if the programmable postamble bit is set in the mode register. The RL is programmed in the mode registers. Pin timings for the data strobe are measured relative to the cross-point of DQS_t and DQS_c.

Figure 101: Burst Read Timing



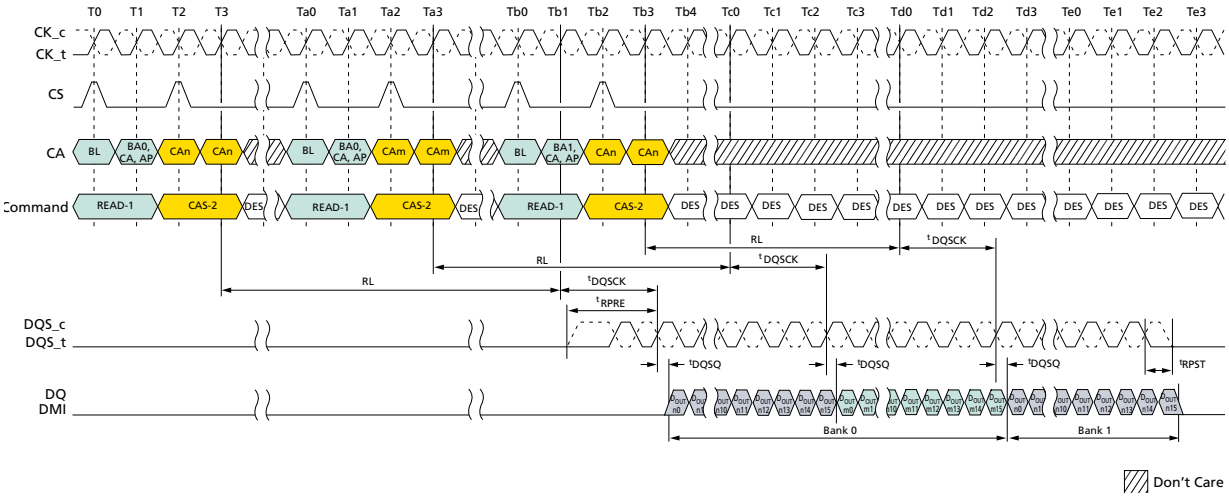
Notes: 1. BL = 32 for column *n*, BL = 16 for column *m*, RL = 14, Preamble = Toggle, Postamble = 0.5*n*CK, DQ/DQS: V_{SSQ} termination.
2. D_{OUT} *n*/*m* = data-out from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 102: Burst Read Followed by Burst Write or Burst Mask Write



Notes: 1. BL = 16, Read preamble = Toggle, Read postamble = 0.5*n*CK, Write preamble = 2*n*CK, Write postamble = 0.5*n*CK, DQ/DQS: V_{SSQ} termination.
2. D_{OUT} *n* = data-out from column *n* and D_{IN} *n* = data-in to column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

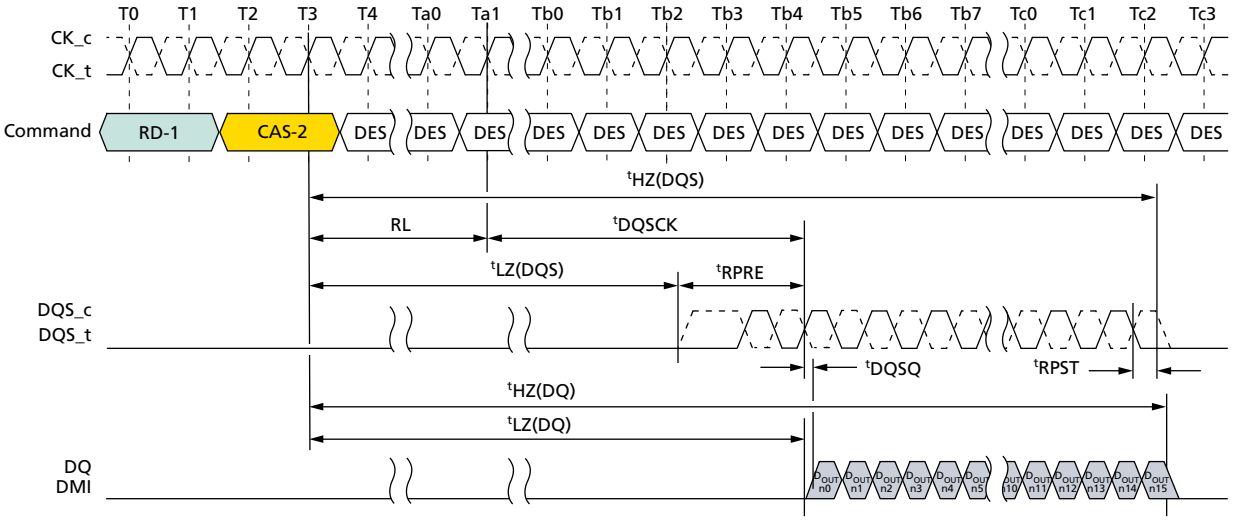
Figure 103: Seamless Burst Read



Notes: 1. BL = 16, ^{t}CCD = 8, Preamble = Toggle, Postamble = 0.5*n*CK, DQ/DQS: V_{SSQ} termination.
2. D_{OUT} *n*/*m* = data-out from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Read Timing

Figure 104: Read Timing



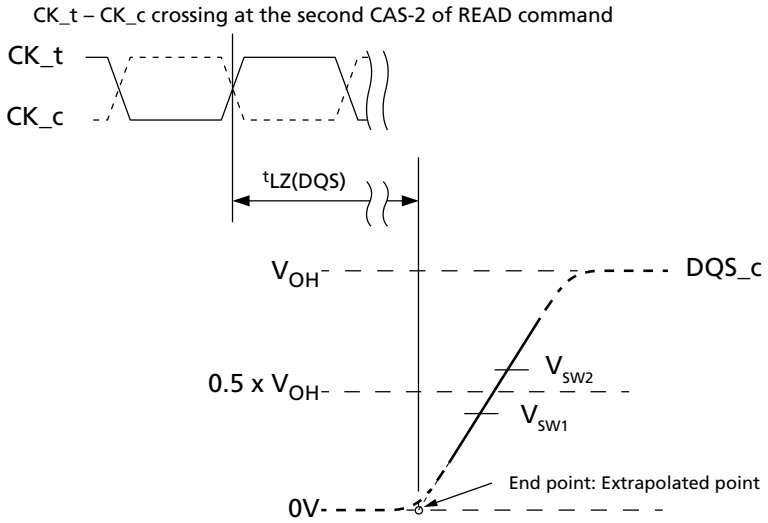
Notes: 1. BL = 16, Preamble = Toggling, Postamble = 0.5*n*CK.
2. DQS, DQ, and DMI terminated V_{SSQ}.
3. Output driver does not turn on before an endpoint of ^{t}LZ(DQS) and ^{t}LZ(DQ).
4. Output driver does not turn off before an endpoint of ^{t}HZ(DQS) and ^{t}HZ(DQ).

^{t}LZ(DQS), ^{t}LZ(DQ), ^{t}HZ(DQS), ^{t}HZ(DQ) Calculation

^{t}HZ and ^{t}LZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving ^{t}HZ(DQS) and ^{t}HZ(DQ), or begins driving ^{t}LZ(DQS) and ^{t}LZ(DQ). This section shows a method to calculate the point when the device is no longer driving ^{t}HZ(DQS) and ^{t}HZ(DQ), or begins driving ^{t}LZ(DQS) and ^{t}LZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters ^{t}LZ(DQS), ^{t}LZ(DQ), ^{t}HZ(DQS), and ^{t}HZ(DQ) are defined as single ended.

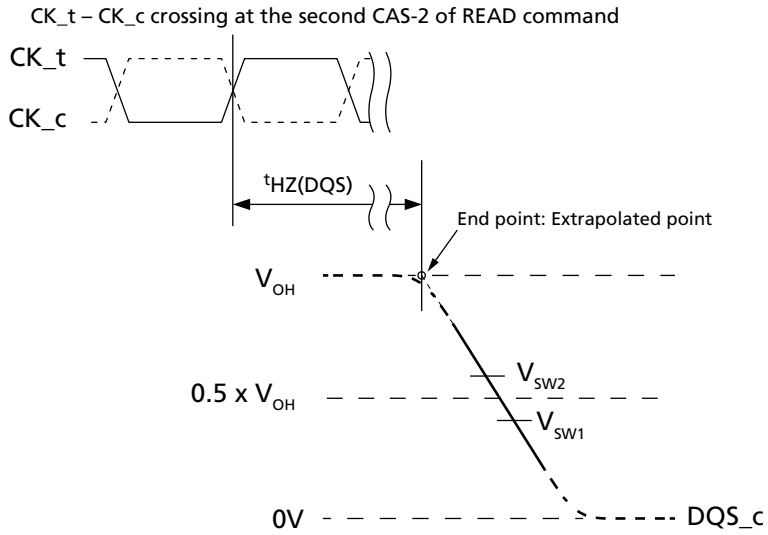
^{t}LZ(DQS) and ^{t}HZ(DQS) Calculation for ATE (Automatic Test Equipment)

Figure 105: ^{t}LZ(DQS) Method for Calculating Transitions and Endpoint



Notes: 1. Conditions for calibration: Pull down driver R_{ON} = 40 ohms, $V_{OH} = V_{DDQ} \times 0.5$.
2. Termination condition for DQS_t and DQS_C = 50 ohms to V_{SSQ}.
3. The V_{OH} level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual V_{OH} value for ^{t}HZ and ^{t}LZ measurements.

Figure 106: ^{t}HZ(DQS) Method for Calculating Transitions and Endpoint



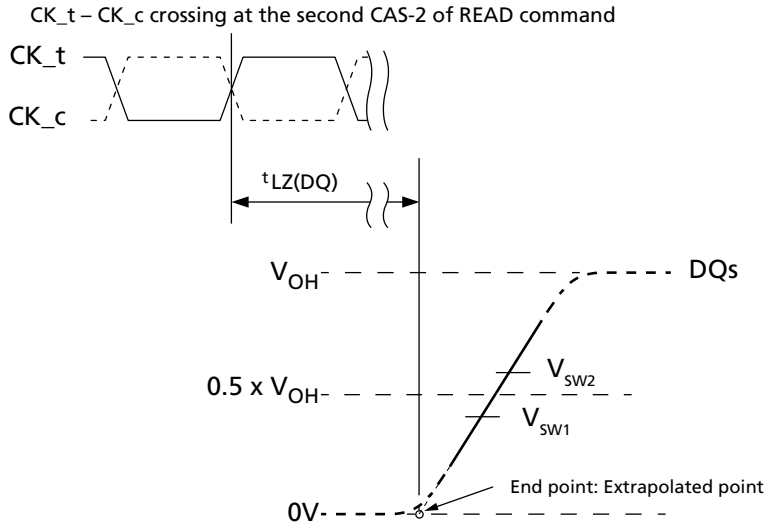
Notes: 1. Conditions for calibration: Pull down driver R_{ON} = 40 ohms, $V_{OH} = V_{DDQ} \times 0.5$.
2. Termination condition for DQS_t and DQS_C = 50 ohms to V_{SSQ}.
3. The V_{OH} level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual V_{OH} value for ^{t}HZ and ^{t}LZ measurements.

Table 131: Reference Voltage for ^{t}LZ(DQS), ^{t}HZ(DQS) Timing Measurements

Measured Parameter	Measured Parameter Symbol	Vsw1	Vsw2	Unit
DQS_c Low-Z time from CK_t, CK_c	^{t}LZ(DQS)	0.4 × V_{OH}	0.6 × V_{OH}	V
DQS_c High-Z time from CK_t, CK_c	^{t}HZ(DQS)	0.4 × V_{OH}	0.6 × V_{OH}	

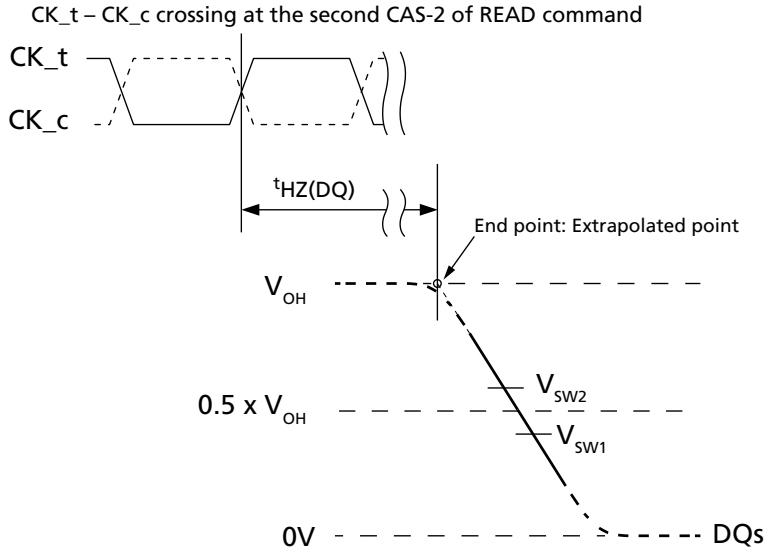
^{t}LZ(DQ) and ^{t}HZ(DQ) Calculation for ATE (Automatic Test Equipment)

Figure 107: ^{t}LZ(DQ) Method for Calculating Transitions and Endpoint



Notes: 1. Conditions for calibration: Pull down driver R_{ON} = 40 ohms, $V_{OH} = V_{DDQ} \times 0.5$.
2. Termination condition for DQ and DMI = 50 ohms to V_{SSQ}.
3. The V_{OH} level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual V_{OH} value for ^{t}HZ and ^{t}LZ measurements.

Figure 108: ^{t}HZ(DQ) Method for Calculating Transitions and Endpoint



Notes: 1. Conditions for calibration: Pull down driver R_{ON} = 40 ohms, $V_{OH} = V_{DDQ} \times 0.5$.
2. Termination condition for DQ and DMI = 50 ohms to V_{SSQ}.
3. The V_{OH} level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual V_{OH} value for ^{t}HZ and ^{t}LZ measurements.

Table 132: Reference Voltage for ^{t}LZ(DQ), ^{t}HZ(DQ) Timing Measurements

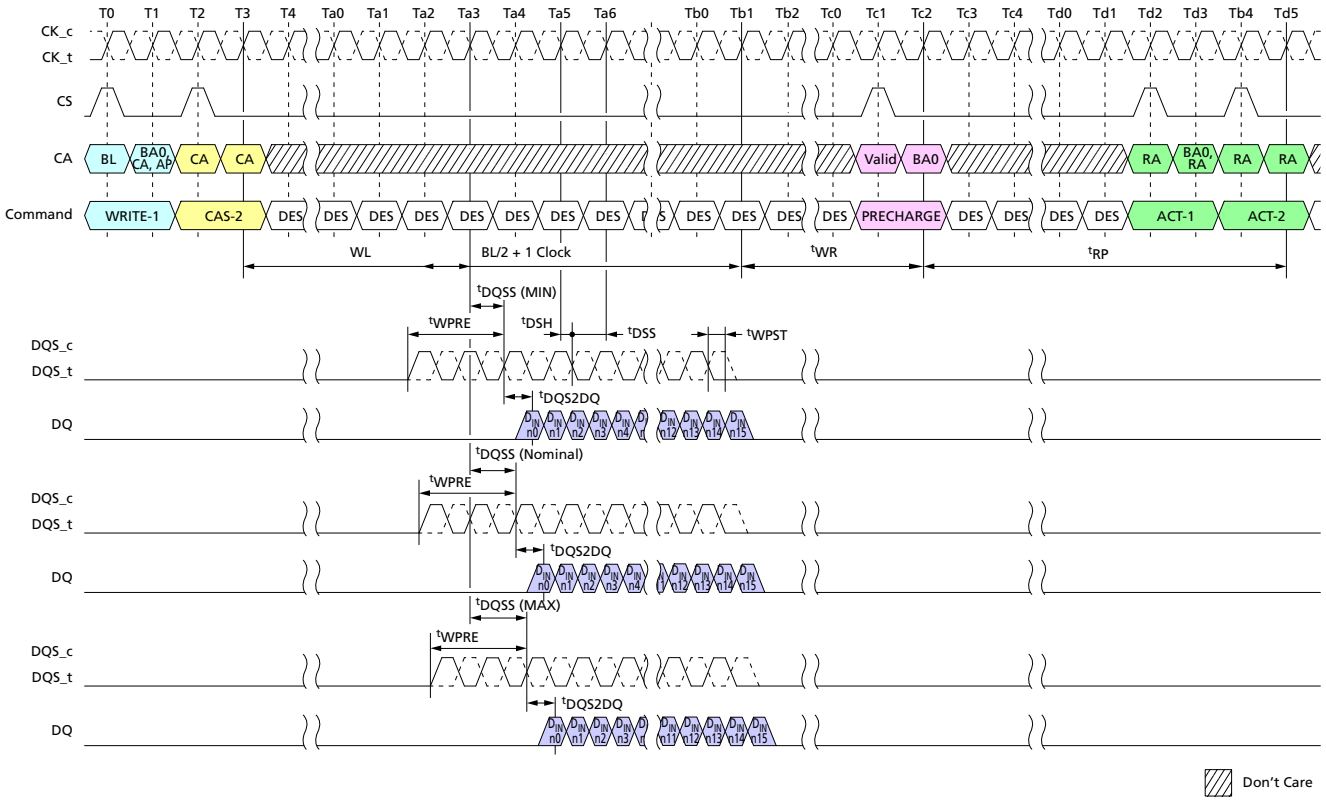
Measured Parameter	Measured Parameter Symbol	Vsw1	Vsw2	Unit
DQ Low-Z time from CK_t, CK_c	^{t}LZ(DQ)	0.4 × V_{OH}	0.6 × V_{OH}	V
DQ High-Z time from CK_t, CK_c	^{t}HZ(DQ)	0.4 × V_{OH}	0.6 × V_{OH}	

Burst WRITE Operation

A burst WRITE command is initiated with CKE, CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. Column addresses C[3:2] should be driven LOW for burst WRITE commands, and column addresses C[1:0] are not transmitted on the CA bus and are assumed to be zero so that the starting column burst address is always aligned with a 32-byte boundary. The WRITE latency (WL) is defined from the last rising edge of the clock that completes a WRITE command (for example, the second rising edge of the CAS-2 command) to the rising edge of the clock from which ^{t}DQSS is measured. The first valid latching edge of DQS must be driven WL × ^{t}CK + ^{t}DQSS after the rising edge of clock that completes a WRITE command.

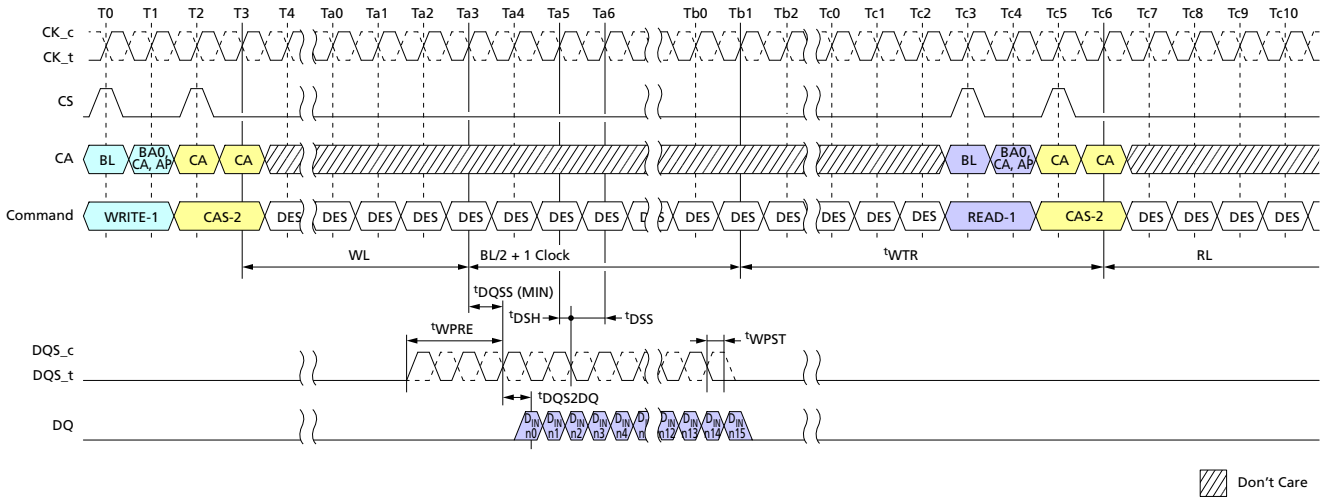
The device uses an unmatched DQS DQ path for lower power, so the DQS strobe must arrive at the SDRAM ball prior to the DQ signal by ^{t}DQS2DQ. The DQS strobe output must be driven ^{t}WPRE before the first valid rising strobe edge. The ^{t}WPRE preamble is required to be 2 × ^{t}CK at any speed ranges. The DQS strobe must be trained to arrive at the DQ pad latch center-aligned with the DQ data. The DQ data must be held for TdiVW, and the DQS must be periodically trained to stay roughly centered in the TdiVW. Burst data is captured by the SDRAM on successive edges of DQS until the 16- or 32-bit data burst is complete. The DQS strobe must remain active (toggling) for ^{t}WPST (write postamble) after the completion of the burst WRITE. After a burst WRITE operation, ^{t}WR must be satisfied before a PRECHARGE command to the same bank can be issued. Signal input timings are measured relative to the cross point of DQS_t and DQS_c.

Figure 109: Burst WRITE Operation



Notes: 1. BL = 16, Write postamble = 0.5*n*CK, DQ/DQS: V_{SSQ} termination.
2. D_{IN} *n* = data-in to column *n*.
3. ^{t}WR starts at the rising edge of CK after the last latching edge of DQS.
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 110: Burst Write Followed by Burst Read

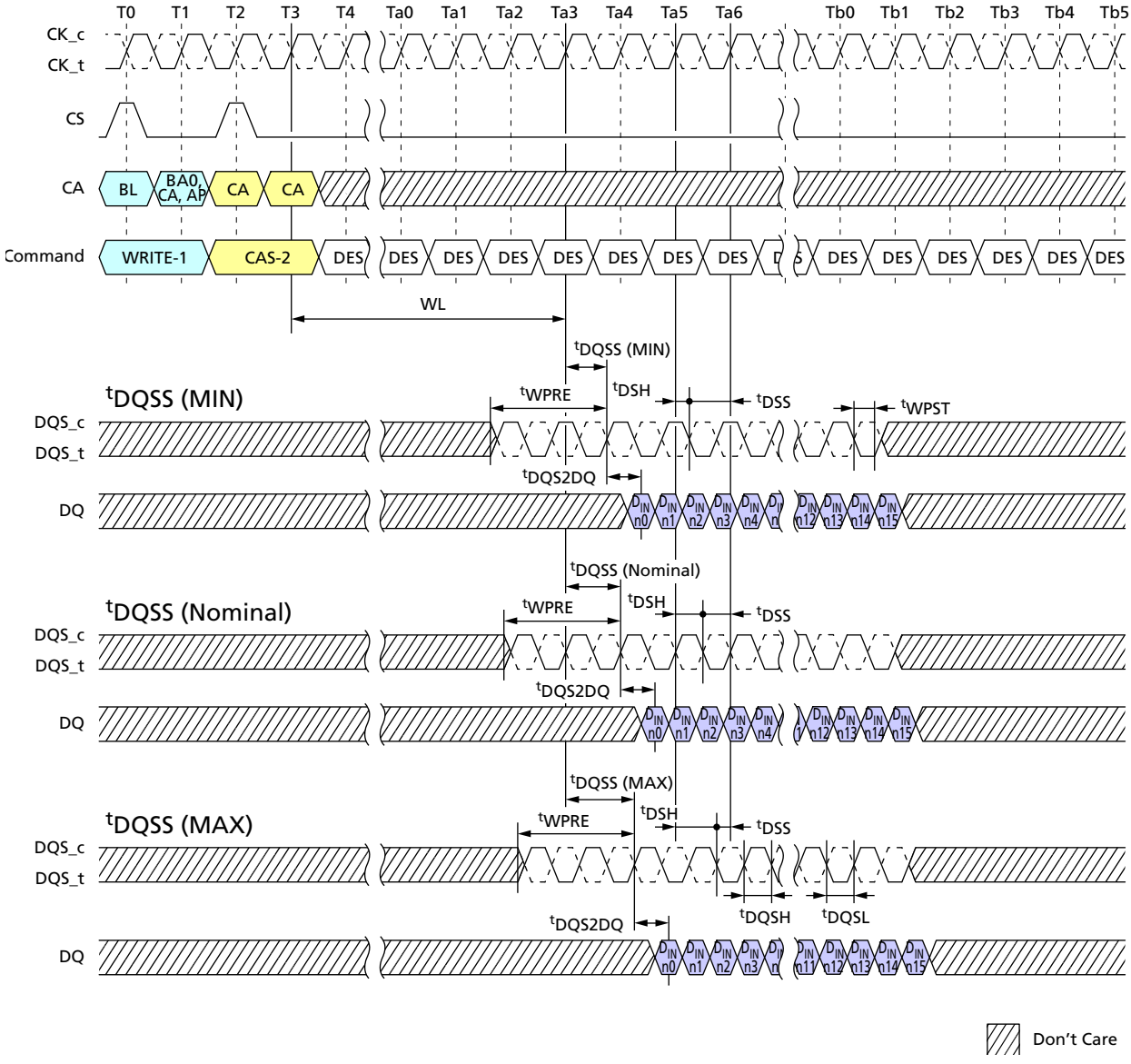


Notes: 1. BL = 16, Write postamble = 0.5*n*CK, DQ/DQS: V_{SSQ} termination.
2. D_{IN} *n* = data-in to column *n*.
3. The minimum number of clock cycles from the burst WRITE command to the burst READ command for any bank is [WL + 1 + BL/2 + RU(^{t}WTR/^{t}CK)].

4. tWTR starts at the rising edge of CK after the last latching edge of DQS.
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

Write Timing

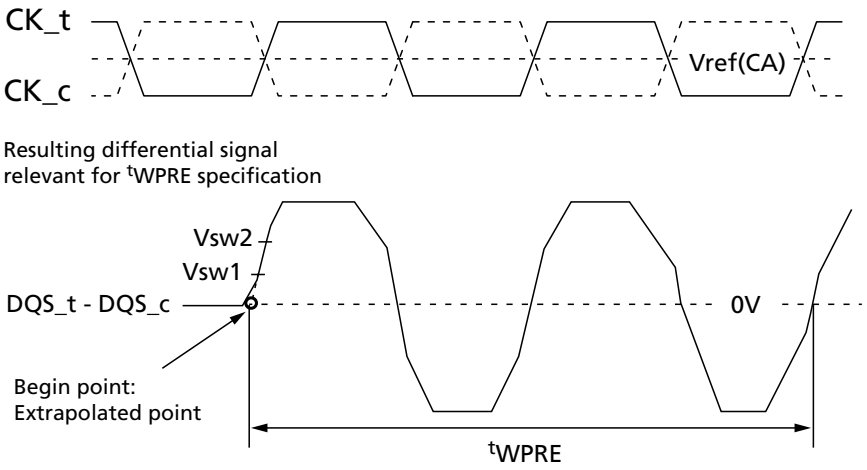
Figure 111: Write Timing



Notes: 1. BL = 16, Write postamble = 0.5*n*CK.
2. D_{IN} *n* = data-in to column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

tWPRE Calculation for ATE (Automatic Test Equipment)

Figure 112: Method for Calculating tWPRE Transitions and Endpoints



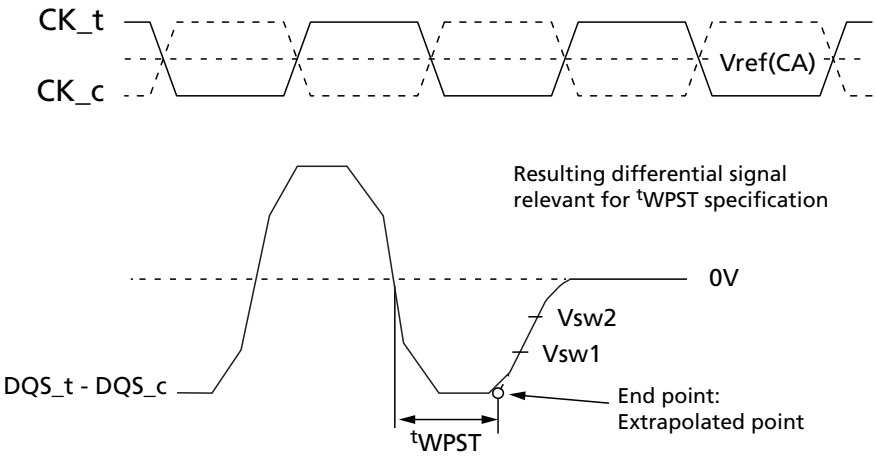
Note: 1. Termination condition for DQS_t, DQS_c, DQ, and DMI = 50 ohms to V_{SSQ}.

Table 133: Method for Calculating tWPRE Transitions and Endpoints

Measured Parameter	Measured Parameter Symbol	Vsw1	Vsw2	Unit
DQS_t, DQS_c differential write preamble	tWPRE	$V_{IHL\_AC} \times 0.3$	$V_{IHL\_AC} \times 0.7$	V

tWPST Calculation for ATE (Automatic Test Equipment)

Figure 113: Method for Calculating tWPST Transitions and Endpoints



Notes: 1. Termination condition for DQS_t, DQS_c, DQ, and DMI = 50 ohms to V_{SSQ}.
2. Write postamble: 0.5tCK
3. The method for calculating differential pulse widths for 1.5tCK postamble is same as 0.5tCK postamble.

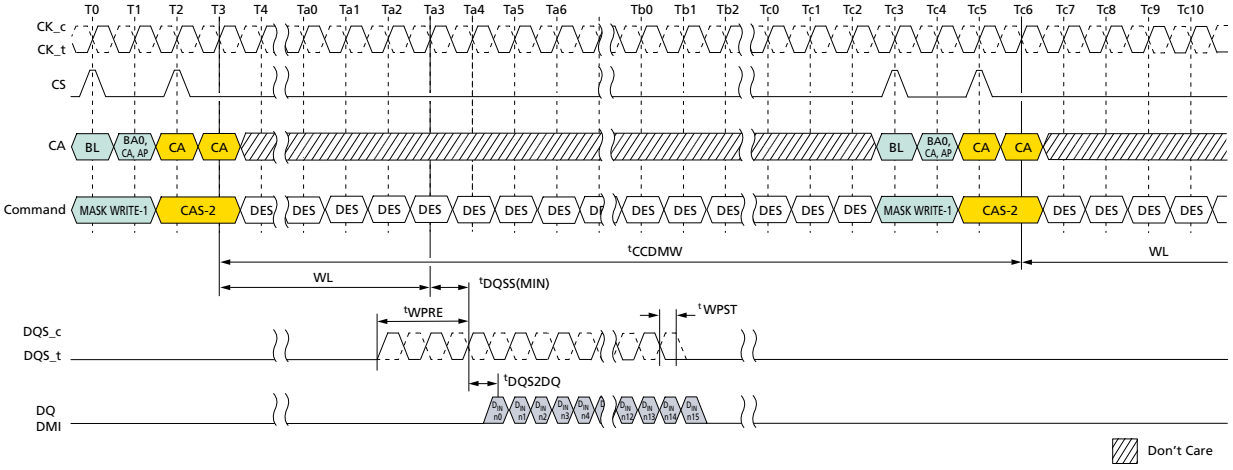
Table 134: Reference Voltage for tWPST Timing Measurements

Measured Parameter	Measured Parameter Symbol	Vsw1	Vsw2	Unit
DQS_t, DQS_c differential write postamble	tWPST	$-(V_{IHL\_AC} \times 0.7)$	$-(V_{IHL\_AC} \times 0.3)$	V

MASK WRITE Operation

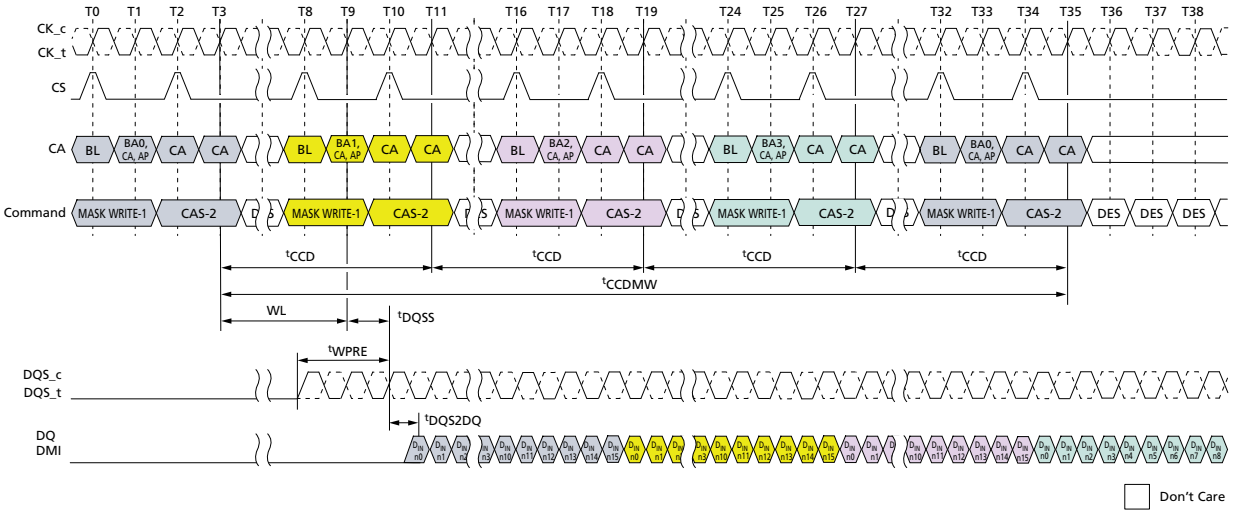
The device requires that WRITE operations that include a byte mask anywhere in the burst sequence must use the MASK WRITE command. This allows the device to implement efficient data protection schemes based on larger data blocks. The MASK WRITE-1 command is used to begin the operation, followed by a CAS-2 command. A MASKED WRITE command to the same bank cannot be issued until ^{t}CCDMW later, to allow the device to finish the internal READ-MODIFY-WRITE operation. One data-mask-invert (DMI) pin is provided per byte lane, and the data-mask-invert timings match data bit (DQ) timing. See Data Mask Invert for more information on the use of the DMI signal.

Figure 114: MASK WRITE Command – Same Bank



Notes: 1. BL = 16, Write postamble = 0.5*n*CK, DQ/DQS: V_{SSQ} termination.
2. D_{IN} *n* = data-in to column *n*.
3. Mask-write supports only BL16 operations. For BL32 configuration, the system needs to insert only 16-bit wide data for MASKED WRITE operation.
4. DES commands are shown for ease of illustration; other commands may be valid at these time.

Figure 115: MASK WRITE Command – Different Bank



Notes: 1. BL = 16, DQ/DQS/DMI: V_{SSQ} termination.
2. D_{IN} *n* = data-in to column *n*.
3. Mask-write supports only BL16 operations. For BL32 configuration, the system needs to insert only 16-bit wide data for MASKED WRITE operation.

4. DES commands are shown for ease of illustration; other commands may be valid at these time.

Mask Write Timing Constraints for BL16

Table 135: Same Bank (ODT Disabled)

Next CMD / Current CMD	ACTIVE	READ (BL = 16 or 32)	WRITE (BL = 16 or 32)	MASK WRITE	PRECHARGE
ACTIVE	Illegal	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRAS/tCK)
READ (with BL = 16)	Illegal	8[1]	RL + RU(tDQSCK(MAX)/tCK) + BL/2 - WL + tWPRE + RD(tRPST)	RL + RU(tDQSCK(MAX)/tCK) + BL/2 - WL + tWPRE + RD(tRPST)	BL/2 + MAX{(8,RU(tRTP/tCK)} - 8
READ (with BL = 32)	Illegal	16[2]	RL + RU(tDQSCK(MAX)/tCK) + BL/2 - WL + tWPRE + RD(tRPST)	RL + RU(tDQSCK(MAX)/tCK) + BL/2 - WL + tWPRE + RD(tRPST)	BL/2 + MAX{(8,RU(tRTP/tCK)} - 8
WRITE (with BL = 16)	Illegal	WL + 1+ BL/2 + RU(tWTR/tCK)	8[1]	tCCDMW[3]	WL + 1 + BL/2 + RU(tWR/tCK)
WRITE (with BL = 32)	Illegal	WL + 1 + BL/2 + RU(tWTR/tCK)	16[2]	tCCDMW + 8[4]	WL + 1 + BL/2 + RU(tWR/tCK)
MASK WRITE	Illegal	WL + 1 + BL/2 + RU(tWTR/tCK)	tCCD	tCCDMW[3]	WL + 1 + BL/2 + RU(tWR/tCK)
PRECHARGE	RU(tRP/tCK), RU(tRPab/tCK)	Illegal	Illegal	Illegal	4

Notes: 1. In the case of BL = 16, tCCD is 8 × tCK.
2. In the case of BL = 32, tCCD is 16 × tCK.
3. tCCDMW = 32 × tCK (4 × tCCD at BL = 16).
4. WRITE with BL = 32 operation is 8 × tCK longer than BL = 16.

Table 136: Different Bank (ODT Disabled)

Next CMD / Current CMD	ACTIVE	READ (BL = 16 or 32)	WRITE (BL = 16 or 32)	MASK WRITE	PRECHARGE
ACTIVE	RU(tRRD/tCK)	4	4	4	2[2]
READ (with BL = 16)	4	8[1]	RL + RU(tDQSCK(MAX)/tCK) + BL/2 - WL + tWPRE + RD(tRPST)	RL + RU(tDQSCK(MAX)/tCK) + BL/2 - WL + tWPRE + RD(tRPST)	2[2]
READ (with BL = 32)	4	16[2]	RL + RU(tDQSCK(MAX)/tCK) + BL/2 - WL + tWPRE + RD(tRPST)	RL + RU(tDQSCK(MAX)/tCK) + BL/2 - WL + tWPRE + RD(tRPST)	2[2]
WRITE (with BL = 16)	4	WL + 1+ BL/2 + RU(tWTR/tCK)	8[1]	8[1]	2[2]
WRITE (with BL = 32)	4	WL + 1 + BL/2 + RU(tWTR/tCK)	16[2]	16[2]	2[2]
MASK WRITE	4	WL + 1 + BL/2 + RU(tWTR/tCK)	8[1]	8[1]	2[2]
PRECHARGE	4	4	4	4	4

Notes: 1. In the case of BL = 16, tCCD is 8 × tCK
2. In the case of BL = 32, tCCD is 16 × tCK

Table 137: Same Bank (ODT Enabled)

Next CMD / Current CMD	ACTIVE	READ (BL = 16 or 32)	WRITE (BL = 16 or 32)	MASK WRITE	PRECHARGE
ACTIVE	Illegal	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRAS/tCK)
READ (with BL = 16)	Illegal	8[1]	RL + RU(tDQSCK(MAX)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/tCK)	RL + RU(tDQSCK(MAX)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/tCK)	BL/2 + MAX{(8,RU(tRTP/tCK)} - 8
READ (with BL = 32)	Illegal	16[2]	RL + RU(tDQSCK(MAX)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/tCK)	RL + RU(tDQSCK(MAX)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/tCK)	BL/2 + MAX{(8,RU(tRTP/tCK)} - 8
WRITE (with BL = 16)	Illegal	WL + 1+ BL/2 + RU(tWTR/tCK)	8[1]	tCCDMW[3]	WL + 1 + BL/2 + RU(tWR/tCK)
WRITE (with BL = 32)	Illegal	WL + 1 + BL/2 + RU(tWTR/tCK)	16[2]	tCCDMW + 8[4]	WL + 1 + BL/2 + RU(tWR/tCK)
MASK WRITE	Illegal	WL + 1 + BL/2 + RU(tWTR/tCK)	tCCD	tCCDMW[3]	WL + 1 + BL/2 + RU(tWR/tCK)
PRECHARGE	RU(tRP/tCK), RU(tRPab/tCK)	Illegal	Illegal	Illegal	4

Notes: 1. In the case of BL = 16, tCCD is 8 × tCK.
2. In the case of BL = 32, tCCD is 16 × tCK.
3. tCCDMW = 32 × tCK (4 × tCCD at BL = 16).
4. WRITE with BL = 32 operation is 8 × tCK longer than BL = 16.

Table 138: Different Bank (ODT Enabled)

Next CMD / Current CMD	ACTIVE	READ (BL = 16 or 32)	WRITE (BL = 16 or 32)	MASK WRITE	PRECHARGE
ACTIVE	RU(tRRD/tCK)	4	4	4	2[2]
READ (with BL = 16)	4	8[1]	RL + RU(tDQSCK(MAX)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/tCK)	RL + RU(tDQSCK(MAX)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/tCK)	2[2]
READ (with BL = 32)	4	16[2]	RL + RU(tDQSCK(MAX)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/tCK)	RL + RU(tDQSCK(MAX)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/tCK)	2[2]
WRITE (with BL = 16)	4	WL + 1+ BL/2 + RU(tWTR/tCK)	8[1]	8[1]	2[2]

Table 138: Different Bank (ODT Enabled) (Continued)

Next CMD Current CMD	ACTIVE	READ (BL = 16 or 32)	WRITE (BL = 16 or 32)	MASK WRITE	PRECHARGE
WRITE (with BL = 32)	4	WL + 1 + BL/2 + RU(^{t}WTR/^{t}CK)	16[2]	16[2]	2[2]
MASK WRITE	4	WL + 1 + BL/2 + RU(^{t}WTR/^{t}CK)	8[1]	8[1]	2[2]
PRECHARGE	4	4	4	4	4

Notes: 1. In the case of BL = 16, ^{t}CCD is 8 × ^{t}CK.
2. In the case of BL = 32, ^{t}CCD is 16 × ^{t}CK.

Data Mask and Data Bus Inversion (DBI [DC]) Function

Data mask (DM) is supported for WRITE operations and the data bus inversion DBI (DC) is supported for READ, WRITE, MASK WRITE, MRR, and MRW operations. DM and DBI (DC) functions are supported with byte granularity. DBI (DC) for READ operations (READ, MRR) can be enabled or disabled via MR3 OP[6]. DBI (DC) for WRITE operations (WRITE, MASK WRITE, MRW) can be enabled or disabled via MR3 OP[7]. DM for MASK WRITE operations can be enabled or disabled via MR13 OP[5]. The device has one data mask inversion (DMI) pin per byte and a total of two DMI pins per channel. The DMI signal is a bidirectional DDR signal, is sampled with the DQ signals, and is electrically identical to a DQ signal.

There are eight possible states for the device with the DM and DBI (DC) functions.

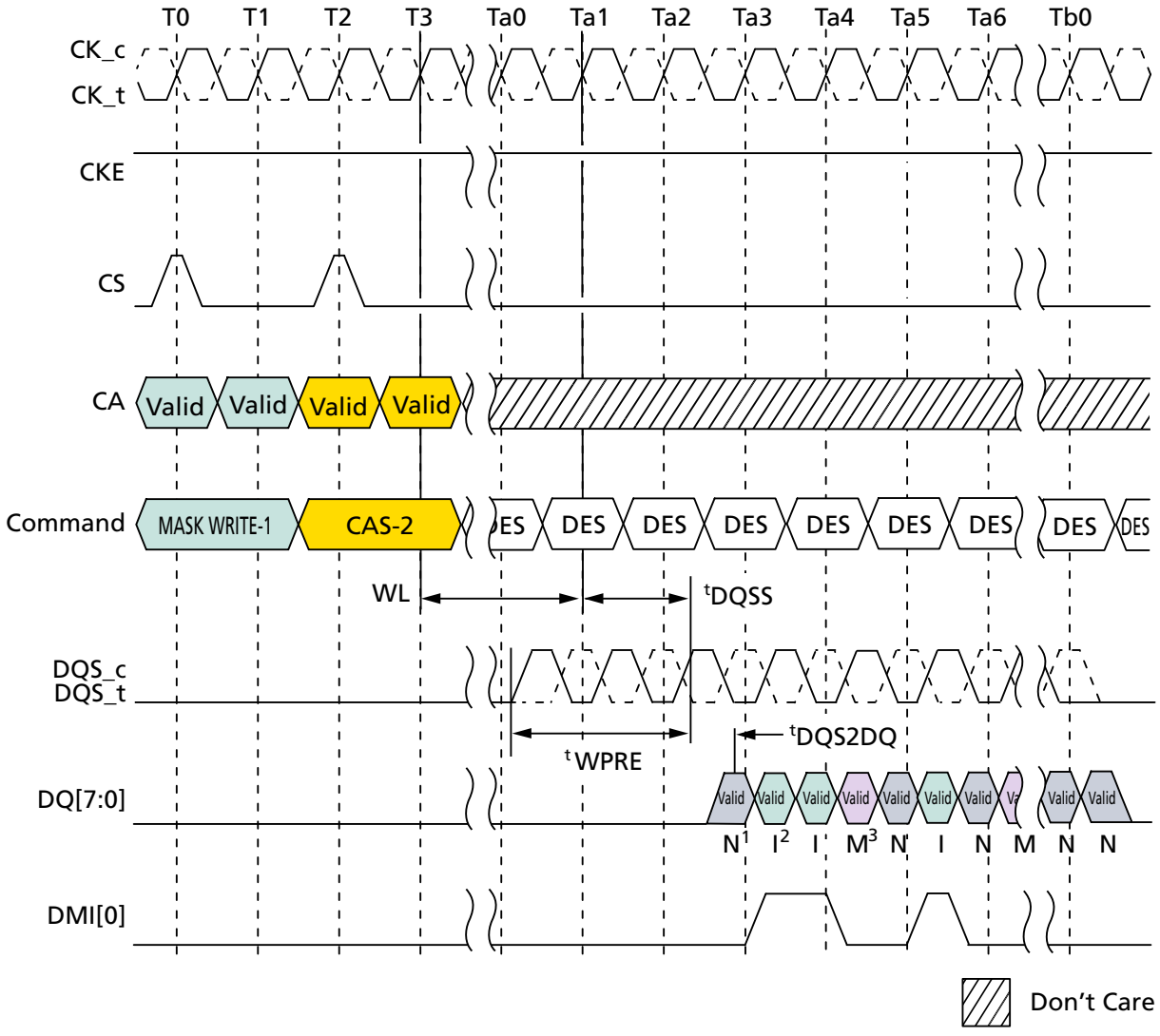
Table 139: Function Behavior of DMI Signal During WRITE, MASKED WRITE, and READ Operations

DM Function	Write DBI (DC)	Read DBI (DC)	DMI Signal					
			During WRITE	During MASKED WRITE	During READ	During MPC[WRITE-FIFO]	During MPC[READ-FIFO]	During MPC[READ DQ CAL]
Disabled	Disabled	Disabled	Don't Care[1]	Illegal[1, 3]	High-Z[2]	Don't Care[1]	High-Z[2]	High-Z[2]
Disabled	Enabled	Disabled	DBI (DC)[4]	Illegal[3]	High-Z[2]	Train[9]	Train[10]	Train[11]
Disabled	Disabled	Enabled	Don't Care[1]	Illegal[3]	DBI (DC)[5]	Train[9]	Train[10]	Train[11]
Disabled	Enabled	Enabled	DBI (DC)[4]	Illegal[3]	DBI (DC)[5]	Train[9]	Train[10]	Train[11]
Enabled	Disabled	Disabled	Don't Care[6]	DM[7]	High-Z[2]	Train[9]	Train[10]	Train[11]
Enabled	Enabled	Disabled	DBI (DC)[4]	DBI (DC)[8]	High-Z[2]	Train[9]	Train[10]	Train[11]
Enabled	Disabled	Enabled	Don't Care[6]	DM[7]	DBI (DC)[5]	Train[9]	Train[10]	Train[11]
Enabled	Enabled	Enabled	DBI (DC)[4]	DBI (DC)[8]	DBI (DC)[5]	Train[9]	Train[10]	Train[11]

Notes: 1. The DMI input signal is "Don't Care." DMI input receivers are turned off.
2. DMI output drivers are turned off.
3. The MASK WRITE command is not allowed and is considered an illegal command when the DM function is disabled.
4. The DMI signal is treated as DBI and indicates whether the device needs to invert the write data received on DQ within a byte. The device inverts write data received on the DQ inputs if DMI is sampled HIGH and leaves the write data non-inverted if DMI is sampled LOW.
5. The device inverts read data on its DQ outputs associated within a byte and drives the DMI signal HIGH when more than four data bits = 1 within a given byte lane; otherwise, the device does not invert the read data and drives DMI signal LOW.
6. The device does not perform a MASK operation when it receives a WRITE (or MRW) command. During the WRITE burst, the DMI signal must be driven LOW.

7. The device requires an explicit MASKED WRITE command for all MASKED WRITE operations. The DMI signal is treated as a data mask (DM) and indicates which bytes within a burst will be masked. When the DMI signal is sampled HIGH, the device masks that beat of the burst for the given byte lane. All DQ input signals within a byte are "Don't Care" (either HIGH or LOW) when DMI is HIGH. When the DMI signal is sampled LOW, the device does not perform a MASK operation and data received on the DQ inputs is written to the array.
8. The device requires an explicit MASKED WRITE command for all MASKED WRITE operations. The device masks the write data received on the DQ inputs if five or more data bits = 1 on DQ[2:7] or DQ[10:15] (for lower byte or upper byte respectively) and the DMI signal is LOW. Otherwise, the device does not perform the MASK operation and treats it as a legal DBI pattern. The DMI signal is treated as a DBI signal, and data received on the DQ input is written to the array.
9. The DMI signal is treated as a training pattern. The device does not perform any MASK operation and does not invert write data received on the DQ inputs.
10. The DMI signal is treated as a training pattern. The device returns the data pattern written to the WRITE-FIFO.
11. The DMI signal is treated as a training pattern. For more information, see the Read DQ Calibration Training section.

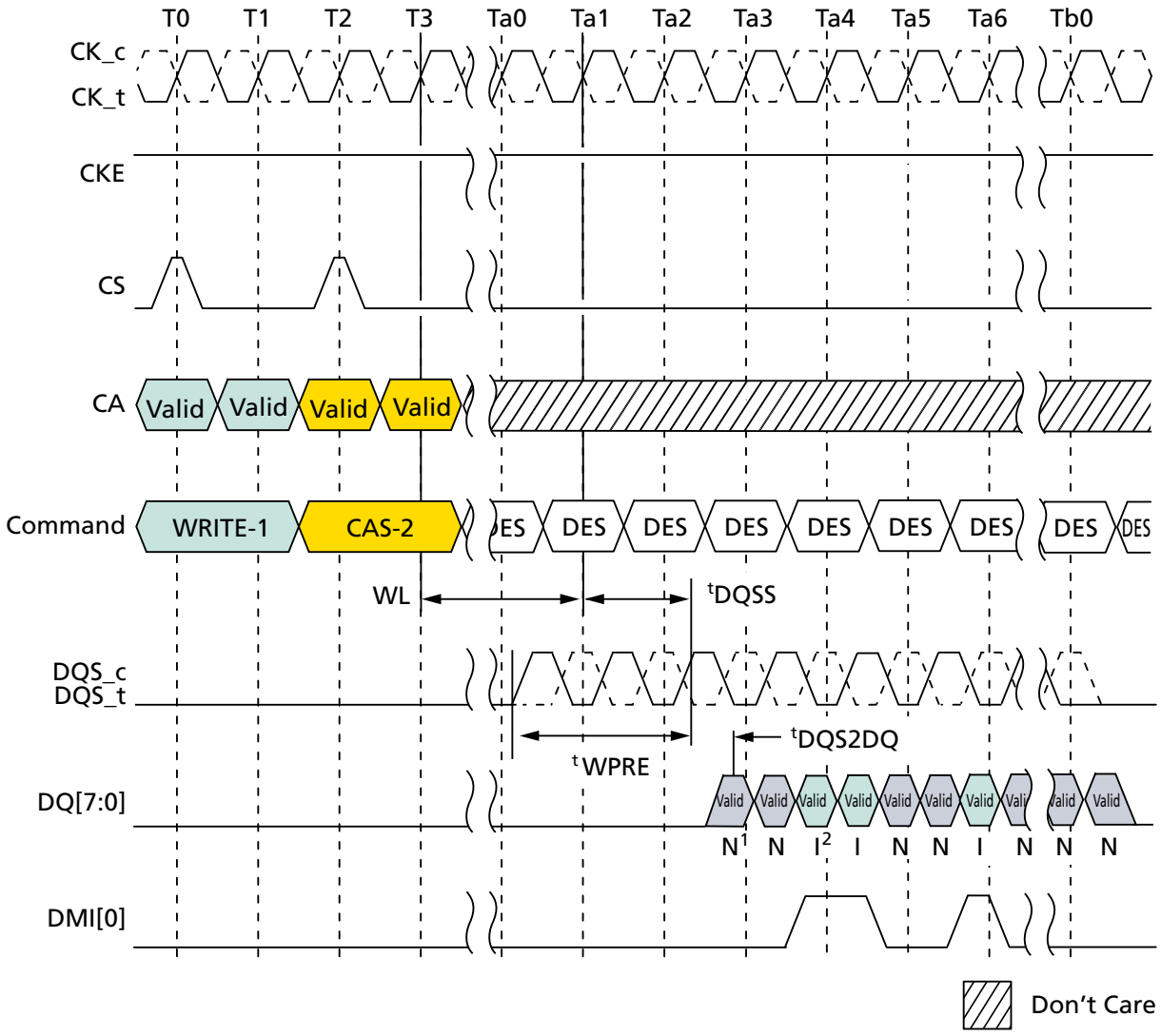
Figure 116: MASKED WRITE Command with Write DBI Enabled; DM Enabled



Notes: 1. N: Input data is written to DRAM cell.
2. I: Input data is inverted, then written to DRAM cell.
3. M: Input data is masked. The total count of 1 data bits on DQ[7:2] is equal to or greater than five.

4. Data mask (DM) is enable: MR13 OP [5] = 0, Data bus inversion (DBI) write is enable: MR3 OP[7] = 1.

Figure 117: WRITE Command with Write DBI Enabled; DM Disabled



Notes: 1. N: Input data is written to DRAM cell.

2. I: Input data is inverted, then written to DRAM cell.

3. Data mask (DM) is disable: MR13 OP [5] = 1, Data bus inversion (DBI) write is enable: MR3 OP[7] = 1.

WRITE and MASKED WRITE Operation DQS Control (WDQS Control)

The device supports WRITE, MASKED WRITE, and WR-FIFO operations with the following DQS controls. Before and after WRITE, MASKED WRITE, and WR-FIFO operations, DQS_t, and DQS_c are required to have sufficient voltage gap to make sure the write buffers operate normally without any risk of meta-stability.

The device is supported by either of the two WDQS control modes below.

- Mode 1: Read-based control
- Mode 2: WDQS_on/WDQS_off definition based control

Regardless of ODT enable/disable, WDQS-related timing described here does not allow any change of existing command timing constraints for all READ/WRITE operations. In case of any conflict or ambiguity on the command timing constraints caused by the specification here, the specification defined in the Timing Constraints for Training Commands table should have higher priority than WDQS control requirements.

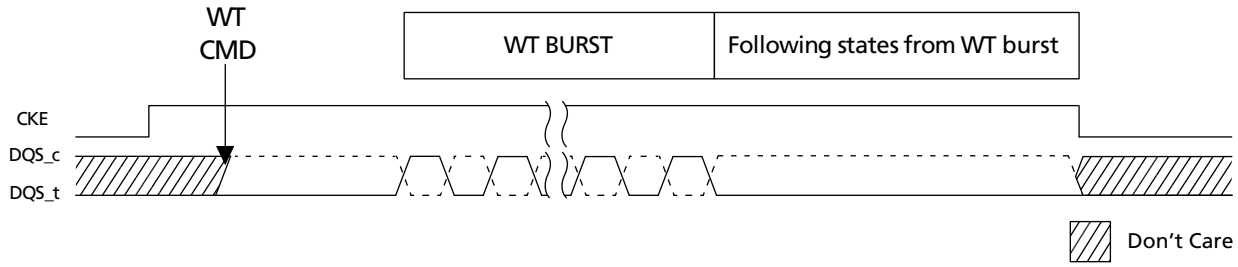
To prevent write preamble related failure, either of the two WDQS controls to the device should be supported.

WDQS Control Mode 1 – Read-Based Control

The device needs to be guaranteed the differential WDQS, but the differential WDQS can be controlled as described below. WDQS control requirements here can be ignored while differential read DQS is operated or while DQS hands over from read to write or vice versa.

1. When WRITE/MASKED WRITE command is issued, SoC makes the transition from driving DQS_c HIGH to driving differential DQS_t/DQS_c, followed by normal differential burst on DQS pins.
2. At the end of post amble of WRITE/MASKED WRITE burst, SoC resumes driving DQS_c HIGH through the subsequent states except for DQS toggling and DQS turn around time of WT-RD and RD-WT as long as CKE is HIGH.
3. When CKE is LOW, the state of DQS_t/DQS_c is allowed to be “Don’t Care.”

Figure 118: WDQS Control Mode 1



WDQS Control Mode 2 – WDQS_On/Off

After WRITE/MASKED WRITE command is issued, DQS_t and DQS_c required to be differential from WDQS_on, and DQS_t and DQS_c can be “Don’t Care” status from WDQS_off of WRITE/MASKED WRITE command. When ODT is enabled, WDQS_on and WDQS_off timing is located in the middle of the operations. When host disables ODT, WDQS_on and WDQS_off constraints conflict with ^{t}RTW. The timing does not conflict when ODT is enabled because WDQS_on and WDQS_off timing is covered in ODTLon and ODTLoff. However, regardless of ODT on/off, WDQS_on/off timing below does not change any command timing constraints for all read and write operations. To prevent the conflict, WDQS_on/off requirement can be ignored where WDQS_on/off timing is overlapped with read operation period including READ burst period and ^{t}RPST or overlapped with turn-around time (RD-WT or WT-RD). In addition, the period during DQS toggling caused by read and write can be counted as WDQS_on/off.

Parameters

- WDQS_on: The maximum delay from WRITE/MASKED WRITE command to differential DQS_t and DQS_c
- WDQS_off: The minimum delay for DQS_t and DQS_c differential input after the last WRITE/MASKED WRITE command
- WDQS_Exception: The period where WDQS_on and WDQS_off timing is overlapped with READ operation or with DQS turn around (RD-WT, WT-RD)
  - WDQS_Exception @ ODT disable = MAX(WL-WDQS_on + ^{t}DQSTA - ^{t}WPRE - *n* ^{t}CK, 0 ^{t}CK) where RD to WT command gap = ^{t}RTW(MIN)@ODT disable + *n* ^{t}CK
  - WDQS_Exception @ ODT enable = ^{t}DQSTA

Table 140: WDQS_On/WDQS_Off Definition

WRITE Latency				WDQS_On (Max)		WDQS_Off (Min)		Lower Frequency Limit (>)	Upper Frequency Limit (≤)
Set A	Set B	*n*WR	*n*RTP	Set A	Set B	Set A	Set B		
4	4	6	8	0	0	15	15	10	266
6	8	10	8	0	0	18	20	266	533
8	12	16	8	0	6	21	25	533	800
10	18	20	8	4	12	24	32	800	1066
12	22	24	10	4	14	27	37	1066	1333
14	26	30	12	6	18	30	42	1333	1600
16	30	34	14	6	20	33	47	1600	1866
18	34	40	16	8	24	36	52	1866	2133

Notes: 1. WDQS_on/off requirement can be ignored when WDQS_on/off timing is overlapped with READ operation period including READ burst period and ^{t}RPST or overlapped with turn-around time (RD-WT or WT-RD).
2. DQS toggling period caused by read and write can be counted as WDQS_on/off.

Table 141: WDQS_On/WDQS_Off Allowable Variation Range

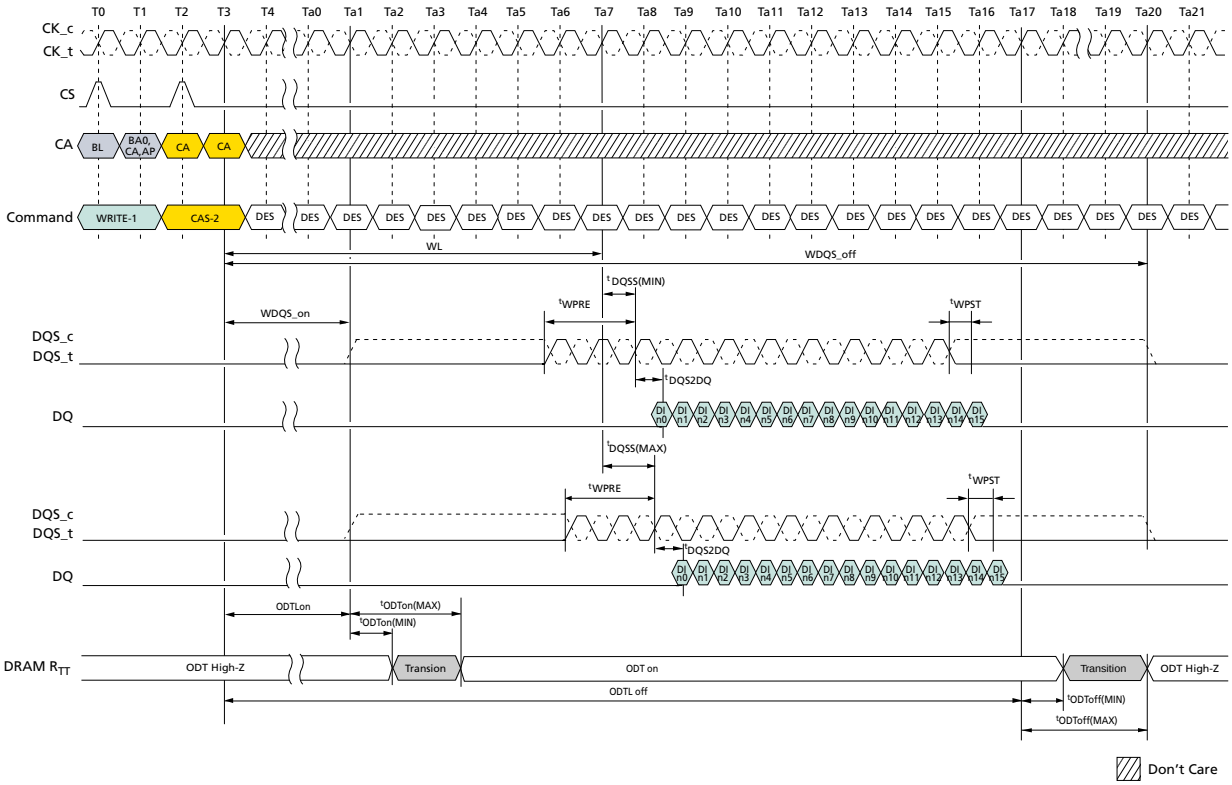
	Min	Max	Unit
WDQS_on	–0.25	0.25	^{t}CK(avg)
WDQS_off	–0.25	0.25	^{t}CK(avg)

Table 142: DQS Turn-Around Parameter

Parameter	Description	Value	Unit	Note
^{t}DQSTA	Turn-around time RDQS to WDQS for WDQS control case	TBD	–	1

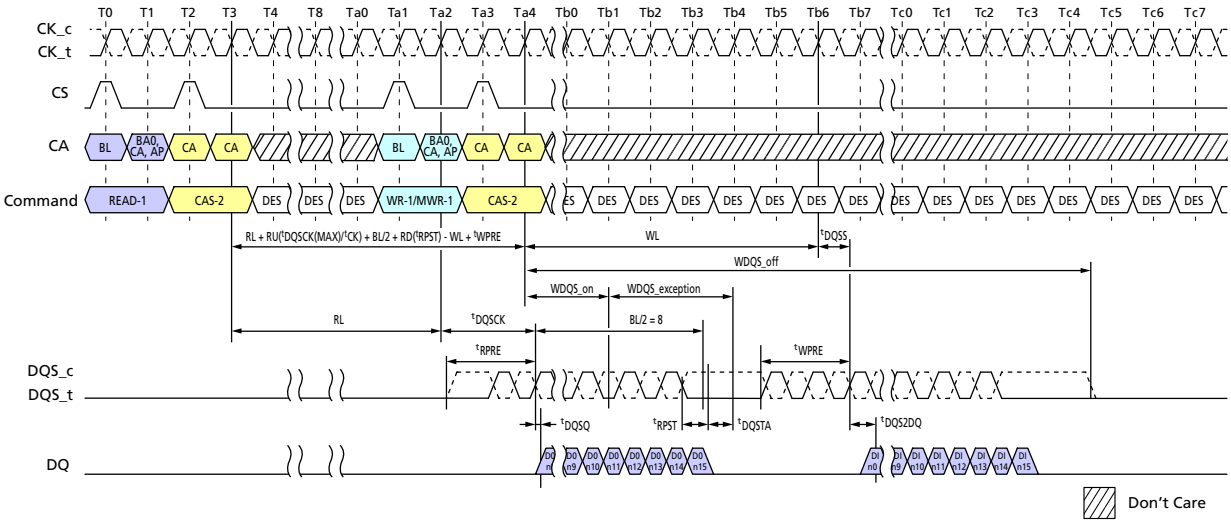
Note: 1. ^{t}DQSTA is only applied to WDQS_exception case when WDQS Control. Except for WDQS Control, ^{t}DQSTA can be ignored.

Figure 119: Burst WRITE Operation



Notes: 1. BL=16, Write postamble = 0.5*n*CK, DQ/DQS: V_{SSQ} termination.
2. DI *n* = data-in to column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. DRAM R_{TT} is only applied when ODT is enabled (MR11 OP[2:0] is not 000b).

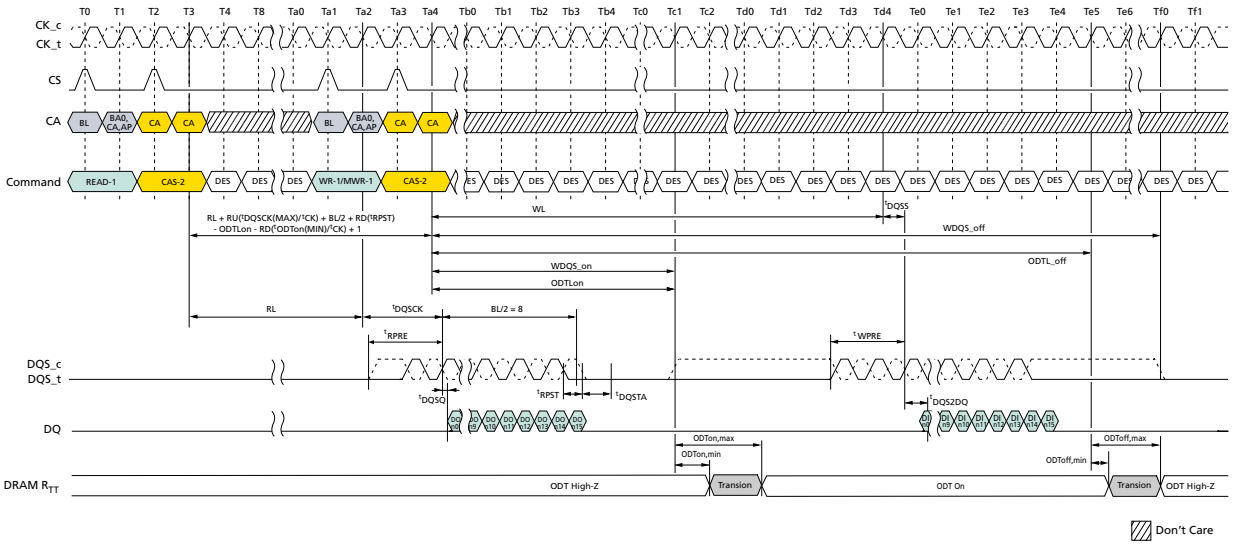
Figure 120: Burst READ Followed by Burst WRITE or Burst MASKED WRITE (ODT Disable)



Notes: 1. BL = 16, Read preamble = Toggle, Read postamble = 0.5*n*CK, Write preamble = 2*n*CK, Write postamble = 0.5*n*CK.
2. DO *n* = data-out from column *n*, DI *n* = data-in to column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

4. WDQS_on and WDQS_off requirement can be ignored where WDQS_on/off timing is overlapped with READ operation period including READ burst period and ^{t}RPST or overlapped with turn-around time (RD-WT or WT-RD).

Figure 121: Burst READ Followed by Burst WRITE or Burst MASKED WRITE (ODT Enable)



Notes: 1. BL = 16, Read preamble = Toggle, Read postamble = 0.5*n*CK, Write preamble = 2*n*CK, Write postamble = 0.5*n*CK, DQ/DQS: V_{SSQ} termination.
2. DO *n* = data-out from column *n*, DI *n* = data-in to column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. WDQS_on and WDQS_off requirement can be ignored where WDQS_on/off timing is overlapped with READ operation period including READ burst period and ^{t}RPST or overlapped with turn-around time (RD-WT or WT-RD).

Preamble and Postamble Behavior

Preamble, Postamble Behavior in READ-to-READ Operations

The following illustrations show the behavior of the device's read DQS_t and DQS_c pins during cases where the preamble, postamble, and/or data clocking overlap.

DQS will be driven with the following priority

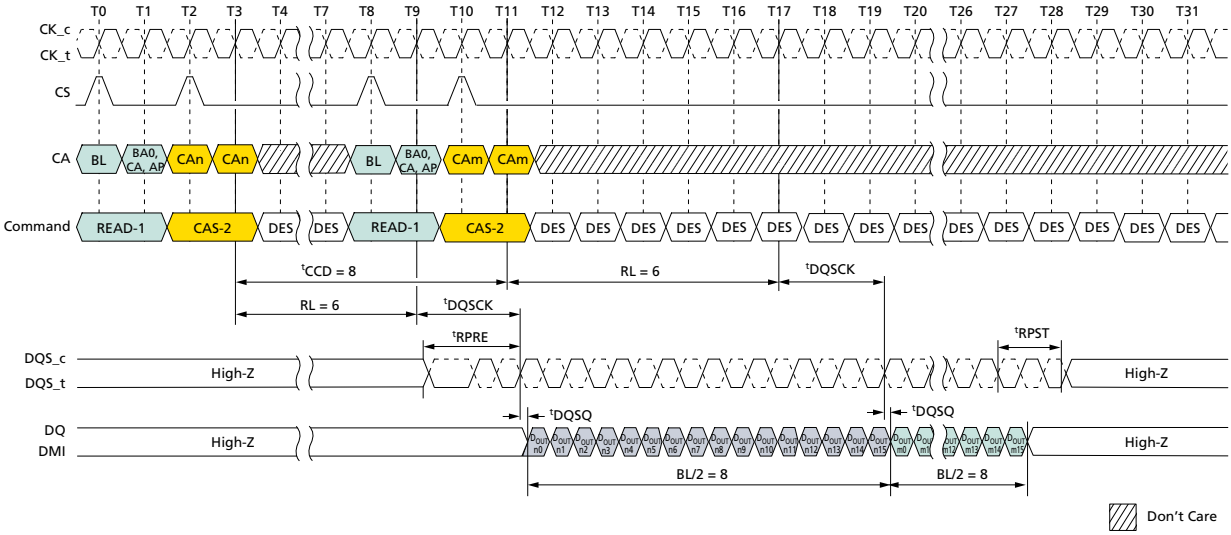
1. Data clocking edges will always be driven
2. Postamble
3. Preamble

Essentially the data clocking, preamble, and postamble will be ordered such that all edges will be driven.

Additional examples of seamless and borderline non-overlapping cases have been included for clarity.

READ-to-READ Operations – Seamless

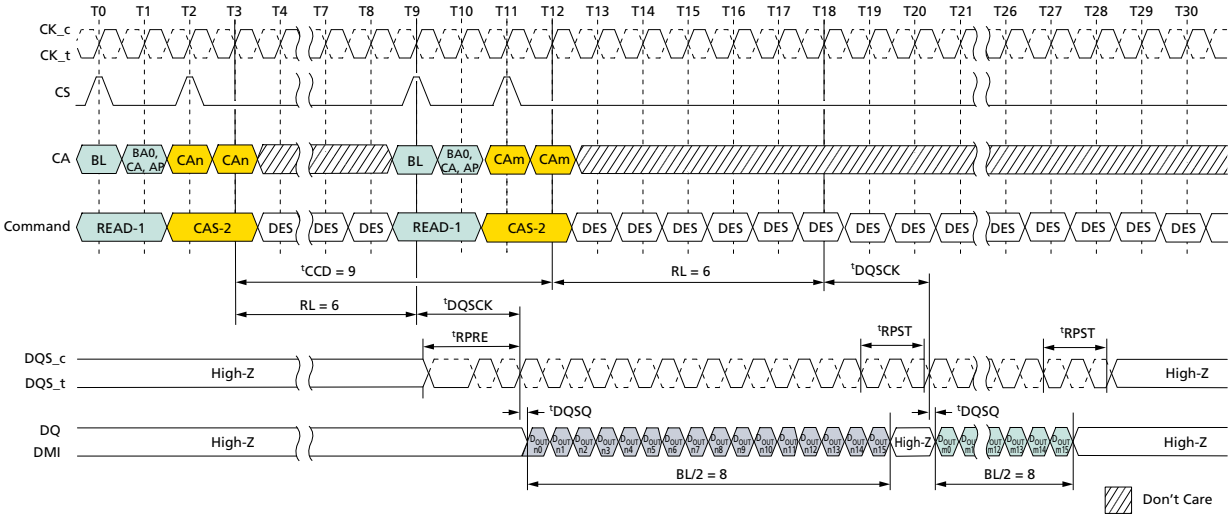
Figure 122: READ Operations: tCCD = MIN, Preamble = Toggle, 1.5nCK Postamble



Notes: 1. BL = 16 for column *n* and column *m*; RL = 6; Preamble = Toggle; Postamble = 1.5*n*CK.
2. D_{OUT} *n*/*m* = data-out from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

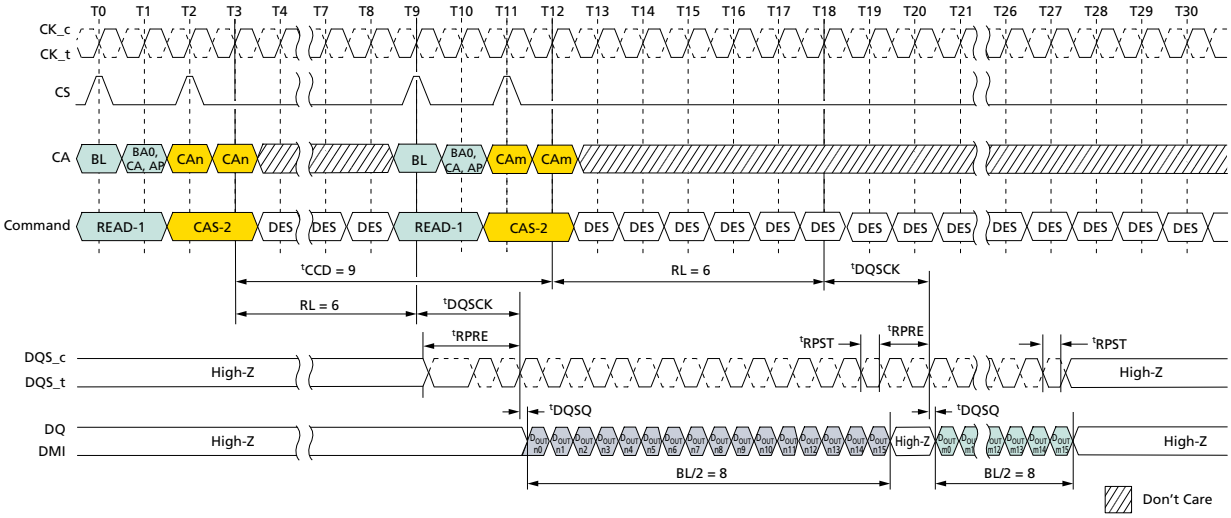
READ-to-READ Operations – Consecutive

Figure 123: Seamless READ: tCCD = MIN + 1, Preamble = Toggle, 1.5nCK Postamble



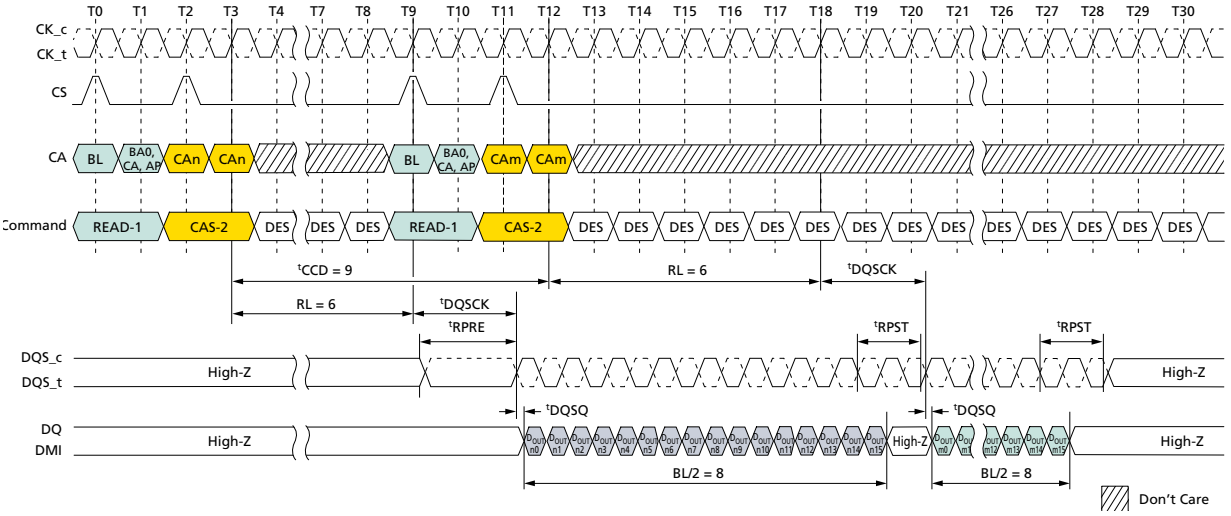
Notes: 1. BL = 16 for column *n* and column *m*; RL = 6; Preamble = Toggle; Postamble = 1.5*n*CK.
2. D_{OUT} *n*/*m* = data-out from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 124: Consecutive READ: ^{t}CCD = MIN + 1, Preamble = Toggle, 0.5*n*CK Postamble



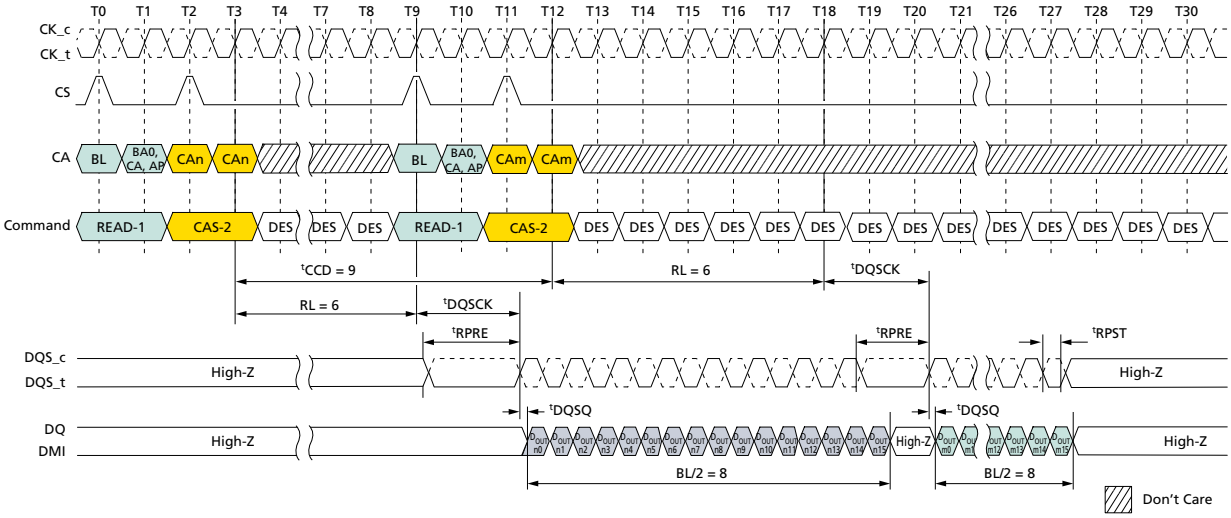
Notes: 1. BL = 16 for column *n* and column *m*; RL = 6; Preamble = Toggle; Postamble = 0.5*n*CK.
2. D_{OUT} *n*/*m* = data-out from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 125: Consecutive READ: ^{t}CCD = MIN + 1, Preamble = Static, 1.5*n*CK Postamble



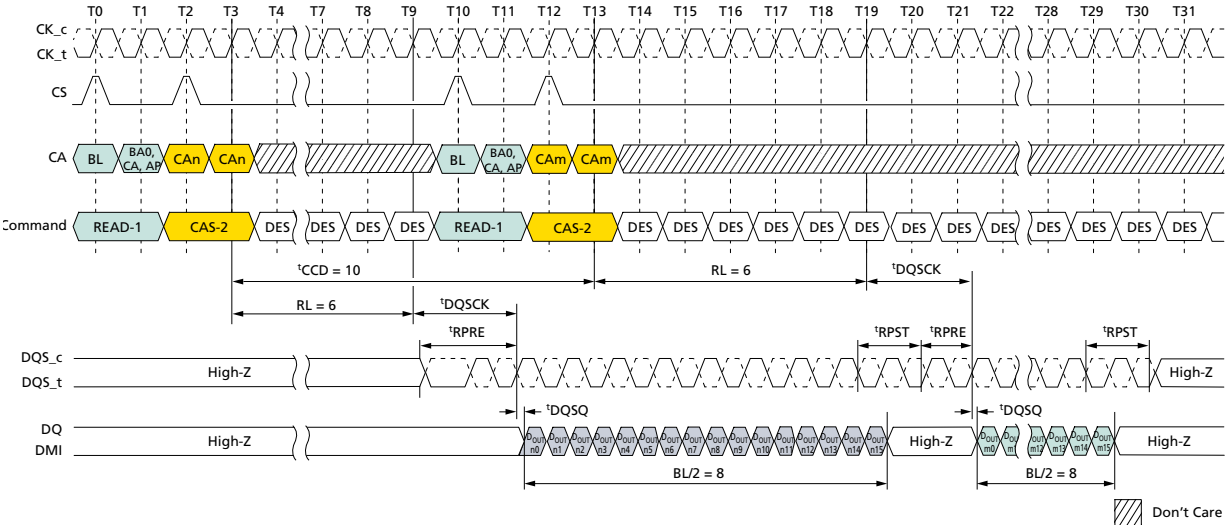
Notes: 1. BL = 16 for column *n* and column *m*; RL = 6; Preamble = Static; Postamble = 1.5*n*CK.
2. D_{OUT} *n*/*m* = data-out from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 126: Consecutive READ: ^{t}CCD = MIN + 1, Preamble = Static, 0.5*n*CK Postamble



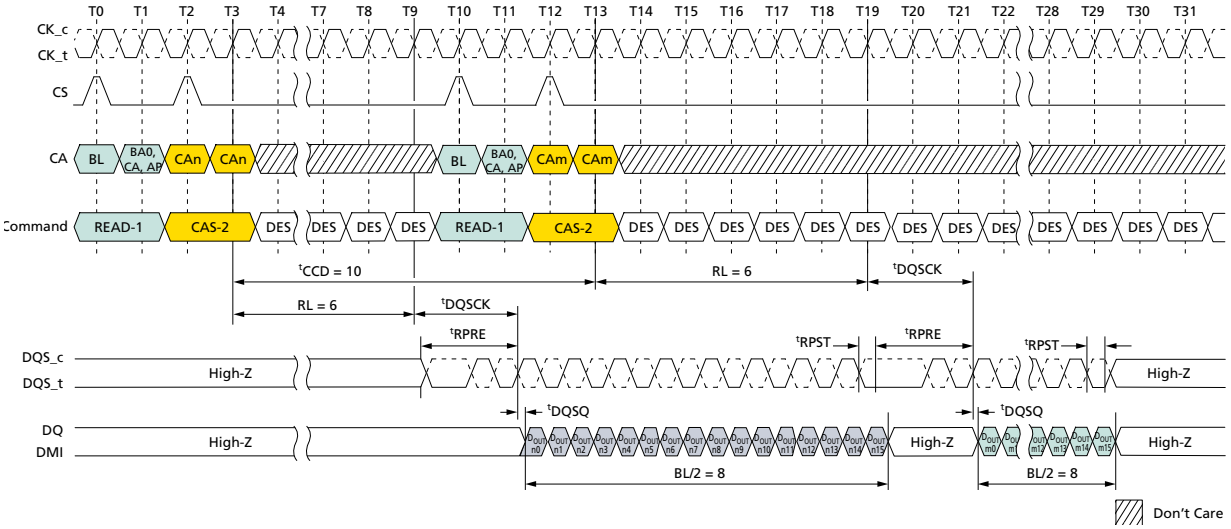
Notes: 1. BL = 16 for column *n* and column *m*; RL = 6; Preamble = Static; Postamble = 0.5*n*CK.
2. D_{OUT} *n*/*m* = data-out from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 127: Consecutive READ: ^{t}CCD = MIN + 2, Preamble = Toggle, 1.5*n*CK Postamble



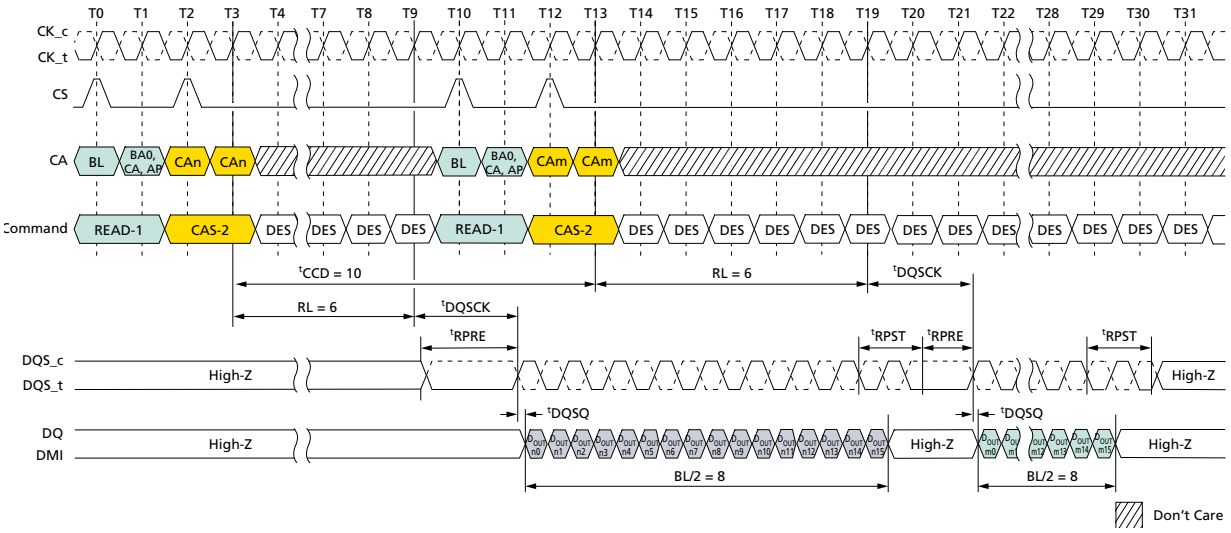
Notes: 1. BL = 16 for column *n* and column *m*; RL = 6; Preamble = Toggle; Postamble = 1.5*n*CK.
2. D_{OUT} *n*/*m* = data-out from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 128: Consecutive READ: ^{t}CCD = MIN + 2, Preamble = Toggle, 0.5*n*CK Postamble



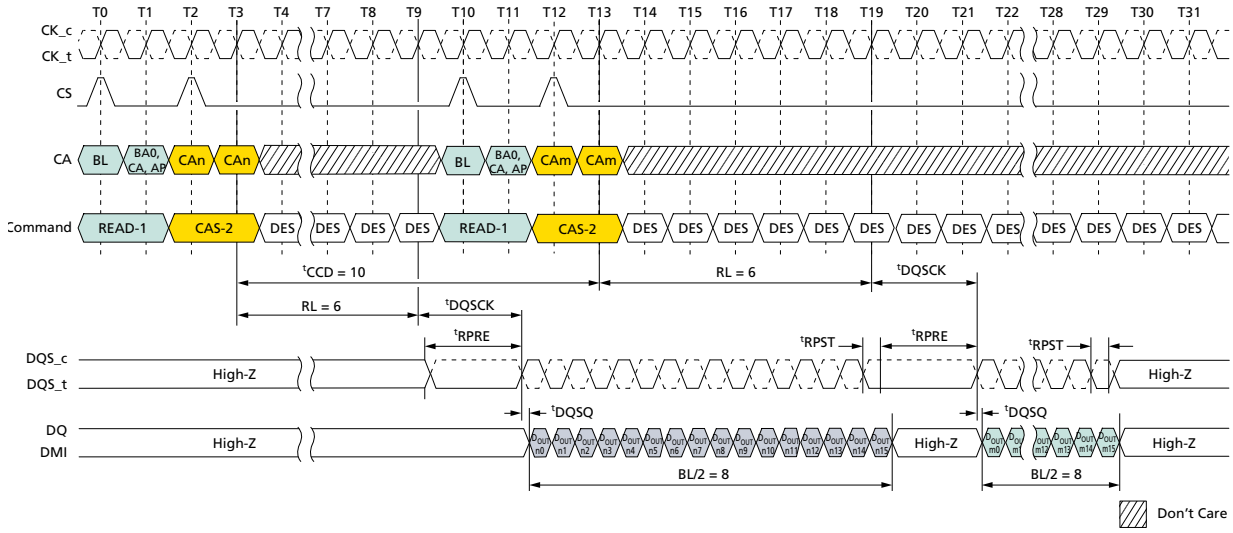
Notes: 1. BL = 16 for column *n* and column *m*; RL = 6; Preamble = Toggle; Postamble = 0.5*n*CK.
2. D_{OUT} *n*/*m* = data-out from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 129: Consecutive READ: ^{t}CCD = MIN + 2, Preamble = Static, 1.5*n*CK Postamble



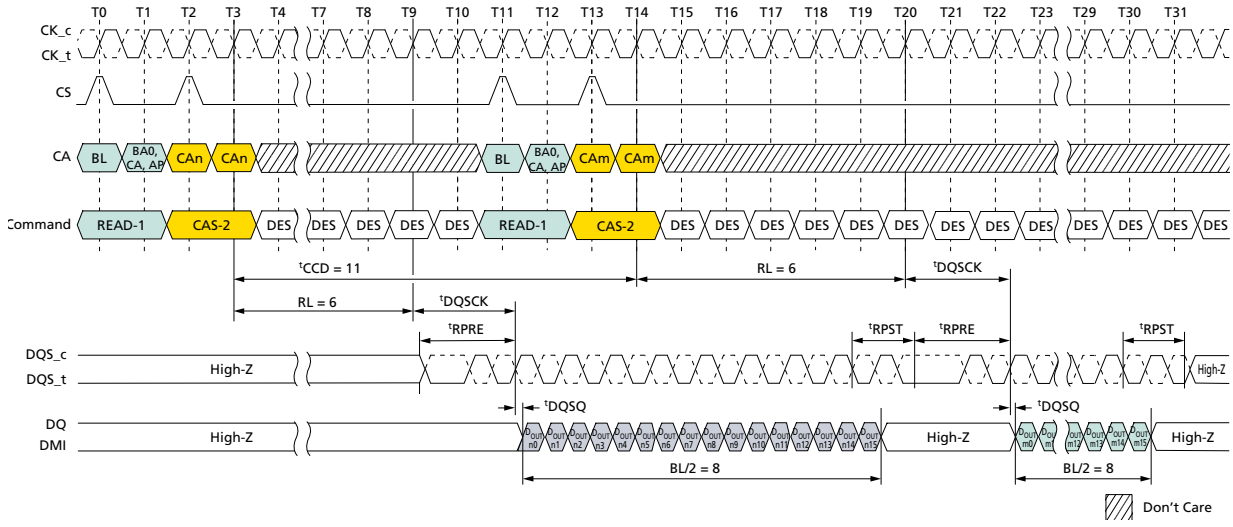
Notes: 1. BL = 16 for column *n* and column *m*; RL = 6; Preamble = Static; Postamble = 1.5*n*CK.
2. D_{OUT} *n*/*m* = data-out from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 130: Consecutive READ: ^{t}CCD = MIN + 2, Preamble = Static, 0.5*n*CK Postamble



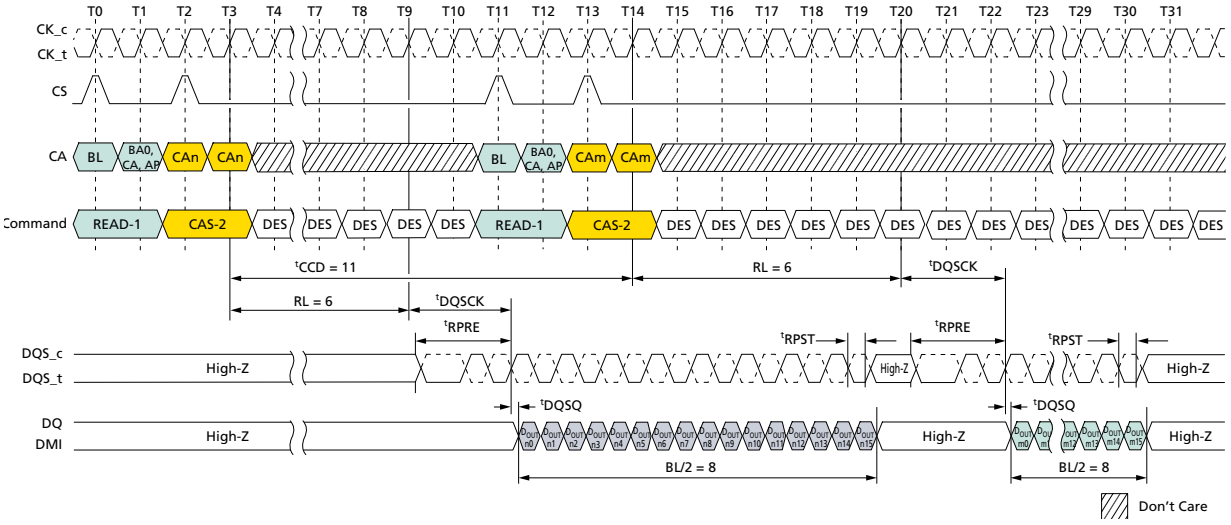
Notes: 1. BL = 16 for column *n* and column *m*; RL = 6; Preamble = Static; Postamble = 0.5*n*CK.
2. D_{OUT} *n*/*m* = data-out from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 131: Consecutive READ: ^{t}CCD = MIN + 3, Preamble = Toggle, 1.5*n*CK Postamble



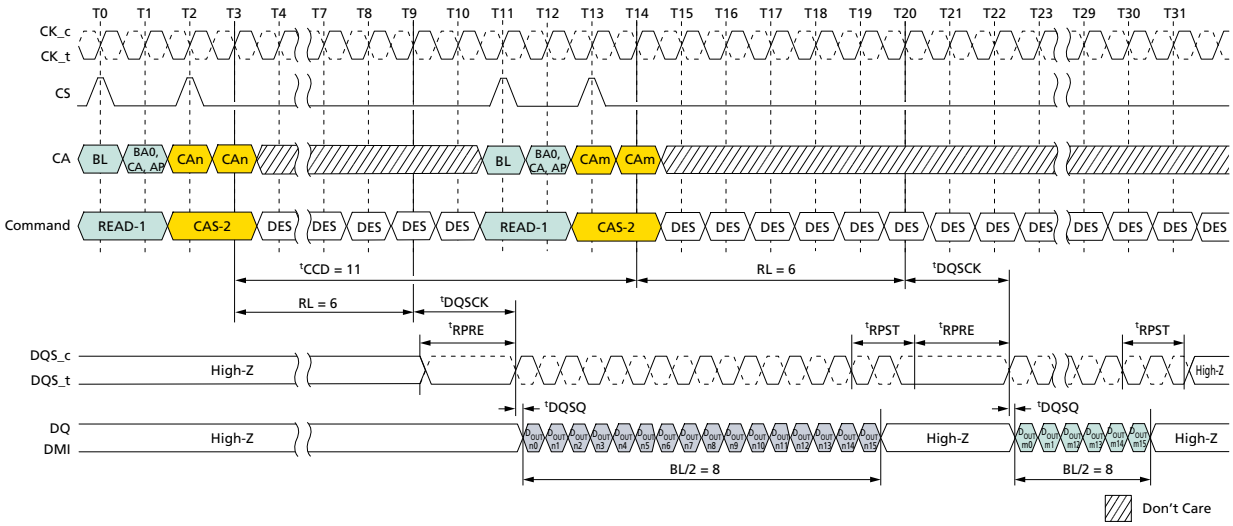
Notes: 1. BL = 16 for column *n* and column *m*; RL = 6; Preamble = Toggle; Postamble = 1.5*n*CK.
2. D_{OUT} *n*/*m* = data-out from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 132: Consecutive READ: ^{t}CCD = MIN + 3, Preamble = Toggle, 0.5*n*CK Postamble



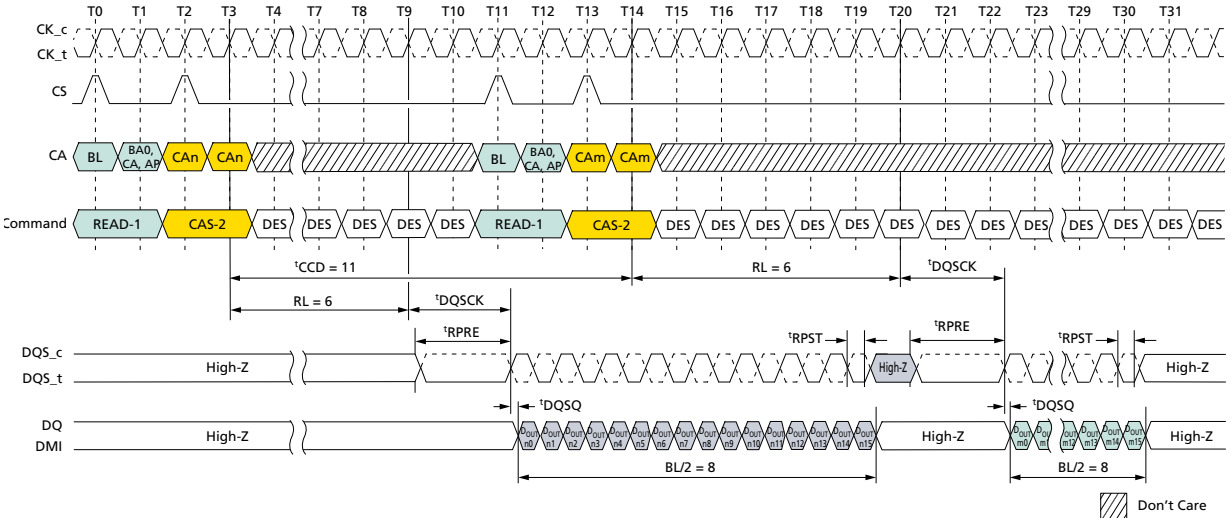
Notes: 1. BL = 16 for column *n* and column *m*; RL = 6; Preamble = Toggle; Postamble = 0.5*n*CK.
2. D_{OUT} *n*/*m* = data-out from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 133: Consecutive READ: ^{t}CCD = MIN + 3, Preamble = Static, 1.5*n*CK Postamble



Notes: 1. BL = 16 for column *n* and column *m*; RL = 6; Preamble = Static; Postamble = 1.5*n*CK.
2. D_{OUT} *n*/*m* = data-out from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

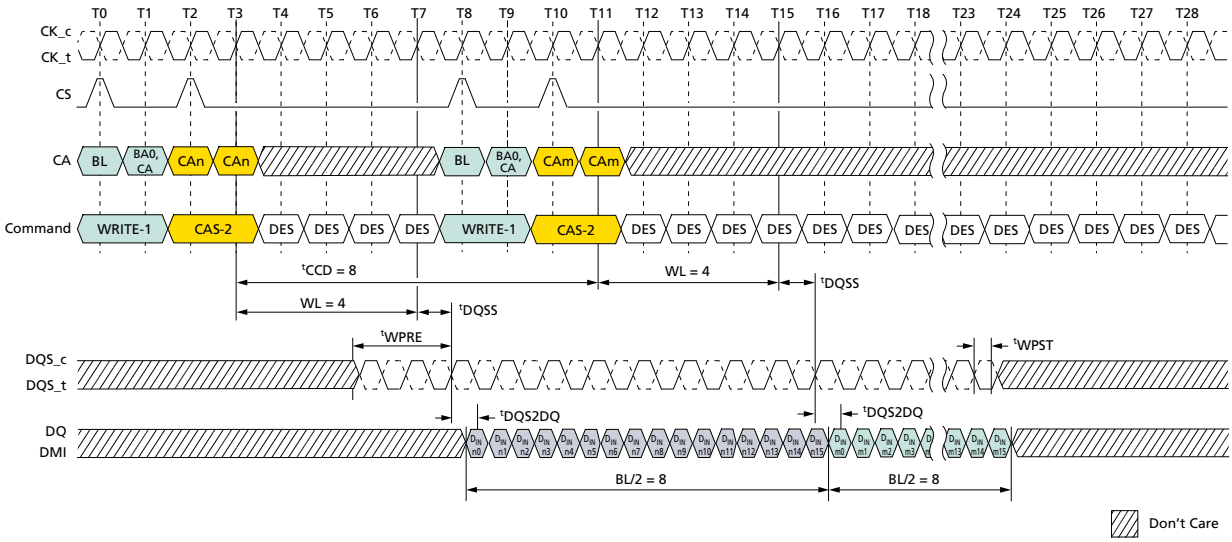
Figure 134: Consecutive READ: ^{t}CCD = MIN + 3, Preamble = Static, 0.5*n*CK Postamble



Notes: 1. BL = 16 for column *n* and column *m*; RL = 6, Preamble = Static; Postamble = 0.5*n*CK
2. D_{OUT} *n*/*m* = data-out from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

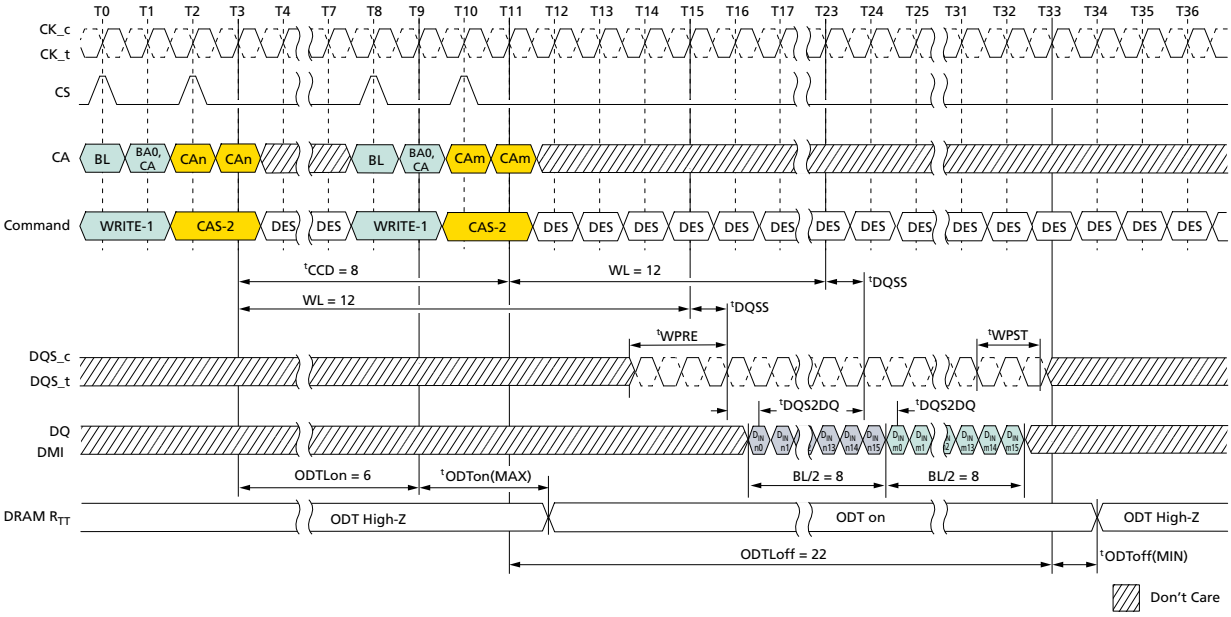
WRITE-to-WRITE Operations – Seamless

Figure 135: Seamless WRITE: ^{t}CCD = MIN, 0.5*n*CK Postamble



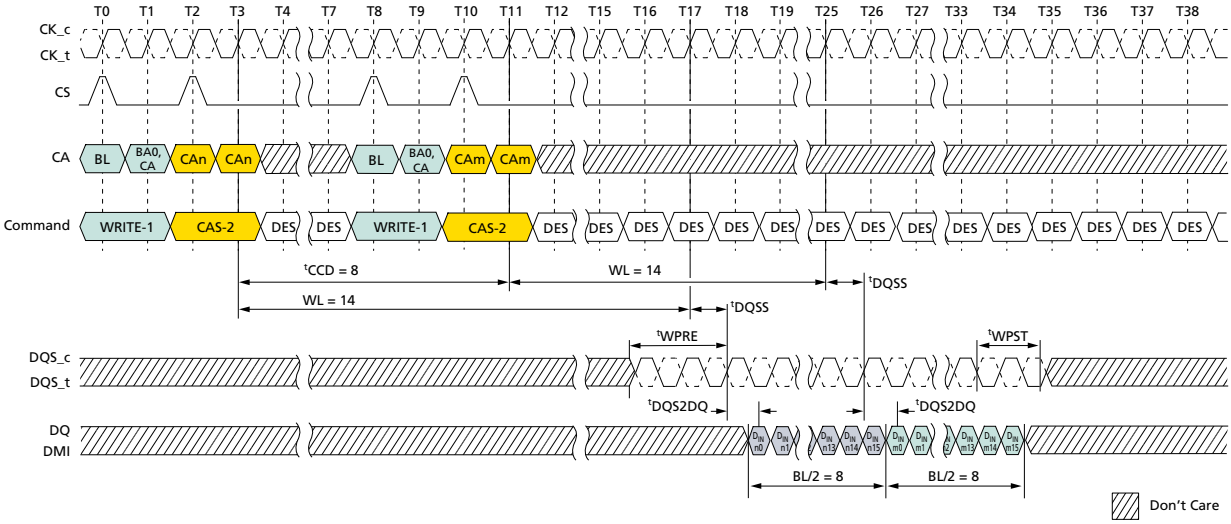
Notes: 1. BL = 16, Write postamble = 0.5*n*CK.
2. D_{IN} *n*/*m* = data-in from column *n* and column *m*.
3. The minimum number of clock cycles from the burst WRITE command to the burst WRITE command for any bank is BL/2.
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 136: Seamless WRITE: ^{t}CCD = MIN, 1.5*n*CK Postamble, 533 MHz < Clock Frequency <= 800 MHz, ODT Worst Timing Case



Notes: 1. Clock frequency = 800 MHz, ^{t}CK(AVG) = 1.25ns.
2. BL = 16, Write postamble = 1.5*n*CK.
3. D_{IN} *n*/*m* = data-in from column *n* and column *m*.
4. The minimum number of clock cycles from the burst WRITE command to the burst WRITE command for any bank is BL/2.
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

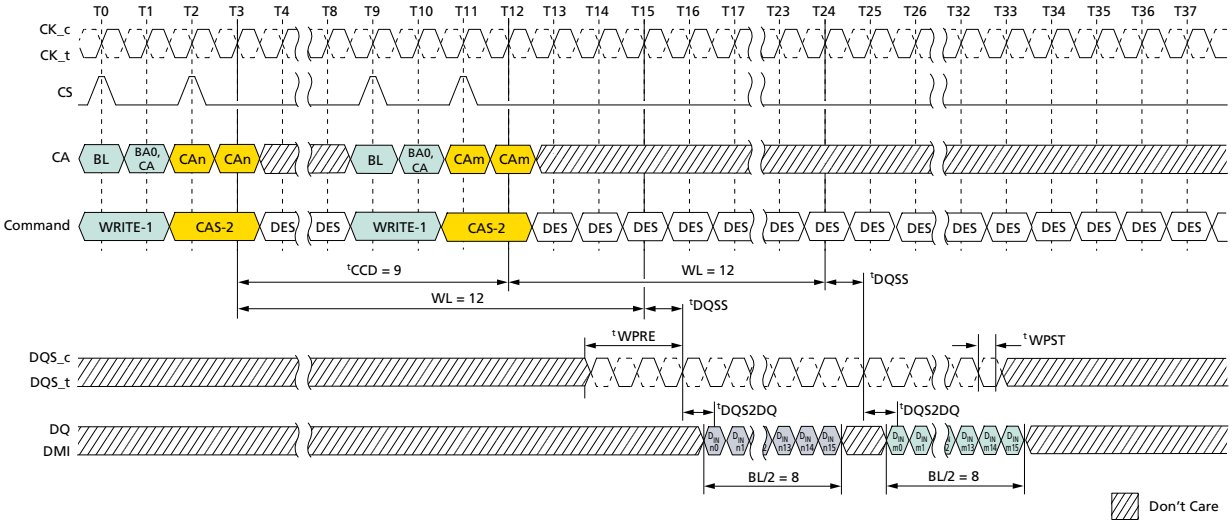
Figure 137: Seamless WRITE: ^{t}CCD = MIN, 1.5*n*CK Postamble



Notes: 1. BL = 16, Write postamble = 1.5*n*CK.
2. D_{IN} *n*/*m* = data-in from column *n* and column *m*.
3. The minimum number of clock cycles from the burst WRITE command to the burst WRITE command for any bank is BL/2.
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

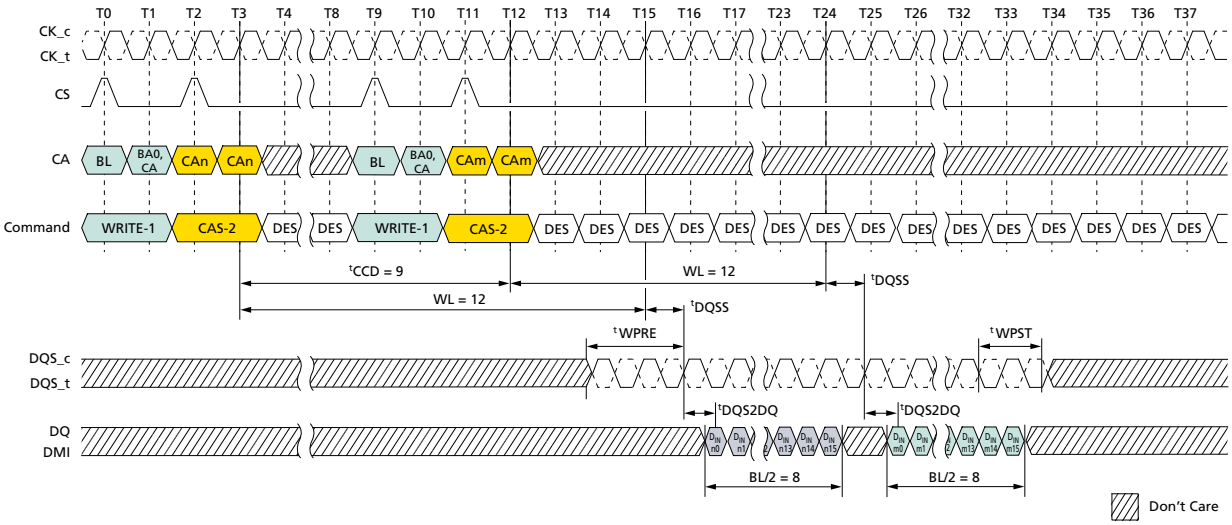
WRITE-to-WRITE Operations – Consecutive

Figure 138: Consecutive WRITE: ^{t}CCD = MIN + 1, 0.5*n*CK Postamble



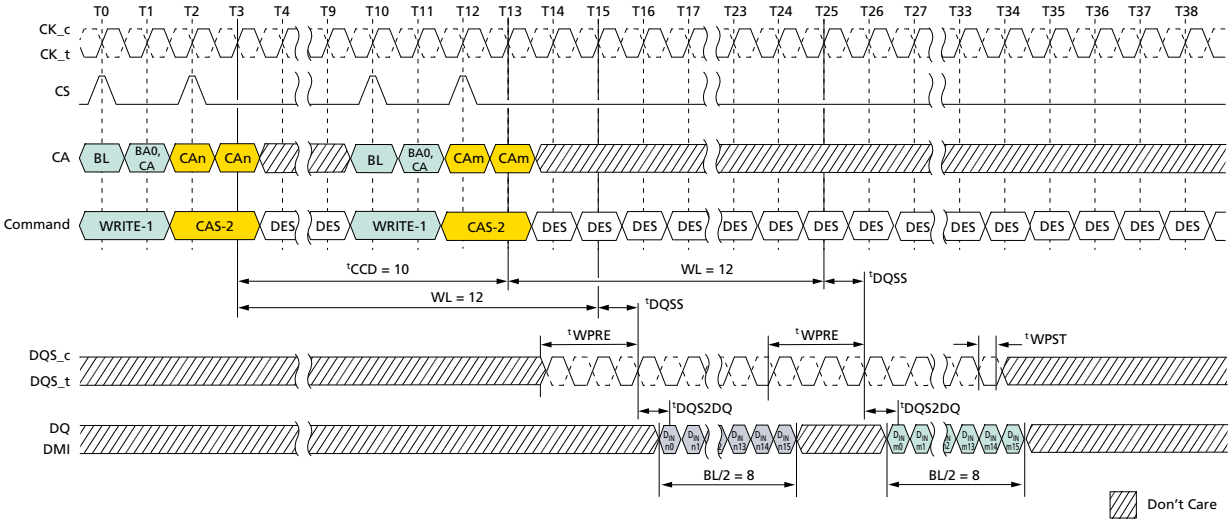
Notes: 1. BL = 16, Write postamble = 0.5*n*CK.
2. D_{IN} *n*/*m* = data-in from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 139: Consecutive WRITE: ^{t}CCD = MIN + 1, 1.5*n*CK Postamble



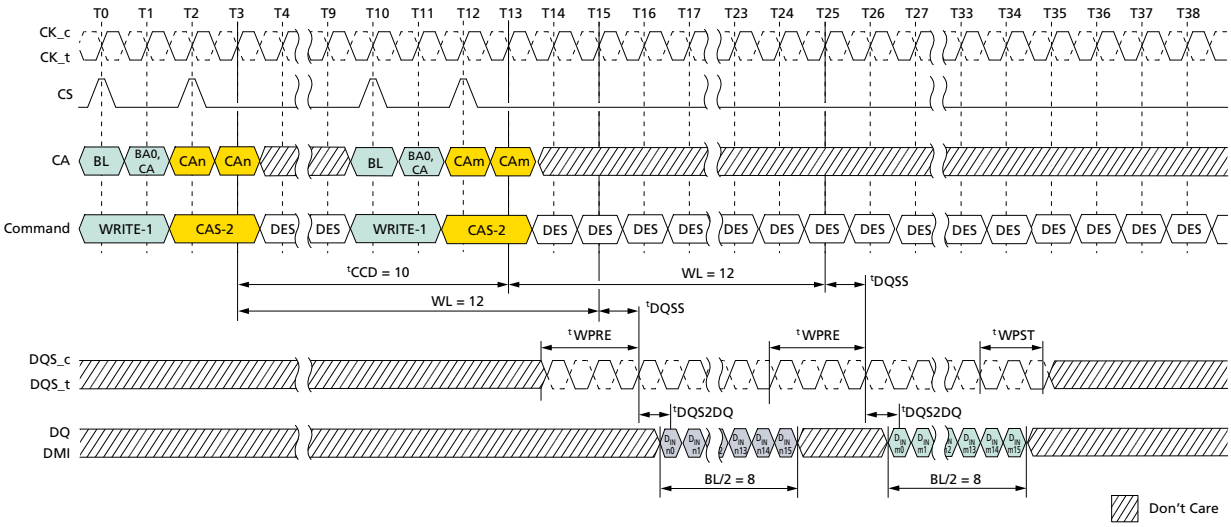
Notes: 1. BL = 16, Write postamble = 1.5*n*CK.
2. D_{IN} *n*/*m* = data-in from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 140: Consecutive WRITE: ^{t}CCD = MIN + 2, 0.5*n*CK Postamble



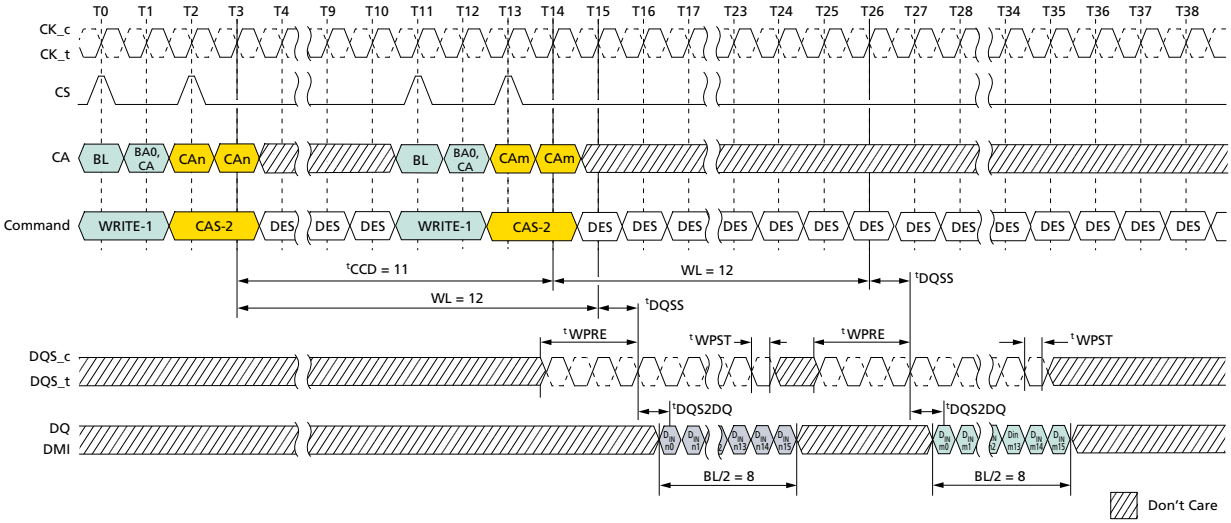
Notes: 1. BL = 16, Write postamble = 0.5*n*CK.
2. D_{IN} *n*/*m* = data-in from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 141: Consecutive WRITE: ^{t}CCD = MIN + 2, 1.5*n*CK Postamble



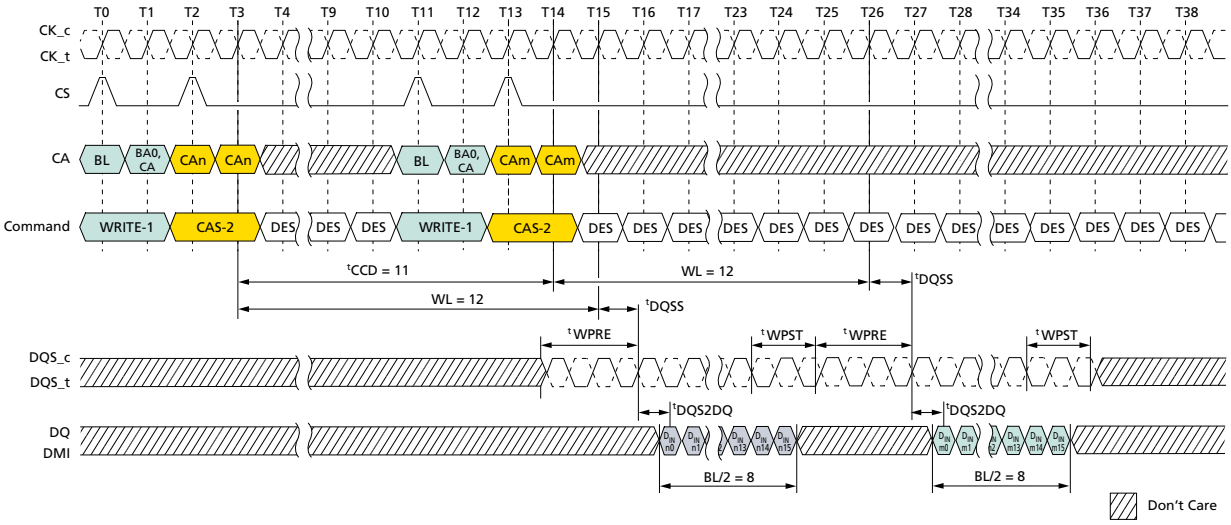
Notes: 1. BL = 16, Write postamble = 1.5*n*CK.
2. D_{IN} *n*/*m* = data-in from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 142: Consecutive WRITE: ^{t}CCD = MIN + 3, 0.5*n*CK Postamble



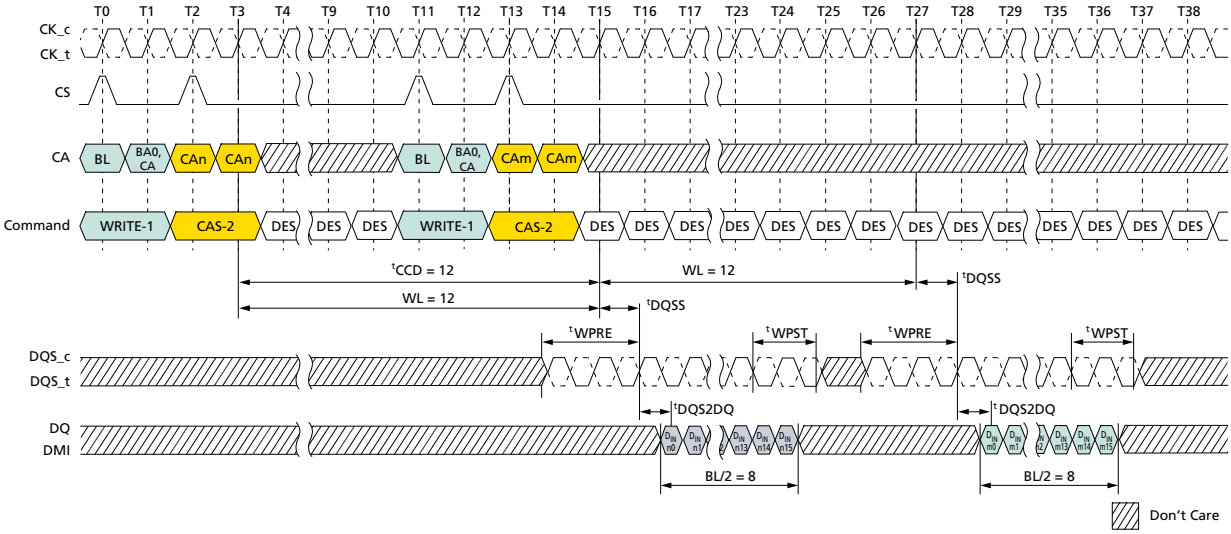
Notes: 1. BL = 16, Write postamble = 0.5*n*CK.
2. D_{IN} *n*/*m* = data-in from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 143: Consecutive WRITE: ^{t}CCD = MIN + 3, 1.5*n*CK Postamble



Notes: 1. BL = 16, Write postamble = 1.5*n*CK.
2. D_{IN} *n*/*m* = data-in from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 144: Consecutive WRITE: ^{t}CCD = MIN + 4, 1.5*n*CK Postamble



Notes: 1. BL = 16, Write postamble = 1.5*n*CK.
2. D_{IN} *n*/*m* = data-in from column *n* and column *m*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

PRECHARGE Operation

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with CKE, CS, and CA[5:0] in the proper state (see Command Truth Table). The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. The all banks (AB) flag and the bank address bit are used to determine which bank(s) to precharge. The precharged bank(s) will be available for subsequent row access ^{t}RPab after an all-bank PRECHARGE command is issued, or ^{t}RPpb after a single-bank PRECHARGE command is issued.

To ensure that the device can meet the instantaneous current demands, the row precharge time for an all-bank PRECHARGE (^{t}RPab) is longer than the per-bank precharge time (^{t}RPpb).

Table 143: Precharge Bank Selection

AB (CA[5], R1)	BA2 (CA[2], R2)	BA1 (CA[1], R2)	BA0 (CA[0], R2)	Precharged Bank
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 4 only
0	1	0	1	Bank 5 only
0	1	1	0	Bank 6 only
0	1	1	1	Bank 7 only
1	Don't Care	Don't Care	Don't Care	All banks

Burst READ Operation Followed by Precharge

The PRECHARGE command can be issued as early as BL/2 clock cycles after a READ command, but the PRECHARGE command cannot be issued until after ^{t}RAS is satisfied. A new bank ACTIVATE command can be issued to the same bank after the row precharge time (^{t}RP) has elapsed. The minimum read-to-precharge time must also satisfy a minimum analog time from the second rising clock edge of the CAS-2 command. ^{t}RTP begins BL/2 - 8 clock cycles after the READ command.

Figure 145: Burst READ Followed by Precharge – BL16, Toggling Preamble, 0.5*n*CK Postamble

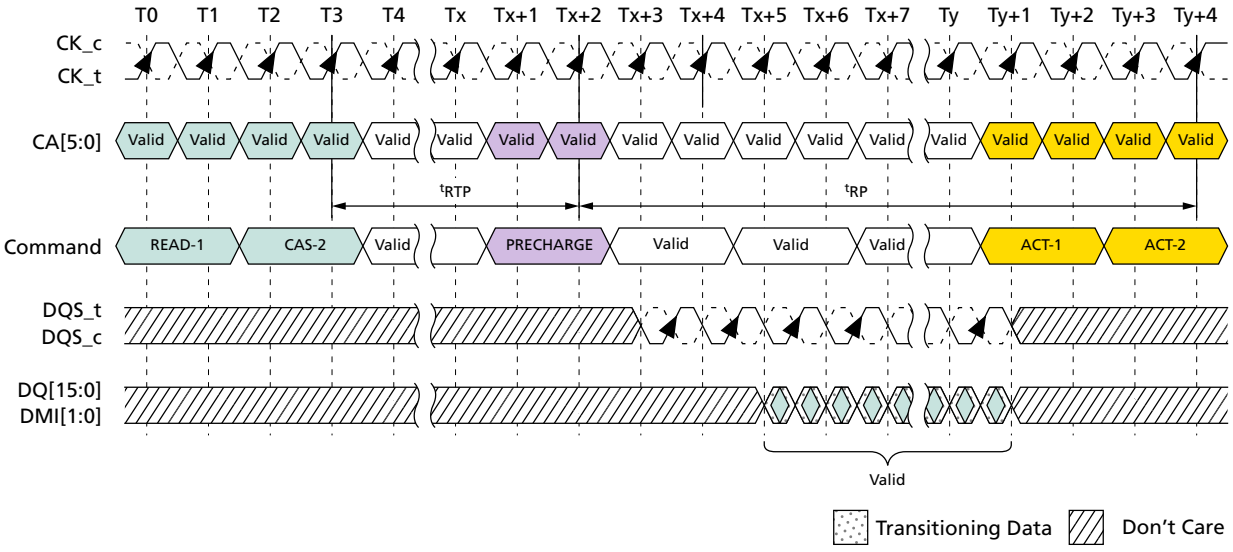
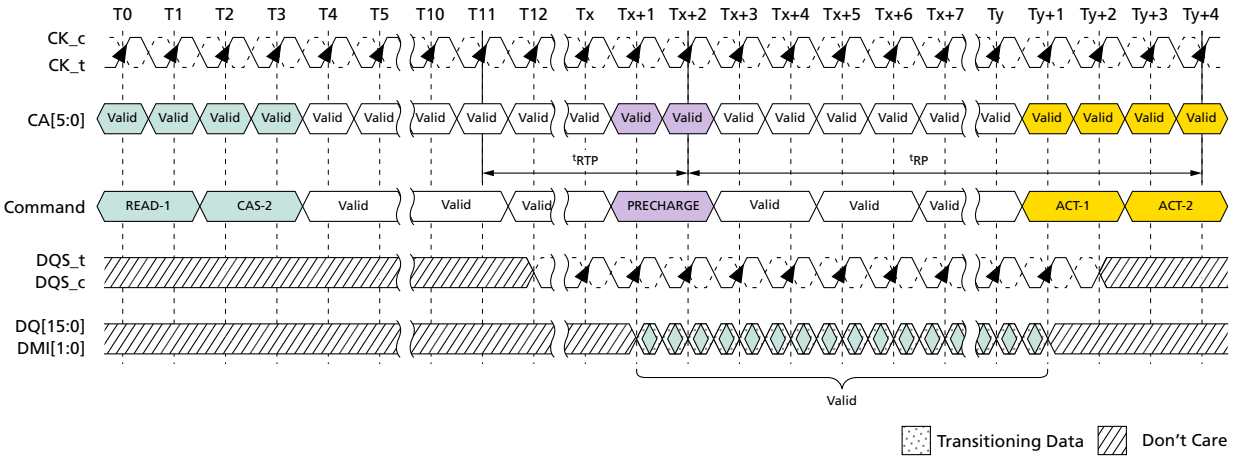


Figure 146: Burst READ Followed by Precharge – BL32, 2tCK, 0.5nCK Postamble

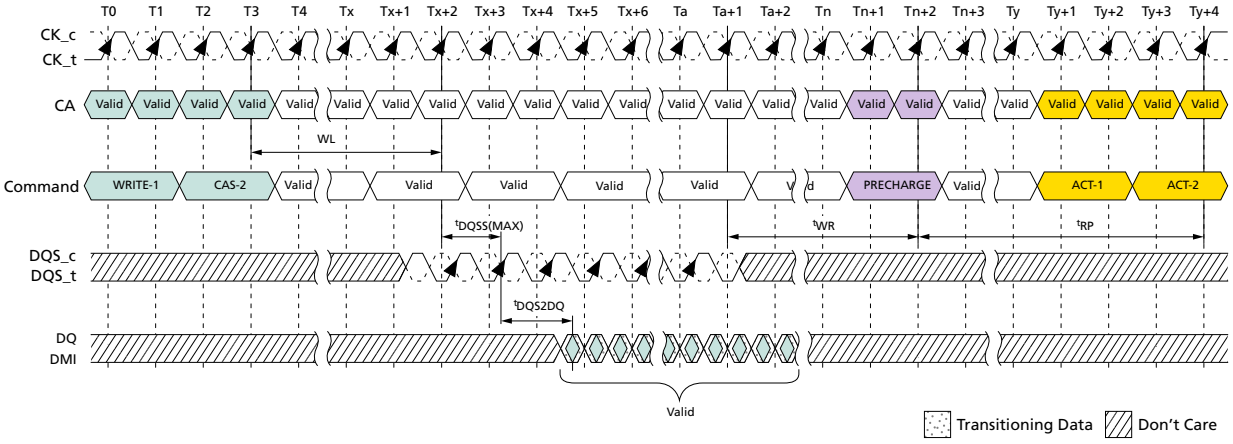


Burst WRITE Followed by Precharge

A write recovery time (tWR) must be provided before a PRECHARGE command may be issued. This delay is referenced from the next rising edge of CK after the last valid DQS clock of the burst.

Devices write data to the memory array in prefetch multiples (prefetch = 16). An internal WRITE operation can only begin after a prefetch group has been clocked; therefore, tWR starts at the prefetch boundaries. The minimum write-to-precharge time for commands to the same bank is WL + BL/2 + 1 + RU(tWR /tCK) clock cycles.

Figure 147: Burst WRITE Followed by PRECHARGE – BL16, 2nCK Preamble, 0.5nCK Postamble



Auto Precharge

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the auto precharge (AP) function. When a READ or a WRITE command is issued to the device, the AP bit (CA5) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ or WRITE cycle.

If AP is LOW when the READ or WRITE command is issued, the normal READ or WRITE burst operation is executed, and the bank remains active at the completion of the burst.

If AP is HIGH when the READ or WRITE command is issued, the auto PRECHARGE function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during

burst READ cycles (dependent upon READ or WRITE latency), thus improving system performance for random data access.

Burst READ With Auto Precharge

If AP is HIGH when a READ command is issued, the READ with AUTO PRECHARGE function is engaged. The devices start an AUTO PRECHARGE operation on the rising edge of the clock at BL/2 after the second beat of the READ w/AP command, or BL/4 - 4 + RU(^{t}RTP/^{t}CK) clock cycles after the second beat of the READ w/AP command, whichever is greater. Following an AUTO PRECHARGE operation, an ACTIVATE command can be issued to the same bank if the following two conditions are both satisfied:

1. The RAS precharge time (^{t}RP) has been satisfied from the clock at which the auto precharge began, and
2. The RAS cycle time (^{t}RC) from the previous bank activation has been satisfied.

Figure 148: Burst READ With Auto Precharge – BL16, Non-Toggling Preamble, 0.5*n*CK Postamble

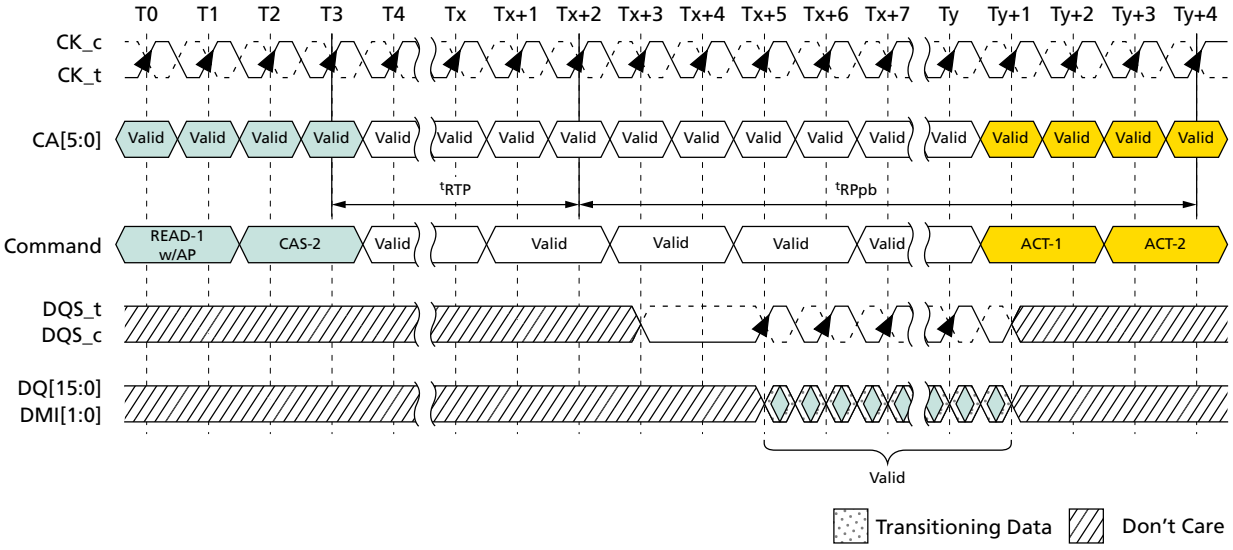
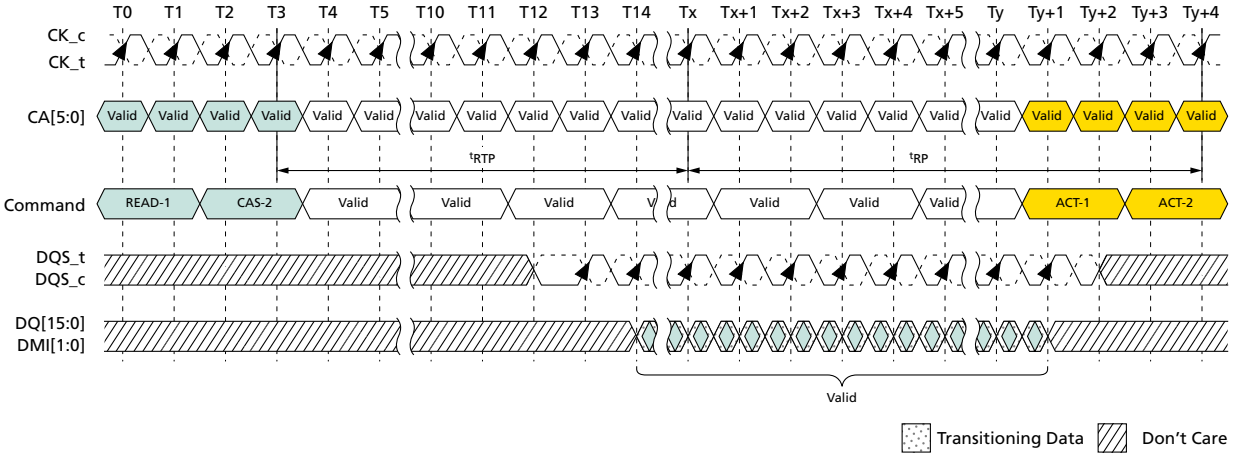


Figure 149: Burst READ With Auto Precharge – BL32, Toggling Preamble, 1.5*n*CK Postamble



Burst WRITE With Auto Precharge

If AP is HIGH when a WRITE command is issued, the WRITE with AUTO PRECHARGE function is engaged. The device starts an auto precharge on the rising edge ^{t}WR cycles after the completion of the burst WRITE.

Following a WRITE with AUTO PRECHARGE, an ACTIVATE command can be issued to the same bank if the following conditions are met:

1. The RAS precharge time (^{t}RP) has been satisfied from the clock at which the auto precharge began, and
2. The RAS cycle time (^{t}RC) from the previous bank activation has been satisfied.

Figure 150: Burst WRITE With Auto Precharge – BL16, 2*n*CK Preamble, 0.5*n*CK Postamble

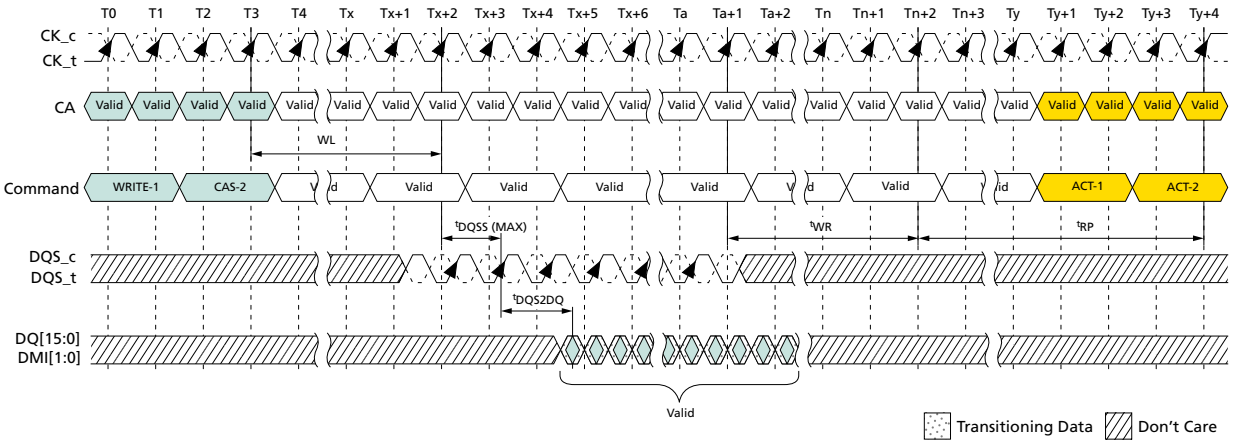


Table 144: Timing Between Commands (PRECHARGE and AUTO PRECHARGE): DQ ODT is Disable

From Command	To Command	Minimum Delay Between "From Command" and "To Command"	Unit	Notes
READ BL = 16	PRECHARGE (to same bank as READ)	^{t}RTP	^{t}CK	1, 6
	PRECHARGE ALL	^{t}RTP	^{t}CK	1, 6
READ BL = 32	PRECHARGE (to same bank as READ)	8^{t}CK + ^{t}RTP	^{t}CK	1, 6
	PRECHARGE ALL	8^{t}CK + ^{t}RTP	^{t}CK	1, 6

Table 144: Timing Between Commands (PRECHARGE and AUTO PRECHARGE): DQ ODT is Disable (Continued)

From Command	To Command	Minimum Delay Between "From Command" and "To Command"	Unit	Notes
READ w/AP BL = 16	PRECHARGE (to same bank as READ w/AP)	*n*RTP	^{t}CK	1, 10
	PRECHARGE ALL	*n*RTP	^{t}CK	1, 10
	ACTIVATE (to same bank as READ w/AP)	*n*RTP + ^{t}RPpb	^{t}CK	1, 8, 10
	WRITE or WRITE w/AP (same bank)	Illegal	–	
	MASK-WR or MASK-WR w/AP (same bank)	Illegal	–	
	WRITE or WRITE w/AP (different bank)	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 + RD(^{t}RPST) - WL + ^{t}WPRE	^{t}CK	3, 4, 5
	MASK-WR or MASK-WR w/AP (different bank)	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 + RD(^{t}RPST) - WL + ^{t}WPRE	^{t}CK	3, 4, 5
	READ or READ w/AP (same bank)	Illegal	–	
	READ or READ w/AP (different bank)	BL/2	^{t}CK	3
READ w/AP BL = 32	PRECHARGE (to same bank as READ w/AP)	8^{t}CK + *n*RTP	^{t}CK	1, 10
	PRECHARGE ALL	8^{t}CK + *n*RTP	^{t}CK	1, 10
	ACTIVATE (to same bank as READ w/AP)	8^{t}CK + *n*RTP + ^{t}RPpb	^{t}CK	1, 8, 10
	WRITE or WRITE w/AP (same bank)	Illegal	–	
	MASK-WR or MASK-WR w/AP (same bank)	Illegal	–	
	WRITE or WRITE w/AP (different bank)	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 + RD(^{t}RPST) - WL + ^{t}WPRE	^{t}CK	3, 4, 5
	MASK-WR or MASK-WR w/AP (different bank)	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 + RD(^{t}RPST) - WL + ^{t}WPRE	^{t}CK	3, 4, 5
	READ or READ w/AP (same bank)	Illegal	–	
	READ or READ w/AP (different bank)	BL/2	^{t}CK	3
WRITE BL = 16 and 32	PRECHARGE (to same bank as WRITE)	WL + BL/2 + ^{t}WR + 1	^{t}CK	1, 7
	PRECHARGE ALL	WL + BL/2 + ^{t}WR + 1	^{t}CK	1, 7
MASK-WR BL = 16	PRECHARGE (to same bank as MASK-WR)	WL + BL/2 + ^{t}WR + 1	^{t}CK	1, 7
	PRECHARGE ALL	WL + BL/2 + ^{t}WR + 1	^{t}CK	1, 7

Table 144: Timing Between Commands (PRECHARGE and AUTO PRECHARGE): DQ ODT is Disable (Continued)

From Command	To Command	Minimum Delay Between "From Command" and "To Command"	Unit	Notes
WRITE w/AP BL = 16 and 32	PRECHARGE (to same bank as WRITE w/AP)	WL + BL/2 + *n*WR + 1	^{t}CK	1, 11
	PRECHARGE ALL	WL + BL/2 + *n*WR + 1	^{t}CK	1, 11
	ACTIVATE (to same bank as WRITE w/AP)	WL + BL/2 + *n*WR + 1 + ^{t}RPpb	^{t}CK	1, 8, 11
	WRITE or WRITE w/AP (same bank)	Illegal	–	
	READ or READ w/AP (same bank)	Illegal	–	
	WRITE or WRITE w/AP (different bank)	BL/2	^{t}CK	3
	MASK-WR or MASK-WR w/AP (different bank)	BL/2	^{t}CK	3
	READ or READ w/AP (different bank)	WL + BL/2 + ^{t}WTR + 1	^{t}CK	3, 9
MASK-WR w/AP BL = 16	PRECHARGE (to same bank as MASK-WR w/AP)	WL + BL/2 + *n*WR +1	^{t}CK	1, 11
	PRECHARGE ALL	WL + BL/2 + *n*WR + 1	^{t}CK	1, 11
	ACTIVATE (to same bank as MASK-WR w/AP)	WL + BL/2 + *n*WR + 1 + ^{t}RPpb	^{t}CK	1, 8, 11
	WRITE or WRITE w/AP (same bank)	Illegal	–	3
	MASK-WR or MASK-WR w/AP (same bank)	Illegal	–	3
	WRITE or WRITE w/AP (different bank)	BL/2	^{t}CK	3
	MASK-WR or MASK-WR w/AP (different bank)	BL/2	^{t}CK	3
	READ or READ w/AP (same bank)	Illegal	–	3
	READ or READ w/AP (different bank)	WL + BL/2 + ^{t}WTR + 1	^{t}CK	3, 9
PRECHARGE	PRECHARGE (to same bank as PRECHARGE)	4	^{t}CK	1
	PRECHARGE ALL	4	^{t}CK	1
PRECHARGE ALL	PRECHARGE	4	^{t}CK	1
	PRECHARGE ALL	4	^{t}CK	1

Notes: 1. For a given bank, the precharge period should be counted from the latest PRECHARGE command, whether per-bank or all-bank, issued to that bank. The precharge period is satisfied ^{t}RP after that latest PRECHARGE command.
2. Any command issued during the minimum delay time as specified in the table above is illegal.

3. After READ w/AP, seamless READ operations to different banks are supported. After WRITE w/AP or MASK-WR w/AP, seamless WRITE operations to different banks are supported. READ, WRITE, and MASK-WR operations may not be truncated or interrupted.
4. ^{t}RPST values depend on MR1 OP[7] respectively.
5. ^{t}WPRE values depend on MR1 OP[2] respectively.
6. Minimum delay between "from command" and "to command" in clock cycle is calculated by dividing ^{t}RTP (in ns) by ^{t}CK (in ns) and rounding up to the next integer: Minimum delay [cycles] = roundup(^{t}RTP [ns]/^{t}CK [ns]).
7. Minimum delay between "from command" and "to command" in clock cycle is calculated by dividing ^{t}WR (in ns) by ^{t}CK (in ns) and rounding up to the next integer: Minimum delay [cycles] = roundup(^{t}WR [ns]/^{t}CK [ns]).
8. Minimum delay between "from command" and "to command" in clock cycle is calculated by dividing ^{t}RPpb (in ns) by ^{t}CK (in ns) and rounding up to the next integer: Minimum delay [cycles] = roundup(^{t}RPpb [ns]/^{t}CK [ns]).
9. Minimum delay between "from command" and "to command" in clock cycle is calculated by dividing ^{t}WTR (in ns) by ^{t}CK (in ns) and rounding up to the next integer: Minimum delay [cycles] = roundup(^{t}WTR [ns]/^{t}CK [ns]).
10. For READ w/AP the value is *n*RTP, which is defined in mode register 2.
11. For WRITE w/AP the value is *n*WR, which is defined in mode register 1.

Table 145: Timing Between Commands (PRECHARGE and AUTO PRECHARGE): DQ ODT is Enable

From Command	To Command	Minimum Delay Between "From Command" and "To Command"	Unit	Notes
READ w/AP BL = 16	WRITE or WRITE w/AP (different bank)	RL + RU(tDQSCK(MAX)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/tCK) + 1	tCK	2, 3
	MASK-WR or MASK-WR w/AP (different bank)	RL + RU(tDQSCK(MAX)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/tCK) + 1	tCK	2, 3
READ w/AP BL = 32	WRITE or WRITE w/AP (different bank)	RL + RU(tDQSCK(MAX)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/tCK) + 1	tCK	2, 3
	MASK-WR or MASK-WR w/AP (different bank)	RL + RU(tDQSCK(MAX)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/tCK) + 1	tCK	2, 3

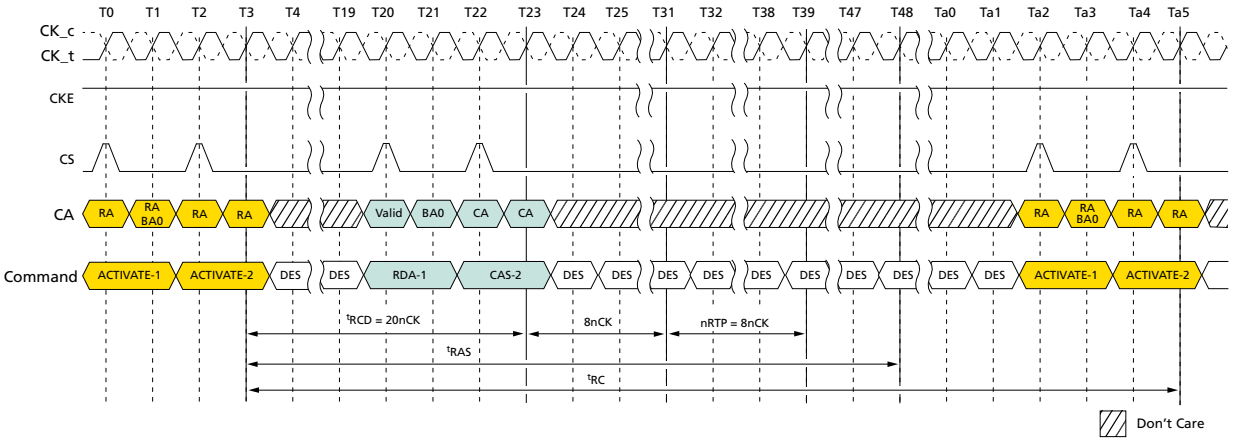
Notes: 1. The rest of the timing about PRECHARGE and AUTO PRECHARGE is same as DQ ODT is disable case.
2. After READ w/AP, seamless read operations to different banks are supported. READ, WRITE, and MASK-WR operations may not be truncated or interrupted.
3. tRPST values depend on MR1 OP[7] respectively.

RAS Lock Function

READ with AUTO PRECHARGE or WRITE/MASK WRITE with AUTO PRECHARGE commands may be issued after tRCD has been satisfied. The LPDDR4 SDRAM RAS lockout feature will schedule the internal precharge to assure that tRAS is satisfied. tRC needs to be satisfied prior to issuing subsequent ACTIVATE commands to the same bank.

The figure below shows example of RAS lock function.

Figure 151: Command Input Timing with RAS Lock

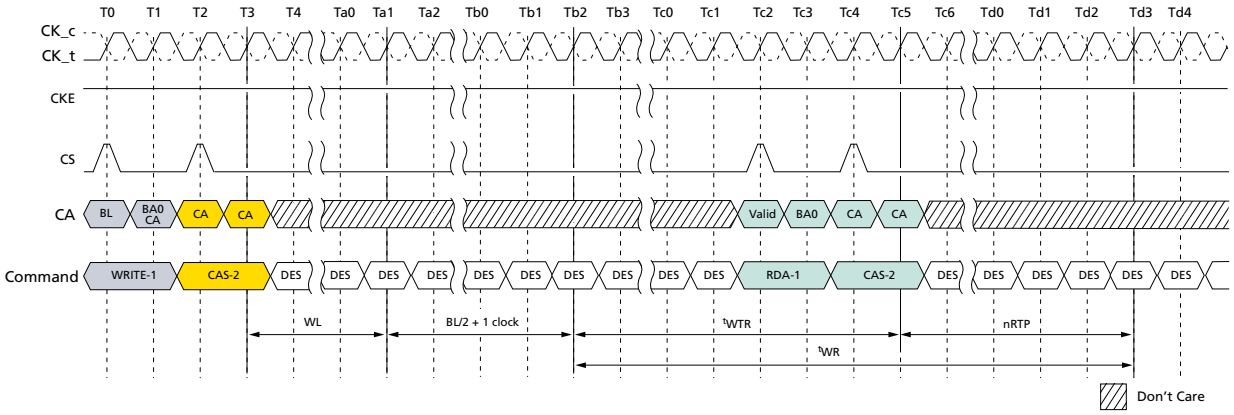


Notes: 1. tCK (AVG) = 0.938ns, Data rate = 2133 Mb/s, tRCD(MIN) = MAX(18ns, 4*n*CK), tRAS(MIN) = MAX(42ns, 3*n*CK), *n*RTP = 8*n*CK, BL = 32.
2. tRCD = 20*n*CK comes from roundup(18ns/0.938ns).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Delay Time From WRITE-to-READ with Auto Precharge

In the case of WRITE command followed by READ with AUTO PRECHARGE, controller must satisfy tWR for the WRITE command before initiating the device internal auto-precharge. It means that (tWTR + *n*RTP) should be equal or longer than (tWR) when BL setting is 16, as well as (tWTR + *n*RTP + 8*n*CK) should be equal or longer than (tWR) when BL setting is 32. Refer to the following figure for details.

Figure 152: Delay Time From WRITE-to-READ with Auto Precharge



Notes: 1. Burst length at read = 16.
2. DES commands are shown for ease of illustration; other commands may be valid at these times.

REFRESH Command

The REFRESH command is initiated with CS HIGH, CA0 LOW, CA1 LOW, CA2 LOW, CA3 HIGH and CA4 LOW at the first rising edge of clock. Per-bank REFRESH is initiated with CA5 LOW at the first rising edge of the clock. The all-bank REFRESH is initiated with CA5 HIGH at the first rising edge of clock.

A per-bank REFRESH command (REFpb) is performed to the bank address as transferred on CA0, CA1, and CA2 on the second rising edge of the clock. Bank address BA0 is transferred on CA0, bank address BA1 is transferred on CA1, and bank address BA2 is transferred on CA2. A per-bank REFRESH command (REFpb) to the eight banks can be issued in any order. For example, REFpb commands may be issued in the following order: 1-3-0-2-4-7-5-6. After the eight banks have been refreshed using the per-bank REFRESH command, the controller can send another set of per-bank REFRESH commands in the same order or a different order. One possible order can be a sequential round robin: 0-1-2-3-4-5-6-7. It is illegal to send a per-bank REFRESH command to the same bank unless all eight banks have been refreshed using the per-bank REFRESH command. The count of eight REFpb commands starts with the first REFpb command after a synchronization event.

The bank count is synchronized between the controller and the device by resetting the bank count to zero. Synchronization can occur upon reset procedure or at every exit from self refresh. The REFab command also synchronizes the counter between the controller and the device to zero. The device can be placed in self refresh, or a REFab command can be issued at any time without cycling through all eight banks using per-bank REFRESH command. After the bank count is synchronized to zero, the controller can issue per-bank REFRESH commands in any order, as described above.

A REFab command issued when the bank counter is not zero will reset the bank counter to zero and the device will perform refreshes to all banks as indicated by the row counter. If another REFRESH command (REFab or REFpb) is issued after the REFab command then it uses an incremented value of the row counter.

The table below shows examples of both bank and refresh counter increment behavior.

Table 146: Bank and Refresh Counter Increment Behavior

#	Command	BA2	BA1	BA0	Refresh Bank #	Bank Counter #	Ref. Counter # (Row Address #)
0	Reset, SRX, or REFab					To 0	–

Table 146: Bank and Refresh Counter Increment Behavior (Continued)

#	Command	BA2	BA1	BA0	Refresh Bank #	Bank Counter #	Ref. Counter # (Row Address #)
1	REFpb	0	0	0	0	0 to 1	n
2	REFpb	0	0	1	1	1 to 2	
3	REFpb	0	1	0	2	2 to 3	
4	REFpb	0	1	1	3	3 to 4	
5	REFpb	1	0	0	4	4 to 5	
6	REFpb	1	0	1	5	5 to 6	
7	REFpb	1	1	0	6	6 to 7	
8	REFpb	1	1	1	7	7 to 0	
9	REFpb	1	1	0	6	0 to 1	n + 1
10	REFpb	1	1	1	7	1 to 2	
11	REFpb	0	0	1	1	2 to 3	
12	REFpb	0	1	1	3	3 to 4	
13	REFpb	1	0	1	5	4 to 5	
14	REFpb	0	1	0	2	5 to 6	
15	REFpb	0	0	0	0	6 to 7	
16	REFpb	1	0	0	4	7 to 0	
17	REFpb	0	0	0	0	0 to 1	n + 2
18	REFpb	0	0	1	1	1 to 2	
19	REFpb	0	1	0	2	2 to 3	
20	***REFab***	***V***	***V***	***V***	***0 to 7***	***To 0***	***n + 2***
21	REFpb	1	1	0	6	0 to 1	n + 3
22	REFpb	1	1	1	7	1 to 2	
Snip							

A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions have been met:

- ^{t}RFCab has been satisfied after the prior REFab command
- ^{t}RFCpb has been satisfied after the prior REFpb command
- ^{t}RP has been satisfied after the prior PRECHARGE command to that bank
- ^{t}RRD has been satisfied after the prior ACTIVATE command (for example, after activating a row in a different bank than the one affected by the REFpb command)

The target bank is inaccessible during per-bank REFRESH cycle time (^{t}RFCpb). However, other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or a WRITE command. When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, the following conditions must be met:

- ^{t}RFCpb must be satisfied before issuing a REFab command
- ^{t}RFCpb must be satisfied before issuing an ACTIVATE command to the same bank
- ^{t}RRD must be satisfied before issuing an ACTIVATE command to a different bank

- ^{t}RFCpb must be satisfied before issuing another REFpb command

An all-bank REFRESH command (REFab) issues a REFRESH command to every bank in a channel. All banks must be idle when REFab is issued (for example, by issuing a PRECHARGE ALL command prior to issuing an all-bank REFRESH command). The REFab command must not be issued to the device until the following conditions have been met:

- ^{t}RFCab has been satisfied following the prior REFab command
- ^{t}RFCpb has been satisfied following the prior REFpb command
- ^{t}RP has been satisfied following the prior PRECHARGE command

When an all-bank REFRESH cycle has completed, all banks will be idle. After issuing REFab:

- RFCab latency must be satisfied before issuing an ACTIVATE command,
- RFCab latency must be satisfied before issuing a REFab or REFpb command

Table 147: REFRESH Command Timing Constraints

Symbol	Minimum Delay From...	To	Notes
^{t}RFCab	REFab	REFab	
		ACTIVATE command to any bank	
		REFpb	
^{t}RFCpb	REFpb	REFab	
		ACTIVATE command to same bank as REFpb	
		REFpb	
^{t}RRD	REFpb	ACTIVATE command to a different bank than REFpb	
	ACTIVATE	REFpb	1
		ACTIVATE command to a different bank than the prior ACTIVATE command	

Note: 1. A bank must be in the idle state before it is refreshed; therefore, REFab is prohibited following an ACTIVATE command. REFpb is supported only if it affects a bank that is in the idle state.

Figure 153: All-Bank REFRESH Operation

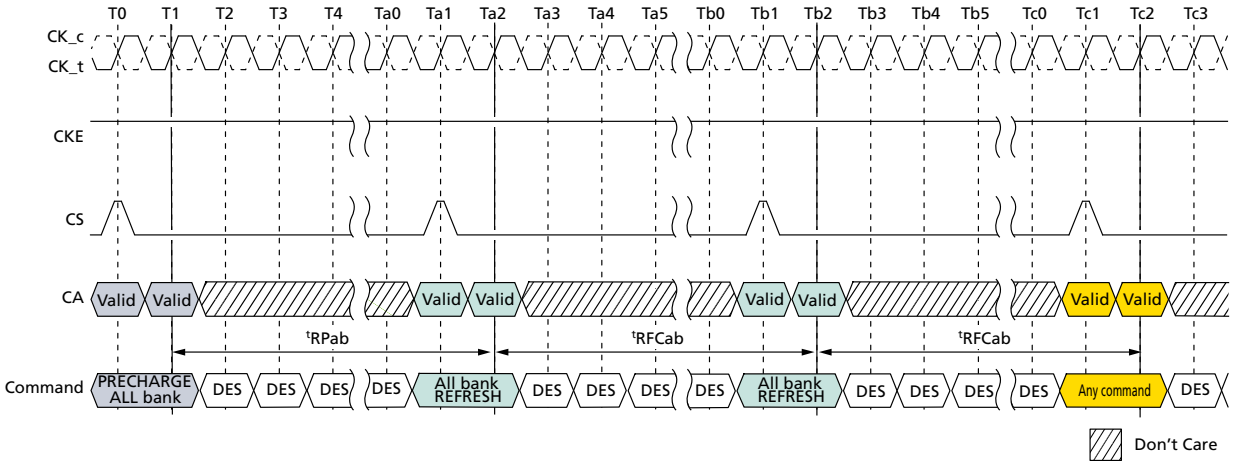
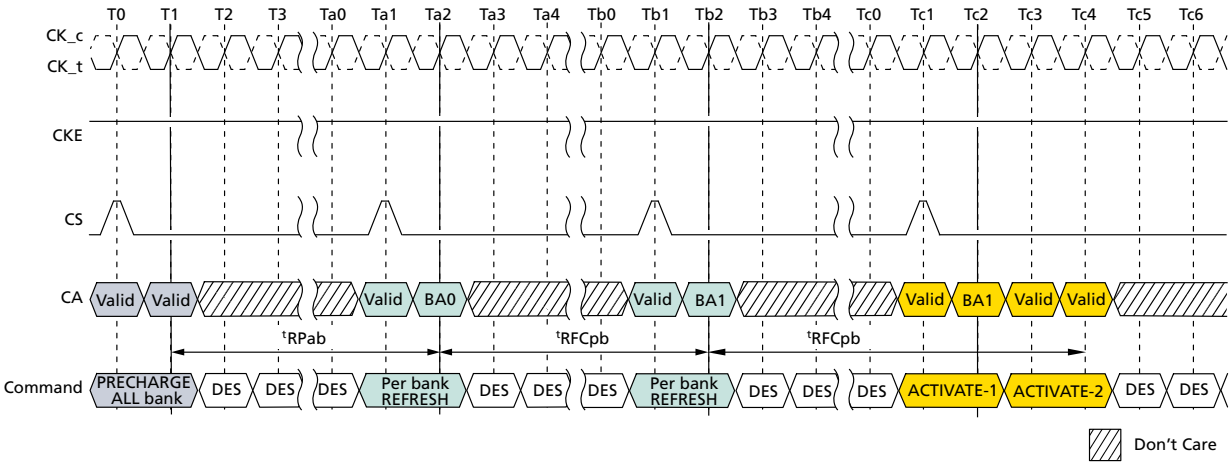


Figure 154: Per-Bank REFRESH Operation



Notes: 1. In the beginning of this example, the REFpb bank is pointing to bank 0.
2. Operations to banks other than the bank being refreshed are supported during the ^{t}RFCpb period.

In general, a REFRESH command needs to be issued to the device regularly every ^{t}REFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be postponed during operation of the device, but at no point in time are more than a total of eight REFRESH commands allowed to be postponed. And a maximum number of pulled-in or postponed REF command is dependent on refresh rate. It is described in the table below. In the case where eight REFRESH commands are postponed in a row, the resulting maximum interval between the surrounding REFRESH commands is limited to 9 × ^{t}REFI. A maximum of eight additional REFRESH commands can be issued in advance (pulled in), with each one reducing the number of regular REFRESH commands required later by one. Note that pulling in more than eight REFRESH commands in advance does not reduce the number of regular REFRESH commands required later; therefore, the resulting maximum interval between two surrounding REFRESH commands is limited to 9 × ^{t}REFI. At any given time, a maximum of 16 REFRESH commands can be issued within 2 × ^{t}REFI.

Self refresh mode may be entered with a maximum of eight REFRESH commands being postponed. After exiting self refresh mode with one or more REFRESH commands postponed, additional REFRESH commands may be postponed to the extent that the total number of postponed REFRESH commands (before and after self refresh) will never exceed eight. During self refresh mode, the number of postponed or pulled-in REFRESH commands does not change.

And for per-bank refresh, a maximum of 8 x 8 per-bank REFRESH commands can be postponed or pulled in for scheduling efficiency. At any given time, a maximum of 2 x 8 x 8 per-bank REFRESH commands can be issued within 2 × ^{t}REFI.

Table 148: Legacy REFRESH Command Timing Constraints

MR4 OP[2:0]	Refresh rate	Max. No. of pulled-in or postponed REFab	Max. Interval between two REFab	Max. No. of REFab[1]	Per-bank REFRESH
000b	Low temp. limit	N/A	N/A	N/A	N/A
001b	4 × ^{t}REFI	8	9 × 4 × ^{t}REFI	16	1/8 of REFab
010b	2 × ^{t}REFI	8	9 × 2 × ^{t}REFI	16	1/8 of REFab
011b	1 × ^{t}REFI	8	9 × ^{t}REFI	16	1/8 of REFab
100b	0.5 × ^{t}REFI	8	9 × 0.5 × ^{t}REFI	16	1/8 of REFab

Table 148: Legacy REFRESH Command Timing Constraints (Continued)

MR4 OP[2:0]	Refresh rate	Max. No. of pulled-in or postponed REFab	Max. Interval between two REFab	Max. No. of REFab[1]	Per-bank REFRESH
101b	0.25 × ^{t}REFI	8	9 × 0.25 × ^{t}REFI	16	1/8 of REFab
110b	0.25 × ^{t}REFI	8	9 × 0.25 × ^{t}REFI	16	1/8 of REFab
111b	High temp. limit	N/A	N/A	N/A	N/A

Note: 1. Maximum number of REFab within MAX(2 × ^{t}REFI × refresh rate multiplier, 16 × ^{t}RFC).

Table 149: Modified REFRESH Command Timing Constraints

MR4 OP[2:0]	Refresh Rate	Max. No. of Pulled-in or Postponed REFab	Max. Interval between Two REFab	Max. No. of REFab[1]	Per-bank REFRESH
000B	Low temp. limit	N/A	N/A	N/A	N/A
001B	4 × ^{t}REFI	2	3 × 4 × ^{t}REFI	4	1/8 of REFab
010B	2 × ^{t}REFI	4	5 × 2 × ^{t}REFI	8	1/8 of REFab
011B	1 × ^{t}REFI	8	9 × ^{t}REFI	16	1/8 of REFab
100B	0.5 × ^{t}REFI	8	9 × 0.5 × ^{t}REFI	16	1/8 of REFab
101B	0.25 × ^{t}REFI	8	9 × 0.25 × ^{t}REFI	16	1/8 of REFab
110B	0.25 × ^{t}REFI	8	9 × 0.25 × ^{t}REFI	16	1/8 of REFab
111B	High temp. limit	N/A	N/A	N/A	N/A

Notes: 1. For any thermal transition phase where refresh mode is transitioned to either 2 × ^{t}REFI or 4 × ^{t}REFI, LPDDR4 devices will support the previous postponed refresh requirement provided the number of postponed refreshes is monotonically reduced to meet the new requirement. However, the pulled-in REFRESH commands in the previous thermal phase are not applied in the new thermal phase. Entering a new thermal phase, the controller must count the number of pulled-in REFRESH commands as zero, regardless of the number of remaining pulled-in REFRESH commands in the previous thermal phase.

2. LPDDR4 devices are refreshed properly if the memory controller issues REFRESH commands with same or shorter refresh period than reported by MR4 OP[2:0]. If a shorter refresh period is applied, the corresponding requirements from this table apply. For example, when MR4 OP[2:0] = 001b, the controller can be in any refresh rate from 4 × ^{t}REFI to 0.25 × ^{t}REFI. When MR4 OP[2:0] = 010b, the only prohibited refresh rate is 4 × ^{t}REFI.

Figure 155: Postponing REFRESH Commands (Example)

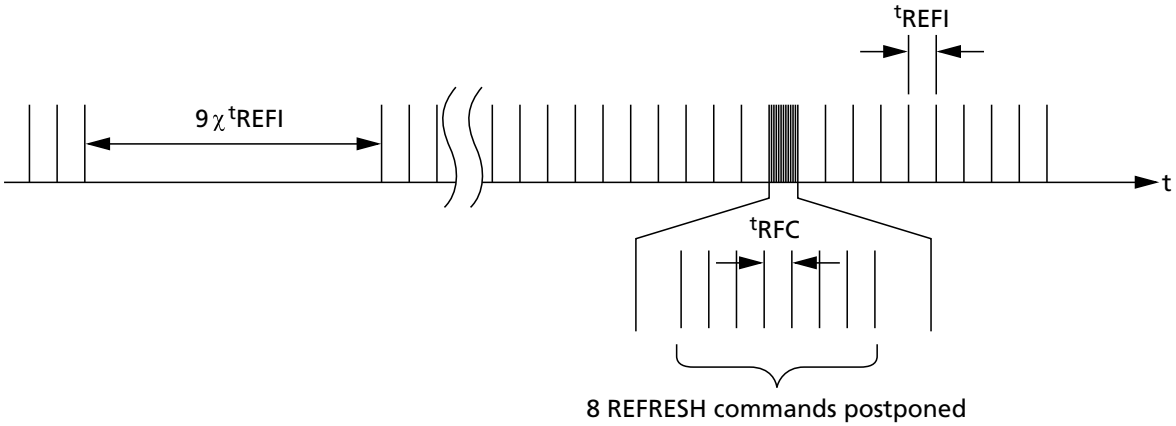
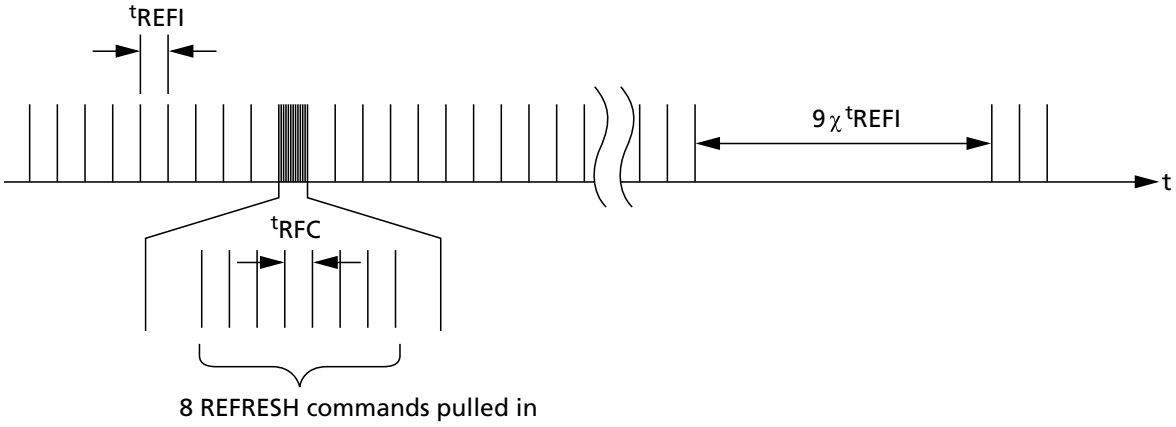
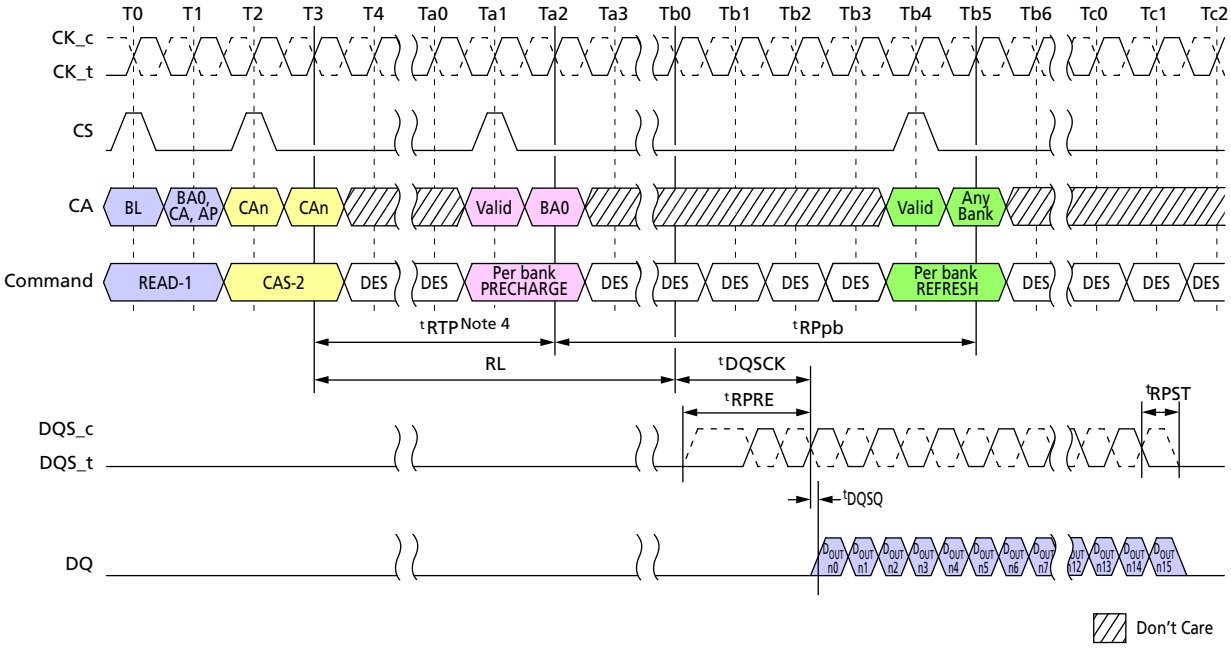


Figure 156: Pulling in REFRESH Commands (Example)



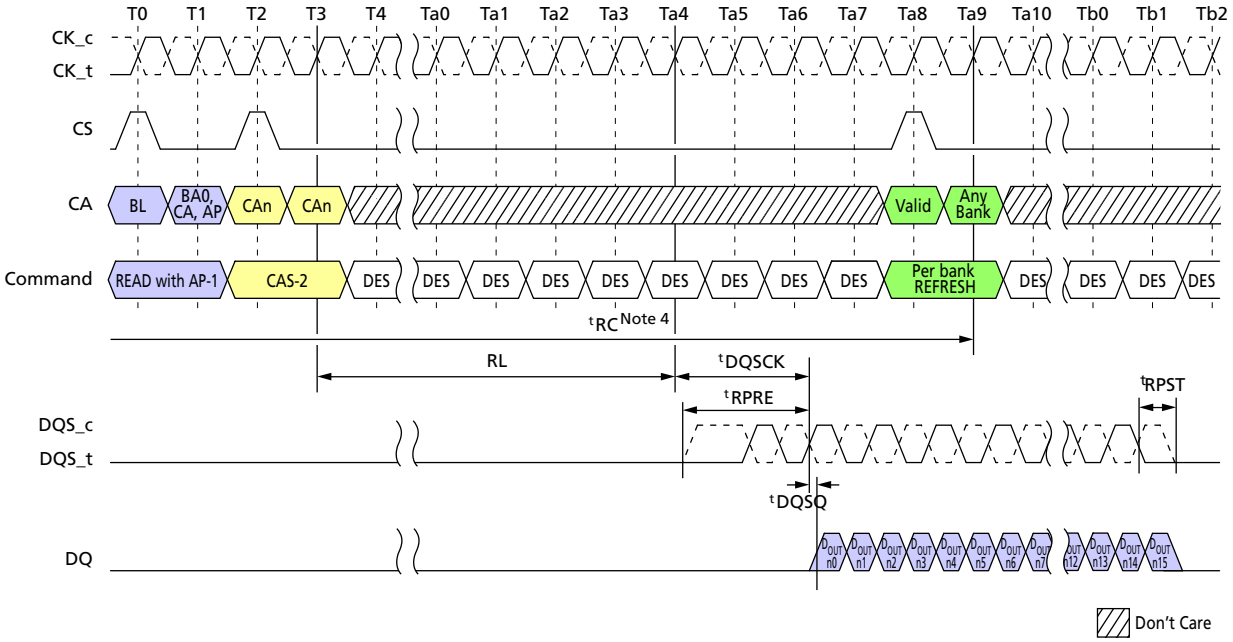
Burst READ Operation Followed by Per-Bank Refresh

Figure 157: Burst READ Operation Followed by Per-Bank Refresh



Notes: 1. The per-bank REFRESH command can be issued after tRTP + tRPpb from READ command.
2. BL = 16; Preamble = Toggle; Postamble = 0.5*n*CK; DQ/DQS: V_{SSQ} termination.
3. D_{OUT} *n* = data-out from column *n*.
4. In the case of BL = 32, delay time from read to per-bank precharge is 8*n*CK + tRTP.
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 158: Burst READ With AUTO PRECHARGE Operation Followed by Per-Bank Refresh



Notes: 1. BL = 16; Preamble = Toggle; Postamble = 0.5*n*CK; DQ/DQS: V_{SSQ} termination.
2. D_{OUT} *n* = data-out from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. ^{t}RC needs to be satisfied prior to issuing a subsequent per-bank REFRESH command.

Refresh Requirement

Between the SRX command and SRE command, at least one extra REFRESH command is required. After the SELF REFRESH EXIT command, in addition to the normal REFRESH command at ^{t}REFI interval, the device requires a minimum of one extra REFRESH command prior to the SELF REFRESH ENTRY command.

Table 150: Refresh Requirement Parameters

Parameter		Symbol	Density (per channel)							Unit
			2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	
Number of banks per channel		–	8							–
Refresh window (^{t}REFW): (1 × Refresh)[3]		^{t}REFW	32							ms
Required number of REFRESH commands in ^{t}REFW window		R	8192							–
Average refresh interval (1 × Refresh)[3]	REFab	^{t}REFI	3.906							µs
	REFpb	^{t}REFIpb	488							ns
REFRESH cycle time (all banks)		^{t}RFCab	130	180		280		380		ns
REFRESH cycle time (per bank)		^{t}RFCpb	60	90		140		190		ns
Per bank refresh to per bank refresh time (different bank)		^{t}PBR2PBR	60	90		90		90		ns

Notes: 1. Refresh for each channel is independent of the other channel on the die, or other channels in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.
2. Self refresh abort feature is available for higher density devices starting with 6Gb density per channel device and ^{t}XSR_abort(MIN) is defined as ^{t}RFCpb + 17.5ns.
3. Refer to MR4 OP[2:0] for detailed refresh rate and its multipliers.

Refresh Management Command

Refresh Management Command Definition

Periods of high LPDDR4 SDRAM activity may require additional REFRESH commands to protect the integrity of the device data. The devices that require additional activity based refreshes include support for an activation-based REFRESH MANAGEMENT (RFM) command. The device will indicate the requirement for additional refresh management (RFM) by setting read-only MR24 opcode bit 0. OP[0] = 0 indicates no additional refresh management is needed beyond the requirement in the Refresh section of the specification. However, specific attempts to bypass the on-die circuitry designed to protect data integrity may result in data disturb. OP[0] = 1 indicates additional refresh management is required.

A suggested implementation of refresh management by the controller monitors ACT commands issued per bank to the device. This activity can be monitored as a rolling accumulated ACT (RAA) count. Each ACT command increments the RAA count by one for the individual bank receiving the ACT command.

When the RAA counter reaches a DRAM vendor-specified initial management threshold (RAAIMT), which is set by the DRAM vendor in the read-only MR24 opcode bits 5:1, additional LPDRAM refresh management may be required. Executing the RFM command allows additional time for the LPDRAM to manage refresh internally. The RFM operation can be initiated to all banks on the LPDRAM with the RFMab command, or to a single bank with the RFMpb command.

The RFM command bits are the same as the REF command, except for CA3. If the refresh management required bit is 0 (MR24 OP[0] = 0), the state of CA3 is ignored. If the refresh management required bit is 1 (MR24 OP[0] = 1), CA3 = L executes the REF command and CA3 = H executes an RFMab command if CA5 = H or an RFMpb command if CA5 = L.

Table 151: REFRESH Command With RFM

Command	CS	SDR Command/Address Pins						CK Edge
		CA0	CA1	CA2	CA3	CA4	CA5	
REFRESH	H	L	L	L	H	L	AB	R1
	L	BA0	BA1	BA2	RFM	V	V	R2

Notes: 1. CA3 R2 edge is V when RFM is not required, but becomes RFM when read-only MR24 OP[0] = 1b.
2. Issuing the RFMpb or RFMab command allows the device to use the command period for additional refresh management.

Table 152: Refresh Management Parameters

Refresh Requirements	Symbol	Density per channel									Units
		2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb	
Refresh management cycle time – all bank	^{t}RFMab	TBD	TBD	TBD	TBD	210	280	280	TBD	TBD	ns
Refresh management cycle time – per bank	^{t}RFMpb	TBD	TBD	TBD	TBD	170	190	190	TBD	TBD	ns

When an RFM command is issued to the device, the RAA counter in any bank receiving the command can be decremented. The decrease in RAA count for an RFM command is determined by the RAAIMT multiplier value RAADEC, set by MR36 OP[1:0]. Issuing a RFMab command allows the RAA count in all banks to be decremented by the RAAIMT multiplied by the RAADEC value. Issuing an RFMpb command with BA[2:0] allows the RAA count only for the bank specified by BA[2:0] to be decremented by RAAIMT × RAADEC.

The RAA counter can only be decremented to a minimum RAA value of 0. No negative RAA value or pull-in of RFM command is allowed.

RFM commands are allowed to accumulate or postpone, but the RAA counter should never exceed the vendor-specified RAA maximum management threshold (RAAMMT), which is determined by multiplying the RAAIMT value by the RAAMULT value set by the DRAM vendor in read-only MR24 OP[7:6]. If the RAA counter for a bank reaches RAAMMT, no additional ACT commands are allowed to that LPDRAM bank until one or more REF or RFM commands have been issued to reduce the RAA counter below the maximum value.

RFM command scheduling should meet the same minimum separation requirements as those for the REF command.

An RFM command does not replace the requirement for the controller to issue periodic REF commands to the LPDRAM. The RFM commands are supplemental time for the LPDRAM to manage refresh internally. Issuing an REF command allows the RAA counter to be decremented by RAAIMT for the bank or banks being refreshed. Hence, any periodic REF command issued to the LPDRAM allows the RAA counter of the banks being refreshed to be decremented by the RAAIMT value. This would nominally occur once every effective refresh interval ^{t}REFIe, which is the average REFRESH command interval currently being supplied to the SDRAM. This ^{t}REFIe must be equal to or less than the MR4 OP[4:0] RM x 3.906µs. Issuing a REFab command allows the RAA count in all banks to be decremented. Issuing an REFpb command with a bank address allows the RAA count only with that bank address to be decremented. No decrement to the RAA count values is allowed for entering/exiting self refresh. The per-bank count values prior to entering self refresh will be the same upon exiting self refresh.

Issuing an RFM command also allows decrementing of the RAA counter.

Devices which require refresh management may not require RFM at every refresh rate multiplier. The refresh management threshold value RFMTH defines an effective refresh interval (^{t}REFIe) above which refresh management is required. RFMTH is determined by the equation: RFMTH = RAAIMT × ^{t}RC absolute minmum.

Maximum interval between two REFab without RFM requirement is defined with following formula ^{t}REFIe ≤ RFMTH. When RFMTH is longer than ^{t}RFEIe Interval between two REFab defined in the REFRESH Command Timing Constraints table, no RFM command is required even using maximum pull-in and postpone.

Operation at any refresh rate slower (i.e. longer ^{t}REFIe) than that indicated by RFMTH requires RFM to ensure integrity of data stored in the LPDRAM. Operation at the ^{t}REFIe indicated by RFMTH, or operation at any higher refresh rate (that is, shorter ^{t}REFIe), is exempt from RFM requirements, regardless of any RAA count value.

Refresh Management Operation Examples

Following are some operation examples to aid in understanding of the REFRESH MANAGEMENT function. Values shown are hypothetical and may not represent values from any actual device design now or in the future.

Table 153: RFM Operation Example (One Bank)

Device-Specific RFM Requirements				Current Device State		
RAAIMT	RAAMULT	RAADEC	RFMTH	tREFIe	RAA	Operating Requirements
160	4x	2x	9600ns (160 × 60ns)	7.8µs	120	No additional commands required, RAA < RAAIMT and tREFIe < RFMTH
160	4x	2x	9600ns	7.8µs	500	No additional commands required, tREFIe < RFMTH
160	4x	2x	9600ns	15.6µs	120	No additional commands required, RAA < RAAIMT
160	4x	2x	9600ns	15.6µs	500	No additional commands required immediately since RAA < RAAMMT, but RAA is approaching RAAMMT so one or more RFM commands to this bank are recommended to prevent interruption of operation
160	4x	2x	9600ns	15.6µs	640	RFM or REF command to this bank required before any ACTIVATE command to this bank, since RAA = RAAMMT. Issuing one RFMpb or RFMab command reduces RAA to 320 since RAADEC = 2x. Issuing one REFpb or REFab command reduces RAA to 480.
120	4x	1.5x	7200ns	7.8µs	480	RFM or REF command to this bank required before any ACTIVATE command to this bank, since RAA = RAAMMT. Issuing one RFMpb or RFMab command reduces RAA to 300 since RAADEC = 1.5x. Issuing one REFpb or REFab command reduces RAA to 360.

SELF REFRESH Operation

Self Refresh Entry and Exit

The SELF REFRESH command can be used to retain data in the device without external REFRESH commands. The device has a built-in timer to accommodate SELF REFRESH operation. Self refresh is entered by the SELF REFRESH ENTRY command defined by having CS HIGH, CA0 LOW, CA1 LOW, CA2 LOW, CA3 HIGH, CA4 HIGH, and CA5 valid (valid meaning that it is at a logic level HIGH or LOW) for the first rising edge, and CS LOW, CA0 valid, CA1 valid, CA2 valid, CA3 valid, CA4 valid, and CA5 valid at the second rising edge of clock. The SELF REFRESH command is only allowed when READ DATA burst is completed and the device is in the idle state.

During self refresh mode, external clock input is needed and all input pins of the device are activated. The device can accept the following commands: MRR-1, CAS-2, DES, SRX, MPC, MRW-1, and MRW-2, except PASR bank/segment mask setting and SR abort setting.

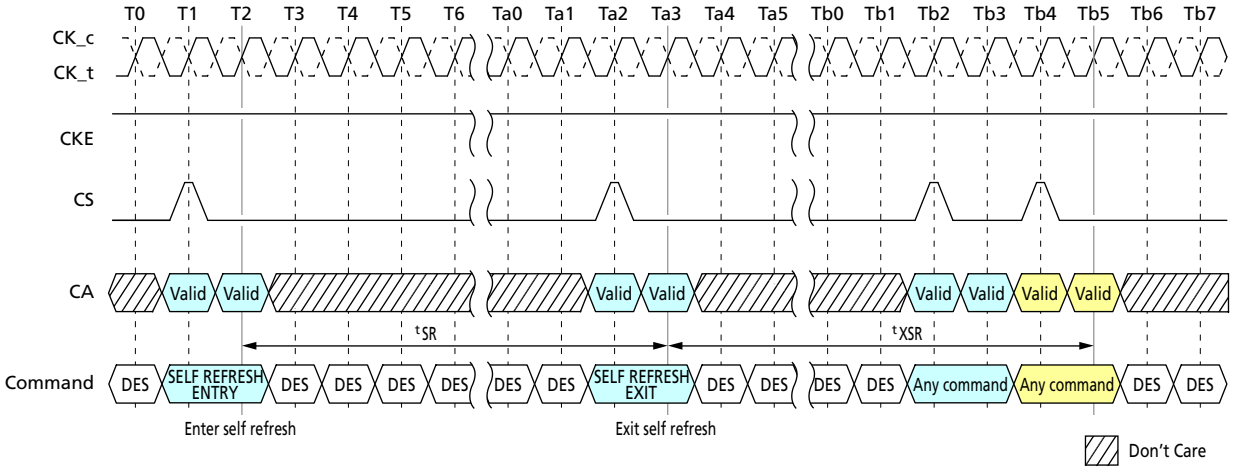
The device can operate in self refresh mode within the standard and elevated temperature ranges. It also manages self refresh power consumption when the operating temperature changes: lower at low temperatures and higher at high temperatures.

For proper SELF REFRESH operation, power supply pins (V_{DD1}, V_{DD2}, and V_{DDQ}) must be at valid levels. V_{DDQ} can be turned off during self refresh with power-down after tCKELCK is satisfied. (Refer to the Self Refresh Entry/Exit Timing with Power-Down Entry/Exit figure.) Prior to exiting self refresh with power-down, V_{DDQ} must be within specified limits. The minimum time that the device must remain in self refresh mode is tSR(MIN). After self refresh exit is registered, only MRR-1, CAS-2, DES,

MPC, MRW-1, and MRW-2 except PASR bank/segment mask setting and SR abort setting are allowed until tXSR is satisfied.

The use of self refresh mode introduces the possibility that an internally timed refresh event can be missed when self refresh exit is registered. Upon exit from self refresh, it is required that at least one REFRESH command (8 per-bank or 1 all-bank) is issued before entry into a subsequent self refresh. This REFRESH command is not included in the count of regular REFRESH commands required by the tREFI interval, and does not modify the postponed or pulled-in refresh counts; the REFRESH command does count toward the maximum refreshes permitted within 2 × tREFI.

Figure 159: Self Refresh Entry/Exit Timing

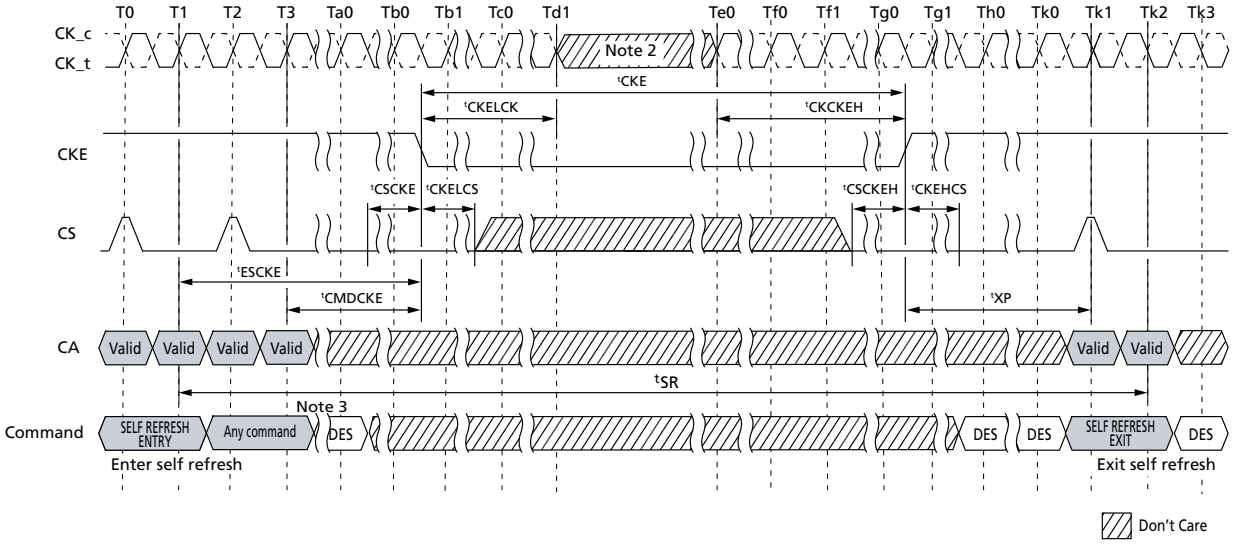


Notes: 1. MRR-1, CAS-2, DES, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment mask setting and SR abort setting) are allowed during self refresh.
2. DES commands are shown for ease of illustration; other commands may be valid at these times.

Power-Down Entry and Exit During Self Refresh

Entering/exiting power-down mode is allowed during self refresh mode. The related timing parameters between self refresh entry/exit and power-down entry/exit are shown below.

Figure 160: Self Refresh Entry/Exit Timing with Power-Down Entry/Exit

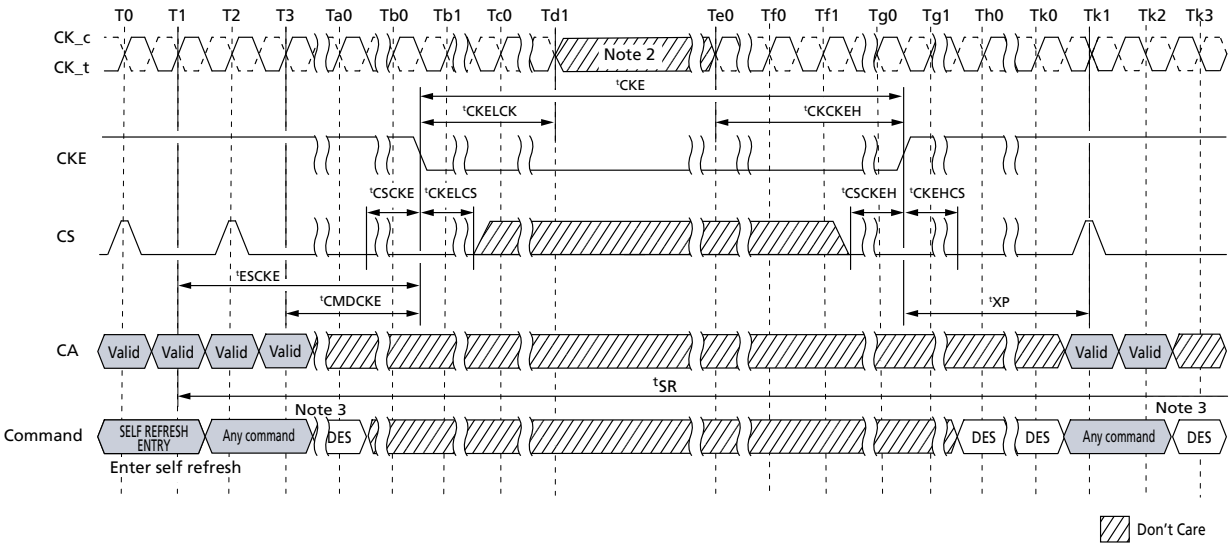


Notes: 1. MRR-1, CAS-2, DES, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment mask setting and SR abort setting) are allowed during self refresh.
2. Input clock frequency can be changed, or the input clock can be stopped, or floated after tCKELCK satisfied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCKEH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
3. Two clock command for example.

Command Input Timing After Power-Down Exit

Command input timings after power-down exit during self refresh mode are shown below.

Figure 161: Command Input Timings after Power-Down Exit During Self Refresh



Notes: 1. MRR-1, CAS-2, DES, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment setting) are allowed during self refresh.
2. Input clock frequency can be changed or the input clock can be stopped or floated after tCKELCK satisfied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCKEH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
3. Two clock command for example.

Self Refresh Abort

If MR4 OP[3] is enabled, the device aborts any ongoing refresh during self refresh exit and does not increment the internal refresh counter. The controller can issue a valid command after a delay of tXSR_abort instead of tXSR.

The value of tXSR_abort(MIN) is defined as tRFCpb + 17.5ns.

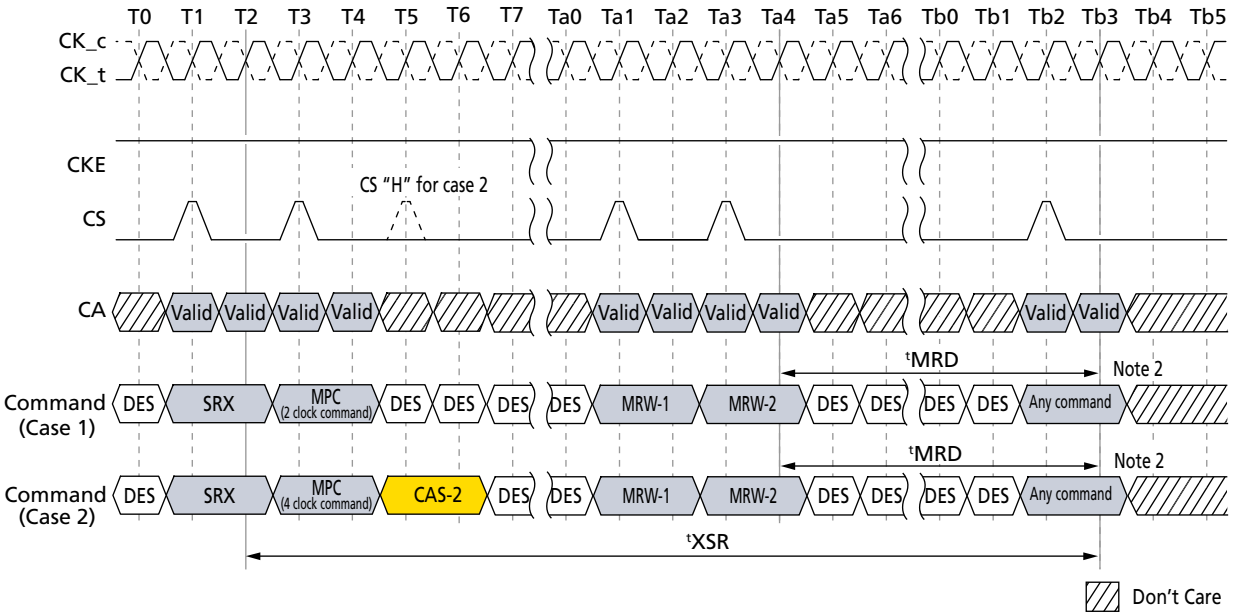
Upon exit from self refresh mode, the device requires a minimum of one extra refresh (eight per bank or one for the entire bank) before entering a subsequent self refresh mode. This requirement remains the same irrespective of the setting of the MR bit for self refresh abort.

Self refresh abort feature is valid for 6Gb density per channel and larger densities only.

MRR, MRW, MPC Commands During tXSR, tRFC

MODE REGISTER READ (MRR), MULTI PURPOSE (MPC), and MODE REGISTER WRITE (MRW) command except PASR bank/segment mask setting and SR abort setting can be issued during tXSR period.

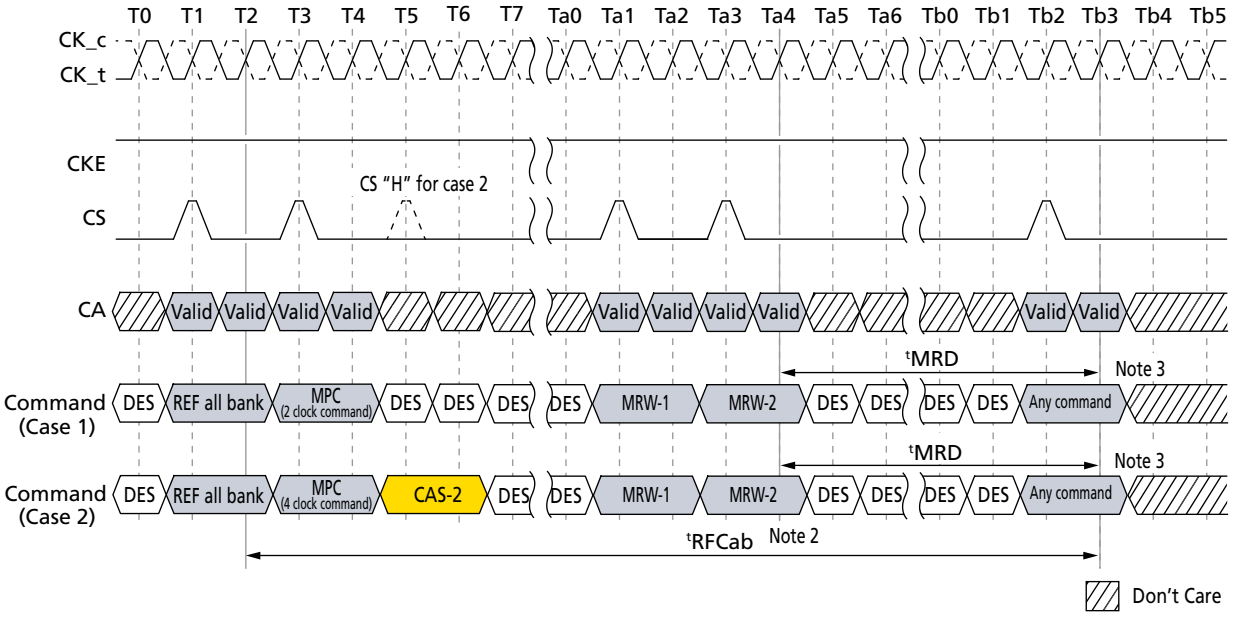
Figure 162: MRR, MRW, and MPC Commands Issuing Timing During tXSR



Notes: 1. MPC and MRW commands are shown. Any combination of MRR, MRW, and MPC is allowed during tXSR period.
2. "Any command" includes MRR, MRW, and all MPC commands.

MRR, MRW, and MPC can be issued during tRFC period.

Figure 163: MRR, MRW, and MPC Commands Issuing Timing During tRFC



Notes: 1. MPC and MRW commands are shown. Any combination of MRR, MRW, and MPC is allowed during tRFCab or tRFCpb period.
2. REFRESH cycle time depends on REFRESH command. In the case of per bank REFRESH command issued, REFRESH cycle time will be tRFCpb.
3. "Any command" includes MRR, MRW, and all MPC commands.

Power-Down Mode

Power-Down Entry and Exit

Power-down is asynchronously entered when CKE is driven LOW. CKE must not go LOW while the following operations are in progress:

- Mode register read
- Mode register write
- Read
- Write
- $V_{REF(CA)}$ range and value setting via MRW
- $V_{REF(DQ)}$ range and value setting via MRW
- Command bus training mode entering/exiting via MRW
- VRCG HIGH current mode entering/exiting via MRW

CKE can go LOW while any other operations such as row activation, precharge, auto precharge, or refresh are in progress. The power-down I_{DD} specification will not be applied until such operations are complete. Power-down entry and exit are shown below.

Entering power-down deactivates the input and output buffers, excluding CKE and RESET_n. To ensure that there is enough time to account for internal delay on the CKE signal path, CS input is required stable LOW level and CA input level is "Don't Care" after CKE is driven LOW, this timing period is defined as ^{t}CKELCS. Clock input is required after CKE is driven LOW, this timing period is defined as ^{t}CKELCK. CKE LOW will result in deactivation of all input receivers except RESET_n after ^{t}CKELCK has expired. In power-down mode, CKE must be held LOW; all other input signals except RESET_n are "Don't Care." CKE LOW must be maintained until ^{t}CKE(MIN) is satisfied.

V_{DDQ} can be turned off during power-down after ^{t}CKELCK is satisfied. Prior to exiting power-down, V_{DDQ} must be within its minimum/maximum operating range. No REFRESH operations are performed in power-down mode except self refresh power-down. The maximum duration in non-self-refresh power-down mode is only limited by the refresh requirements outlined in the REFRESH command section.

The power-down state is asynchronously exited when CKE is driven HIGH. CKE HIGH must be maintained until ^{t}CKE(MIN) is satisfied. A valid, executable command can be applied with power-down exit latency ^{t}XP after CKE goes HIGH. Power-down exit latency is defined in the AC timing parameter table.

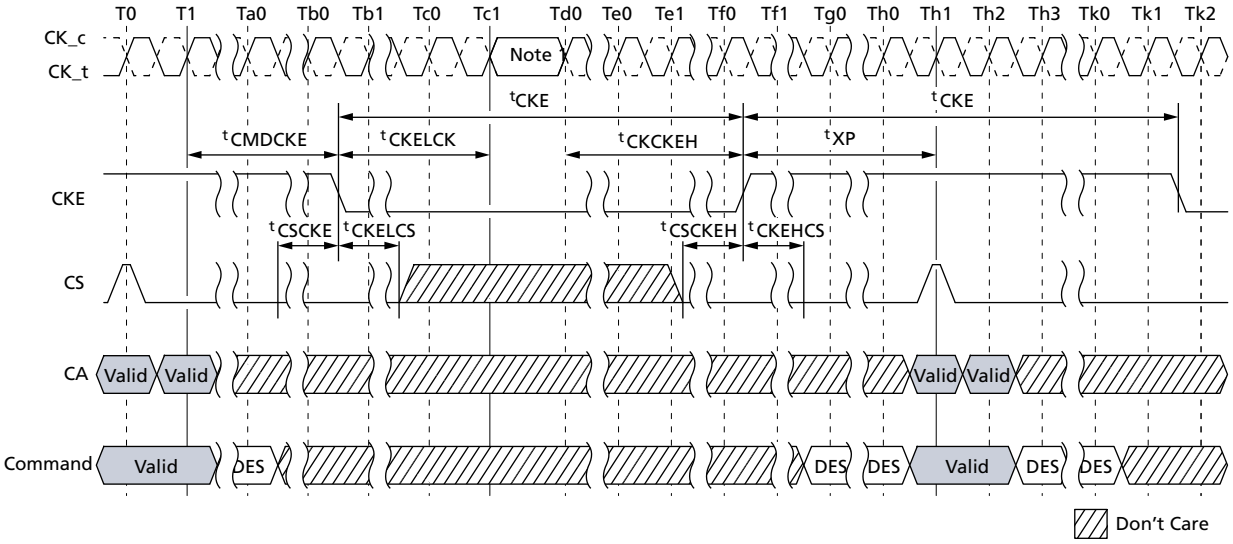
Clock frequency change or clock stop is inhibited during ^{t}CMDCKE, ^{t}CKELCK, ^{t}CKCKEH, ^{t}XP, ^{t}MRWCKEL, and ^{t}ZQCKE periods.

If power-down occurs when all banks are idle, this mode is referred to as idle power-down. if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. And If power-down occurs when self refresh is in progress, this mode is referred to as self refresh power-down in which the internal refresh is continuing in the same way as self refresh mode.

When CA, CK, and/or CS ODT is enabled via MR11 OP[6:4] and also via MR22 or CA-ODT pad setting, the rank providing ODT will continue to terminate the command bus in all DRAM states including power-down when V_{DDQ} is stable and within its minimum/maximum operating range.

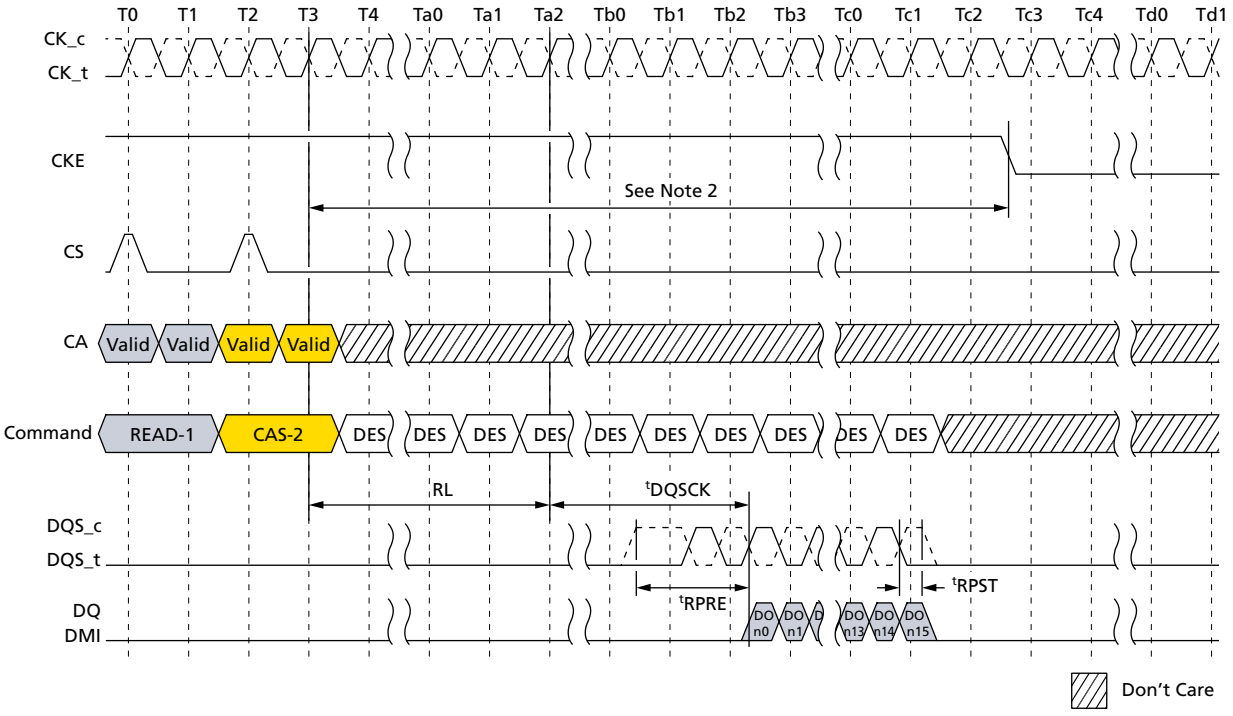
The LPDDR4 DRAM cannot be placed in power-down state during start DQS interval oscillator operation.

Figure 164: Basic Power-Down Entry and Exit Timing



Note: 1. Input clock frequency can be changed or the input clock can be stopped or floated during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of ^{t}CKCKEH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

Figure 165: Read and Read with Auto Precharge to Power-Down Entry



Notes: 1. CKE must be held HIGH until the end of the burst operation.

2. Minimum delay time from READ command or READ with AUTO PRECHARGE command to falling edge of CKE signal is as follows:

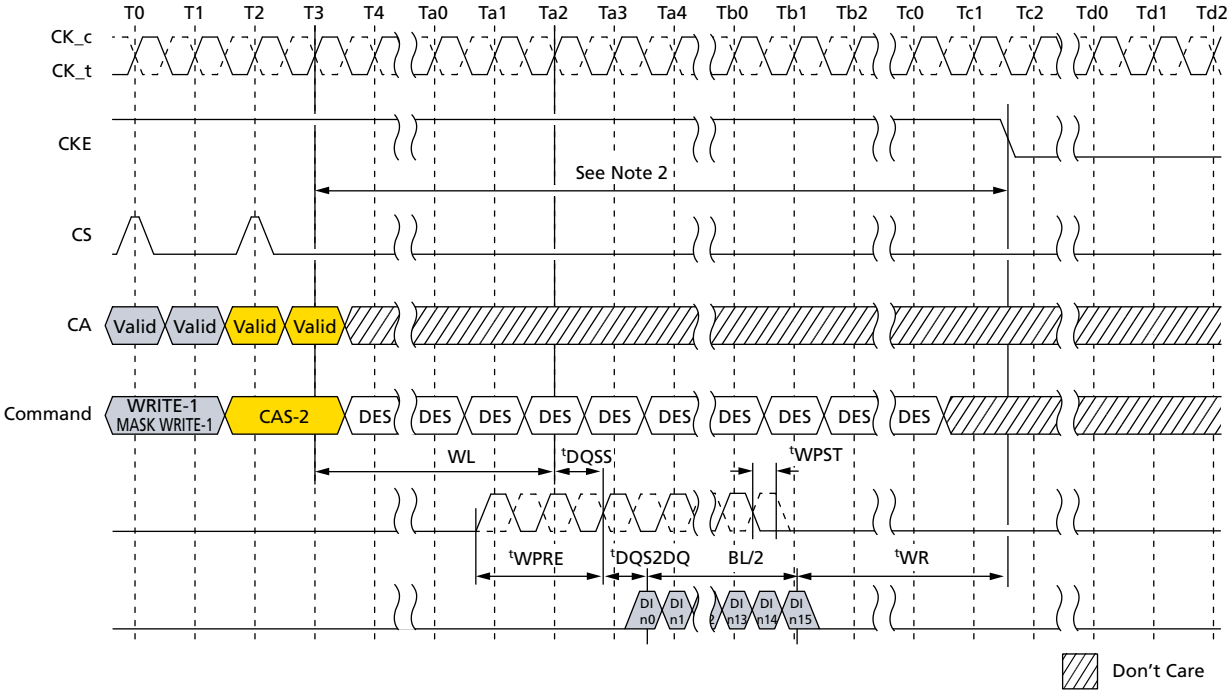
   When read postamble = 0.5*n*CK (MR1 OP[7] = [0]),

   (RL × ^{t}CK) + ^{t}DQSCK(MAX) + ((BL/2) × ^{t}CK) + 1^{t}CK

When read postamble = 1.5*n*CK (MR1 OP[7] = [1]),

(RL × ^{t}CK) + ^{t}DQSCK(MAX) + ((BL/2) × ^{t}CK) + 2^{t}CK

Figure 166: Write and Mask Write to Power-Down Entry



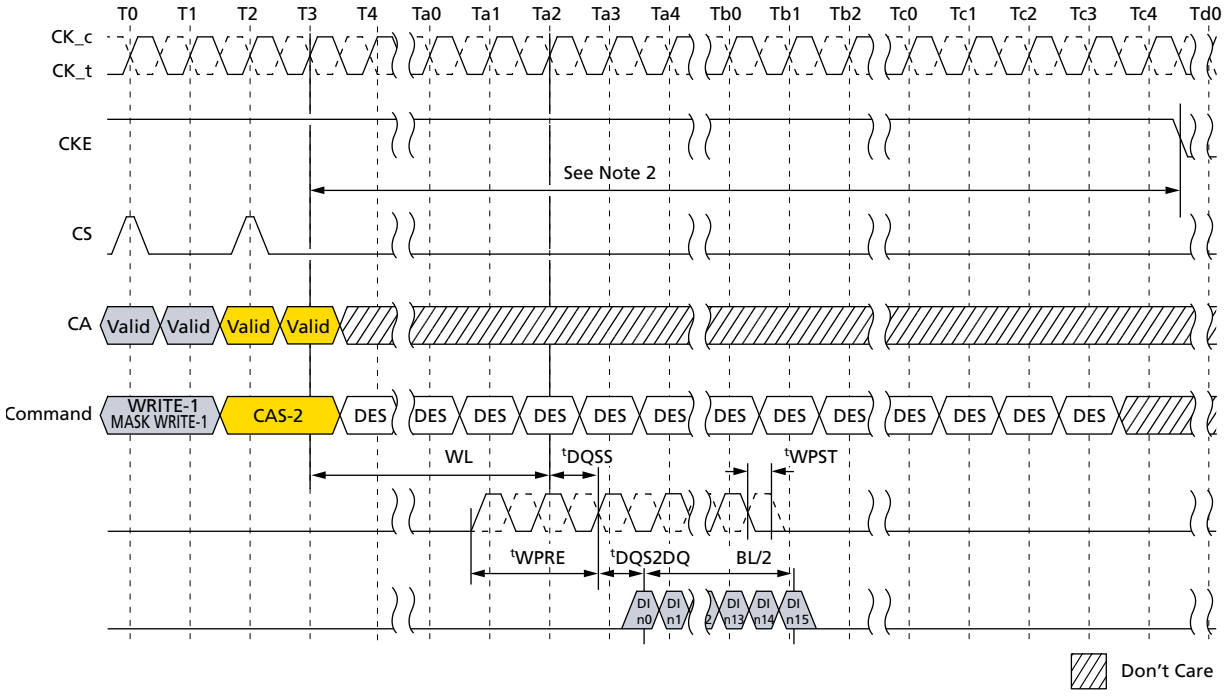
Notes: 1. CKE must be held HIGH until the end of the burst operation.

2. Minimum delay time from WRITE command or MASK WRITE command to falling edge of CKE signal is as follows:

   (WL × ^{t}CK) + ^{t}DQSS(MAX) + ^{t}DQS2DQ(MAX) + ((BL/2) × ^{t}CK) + ^{t}WR

3. This timing is applied regardless of DQ ODT disable/enable setting: MR11 OP[2:0].
4. This timing diagram only applies to the WRITE and MASK WRITE commands without auto precharge.

Figure 167: Write With Auto Precharge and Mask Write With Auto Precharge to Power-Down Entry

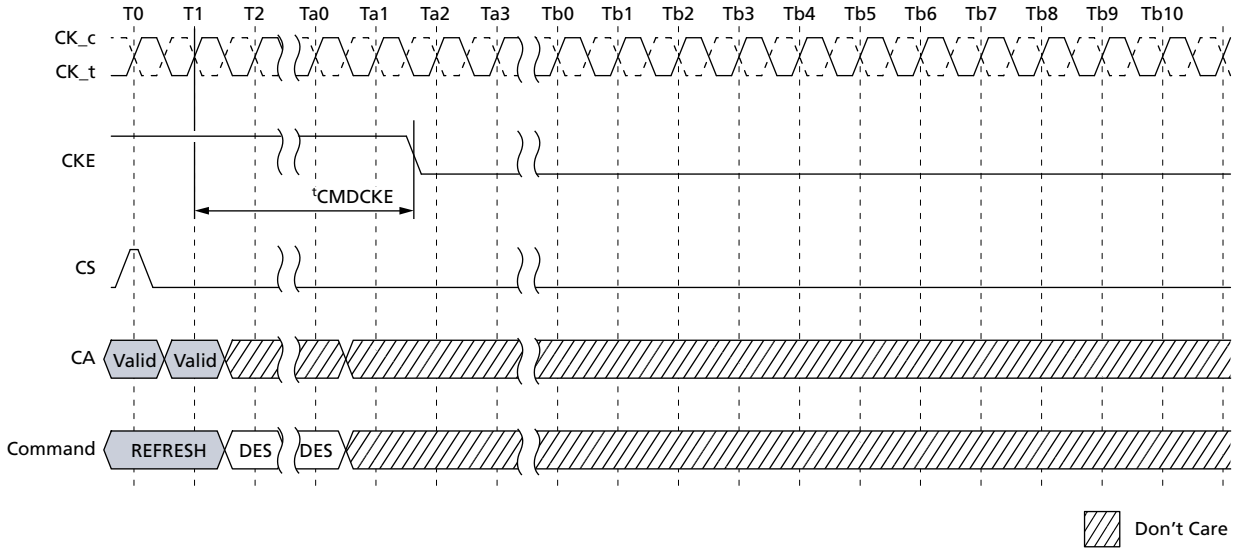


Notes: 1. CKE must be held HIGH until the end of the burst operation.

2. Delay time from WRITE with AUTO PRECHARGE command or MASK WRITE with AUTO PRECHARGE command to falling edge of CKE signal is more than
(WL × ^{t}CK) + ^{t}DQSS(MAX) + ^{t}DQS2DQ(MAX) + ((BL/2) × ^{t}CK) + (*n*WR × ^{t}CK) + (2 × ^{t}CK)

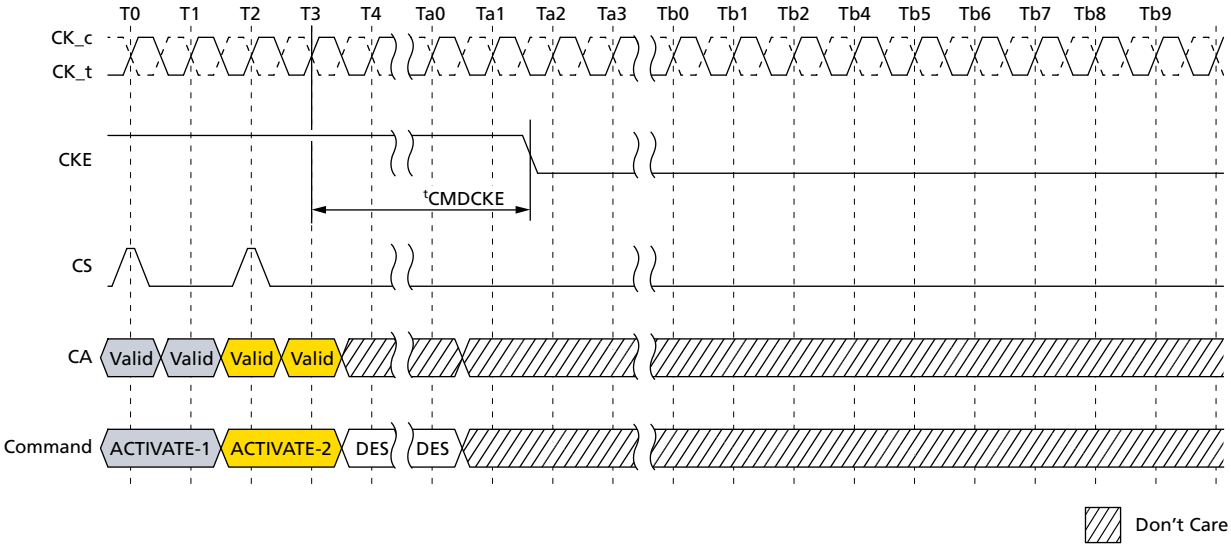
3. This timing is applied regardless of DQ ODT disable/enable setting: MR11 OP[2:0].

Figure 168: Refresh Entry to Power-Down Entry



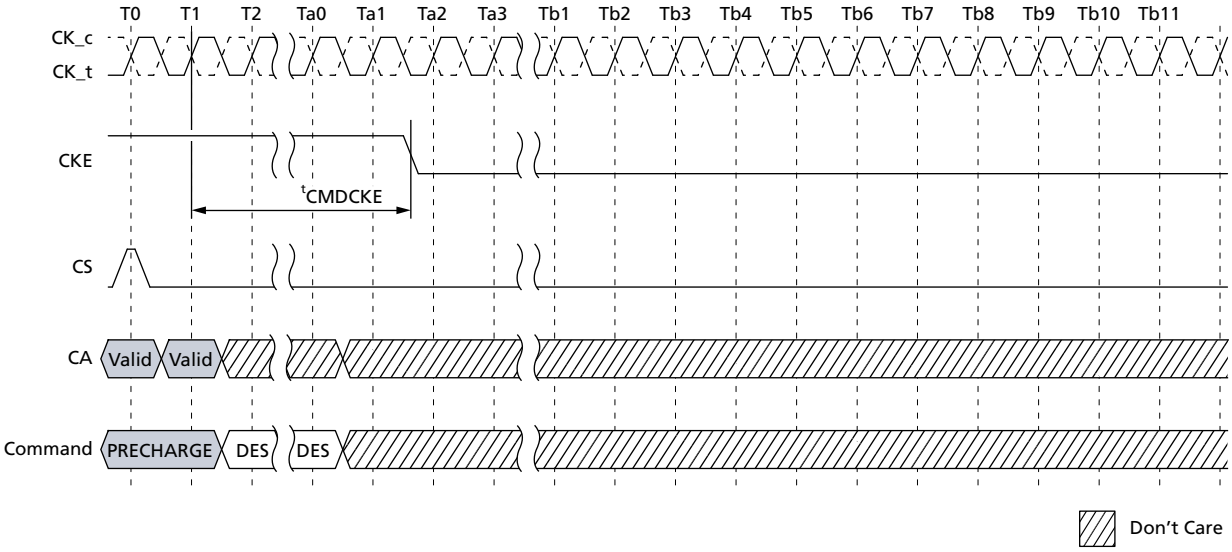
Note: 1. CKE must be held HIGH until ^{t}CMDCKE is satisfied.

Figure 169: ACTIVATE Command to Power-Down Entry



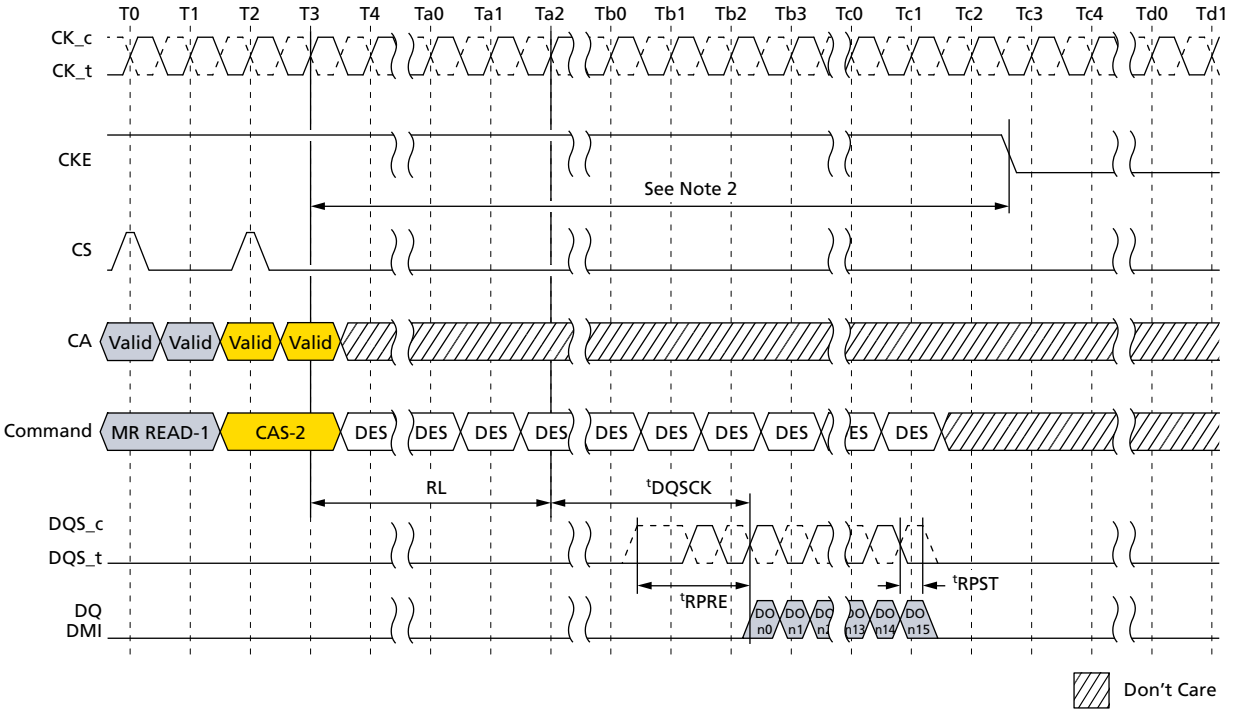
Note: 1. CKE must be held HIGH until ^{t}CMDCKE is satisfied.

Figure 170: PRECHARGE Command to Power-Down Entry



Note: 1. CKE must be held HIGH until ^{t}CMDCKE is satisfied.

Figure 171: Mode Register Read to Power-Down Entry



Notes: 1. CKE must be held HIGH until the end of the burst operation.

2. Minimum delay time from MODE REGISTER READ command to falling edge of CKE signal is as follows:

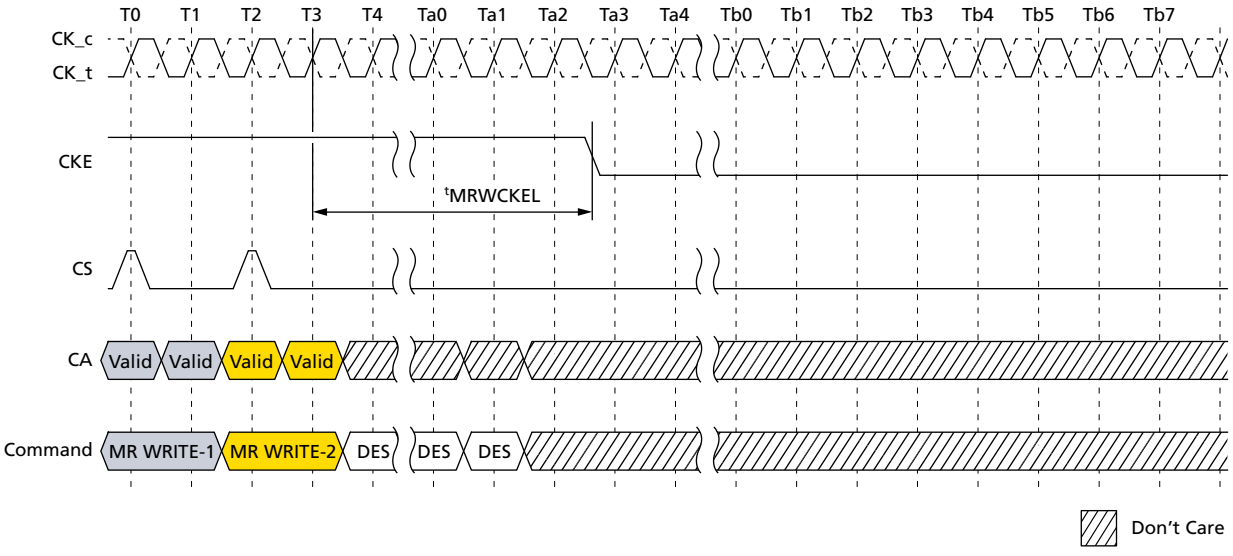
When read postamble = 0.5nCK (MR1 OP[7] = [0]),

(RL × ^{t}CK) + ^{t}DQSCK(MAX) + ((BL/2) × ^{t}CK) + 1^{t}CK

When read postamble = 1.5nCK (MR1 OP[7] = [1]),

(RL × ^{t}CK) + ^{t}DQSCK(MAX) + ((BL/2) × ^{t}CK) + 2^{t}CK

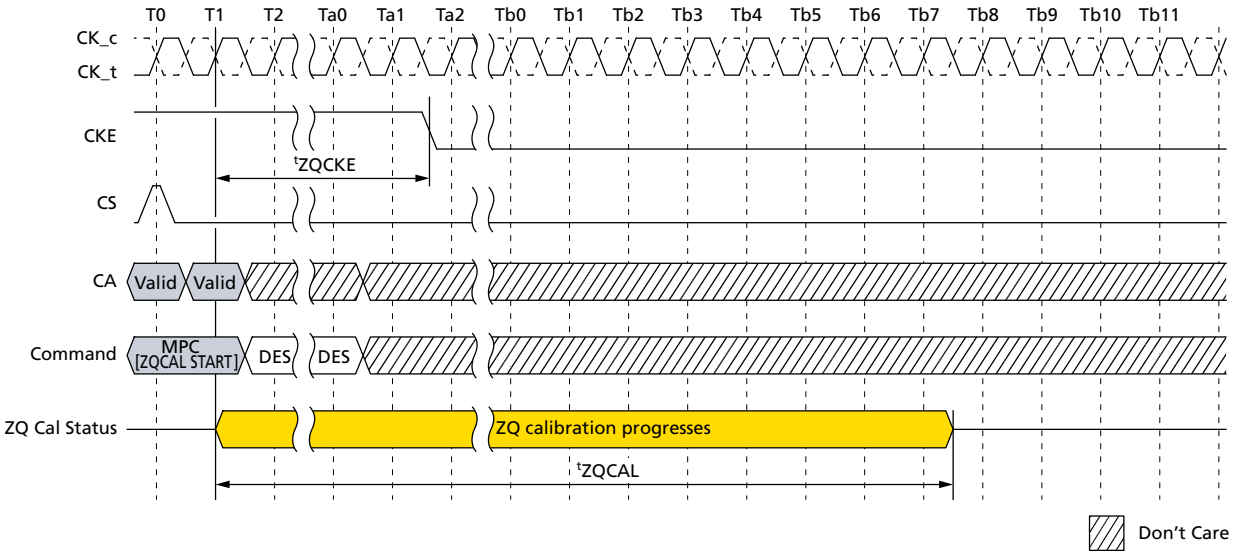
Figure 172: Mode Register Write to Power-Down Entry



Notes: 1. CKE must be held HIGH until ^{t}MRWCKEL is satisfied.

2. This timing is the general definition for power-down entry after MODE REGISTER WRITE command. When a MODE REGISTER WRITE command changes a parameter or starts an operation that requires special timing longer than tMRWCKEL, that timing must be satisfied before CKE is driven LOW. Changing the $V_{REF(DQ)}$ value is one example, in this case the appropriate tVREF-SHORT/MIDDLE/LONG must be satisfied.

Figure 173: MULTI PURPOSE Command for ZQCAL Start to Power-Down Entry



Note: 1. ZQ calibration continues if CKE goes LOW after tZQCKE is satisfied.

Input Clock Stop and Frequency Change

Clock Frequency Change – CKE LOW

During CKE LOW, the device supports input clock frequency changes under the following conditions:

- ^{t}CK(abs)min is met for each clock cycle
- Refresh requirements apply during clock frequency change
- During clock frequency change, only REFab or REFpb commands may be executing
- Any ACTIVATE or PRECHARGE commands have completed prior to changing the frequency
- Related timing conditions, ^{t}RCD and ^{t}RP, have been met prior to changing the frequency
- The initial clock frequency must be maintained for a minimum of ^{t}CKELCK after CKE goes LOW
- The clock satisfies ^{t}CH(abs) and ^{t}CL(abs) for a minimum of ^{t}CKCKEH prior to CKE going HIGH

After the input clock frequency changes and CKE is held HIGH, additional MRW commands may be required to set the WR, RL, and so forth. These settings may require adjustment to meet minimum timing requirements at the target clock frequency.

Clock Stop – CKE LOW

During CKE LOW, the device supports clock stop under the following conditions:

- CK_t and CK_c are don't care during clock stop
- Refresh requirements apply during clock stop
- During clock stop, only REFab or REFpb commands may be executing
- Any ACTIVATE or PRECHARGE commands have completed prior to stopping the clock
- Related timing conditions, ^{t}RCD and ^{t}RP, have been met prior to stopping the clock
- The initial clock frequency must be maintained for a minimum of ^{t}CKELCK after CKE goes LOW
- The clock satisfies ^{t}CH(abs) and ^{t}CL(abs) for a minimum of ^{t}CKCKEH prior to CKE going HIGH

Clock Frequency Change – CKE HIGH

During CKE HIGH, the device supports input clock frequency change under the following conditions:

- ^{t}CK(abs)min is met for each clock cycle
- Refresh requirements apply during clock frequency change
- During clock frequency change, only REFab or REFpb commands may be executing
- Any ACTIVATE, READ, WRITE, PRECHARGE, MODE REGISTER WRITE, or MODE REGISTER READ commands (and any associated data bursts) have completed prior to changing the frequency
- Related timing conditions (^{t}RCD, ^{t}WR, ^{t}RP, ^{t}MRW, and ^{t}MRR) have been met prior to changing the frequency
- During clock frequency change, CS is held LOW
- The device is ready for normal operation after the clock satisfies ^{t}CH(abs) and ^{t}CL(abs) for a minimum of $2 \times {}^{t}\text{CK} + {}^{t}\text{XP}$

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL, and so forth. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

Clock Stop – CKE HIGH

During CKE HIGH, the device supports clock stop under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop
- During clock stop, CS is held LOW
- Refresh requirements apply during clock stop

- During clock stop, only REFab or REFpb commands may be executing
- Any ACTIVATE, READ, WRITE, MPC (WRITE-FIFO, READ-FIFO, READ DQ CALIBRATION), PRECHARGE, MODE REGISTER WRITE, or MODE REGISTER READ commands have completed, including any associated data bursts and extra 4 clock cycles must be provided prior to stopping the clock
- Related timing conditions (^{t}RCD, ^{t}WR, ^{t}RP, ^{t}MRW, ^{t}MRR, ^{t}ZQLAT, and so forth) have been met prior to stopping the clock
- READ with AUTO PRECHARGE and WRITE with AUTO PRECHARGE commands need extra 4 clock cycles in addition to the related timing constraints, nWR and nRTP, to complete the operations
- REFab, REFpb, SRE, SRX, and MPC[ZQCAL START] commands are required to have extra 4 clock cycles prior to stopping the clock
- The device is ready for normal operation after the clock is restarted and satisfies ^{t}CH(abs) and ^{t}CL(abs) for a minimum of 2 × ^{t}CK + ^{t}XP

MODE REGISTER READ Operation

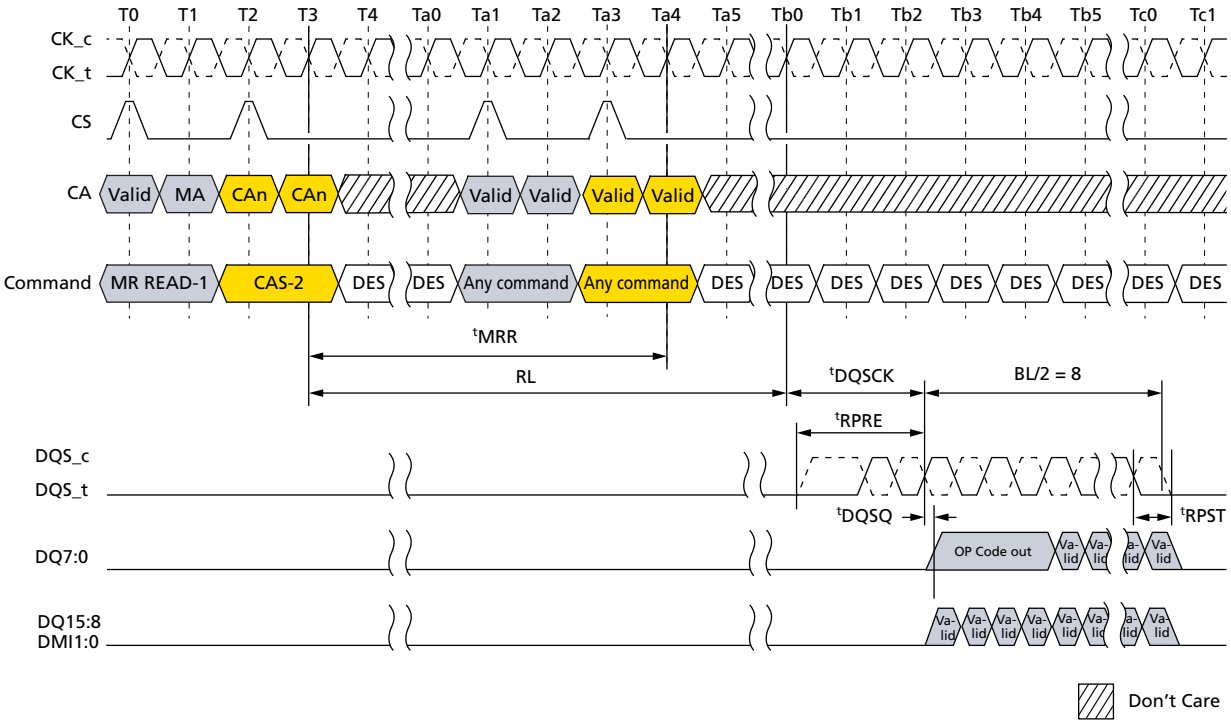
The MODE REGISTER READ (MRR) command is used to read configuration and status data from the device registers. The MRR command is initiated with CS and CA[5:0] in the proper state as defined by the Command Truth Table. The mode register address operands (MA[5:0]) enable the user to select one of 64 registers. The mode register contents are available on the first four UI data bits of DQ[7:0] after RL × ^{t}CK + ^{t}DQSCK + ^{t}DQSQ following the MRR command. Subsequent data bits contain valid but undefined content. DQS is toggled for the duration of the MODE REGISTER READ burst. The MRR has a command burst length of 16. MRR operation must not be interrupted.

Table 154: MRR

UI	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DQ0	OP0				V											
DQ1	OP1				V											
DQ2	OP2				V											
DQ3	OP3				V											
DQ4	OP4				V											
DQ5	OP5				V											
DQ6	OP6				V											
DQ7	OP7				V											
DQ8–DQ15	V															
DMI0–DMI1	V															

Notes: 1. MRR data are extended to the first 4 UIs, allowing the LPDRAM controller to sample data easily.
2. DBI during MRR depends on mode register setting MR3 OP[6].
3. The read preamble and postamble of MRR are the same as for a normal read.

Figure 174: MODE REGISTER READ Operation

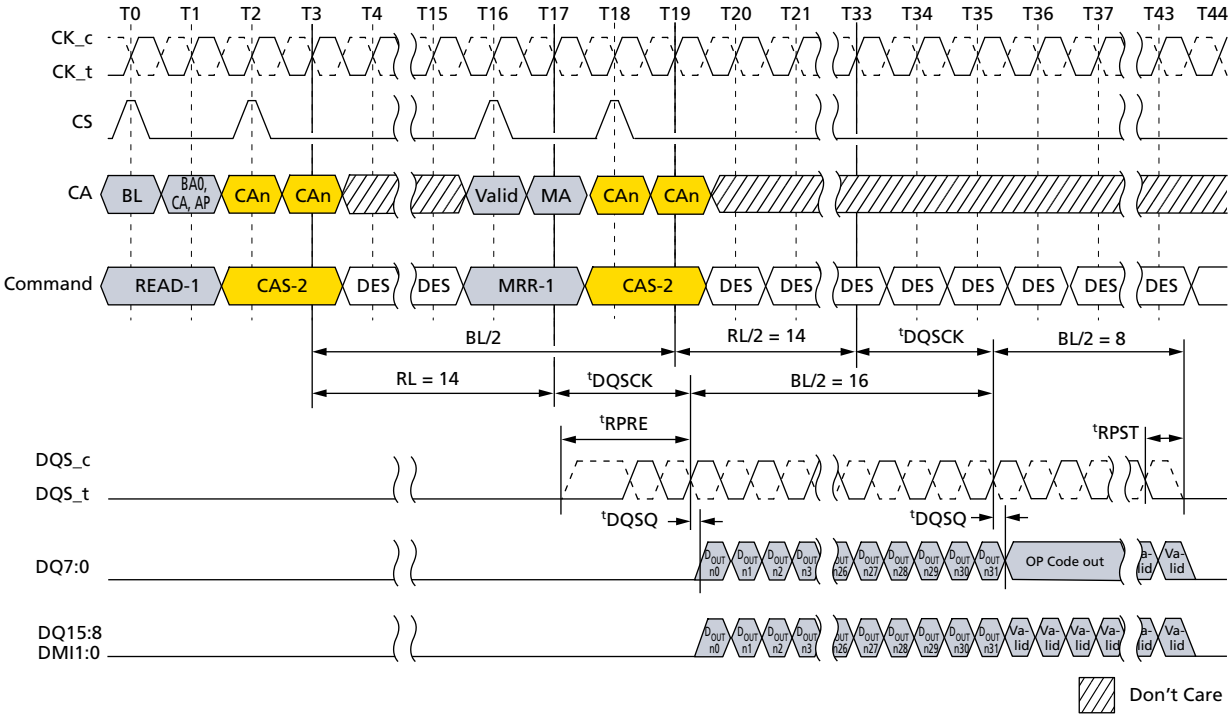


Notes: 1. Only BL = 16 is supported.
2. Only DESELECT is allowed during ^{t}MRR period.
3. There are some exceptions about issuing commands after ^{t}MRR. Refer to MRR/MRW Timing Constraints Table for detail.
4. DBI is disable mode.
5. DES commands except ^{t}MRR period are shown for ease of illustration; other commands may be valid at these times.
6. DQ/DQS: V_{SSQ} termination

MRR After a READ and WRITE Command

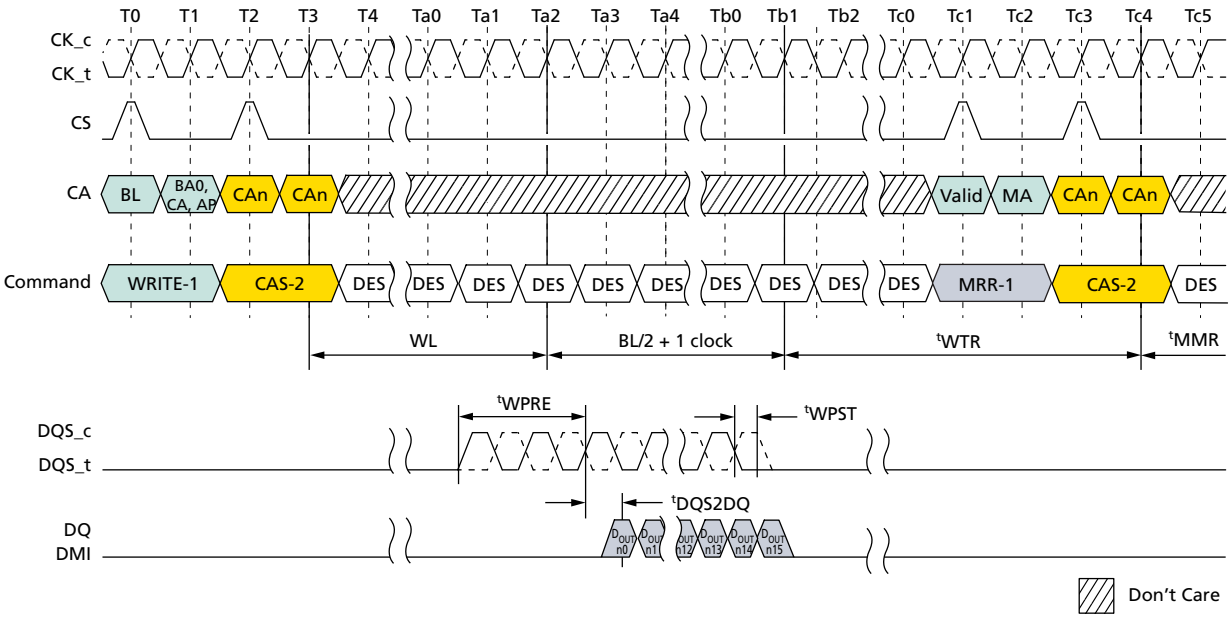
After a prior READ command, the MRR command must not be issued earlier than BL/2 clock cycles, in a similar way WL + BL/2 + 1 + RU(^{t}WTR/^{t}CK) clock cycles after a PRIOR WRITE, WRITE with AP, MASK WRITE, MASK WRITE with AP, and MPC[WRITE-FIFO] command in order to avoid the collision of READ and WRITE burst data on device internal data bus.

Figure 175: READ-to-MRR Timing



Notes: 1. The minimum number of clock cycles from the burst READ command to the MRR command is BL/2.
2. Read BL = 32, MRR BL = 16, RL = 14, Preamble = Toggle, Postamble = 0.5*n*CK, DBI = Disable, DQ/DQS: V_{SSQ} termination.
3. D_{OUT} *n* = data-out to column *n*.
4. DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.

Figure 176: WRITE-to-MRR Timing



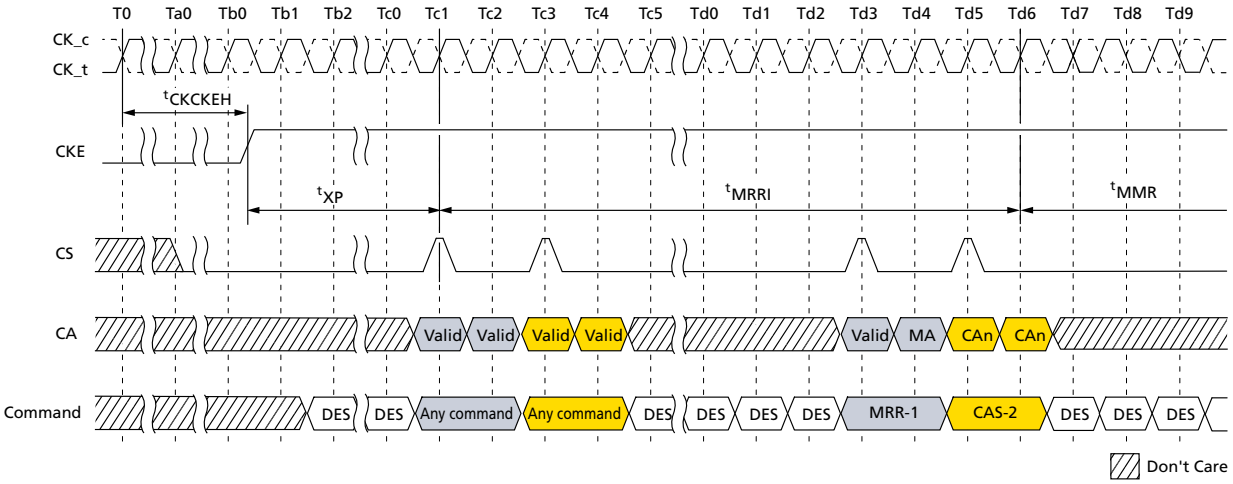
Notes: 1. Write BL = 16, Write postamble = 0.5*n*CK, DQ/DQS: V_{SSQ} termination.

2. Only DES is allowed during ^{t}MRR period.
3. D_{OUT} *n* = data-out to column *n*.
4. The minimum number of clock cycles from the BURST WRITE command to MRR command is WL + BL/2 + 1 + RU(^{t}WTR/^{t}CK).
5. ^{t}WTR starts at the rising edge of CK after the last latching edge of DQS.
6. DES commands except ^{t}MRR period are shown for ease of illustration; other commands may be valid at these times.

MRR After Power-Down Exit

Following the power-down state, an additional time, ^{t}MRRI, is required prior to issuing the MODE REGISTER READ (MRR) command. This additional time (equivalent to ^{t}RCD) is required in order to maximize power-down current savings by allowing more power-up time for the MRR data path after exit from power-down mode.

Figure 177: MRR Following Power-Down

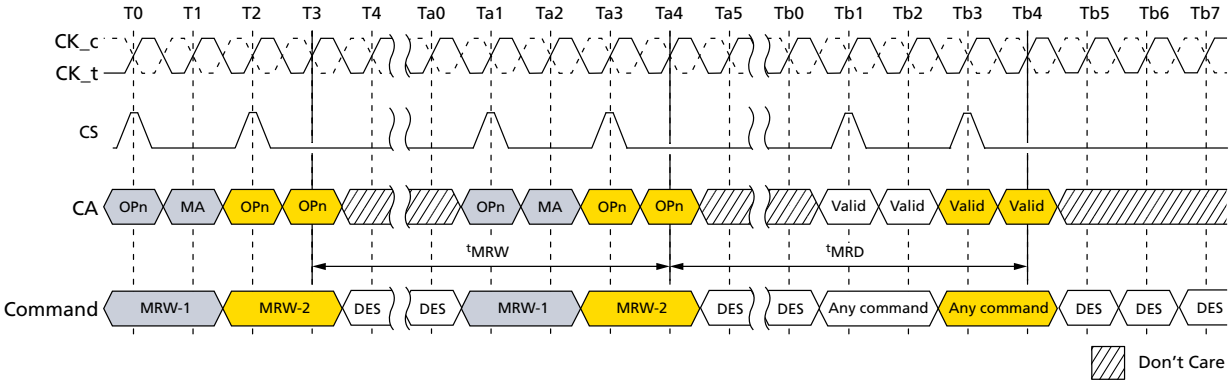


Notes: 1. Only DES is allowed during ^{t}MRR period.
2. DES commands except ^{t}MRR period are shown for ease of illustration; other commands may be valid at these times.

MODE REGISTER WRITE

The MODE REGISTER WRITE (MRW) writes configuration data to the mode registers. The MRW command is initiated with CKE, CS, and CA[5:0] to valid levels at the rising edge of the clock. The mode register address and the data written to it is contained in CA[5:0] according to the Command Truth Table. The MRW command period is defined by ^{t}MRW. Mode register WRITEs to read-only registers have no impact on the functionality of the device.

Figure 178: MODE REGISTER WRITE Timing



Mode Register Write States

MRW can be issued from either a bank-idle or a bank-active state. Certain restrictions may apply for MRW from an active state.

Table 155: Truth Table for MRR and MRW

Current State	Command	Intermediate State	Next State
All banks idle	MRR	Reading mode register, all banks idle	All banks idle
	MRW	Writing mode register, all banks idle	All banks idle
Bank(s) active	MRR	Reading mode register	Bank(s) active
	MRW	Writing mode register	Bank(s) active

Table 156: MRR/MRW Timing Constraints: DQ ODT is Disable

From Command	To Command	Minimum Delay Between "From Command" and "To Command"	Unit	Notes
MRR	MRR	^{t}MRR	–	
	RD/RDA	^{t}MRR	–	
	WR/WRA/MWR/MWRA	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 -WL + ^{t}WPRE + RD(^{t}RPST)	*n*CK	
	MRW	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 + 3	*n*CK	
RD/RDA	MRR	BL/2	*n*CK	
WR/WRA/MWR/MWRA		WL + 1 + BL/2 + RU(^{t}WTR/^{t}CK)	*n*CK	
MRW		^{t}MRD	–	
POWER-DOWN EXIT		^{t}XP + ^{t}MRRI	–	
MRW	RD/RDA	^{t}MRD	–	
	WR/WRA/MWR/MWRA	^{t}MRD	–	
	MRW	^{t}MRW	–	

Table 156: MRR/MRW Timing Constraints: DQ ODT is Disable (Continued)

From Command	To Command	Minimum Delay Between "From Command" and "To Command"	Unit	Notes
RD/ RD-FIFO/ READ DQ CAL	MRW	RL + BL/2 + RU(^{t}DQSCK(MAX)/^{t}CK) + RD(^{t}RPST) + MAX(RU(7.5ns/^{t}CK), 8*n*CK)	*n*CK	
RD with AUTO PRECHARGE		RL + BL/2 + RU(^{t}DQSCK(MAX)/^{t}CK) + RD(^{t}RPST) + MAX(RU(7.5ns/^{t}CK), 8*n*CK) + *n*RTP - 8	*n*CK	
WR/ MWR/ WR-FIFO		WL + 1 + BL/2 + MAX(RU(7.5ns/^{t}CK), 8*n*CK)	*n*CK	
WR/MWR with AUTO PRECHARGE		WL + 1 + BL/2 + MAX(RU(7.5ns/^{t}CK), 8*n*CK) + *n*WR	*n*CK	

Table 157: MRR/MRW Timing Constraints: DQ ODT is Enable

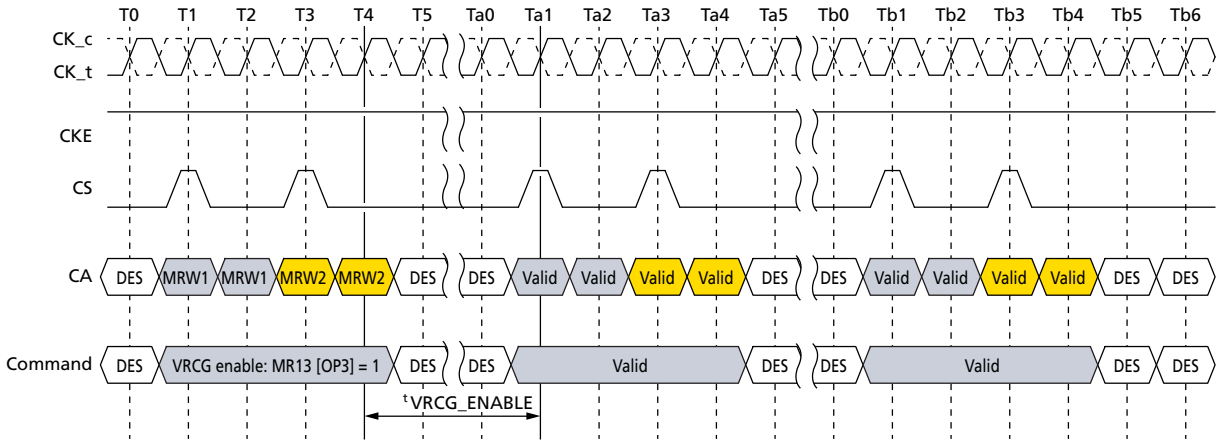
From Command	To Command	Minimum Delay Between "From Command" and "To Command"	Unit	Notes
MRR	MRR	^{t}MRR	–	
	RD/RDA	^{t}MRR	–	
	WR/WRA/MWR/MWRA	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 - ODTLon - RD(^{t}ODTon(MIN)/^{t}CK) + RD(^{t}RPST) + 1	*n*CK	
	MRW	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 + 3	*n*CK	
RD/RDA	MRR	BL/2	*n*CK	
WR/WRA/MWR/ MWRA		WL + 1 + BL/2 + RU(^{t}WTR/^{t}CK)	*n*CK	
MRW		^{t}MRD	–	
POWER-DOWN EXIT		^{t}XP + ^{t}MRRI	–	
MRW	RD/RDA	^{t}MRD	–	
	WR/WRA/MWR/MWRA	^{t}MRD	–	
	MRW	^{t}MRW	–	
RD/ RD-FIFO/ READ DQ CAL	MRW	RL + BL/2 + RU(^{t}DQSCK(MAX)/^{t}CK) + RD(^{t}RPST) + MAX(RU(7.5ns/^{t}CK), 8*n*CK)	*n*CK	
RD with AUTO PRECHARGE		RL + BL/2 + RU(^{t}DQSCK(MAX)/^{t}CK) + RD(^{t}RPST) + MAX(RU(7.5ns/^{t}CK), 8*n*CK) + *n*RTP - 8	*n*CK	
WR/ MWR/ WR-FIFO		WL + 1 + BL/2 + MAX(RU(7.5ns/^{t}CK), 8*n*CK)	*n*CK	
WR/MWR with AUTO PRECHARGE		WL + 1 + BL/2 + MAX(RU(7.5ns/^{t}CK), 8*n*CK) + *n*WR	*n*CK	

V_{REF} Current Generator (VRCG)

LPDDR4 SDRAM V_{REF} current generators (VRCG) incorporate a high current mode to reduce the settling time of the internal $V_{REF(DQ)}$and $V_{REF(CA)}$ levels during training and when changing frequency set points during operation. The high current mode is enabled by setting MR13[OP3] = 1. Only

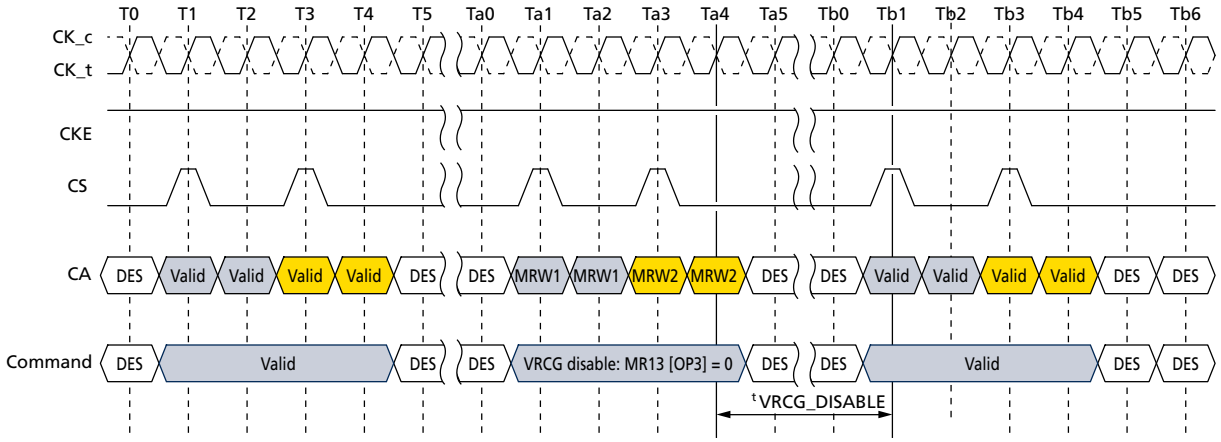
DESELECT commands may be issued until ^{t}VRCG_ENABLE is satisfied. ^{t}VRCG_ENABLE timing is shown below.

Figure 179: VRCG Enable Timing



VRCG high current mode is disabled by setting MR13[OP3] = 0. Only DESELECT commands may be issued until ^{t}VRCG_DISABLE is satisfied. ^{t}VRCG_DISABLE timing is shown below.

Figure 180: VRCG Disable Timing



Note that LPDDR4 SDRAM devices support $V_{FER(CA)}$ and $V_{REF(DQ)}$ range and value changes without enabling VRCG high current mode.

Table 158: VRCG Enable/Disable Timing

Parameter	Symbol	Min	Max	Unit
V_{REF} high current mode enable time	^{t}VRCG_ENABLE	–	200	ns
V_{REF} high current mode disable time	^{t}VRCG_DISABLE	–	100	ns

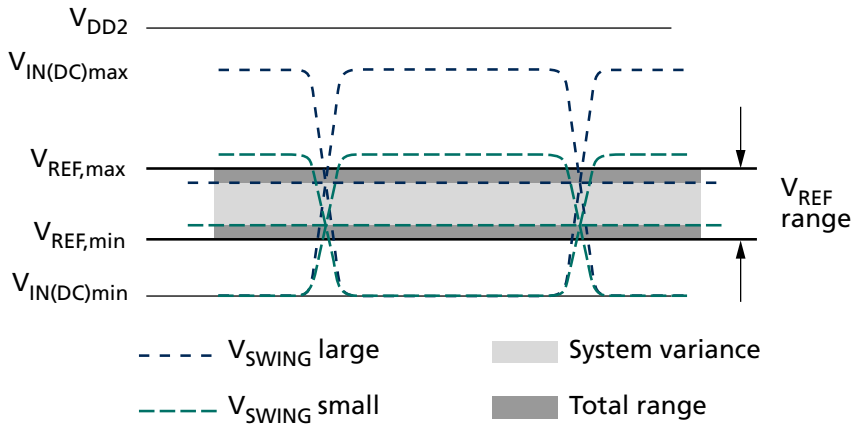
V_{REF} Training

$V_{REF(CA)}$ Training

The device's internal $V_{REF(CA)}$ specification parameters are operating voltage range, step size, V_{REF} step time, V_{REF} full-range step time, and V_{REF} valid level.

The voltage operating range specifies the minimum required V_{REF} setting range for LPDDR4 devices. The minimum range is defined by $V_{REF,max}$ and $V_{REF,min}$.

Figure 181: V_{REF} Operating Range ($V_{REF,max}$, $V_{REF,min}$)

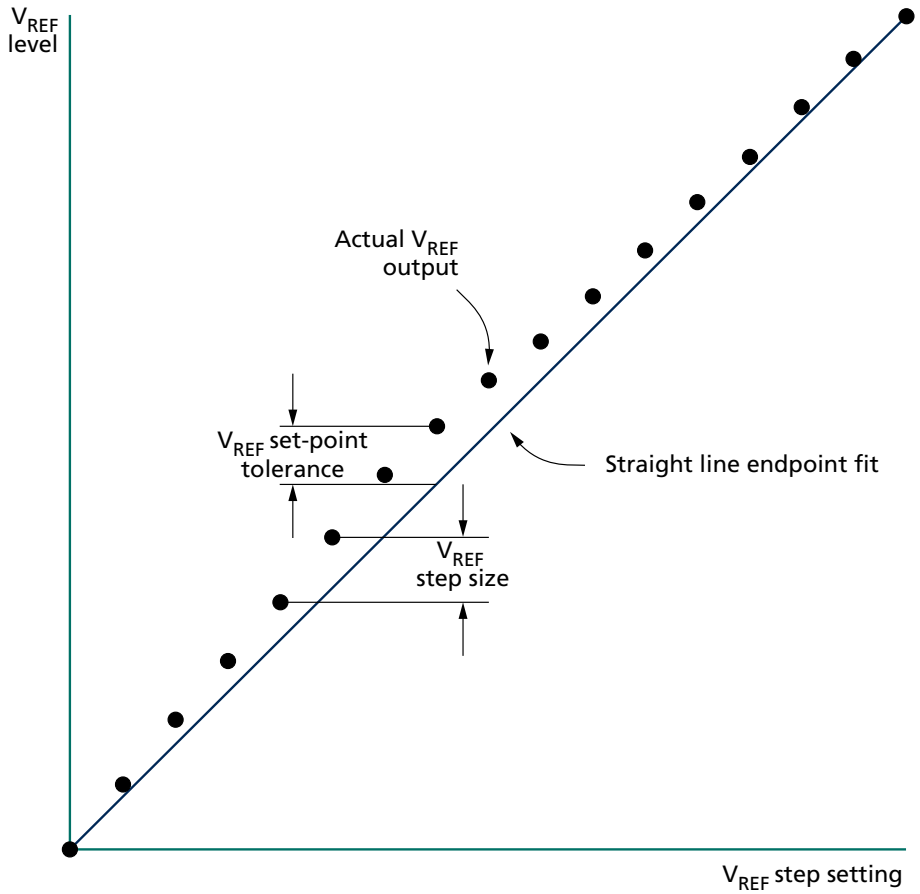


The V_{REF} step size is defined as the step size between adjacent steps. However, for a given design, the device has one value for V_{REF} step size that falls within the given range.

The V_{REF} set tolerance is the variation in the V_{REF} voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for V_{REF} set tolerance uncertainty. The range of V_{REF} set tolerance uncertainty is a function of the number of steps *n*.

The V_{REF} set tolerance is measured with respect to the ideal line that is based on the two endpoints, where the endpoints are at the minimum and maximum V_{REF} values for a specified range.

Figure 182: V_{REF} Set-Point Tolerance and Step Size



The V_{REF} increment/decrement step times are defined by ${}^{t}V_{REF}$_TIME-SHORT, ${}^{t}V_{REF}$_TIME-MIDDLE, and ${}^{t}V_{REF}$_TIME-LONG. The parameters are defined from TS to TE as shown below, where TE is referenced to when the V_{REF} voltage is at the final DC level within the V_{REF} valid tolerance (V_{REF,val_tol}).

The V_{REF} valid level is defined by V_{REF,val_tol} to qualify the step time TE (see the following figures). This parameter is used to ensure an adequate RC time constant behavior of the voltage level change after any V_{REF} increment/decrement adjustment. This parameter is only applicable for LPDDR4 component level validation/characterization.

${}^{t}V_{REF}$_TIME-SHORT is for a single step size increment/decrement change in the V_{REF} voltage.

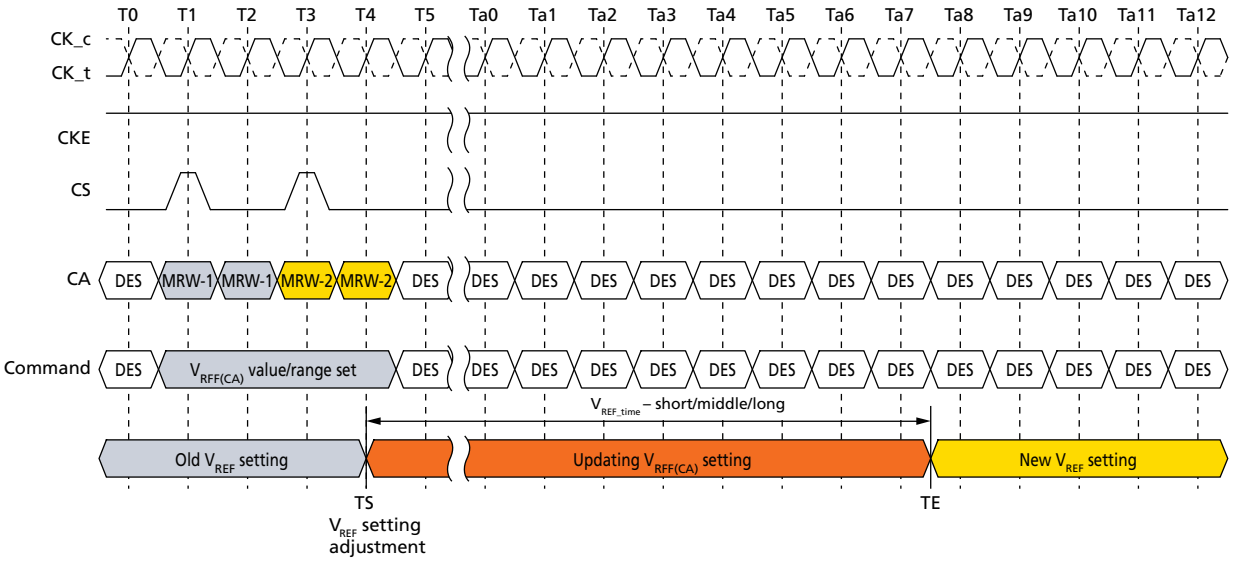
${}^{t}V_{REF}$_TIME-MIDDLE is at least two stepsizes increment/decrement change within the same $V_{REF(CA)}$ range in V_{REF} voltage.

${}^{t}V_{REF}$_TIME-LONG is the time including up to $V_{REF,min}$ to $V_{REF,max}$ or $V_{REF,max}$ to $V_{REF,min}$ change across the $V_{REF(CA)}$ range in V_{REF} voltage.

TS is referenced to MRW command clock.

TE is referenced to $V_{REF\_val\_tol}$.

Figure 183: $^{t}V_{ref}$ for Short, Middle, and Long Timing Diagram



The MRW command to the mode register bits are as follows;

MR12 OP[5:0] : $V_{REF(CA)}$ Setting

MR12 OP[6] : $V_{REF(CA)}$ Range

The minimum time required between two V_{REF} MRW commands is $^{t}V_{REF}$_TIME-SHORT for a single step and $^{t}V_{REF}$_TIME-MIDDLE for a full voltage range step.

Figure 184: $V_{REF(CA)}$ Single-Step Increment

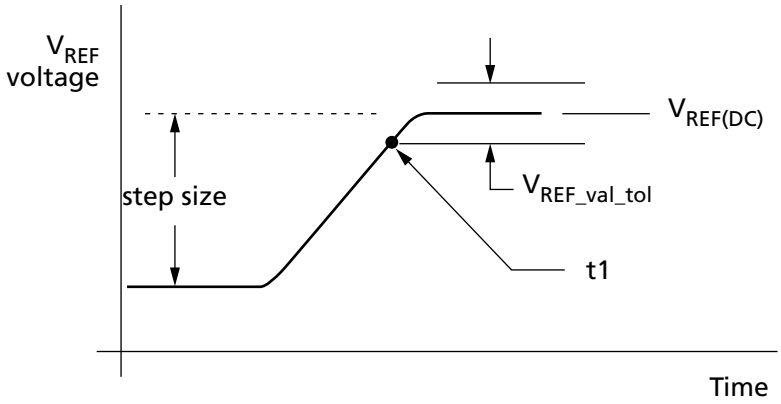


Figure 185: $V_{REF(CA)}$ Single-Step Decrement

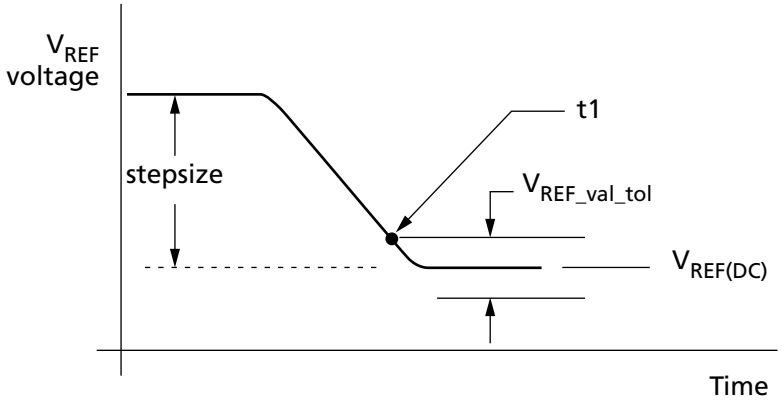


Figure 186: $V_{REF(CA)}$ Full Step from $V_{REF,min}$ to $V_{REF,max}$

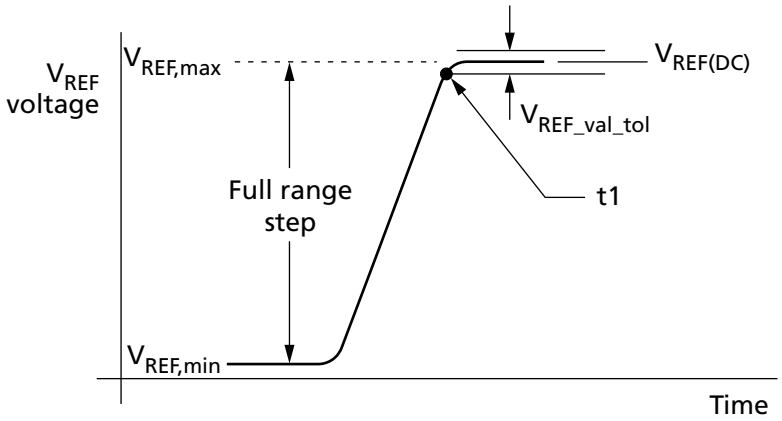
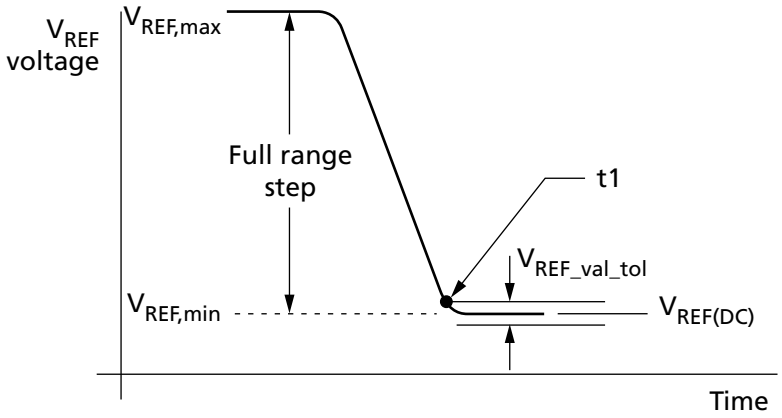


Figure 187: $V_{REF(CA)}$ Full Step from $V_{REF,max}$ to $V_{REF,min}$



The following table contains the CA internal V_{REF} specification that will be characterized at the component level for compliance.

Table 159: Internal $V_{REF(CA)}$ Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{REF(CA),max\_r0}$	$V_{REF(CA)}$ range-0 MAX operating point	–	–	44.9%	V_{DDQ}	1, 11

Table 159: Internal $V_{REF(CA)}$ Specifications (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{REF(CA),min\_r0}$	$V_{REF(CA)}$ range-0 MIN operating point	15.0%	–	–	V_{DDQ}	1, 11
$V_{REF(CA),max\_r1}$	$V_{REF(CA)}$ range-1 MAX operating point	–	–	62.9%	V_{DDQ}	1, 11
$V_{REF(CA),min\_r1}$	$V_{REF(CA)}$ range-1 MIN operating point	32.9%	–	–	V_{DDQ}	1, 11
$V_{REF(CA),step}$	$V_{REF(CA)}$ step size	0.50%	0.60%	0.70%	V_{DDQ}	2
$V_{REF(CA),set\_tol}$	$V_{REF(CA)}$ set tolerance	–11	0	11	mV	3, 4, 6
		–1.1	0	1.1	mV	3, 5, 7
$^{t}V_{REF_}$TIME-SHORT	$V_{REF(CA)}$ step time	–	–	100	ns	8
$^{t}V_{REF_}$TIME-MIDDLE		–	–	200	ns	12
$^{t}V_{REF_}$TIME-LONG		–	–	250	ns	9
$^{t}V_{REF\_time\_weak}$		–	–	1	ms	13, 14
$V_{REF(CA)\_val\_tol}$	$V_{REF(CA)}$ valid tolerance	–0.10%	0.00%	0.10%	V_{DDQ}	10

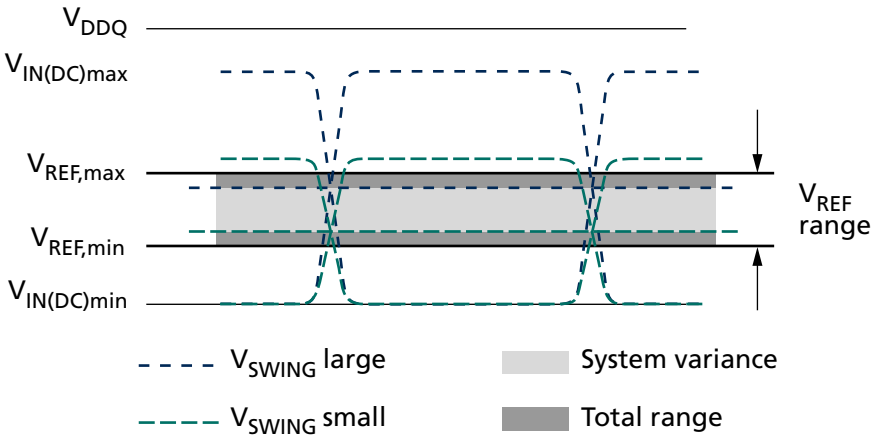
Notes: 1. $V_{REF(CA)}$ DC voltage referenced to $V_{DDQ(DC)}$.
2. $V_{REF(CA)}$ step size increment/decrement range. $V_{REF(CA)}$ at DC level.
3. $V_{REF(CA),new} = V_{REF(CA),old} + n \times V_{REF(CA),step}$; n = number of steps; if increment, use "+"; if decrement, use "–".
4. The minimum value of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new}$ - 11mV. The maximum value of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new}$ + 11mV. For n > 4.
5. The minimum value of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new}$ - 1.1mV. The maximum value of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new}$ + 1.1mV. For n ≤ 4.
6. Measured by recording the minimum and maximum values of the $V_{REF(CA)}$output over the range, drawing a straight line between those points and comparing all other $V_{REF(CA)}$ output settings to that line.
7. Measured by recording the minimum and maximum values of the $V_{REF(CA)}$ output across four consecutive steps (n = 4), drawing a straight line between those points and comparing all other $V_{REF(CA)}$ output settings to that line.
8. Time from MRW command to increment or decrement one step size for $V_{REF(CA)}$.
9. Time from MRW command to increment or decrement $V_{REF,min}$ to $V_{REF,max}$ or $V_{REF,max}$ to $V_{REF,min}$ change across the $V_{REF(CA)}$ range in V_{REF} voltage.
10. Only applicable for DRAM component level test/characterization purposes. Not applicable for normal mode of operation. V_{REF} valid is to qualify the step times which will be characterized at the component level.
11. DRAM range-0 or range-1 set by MR12 OP[6].
12. Time from MRW command to increment or decrement more than one step size up to a full range of V_{REF} voltage within the same $V_{REF(CA)}$ range.
13. Applies when VRCG high current mode is not enabled, specified by MR13 [OP3] = 0b.
14. $^{t}V_{REF_}$time_weak covers all $V_{REF(CA)}$ range and value change conditions are applied to $^{t}V_{REF_}$TIME-SHORT/MIDDLE/LONG.

$V_{REF(DQ)}$ Training

The device's internal $V_{REF(DQ)}$ specification parameters are operating voltage range, step size, V_{REF} step tolerance, V_{REF} step time and V_{REF} valid level.

The voltage operating range specifies the minimum required V_{REF} setting range for LPDDR4 devices. The minimum range is defined by $V_{REF,max}$ and $V_{REF,min}$.

Figure 188: V_{REF} Operating Range ($V_{REF,max}$, $V_{REF,min}$)

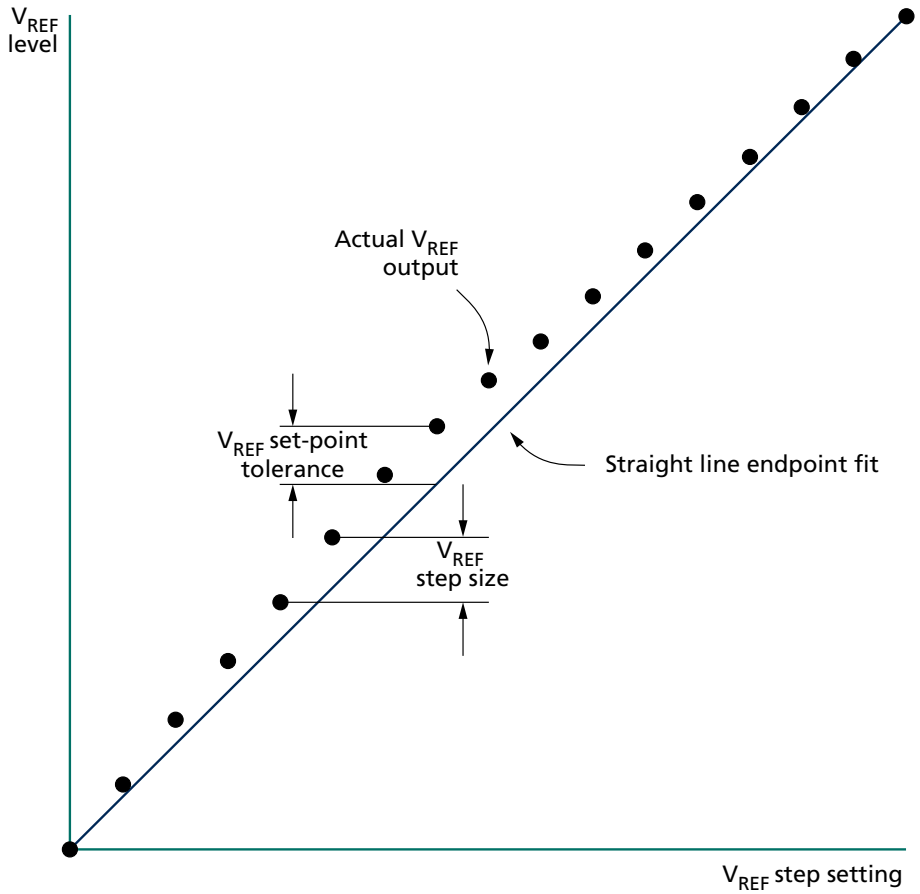


The V_{REF} step size is defined as the step size between adjacent steps. However, for a given design, the device has one value for V_{REF} step size that falls within the given range.

The V_{REF} set tolerance is the variation in the V_{REF} voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for V_{REF} set tolerance uncertainty. The range of V_{REF} set tolerance uncertainty is a function of the number of steps *n*.

The V_{REF} set tolerance is measured with respect to the ideal line that is based on the two endpoints, where the endpoints are at the minimum and maximum V_{REF} values for a specified range.

Figure 189: V_{REF} Set Tolerance and Step Size



The V_{REF} increment/decrement step times are defined by ${}^{t}V_{REF}$_TIME-SHORT, ${}^{t}V_{REF}$_TIME-MIDDLE and ${}^{t}V_{REF}$_TIME-LONG. The ${}^{t}V_{REF}$_TIME-SHORT, ${}^{t}V_{REF}$_TIME-MIDDLE and ${}^{t}V_{REF}$_TIME-LONG times are defined from TS to TE in the following figure where TE is referenced to when the V_{REF} voltage is at the final DC level within the V_{REF} valid tolerance (V_{REF,VAL_TOL}).

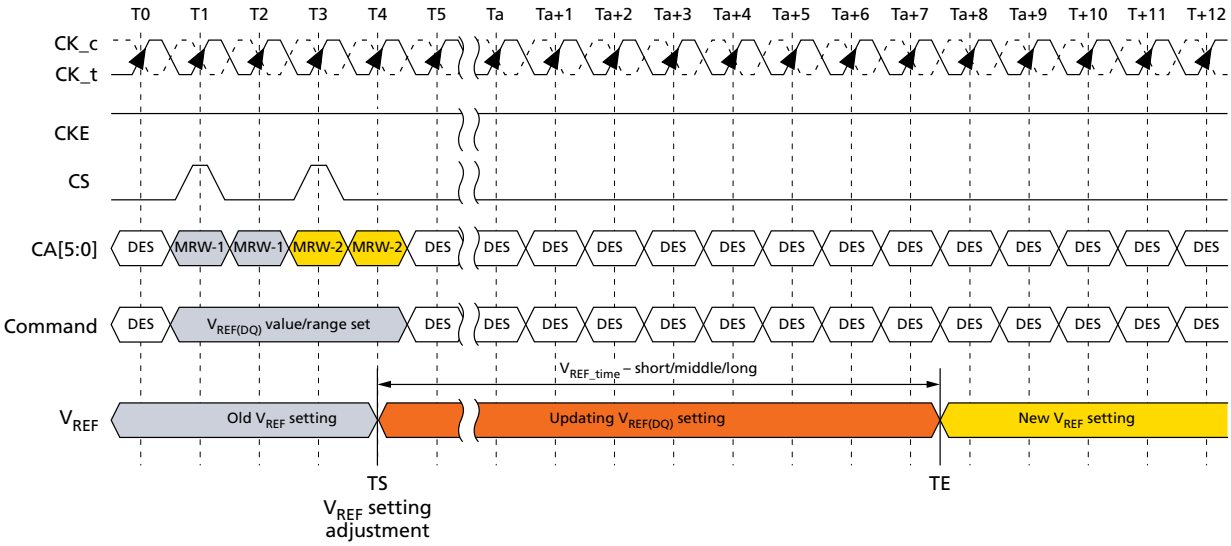
The V_{REF} valid level is defined by V_{REF,VAL_TOL} to qualify the step time TE (see the figure below). This parameter is used to ensure an adequate RC time constant behavior of the voltage level change after any V_{REF} increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

${}^{t}V_{REF}$_TIME-SHORT is for a single step size increment/decrement change in the V_{REF} voltage.

${}^{t}V_{REF}$_TIME-MIDDLE is at least two step sizes of increment/decrement change in the $V_{REF(DQ)}$ range in the V_{REF}voltage.

${}^{t}V_{REF}$_TIME-LONG is the time including and up to the full range of V_{REF} (MIN to MAX or MAX to MIN) across the $V_{REF(DQ)}$ range in V_{REF} voltage.

Figure 190: $V_{REF(DQ)}$ Transition Time for Short, Middle, or Long Changes



Notes: 1. TS is referenced to MRW command clock.
2. TE is referenced to V_{REF,VAL_TOL}.

The MRW command to the mode register bits are defined as:

MR14 OP[5:0]: $V_{REF(DQ)}$ setting

MR14 OP[6]: $V_{REF(DQ)}$ range

The minimum time required between two V_{REF} MRW commands is ${}^{t}V_{REF}$_TIME-SHORT for a single step and ${}^{t}V_{REF}$_TIME-MIDDLE for a full voltage range step.

Figure 191: $V_{REF(DQ)}$ Single-Step Size Increment

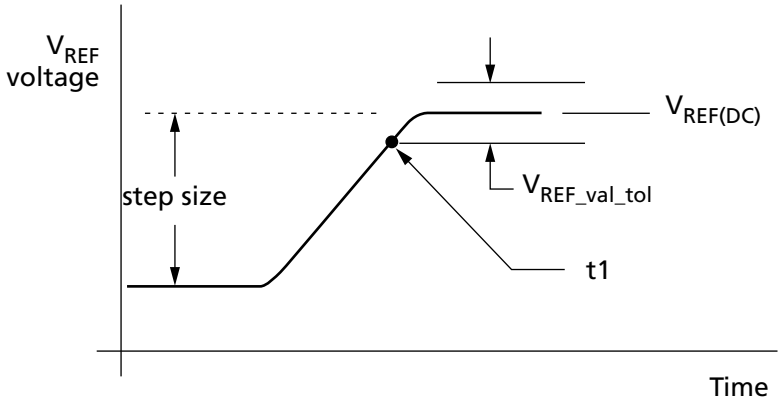


Figure 192: $V_{REF(DQ)}$ Single-Step Size Decrement

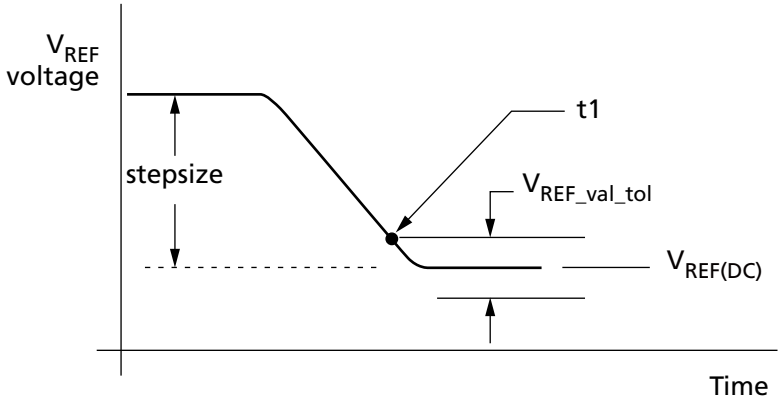


Figure 193: $V_{REF(DQ)}$ Full Step from $V_{REF,min}$ to $V_{REF,max}$

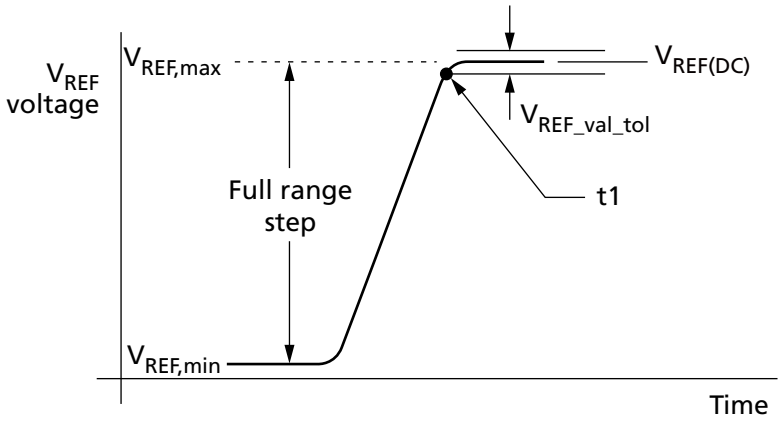
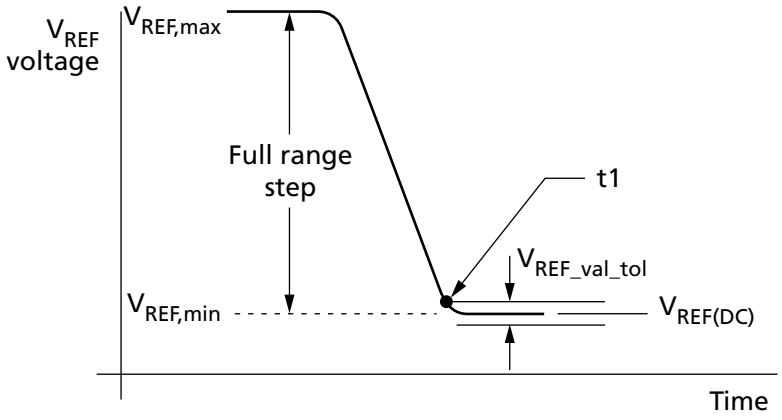


Figure 194: $V_{REF(DQ)}$ Full Step from $V_{REF,max}$ to $V_{REF,min}$



The following table contains the DQ internal V_{REF} specification that will be characterized at the component level for compliance.

Table 160: Internal $V_{REF(DQ)}$ Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{REF(DQ),max\_r0}$	V_{REF} MAX operating point Range-0	–	–	44.9%	V_{DDQ}	1, 11

Table 160: Internal $V_{REF(DQ)}$ Specifications (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{REF(DQ),min\_r0}$	V_{REF} MIN operating point Range-0	15.0%	–	–	V_{DDQ}	1, 11
$V_{REF(DQ),max\_r1}$	V_{REF} MAX operating point Range-1	–	–	62.9%	V_{DDQ}	1, 11
$V_{REF(DQ),min\_r1}$	V_{REF} MIN operating point Range-1	32.9%	–	–	V_{DDQ}	1, 11
$V_{REF(DQ),step}$	$V_{REF(DQ)}$ step size	0.50%	0.60%	0.70%	V_{DDQ}	2
$V_{REF(DQ),set\_tol}$	$V_{REF(DQ)}$ set tolerance	–11	0	11	mV	3, 4, 6
		–1.1	0	1.1	mV	3, 5, 7
$^{t}V_{REF_}$TIME-SHORT	$V_{REF(DQ)}$ step time	–	–	100	ns	8
$^{t}V_{REF_}$TIME-MIDDLE		–	–	200	ns	12
$^{t}V_{REF_}$TIME-LONG		–	–	250	ns	9
$^{t}V_{REF\_time\_weak}$		–	–	1	ms	13, 14
$V_{REF(DQ),val\_tol}$	$V_{REF(DQ)}$ valid tolerance	–0.10%	0.00%	0.10%	V_{DDQ}	10

Notes:
1. $V_{REF(DQ)}$ DC voltage referenced to $V_{DDQ(DC)}$.
2. $V_{REF(DQ)}$ step size increment/decrement range. $V_{REF(DQ)}$ at DC level.
3. $V_{REF(DQ),new} = V_{REF(DQ),old} + n \times V_{REF(DQ),step}$; n = number of steps; if increment, use "+"; if decrement, use "–".
4. The minimum value of $V_{REF(DQ)}$ setting tolerance = $V_{REF(DQ),new}$ - 11mV. The maximum value of $V_{REF(DQ)}$ setting tolerance = $V_{REF(DQ),new}$ + 11mV. For n > 4.
5. The minimum value of $V_{REF(DQ)}$setting tolerance = $V_{REF(DQ),new}$ - 1.1mV. The maximum value of $V_{REF(DQ)}$ setting tolerance = $V_{REF(DQ),new}$ + 1.1mV. For n ≤ 4.
6. Measured by recording the minimum and maximum values of the $V_{REF(DQ)}$ output over the range, drawing a straight line between those points and comparing all other $V_{REF(DQ)}$ output settings to that line.
7. Measured by recording the minimum and maximum values of the $V_{REF(DQ)}$output across four consecutive steps (n = 4), drawing a straight line between those points and comparing all other $V_{REF(DQ)}$ output settings to that line.
8. Time from MRW command to increment or decrement one step size for $V_{REF(DQ)}$.
9. Time from MRW command to increment or decrement $V_{REF,min}$ to $V_{REF,max}$ or $V_{REF,max}$ to $V_{REF,min}$ change across the $V_{REF(DQ)}$ Range in $V_{REF(DQ)}$ Voltage.
10. Only applicable for DRAM component level test/characterization purposes. Not applicable for normal mode of operation. V_{REF} valid is to qualify the step times which will be characterized at the component level.
11. DRAM range-0 or range-1 set by MR14 OP[6].
12. Time from MRW command to increment or decrement more than one step size up to a full range of V_{REF} voltage within the same $V_{REF(DQ)}$ range.
13. Applies when VRCG high current mode is not enabled, specified by MR13 [OP3] = 0.
14. $^{t}V_{REF\_time\_weak}$ covers all $V_{REF(DQ)}$ Range and Value change conditions are applied to $^{t}V_{REF_}$TIME-SHOR/MIDDLE/LONG.

Command Bus Training

Command Bus Training Mode

The command bus must be trained before enabling termination for high-frequency operation. The device provides an internal $V_{REF(CA)}$ that defaults to a level suitable for unterminated, low-frequency operation, but the $V_{REF(CA)}$ must be trained to achieve suitable receiver voltage margin for terminated, high-frequency operation.

The training mode described here centers the internal $V_{REF(CA)}$ in the CA data eye and at the same time allows for timing adjustments of the CS and CA signals to meet setup/hold requirements. Because it can be difficult to capture commands prior to training the CA inputs, the training mode described here uses a minimum of external commands to enter, train, and exit the CA bus training mode.

The die has a bond-pad (ODT_CA) but ODT_CA pin is ignored by LPDDR4X devices. CA ODT is fully controlled through MR11 and MR22. See On-Die Termination for more information.

The device uses frequency set points to enable multiple operating settings for the die. The device defaults to FSP-OP[0] at power-up, which has the default settings to operate in un-terminated, low-frequency environments. Prior to training, the termination should be enabled for one die in each channel by setting MR13 OP[6] = 1b (FSP-WR[1]) and setting all other mode register bits for FSP-OP[1] to the desired settings for high-frequency operation. Upon training entry, the device will automatically switch to FSP-OP[1] and use the high-frequency settings during training (See the Command Bus Training Entry Timing figure for more information on FSP-OP register sets). Upon training exit, the device will automatically switch back to FSP-OP[0], returning to a "known-good" state for unterminated, low-frequency operation.

To enter command bus training mode, issue a MRW-1 command followed by a MRW-2 command to set MR13 OP[0] = 1b (command bus training mode enabled).

After time^{t}MRD, CKE may be set LOW, causing the device to switch to FSP-OP[1], and completing the entry into command bus training mode.

A status DQS_t, DQS_c, DQ, and DMI are as noted below; the DQ ODT state will be followed by FREQUENCY SET POINT function except in the case of output pins.

- DQS_t[0], DQS_c[0] become input pins for capturing DQ[6:0] levels by toggling.
- DQ[5:0] become input pins for setting $V_{REF(CA)}$ level.
- DQ[6] becomes an input pin for setting $V_{REF(CA)}$ range.
- DQ[7] and DMI[0] become input pins, and their input level is valid or floating.
- DQ[13:8] become output pins to feedback, capturing value via the command bus using the CS signal.
- DQS_t[1], DQS_c[1], DMI[1], and DQ[15:14] become output pins or are disabled, meaning the device may be driven to a valid level or may be left floating.

At time^{t}CAENT later, the device may change its $V_{REF(CA)}$ range and value using input signals DQS_t[0], DQS_c[0], and DQ[6:0] from existing value that is set via MR12 OP[6:0]. The mapping between MR12 OP code and DQs is shown below. At least one $V_{REF(CA)}$ setting is required before proceeding to the next training step.

Table 161: Mapping MR12 Op Code and DQ Numbers

	Mapping						
MR12 OP code	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ number	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0

The new $V_{REF(CA)}$ value must "settle" for time ^{t}VREFCA_Long before attempting to latch CA information.

Note: If DQ ODT is enabled in MR11-OP[2:0], then the SDRAM will terminate the DQ lanes during command bus training when entering $V_{REF(CA)}$ range and values on DQ[6:0].

To verify that the receiver has the correct $V_{REF(CA)}$ setting, and to further train the CA eye relative to clock (CK), values latched at the receiver on the CA bus are asynchronously output to the DQ bus.

To exit command bus training mode, drive CKE HIGH, and after time ^{t}VREFCA_Long, issue the MRW-1 command followed by the MRW-2 command to set MR13 OP[0] = 0b. After time ^{t}MRW, the device is ready for normal operation. After training exit, the device will automatically switch back to the FSP-OP registers that were in use prior to training.

Command bus training (CBT) may be executed from the idle or self refresh state. When executing CBT within the self refresh state, the device must not be in a power-down state (for example, CKE must be HIGH prior to training entry). CBT entry and exit is the same, regardless of the state from which CBT is initiated.

Training Sequence for Single-Rank Systems

The sequence example shown here assumes an initial low-frequency, non-terminating operating point training a high-frequency, terminating operating point. The **bold text** shows high-frequency instructions. Any operating point may be trained from any known good operating point.

1. Set MR13 OP[6] = 1b to enable writing to frequency set point 1 (FSP-WR[1]) (or FSP-OP[0]).
2. Write FSP-WR[1] (or FSP-WR[0]) registers for all channels to set up high-frequency operating parameters.
3. Issue MRW-1 and MRW-2 commands to enter command bus training mode.
4. Drive CKE LOW, **and change CK frequency to the high-frequency operating point.**
5. **Perform command bus training ($V_{REF(CA)}$, CS, and CA).**
6. **Exit training by driving CKE HIGH**, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the device will automatically switch back to the FSP-OP registers that were in use prior to training (trained values are not retained).
7. Write the trained values to FSP-WR[1] (or FSP-WR[0]) by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
8. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[1] (or FSP-OP[0]), to turn on termination, **and change CK frequency to the high-frequency operating point. At this point the command bus is trained and you may proceed to other training or normal operation.**

Training Sequence for Multiple-Rank Systems

The sequence example shown here is assuming an initial low-frequency operating point, training a high-frequency operating point. The **bold text** shows high-frequency instructions. Any operating point may be trained from any known good operating point.

1. Set MR13 OP[6] = 1b to enable writing to frequency set point 1 (FSP-WR[1]) (or FSP-WR[0]).
2. Write FSP-WR[1] (or FSP-WR[0]) registers for all channels and ranks to set up high-frequency operating parameters.
3. Read MR0 OP[7] on all channels and ranks to determine which die are terminating, signified by MR0 OP[7] = 1b.
4. Issue MRW-1 and MRW-2 commands to enter command bus training mode on the terminating rank.
5. Drive CKE LOW on the terminating rank (or all ranks), **and change CK frequency to the high-frequency operating point.**

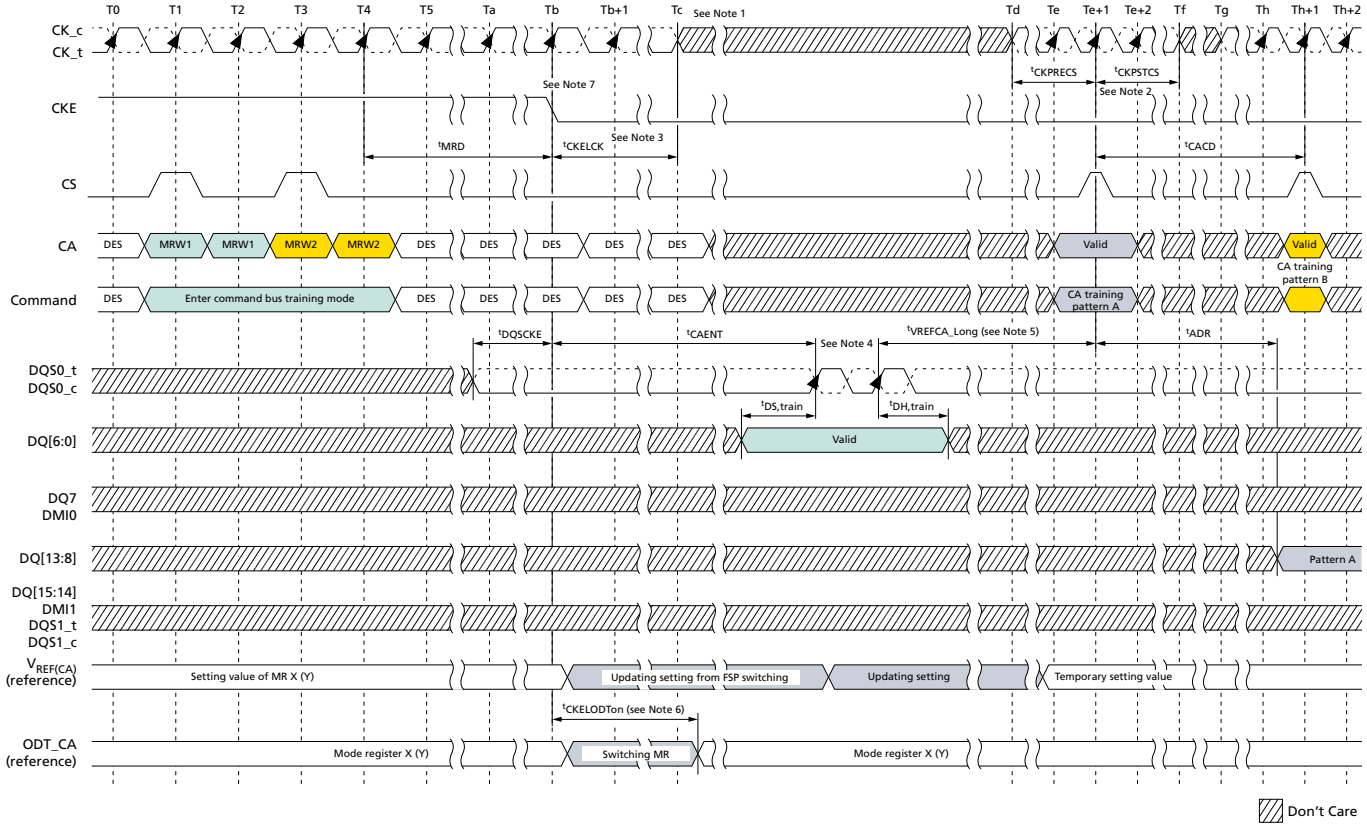
6. **Perform command bus training on the terminating rank ($V_{REF(CA)}$, CS, and CA).**
7. **Exit training by driving CKE HIGH**, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands to write the trained values to FSP-WR[1] (or FSP-WR[0]). When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (trained values are not retained by the device).
8. Issue MRW-1 and MRW-2 commands to enter training mode on the non-terminating rank (but keep CKE HIGH).
9. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[1] (or FSP-OP[0]), to turn on termination, **and change CK frequency to the high-frequency operating point.**
10. **Drive CKE LOW on the non-terminating (or all) ranks. The non-terminating rank(s) will now be using FSP-OP[1] (or FSP-OP[0]).**
11. **Perform command bus training on the non-terminating rank ($V_{REF(CA)}$, CS, and CA).**
12. **Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[0] (or FSP-OP[1]) to turn off termination.**
13. **Exit training by driving CKE HIGH on the non-terminating rank**, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the device will automatically switch back to the FSP-OP registers that were in use prior to training (that is, trained values are not retained by the device).
14. Write the trained values to FSP-WR[1] (or FSP-WR[0]) by issuing MRW-1 and MRW-2 commands and setting all applicable mode register parameters.
15. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[1] (or FSP-OP[0]), to turn on termination,**and change CK frequency to the high-frequency operating point. At this point the command bus is trained for both ranks and the user may proceed to other training or normal operation.**

Relation Between CA Input Pin and DQ Output Pin

Table 162: Mapping CA Input Pin and DQ Output Pin

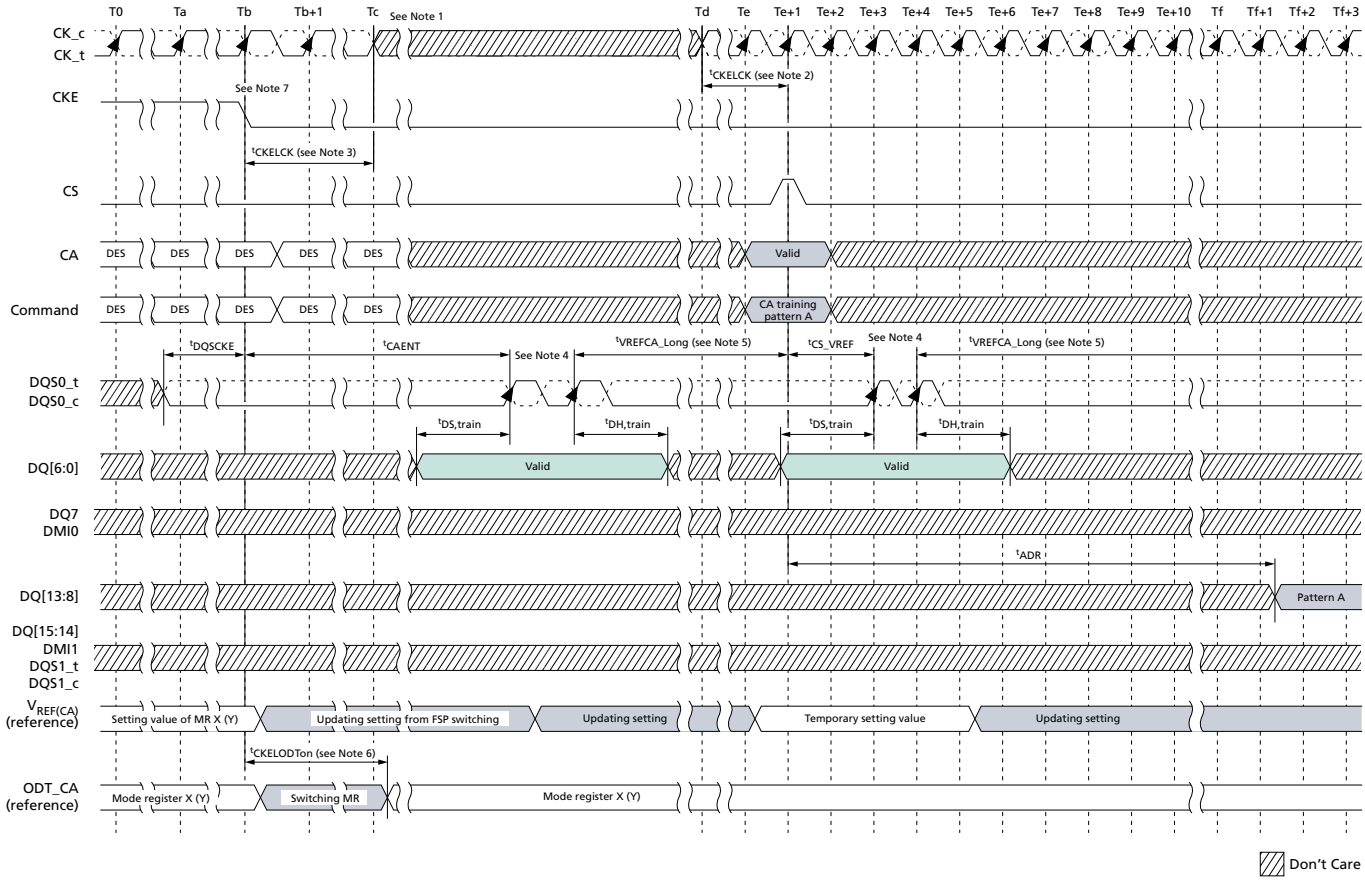
	Mapping					
CA number	CA5	CA4	CA3	CA2	CA1	CA0
DQ number	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8

Figure 195: Command Bus Training Mode Entry – CA Training Pattern I/O with $V_{REF(CA)}$ Value Update



Notes: 1. After ^{t}CKELCK, the clock can be stopped or the frequency changed any time.
2. The input clock condition should be satisfied ^{t}CKPRECS and ^{t}CKPSTCS.
3. Continue to drive CK, and hold CA and CS LOW, until ^{t}CKELCK after CKE is LOW (which disables command decoding).
4. The device may or may not capture the first rising edge of DQS_t/DQS_c due to an unstable first rising edge. Therefore, at least two consecutive pulses of DQS signal input is required every for DQS input signal while capturing DQ[6:0] signals. The captured value of the DQ[6:0] signal level by each DQS edge may be overwritten at any time and the device will temporarily update the $V_{REF(CA)}$ setting of MR12 after time ^{t}VREFCA_Long.
5. ^{t}VREFCA_Long may be reduced to ^{t}VREFCA_Short if the following conditions are met: 1) The new V_{REF} setting is a single step above or below the old V_{REF} setting; 2) The DQS pulses a single time, or the new V_{REF} setting value on DQ[6:0] is static and meets ^{t}DS,train/^{t}DH,train for every DQS pulse applied.
6. When CKE is driven LOW, the device will switch its FSP-OP registers to use the alternate (non-active) set. For example, if the device is currently using FSP-OP[0], then it will switch to FSP-OP[1] when CKE is driven LOW. All operating parameters should be written to the alternate mode registers before entering command bus training to ensure that ODT settings, RL/WL/nWR setting, and so forth, are set to the correct values.
7. When CKE is driven LOW in command bus training mode, the device will change operation to the alternate FSP, that is, the inverse of the FSP programmed in the FSP-OP mode register.

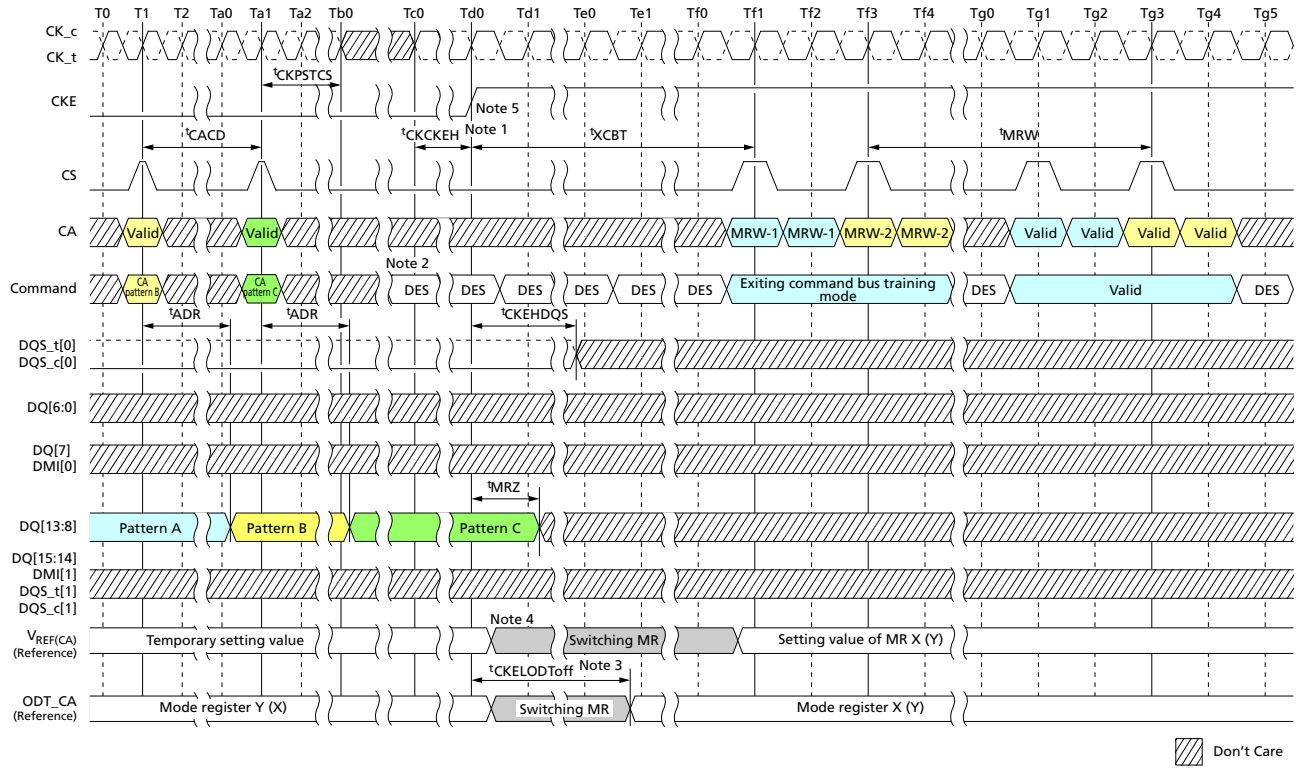
Figure 196: Consecutive $V_{REF(CA)}$ Value Update



Notes: 1. After ^{t}CKELCK, the clock can be stopped or the frequency changed any time.

2. The input clock condition should be satisfied ^{t}CKPRECS and ^{t}CKPSTCS.
3. Continue to drive CK, and hold CA and CS LOW, until ^{t}CKELCK after CKE is LOW (which disables command decoding).
4. The device may or may not capture the first rising edge of DQS_t/DQS_c due to an unstable first rising edge. Therefore, at least two consecutive pulses of DQS signal input is required every for DQS input signal while capturing DQ[6:0] signals. The captured value of the DQ[6:0] signal level by each DQS edge may be overwritten at any time and the device will temporarily update the $V_{REF(CA)}$ setting of MR12 after time ^{t}VREFCA_Long.
5. ^{t}VREFCA_Long may be reduced to ^{t}VREFCA_Short if the following conditions are met: 1) The new V_{REF} setting is a single step above or below the old V_{REF} setting; 2) The DQS pulses a single time, or the new V_{REF} setting value on DQ[6:0] is static and meets ^{t}DS,train/^{t}DH,train for every DQS pulse applied.
6. When CKE is driven LOW, the device will switch its FSP-OP registers to use the alternate (non-active) set. For example, if the device is currently using FSP-OP[0], then it will switch to FSP-OP[1] when CKE is driven LOW. All operating parameters should be written to the alternate mode registers before entering command bus training to ensure that ODT settings, RL/WL/nWR setting, and so forth, are set to the correct values.
7. When CKE is driven LOW in command bus training mode, the device will change operation to the alternate FSP, that is, the inverse of the FSP programmed in the FSP-OP mode register.

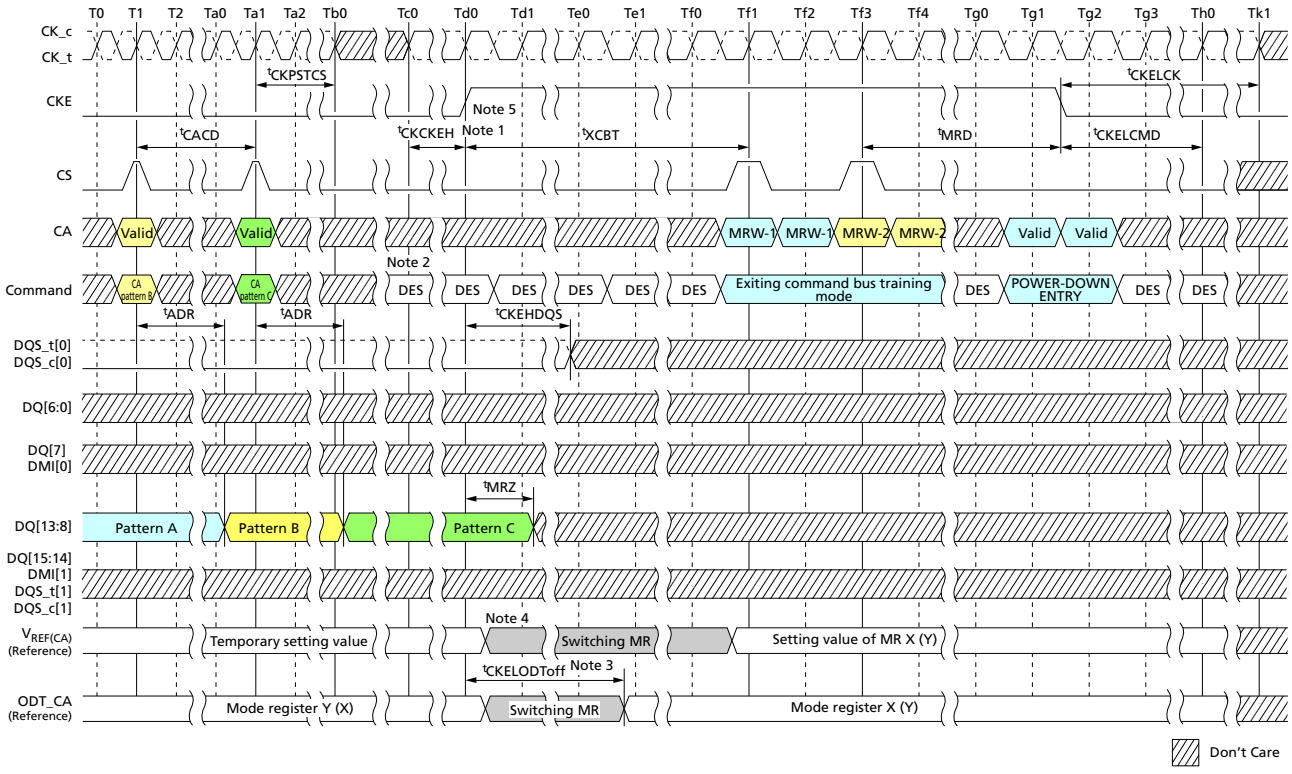
Figure 197: Command Bus Training Mode Exit with Valid Command



Notes: 1. The clock can be stopped or the frequency changed any time before tCKCKEH. CK must meet tCKCKEH before CKE is driven HIGH. When CKE is driven HIGH, the clock frequency must be returned to the original frequency (that is, the frequency corresponding to the FSP at command bus training mode entry.

2. CS and CA[5:0] must be deselected (LOW) tCKCKEH before CKE is driven HIGH.
3. When CKE is driven HIGH, ODT_CA will revert to the state/value defined by FSP-OP prior to command bus training mode entry, that is, the original frequency set point (FSP-OP, MR13-OP[7]). For example, if the device was using FSP-OP[1] for training, then it will switch to FSP-OP[0] when CKE is driven HIGH.
4. Training values are not retained by the device and must be written to the FSP-OP register set before returning to operation at the trained frequency. For example, $V_{REF(CA)}$ will return to the value programmed in the original set point.
5. When CKE is driven HIGH, the device will revert to the FSP in operation at command bus training mode entry.

Figure 198: Command Bus Training Mode Exit with Power-Down Entry



Notes: 1. The clock can be stopped or the frequency changed any time before ^{t}CKCKEH. CK must meet ^{t}CKCKEH before CKE is driven HIGH. When CKE is driven HIGH, the clock frequency must be returned to the original frequency (that is, the frequency corresponding to the FSP at command bus training mode entry.

2. CS and CA[5:0] must be deselected (LOW) ^{t}CKCKEH before CKE is driven HIGH.
3. When CKE is driven HIGH, ODT_CA will revert to the state/value defined by FSP-OP prior to command bus training mode entry, that is, the original frequency set point (FSP-OP, MR13-OP[7]). For example, if the device was using FSP-OP[1] for training, then it will switch to FSP-OP[0] when CKE is driven HIGH.
4. Training values are not retained by the device and must be written to the FSP-OP register set before returning to operation at the trained frequency. For example, $V_{REF(CA)}$ will return to the value programmed in the original set point.
5. When CKE is driven HIGH, the device will revert to the FSP in operation at command bus training mode entry.

Write Leveling

Mode Register Write-WR Leveling Mode

To improve signal-integrity performance, the device provides a write leveling feature to compensate for CK-to-DQS timing skew, affecting timing parameters such as ^{t}DQSS, ^{t}DSS, and ^{t}DSH. The memory controller uses the write leveling feature to receive feedback from the device, enabling it to adjust the clock-to-data strobe signal relationship for each DQS_t/DQS_c signal pair. The device samples the clock state with the rising edge of DQS signals and asynchronously feeds back to the memory controller. The memory controller references this feedback to adjust the clock-to-data strobe signal relationship for each DQS_t/DQS_c signal pair.

All data bits (DQ[7:0] for DQS[0] and DQ[15:8] for DQS[1]) carry the training feedback to the controller. Both DQS signals in each channel must be leveled independently. Write leveling entry/exit is independent between channels for dual-channel devices.

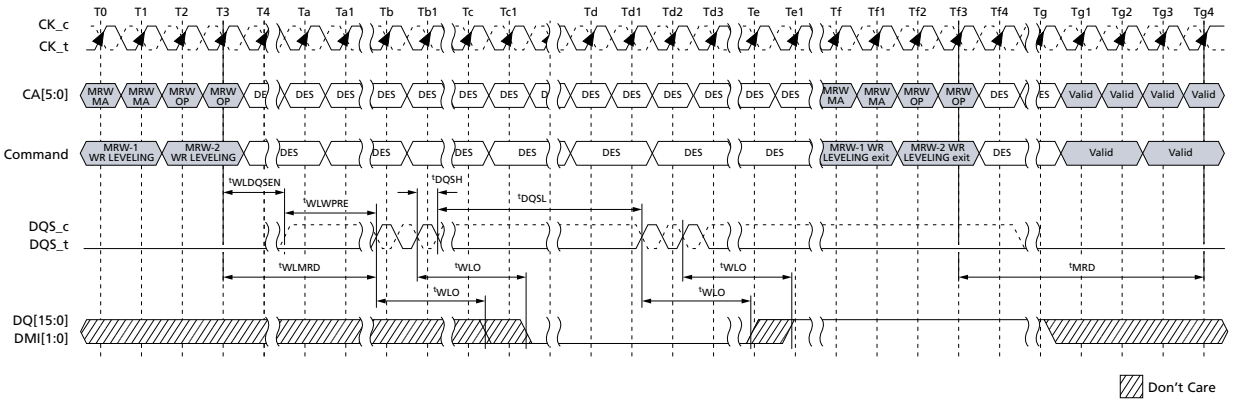
The device enters write leveling mode when mode register MR2-OP[7] is set HIGH. When entering write leveling mode, the state of the DQ pins is undefined. During write leveling mode, only DESELECT commands, or a MRW command to exit the WRITE LEVELING operation, are allowed. Depending on the absolute values of ^{t}QSL and ^{t}QSH in the application, the value of ^{t}DQSS may have to be better than the limits provided in the AC Timing Parameters section in order to satisfy the ^{t}DSS and ^{t}DSH specifications. Upon completion of the WRITE LEVELING operation, the device exits write leveling mode when MR2-OP[7] is reset LOW.

Write leveling should be performed before write training (DQS2DQ training).

Write Leveling Procedure

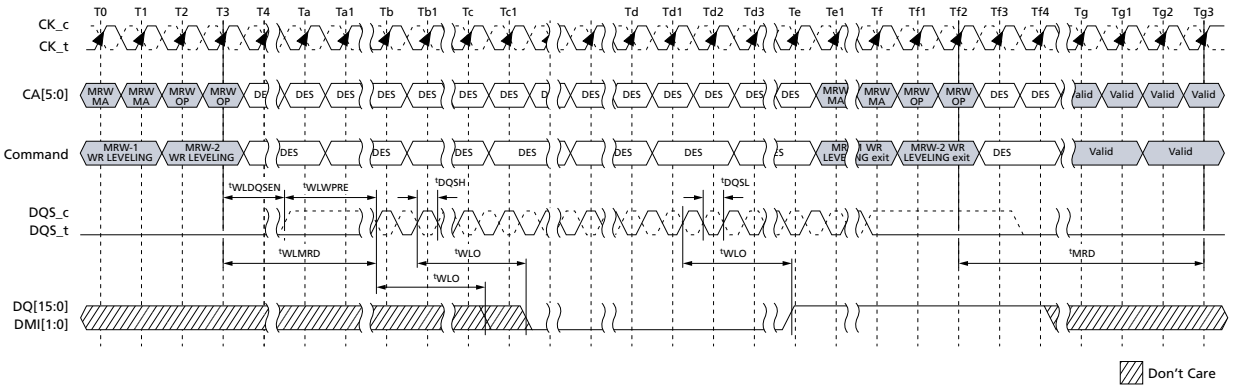
1. Enter write leveling mode by setting MR2-OP[7]=1.
2. Once in write leveling mode, DQS_t must be driven LOW and DQS_c HIGH after a delay of ^{t}WLDQSEN.
3. Wait for a time ^{t}WLMRD before providing the first DQS signal input. The delay time ^{t}WLMRD(MAX) is controller-dependent.
4. The device may or may not capture the first rising edge of DQS_t due to an unstable first rising edge; therefore, at least two consecutive pulses of DQS signal input is required for every DQS input signal during write training mode. The captured clock level for each DQS edge is overwritten, and the device provides asynchronous feedback on all DQ bits after time ^{t}WLO.
5. The feedback provided by the device is referenced by the controller to increment or decrement the DQS_t and/or DQS_c delay settings.
6. Repeat steps 4 and 5 until the proper DQS_t/DQS_c delay is established.
7. Exit write leveling mode by setting MR2-OP[7] = 0.

Figure 199: Write Leveling Timing – ^{t}DQSL(MAX)



Note: 1. Clock can be stopped except during DQS toggle period (CK_t = LOW, CK_c = HIGH). However, a stable clock prior to sampling is required to ensure timing accuracy.

Figure 200: Write Leveling Timing – ^{t}DQSL(MIN)

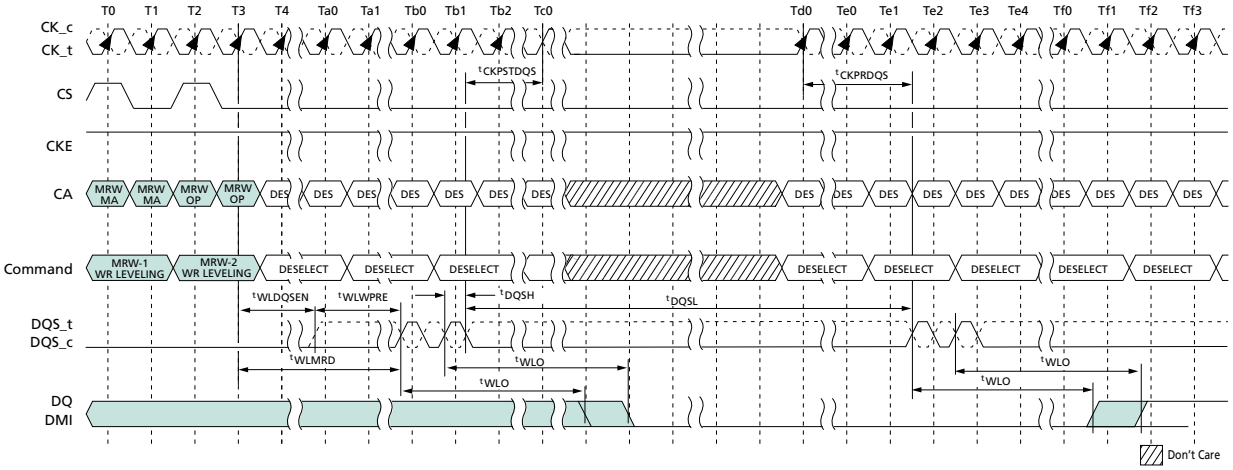


Note: 1. Clock can be stopped except during DQS toggle period (CK_t = LOW, CK_c = HIGH). However, a stable clock prior to sampling is required to ensure timing accuracy.

Input Clock Frequency Stop and Change

The input clock frequency can be stopped or changed from one stable clock rate to another stable clock rate during write leveling mode. The frequency stop or change timing is shown below.

Figure 201: Clock Stop and Timing During Write Leveling



Notes: 1. CK_t is held LOW and CK_c is held HIGH during clock stop.
2. CS will be held LOW during clock stop.

Table 163: Write Leveling Timing Parameters

Parameter	Symbol	Min/Max	Value	Units
DQS_t/DQS_c delay after write leveling mode is programmed	^{t}WLDQSEN	MIN	20	^{t}CK
		MAX	–	
Write preamble for write leveling	^{t}WLWPRE	MIN	20	^{t}CK
		MAX	–	
First DQS_t/DQS_c edge after write leveling mode is programmed	^{t}WLMRD	MIN	40	^{t}CK
		MAX	–	
Write leveling output delay	^{t}WLO	MIN	0	ns
		MAX	20	
MODE REGISTER SET command delay	^{t}MRD	Refer to Mode Register Timing Parameter Table		
Valid clock requirement before DQS toggle	^{t}CKPRDQS	MIN	MAX(7.5ns, 4*n*CK)	–
		MAX	–	
Valid clock requirement after DQS toggle	^{t}CKPSTDQS	MIN	MAX(7.5ns, 4*n*CK)	–
		MAX	–	

Table 164: Write Leveling Setup and Hold Timing

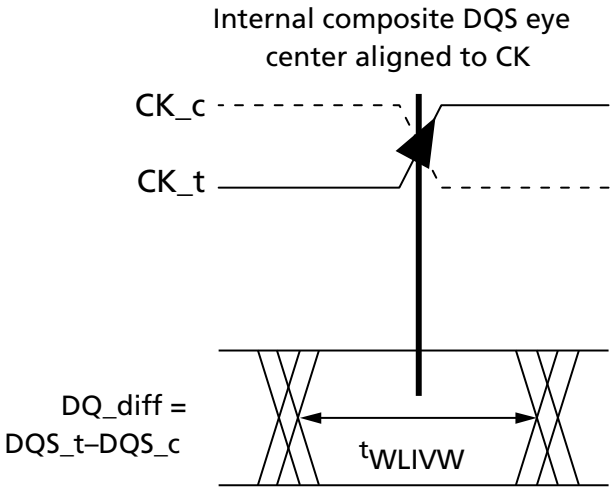
Parameter	Symbol	Min/Max	Data Rate					Unit
			1600	2400	3200	3733	4267	
Write leveling hold time	^{t}WLH	MIN	150	100	75	62.5	50	ps
Write leveling setup time	^{t}WLS	MIN	150	100	75	62.5	50	ps
Write leveling input valid window	^{t}WLIVW	MIN	240	160	120	105	90	ps

Notes: 1. In addition to the traditional setup and hold time specifications, there is value in an invalid window-based specification for write leveling training. As the training is based on each device, worst-case process skews for setup and hold do not make sense to close timing between CK and DQS.

2. ^{t}WLIVW is defined in a similar manner to TdIVW_total, except that here it is a DQS invalid window with respect to CK. This would need to account for all voltage and temperature (VT) drift terms between CK and DQS within the device that affect the write leveling invalid window.

The figure below shows the DQS input mask for timing with respect to CK. The "total" mask (^{t}WLIVW) defines the time the input signal must not encroach in order for the DQS input to be successfully captured by CK. The mask is a receiver property and it is not the valid data-eye.

Figure 202: DQS_t/DQS_c to CK_t/CK_c Timings at the Pins Referenced from the Internal Latch



MULTIPURPOSE Operation

The device uses the MULTIPURPOSE command to issue a NO OPERATION (NOP) command and to access various training modes. The MPC command is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. The MPC command has seven operands (OP[6:0]) that are decoded to execute specific commands in the SDRAM. OP[6] is a special bit that is decoded on the first rising CK edge of the MPC command. When OP[6] = 0, the device executes a NOP command, and when OP[6] = 1, the device further decodes one of several training commands.

When OP[6] = 1 and the training command includes a READ or WRITE operation, the MPC command must be followed immediately by a CAS-2 command. For training commands that read or write, READ latency (RL) and WRITE latency (WL) are counted from the second rising CK edge of the CAS-2 command with the same timing relationship as a typical READ or WRITE command. The operands of the CAS-2 command following a MPC READ/WRITE command must be driven LOW. The following MPC commands must be followed by a CAS-2 command:

- WRITE-FIFO
- READ-FIFO
- READ DQ CALIBRATION

All other MPC commands do not require a CAS-2 command, including the following:

- NOP
- START DQS INTERVAL OSCILLATOR
- STOP DQS INTERVAL OSCILLATOR
- ZQCAL START (ZQ CALIBRATION START)
- ZQCAL LATCH (ZQ CALIBRATION LATCH)

Table 165: MPC Command Definition

SDR Command	SDR Command Pins			SDR CA Pins						CK_t Edge	Notes
	CKE										
	CK_t (n-1)	CK_t (n)	CS	CA0	CA1	CA2	CA3	CA4	CA5		
MPC (Train, NOP)	H	H	H	L	L	L	L	L	OP6	↑	1, 2
			L	OP0	OP1	OP2	OP3	OP4	OP5	↑	

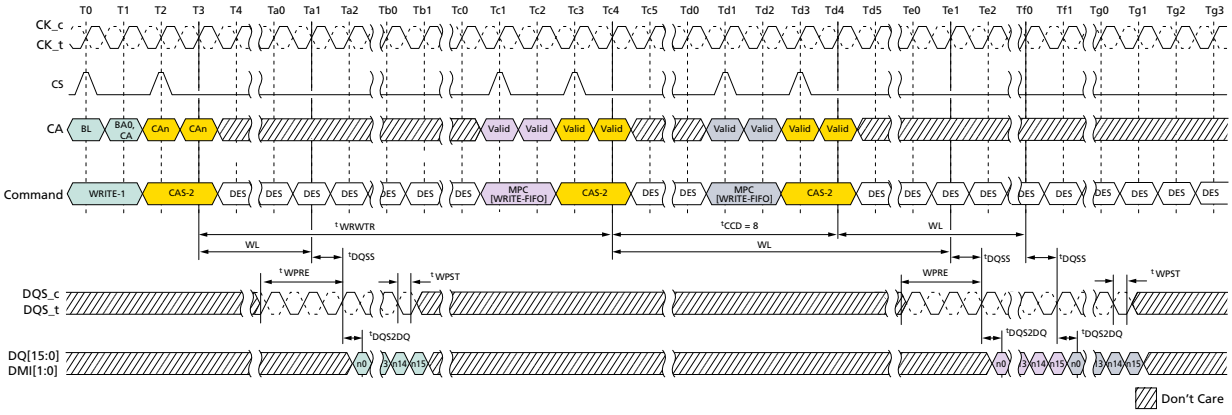
Notes: 1. See the Command Truth Table for more information.
2. MPC commands for READ or WRITE TRAINING operations must be immediately followed by the CAS-2 command, consecutively, without any other commands in between. The MPC command must be issued before issuing the CAS-2 command.

Table 166: MPC Commands

Function	Operand	Data
Training Modes	OP[6:0]	**0XXXXXXb:** NOP
		1000001b: READ-FIFO: READ-FIFO supports only BL16 operation
		1000011b: READ DQ CALIBRATION (MR32/MR40)
		1000101b: RFU
		1000111b: WRITE-FIFO: WRITE-FIFO supports only BL16 operation
		1001001b: RFU
		1001011b: START DQS OSCILLATOR
		1001101b: STOP DQS OSCILLATOR
		1001111b: ZQCAL START
		1010001b: ZQCAL LATCH
		All Others: Reserved

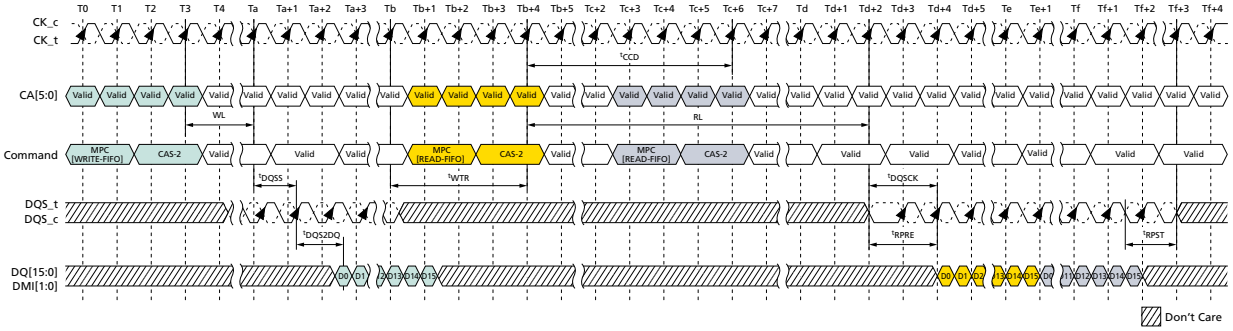
Notes: 1. See command truth table for more information.
2. MPC commands for READ or WRITE TRAINING operations must be immediately followed by CAS-2 command consecutively without any other commands in-between. MPC command must be issued first before issuing the CAS-2 command.
3. WRITE-FIFO and READ-FIFO commands will only operate as BL16, ignoring the burst length selected by MR1 OP[1:0].

Figure 203: WRITE-FIFO – ^{t}WPRE = 2*n*CK, ^{t}WPST = 0.5*n*CK



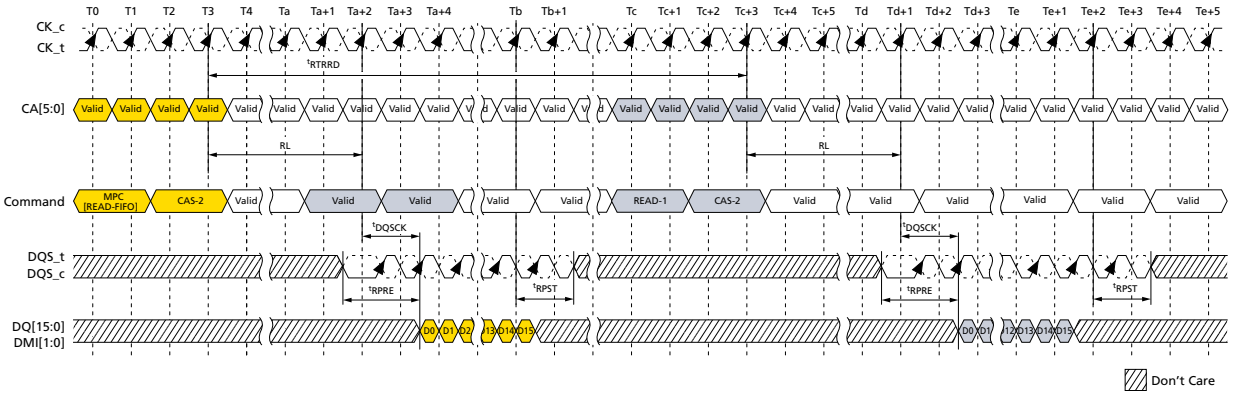
Notes: 1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active, during refresh or during self refresh, with CKE HIGH.
2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timing from Write-1 to MPC[WRITE-FIFO] is ^{t}WRWTR.
3. Seamless MPC[WRITE-FIFO] commands may be executed by repeating the command every^{t}CCD time.
4. MPC[WRITE-FIFO] uses the same command-to-data timing relationship (WL, ^{t}DQSS, ^{t}DQS2DQ) as a WRITE-1 command.
5. A maximum of five MPC[WRITE-FIFO] commands may be executed consecutively without corrupting FIFO data. The sixth MPC[WRITE-FIFO] command will overwrite the FIFO data from the first command. If fewer than five MPC[WRITE-FIFO] commands are executed, then the remaining FIFO locations will contain undefined data.
6. For the CAS-2 command following an MPC command, the CAS-2 operands must be driven LOW.
7. To avoid corrupting the FIFO contents, MPC[READ-FIFO] must immediately follow MPC[WRITE-FIFO]/CAS-2 without any other commands in-between. See Write Training section for more information on FIFO pointer behavior.

Figure 204: READ-FIFO – ^{t}WPRE = 2*n*CK, ^{t}WPST = 0.5*n*CK, ^{t}RPRE = Toggling, ^{t}RPST = 1.5*n*CK



Notes: 1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active, during refresh or during self refresh with CKE HIGH.
2. Seamless MPC[READ-FIFO] commands may be executed by repeating the command every ^{t}CCD time.
3. MPC[READ-FIFO] uses the same command-to-data timing relationship (RL, ^{t}DQSCK) as a READ-1 command.
4. Data may be continuously read from the FIFO without any data corruption. After five MPC[READ-FIFO] commands, the FIFO pointer will wrap back to the first FIFO and continue advancing. If fewer than five MPC[WRITE-FIFO] commands were executed, then the MPC[READ-FIFO] commands to those FIFO locations will return undefined data. See Write Training for more information on the FIFO pointer behavior.
5. For the CAS-2 command immediately following an MPC command, the CAS-2 operands must be driven LOW.
6. DMI[1:0] signals will be driven if WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training for more information on DMI behavior.

Figure 205: READ-FIFO – ^{t}RPRE = Toggling, ^{t}RPST = 1.5*n*CK



Notes: 1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active, during refresh or during self refresh with CKE HIGH.
2. MPC[READ-FIFO] to READ-1 operation is shown as an example of command-to-command timing for MPC. Timing from MPC[READ-FIFO] command to read is ^{t}RTRRD.
3. Seamless MPC[READ-FIFO] commands may be executed by repeating the command every ^{t}CCD time.
4. MPC[READ-FIFO] uses the same command-to-data timing relationship (RL, ^{t}DQSCK) as a READ-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After five MPC[READ-FIFO] commands, the FIFO pointer will wrap back to the first FIFO and continue advancing. If fewer than five MPC[WRITE-FIFO] commands are executed, then the MPC[READ-FIFO] commands to those FIFO locations will return undefined data. See Write Training for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following an MPC command, the CAS-2 operands must be driven LOW.
7. DMI[1:0] signals will be driven if WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training for more information on DMI behavior.

Table 167: Timing Constraints for Training Commands

Previous Command	Next Command	Minimum Delay	Unit	Notes
WR/MWR	MPC[WRITE-FIFO]	^{t}WRWTR	*n*CK	1
	MPC[READ-FIFO]	Not allowed	–	2
	MPC[READ DQ CALIBRATION]	WL + RU(^{t}DQSS(MAX)/^{t}CK) + BL/2 + RU(^{t}WTR/^{t}CK)	*n*CK	
RD/MRR	MPC[WRITE-FIFO]	^{t}RTRRD	*n*CK	3
	MPC[READ-FIFO]	Not allowed	–	2
	MPC[READ DQ CALIBRATION]	^{t}RTRRD	*n*CK	3
MPC[WRITE-FIFO]	WR/MWR	Not allowed	–	2
	MPC[WRITE-FIFO]	^{t}CCD	*n*CK	
	RD/MRR	Not allowed	–	2
	MPC[READ-FIFO]	WL + RU(^{t}DQSS(MAX)/^{t}CK) + BL/2 + RU(^{t}WTR/^{t}CK)	*n*CK	
	MPC[READ DQ CALIBRATION]	Not allowed	–	2
MPC[READ-FIFO]	WR/MWR	^{t}RTRRD	*n*CK	3
	MPC[WRITE-FIFO]	^{t}RTW	*n*CK	4
	RD/MRR	^{t}RTRRD	*n*CK	3
	MPC[READ-FIFO]	^{t}CCD	*n*CK	
	MPC[READ DQ CALIBRATION]	^{t}RTRRD	*n*CK	3
MPC[READ DQ CALIBRATION]	WR/MWR	^{t}RTRRD	*n*CK	3
	MPC[WRITE-FIFO]	^{t}RTRRD	*n*CK	3
	RD/MRR	^{t}RTRRD	*n*CK	3
	MPC[READ-FIFO]	Not allowed	–	2
	MPC[READ DQ CALIBRATION]	^{t}CCD	*n*CK	

Notes: 1. ^{t}WRWTR = WL + BL/2 + RU(^{t}DQSS(MAX)/^{t}CK) + MAX(RU(7.5ns/^{t}CK), 8*n*CK).
2. No commands are allowed between MPC[WRITE-FIFO] and MPC[READ-FIFO] except the MRW commands related to training parameters.
3. ^{t}RTRRD = RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 + RD(^{t}RPST) + MAX(RU(7.5ns/^{t}CK), 8*n*CK).
4. In case of DQ ODT disable MR11 OP[2:0] = 000b,

   ^{t}RTW = RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 - WL + ^{t}WPRE + RD(^{t}RPST).

   In case of DQ ODT enable MR11 OP[2:0] ≠ 000b,

   ^{t}RTW = RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 + RD(^{t}RPST) - ODTLon - RD(^{t}ODTon(MIN)/^{t}CK) + 1.

Read DQ Calibration Training

Read DQ Calibration Training Procedure

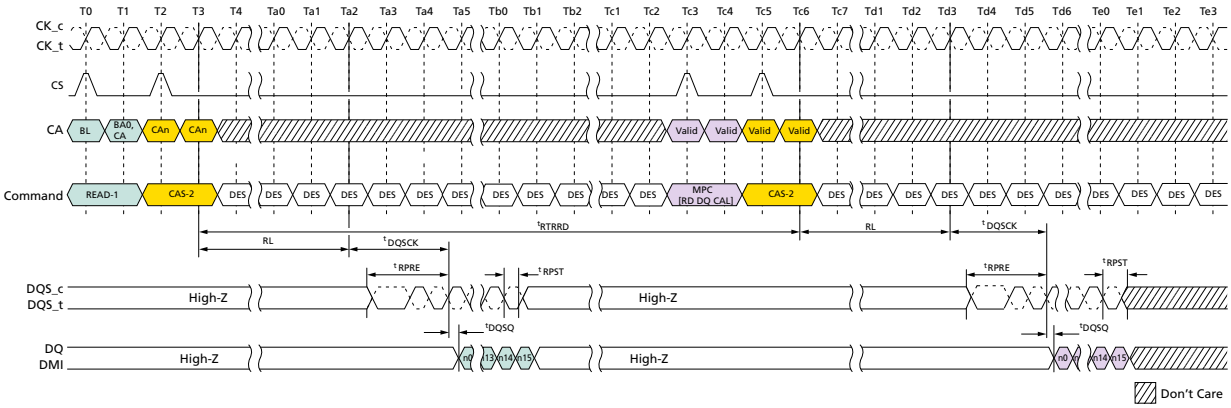
The READ DQ CALIBRATION TRAINING function outputs a 16-bit, user-defined pattern on the DQ pins. Read DQ calibration is initiated by issuing a MPC[READ DQ CALIBRATION] command followed by a CAS-2 command, which causes the device to drive the contents of MR32, followed by the contents of MR40 on each of DQ[15:0] and DMI[1:0]. The pattern can be inverted on selected DQ pins according to user-defined invert masks written to MR15 and MR20.

1. Issue MRW commands to write MR32 (first eight bits), MR40 (second eight bits), MR15 (eight-bit invert mask for byte 0), and MR20 (eight-bit invert mask for byte 1).
   In the alternative, this step could be replaced with the default pattern:
   - MR32 default = 5Ah
   - MR40 default = 3Ch
   - MR15 default = 55h
   - MR20 default = 55h
2. Issue an MPC command, followed immediately by a CAS-2 command.
   - Each time an MPC command followed by a CAS-2 is received by the device, a 16-bit data burst will drive the eight bits programmed in MR32 followed by the eight bits programmed in MR40 on all I/O pins after the currently-set RL.
   - The data pattern will be inverted for I/O pins with a 1 programmed in the corresponding invert mask mode register bit (see table below).
   - The pattern is driven on the DMI pins, but no DATA BUS INVERSION function is enabled, even if read DBI is enabled in the mode register.
   - The MPC command can be issued every ^{t}CCD seamlessly, and ^{t}RTRRD delay is required between ARRAY READ command and the MPC command as well the delay required between the MPC command and an ARRAY READ.
   - The operands received with the CAS-2 command must be driven LOW.
3. DQ
   - Read DQ calibration training can be performed with any or no banks active during refresh or during self refresh with CKE HIGH.

Table 168: Invert Mask Assignments

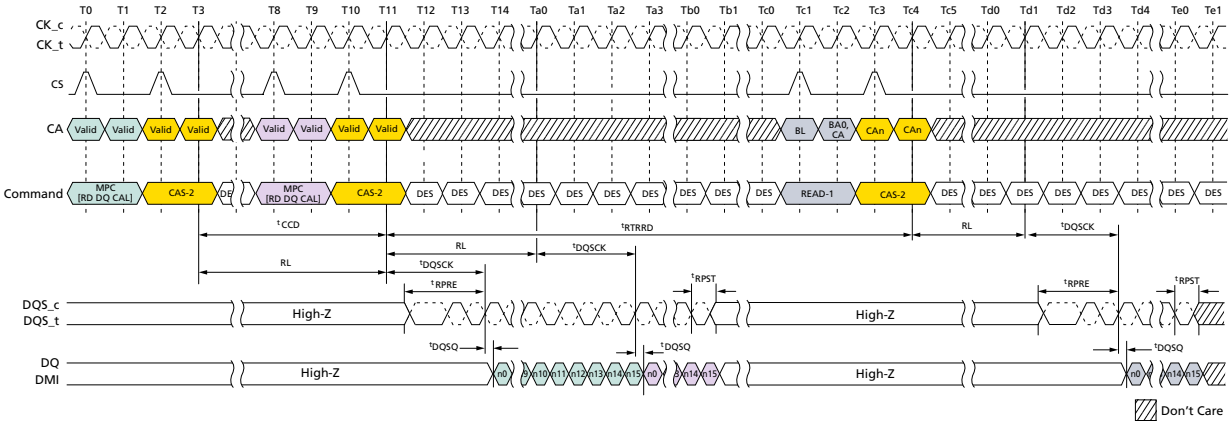
DQ pin	0	1	2	3	DMI0	4	5	6	7
MR15 bit	0	1	2	3	N/A	4	5	6	7
DQ pin	8	9	10	11	DMI1	12	13	14	15
MR20 bit	0	1	2	3	N/A	4	5	6	7

Figure 206: Read DQ Calibration Training Timing: Read-to-Read DQ Calibration



Notes: 1. Read-1 to MPC operation is shown as an example of command-to-command timing. Timing from Read-1 to MPC command is ^{t}RTRRD.
2. MPC uses the same command-to-data timing relationship (RL, ^{t}DQSCK, ^{t}DQSQ) as a Read-1 command.
3. BL = 16, Read preamble: Toggle, Read postamble: 0.5*n*CK.
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 207: Read DQ Calibration Training Timing: Read DQ Calibration to Read DQ Calibration/ Read



Notes: 1. MPC[READ DQ CALIBRATION] to MPC[READ DQ CALIBRATION] operation is shown as an example of command-to-command timing.
2. MPC[READ DQ CALIBRATION] to READ-1 operation is shown as an example of command-to-command timing.
3. MPC[READ DQ CALIBRATION] uses the same command-to-data timing relationship (RL, ^{t}DQSCK, ^{t}DQSQ) as a READ-1 command.
4. Seamless MPC[READ DQ CALIBRATION] commands may be executed by repeating the command every ^{t}CCD time.
5. Timing from MPC[READ DQ CALIBRATION] command to READ-1 is ^{t}RTRRD.
6. BL = 16, Read preamble: Toggle, Read postamble: 0.5*n*CK.
7. DES commands are shown for ease of illustration; other commands may be valid at these times.

Read DQ Calibration Training Example

An example of read DQ calibration training output is shown in table below. This shows the 16-bit data pattern that will be driven on each DQ in byte 0 when one READ DQ CALIBRATION TRAINING command is executed. This output assumes the following mode register values are used:

- MR32 = 1CH
- MR40 = 59H

- MR15 = 55H
- MR20 = 55H

Table 169: Read DQ Calibration Bit Ordering and Inversion Example

	Bit Sequence→																
Pin	Invert	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQ0	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ1	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ2	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ3	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DMI0	Never	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ4	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ5	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ6	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ7	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ8	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ9	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ10	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ11	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DMI1	Never	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ12	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ13	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ14	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ15	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0

Notes: 1. The patterns contained in MR32 and MR40 are transmitted on DQ[15:0] and DMI[1:0] when read DQ calibration is initiated via a MPC[READ DQ CALIBRATION] command. The pattern transmitted serially on each data lane, organized little endian such that the low-order bit in a byte is transmitted first. If the data pattern is 27H, then the first bit transmitted with be a 1, followed by 1, 1, 0, 0, 1, 0, and 0. The bit stream will be 00100111 →.
2. MR15 and MR20 may be used to invert the MR32/MR40 data pattern on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
3. DMI [1:0] outputs status follows MR Setting vs. DMI Status table.
4. No DATA BUS INVERSION (DBI) function is enacted during read DQ calibration, even if DBI is enabled in MR3-OP[6].

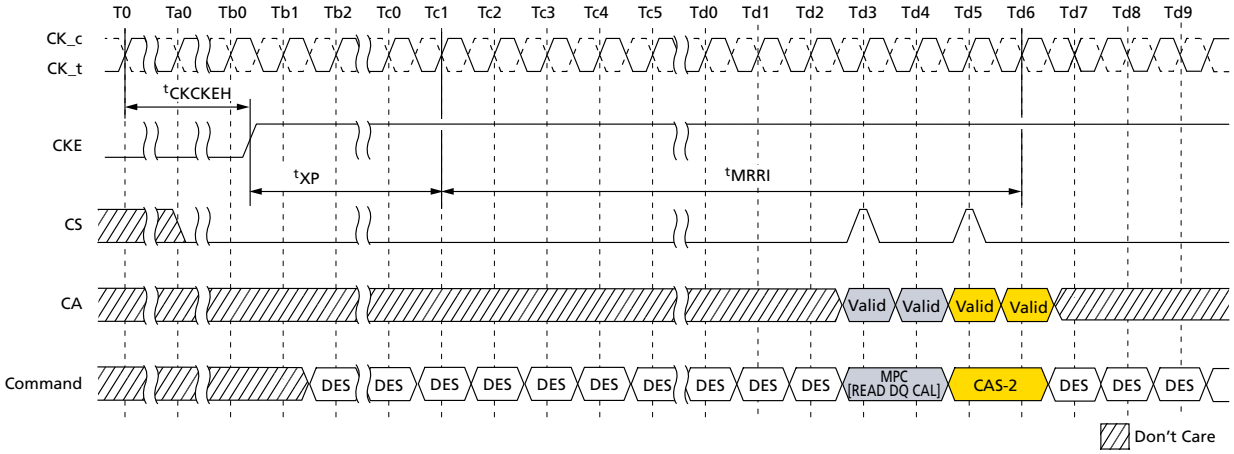
Table 170: MR Setting vs. DMI Status

DM Function MR13 OP[5]	WRITE DBIdc Function MR3 OP[7]	READ DBIdc Function MR3 OP[6] DMI	Status
1: Disable	0: Disable	0: Disable	High-Z
1: Disable	1: Enable	0: Disable	The data pattern is transmitted
1: Disable	0: Disable	1: Enable	The data pattern is transmitted
1: Disable	1: Enable	1: Enable	The data pattern is transmitted
0: Enable	0: Disable	0: Disable	The data pattern is transmitted
0: Enable	1: Enable	0: Disable	The data pattern is transmitted
0: Enable	0: Disable	1: Enable	The data pattern is transmitted
0: Enable	1: Enable	1: Enable	The data pattern is transmitted

MPC[READ DQ CALIBRATION] After Power-Down Exit

Following the power-down state, an additional time, tMRRI, is required prior to issuing the MPC[READ DQ CALIBRATION] command. This additional time (equivalent to tRCD) is required in order to be able to maximize power-down current savings by allowing more power-up time for the read DQ data in MR32 and MR40 data path after exit from standby, power-down mode.

Figure 208: MPC[READ DQ CALIBRATION] Following Power-Down State



Write Training

The device uses an unmatched DQS-DQ path to enable high-speed performance and save power. As a result, the DQS strobe must be trained to arrive at the DQ latch center-aligned with the data eye. The DQ receiver is located at the DQ pad and has a shorter internal delay than the DQS signal. The DQ receiver will latch the data present on the DQ bus when DQS reaches the latch, and training is accomplished by delaying the DQ signals relative to DQS such that the data eye arrives at the receiver latch centered on the DQS transition.

Two modes of training are available:

- Command-based FIFO WR/RD with user patterns
- An internal DQS clock-tree oscillator, which determines the need for, and the magnitude of, required training

The command-based FIFO WR/RD uses the MPC command with operands to enable this special mode of operation. When issuing the MPC command, if CA[5] is set LOW (OP[6] = 0), then the device will perform a NOP command. When CA[5] is set HIGH, the CA[4:0] pins enable training functions or are reserved for future use (RFU). MPC commands that initiate a read or write to the device must be followed immediately by a CAS-2 command. See the MPC Operation section for more information.

To perform write training, the controller can issue an MPC[WRITE-FIFO] command with OP[6:0] set, followed immediately by a CAS-2 command (CAS-2 operands should be driven LOW) to initiate a WRITE-FIFO. Timings for MPC[WRITE-FIFO] are identical to WRITE commands, with WL timed from the second rising clock edge of the CAS-2 command. Up to five consecutive MPC[WRITE-FIFO] commands with user-defined patterns may be issued to the device, which will store up to 80 values (BL16 × 5) per pin that can be read back via the MPC[READ-FIFO] command. (The WRITE/READ-FIFO POINTER operation is described in a different section.

After writing data with the MPC[WRITE-FIFO] command, the data can be read back with the MPC[READ-FIFO] command and results can be compared with "expected" data to determine whether further training (DQ delay) is needed. MPC[READ-FIFO] is initiated by issuing an MPC command, as described in the MPC Operation section, followed immediately by a CAS-2 command

(CAS-2 operands must be driven LOW). Timings for the MPC[READ-FIFO] command are identical to READ commands, with RL timed from the second rising clock edge of the CAS-2 command.

READ-FIFO is nondestructive to the data captured in the FIFO; data may be read continuously until it is disturbed by another command, such as a READ, WRITE, or another MPC[WRITE-FIFO]. If fewer than five WRITE-FIFO commands are executed, unwritten registers will have undefined (but valid) data when read back.

For example, if five WRITE-FIFO commands are executed sequentially, then a series of READ-FIFO commands will read valid data from FIFO[0], FIFO[1]….FIFO[4] and then wrap back to FIFO[0] on the next READ-FIFO. However, if fewer than five WRITE-FIFO commands are executed sequentially (example = 3), then a series of READ-FIFO commands will return valid data for FIFO[0], FIFO[1], and FIFO[2], but the next two READ-FIFO commands will return undefined data for FIFO[3] and FIFO[4] before wrapping back to the valid data in FIFO[0].

The READ-FIFO pointer and WRITE-FIFO pointer are reset under the following conditions:

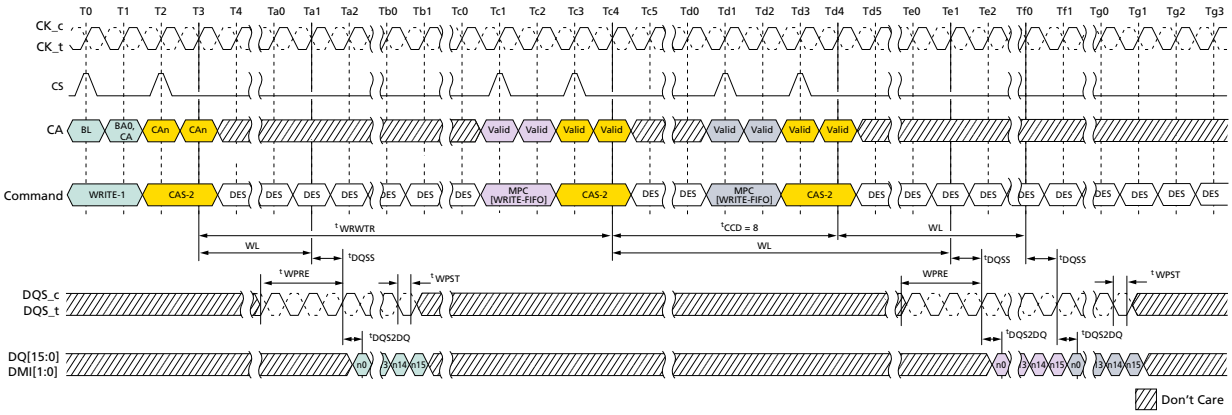
- Power-up initialization
- RESET_n asserted
- Power-down entry
- Self refresh power-down entry

The MPC[WRITE-FIFO] command advances the WRITE-FIFO pointer, and the MPC[READ-FIFO] advances the READ-FIFO pointer. Also any normal (non-FIFO) READ operation (RD, RDA) advances both WRITE-FIFO pointer and READ-FIFO pointer. Issuing (non-FIFO) READ operation command is inhibited during write training period. To keep the pointers aligned, the SoC memory controller must adhere to the following restriction at the end of Write training period:

$b = a + (n \times c)$

Where:
'a' is the number of MPC[WRITE-FIFO] commands
'b' is the number of MPC[READ-FIFO] commands
'c' is the FIFO depth (= 5 for LPDDR4)
'n' is a positive integer, ≥0

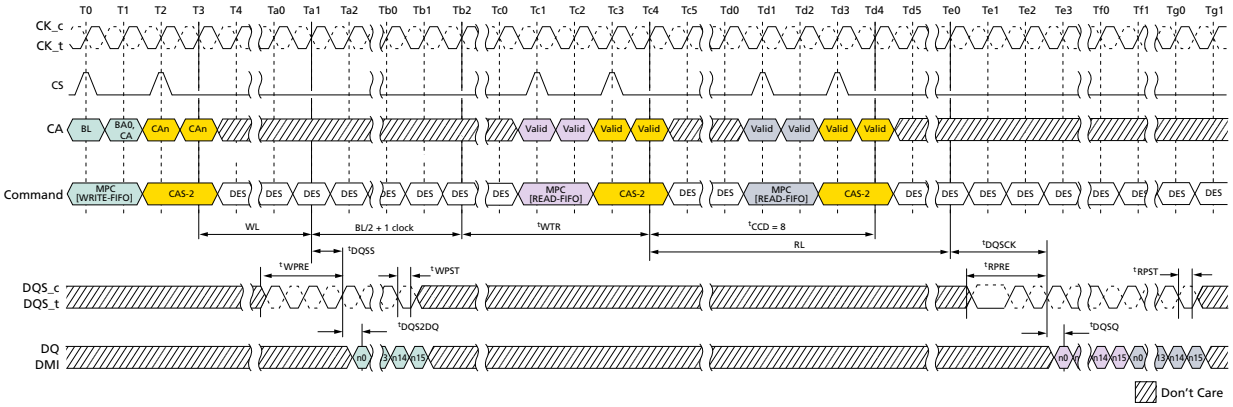
Figure 209: WRITE-to-MPC[WRITE-FIFO] Operation Timing



Notes: 1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active during REFRESH or during SELF REFRESH with CKE HIGH.
2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timing from Write-1 to MPC[WRITE-FIFO] is ^{t}WRWTR.
3. Seamless MPC[WR-FIFO] commands may be executed by repeating the command every^{t}CCD time.

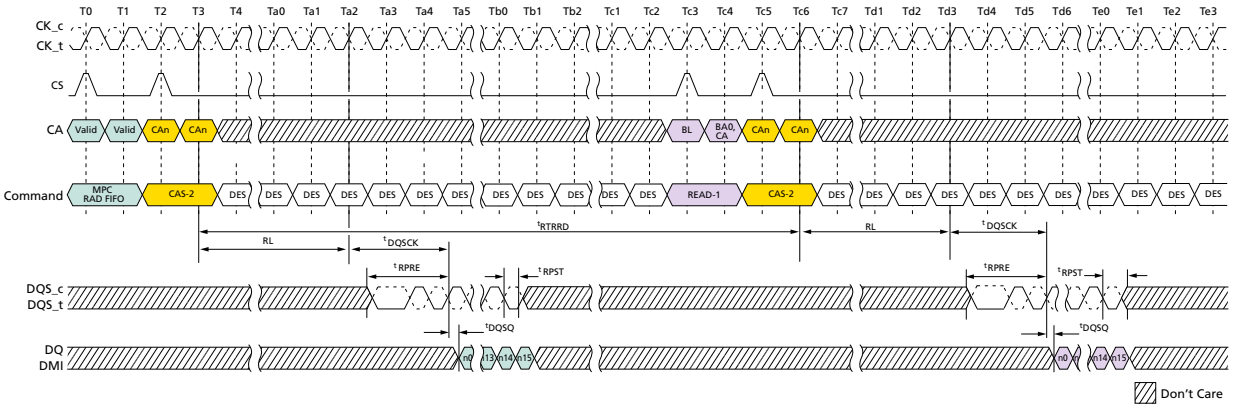
4. MPC[WRITE-FIFO] uses the same command-to-data timing relationship (WL, ^{t}DQSS, ^{t}DQS2DQ) as a WRITE-1 command.
5. A maximum of five MPC[WRITE-FIFO] commands may be executed consecutively without corrupting FIFO data. The sixth MPC[WRITE-FIFO] command will overwrite the FIFO data from the first command. If fewer than five MPC[WRITE-FIFO] commands are executed, then the remaining FIFO locations will contain undefined data.
6. For the CAS-2 command following an MPC command, the CAS-2 operands must be driven LOW.
7. To avoid corrupting the FIFO contents, MPC[READ-FIFO] must immediately follow MPC[WRITE-FIFO]/CAS-2 without any other commands disturbing FIFO pointers in between. FIFO pointers are disturbed by CKE LOW, WRITE, MASKED WRITE, READ, READ DQ CALIBRATION, and MRR.
8. BL = 16, Write postamble = 0.5*n*CK.
9. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 210: MPC[WRITE-FIFO]-to-MPC[READ-FIFO] Timing



Notes: 1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active during refresh or during self refresh with CKE HIGH.
2. MPC[WRITE-FIFO] to MPC[READ-FIFO] is shown as an example of command-to-command timing for MPC. Timing from MPC[WRITE-FIFO] to MPC[READ-FIFO] is specified in the command-to-command timing table.
3. Seamless MPC[READ-FIFO] commands may be executed by repeating the command every ^{t}CCD time.
4. MPC[READ-FIFO] uses the same command-to-data timing relationship (RL, ^{t}DQSCK, ^{t}DQSQ) as a READ-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After five MPC[READ-FIFO] commands, the FIFO pointer will wrap back to the first FIFO and continue advancing. If fewer than five MPC[WRITE-FIFO] commands were executed, then the MPC[READ-FIFO] commands to those FIFO locations will return undefined data. See Write Training for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following an MPC command, the CAS-2 operands must be driven LOW.
7. DMI[1:0] signals will be driven if WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.
8. BL = 16, Write postamble = 0.5*n*CK, Read preamble: Toggle, Read postamble: 0.5*n*CK.
9. DES commands are shown for ease of illustration; other commands may be valid at these times.

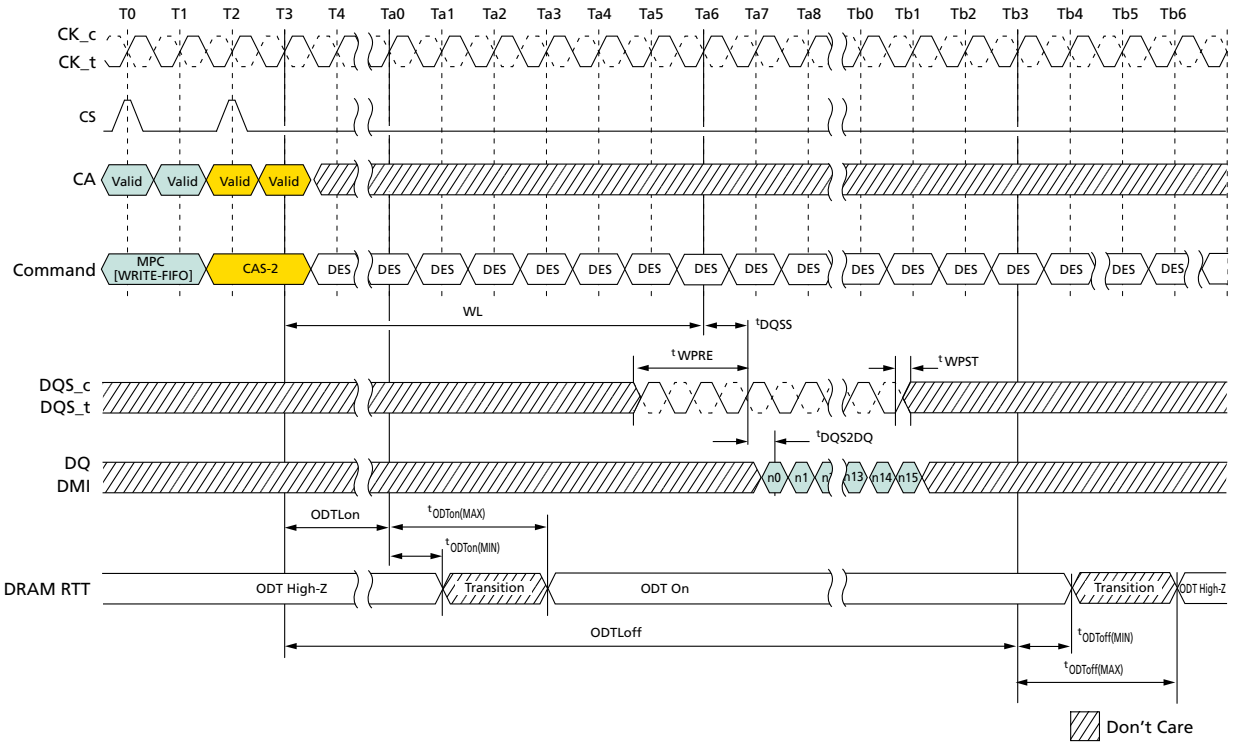
Figure 211: MPC[READ-FIFO] to Read Timing



Notes: 1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active during refresh or during self refresh with CKE HIGH.

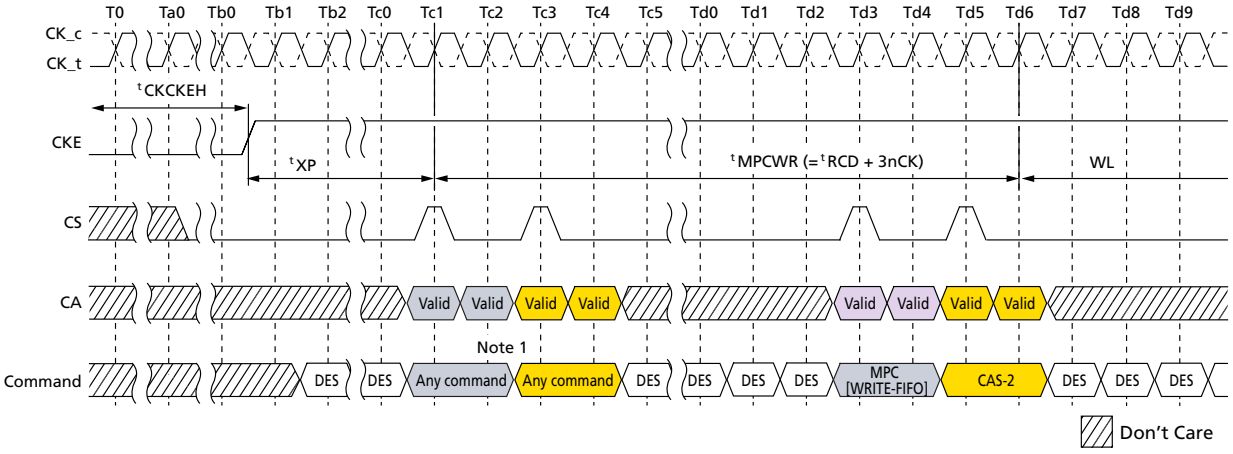
2. MPC[READ-FIFO] to READ-1 operation is shown as an example of command-to-command timing for MPC. Timing from MPC[READ-FIFO] command to READ is ^{t}RTRRD.
3. Seamless MPC[READ-FIFO] commands may be executed by repeating the command every ^{t}CCD time.
4. MPC[READ-FIFO] uses the same command-to-data timing relationship (RL, ^{t}DQSCK, ^{t}DQSQ) as a READ-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After five MPC[READ-FIFO] commands, the FIFO pointer will wrap back to the first FIFO and continue advancing. If fewer than five MPC[WRITE-FIFO] commands were executed, then the MPC[READ-FIFO] commands to those FIFO locations will return undefined data. See Write Training for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following an MPC command, the CAS-2 operands must be driven LOW.
7. DMI[1:0] signals will be driven if WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training for more information on DMI behavior.
8. BL = 16, Read preamble: Toggle, Read postamble: 0.5*n*CK
9. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 212: MPC[WRITE-FIFO] with DQ ODT Timing



Notes: 1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active during refresh or during self refresh with CKE HIGH.
2. MPC[WRITE-FIFO] uses the same command-to-data/ODT timing relationship (RL, ^{t}DQSCK, ^{t}DQS2DQ, ODTLon, ODTLoff, ^{t}ODTon, ^{t}ODToff) as a WRITE-1 command.
3. For the CAS-2 command immediately following an MPC command, the CAS-2 operands must be driven LOW.
4. BL = 16, Write postamble = 0.5*n*CK.
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 213: Power-Down Exit to MPC[WRITE-FIFO] Timing



Notes: 1. Any commands except MPC[WRITE-FIFO] and other exception commands defined other section in this document (for example. MPC[READ DQ CALIBRATION]).
2. DES commands are shown for ease of illustration; other commands may be valid at these times.

Table 171: MPC[WRITE-FIFO] AC Timing

Parameter	Symbol	MinMax	Value	Unit
Additional time after ^{t}XP has expired until MPC[WRITE-FIFO] command may be issued	^{t}MPCWR	MIN	^{t}RCD + 3*n*CK	–

Internal Interval Timer

As voltage and temperature change on the device, the DQS clock-tree delay will shift, requiring retraining. The device includes an internal DQS clock-tree oscillator to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The DQS oscillator will provide the controller with important information regarding the need to retrain and the magnitude of potential error.

The DQS interval oscillator is started by issuing an MPC command with OP[6:0] set as described in MPC Operation, which will start an internal ring oscillator that counts the number of time a signal propagates through a copy of the DQS clock tree.

The DQS oscillator may be stopped by issuing an MPC[STOP DQS OSCILLATOR] command with OP[6:0] set as described in MPC Operation, or the controller may instruct the SDRAM to count for a specific number of clocks and then stop automatically (See MR23 for more information). If MR23 is set to automatically stop the DQS oscillator, then the MPC[STOP DQS OSCILLATOR] command should not be used (illegal). When the DQS oscillator is stopped by either method, the result of the oscillator counter is automatically stored in MR18 and MR19.

The controller may adjust the accuracy of the result by running the DQS interval oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation, where run time = total time between START and STOP commands and DQS delay = the value of the DQS clock tree delay (^{t}DQS2DQ(MIN)/(MAX)):

$$\text{DQS oscillator granularity error} = \frac{2 \times (\text{DQS delay})}{\text{run time}}$$

Additional matching error must be included, which is the difference between DQS training circuit and the actual DQS clock tree across voltage and temperature. The matching error is vendor specific. Therefore, the total accuracy of the DQS oscillator counter is given by:

$$\text{DQS oscillator accuracy} = 1 - \text{granularity error} - \text{matching error}$$

For example, if the total time between START and STOP commands is 100ns, and the maximum DQS clock tree delay is 800ps (^{t}DQS2DQ(MAX)), then the DQS oscillator granularity error is:

$$\text{DQS oscillator granularity error} = \frac{2 \times (0.8\text{ns})}{100\text{ns}} = 1.6\%$$

This equates to a granularity timing error of 12.8ps. Assuming a circuit matching error of 5.5ps across voltage and temperature, the accuracy is:

$$\text{DQS oscillator accuracy} = 1 - \frac{12.8 + 5.5}{800} = 97.7\%$$

For example, running the DQS oscillator for a longer period improves the accuracy. If the total time between START and STOP commands is 500ns, and the maximum DQS clock tree delay is 800ps (^{t}DQS2DQ(MAX)), then the DQS oscillator granularity error is:

$$\text{DQS oscillator granularity error} = \frac{2 \times (0.8\text{ns})}{500\text{ns}} = 0.32\%$$

This equates to a granularity timing error or 2.56ps. Assuming a circuit matching error of 5.5ps across voltage and temperature, the accuracy is:

$$\text{DQS oscillator accuracy} = 1 - \frac{2.56 + 5.5}{800} = 99.0\%$$

The result of the DQS interval oscillator is defined as the number of DQS clock tree delays that can be counted within the run time, determined by the controller. The result is stored in MR18-OP[7:0] and MR19-OP[7:0].

MR18 contains the least significant bits (LSB) of the result, and MR19 contains the most significant bits (MSB) of the result. MR18 and MR19 are overwritten by the SDRAM when a MPC[STOP DQS OSCILLATOR] command is received.

The SDRAM counter will count to its maximum value (= 2^16) and stop. If the maximum value is read from the mode registers, the memory controller must assume that the counter overflowed the register and therefore discard the result. The longest run time for the oscillator that will not overflow the counter registers can be calculated as follows:

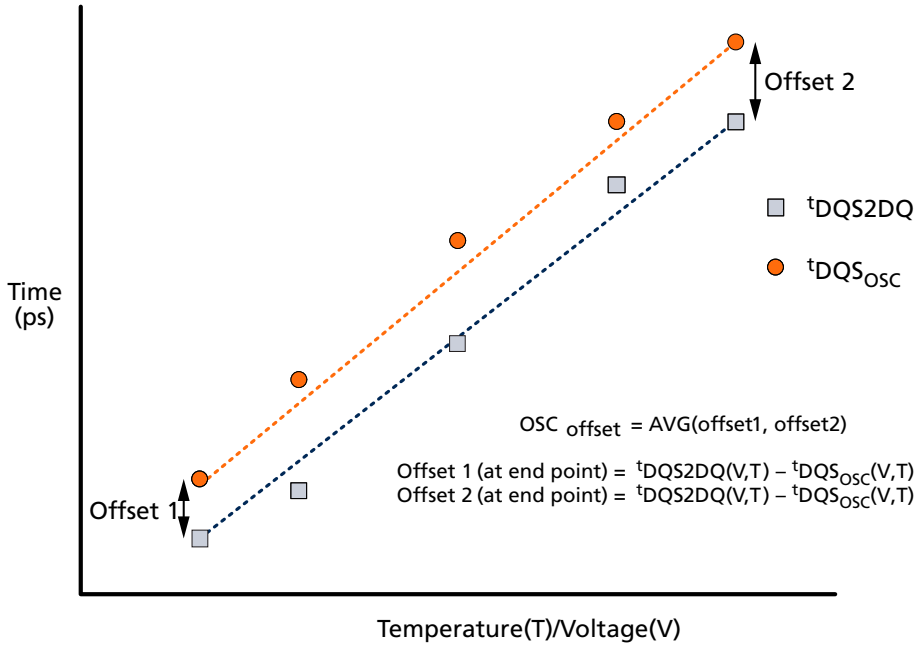
$$\text{Longest runtime interval} = 2^{16} \times {}^{t}\text{DQS2DQ(MIN)} = 2^{16} \times 0.2\text{ns} = 13.1\mu\text{s}$$

DQS Interval Oscillator Matching Error

The interval oscillator matching error is defined as the difference between the DQS training ckt (interval oscillator) and the actual DQS clock tree across voltage and temperature.

Parameters:
^{t}DQS2DQ: Actual DQS clock tree delay
${}^{t}\text{DQS}_{\text{OSC}}$: Training ckt (interval oscillator) delay
$\text{OSC}_{\text{Offset}}$: Average delay difference over voltage and temperature (shown below)
$\text{OSC}_{\text{Match}}$: DQS oscillator matching error

Figure 214: Interval Oscillator Offset – $\text{OSC}_{\text{offset}}$



$\text{OSC}_{\text{Match}}$:

$$OSC_{Match} = [\ {}^{t}DQS2DQ(V,T) - {}^{t}DQS_{OSC}(V,T) - OSC_{offset}\ ]$$

$${}^{t}DQS_{OSC}:$$

$${}^{t}DQS_{OSC}(V,T) = [\ \frac{Runtime}{2 \times Count}\ ]$$

Table 172: DQS Oscillator Matching Error Specification

Parameter	Symbol	Min	Max	Unit	Notes
DQS oscillator matching error	OSC_{Match}	–20	20	ps	1, 2, 3, 4, 5, 6, 7, 8
DQS oscillator offset	OSC_{offset}	–100	100	ps	2, 4. 7

Notes: 1. The OSC_{Match} is the matching error per between the actual DQS and DQS interval oscillator over voltage and temperature.
2. This parameter will be characterized or guaranteed by design.
3. The OSC_{Match} is defined as the following:

$$OSC_{Match} = [\ {}^{t}DQS2DQ_{(V,\ T)} - {}^{t}DQS_{OSC(V,\ T)} - OSC_{offset}\ ]$$

Where ${}^{t}DQS2DQ(V,T)$ and ${}^{t}DQS_{OSC}(V,T)$ are determined over the same voltage and temperature conditions.
4. The runtime of the oscillator must be at least 200ns for determining ${}^{t}DQS_{OSC}(V,T)$.

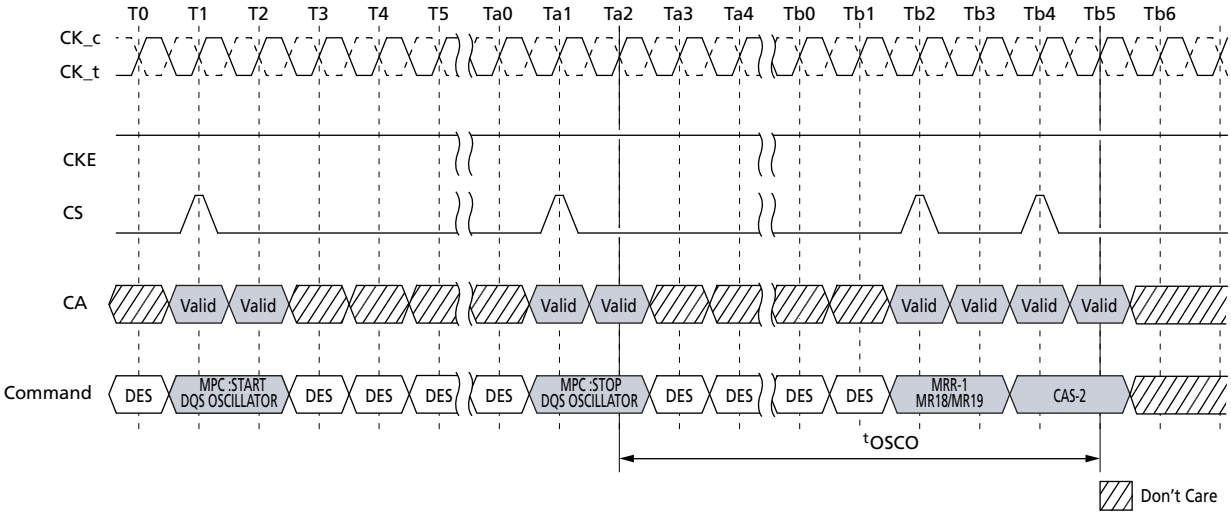
$${}^{t}DQS_{OSC}(V,T) = [\ \frac{Runtime}{2 \times Count}\ ]$$

5. The input stimulus for ${}^{t}DQS2DQ$ will be consistent over voltage and temperature conditions.
6. The OSC_{offset} is the average difference of the endpoints across voltage and temperature.
7. These parameters are defined per channel.
8. ${}^{t}DQS2DQ(V,T)$ delay will be the average of DQS-to-DQ delay over the runtime period.

OSC Count Readout Time

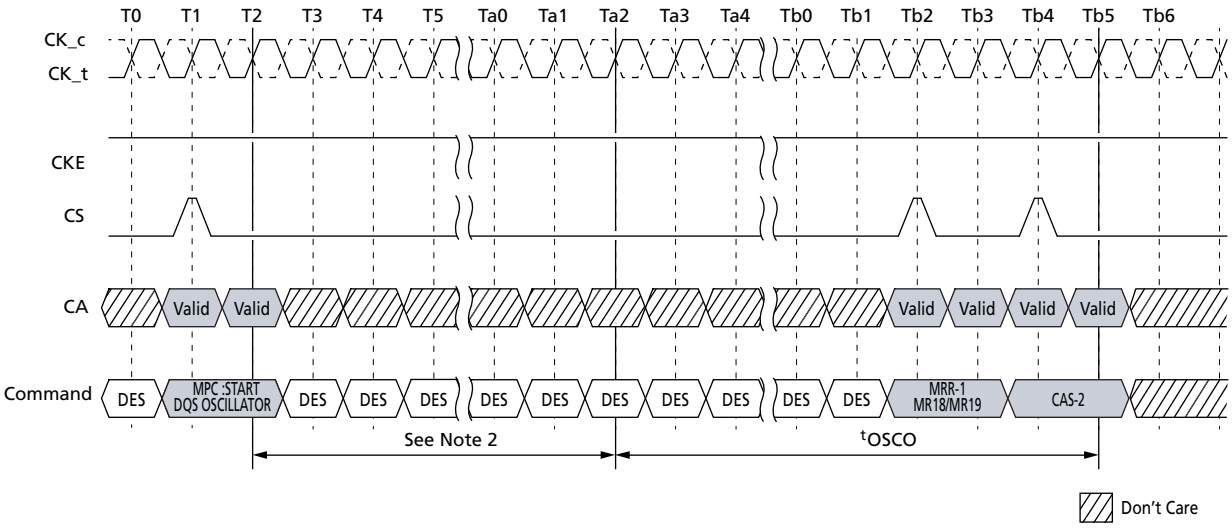
OSC Stop to its counting value readout timing is shown in following figures.

Figure 215: In Case of DQS Interval Oscillator is Stopped by MPC Command



Note: 1. DQS interval timer run time setting: MR23 OP[7:0] = 00000000b.

Figure 216: In Case of DQS Interval Oscillator is Stopped by DQS Interval Timer



Notes: 1. DQS interval timer run time setting: MR23 OP[7:0] = 00000000b.
2. Setting counts of MR23.

Table 173: DQS Interval Oscillator AC Timing

Parameter	Symbol	Min/Max	Value	Unit
Delay time from OSC stop to mode register readout	^{t}OSCO	MIN	MAX(40ns, 8*n*CK)	ns

Note: 1. START DQS OSCILLATOR command is prohibited until ^{t}OSCO(MIN) is satisfied.

Thermal Offset

Because of tight thermal coupling, hot spots on an SOC can induce thermal gradients across the device. Because these hot spots may not be located near the thermal sensor, the temperature compensated self refresh (TCSR) circuit may not generate enough refresh cycles to guarantee memory retention. To address this shortcoming, the controller can provide a thermal offset that the memory can use to adjust its TCSR circuit to ensure reliable operation.

This thermal offset is provided through MR4 OP[6:5] to either or both channels (dual-channel devices). This temperature offset may modify refresh behaviour for the channel to which the offset is provided. It will take a maximum of 200µs to have the change reflected in MR4 OP[2:0] for the channel to which the offset is provided. If the induced thermal gradient from the device temperature sensor location to the hot spot location of the controller is greater than 15°C, self refresh mode will not reliably maintain memory contents.

To accurately determine the temperature gradient between the memory thermal sensor and the induced hot spot, the memory thermal sensor location must be provided to the controller.

Temperature Sensor

The device has a temperature sensor that can be read from MR4. This sensor can be used to determine the appropriate refresh rate, to determine whether AC timing de-rating is required at an elevated temperature range, and to monitor the operating temperature. Either the temperature sensor or the device T_{OPER} can be used to determine if operating temperature requirements are being met.

The device monitors device temperature and updates MR4 according to ^{t}TSI. Upon exiting self refresh or power-down, the device temperature status bits shall be no older than ^{t}TSI.

When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} specification that applies to standard or elevated temperature ranges. For example, T_{CASE} may be above 85°C when MR4[2:0] = b011. The device enables a 2°C temperature margin between the point when the device updates the MR4 value and the point when the controller reconfigures the system accordingly. When performing tight thermal coupling of the device to external hot spots, the maximum device temperature may be higher than indicated by MR4.

To ensure proper operation when using the temperature sensor, consider the following:

- TempGradient is the maximum temperature gradient experienced by the device at the temperature of interest over a range of 2°C.
- ReadInterval is the time period between MR4 reads from the system.
- TempSensorInterval (^{t}TSI) is the maximum delay between the internal updates of MR4.
- SysRespDelay is the maximum time between a read of MR4 and a response from the system.

In order to determine the required frequency of polling MR4, the system uses the TempGradient and the maximum response time of the system in the following equation:

TempGradient × (ReadInterval + ^{t}TSI + SysRespDelay) ≤ 2°C

Table 174: Temperature Sensor

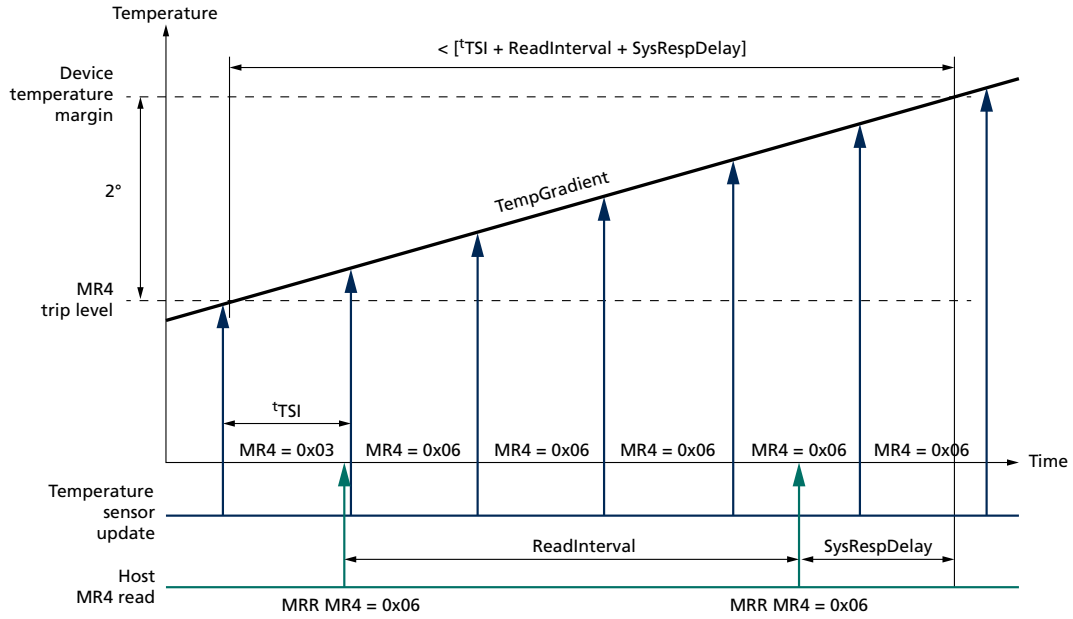
Parameter	Symbol	Max/Min	Value	Unit
System temperature gradient	TempGradient	MAX	System Dependent	°C/s
MR4 read interval	ReadInterval	MAX	System Dependent	ms
Temperature sensor interval	^{t}TSI	MAX	32	ms
System response delay	SysRespDelay	MAX	System Dependent	ms
Device temperature margin	TempMargin	MAX	2	°C

For example, if TempGradient is 10°C/s and the SysRespDelay is 1ms:

(10°C/s) x (ReadInterval + 32ms + 1ms) ≤ 2°C

In this case, ReadInterval shall be no greater than 167ms.

Figure 217: Temperature Sensor Timing



ZQ Calibration

The MPC command is used to initiate ZQ calibration, which calibrates the output driver impedance and CA/DQ ODT impedance across process, temperature, and voltage. ZQ calibration occurs in the background of device operation and is designed to eliminate any need for coordination between channels (that is, it allows for channel independence). ZQ calibration is required each time that the PU-Cal value (MR3-OP[0]) is changed. Additional ZQ CALIBRATION commands may be required as the voltage and temperature change in the system environment. CA ODT values (MR11-OP[6:4]) and DQ ODT values (MR11-OP[2:0]) may be changed without performing ZQ calibration, as long as the PU-Cal value doesn't change.

There are two ZQ calibration modes initiated with the MPC command: ZQCAL START and ZQCAL LATCH. ZQCAL START initiates the calibration procedure, and ZQCAL LATCH captures the result and loads it into the drivers.

A ZQCAL START command may be issued anytime the device is not in a power-down state. A ZQCAL LATCH command may be issued anytime outside of power-down after ^{t}ZQCAL has expired and all DQ bus operations have completed. The CA bus must maintain a deselect state during ^{t}ZQLAT to allow

CA ODT calibration settings to be updated. The DQ calibration value will not be updated until ZQCAL LATCH is performed and ^{t}ZQLAT has been met. The following mode register fields that modify I/O parameters cannot be changed following a ZQCAL START command and before ^{t}ZQCAL has expired:

- PU-Cal (pull-up calibration V_{OH} point)
- PDDS (pull-down drive strength and Rx termination)
- DQ ODT (DQ ODT value)
- CA ODT (CA ODT value)

ZQCAL Reset

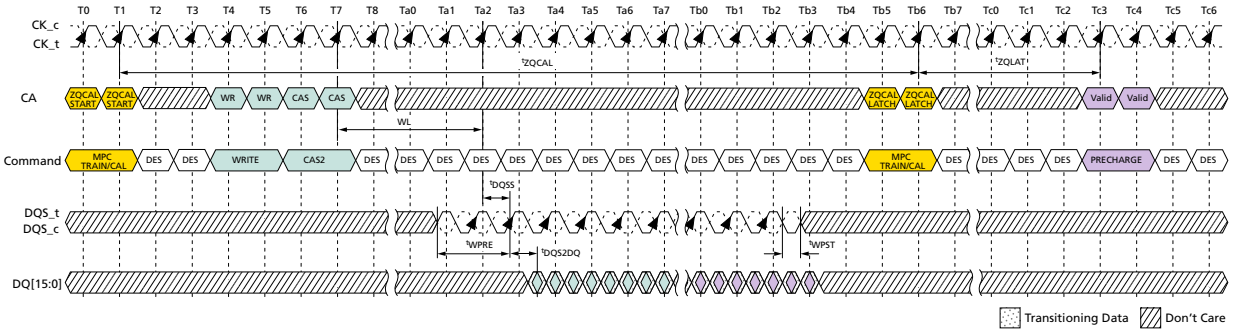
The ZQCAL RESET command resets the output impedance calibration to a default accuracy of ±30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to ±30% when ZQCAL START and ZQCAL LATCH commands are not used.

The ZQCAL RESET command is executed by writing MR10-OP[0] = 1B.

Table 175: ZQ Calibration Parameters

Parameter	Symbol	Min/Max	Value	Unit
ZQCAL START to ZQCAL LATCH command interval	^{t}ZQCAL	MIN	1	µs
ZQCAL LATCH to next valid command interval	^{t}ZQLAT	MIN	MAX(30ns, 8*n*CK)	ns
ZQCAL RESET to next valid command interval	^{t}ZQRESET	MIN	MAX(50ns, 3*n*CK)	ns

Figure 218: ZQCAL Timing



Notes: 1. WRITE and PRECHARGE operations are shown for illustrative purposes. Any single or multiple valid commands may be executed within the ^{t}ZQCAL time and prior to latching the results.

2. Before the ZQCAL LATCH command can be executed, any prior commands that utilize the DQ bus must have completed. WRITE commands with DQ termination must be given enough time to turn off the DQ ODT before issuing the ZQCAL LATCH command. See the ODT section for ODT timing.

Multichannel Considerations

The device includes a single ZQ pin and associated ZQ calibration circuitry. Calibration values from this circuit will be used by both channels according to the following protocol:

- The ZQCAL START command can be issued to either or both channels.
- The ZQCAL START command can be issued when either or both channels are executing other commands, and other commands can be issued during ^{t}ZQCAL.
- The ZQCAL START command can be issued to both channels simultaneously.
- The ZQCAL START command will begin the calibration unless a previously requested ZQ calibration is in progress.
- If the ZQCAL START command is received while a ZQ calibration is in progress, the command will be ignored and the in-progress calibration will not be interrupted.

- The ZQCAL LATCH command is required for each channel.
- The ZQCAL LATCH command can be issued to both channels simultaneously.
- The ZQCAL LATCH command will latch results of the most recent ZQCAL START command provided ^{t}ZQCAL has been met.
- ZQCAL LATCH commands that do not meet ^{t}ZQCAL will latch the results of the most recently completed ZQ calibration.
- The ZQRESET MRW commands will only reset the calibration values for the channel issuing the command.

In compliance with complete channel independence, either channel may issue ZQCAL START and ZQCAL LATCH commands as needed without regard to the state of the other channel.

ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ CALIBRATION function, a 240 ohms, ±1% tolerance external resistor must be connected between the ZQ pin and V_{DDQ}.

If the system configuration shares the CA bus to form a x32 (or wider) channel, the ZQ pin of each die's x16 channel must use a separate ZQCAL resistor.

If the system configuration has more than one rank, and if the ZQ pins of both ranks are attached to a single resistor, then the SDRAM controller must ensure that the ZQCAL's don't overlap.

The total capacitive loading on the ZQ pin must be limited to 25pF. For example, if a system configuration shares a CA bus between *n* channels to form an *n* x16 wide bus, and no means are available to control the ZQCAL separately for each channel (that is, separate CS, CKE, or CK), then each x16 channel must have a separate ZQCAL resistor. For a x32, two-rank system, each x16 channel must have its own ZQCAL resistor, but the ZQCAL resistor can be shared between ranks on each x16 channel. In this configuration, the CS signal can be used to ensure that the ZQCAL commands for Rank[0] and Rank[1] don't overlap.

Frequency Set Points

Frequency set points enable the CA bus to be switched between two differing operating frequencies with changes in voltage swings and termination values, without ever being in an untrained state, which could result in a loss of communication to the device. This is accomplished by duplicating all CA bus mode register parameters, as well as other mode register parameters commonly changed with operating frequency.

These duplicated registers form two sets that use the same mode register addresses, with read/write access controlled by MR bit FSP-WR (frequency set point write/read) and the operating point controlled by MR bit FSP-OP (FREQUENCY SET POINT operation). Changing the FSP-WR bit enables MR parameters to be changed for an alternate frequency set point without affecting the current operation.

Once all necessary parameters have been written to the alternate set point, changing the FSP-OP bit will switch operation to use all of the new parameters simultaneously (within ^{t}FC), eliminating the possibility of a loss of communication that could be caused by a partial configuration change.

Parameters that have two physical registers controlled by FSP-WR and FSP-OP include those in the following table.

Table 176: Mode Register Function With Two Physical Registers

MR Number	Operand	Function	Notes
MR1	OP[2]	WR-PRE (Write preamble length)	
	OP[3]	RD-PRE (Read preamble type)	
	OP[6:4]	*n*WR (Write-recovery for AUTO PRECHARGE command)	
	OP[7]	RD-PST (Read postamble length)	
MR2	OP[2:0]	RL (READ latency)	
	OP[5:3]	WL (WRITE latency)	
	OP[6]	WLS (WRITE latency set)	
MR3	OP[0]	PU-CAL (Pull-up calibration point)	1
	OP[1]	WR-PST(Write postamble length)	
	OP[5:3]	PDDS (Pull-down drive strength)	
	OP[6]	DBI-RD (DBI-read enable)	
	OP[7]	DBI-WR (DBI-write enable)	
MR11	OP[2:0]	DQ ODT (DQ bus receiver on-die termination)	
	OP[6:4]	CA ODT (CA bus receiver on-die termination)	
MR12	OP[5:0]	$V_{REF(CA)}$ ($V_{REF(CA)}$ setting)	
	OP[6]	VR_{CA} ($V_{REF(CA)}$ range)	
MR14	OP[5:0]	$V_{REF(DQ)}$ ($V_{REF(DQ)}$ setting)	
	OP[6]	VR_{DQ} ($V_{REF(DQ)}$ range)	
MR22	OP[2:0]	SOC ODT (Controller ODT value for V_{OH} calibration)	
	OP[3]	ODTE-CK (CK ODT enabled for non-terminating rank)	
	OP[4]	ODTE-CS (CS ODT enable for non-terminating rank)	
	OP[5]	ODTD-CA (CA ODT termination disable)	

Note: 1. For dual-channel devices, PU-CAL setting is required as the same value for both Ch.A and Ch.B before issuing ZQCAL START command. See Mode Register Definition section for more details.

The table below shows how the two mode registers for each of the parameters in the previous table can be modified by setting the appropriate FSP-WR value and how device operation can be switched between operating points by setting the appropriate FSP-OP value. The FSP-WR and FSP-OP functions operate completely independently.

Table 177: Relation Between MR Setting and DRAM Operation

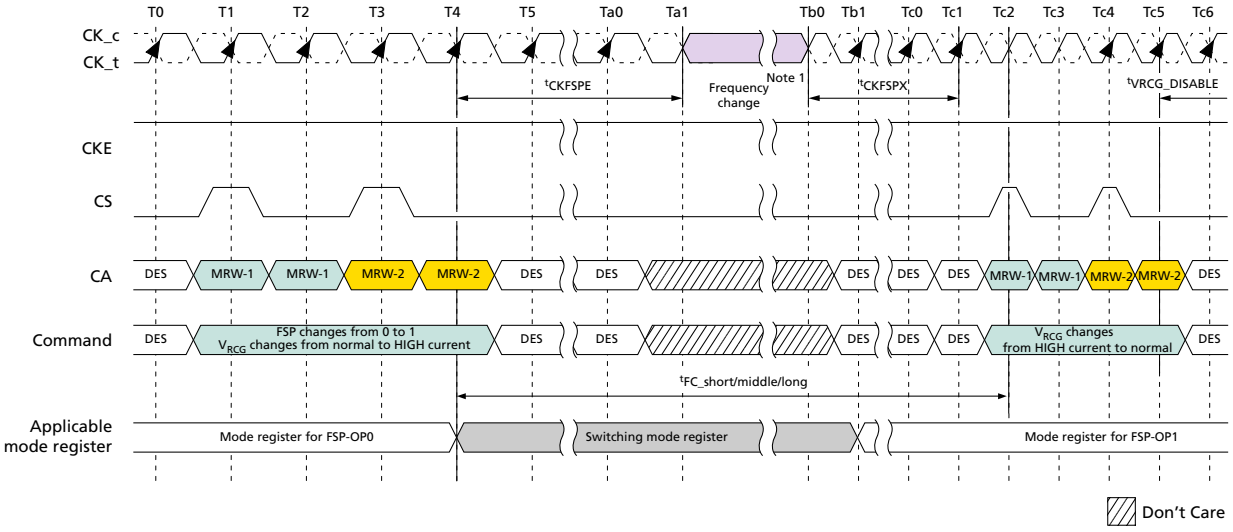
Function	MR# and Operand	Data	Operation	Notes
FSP-WR	MR13 OP[6]	0 (default)	Data write to mode register N for FSP-OP[0] by MRW command.	1
			Data read from mode register N for FSP-OP[0] by MRR command.	
		1	Data write to mode register N for FSP-OP[1] by MRW command.	
			Data read from mode register N for FSP-OP[1] by MRR command.	
FSP-OP	MR13 OP[7]	0 (default)	DRAM operates with mode register N for FSP-OP[0] setting.	2
		1	DRAM operates with mode register N for FSP-OP[1] setting.	

Notes: 1. FSP-WR stands for frequency set point write/read.
2. FSP-OP stands for frequency set point operating point.

Frequency Set Point Update Timing

The frequency set point update timing is shown below. When changing the frequency set point via MR13 OP[7], the V_{RCG}setting: MR13 OP[3] have to be changed into V_{REF} fast response (high current) mode at the same time. After frequency change time (^{t}FC) is satisfied. V_{RCG} can be changed into normal operation mode via MR13 OP[3].

Figure 219: Frequency Set Point Switching Timing



Note: 1. For frequency change during frequency set point switching, refer to Input Clock Stop and Frequency Change section.

Table 178: Frequency Set Point AC Timing

Parameter	Symbol	Min/ Max	Data Rate				Unit	Notes
			1600	3200	3733	4267		
Frequency set point switching time	tFC_short	MIN	200				ns	1
	tFC_middle	MIN	200				ns	
	tFC_long	MIN	250				ns	
Valid clock requirement after entering FSP change	tCKFSPE	MIN	MAX(7.5ns, 4*n*CK)				–	
Valid clock requirement before first valid command after FSP change	tCKFSPX	MIN	MAX(7.5ns, 4*n*CK)				–	

Note: 1. Frequency set point switching time depends on value of $V_{REF(CA)}$ setting: MR12 OP[5:0] and $V_{REF(CA)}$ range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in table below. Additionally change of frequency set point may affect $V_{REF(DQ)}$ setting. Settling time of $V_{REF(DQ)}$ level is the same as $V_{REF(CA)}$ level.

Table 179: tFC Value Mapping

Application	Step Size		Range	
	From FSP-OP0	To FSP-OP1	From FSP -OP0	To FSP-OP1
tFC_short	Base	A single step size increment/decrement	Base	No change
tFC_middle	Base	Two or more step size increment/decrement	Base	No change
tFC_long	–	–	Base	Change

Note: 1. As well as change from FSP-OP1 to FSP-OP0.

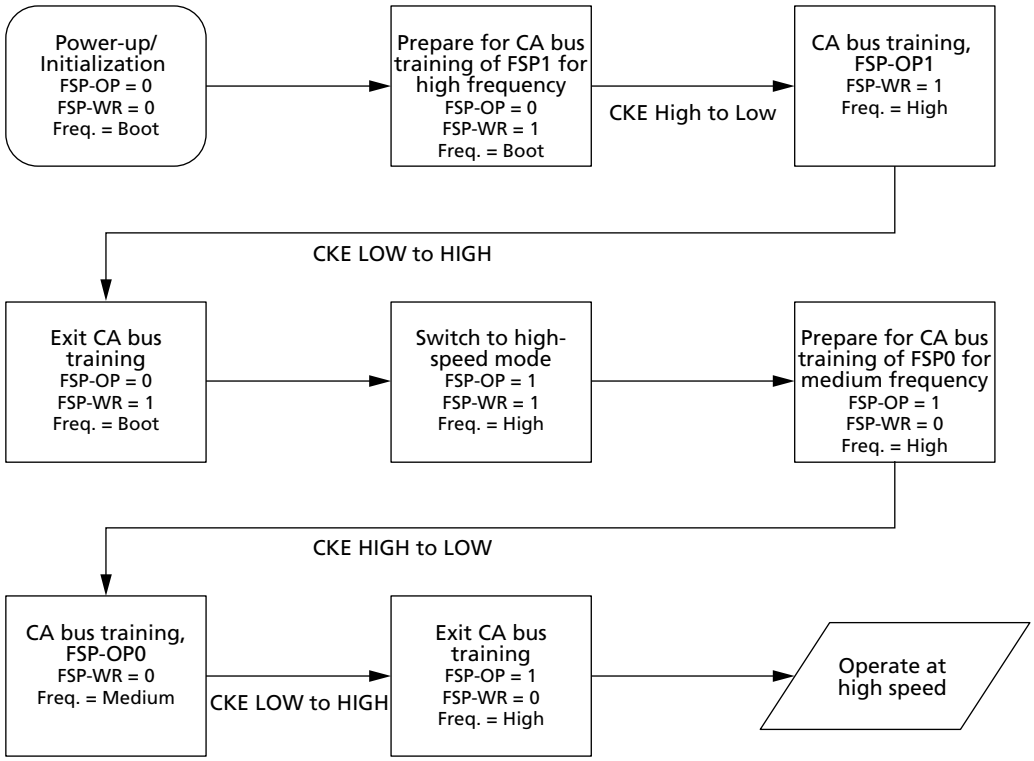
Table 180: tFC Value Mapping: Example

Case	From/To	FSP-OP: MR13 OP[7]	$V_{REF(CA)}$ Setting: MR12: OP[5:0]	$V_{REF(CA)}$ Range: MR12 OP[6]	Application	Notes
1	From	0	001100	0	tFC_short	1
	To	1	001101	0		
2	From	0	001100	0	tFC_middle	2
	To	1	001110	0		
3	From	0	Don't Care	0	tFC_long	3
	To	1	Don't Care	1		

Notes: 1. A single step size increment/decrement for $V_{REF(CA)}$ setting value.
2. Two or more step size increment/decrement for $V_{REF(CA)}$ setting value.
3. $V_{REF(CA)}$ range is changed. In this case, changing $V_{REF(CA)}$ setting doesn't affect tFC value.

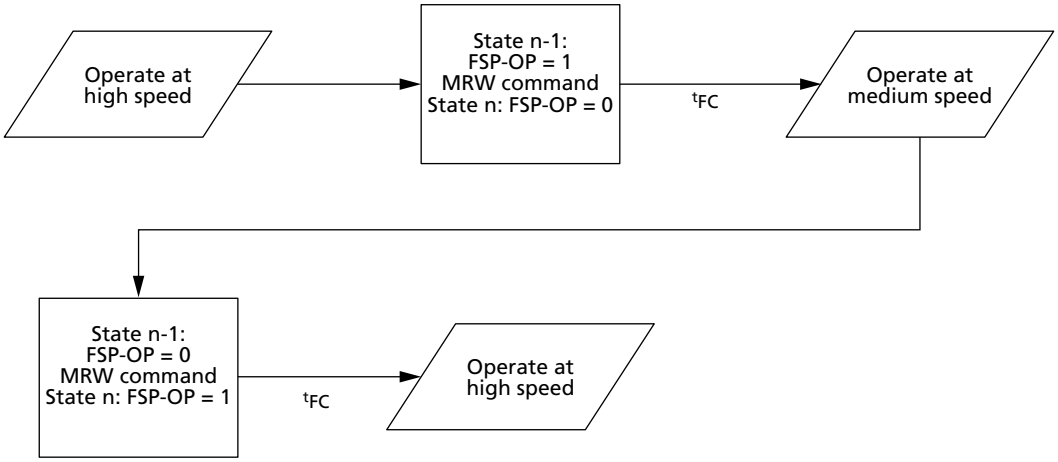
The LPDDR4 SDRAM defaults to FSP-OP[0] at power-up. Both set points default to settings needed to operate in un-terminated, low-frequency environments. To enable the device to operate at higher frequencies, Command bus training mode should be utilized to train the alternate frequency set point. See Command Bus Training section for more details on this training mode.

Figure 220: Training for Two Frequency Set Points



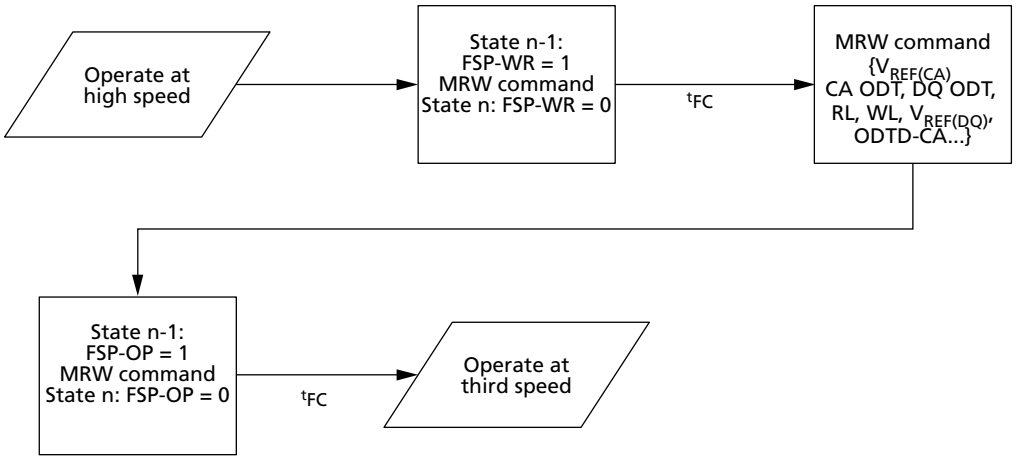
Once both of the frequency set points have been trained, switching between points can be performed with a single MRW followed by waiting for time ^{t}FC.

Figure 221: Example of Switching Between Two Trained Frequency Set Points



Switching to a third (or more) set point can be accomplished if the memory controller has stored the previously-trained values (in particular the $V_{REF(CA)}$ calibration value) and rewrites these to the alternate set point before switching FSP-OP.

Figure 222: Example of Switching to a Third Trained Frequency Set Point



Pull-Up and Pull-Down Characteristics and Calibration

Table 181: Pull-Down Driver Characteristics – ZQ Calibration

$R_{ONPD,nom}$	Register	Min	Nom	Max	Unit
40 ohms	R_{ON40PD}	0.90	1.0	1.10	$R_{ZQ}/6$
48 ohms	R_{ON48PD}	0.90	1.0	1.10	$R_{ZQ}/5$
60 ohms	R_{ON60PD}	0.90	1.0	1.10	$R_{ZQ}/4$
80 ohms	R_{ON80PD}	0.90	1.0	1.10	$R_{ZQ}/3$
120 ohms	$R_{ON120PD}$	0.90	1.0	1.10	$R_{ZQ}/2$
240 ohms	$R_{ON240PD}$	0.90	1.0	1.10	$R_{ZQ}/1$

Note: 1. All value are after ZQ calibration. Without ZQ calibration, R_{ONPD} values are ±30%.

Table 182: Pull-Up Characteristics – ZQ Calibration

$V_{OHPU,nom}$	$V_{OH,nom}$	Min	Nom	Max	Unit
V_{DDQ} × 0.5	300	0.90	1.0	1.10	$V_{OH,nom}$
V_{DDQ} × 0.6	360	0.90	1.0	1.10	$V_{OH,nom}$

Notes: 1. All value are after ZQ calibration. Without ZQ calibration, R_{ONPD} values are ±30%.
2. $V_{OH,nom}$ (mV) values are based on a nominal V_{DDQ} = 0.6V.

Table 183: Valid Calibration Points

V_{OHPU}	ODT Value					
	240	120	80	60	48	40
V_{DDQ} × 0.5	Valid	Valid	Valid	Valid	Valid	Valid
V_{DDQ} × 0.6	DNU	Valid	DNU	Valid	DNU	DNU

Notes: 1. After the output is calibrated for a given $V_{OH,nom}$ calibration point, the ODT value may be changed without recalibration.
2. If the $V_{OH,nom}$ calibration point is changed, then recalibration is required.
3. DNU = Do not use.

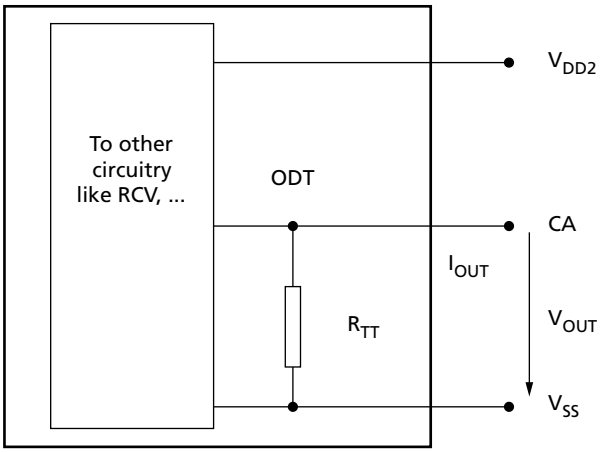
On-Die Termination for the Command/Address Bus

The on-die termination (ODT) feature allows the device to turn on/off termination resistance for CK_t, CK_c, CS, and CA[5:0] signals without the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via the mode register setting.

A simple functional representation of the DRAM ODT feature is shown below.

Figure 223: ODT for CA

$$R_{TT} = \frac{V_{OUT}}{|I_{OUT}|}$$



ODT Mode Register and ODT State Table

ODT termination values are set and enabled via MR11. The CA bus (CK_t, CK_c, CS, CA[5:0]) ODT resistance values are set by MR11 OP[6:4]. The default state for the CA is ODT disabled.

ODT is applied on the CA bus to the CK_t, CK_c, CS, and CA signals. Generally only one termination load will be present even if multiple devices are sharing the command signals. In contrast to LPDDR4 where the ODT_CA input is used in combination with mode registers, LPDDR4X uses mode registers exclusively to enable CA termination. Before enabling CA termination via MR11, all ranks should have appropriate MR22 termination settings programmed. In a multi rank system, the terminating rank should be trained first, followed by the non-terminating rank(s).

Table 184: Command Bus ODT State

CA ODT MR11[6:4]	ODTD-CA MR22 OP[5]	ODTE-CK MR22 OP[3]	ODTE-CS MR22 OP[4]	ODT State for CA	ODT State for CK	ODT State for CS
Disabled[1]	Valid[2]	Valid[2]	Valid[2]	Off	Off	Off
Valid[2]	0	0	0	On	On	On
Valid[2]	0	0	1	On	On	Off
Valid[2]	0	1	0	On	Off	On
Valid[2]	0	1	1	On	Off	Off
Valid[2]	1	0	0	Off	On	On
Valid[2]	1	0	1	Off	On	Off
Valid[2]	1	1	0	Off	Off	On
Valid[2]	1	1	1	Off	Off	Off

Notes: 1. Default value
2. Valid = 0 or 1

ODT Mode Register and ODT Characteristics

Table 185: ODT DC Electrical Characteristics for Command/Address Bus

MR11 OP[6:4]	R_{TT}	V_{OUT}	Min	Nom	Max	Unit	Notes
001b	240Ω	$V_{OL(DC)} = 0.2 \times V_{DDQ}$	0.8	1.0	1.1	$R_{ZQ}/1$	1, 2
		$V_{OM(DC)} = 0.50 \times V_{DDQ}$	0.9	1.0	1.1		
		$V_{OH(DC)} = 0.75 \times V_{DDQ}$	0.9	1.0	1.3		
010b	120Ω	$V_{OL(DC)} = 0.2 \times V_{DDQ}$	0.8	1.0	1.1	$R_{ZQ}/2$	1, 2
		$V_{OM(DC)} = 0.50 \times V_{DDQ}$	0.9	1.0	1.1		
		$V_{OH(DC)} = 0.75 \times V_{DDQ}$	0.9	1.0	1.3		
011b	80Ω	$V_{OL(DC)} = 0.2 \times V_{DDQ}$	0.8	1.0	1.1	$R_{ZQ}/3$	1, 2
		$V_{OM(DC)} = 0.50 \times V_{DDQ}$	0.9	1.0	1.1		
		$V_{OH(DC)} = 0.75 \times V_{DDQ}$	0.9	1.0	1.3		
100b	60Ω	$V_{OL(DC)} = 0.2 \times V_{DDQ}$	0.8	1.0	1.1	$R_{ZQ}/4$	1, 2
		$V_{OM(DC)} = 0.50 \times V_{DDQ}$	0.9	1.0	1.1		
		$V_{OH(DC)} = 0.75 \times V_{DDQ}$	0.9	1.0	1.3		
101b	48Ω	$V_{OL(DC)} = 0.2 \times V_{DDQ}$	0.8	1.0	1.1	$R_{ZQ}/5$	1, 2
		$V_{OM(DC)} = 0.50 \times V_{DDQ}$	0.9	1.0	1.1		
		$V_{OH(DC)} = 0.75 \times V_{DDQ}$	0.9	1.0	1.3		
110b	40Ω	$V_{OL(DC)} = 0.2 \times V_{DDQ}$	0.8	1.0	1.1	$R_{ZQ}/6$	1, 2
		$V_{OM(DC)} = 0.50 \times V_{DDQ}$	0.9	1.0	1.1		
		$V_{OH(DC)} = 0.75 \times V_{DDQ}$	0.9	1.0	1.3		
Mismatch CA-to-CA within clock group		$0.50 \times V_{DDQ}$	–	–	2	%	1, 2, 3

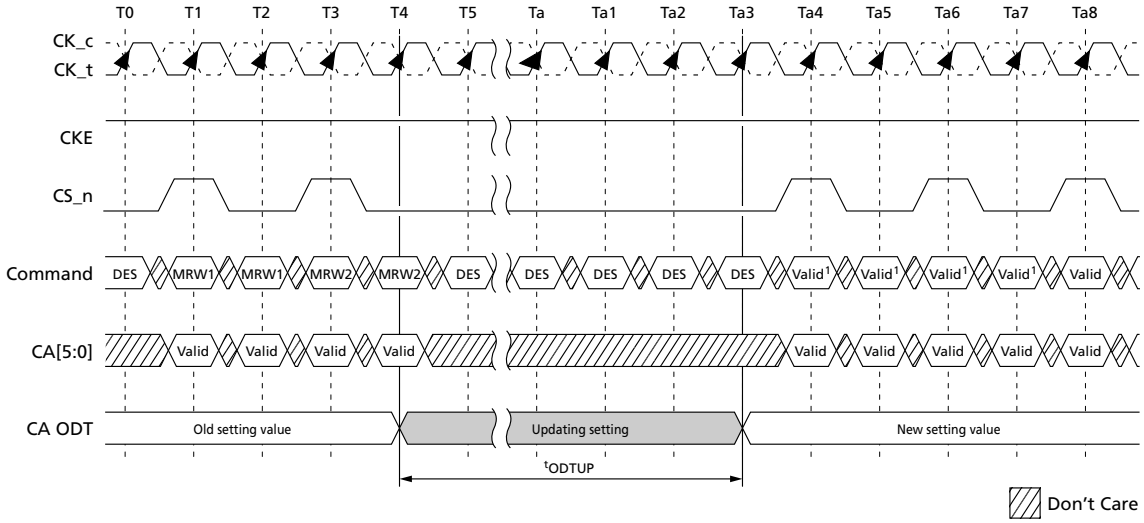
Notes: 1. The tolerance limits are specified after calibration with stable temperature and voltage. To understand the behavior of the tolerance limits when voltage or temperature changes after calibration, see the section on voltage and temperature sensitivity.
2. Pull-down ODT resistors are recommended to be calibrated at $0.50 \times V_{DDQ}$. Other calibration points may be used to achieve the linearity specification shown above; for example, calibration at $0.75 \times V_{DDQ}$ and $0.20 \times V_{DDQ}$.
3. CA to CA mismatch within clock group variation for a given component, including CK_t, CK_c, and CS (characterized).

$$\text{CA-to-CA mismatch} = \frac{R_{ODT}(\text{MAX}) - R_{ODT}(\text{MIN})}{R_{ODT}(\text{AVG})}$$

4. R_{ZQ} = 240Ω ±1% over entire operating range after calibration.

ODT for CA Update Time

Figure 224: ODT for CA Setting Update Timing in 4-Clock Cycle Command



DQ On-Die Termination

On-die termination (ODT) is a feature that allows the device to turn on/off termination resistance for each DQ, DQS, and DMI signal without the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices during WRITE or MASK WRITE operation.

The ODT feature is off and cannot be supported in power-down and self refresh modes.

The switch is enabled by the internal ODT control logic, which uses the WRITE-1 or MASK WRITE-1 command and other mode register control information. The value of R_{TT} is determined by the MR bits.

Figure 225: Functional Representation of DQ ODT

$$R_{TT} = \frac{V_{OUT}}{|I_{OUT}|}$$

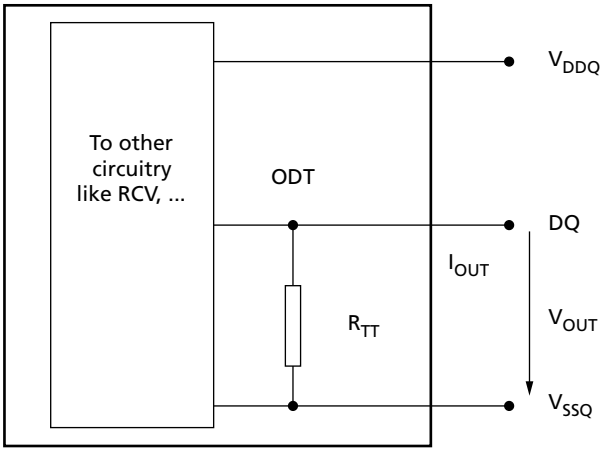


Table 186: ODT DC Electrical Characteristics for DQ Bus

MR11 OP[2:0]	R_{TT}	V_{OUT}	Min	Nom	Max	Unit	Notes
001b	240Ω	$V_{OL(DC)} = 0.2 \times V_{DDQ}$	0.8	1.0	1.1	$R_{ZQ}/1$	1, 2
		$V_{OM(DC)} = 0.50 \times V_{DDQ}$	0.9	1.0	1.1		
		$V_{OH(DC)} = 0.75 \times V_{DDQ}$	0.9	1.0	1.3		
010b	120Ω	$V_{OL(DC)} = 0.2 \times V_{DDQ}$	0.8	1.0	1.1	$R_{ZQ}/2$	1, 2
		$V_{OM(DC)} = 0.50 \times V_{DDQ}$	0.9	1.0	1.1		
		$V_{OH(DC)} = 0.75 \times V_{DDQ}$	0.9	1.0	1.3		
011b	80Ω	$V_{OL(DC)} = 0.2 \times V_{DDQ}$	0.8	1.0	1.1	$R_{ZQ}/3$	1, 2
		$V_{OM(DC)} = 0.50 \times V_{DDQ}$	0.9	1.0	1.1		
		$V_{OH(DC)} = 0.75 \times V_{DDQ}$	0.9	1.0	1.3		
100b	60Ω	$V_{OL(DC)} = 0.2 \times V_{DDQ}$	0.8	1.0	1.1	$R_{ZQ}/4$	1, 2
		$V_{OM(DC)} = 0.50 \times V_{DDQ}$	0.9	1.0	1.1		
		$V_{OH(DC)} = 0.75 \times V_{DDQ}$	0.9	1.0	1.3		
101b	48Ω	$V_{OL(DC)} = 0.2 \times V_{DDQ}$	0.8	1.0	1.1	$R_{ZQ}/5$	1, 2
		$V_{OM(DC)} = 0.50 \times V_{DDQ}$	0.9	1.0	1.1		
		$V_{OH(DC)} = 0.75 \times V_{DDQ}$	0.9	1.0	1.3		

Table 186: ODT DC Electrical Characteristics for DQ Bus (Continued)

MR11 OP[2:0]	R_{TT}	V_{OUT}	Min	Nom	Max	Unit	Notes
110b	40Ω	$V_{OL(DC)} = 0.2 \times V_{DDQ}$	0.8	1.0	1.1	$R_{ZQ}/6$	1, 2
		$V_{OM(DC)} = 0.50 \times V_{DDQ}$	0.9	1.0	1.1		
		$V_{OH(DC)} = 0.75 \times V_{DDQ}$	0.9	1.0	1.3		
Mismatch DQ-to-DQ within clock group		$0.50 \times V_{DDQ}$	–	–	2	%	1, 2, 3

Notes: 1. The ODT tolerance limits are specified after calibration with stable temperature and voltage. To understand the behavior of the tolerance limits when voltage or temperature changes after calibration, see the following section on voltage and temperature sensitivity.
2. Pull-down ODT resistors are recommended to be calibrated at $0.50 \times V_{DDQ}$. Other calibration points may be used to achieve the linearity specification shown above, for example, calibration at $0.75 \times V_{DDQ}$ and $0.20 \times V_{DDQ}$.
3. DQ-to-DQ mismatch within byte variation for a given component, including DQS (characterized).

$$\text{DQ-to-DQ mismatch} = \frac{R_{ODT}(MAX) - R_{ODT}(MIN)}{R_{ODT}(AVG)}$$

4. R_{ZQ} = 240Ω ±1% over entire operating range after calibration.

Output Driver and Termination Register Temperature and Voltage Sensitivity

When temperature and/or voltage change after calibration, the tolerance limits widen according to the tables below.

Table 187: Output Driver and Termination Register Sensitivity Definition

Resistor	Definition Point	Min	Max	Unit	Notes
R_{ONPD}	$0.50 \times V_{DDQ}$	$90 - (dR_{ONdT} \times \lvert\Delta T\rvert) - (dR_{ONdV} \times \lvert\Delta V\rvert)$	$110 + (dR_{ONdT} \times \lvert\Delta T\rvert) + (dR_{ONdV} \times \lvert\Delta V\rvert)$	%	1, 2
V_{OHPU}	$0.50 \times V_{DDQ}$	$90 - (dV_{OHdT} \times \lvert\Delta T\rvert) - (dV_{OHdV} \times \lvert\Delta V\rvert)$	$110 + (dV_{OHdT} \times \lvert\Delta T\rvert) + (dV_{OHdV} \times \lvert\Delta V\rvert)$		1, 2
$R_{TT(I/O)}$	$0.50 \times V_{DDQ}$	$90 - (dR_{ONdT} \times \lvert\Delta T\rvert) - (dR_{ONdV} \times \lvert\Delta V\rvert)$	$110 + (dR_{ONdT} \times \lvert\Delta T\rvert) + (dR_{ONdV} \times \lvert\Delta V\rvert)$		1, 2, 3
$R_{TT(IN)}$	$0.50 \times V_{DD2}$	$90 - (dR_{ONdT} \times \lvert\Delta T\rvert) - (dR_{ONdV} \times \lvert\Delta V\rvert)$	$110 + (dR_{ONdT} \times \lvert\Delta T\rvert) + (dR_{ONdV} \times \lvert\Delta V\rvert)$		1, 2, 4

Notes: 1. $\Delta T = T - T(@calibration)$, $\Delta V = V - V(@calibration)$
2. dR_{ONdT}, dR_{ONdV}, dV_{OHdT}, dV_{OHdV}, dR_{TTdV}, and dR_{TTdT} are not subject to production test but are verified by design and characterization.
3. This parameter applies to input/output pin such as DQS, DQ, and DMI.
4. This parameter applies to input pin such as CK, CA, and CS.
5. Refer to Pull-Up/Pull-Down Driver Characteristics for V_{OHPU}.

Table 188: Output Driver and Termination Register Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
dR_{ONdT}	R_{ON} temperature sensitivity	0	0.75	%/°C
dR_{ONdV}	R_{ON} voltage sensitivity	0	0.20	%/mV
dV_{OHdT}	V_{OH} temperature sensitivity	0	0.75	%/°C
dV_{OHdV}	V_{OH} voltage sensitivity	0	0.35	%/mV
dR_{TTdT}	R_{TT} temperature sensitivity	0	0.75	%/°C
dR_{TTdV}	R_{TT} voltage sensitivity	0	0.20	%/mV

ODT Mode Register

The ODT mode is enabled if MR11 OP[2:0] are non-zero. In this case, the value of R_{TT} is determined by the settings of those bits. The ODT mode is disabled if MR11 OP[2:0] = 0.

Asynchronous ODT

When ODT mode is enabled in MR11 OP[2:0], DRAM ODT is always High-Z. The DRAM ODT feature is automatically turned ON asynchronously after a WRITE-1, MASK WRITE-1, or MPC[WRITE-FIFO] command. After the burst write is complete, the DRAM ODT turns OFF asynchronously. The DQ bus ODT control is automatic and will turn the ODT resistance on/off if DQ ODT is enabled in the mode register.

The following timing parameters apply when the DQ bus ODT is enabled:

- ODTLon, ^{t}ODTon(MIN), ^{t}ODTon(MAX)
- ODTLoff, ^{t}ODToff(MIN), ^{t}ODToff(MAX)

$ODTL_{ON}$ is a synchronous parameter and is the latency from a CAS-2 command to the ^{t}ODTon reference. $ODTL_{ON}$ latency is a fixed latency value for each speed bin. Each speed bin has a different $ODTL_{ON}$ latency.

Minimum R_{TT}turn-on time (^{t}ODTon(MIN)) is the point in time when the device termination circuit leaves High-Z and ODT resistance begins to turn on.

Maximum R_{TT}turn on time (^{t}ODTon(MAX)) is the point in time when the ODT resistance is fully on.

^{t}ODTon(MIN) and ^{t}ODTon(MAX) are measured after $ODTL_{ON}$ latency is satisfied from CAS-2 command.

$ODTL_{OFF}$is a synchronous parameter and it is the latency from CAS-2 command to ^{t}ODToff reference. $ODTL_{OFF}$ latency is a fixed latency value for each speed bin. Each speed bin has a different $ODTL_{OFF}$ latency.

Minimum R_{TT}turn-off time (^{t}ODToff(MIN)) is the point in time when the device termination circuit starts to turn off the ODT resistance.

Maximum ODT turn off time (^{t}ODToff(MAX)) is the point in time when the on-die termination has reached High-Z.

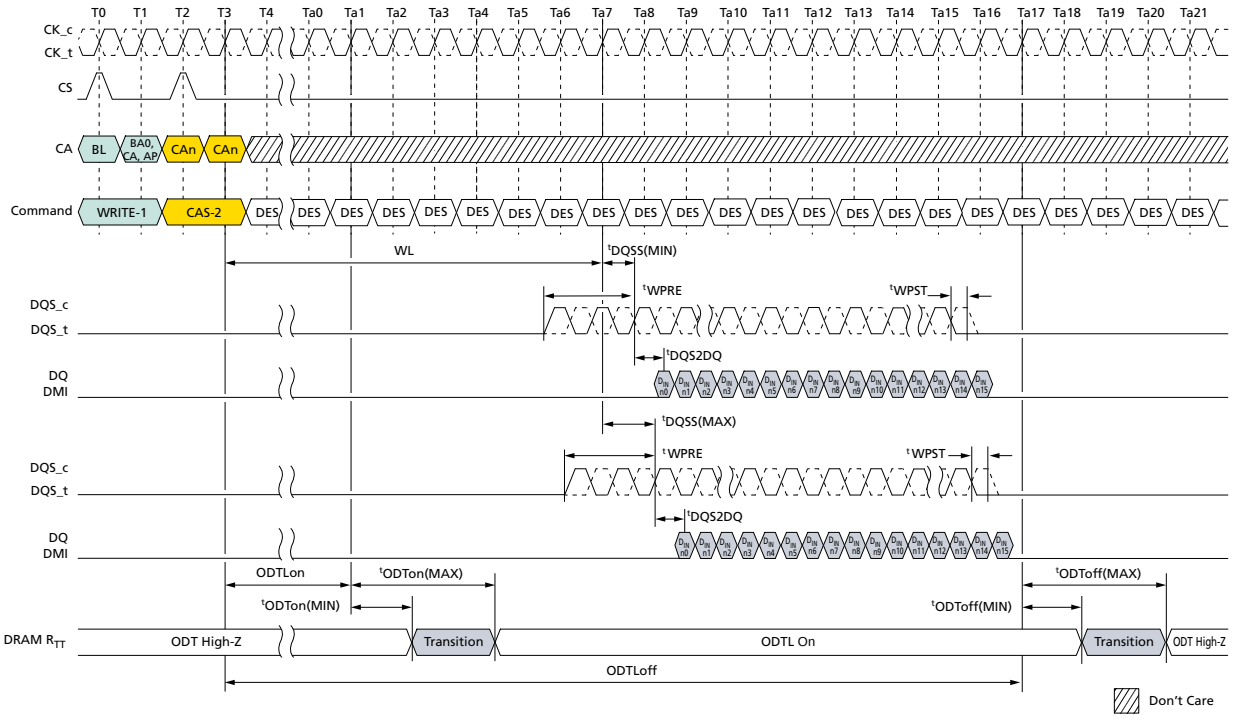
^{t}ODToff(MIN) and ^{t}ODToff(MAX) are measured after $ODTL_{OFF}$ latency is satisfied from CAS-2 command.

Table 189: $ODTL_{ON}$ and $ODTL_{OFF}$ Latency Values

$ODTL_{ON}$ Latency[1]		$ODTL_{OFF}$ Latency[2]			
^{t}WPRE = 2 ^{t}CK					
WL Set A (*n*CK)	WL Set B (*n*CK)	WL Set A (*n*CK)	WL Set B (*n*CK)	Lower Frequency Limit (>) (MHz)	Upper Frequency Limit (≤) (MHz)
N/A	N/A	N/A	N/A	10	266
N/A	N/A	N/A	N/A	266	533
N/A	6	N/A	22	533	800
4	12	20	28	800	1066
4	14	22	32	1066	1333
6	18	24	36	1333	1600
6	20	26	40	1600	1866
8	24	28	44	1866	2133

Notes: 1. $ODTL_{ON}$ is referenced from CAS-2 command.
2. $ODTL_{OFF}$ as shown in table assumes BL = 16. For BL32, 8^{t}CK should be added.

Figure 226: Asynchronous ODTon/ODToff Timing



Notes: 1. BL = 16, Write postamble = 0.5*n*CK, DQ/DQS: V_{SSQ} termination.
2. D_{IN} *n* = data-in to column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

DQ ODT During Power-Down and Self Refresh Modes

DQ bus ODT will be disabled in power-down mode. In self refresh mode, the ODT will be turned off when CKE is LOW but will be enabled if CKE is HIGH and DQ ODT is enabled in the mode register.

ODT During Write Leveling Mode

If ODT is enabled in MR11 OP[2:0] in write leveling mode, the device always provides the termination on DQS signals. DQ termination is always off in write leveling mode.

Table 190: Termination State in Write Leveling Mode

ODT State in MR11 OP[2:0]	DQS Termination	DQ[15:0]/DMI[1:0] Termination
Disabled	Off	Off
Enabled	On	Off

Target Row Refresh Mode

The device limits the number of times that a given row can be accessed within a refresh period (^{t}REFW × 2) prior to requiring adjacent rows to be refreshed. The maximum activate count (MAC) is the maximum number of activates that a single row can sustain within a refresh period before the adjacent rows need to be refreshed. The row receiving the excessive actives is the target row (TRn), the adjacent rows to be refreshed are the victim rows. When the MAC limit is reached on TRn, either the device receives all (R × 2) REFRESH commands before another row activate is issued, or the device should be placed into targeted row refresh (TRR) mode. The TRR mode will refresh the rows adjacent to the TRn that encountered ^{t}MAC limit.

If the device supports unlimited MAC value: MR24 OP[2:0] = 000 and MR24 OP[3] = 1, TARGET ROW REFRESH operation is not required. Even though the device allows to set MR24 OP[7] = 1: TRR mode enable, in this case the device behavior is vendor specific. For example, a certain device may ignore MRW command for entering/exiting TRR mode or a certain device may support commands related TRR mode. See vendor device data sheets for details about TRR mode definition at supporting unlimited MAC value case.

There could be a maximum of two target rows to a victim row in a bank. The cumulative value of the activates from the two target rows on a victim row in a bank should not exceed MAC value.

MR24 fields are required to support the new TRR settings. Setting MR24 OP[7] = 1 enables TRR mode and setting MR24 OP[7] = 0 disables TRR mode. MR24 OP[6:4] defines which bank (BAn) the target row is located in (refer to MR24 table for details).

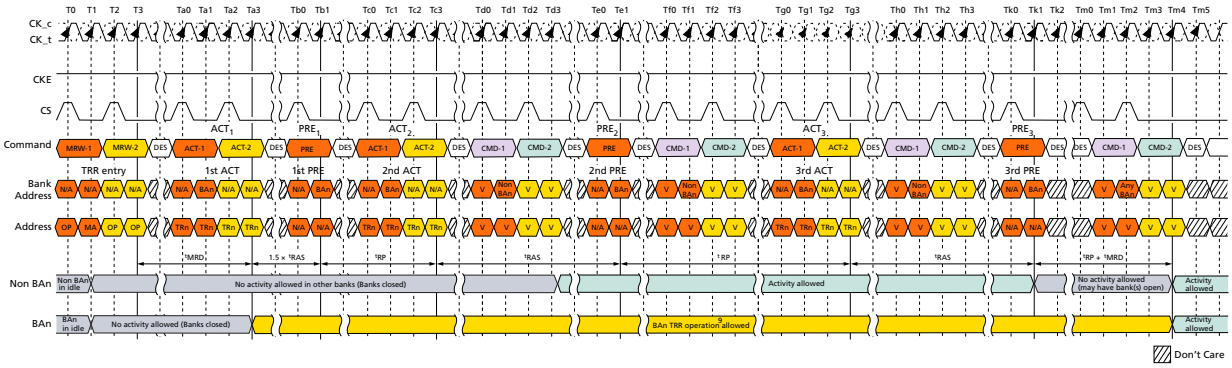
The TRR mode must be disabled during initialization as well as any other device calibration modes. The TRR mode is entered from a DRAM idle state, once TRR mode has been entered, no other mode register commands are allowed until TRR mode is completed; however, setting MR24 OP[7] = 0 to interrupt and reissue the TRR mode is allowed.

When enabled, TRR mode is self-clearing. The mode will be disabled automatically after the completion of defined TRR flow (after the third BAn precharge has completed plus ^{t}MRD). Optionally, the TRR mode can also be exited via another MRS command at the completion of TRR by setting MR24 OP[7] = 0. If the TRR is exited via another MRS command, the value written to MR24 OP[6:4] are "Don't Care."

TRR Mode Operation

1. The timing diagram depicts TRR mode. The following steps must be performed when TRR mode is enabled. This mode requires all three ACT (ACT1, ACT2, and ACT3) and three corresponding PRE commands (PRE1, PRE2, and PRE3) to complete TRR mode. PRECHARGE All (PREA) commands issued while the device is in TRR mode will also perform precharge to BAn and counts towards PREn command.
2. Prior to issuing the MRW command to enter TRR mode, the device should be in the idle state. MRW command must be issued with MR24 OP[7] = 1 and MR24 OP[6:4] defining the bank in which the targeted row is located. All other MR24 bits should remain unchanged.
3. No activity is to occur with the device until ^{t}MRD has been satisfied. When ^{t}MRD has been satisfied, the only commands allowed BAn, until TRR mode has completed, are ACT and PRE.
4. The first ACT to the BAn with the TRn address can now be applied; no other command is allowed at this point. All other banks must remain inactive from when the first BAn ACT command is issued until [(1.5 x ^{t}RAS) + ^{t}RP] is satisfied.
5. After the first ACT to the BAn with the TRn address is issued, PRE to BAn is to be issued (1.5 × ^{t}RAS) later; and then followed ^{t}RP later by the second ACT to the BAn with the TRn address.
6. After the second ACT to the BAn with the TRn address is issued, PRE to BAn is to be issued ^{t}RAS later and then followed ^{t}RP later by the third ACT to the BAn with the TRn address.
7. After the third ACT to the BAn with the TRn address is issued, PRE to BAn would be issued ^{t}RAS later. TRR mode is completed once ^{t}RP plus ^{t}MRD is satisfied.
8. TRR mode must be completed as specified to guarantee that adjacent rows are refreshed. Anytime the TRR mode is interrupted and not completed, the interrupted TRR mode must be cleared and then subsequently performed again. To clear an interrupted TRR mode, MR24 change is required with setting MR24 OP[7] = 0, MR24 OP[6:4] are "Don't Care," followed by three PRE to BAn, with ^{t}RP time in between each PRE command. The complete TRR sequence (steps 2–7) must be then reissued and completed to guarantee that the adjacent rows are refreshed.
9. A REFRESH command to the device, or entering self refresh mode, is not allowed while the device is in TRR mode.

Figure 227: Target Row Refresh Mode



Notes: 1. TRn is the targeted row.
2. Bank BAn represents the bank in which the targeted row is located.
3. TRR mode self-clears after ^{t}MRD + ^{t}RP measured from the third BAn precharge PRE3 at clock edge Th4.
4. TRR mode or any other activity can be re-engaged after ^{t}RP + ^{t}MRD from the third BAn precharge PRE3. PRE_ALL also counts if it is issued instead of PREn. TRR mode is cleared by the device after PRE3 to the BAn bank.
5. ACTIVATE commands to BAn during TRR mode do not provide refresh support (the refresh counter is unaffected).
6. The device must restore the degraded row(s) caused by excessive activation of the targeted row (TRn) necessary to meet refresh requirements.
7. A new TRR mode must wait ^{t}MRD + ^{t}RP time after the third precharge.
8. BAn may not be used with any other command.
9. ACT and PRE are the only allowed commands to BAn during TRR mode.
10. REFRESH commands are not allowed during TRR mode.
11. All timings are to be met by DRAM during TRR mode, such as ^{t}FAW. Issuing ACT1, ACT2, and ACT3 counts towards ^{t}FAW budget.

Post-Package Repair

The device has fail row address repair as an optional post-package repair (PPR) feature and it is readable through MR25 OP[7:0].

PPR provides simple and easy repair method in the system and fail row address can be repaired by the electrical programming of Electrical-fuse scheme. The device can correct one row per bank with PPR.

Electrical-fuse cannot be switched back to un-fused states once it is programmed. The controller should prevent unintended PPR mode entry and repair.

Failed Row Address Repair

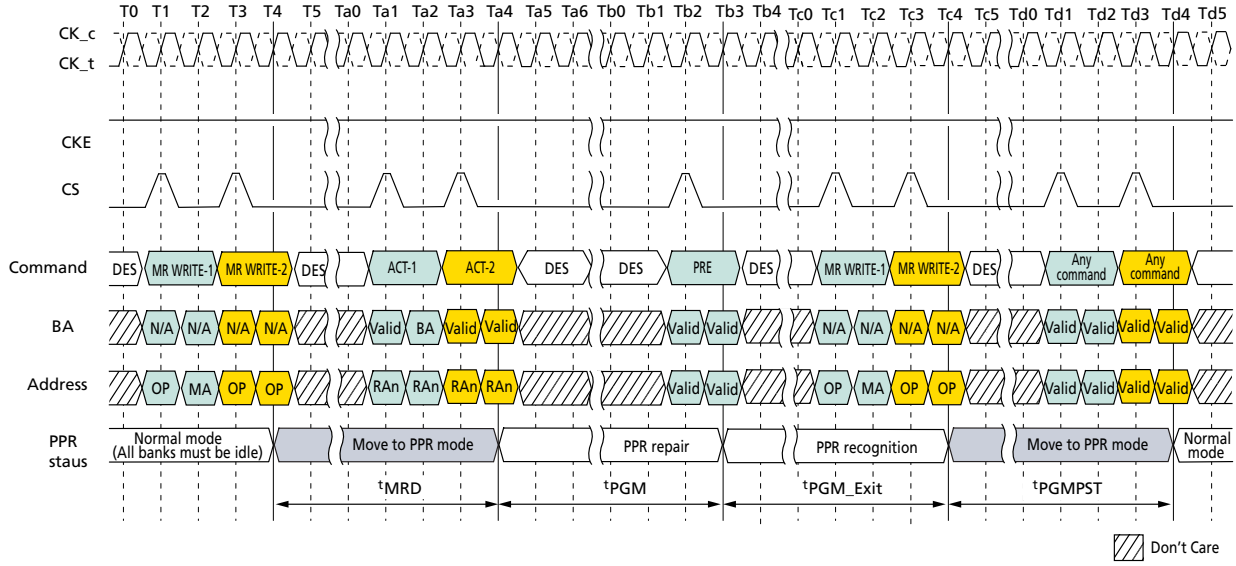
The following is procedure of PPR:

1. Before entering PPR mode, all banks must be precharged.
2. Enable PPR using MR4 OP[4] = 1 and wait ^{t}MRD.
3. Issue ACT command with fail row address.
4. Wait ^{t}PGM to allow the device repair target row address internally then issue PRECHARGE
5. Wait ^{t}PGM_EXIT after PRECHARGE, which allows the device to recognize repaired row address RAn.
6. Exit PPR mode with setting MR4 OP[4] = 0.
7. The device is ready for any valid command after ^{t}PGMPST.
8. In more than one fail address repair case, repeat step 2 to 7.

Once PPR mode is exited, to confirm whether the target row has correctly repaired, the host can verify the repair by writing data into the target row and reading it back after PPR exit with MR4 OP[4] = 0 and ^{t}PGMPST.

The following timing diagram shows PPR operation.

Figure 228: Post-Package Repair Timing



Notes: 1. During ^{t}PGM, any other commands (including refresh) are not allowed on each die.
2. With one PPR command, only one row can be repaired at one time per die.
3. When PPR procedure completes, reset procedure is required before normal operation.
4. During PPR, memory contents are not refreshed and may be lost.

Table 191: Post-Package Repair Timing Parameters

Parameter	Symbol	Min	Max	Units
PPR programming time	^{t}PGM	1000	–	ms
PPR exit time	^{t}PGM_EXIT	15	–	ns
New address setting time	^{t}PGMPST	50	–	µs

Read Preamble Training

Read preamble training is supported through the MPC function.

This mode can be used to train or read level the DQS receivers. After read preamble training is enabled by MR13 OP[1] = 1, the device will drive DQS_t LOW and DQS_c HIGH within ^{t}SDO and remain at these levels until an MPC[READ DQ CALIBRATION] command is issued.

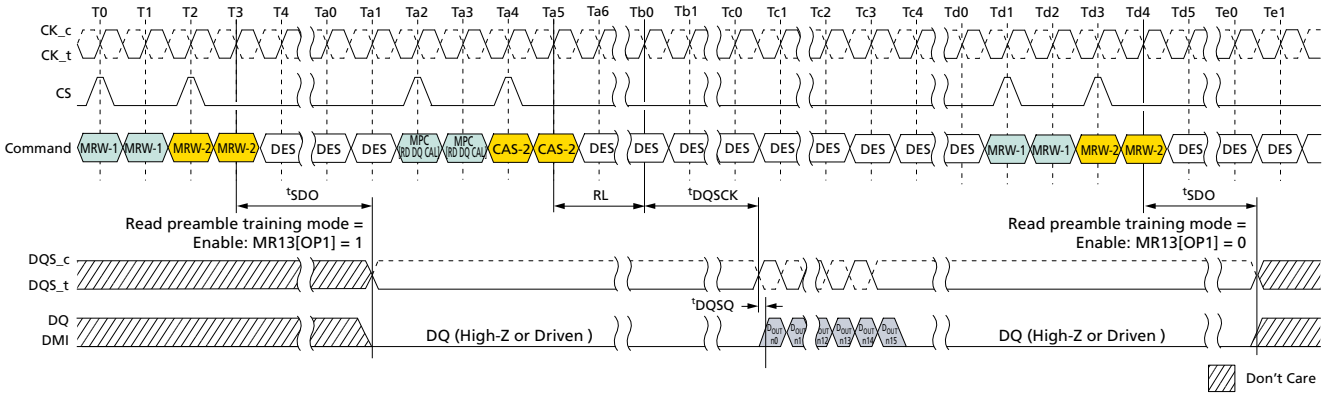
During read preamble training, the DQS preamble provided during normal operation will not be driven by the device. After the MPC[READ DQ CALIBRATION] command is issued, the device will drive DQS_t/DQS_c and DQ like a normal READ burst after RL and ^{t}DQSCK. Prior to the MPC[READ DQ CALIBRATION] command, the device may or may not drive DQ[15:0] in this mode.

While in read preamble training mode, only READ DQ CALIBRATION commands may be issued.

- Issue an MPC[READ DQ CALIBRATION] command followed immediately by a CAS-2 command.
- Each time an MPC[READ DQ CALIBRATION] command followed by a CAS-2 is received by the device, a 16-bit data burst will, after the currently set RL, drive the eight bits programmed in MR32 followed by the eight bits programmed in MR40 on all I/O pins.
- The data pattern will be inverted for I/O pins with a 1 programmed in the corresponding invert mask mode register bit.
- Note that the pattern is driven on the DMI pins, but no DATA BUS INVERSION function is enabled, even if read DBI is enabled in the DRAM mode register.
- This command can be issued every ^{t}CCD seamlessly.
- The operands received with the CAS-2 command must be driven LOW.

Read preamble training is exited within ^{t}SDO after setting MR13 OP[1] = 0.

Figure 229: Read Preamble Training



Note: 1. Read DQ calibration supports only BL16 operation.

Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed in the table below may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these conditions, or any other conditions outside those indicated in the operational sections of this document, is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 192: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit	Notes
V_{DD1} supply voltage relative to V_{SS}	V_{DD1}	–0.4	2.1	V	1
V_{DD2} supply voltage relative to V_{SS}	V_{DD2}	–0.4	1.5	V	1
V_{DDQ} supply voltage relative to V_{SS}	V_{DDQ}	–0.4	1.5	V	1
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.4	1.5	V	
Storage temperature	T_{STG}	–55	125	°C	2

Notes: 1. For information about relationships between power supplies, see the Voltage Ramp and Device Initialization section.
2. Storage temperature is the case surface temperature on the center/top side of the device. For measurement conditions, refer to the JESD51-2 standard.

AC and DC Operating Conditions

Operation or timing that is not specified is illegal. To ensure proper operation, the device must be initialized properly.

Table 193: Recommended DC Operating Conditions

Symbol	Min	Typ	Max	DRAM	Unit	Notes
V_{DD1}	1.70	1.80	1.95	Core 1 power	V	1, 2
V_{DD2}	1.06	1.10	1.17	Core 2 power/Input buffer power	V	1, 2, 3
V_{DDQ}	0.57	0.60	0.65	I/O buffer power	V	2, 3

Notes: 1. V_{DD1} uses significantly less power than V_{DD2}.
2. The voltage range is for DC voltage only. DC voltage is the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.
3. The voltage noise tolerance from DC to 20 MHz exceeding a peak-to-peak tolerance of 45mV at the DRAM ball is not included in the TdIVW.

Table 194: Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input leakage current	I_L	–4	4	µA	1, 2

Notes: 1. For CK_t, CK_c, CKE, CS, CA, ODT_CA, and RESET_n. Any input $0V \le V_{IN} \le V_{DD2}$. All other pins not under test = 0V.
2. CA ODT is disabled for CK_t, CK_c, CS, and CA.

Table 195: Input/Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/Output leakage current	I_{OZ}	–5	5	µA	1, 2

Notes: 1. For DQ, DQS_t, DQS_c, and DMI. Any I/O 0V ≤ V_{OUT} ≤ V_{DDQ}.
2. I/Os status are disabled: High impedance and ODT off.

Table 196: Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
Standard	T_{OPER}	Note 4	85	°C
Elevated		85	Note 4	°C

Notes: 1. Operating temperature is the case surface temperature at the center of the top side of the device. For measurement conditions, refer to the JESD51-2 standard.
2. Some applications require the operation of LPDDR4 in the maximum temperature conditions in the elevated temperature range from 85°C to 105°C case temperature. For LPDDR4 devices, derating may be necessary to operate in this range. Refer to MR4.
3. Either the device case temperature rating or the temperature sensor can be used to set an appropriate refresh rate, determine the need for AC timing derating, and/or monitor the operating temperature (see Temperature Sensor). When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the standard or elevated temperature range. For example, T_{CASE} could be above +85°C when the temperature sensor indicates a temperature of less than +85°C.
4. Refer to operating temperature range on top page.

AC and DC Input Measurement Levels

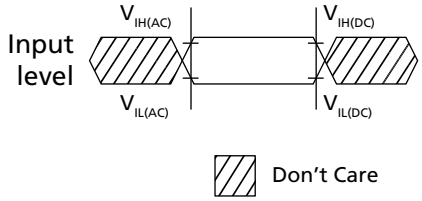
Input Levels for CKE

Table 197: Input Levels

Parameter	Symbol	Min	Max	Unit	Notes
Input HIGH level (AC)	$V_{IH(AC)}$	0.75 × V_{DD2}	V_{DD2} + 0.2	V	1
Input LOW level (AC)	$V_{IL(AC)}$	–0.2	0.25 × V_{DD2}	V	1
Input HIGH level (DC)	$V_{IH(DC)}$	0.65 × V_{DD2}	V_{DD2} + 0.2	V	
Input LOW level (DC)	$V_{IL(DC)}$	–0.2	0.35 × V_{DD2}	V	

Note: 1. See the AC Overshoot and Undershoot section.

Figure 230: Input Timing Definition for CKE



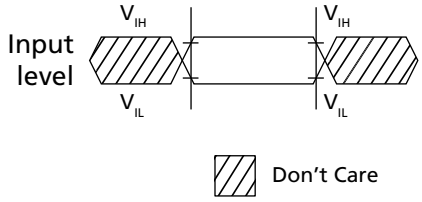
Input Levels for RESET_n

Table 198: Input Levels

Parameter	Symbol	Min	Max	Unit	Notes
Input HIGH level	V_{IH}	0.80 × V_{DD2}	V_{DD2} + 0.2	V	1
Input LOW level	V_{IL}	–0.2	0.20 × V_{DD2}	V	1

Note: 1. See the AC Overshoot and Undershoot section.

Figure 231: Input Timing Definition for RESET_n



Differential Input Voltage for CK

The minimum input voltage needs to satisfy both V_{indiff_CK} and $V_{indiff\_CK}/2$ specification at input receiver and their measurement period is $1^{t}CK$. V_{indiff_CK} is the peak-to-peak voltage centered on 0 volts differential and $V_{indiff\_CK}/2$ is maximum and minimum peak voltage from 0 volts.

Figure 232: CK Differential Input Voltage

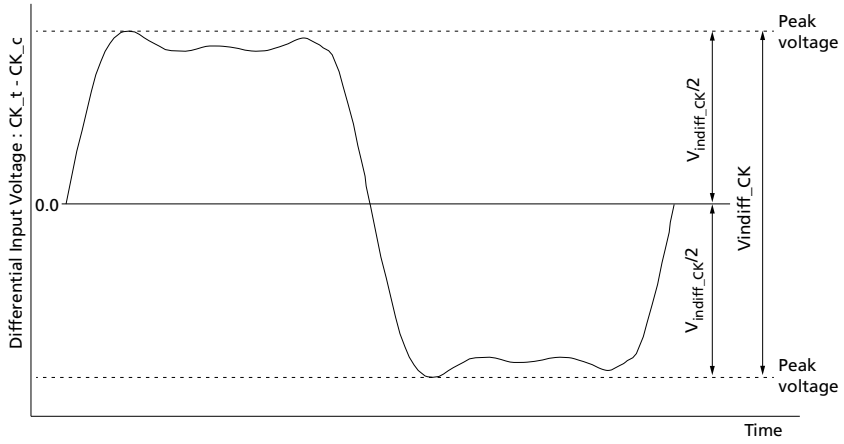


Table 199: CK Differential Input Voltage

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit	Note
		Min	Max	Min	Max	Min	Max		
CK differential input voltage	V_{indiff_CK}	420	–	380	–	360	–	mV	1

Note: 1. The peak voltage of differential CK signals is calculated in a following equation.

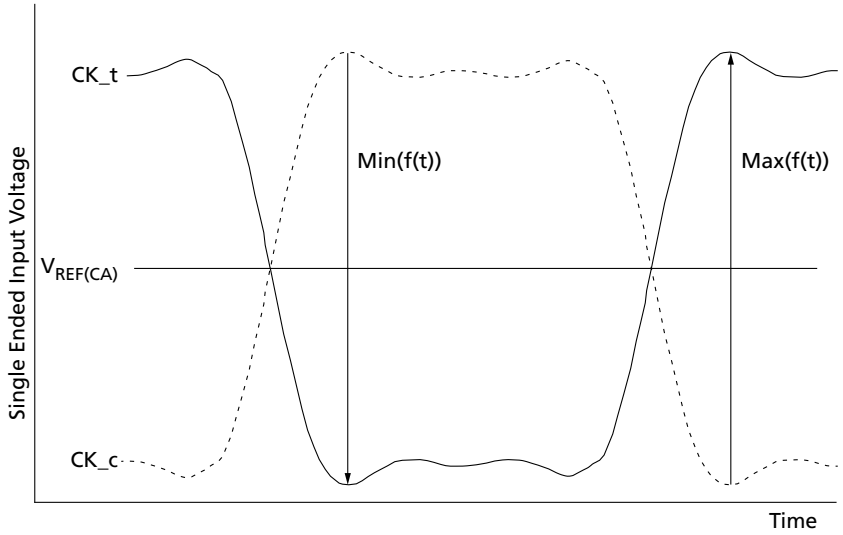
- V_{indiff_CK} = (Maximum peak voltage) - (Minimum peak voltage)
- Maximum peak voltage = MAX(f(t))
- Minimum peak voltage = MIN(f(t))
- f(t) = V_{CK_t} - V_{CK_c}

Peak Voltage Calculation Method

The peak voltage of differential clock signals are calculated in a following equation.

- $V_{IH.DIFF.peak}$ voltage = MAX(f(t))
- $V_{IL.DIFF.peak}$ voltage = MIN(f(t))
- f(t) = V_{CK_t} - V_{CK_c}

Figure 233: Definition of Differential Clock Peak Voltage

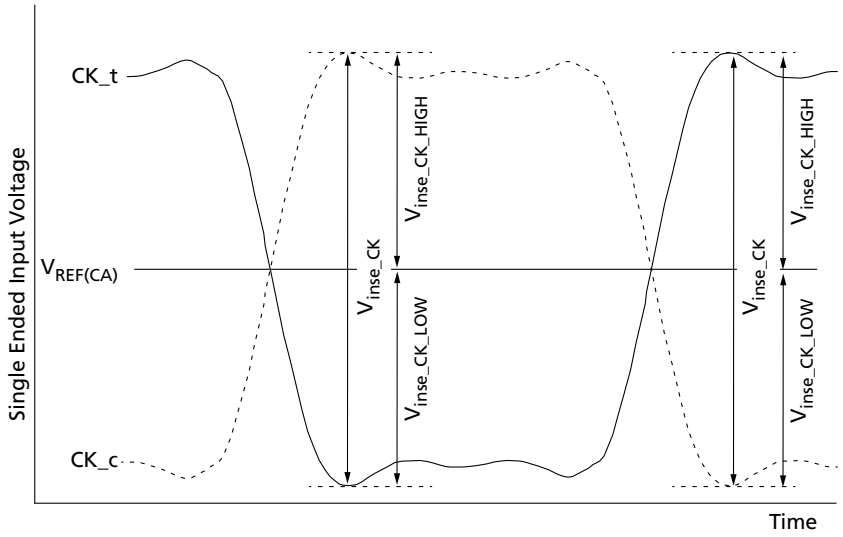


Note: 1. $V_{REF(CA)}$ is device internal setting value by V_{REF} training.

Single-Ended Input Voltage for Clock

The minimum input voltage need to satisfy V_{inse_CK}, $V_{inse\_CK\_HIGH}$, and $V_{inse\_CK\_LOW}$ specification at input receiver.

Figure 234: Clock Single-Ended Input Voltage



Note: 1. $V_{REF(CA)}$ is device internal setting value by V_{REF} training.

Table 200: Clock Single-Ended Input Voltage

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
Clock single-ended input voltage	V_{inse_CK}	210	–	190	–	180	–	mV
Clock single-ended input voltage HIGH from $V_{REF(CA)}$	$V_{inse\_CK\_HIGH}$	105	–	95	–	90	–	mV

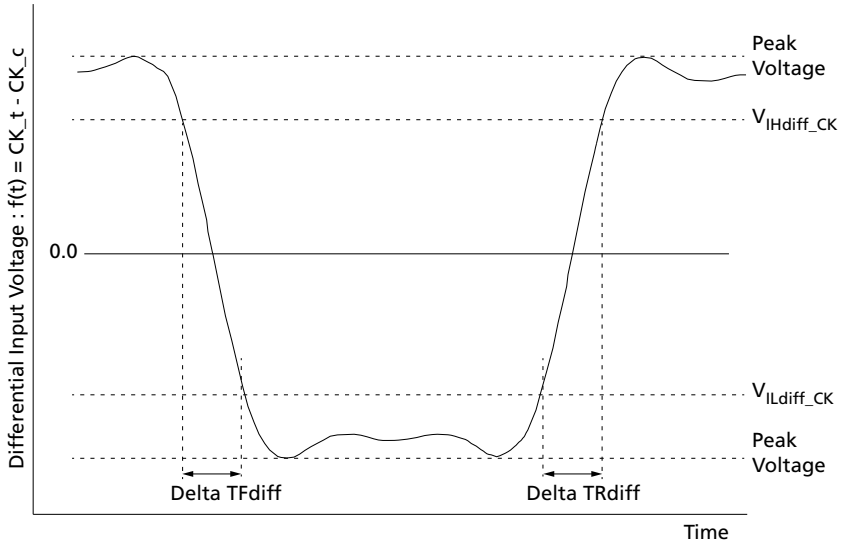
Table 200: Clock Single-Ended Input Voltage (Continued)

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
Clock single-ended input voltage LOW from $V_{REF(CA)}$	$V_{inse\_CK\_LOW}$	105	–	95	–	90	–	mV

Differential Input Slew Rate Definition for Clock

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown below in figure and the tables.

Figure 235: Differential Input Slew Rate Definition for CK_t, CK_c



Notes: 1. Differential signal rising edge from V_{ILdiff_CK} to V_{IHdiff_CK} must be monotonic slope.
2. Differential signal falling edge from V_{IHdiff_CK} to V_{ILdiff_CK} must be monotonic slope.

Table 201: Differential Input Slew Rate Definition for CK_t, CK_c

Description	From	To	Defined by
Differential input slew rate for rising edge (CK_t - CK_c)	V_{ILdiff_CK}	V_{IHdiff_CK}	$\lvert V_{ILdiff\_CK} - V_{IHdiff\_CK}\rvert / \Delta TRdiff$
Differential input slew rate for falling edge (CK_t - CK_c)	V_{IHdiff_CK}	V_{ILdiff_CK}	$\lvert V_{ILdiff\_CK} - V_{IHdiff\_CK}\rvert / \Delta TFdiff$

Table 202: Differential Input Level for CK_t, CK_c

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
Differential Input HIGH	V_{IHdiff_CK}	175	–	155	–	145	–	mV
Differential Input LOW	V_{ILdiff_CK}	–	–175	–	–155	–	–145	mV

Table 203: Differential Input Slew Rate for CK_t, CK_c

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
Differential input slew rate for clock	SRIdiff_CK	2	14	2	14	2	14	V/ns

Differential Input Cross-Point Voltage

The cross-point voltage of differential input signals (CK_t, CK_c) must meet the requirements in table below. The differential input cross-point voltage V_{IX} is measured from the actual cross-point of true and complement signals to the mid level.

Figure 236: V_{ix}Definition (Clock)

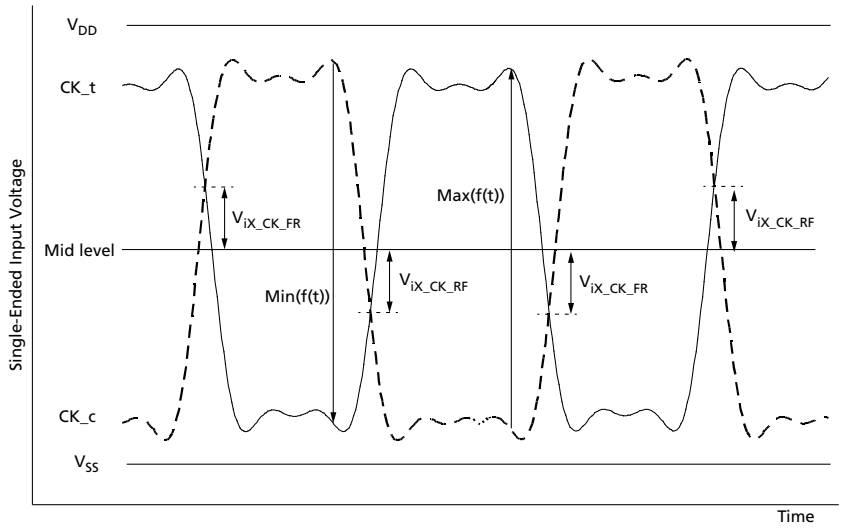


Table 204: Cross-Point Voltage for Differential Input Signals (Clock)

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
Clock differential input cross-point voltage ratio	$V_{ix\_CK\_ratio}$	–	25	–	25	–	25	%

Notes: 1. $V_{ix\_CK\_ratio}$ is defined by this equation: $V_{ix\_CK\_ratio} = V_{ix\_CK\_FR}/|MIN(f(t))|$
2. $V_{ix\_CK\_ratio}$ is defined by this equation: $V_{ix\_CK\_ratio} = V_{ix\_CK\_RF}/MAX(f(t))$
3. $V_{ix\_CK\_FR}$ is defined as delta between crosspoint (CK_t fall, CK_c rise) to MIN(f(t))/2.
4. In LPDDR4X un-terminated case, CK mid level is calculated as:
   - High level = V_{DDQ}; Low level = V_{SS}; Mid level = $V_{DDQ/2}$
5. In LPDDR4 un-terminated case, mid level must be equal or lower than 369mV (33.6% of V_{DD2})
6. Notes 1–5 apply to entire table.

Differential Input Voltage for DQS

The minimum input voltage needs to satisfy both V_{indiff_DQS} and $V_{indiff\_DQS}/2$ specification at input receiver and their measurement period is 1UI ($^{t}CK/2$). V_{indiff_DQS} is the peak to peak voltage centered on 0 volts differential and $V_{indiff\_DQS}/2$ is maximum and minimum peak voltage from 0 volts.

Figure 237: DQS Differential Input Voltage

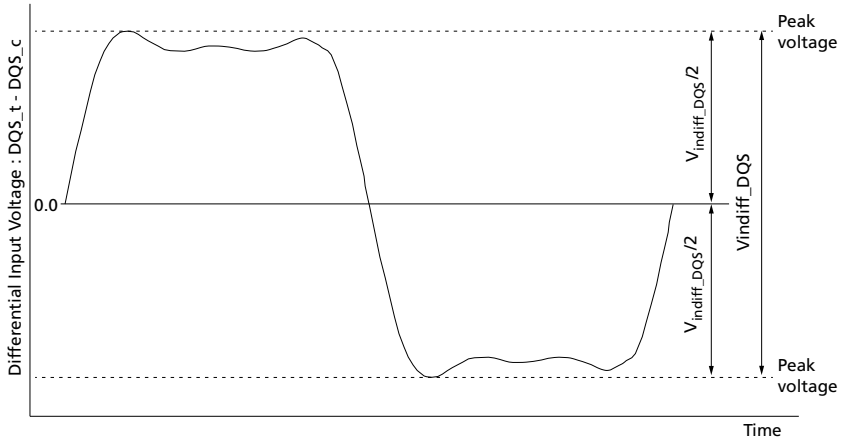


Table 205: DQS Differential Input Voltage

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit	Note
		Min	Max	Min	Max	Min	Max		
DQS differential input voltage	V_{indiff_DQS}	360	–	360	–	340	–	mV	1

Note: 1. The peak voltage of differential DQS signals is calculated in a following equation.

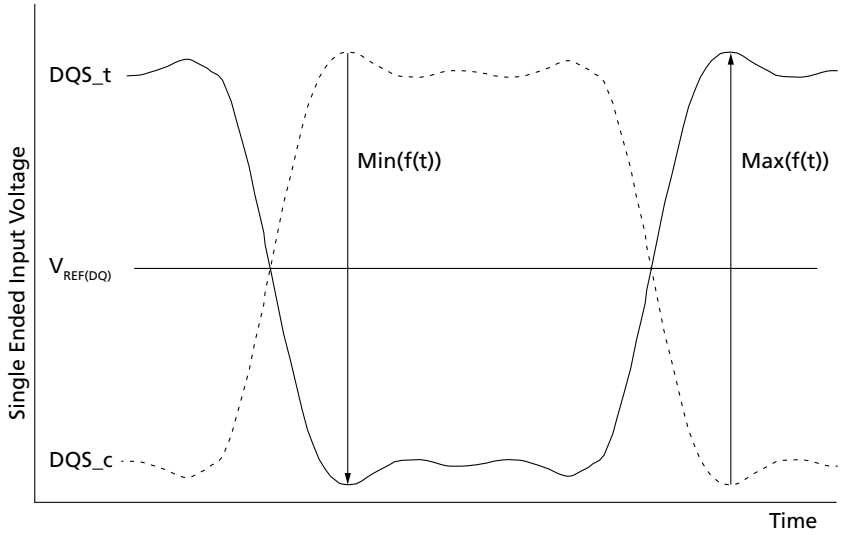
- V_{indiff_DQS} = (Maximum peak voltage) - (Minimum peak voltage)
- Maximum peak voltage = MAX(f(t))
- Minimum peak voltage = MIN(f(t))
- f(t) = V_{DQS_t} - V_{DQS_c}

Peak Voltage Calculation Method

The peak voltage of differential DQS signals are calculated in a following equation.

- $V_{IH.DIFF.peak}$voltage = MAX(f(t))
- $V_{IL.DIFF.peak}$ voltage = MIN(f(t))
- f(t) = V_{DQS_t} - V_{DQS_c}

Figure 238: Definition of Differential DQS Peak Voltage

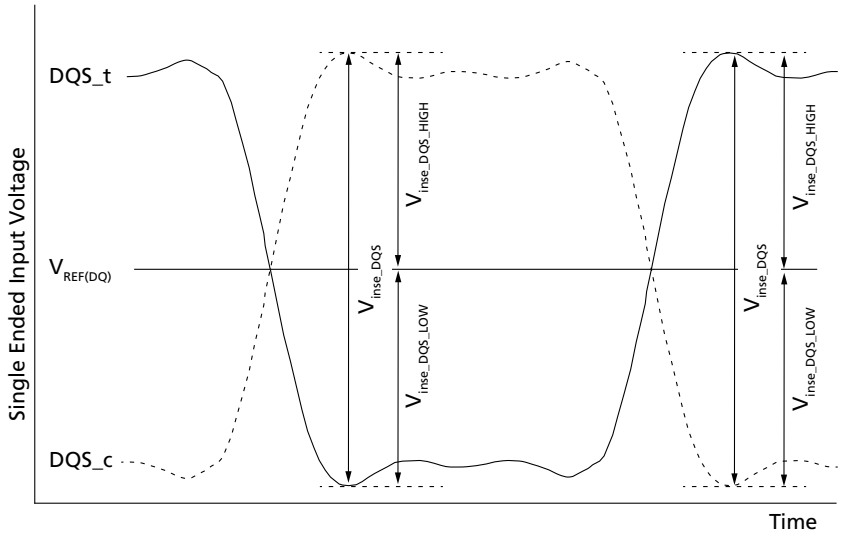


Note: 1. $V_{REF(DQ)}$ is device internal setting value by V_{REF} training.

Single-Ended Input Voltage for DQS

The minimum input voltage need to satisfy V_{inse_DQS}, $V_{inse\_DQS\_HIGH}$, and $V_{inse\_DQS\_LOW}$ specification at input receiver.

Figure 239: DQS Single-Ended Input Voltage



Note: 1. $V_{REF(DQ)}$ is device internal setting value by V_{REF} training.

Table 206: DQS Single-Ended Input Voltage

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
DQS single-ended input voltage	V_{inse_DQS}	180	–	180	–	170	–	mV
DQS single-ended input voltage HIGH from $V_{REF(DQ)}$	$V_{inse\_DQS\_HIGH}$	90	–	90	–	85	–	mV

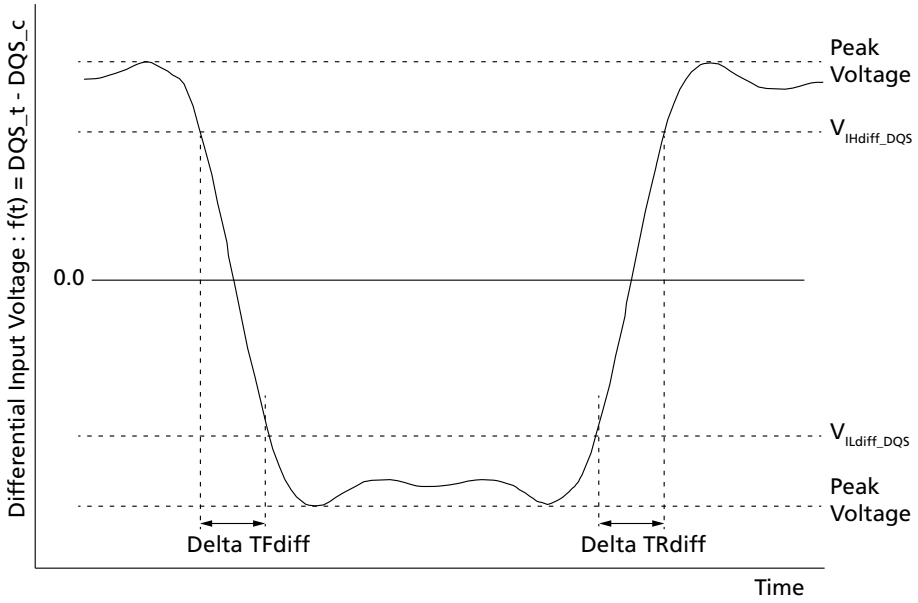
Table 206: DQS Single-Ended Input Voltage (Continued)

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
DQS single-ended input voltage LOW from $V_{REF(DQ)}$	$V_{inse\_DQS\_LOW}$	90	–	90	–	85	–	mV

Differential Input Slew Rate Definition for DQS

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown below in figure and the tables.

Figure 240: Differential Input Slew Rate Definition for DQS_t, DQS_c



Notes: 1. Differential signal rising edge from V_{ILdiff_DQS} to V_{IHdiff_DQS} must be monotonic slope.
2. Differential signal falling edge from V_{IHdiff_DQS} to V_{ILdiff_DQS} must be monotonic slope.

Table 207: Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	From	To	Defined by
Differential input slew rate for rising edge (DQS_t - DQS_c)	V_{ILdiff_DQS}	V_{IHdiff_DQS}	$\lvert V_{ILdiff\_DQS} - V_{IHdiff\_DQS}\rvert / \Delta TRdiff$
Differential input slew rate for falling edge (DQS_t - DQS_c)	V_{IHdiff_DQS}	V_{ILdiff_DQS}	$\lvert V_{ILdiff\_DQS} - V_{IHdiff\_DQS}\rvert / \Delta TFdiff$

Table 208: Differential Input Level for DQS_t, DQS_c

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
Differential Input HIGH	V_{IHdiff_DQS}	140	–	140	–	120	–	mV
Differential Input LOW	V_{ILdiff_DQS}	–	–140	–	–140	–	–120	mV

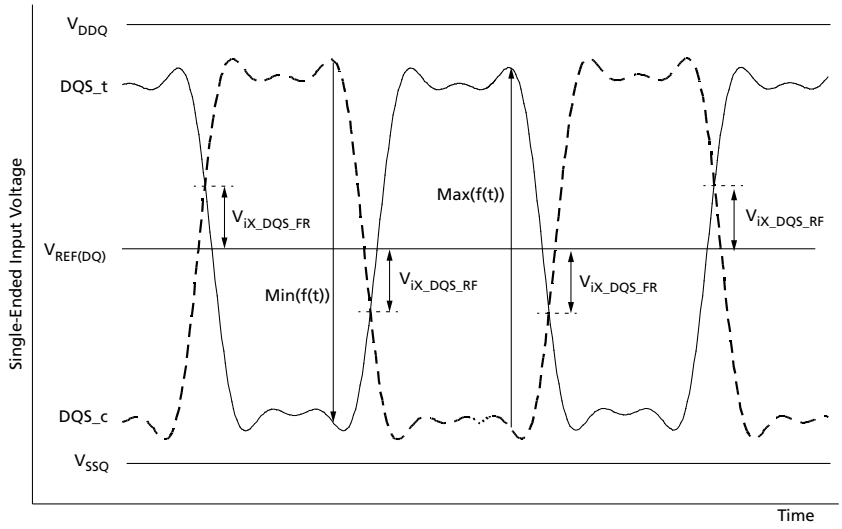
Table 209: Differential Input Slew Rate for DQS_t, DQS_c

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
Differential input slew rate	SRIdiff	2	14	2	14	2	14	V/ns

Differential Input Cross-Point Voltage

The cross-point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in table below. The differential input cross-point voltage V_{IX} is measured from the actual cross-point of true and complement signals to the mid level that is $V_{REF(DQ)}$.

Figure 241: V_{ix}Definition (DQS)



Note: 1. The base levels of $V_{ix\_DQS\_FR}$ and $V_{ix\_DQS\_RF}$ are $V_{REF(DQ)}$ that is device internal setting value by V_{REF} training.

Table 210: Cross-Point Voltage for Differential Input Signals (DQS)

Parameter	Symbol	1600/1867		2133/2400/3200		3733/4267		Unit
		Min	Max	Min	Max	Min	Max	
DQS differential input cross-point voltage ratio	$V_{ix\_DQS\_ratio}$	–	20	–	20	–	20	%

Notes: 1. $V_{ix\_DQS\_ratio}$ is defined by this equation: $V_{ix\_DQS\_ratio} = V_{ix\_DQS\_FR}/|MIN(f(t))|$
2. $V_{ix\_DQS\_ratio}$ is defined by this equation: $V_{ix\_DQS\_ratio} = V_{ix\_DQS\_RF}/MAX(f(t))$
3. Notes 1 and 2 apply to entire table.

Input Levels for ODT_CA

Table 211: Input Levels for ODT_CA

Parameter	Symbol	Min	Max	Unit
ODT input HIGH level	V_{IHODT}	$0.75 \times V_{DD2}$	$V_{DD2} + 0.2$	V
ODT input LOW level	V_{ILODT}	–0.2	$0.25 \times V_{DD2}$	V

Output Slew Rate and Overshoot/Undershoot Specifications

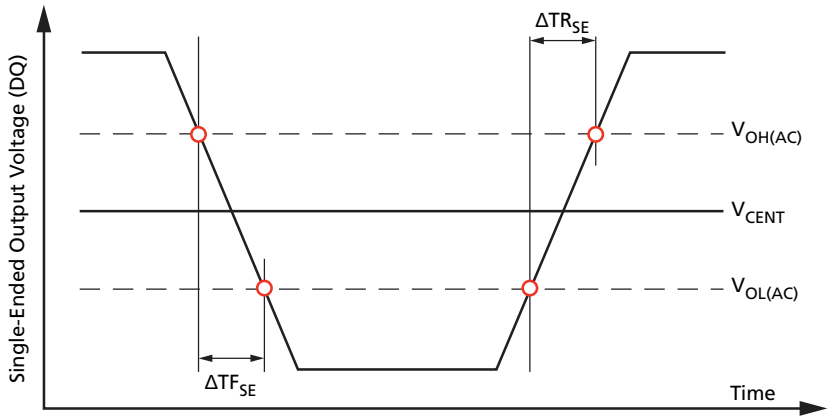
Single-Ended Output Slew Rate

Table 212: Single-Ended Output Slew Rate

Parameter	Symbol	Value		Units
		Min	Max	
Single-ended output slew rate (V_{OH} = V_{DDQ} x 0.5)	SRQse	3.0	9.0	V/ns
Output slew rate matching ratio (rise to fall)	–	0.8	1.2	–

Notes: 1. SR = Slew rate; Q = Query output; se = Single-ended signal.
2. Measured with output reference load.
3. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
4. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ = 0.2 × $V_{OH(DC)}$ and $V_{OH(AC)}$ = 0.8 × $V_{OH(DC)}$.
5. Slew rates are measured under average SSO conditions with 50% of the DQ signals per data byte switching.
6. Notes 1–5 apply to entire table.

Figure 242: Single-Ended Output Slew Rate Definition



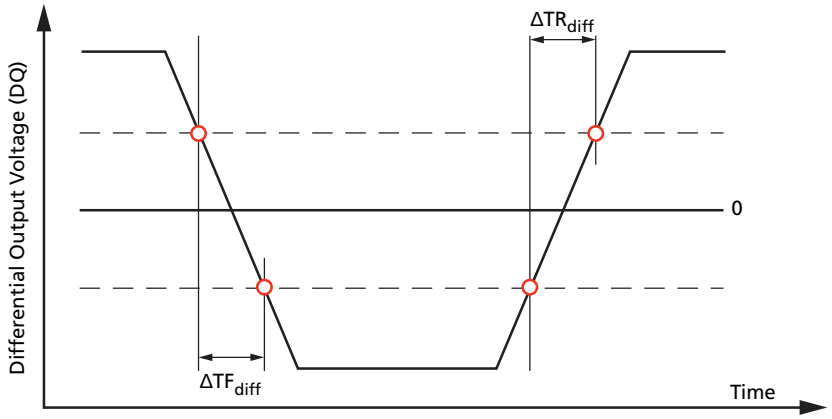
Differential Output Slew Rate

Table 213: Differential Output Slew Rate

Parameter	Symbol	Value		Units
		Min	Max	
Differential output slew rate (V_{OH} = V_{DDQ} x 0.5)	SRQdiff	6	18	V/ns

Notes: 1. SR = Slew rate; Q = Query output; se = Differential signal.
2. Measured with output reference load.
3. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ = –0.8 × $V_{OH(DC)}$ and $V_{OH(AC)}$ = 0.8 × $V_{OH(DC)}$.
4. Slew rates are measured under average SSO conditions with 50% of the DQ signals per data byte switching.
5. Notes 1–4 apply to entire table.

Figure 243: Differential Output Slew Rate Definition



Overshoot and Undershoot Specifications

Table 214: AC Overshoot/Undershoot Specifications

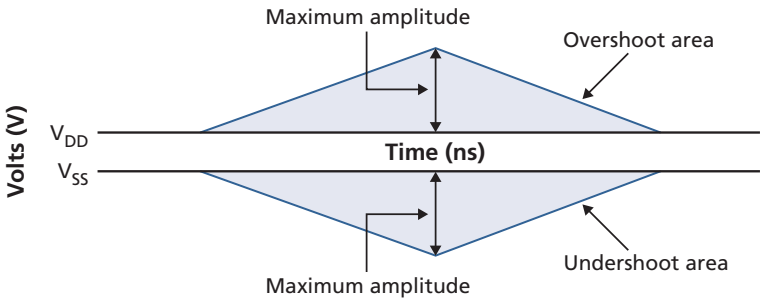
Parameter		1600	1866	3200	3733	4267	Unit
Maximum peak amplitude provided for overshoot area	MAX	0.3	0.3	0.3	0.3	0.3	V
Maximum peak amplitude provided for undershoot area	MAX	0.3	0.3	0.3	0.3	0.3	V
Maximum area above V_{DD}/ V_{DDQ}	MAX	0.1	0.1	0.1	0.1	0.1	V/ns
Maximum area below V_{SS}/ V_{SSQ}	MAX	0.1	0.1	0.1	0.1	0.1	V/ns

Notes: 1. V_{DD} stands for V_{DD2} for CKE, ODT. V_{DD} stands for V_{DDQ} for CA[5:0], CK_t, CS_n, DQ, DMI, DQS_t, and DQS_c.
2. V_{SS} stands for V_{SS} for CA[5:0], CK_t, CK_c, CS_n, CKE, and ODT. V_{SS} stands for V_{SSQ} for DQ, DMI, DQS_t, and DQS_c.
3. Maximum peak amplitude values are referenced from actual V_{DD} and V_{SS} values.
4. Maximum area values are referenced from maximum V_{DD} and V_{SS} values.

Table 215: Overshoot/Undershoot Specification for CKE and RESET

Parameter	Specification
Maximum peak amplitude provided for overshoot area	0.35V
Maximum peak amplitude provided for undershoot area	0.35V
Maximum area above V_{DD}	0.8 V-ns
Maximum area below V_{SS}	0.8 V-ns

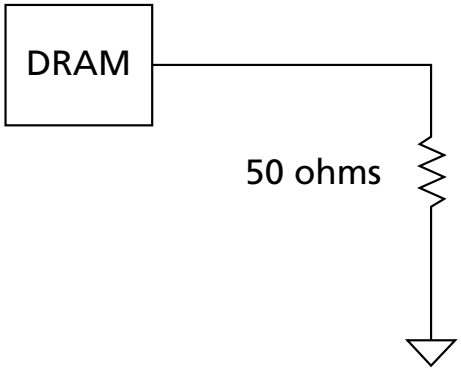
Figure 244: Overshoot and Undershoot Definition



Driver Output Timing Reference Load

Timing reference loads are not intended as a precise representation of any particular system environment or depiction of an actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Figure 245: Driver Output Timing Reference Load

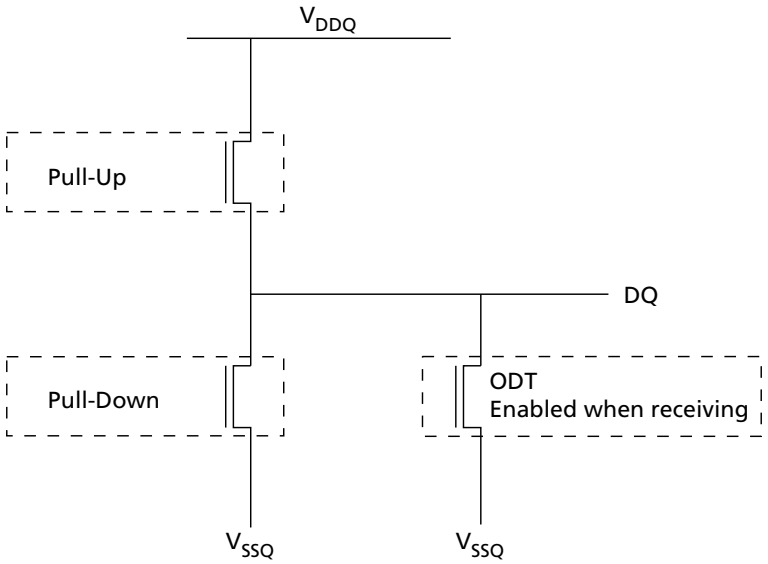


Note: 1. All output timing parameter values are reported with respect to this reference load; this reference load is also used to report slew rate.

LVSTL I/O System

LVSTL I/O cells are comprised of a driver pull-up and pull-down and a terminator.

Figure 246: LVSTL I/O Cell



To ensure that the target impedance is achieved, calibrate the LVSTL I/O cell as following example:

1. Calibrate the pull-down device against a 240 ohm resistor to V_{DDQ} via the ZQ pin.

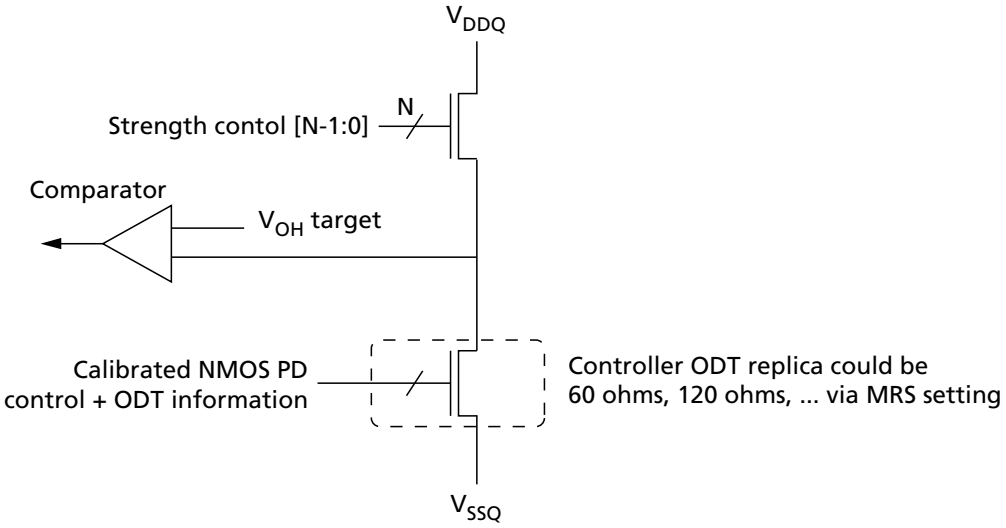
- Set strength control to minimum setting
- Increase drive strength until comparator detects data bit is less than $V_{DDQ}/2$

- NMOS pull-down device is calibrated to 240 ohms

2. Calibrate the pull-up device against the calibrated pull-down device.

- Set V_{OH} target and NMOS controller ODT replica via MRS (V_{OH} can be automatically controlled by ODT MRS)
- Set strength control to minimum setting
- Increase drive strength until comparator detects data bit is greater than V_{OH} target
- NMOS pull-up device is calibrated to V_{OH} target

Figure 247: Pull-Up Calibration



Input/Output Capacitance

Table 216: Input/Output Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance, CK_t and CK_c	C_{CK}	0.5	0.9	pF	
Input capacitance delta, CK_t and CK_c	C_{DCK}	0	0.09		3
Input capacitance, all other input-only pins	C_I	0.5	0.9		4
Input capacitance delta, all other input-only pins	C_{DI}	–0.1	0.1		5
Input/output capacitance, DQ, DMI, DQS_t, DQS_c	C_{IO}	0.7	1.3		6
Input/output capacitance delta, DQS_t, DQS_c	C_{DDQS}	0	0.1		7
Input/output capacitance delta, DQ, DMI	C_{DIO}	–0.1	0.1		8
Input/output capacitance, ZQ pin	C_{ZQ}	0	5.0		

Notes: 1. This parameter applies to LPDDR4 die only (does not include package capacitance).
2. This parameter is not subject to production testing; It is verified by design and characterization. The capacitance is measured according to JEP147 (procedure for measuring input capacitance using a vector network analyzer), with V_{DD1}, V_{DD2}, V_{DDQ}, and V_{SS} applied; All other pins are left floating.
3. Absolute value of $C_{CK\_t} - C_{CK\_c}$.
4. C_I applies to CS, CKE, and CA[5:0].
5. $C_{DI} = C_I - 0.5 \times (C_{CK\_t} + C_{CK\_c})$; It does not apply to CKE.
6. DMI loading matches DQ and DQS.
7. Absolute value of C_{DQS_t} and C_{DQS_c}.

8. $C_{DIO} = C_{IO}$ – Average (C_{DQn}, C_{DMI}, C_{DQS_t}, C_{DQS_c}) in byte-lane.
9. Notes 1 and 2 apply to entire table.

I_{DD} Specification Parameters and Test Conditions

Table 217: I_{DD} Measurement Conditions

Switching for CA								
CK_t Edge	**R1**	**R2**	**R3**	**R4**	**R5**	**R6**	**R7**	**R8**
CKE	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
CS	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Notes: 1. LOW = $V_{IN} \leq V_{IL(DC)}$ MAX.
HIGH = $V_{IN} \geq V_{IH(DC)}$ MIN.
STABLE = Inputs are stable at a HIGH or LOW level.
2. CS must always be driven LOW.
3. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
4. The pattern is used continuously during I_{DD} measurement for I_{DD} values that require switching on the CA bus.

Table 218: CA Pattern for I_{DD4R} for BL = 16

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	READ-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	READ-1	L	H	L	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		H	H	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

Notes: 1. BA[2:0] = 010; C[9:4] = 000000 or 111111; Burst order C[3:2] = 00 or 11 (same as LPDDR3 I_{DDR4R} specification).
2. CA pins are kept LOW with DES command to reduce ODT current (different from LPDDR3 I_{DDR4R} specification).

Table 219: CA Pattern for I_{DD4W} for BL = 16

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	WRITE-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	WRITE-1	L	L	H	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		L	L	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

Notes: 1. BA[2:0] = 010; C[9:4] = 000000 or 111111 (same as LPDDR3 I_{DDR4W} specification).
2. No burst ordering (different from LPDDR3 I_{DDR4W} specification).
3. CA pins are kept LOW with DES command to reduce ODT current (different from LPDDR3 I_{DDR4W} specification).

Table 220: Data Pattern for I_{DD4W} (DBI Off) for BL = 16

DBI Off Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4

Table 220: Data Pattern for I_{DD4W} (DBI Off) for BL = 16 (Continued)

DBI Off Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
# of 1s	16	16	16	16	16	16	16	16		

Note: 1. Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] to reduce complexity for I_{DD4W} pattern programming.

Table 221: Data Pattern for I_{DD4R} (DBI Off) for BL = 16

DBI Off Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4

Table 221: Data Pattern for I_{DD4R} (DBI Off) for BL = 16 (Continued)

DBI Off Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL16	1	1	1	1	1	1	1	1	0	8
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	1	1	1	1	1	1	0	0	0	6
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	1	1	0	8
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	1	1	1	1	1	1	0	0	0	6
BL31	1	1	1	1	0	0	0	0	0	4
# of 1s	16	16	16	16	16	16	16	16		

Note: 1. Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] to reduce complexity for I_{DD4R} pattern programming.

Table 222: Data Pattern for I_{DD4W} (DBI On) for BL = 16

DBI On Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4

Table 222: Data Pattern for I_{DD4W} (DBI On) for BL = 16 (Continued)

DBI On Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
# of 1s	8	8	8	8	8	8	16	16	8	

Note: 1. DBI enabled burst: BL0, BL6, BL8, BL14, BL16, BL22, BL26, and BL28.

Table 223: Data Pattern for I_{DD4R} (DBI On) for BL = 16

DBI On Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4

Table 223: Data Pattern for I_{DD4R} (DBI On) for BL = 16 (Continued)

DBI On Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL16	0	0	0	0	0	0	0	0	1	1
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	1	3
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	0	0	1	1
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	0	0	0	0	0	0	1	1	1	3
BL31	1	1	1	1	0	0	0	0	0	4
# of 1s	8	8	8	8	8	8	16	16	8	

Note: 1. DBI enabled burst: BL0, BL6, BL8, BL14, BL20, BL26, and BL30.

Table 224: CA Pattern for I_{DD4R} for BL = 32

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	READ-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	LOW	DES	L	L	L	L	L	L
N+9	HIGH	LOW	DES	L	L	L	L	L	L
N+10	HIGH	LOW	DES	L	L	L	L	L	L
N+11	HIGH	LOW	DES	L	L	L	L	L	L
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L
N+16	HIGH	HIGH	READ-1	L	H	L	L	L	L

Table 224: CA Pattern for I_{DD4R} for BL = 32 (Continued)

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N+17	HIGH	LOW		L	H	L	L	H	L
N+18	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+19	HIGH	LOW		H	H	L	H	H	H
N+20	HIGH	LOW	DES	L	L	L	L	L	L
N+21	HIGH	LOW	DES	L	L	L	L	L	L
N+22	HIGH	LOW	DES	L	L	L	L	L	L
N+23	HIGH	LOW	DES	L	L	L	L	L	L
N+24	HIGH	LOW	DES	L	L	L	L	L	L
N+25	HIGH	LOW	DES	L	L	L	L	L	L
N+26	HIGH	LOW	DES	L	L	L	L	L	L
N+27	HIGH	LOW	DES	L	L	L	L	L	L
N+28	HIGH	LOW	DES	L	L	L	L	L	L
N+29	HIGH	LOW	DES	L	L	L	L	L	L
N+30	HIGH	LOW	DES	L	L	L	L	L	L
N+31	HIGH	LOW	DES	L	L	L	L	L	L

Note: 1. BA[2:0] = 010, C[9:5] = 00000 or 11111, Burst order C[4:2] = 000 or 111.

Table 225: CA Pattern for I_{DD4W} for BL = 32

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	WRITE-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	LOW	DES	L	L	L	L	L	L
N+9	HIGH	LOW	DES	L	L	L	L	L	L
N+10	HIGH	LOW	DES	L	L	L	L	L	L
N+11	HIGH	LOW	DES	L	L	L	L	L	L
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L
N+16	HIGH	HIGH	WRITE-1	L	L	H	L	L	L
N+17	HIGH	LOW		L	H	L	L	H	L
N+18	HIGH	HIGH	CAS-2	L	H	L	L	H	H

Table 225: CA Pattern for I_{DD4W} for BL = 32 (Continued)

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N+19	HIGH	LOW		L	L	L	H	H	H
N+20	HIGH	LOW	DES	L	L	L	L	L	L
N+21	HIGH	LOW	DES	L	L	L	L	L	L
N+22	HIGH	LOW	DES	L	L	L	L	L	L
N+23	HIGH	LOW	DES	L	L	L	L	L	L
N+24	HIGH	LOW	DES	L	L	L	L	L	L
N+25	HIGH	LOW	DES	L	L	L	L	L	L
N+26	HIGH	LOW	DES	L	L	L	L	L	L
N+27	HIGH	LOW	DES	L	L	L	L	L	L
N+28	HIGH	LOW	DES	L	L	L	L	L	L
N+29	HIGH	LOW	DES	L	L	L	L	L	L
N+30	HIGH	LOW	DES	L	L	L	L	L	L
N+31	HIGH	LOW	DES	L	L	L	L	L	L

Note: 1. BA[2:0] = 010, C[9:5] = 00000 or 11111.

Table 226: Data Pattern for I_{DD4W} (DBI Off) for BL = 32

DBI Off Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0

Table 226: Data Pattern for I_{DD4W} (DBI Off) for BL = 32 (Continued)

DBI Off Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	1	1	1	1	1	1	1	1	0	8
BL33	1	1	1	1	0	0	0	0	0	4
BL34	0	0	0	0	0	0	0	0	0	0
BL35	0	0	0	0	1	1	1	1	0	4
BL36	0	0	0	0	0	0	1	1	0	2
BL37	0	0	0	0	1	1	1	1	0	4
BL38	1	1	1	1	1	1	0	0	0	6
BL39	1	1	1	1	0	0	0	0	0	4
BL40	1	1	1	1	1	1	1	1	0	8
BL41	1	1	1	1	0	0	0	0	0	4
BL42	0	0	0	0	0	0	0	0	0	0
BL43	0	0	0	0	1	1	1	1	0	4
BL44	0	0	0	0	0	0	1	1	0	2
BL45	0	0	0	0	1	1	1	1	0	4
BL46	1	1	1	1	1	1	0	0	0	6
BL47	1	1	1	1	0	0	0	0	0	4
BL48	1	1	1	1	1	1	0	0	0	6
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	1	1	0	2
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	0	0	0	0
BL53	0	0	0	0	1	1	1	1	0	4
BL54	1	1	1	1	1	1	1	1	0	8
BL55	1	1	1	1	0	0	0	0	0	4
BL56	0	0	0	0	0	0	1	1	0	2
BL57	0	0	0	0	1	1	1	1	0	4
BL58	1	1	1	1	1	1	0	0	0	6

Table 226: Data Pattern for I_{DD4W} (DBI Off) for BL = 32 (Continued)

DBI Off Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL59	1	1	1	1	0	0	0	0	0	4
BL60	1	1	1	1	1	1	1	1	0	8
BL61	1	1	1	1	0	0	0	0	0	4
BL62	0	0	0	0	0	0	0	0	0	0
BL63	0	0	0	0	1	1	1	1	0	4
# of 1s	32	32	32	32	32	32	32	32		

Note: 1. Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] to reduce complexity for I_{DD4W} pattern programming.

Table 227: Data Pattern for I_{DD4R} (DBI Off) for BL = 32

DBI Off Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6

Table 227: Data Pattern for I_{DD4R} (DBI Off) for BL = 32 (Continued)

DBI Off Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	1	1	0	2
BL33	0	0	0	0	1	1	1	1	0	4
BL34	1	1	1	1	1	1	0	0	0	6
BL35	1	1	1	1	0	0	0	0	0	4
BL36	1	1	1	1	1	1	1	1	0	8
BL37	1	1	1	1	0	0	0	0	0	4
BL38	0	0	0	0	0	0	0	0	0	0
BL39	0	0	0	0	1	1	1	1	0	4
BL40	0	0	0	0	0	0	1	1	0	2
BL41	0	0	0	0	1	1	1	1	0	4
BL42	1	1	1	1	1	1	0	0	0	6
BL43	1	1	1	1	0	0	0	0	0	4
BL44	1	1	1	1	1	1	1	1	0	8
BL45	1	1	1	1	0	0	0	0	0	4
BL46	0	0	0	0	0	0	0	0	0	0
BL47	0	0	0	0	1	1	1	1	0	4
BL48	1	1	1	1	1	1	1	1	0	8
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	0	0	0	0
BL51	0	0	0	0	1	1	1	1	0	4
BL52	1	1	1	1	1	1	0	0	0	6
BL53	1	1	1	1	0	0	0	0	0	4
BL54	0	0	0	0	0	0	1	1	0	2
BL55	0	0	0	0	1	1	1	1	0	4
BL56	0	0	0	0	0	0	0	0	0	0
BL57	0	0	0	0	1	1	1	1	0	4
BL58	1	1	1	1	1	1	1	1	0	8
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	1	1	0	2
BL61	0	0	0	0	1	1	1	1	0	4
BL62	1	1	1	1	1	1	0	0	0	6
BL63	1	1	1	1	0	0	0	0	0	4
# of 1s	32	32	32	32	32	32	32	32		

Note: 1. Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] to reduce complexity for I_{DD4R} pattern programming.

Table 228: Data Pattern for I_{DD4W} (DBI On) for BL = 32

DBI On Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	0	0	1	1
BL33	1	1	1	1	0	0	0	0	0	4
BL34	0	0	0	0	0	0	0	0	0	0
BL35	0	0	0	0	1	1	1	1	0	4

Table 228: Data Pattern for I_{DD4W} (DBI On) for BL = 32 (Continued)

DBI On Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL36	0	0	0	0	0	0	1	1	0	2
BL37	0	0	0	0	1	1	1	1	0	4
BL38	0	0	0	0	0	0	1	1	1	3
BL39	1	1	1	1	0	0	0	0	0	4
BL40	0	0	0	0	0	0	0	0	1	1
BL41	1	1	1	1	0	0	0	0	0	4
BL42	0	0	0	0	0	0	0	0	0	0
BL43	0	0	0	0	1	1	1	1	0	4
BL44	0	0	0	0	0	0	1	1	0	2
BL45	0	0	0	0	1	1	1	1	0	4
BL46	0	0	0	0	0	0	1	1	1	3
BL47	1	1	1	1	0	0	0	0	0	4
BL48	0	0	0	0	0	0	1	1	1	3
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	1	1	0	2
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	0	0	0	0
BL53	0	0	0	0	1	1	1	1	0	4
BL54	0	0	0	0	0	0	0	0	1	1
BL55	1	1	1	1	0	0	0	0	0	4
BL56	0	0	0	0	0	0	1	1	0	2
BL57	0	0	0	0	1	1	1	1	0	4
BL58	0	0	0	0	0	0	1	1	1	3
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	0	0	1	1
BL61	1	1	1	1	0	0	0	0	0	4
BL62	0	0	0	0	0	0	0	0	0	0
BL63	0	0	0	0	1	1	1	1	0	4
# of 1s	16	16	16	16	16	16	32	32	16	

Note: 1. DBI enabled burst: BL0, BL6, BL8, BL14, BL16, BL22, BL26, BL28, BL32, BL38, BL40, BL46, BL48, BL54, BL58, and BL60.

Table 229: Data Pattern for I_{DD4R} (DBI On) for BL = 32

DBI On Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4

Table 229: Data Pattern for I_{DD4R} (DBI On) for BL = 32 (Continued)

DBI On Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	1	1	0	2
BL33	0	0	0	0	1	1	1	1	0	4
BL34	0	0	0	0	0	0	1	1	1	3
BL35	1	1	1	1	0	0	0	0	0	4
BL36	0	0	0	0	0	0	0	0	1	1
BL37	1	1	1	1	0	0	0	0	0	4
BL38	0	0	0	0	0	0	0	0	0	0
BL39	0	0	0	0	1	1	1	1	0	4
BL40	0	0	0	0	0	0	1	1	0	2
BL41	0	0	0	0	1	1	1	1	0	4

Table 229: Data Pattern for I_{DD4R} (DBI On) for BL = 32 (Continued)

DBI On Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL42	0	0	0	0	0	0	1	1	1	3
BL43	1	1	1	1	0	0	0	0	0	4
BL44	0	0	0	0	0	0	0	0	1	1
BL45	1	1	1	1	0	0	0	0	0	4
BL46	0	0	0	0	0	0	0	0	0	0
BL47	0	0	0	0	1	1	1	1	0	4
BL48	0	0	0	0	0	0	0	0	1	1
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	0	0	0	0
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	1	1	1	3
BL53	1	1	1	1	0	0	0	0	0	4
BL54	0	0	0	0	0	0	1	1	0	2
BL55	0	0	0	0	1	1	1	1	0	4
BL56	0	0	0	0	0	0	0	0	0	0
BL57	0	0	0	0	1	1	1	1	0	4
BL58	0	0	0	0	0	0	0	0	1	1
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	1	1	0	2
BL61	0	0	0	0	1	1	1	1	0	4
BL62	0	0	0	0	0	0	1	1	1	3
BL63	1	1	1	1	0	0	0	0	0	4
# of 1s	16	16	16	16	16	16	32	32	16	

Note: 1. DBI enabled burst: BL0, BL6, BL8, BL14, BL16, BL22, BL26, BL28, BL34, BL36, BL42, BL44, BL48, BL52, BL58, and BL62.

I_{DD} Specifications

I_{DD} values are for the entire operating voltage range, and all of them are for the entire standard temperature range.

Table 230: I_{DD} Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active-precharge current: $^{t}CK = {}^{t}CK$ (MIN); $^{t}RC = {}^{t}RC$ (MIN); CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD01}	V_{DD1}	
	I_{DD02}	V_{DD2}	
	I_{DD0Q}	V_{DDQ}	2
Idle power-down standby current: $^{t}CK = {}^{t}CK$ (MIN); CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD2P1}	V_{DD1}	
	I_{DD2P2}	V_{DD2}	
	I_{DD2PQ}	V_{DDQ}	2

Table 230: I_{DD} Specification Parameters and Operating Conditions (Continued)

Parameter/Condition	Symbol	Power Supply	Notes
Idle power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD2PS1}	V_{DD1}	
	I_{DD2PS2}	V_{DD2}	
	I_{DD2PSQ}	V_{DDQ}	2
Idle non-power-down standby current: ^{t}CK = ^{t}CK (MIN); CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD2N1}	V_{DD1}	
	I_{DD2N2}	V_{DD2}	
	I_{DD2NQ}	V_{DDQ}	2
Idle non-power-down standby current with clock stopped: CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD2NS1}	V_{DD1}	
	I_{DD2NS2}	V_{DD2}	
	I_{DD2NSQ}	V_{DDQ}	2
Active power-down standby current: ^{t}CK = ^{t}CK (MIN); CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD3P1}	V_{DD1}	
	I_{DD3P2}	V_{DD2}	
	I_{DD3PQ}	V_{DDQ}	2
Active power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD3PS1}	V_{DD1}	
	I_{DD3PS2}	V_{DD2}	
	I_{DD3PSQ}	V_{DDQ}	3
Active non-power-down standby current: ^{t}CK = ^{t}CK (MIN); CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD3N1}	V_{DD1}	
	I_{DD3N2}	V_{DD2}	
	I_{DD3NQ}	V_{DDQ}	3
Active non-power-down standby current with clock stopped: CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD3NS1}	V_{DD1}	
	I_{DD3NS2}	V_{DD2}	
	I_{DD3NSQ}	V_{DDQ}	3
Operating burst READ current: ^{t}CK = ^{t}CK (MIN); CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	I_{DD4R1}	V_{DD1}	
	I_{DD4R2}	V_{DD2}	
	I_{DD4RQ}	V_{DDQ}	4
Operating burst WRITE current: ^{t}CK = ^{t}CK (MIN); CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL = WL (MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	I_{DD4W1}	V_{DD1}	
	I_{DD4W2}	V_{DD2}	
	I_{DD4WQ}	V_{DDQ}	3
All-bank REFRESH burst current: ^{t}CK = ^{t}CK (MIN); CKE is HIGH between valid commands; ^{t}RC = ^{t}RFCab (MIN); Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD51}	V_{DD1}	
	I_{DD52}	V_{DD2}	
	I_{DD5Q}	V_{DDQ}	3
All-bank REFRESH average current: ^{t}CK = ^{t}CK (MIN); CKE is HIGH between valid commands; ^{t}RC = ^{t}REFI; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD5AB1}	V_{DD1}	
	I_{DD5AB2}	V_{DD2}	
	I_{DD5ABQ}	V_{DDQ}	3
Per-bank REFRESH average current: ^{t}CK = ^{t}CK (MIN); CKE is HIGH between valid commands; ^{t}RC = ^{t}REFI/8; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD5PB1}	V_{DD1}	
	I_{DD5PB2}	V_{DD2}	
	I_{DD5PBQ}	V_{DDQ}	3

Table 230: I_{DD} Specification Parameters and Operating Conditions (Continued)

Parameter/Condition	Symbol	Power Supply	Notes
Power-down self refresh current: CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate; ODT is disabled	I_{DD61}	V_{DD1}	5, 6
	I_{DD62}	V_{DD2}	5, 6
	I_{DD6Q}	V_{DDQ}	3, 5, 6

Notes: 1. ODT disabled: MR11[2:0] = 000b.
2. I_{DD} current specifications are tested after the device is properly initialized.
3. Measured currents are the summation of V_{DDQ} and V_{DD2}.
4. Guaranteed by design with output load = 5pF and R_{ON} = 40 ohm.
5. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh before going into the elevated temperature range.
6. This is the general definition that applies to full-array self refresh.
7. For all I_{DD} measurements, V_{IHCKE} = 0.8 × V_{DD2}; V_{ILCKE} = 0.2 × V_{DD2}.
8. LPDDR4: V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V
9. LPDDR4X: V_{DD2}= 1.06–1.17V; V_{DDQ} = 0.57–0.65V; V_{DD1} = 1.70–1.95V

AC Timing

Table 231: Clock Timing

Parameter	Symbol	Min/ Max	Data Rate				Unit
			1600	3200	3733	4267	
Average clock period	tCK(AVG)	Min	1250	625	535	468	ps
		Max	100	100	100	100	ns
Average HIGH pulse width	tCH(AVG)	Min	0.46				tCK(AVG)
		Max	0.54				
Average LOW pulse width	tCL(AVG)	Min	0.46				tCK(AVG)
		Max	0.54				
Absolute clock period	tCK(ABS)	Min	tCK(AVG)min + tJIT(per)min				ps
Absolute clock HIGH pulse width	tCH(ABS)	Min	0.43				tCK(AVG)
		Max	0.57				
Absolute clock LOW pulse width	tCL(ABS)	Min	0.43				tCK(AVG)
		Max	0.57				
Clock period jitter	tJIT(per)allowed	Min	–70	–40	–34	–30	ps
		Max	70	40	34	30	
Maximum clock jitter between two consecutive clock cycles (includes clock period jitter)	tJIT(cc)allowed	Max	140	80	68	60	ps

Table 232: Read Output Timing

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
DQS output access time from CK_t/CK_c	tDQSCK	Min	1500								ps	1
		Max	3500									
DQS output access time from CK_t/CK_c - voltage variation	tDQSCK_VOLT	Max	7								ps/mV	2
DQS output access time from CK_t/CK_c - temperature variation	tDQSCK_TEMP	Max	4								ps/°C	3
CK to DQS rank to rank variation	tDQSCK_rank2rank	Max	1.0								ns	4, 5
DQS_t, DQS_c to DQ skew total, per group, per access (DBI Disabled)	tDQSQ	Max	0.18								UI	6
DQ output hold time total from DQS_t, DQS_c (DBI Disabled)	tQH	Min	MIN(tQSH, tQSL)								ps	6
Data output valid window time total, per pin (DBI-Disabled)	tQW_total	Min	0.75			0.73		0.70			UI	6, 11

Table 232: Read Output Timing (Continued)

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
DQS_t, DQS_c to DQ skew total, per group, per access (DBI-Enabled)	^{t}DQSQ_DBI	Max	0.18								UI	6
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	^{t}QH_DBI	Min	MIN(^{t}QSH_DBI, ^{t}QSL_DBI)								ps	6
Data output valid window time total, per pin (DBI-Enabled)	^{t}QW_total_DBI	Min	0.75			0.73		0.70			UI	6, 11
DQS_t, DQS_c differential output LOW time (DBI-Disabled)	^{t}QSL	Min	^{t}CL(ABS) - 0.05								^{t}CK(AVG)	9, 11
DQS_t, DQS_c differential output HIGH time (DBI-Disabled)	^{t}QSH	Min	^{t}CH(ABS) - 0.05								^{t}CK(AVG)	10, 11
DQS_t, DQS_c differential output LOW time (DBI-Enabled)	^{t}QSL-DBI	Min	^{t}CL(ABS) - 0.045								^{t}CK(AVG)	9, 11
DQS_t, DQS_c differential output HIGH time (DBI-Enabled)	^{t}QSH-DBI	Min	^{t}CH(ABS) - 0.045								^{t}CK(AVG)	10, 11
Read preamble	^{t}RPRE	Min	1.8								^{t}CK(AVG)	
Read postamble	^{t}RPST	Min	0.4 (or 1.4 if extra postamble is programmed in MR)								^{t}CK(AVG)	
DQS Low-Z from clock	^{t}LZ(DQS)	Min	(RL × ^{t}CK) + ^{t}DQSCK(MIN) - (^{t}RPRE(MAX) × ^{t}CK) - 200ps								ps	
DQ Low-Z from clock	^{t}LZ(DQ)	Min	(RL × ^{t}CK) + ^{t}DQSCK(MIN) - 200ps								ps	
DQS High-Z from clock	^{t}HZ(DQS)	Max	(RL × ^{t}CK) + ^{t}DQSCK(MAX)+(BL/2 × ^{t}CK) + (^{t}RPST(MAX) × ^{t}CK) - 100ps								ps	
DQ High-Z from clock	^{t}HZ(DQ)	Max	(RL × ^{t}CK) + ^{t}DQSCK(MAX) + ^{t}DQSQ(MAX) + (BL/2 × ^{t}CK) - 100ps								ps	

Notes:
1. This parameter includes DRAM process, voltage, and temperature variation. It also includes the AC noise impact for frequencies >20 MHz and a max voltage of 45mV peak-to-peak from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply with the component MIN/MAX DC operating conditions.
2. ^{t}DQSCK_volt max delay variation as a function of DC voltage variation for $V_{DDQ}$and V_{DD2}. The voltage supply noise must comply with the component MIN/MAX DC operating conditions. The voltage variation is defined as the MAX[ABS(^{t}DQSCK(MIN)@V1 - ^{t}DQSCK(MAX)@V2), ABS(^{t}DQSCK(MAX)@V1 - ^{t}DQSCK(MIN)@V2)]/ABS(V1 - V2).
3. ^{t}DQSCK_temp MAX delay variation as a function of temperature.
4. The same voltage and temperature are applied to ^{t}DQSCK_rank2rank.
5. ^{t}DQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design die.
6. DQ-to-DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER.
7. The deterministic component of the total timing.
8. This parameter will be characterized and guaranteed by design.

9. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from one falling edge to the next consecutive rising edge.
10. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from one falling edge to the next consecutive rising edge.
11. This parameter is a function of input clock jitter. These values assume MIN tCH(ABS) and tCL(ABS). When the input clock jitter MIN tCH(ABS) and tCL(ABS) is 0.44 or greater than tCK(AVG), the minimum value of tQSL will be tCL(ABS) - 0.04 and tQSH will be tCH(ABS) - 0.04.

Table 233: Write Timing

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
Rx timing window total at V_{dIVW} voltage levels	TdIVW_total	Max	0.22					0.25			UI	1, 2, 3
DQ and DMI input pulse width (at V_{CENT_DQ})	TdIPW	Min	0.45								UI	7
DQ-to-DQS offset	tDQS2DQ	Min	200								ps	6
		Max	800									
DQ-to-DQ offset	tDQDQ	Max	30								ps	7
DQ-to-DQS offset temperature variation	tDQS2DQ_temp	Max	0.6								ps/°C	8
DQ-to-DQS offset voltage variation	tDQS2DQ_volt	Max	33								ps/50mV	9
DQ-to-DQS offset rank to rank variation	tDQS2DQ_rank2rank	Max	200								ps	10, 11
WRITE command to first DQS transition	tDQSS	Min	0.75								tCK(AVG)	
		Max	1.25									
DQS input HIGH-level width	tDQSH	Min	0.4								tCK(AVG)	
DQS input LOW-level width	tDQSL	Min	0.4								tCK(AVG)	
DQS falling edge to CK setup time	tDSS	Min	0.2								tCK(AVG)	
DQS falling edge from CK hold time	tDSH	Min	0.2								tCK(AVG)	
Write postamble	tWPST	Min	0.4 (or 1.4 if extra postamble is programmed in MR)								tCK(AVG)	
Write preamble	tWPRE	Min	1.8								tCK(AVG)	

Notes: 1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies >20 MHz with a maximum voltage of 45mV peak-to-peak at a fixed temperature on the package. The voltage supply noise must comply to the component MIN/MAX DC operating conditions.
2. Rx differential DQ-to-DQS jitter total timing window at the V_{dIVW} voltage levels.
3. Defined over the DQ internal V_{REF} range. The Rx mask at the pin must be within the internal $V_{REF(DQ)}$ range irrespective of the input signal common mode.
4. Rx mask defined for one pin toggling with other DQ signals in a steady state.
5. DQ-only minimum input pulse width defined at the $V_{CENT\_DQ(pin\_mid)}$.
6. DQ-to-DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage, and temperature variations.
7. DQ-to-DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.

8. ^{t}DQS2DQ(MAX) delay variation as a function of temperature.
9. ^{t}DQS2DQ(MAX) delay variation as a function of the DC voltage variation for V_{DDQ} and V_{DD2}. It includes the V_{DDQ} and V_{DD2} AC noise impact for frequencies >20 MHz and MAX voltage of 45mV peak-to-peak from DC-20 MHz at a fixed temperature on the package.
10. The same voltage and temperature are applied to ^{t}DQS2DQ_rank2rank.
11. ^{t}DQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design die.
12. UI = ^{t}CK(AVG)(MIN)/2.

Table 234: CKE Input Timing

Parameter	Symbol	Min/ Max	Data Rate				Unit	Notes
			1600	3200	3733	4267		
CKE minimum pulse width (HIGH and LOW pulse width)	^{t}CKE	Min	MAX(7.5ns, 4*n*CK)				ns	1
Delay from valid command to CKE input LOW	^{t}CMDCKE	Min	MAX(1.75ns, 3*n*CK)				ns	1
Valid clock requirement after CKE input LOW	^{t}CKELCK	Min	MAX(5ns, 5*n*CK)				ns	1
Valid CS requirement before CKE input LOW	^{t}CSCKE	Min	1.75				ns	
Valid CS requirement after CKE input LOW	^{t}CKELCS	Min	MAX(5ns, 5*n*CK)				ns	1
Valid Clock requirement before CKE Input HIGH	^{t}CKCKEH	Min	MAX(1.75ns, 3*n*CK)				ns	1
Exit power-down to next valid command delay	^{t}XP	Min	MAX(7.5ns, 5*n*CK)				ns	1
Valid CS requirement before CKE input HIGH	^{t}CSCKEH	Min	1.75				ns	
Valid CS requirement after CKE input HIGH	^{t}CKEHCS	Min	MAX(7.5ns, 5*n*CK)				ns	1
Valid clock and CS requirement after CKE input LOW after MRW command	^{t}MRWCKEL	Min	MAX(14ns, 10*n*CK)				ns	1
Valid clock and CS requirement after CKE input LOW after ZQCAL START command	^{t}ZQCKE	Min	MAX(1.75ns, 3*n*CK)				ns	1

Note: 1. Delay time has to satisfy both analog time(ns) and clock count (*n*CK). For example, ^{t}CMDCKE will not expire until CK has toggled through at least 3 full cycles (3^{t}CK) and 3.75ns has transpired. The case that 3*n*CK is applied to is shown below.

Figure 248: tCMDCKE Timing

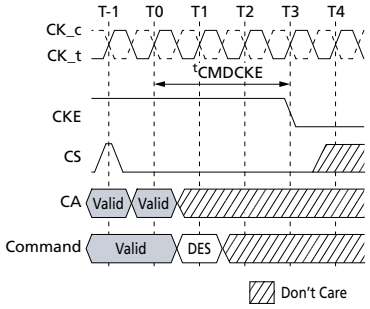


Table 235: Command Address Input Timing

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
Command/address valid window (referenced from CA V_{IL}/V_{IH} to CK V_{IX})	tcIVW	Min	0.3								tCK(AVG)	1, 2, 3
Address and control input pulse width (referenced to V_{REF})	tcIPW	Min	0.55	0.55	0.55	0.6	0.6	0.6	0.6	0.6	tCK(AVG)	4

Notes: 1. CA Rx mask timing parameters at the pin including voltage and temperature drift.
2. Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
3. Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal $V_{REF(CA)}$ range irrespective of the input signal common mode.
4. CA only minimum input pulse width defined at the V_{CENT_CA}(pin mid).

Table 236: Boot Timing Parameters (10–55 MHz)

Parameter	Symbol	Min/ Max	Value	Unit
Clock cycle time	tCKb	Min	18	ns
		Max	100	
DQS output data acess time from CK	tDQSCKb	Min	1.0	ns
		Max	10.0	
DQS edge to output data edge	tDQSQb	Max	1.2	ns

Table 237: Mode Register Timing Parameters

Parameter	Symbol	Min/ Max	Data Rate				Unit
			1600	3200	3733	4267	
MODE REGISTER WRITE (MRW) command period	tMRW	Min	MAX(10ns, 10*n*CK)				ns
MODE REGISTER SET command delay	tMRD	Min	MAX(14ns, 10*n*CK)				ns
MODE REGISTER READ (MRR) command period	tMRR	Min	8				tCK(AVG)

Table 237: Mode Register Timing Parameters (Continued)

Parameter	Symbol	Min/ Max	Data Rate				Unit
			1600	3200	3733	4267	
Additional time after tXP has expired until the MRR command may be issued	tMRRI	Min	tRCD(MIN) + 3*n*CK				ns
Delay from MRW command to DQS driven out	tSDO	Max	MAX(12*n*CK, 20ns)				ns

Table 238: Core Timing Parameters

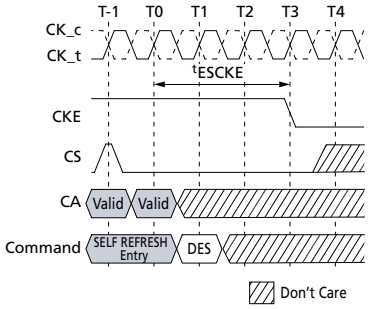
Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
READ latency (DBI disabled)	RL-A	Min	6	10	14	20	24	28	32	36	tCK(AVG)	
READ latency (DBI enabled)	RL-B	Min	6	12	16	22	28	32	36	40	tCK(AVG)	
WRITE latency (Set A)	WL-A	Min	4	6	8	10	12	14	16	18	tCK(AVG)	
WRITE latency (Set B)	WL-B	Min	4	8	12	18	22	26	30	34	tCK(AVG)	
ACTIVATE-to-ACTIVATE command period (same bank)	tRC	Min	tRAS + tRPab (with all-bank precharge) tRAS + tRPpb (with per-bank precharge)								ns	
Minimum self refresh time (entry to exit)	tSR	Min	MAX(15ns, 3*n*CK)								ns	
Self refresh exit to next valid command delay	tXSR	Min	MAX(tRFCab + 7.5ns, 2*n*CK)								ns	
CAS-to-CAS delay	tCCD	Min	8								tCK(AVG)	
CAS-to-CAS delay masked write	tCCDMW	Min	32								tCK(AVG)	
Internal READ-to-PRECHARGE command delay	tRTP	Min	MAX(7.5ns, 8*n*CK)								ns	
RAS-to-CAS delay	tRCD	Min	MAX(18ns, 4*n*CK)								ns	
Row precharge time (single bank)	tRPpb	Min	MAX(18ns, 3*n*CK)								ns	
Row precharge time (all banks)	tRPab	Min	MAX(21ns, 3*n*CK)								ns	
Row active time	tRAS	Min	MAX(42ns, 3*n*CK)								ns	
		Max	MIN(9 × tREFI × Refresh Rate, 70.2)								µs	
Write recovery time	tWR	Min	MAX(18ns, 4*n*CK)								ns	
Write-to-read delay	tWTR	Min	MAX(10ns, 8*n*CK)								ns	
Active bank A to active bank B	tRRD	Min	MAX(10ns, 4*n*CK)							MAX(7.5ns, 4*n*CK)	ns	1
Precharge-to-precharge delay	tPPD	Min	4								tCK(AVG)	2

Table 238: Core Timing Parameters (Continued)

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
Four-bank activate window	tFAW	Min	40							30	ns	1
Delay from SRE command to CKE input LOW	tESCKE	Min	MAX(1.75ns, 3*n*CK)								–	3

Notes: 1. 4267 Mb/s timing value is supported at lower data rates if the device is supporting 4266 Mb/s speed grade.
2. Precharge to precharge timing restriction does not apply to AUTO PRECHARGE commands.
3. Delay time has to satisfy both analog time (ns) and clock count (*n*CK). It means that tESCKE will not expire until CK has toggled through at least three full cycles (3 tCK) and 1.75ns has transpired. The case which 3*n*CK is applied to is shown below.

Figure 249: tESCKE Timing



4. The refresh rate is determined by the value in MR4 OP[2:0].

Table 239: CA Bus ODT Timing

Parameter	Symbol	Min/ Max	Data Rate
			533-4267
CA ODT value update time	tODTUP	Min	RU(20ns/tCK(AVG))

Table 240: CA Bus Training Parameters

Parameter	Symbol	Min/ Max	Data Rate				Unit	Notes
			1600	3200	3733	4267		
Valid clock requirement after CKE input LOW	tCKELCK	Min	MAX(5ns, 5*n*CK)				tCK	
Data setup for V_{REF} training mode	tDStrain	Min	2				ns	
Data hold for V_{REF} training mode	tDHtrain	Min	2				ns	
Asynchronous data read	tADR	Max	20				ns	
CA BUS TRAINING command-to-command delay	tCACD	Min	RU(tADR/tCK)				tCK	1
Valid strobe requirement before CKE LOW	tDQSCKE	Min	10				ns	
First CA BUS TRAINING command following CKE LOW	tCAENT	Min	250				ns	
V_{REF} step time – multiple steps	tVREFca_LONG	Max	250				ns	

Table 240: CA Bus Training Parameters (Continued)

Parameter	Symbol	Min/ Max	Data Rate				Unit	Notes
			1600	3200	3733	4267		
V_{REF} step time – one step	tVREFca_ SHORT	Max	80				ns	
Valid clock requirement before CS HIGH	tCKPRECS	Min	2tCK + tXP				–	
Valid clock requirement after CS HIGH	tCKPSTCS	Min	MAX(7.5ns, 5*n*CK)				–	
Minimum delay from CS to DQS toggle in command bus training	tCS_VREF	Min	2				tCK	
Minimum delay from CKE HIGH to strobe High-Z	tCKEHDQS	Min	10				ns	
CA bus training CKE HIGH to DQ tri-state	tMRZ	Min	1.5				ns	
ODT turn-on latency from CKE	tCKELODTon	Min	20				ns	
ODT turn-off latency from CKE	tCKEHODToff	Min	20				ns	
Exit command bus training mode to next valid command delay	tXCBT_Short	Min	MAX(200ns, 5*n*CK)				–	2
	tXCBT_Middle	Min	MAX(200ns, 5*n*CK)				–	2
	tXCBT_Long	Min	MAX(250ns, 5*n*CK)				–	2

Notes: 1. If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.

2. Exit command bus training mode to next valid command delay time depends on value of $V_{REF(CA)}$ setting: MR12 OP[5:0] and $V_{REF(CA)}$ range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in tFC value mapping table. Additionally exit command bus training mode to next valid command delay time may affect $V_{REF(DQ)}$ setting. Settling time of $V_{REF(DQ)}$ level is same as $V_{REF(CA)}$ level.

Table 241: Asynchronous ODT Turn On and Turn Off Timing

Symbol	800–2133 MHz	Unit
tODTon(MIN)	1.5	ns
tODTon(MAX)	3.5	ns
tODToff(MIN)	1.5	ns
tODToff(MAX)	3.5	ns

Table 242: Temperature Derating Parameters

Parameter	Symbol	Min/ Max	Data Rate				Unit
			1600	3200	3733	4267	
DQS output access time from CK_t/ CK_c (derated)	tDQSCKd	Max	3600				ps
RAS-to-CAS delay (derated)	tRCDd	Min	tRCD + 1.875				ns
ACTIVATE-to-ACTIVATE command period (same bank, derated)	tRCd	Min	tRC + 3.75				ns
Row active time (derated)	tRASd	Min	tRAS + 1.875				ns
Row precharge time (derated)	tRPd	Min	tRP + 1.875				ns
Active bank A to active bank B (derated)	tRRDd	Min	tRRD + 1.875				ns

Note: 1. At higher temperatures (>85°C), AC timing derating may be required. If derating is required the device will set MR4 OP[2:0] = 110b.

CA Rx Voltage and Timing

The command and address (CA), including CS input receiver compliance mask for voltage and timing, is shown in the CA Receiver (Rx) Mask figure below. All CA and CS signals apply the same compliance mask and operate in single data rate mode.

The CA input Rx mask for voltage and timing is applied across all pins, as shown in the figure below. The Rx mask defines the area that the input signal must not encroach if the DRAM input receiver is expected to successfully capture a valid input signal; it is not the valid data eye.

Figure 250: CA Receiver (Rx) Mask

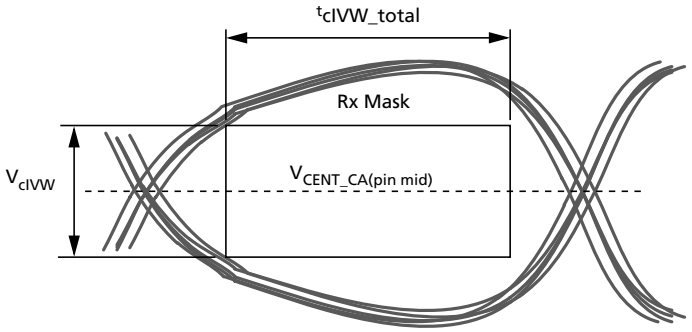
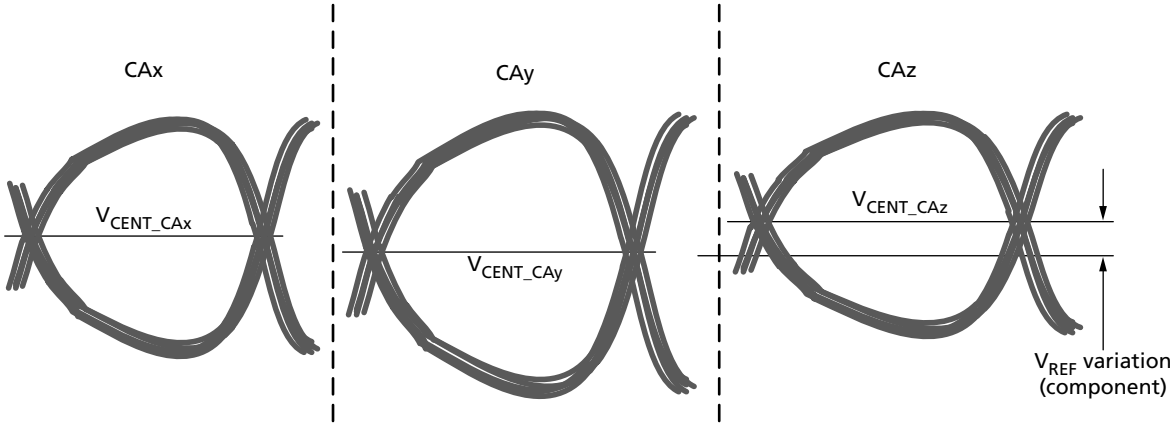
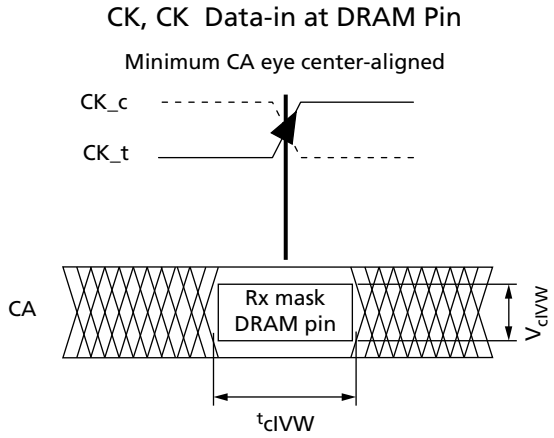


Figure 251: Across Pin $V_{REF\ (CA)}$ Voltage Variation



$V_{CENT\_CA(pin\ mid)}$ is defined as the midpoint between the largest V_{CENT_CA} voltage level and the smallest V_{CENT_CA} voltage level across all CA and CS pins for a given DRAM component. Each CA V_{CENT} level is defined by the center, which is, the widest opening of the cumulative data input eye, as depicted in the figure above. This clarifies that any DRAM component level variation must be accounted for within the CA Rx mask. The component-level V_{REF} will be set by the system to account for R_{ON} and ODT settings.

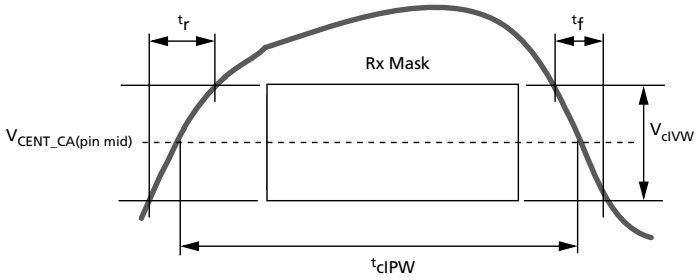
Figure 252: CA Timings at the DRAM Pins



TcIVW for all CA signals is defined as centered on the CK_t/CK_c crossing at the DRAM pin.

Note: 1. All of the timing terms in above figure are measured from the CK_t/CK_c to the center (midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around $V_{CENT\_CA(pin\ mid)}$.

Figure 253: CA ^{t}cIPW and SRIN_cIVW Definition (for Each Input Pulse)



Note: 1. SRIN_cIVW = V_{dIVW_total}/(^{t}r or ^{t}f); signal must be monotonic within ^{t}r and ^{t}f range.

Figure 254: CA V_{IHL_AC}Definition (for Each Input Pulse)

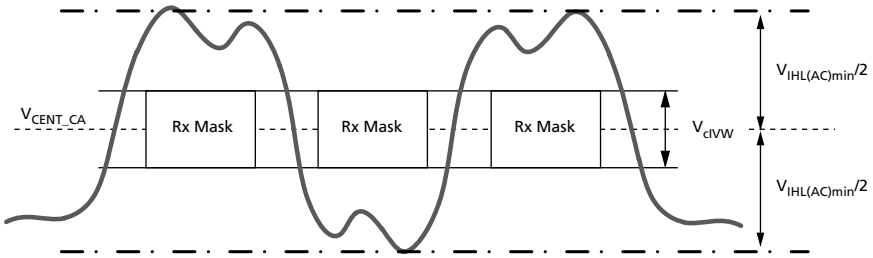


Table 243: DRAM CMD/ADR, CS

Symbol	Parameter	DQ – 1333[7]		DQ – 1600/1867		DQ – 3200/3733		DQ – 4267		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
V_{cIVW}	Rx mask voltage peak-to-peak	–	175	–	175	–	155	–	145	mV	1, 2, 3
$V_{IHL(AC)}$	CA AC input pulse amplitude peak-to-peak	210	–	210	–	190	–	180	–	mV	4, 6

Table 243: DRAM CMD/ADR, CS (Continued)

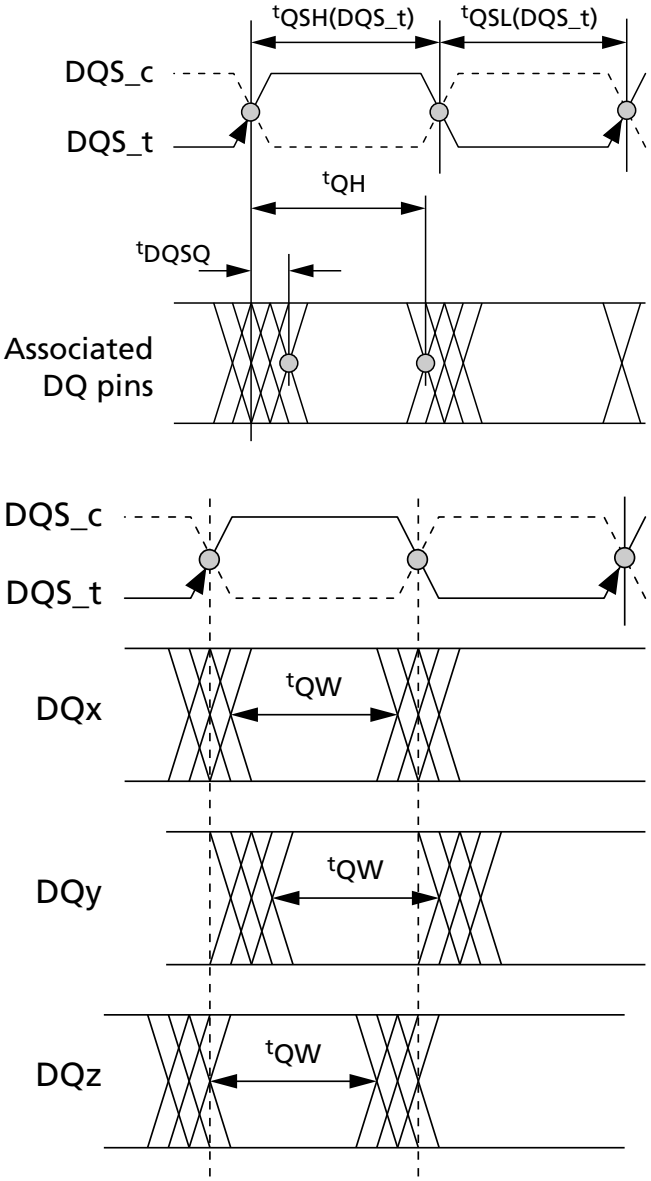
Symbol	Parameter	DQ – 1333[7]		DQ – 1600/1867		DQ – 3200/3733		DQ – 4267		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
SRIN_ clVW	Input slew rate over V_{clVW}	1	7	1	7	1	7	1	7	V/ns	5

Notes: 1. CA Rx mask voltage and timing parameters at the pin, including voltage and temperature drift.
2. Rx mask voltage V_{clVW} total(MAX) must be centered around $V_{CENT\_CA(pin\ mid)}$.
3. Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal $V_{REF(CA)}$ range irrespective of the input signal common mode.
4. CA-only input pulse signal amplitude into the receiver must meet or exceed $V_{IHL(AC)}$ at any point over the total UI. No timing requirement above level. $V_{IHL(AC)}$ is the peak-to-peak voltage centered around $V_{CENT\_CA(pin\ mid)}$, such that $V_{IHL(AC)}/2$ (MIN) must be met both above and below V_{CENT_CA}.
5. Input slew rate over V_{clVW} mask is centered at $V_{CENT\_CA(pin\ mid)}$.
6. $V_{IHL(AC)}$ does not have to be met when no transitions are occurring.
7. The Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the ^{t}cIVW (ps) = 450ps at or below 1333 operating frequencies.
8. UI = ^{t}CK(AVG)MIN.

DQ Tx Voltage and Timing

DRAM Data Timing

Figure 255: Read Data Timing Definitions – ^{t}QH and ^{t}DQSQ Across DQ Signals per DQS Group



DQ Rx Voltage and Timing

The DQ input receiver mask for voltage and timing is applied per pin, as shown in the DQ Receiver (Rx) Mask figure below. The total mask (V_{dIVW_total}, TdIVW_total) defines the area that the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal. The mask is a receiver property, and it is not the valid data eye.

Figure 256: DQ Receiver (Rx) Mask

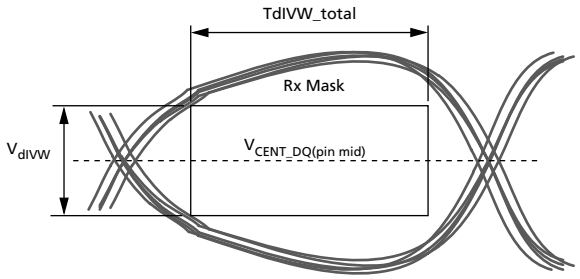
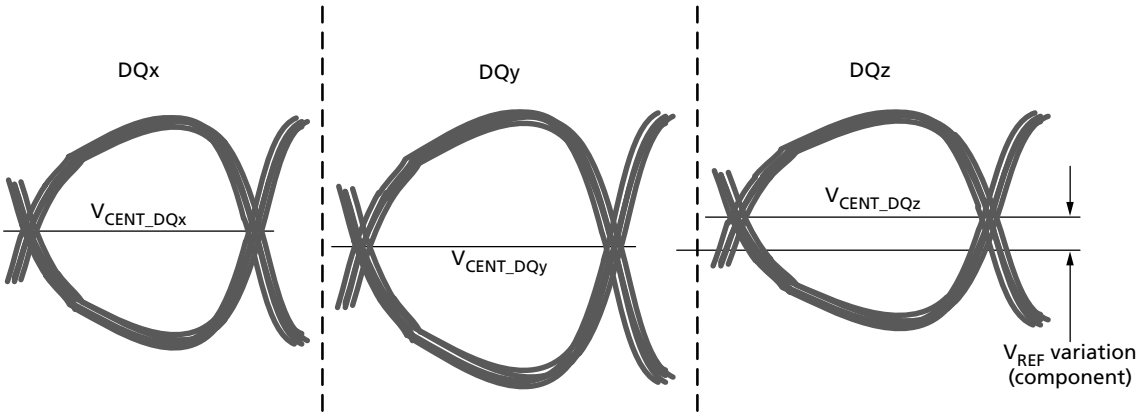
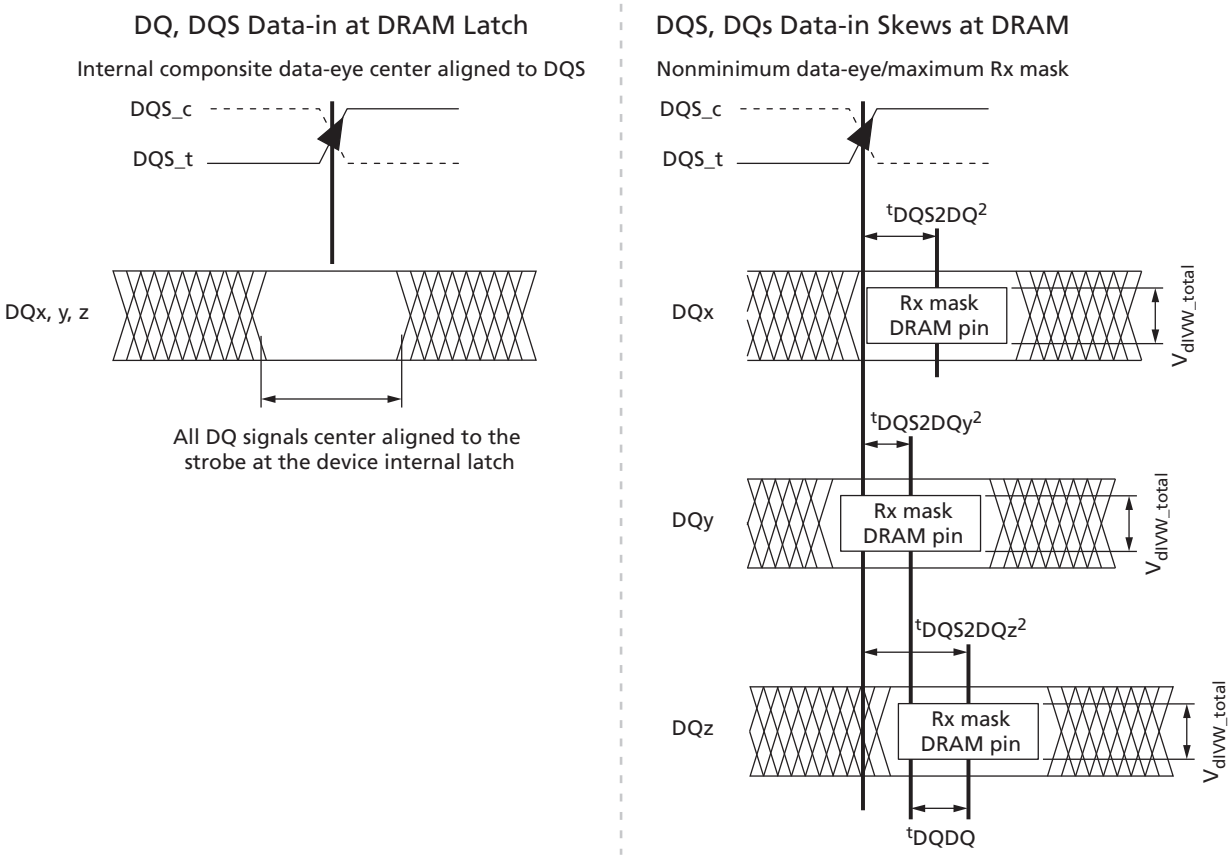


Figure 257: Across Pin V_{REF} DQ Voltage Variation



$V_{CENT\_DQ(pin\_mid)}$ is defined as the midpoint between the largest V_{CENT_DQ} voltage level and the smallest V_{CENT_DQ} voltage level across all DQ pins for a given DRAM component. Each V_{CENT_DQ} is defined by the center, which is the widest opening of the cumulative data input eye as shown in the figure above. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component-level V_{REF} will be set by the system to account for R_{ON} and ODT settings.

Figure 258: DQ-to-DQS ^{t}DQS2DQ and ^{t}DQDQ

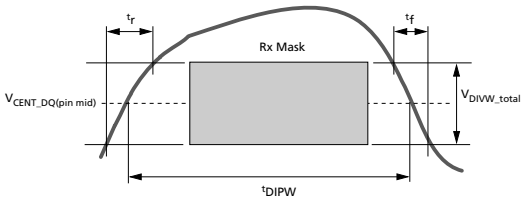


Notes: 1. These timings at the DRAM pins are referenced from the internal latch.
2. ^{t}DQS2DQ is measured at the center (midpoint) of the TdIVW window.
3. DQz represents the MAX ^{t}DQS2DQ in this example.
4. DQy represents the MIN ^{t}DQS2DQ in this example.

All of the timing terms in DQ to DQS_t are measured from the DQS_t/DQS_c to the center (midpoint) of the TdIVW window taken at the V_{dIVW_total} voltage levels centered around $V_{CENT\_DQ(pin\_mid)}$. In figure above, the timings at the pins are referenced with respect to all DQ signals center-aligned to the DRAM internal latch. The data-to-data offset is defined as the difference between the MIN and MAX ^{t}DQS2DQ for a given component.

Figure 259: DQ ^{t}DIPW and SRIN_dIVW Definition for Each Input Pulse

UI = ^{t}CK(AVG) MIN/2



Note: 1. SRIN_dIVW = V_{dIVW_total}/(^{t}r or ^{t}f) signal must be monotonic within ^{t}r and ^{t}f range.

Figure 260: DQ $V_{IHL(AC)}$ Definition (for Each Input Pulse)

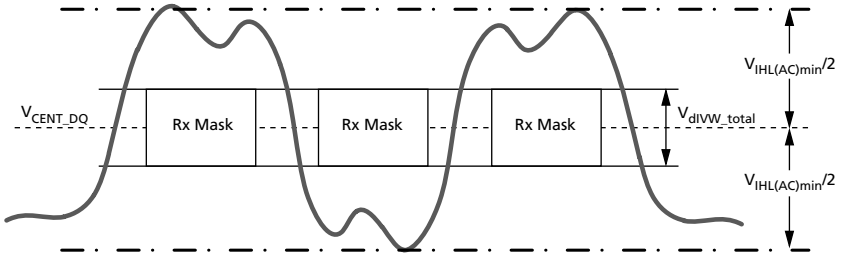


Table 244: DQs In Receive Mode

Symbol	Parameter	1600/1867		2133/2400		3200/3733		4267		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
V_{dIVW_total}	Rx mask voltage – peak-to-peak	–	140	–	140	–	140	–	120	mV	1, 2, 3
$V_{IHL(AC)}$	DQ AC input pulse amplitude peak-to-peak	180	–	180	–	180	–	170	–	mV	1, 7
SRIN_dIVW	Input slew rate over V_{dIVW_total}	1	7	1	7	1	7	1	7	V/ns	6

Notes: 1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies >20 MHz with a maximum voltage of 45mV peak-to-peak at a fixed temperature on the package. The voltage supply noise must comply to the component MIN/MAX DC operating conditions.
2. Rx mask voltage V_{dIVW_total}(MAX) must be centered around $V_{CENT\_DQ(pin\_mid)}$.
3. Defined over the DQ internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} DQ range irrespective of the input signal common mode.
4. Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design.
5. DQ-only input pulse amplitude into the receiver must meet or exceed $V_{IHL(AC)}$ at any point over the total UI. No timing requirement above level. $V_{IHL(AC)}$ is the peak-to-peak voltage centered around $V_{CENT\_DQ(pin\_mid)}$, such that $V_{IHL(AC)}/2$ (MIN) must be met both above and below V_{CENT_DQ}.
6. Input slew rate over V_{dIVW} mask centered at $V_{CENT\_DQ(pin\_mid)}$.
7. $V_{IHL(AC)}$ does not have to be met when no transitions are occurring.
8. UI = ^{t}CK(AVG)(MIN)/2.

Clock Specification

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violating minimum or maximum values may result in device malfunction.

Table 245: Definitions and Calculations

Symbol	Description	Calculation	Notes
^{t}CK(avg) and *n*CK	The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge. Unit ^{t}CK(avg) represents the actual clock average ^{t}CK(avg) of the input clock under operation. Unit *n*CK represents one clock cycle of the input clock, counting from actual clock edge to actual clock edge. ^{t}CK(avg) can change no more than ±1% within a 100-clock-cycle window, provided that all jitter and timing specifications are met.	$^{t}CK(avg) = \left(\sum_{j=1}^{N} {}^{t}CK_{j}\right)/N$ Where N = 200	
^{t}CK(abs)	The absolute clock period, as measured from one rising clock edge to the next consecutive rising clock edge.		1
^{t}CH(avg)	The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses.	$^{t}CH(avg) = \left(\sum_{j=1}^{N} {}^{t}CH_{j}\right)/(N \times {}^{t}CK(avg))$ Where N = 200	
^{t}CL(avg)	The average LOW pulse width, as calculated across any 200 consecutive LOW pulses.	$^{t}CL(avg) = \left(\sum_{j=1}^{N} {}^{t}CL_{j}\right)/(N \times {}^{t}CK(avg))$ Where N = 200	
^{t}JIT(per)	The single-period jitter defined as the largest deviation of any signal ^{t}CK from ^{t}CK(avg).	$^{t}JIT(per) = \min/\max \text{ of } \left({}^{t}CK_{i} - {}^{t}CK(avg)\right)$ Where i = 1 to 200	1
^{t}JIT(per),act	The actual clock jitter for a given system.		
^{t}JIT(per), allowed	The specified clock period jitter allowance.		
^{t}JIT(cc)	The absolute difference in clock periods between two consecutive clock cycles. ^{t}JIT(cc) defines the cycle-to-cycle jitter.	$^{t}JIT(cc) = \max \text{ of } \left({}^{t}CK_{i+1} - {}^{t}CK_{i}\right)$	1
^{t}ERR(nper)	The cumulative error across *n* multiple consecutive cycles from ^{t}CK(avg).	$^{t}ERR(nper) = \left(\sum_{j=i}^{i+n-1} {}^{t}CK_{j}\right) - (n \times {}^{t}CK(avg))$	1
^{t}ERR(nper),act	The actual clock jitter over *n* cycles for a given system.		
^{t}ERR(nper), allowed	The specified clock jitter allowance over *n* cycles.		
^{t}ERR(nper),min	The minimum ^{t}ERR(nper).	$^{t}ERR(nper),min = (1 + 0.68LN(n)) \times {}^{t}JIT(per),min$	2
^{t}ERR(nper),max	The maximum ^{t}ERR(nper).	$^{t}ERR(nper),max = (1 + 0.68LN(n)) \times {}^{t}JIT(per),max$	2
^{t}JIT(duty)	Defined with absolute and average specifications for ^{t}CH and ^{t}CL, respectively.	$^{t}JIT(duty),min = MIN(({}^{t}CH(abs),min - {}^{t}CH(avg),min), ({}^{t}CL(abs),min - {}^{t}CL(avg),min)) \times {}^{t}CK(avg)$ $^{t}JIT(duty),max = MAX(({}^{t}CH(abs),max - {}^{t}CH(avg),max), ({}^{t}CL(abs),max - {}^{t}CL(avg),max)) \times {}^{t}CK(avg)$	

Notes: 1. Not subject to production testing.
2. Using these equations, ^{t}ERR(nper) tables can be generated for each ^{t}JIT(per),act value.

^{t}CK(abs), ^{t}CH(abs), and ^{t}CL(abs)

These parameters are specified with their average values; however, the relationship between the average timing and the absolute instantaneous timing (defined in the following table) is applicable at all times.

Table 246: ^{t}CK(abs), ^{t}CH(abs), and ^{t}CL(abs) Definitions

Parameter	Symbol	Minimum	Unit
Absolute clock period	^{t}CK(abs)	^{t}CK(avg),min + ^{t}JIT(per),min	ps[1]
Absolute clock HIGH pulse width	^{t}CH(abs)	^{t}CH(avg),min + ^{t}JIT(duty),min[2]/^{t}CK(avg),min	^{t}CK(avg)
Absolute clock LOW pulse width	^{t}CL(abs)	^{t}CL(avg),min + ^{t}JIT(duty),min[2]/^{t}CK(avg),min	^{t}CK(avg)

Notes: 1. ^{t}CK(avg),min is expressed in ps for this table.
2. ^{t}JIT(duty),min is a negative value.

Clock Period Jitter

LPDDR4 devices can tolerate some clock period jitter without core timing parameter derating. This section describes device timing requirements with clock period jitter (^{t}JIT(per)) in excess of the values found in the AC Timing table. Calculating cycle time derating and clock cycle derating are also described.

Clock Period Jitter Effects on Core Timing Parameters

Core timing parameters (^{t}RCD, ^{t}RP, ^{t}RTP, ^{t}WR, ^{t}WRA, ^{t}WTR, ^{t}RC, ^{t}RAS, ^{t}RRD, ^{t}FAW) extend across multiple clock cycles. Clock period jitter impacts these parameters when measured in numbers of clock cycles. Within the specification limits, the device is characterized and verified to support ^{t}nPARAM = RU[^{t}PARAM/^{t}CK(avg)]. During device operation where clock jitter is outside specification limits, the number of clocks, or ^{t}CK(avg), may need to be increased based on the values for each core timing parameter.

Cycle Time Derating for Core Timing Parameters

For a given number of clocks (^{t}nPARAM), when ^{t}CK(avg) and ^{t}ERR(^{t}nPARAM),act exceed ^{t}ERR(^{t}nPARAM),allowed, cycle time derating may be required for core timing parameters.

$$\text{CycleTimeDerating} = \max\left\{\left(\frac{{}^{t}\text{PARAM} + {}^{t}\text{ERR}({}^{t}\text{nPARAM}),\text{act} - {}^{t}\text{ERR}({}^{t}\text{nPARAM}),\text{allowed}}{{}^{t}\text{nPARAM}} - {}^{t}\text{CK(avg)}\right), 0\right\}$$

Cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time deratings determined for each individual core timing parameter.

Clock Cycle Derating for Core Timing Parameters

For each core timing parameter and a given number of clocks (^{t}nPARAM), clock cycle derating should be specified with ^{t}JIT(per).

For a given number of clocks (^{t}nPARAM), when ^{t}CK(avg) plus (^{t}ERR(^{t}nPARAM),act) exceed the supported cumulative ^{t}ERR(^{t}nPARAM),allowed, derating is required. If the equation below results in a positive value for a core timing parameter (^{t}CORE), the required clock cycle derating will be that positive value (in clocks).

$$\text{ClockCycleDerating} = \text{RU}\left\{\frac{{}^{t}\text{PARAM} + {}^{t}\text{ERR}({}^{t}\text{nPARAM}),\text{act} - {}^{t}\text{ERR}({}^{t}\text{nPARAM}),\text{allowed}}{{}^{t}\text{CK(avg)}}\right\} - {}^{t}\text{nPARAM}$$

Cycle-time derating analysis should be conducted for each core timing parameter.

Clock Jitter Effects on Command/Address Timing Parameters

Command/address timing parameters (^{t}IS, ^{t}IH, ^{t}ISb, ^{t}IHb) are measured from a command/address signal (CS or CA[5:0]) transition edge to its respective clock signal (CK_t/CK_c) crossing. The specification values are not affected by the ^{t}JIT(per) applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

Clock Jitter Effects on READ Timing Parameters

^{t}RPRE

When the device is operated with input clock jitter, ^{t}RPRE must be derated by the ^{t}JIT(per),act,max of the input clock that exceeds ^{t}JIT(per),allowed,max. Output deratings are relative to the input clock:

$$^{t}\text{RPRE(min,derated)} = 0.9 - \left(\frac{^{t}\text{JIT(per),act,max} - ^{t}\text{JIT(per),allowed,max}}{^{t}\text{CK(avg)}}\right)$$

For example, if the measured jitter into a LPDDR4 device has ^{t}CK(avg) = 625ps, ^{t}JIT(per),act,min = –xx, and ^{t}JIT(per),act,max = +xx ps, then ^{t}RPRE,min,derated = 0.9 - (^{t}JIT(per),act,max - ^{t}JIT(per),allowed,max)/^{t}CK(avg) = 0.9 - (xx - xx)/xx = yy ^{t}CK(avg).

^{t}LZ(DQ),^{t}HZ(DQ),^{t}DQSCK,^{t}LZ(DQS),^{t}HZ(DQS)

These parameters are measured from a specific clock edge to a data signal transition (DM*n* or DQ*m*, where:*n*= 0,1; and*m*= 0–15, and specified timings must be met with respect to that clock edge. Therefore, they are not affected by ^{t}JIT(per).

^{t}QSH,^{t}QSL

These parameters are affected by duty cycle jitter, represented by ^{t}CH(abs)min and ^{t}CL(abs)min. These parameters determine the absolute data-valid window at the device pin. The absolute minimum data-valid window at the device pin = MIN {(^{t}QSH(abs)min - ^{t}DQSQmax), (^{t}QSL(abs)min - ^{t}DQSQmax)}. This minimum data valid window must be met at the target frequency regardless of clock jitter.

^{t}RPST

^{t}RPST is affected by duty cycle jitter, represented by ^{t}CL(abs). Therefore, ^{t}RPST(abs)min can be specified by ^{t}CL(abs)min. ^{t}RPST(abs)min = ^{t}CL(abs)min - 0.05 = ^{t}QSL(abs)min.

Clock Jitter Effects on WRITE Timing Parameters

^{t}DS,^{t}DH

These parameters are measured from a data signal (DMI*n* orDQ*m*, where *n*= 0, 1 and *m*= 0–15) transition edge to its respective data strobe signal (DQSn_t, DQSn_c: *n* = 0,1) crossing. The specification values are not affected by the amount of ^{t}JIT(per) applied, because the setup and hold times are relative to the data strobe signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

^{t}DSS,^{t}DSH

These parameters are measured from a data signal (DQS_t, DQSn_c) crossing to its respective clock signal (CK_t, CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT(per)act}$of the input clock in excess of the allowed period jitter $t_{JIT(per)allowed}$.

^{t}DQSS

^{t}DQSS is measured from a data strobe signal (DQSn_t, DQSn_c) crossing to its respective clock signal (CK_t, CK_c) crossing. When the device is operated with input clock jitter, this parameter must be derated by the actual ^{t}JIT(per),act of the input clock in excess of ^{t}JIT(per)allowed.

$$^{t}DQSS(min,derated) = 0.75 - \left(\frac{^{t}JIT(per),act,min - ^{t}JIT(per),allowed,\ min}{^{t}CK(avg)}\right)$$

$$^{t}DQSS(max,derated) = 1.25 - \left(\frac{^{t}JIT(per),act,max - ^{t}JIT(per),allowed,\ max}{^{t}CK(avg)}\right)$$

For example, if the measured jitter into an LPDDR4 device has ^{t}CK(avg) = 625ps, ^{t}JIT(per),act,min = -xxps, and ^{t}JIT(per),act,max = +xx ps, then:

^{t}DQSS,(min,derated) = 0.75 - (-xx + yy)/625 = xxxx ^{t}CK(avg)

^{t}DQSS,(max,derated) = 1.25 - (xx – yy)/625 = xxxx ^{t}CK(avg)

Revision History

Rev. G – 09/2023

- Updated legal status to Production

Rev. F – 06/2023

- Updated NAND endurance PROGRAM/ERASE cycles

Rev. E – 02/2023

- Corrected Part Number Diagram to change "-46" to "-046"

Rev. D – 01/2023

- Added Z null character back into the MPNs

Rev. C – 11/2022

- Corrected MPNs

Rev. B – 11/2022

- Moved to Preliminary Status
- Added NAND section for M71M.
- Added LPDRAM section for Z42N
- Correct the ball size and pad openings in the Package Dimensions figure.

Rev. A – 07/2022

- Initial Advanced release. Copied from NM112 Auto datasheet

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