

DDR4 SDRAM VLP EUDIMM Addendum

MTA9ADF2G72AZ – 16GB

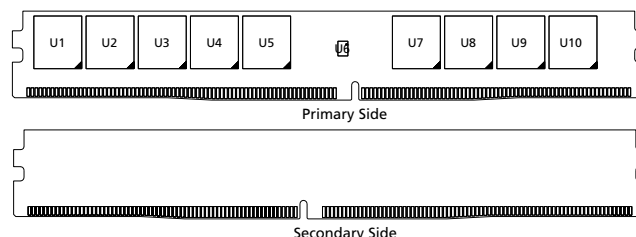
Features

Information provided here is in addition to or supercedes information provided in the Micron DDR4 UDIMM Core data sheet.

- DDR4 functionality and operations supported as defined in the component data sheet
- Features and specifications supported in the Micron DDR4 UDIMM core data sheet
- 288-pin, unbuffered very low profile ECC dual in-line memory module (VLP EUDIMM)
- Fast data transfer rate: PC4-3200
- 16GB (2 Gig x 72)
- Supports ECC error detection and correction
- Data bus inversion (DBI) for data bus
- Single-rank
- On-board I²C temperature sensor with integrated serial presence-detect (SPD) EEPROM

- 16 internal banks; 4 groups of 4 banks each

Figure 1: 288-Pin VLP EUDIMM



Options

- Operating temperature
 - Commercial (0°C ≤ T_{OPER} ≤ 95°C)
- Package
 - 288-pin DIMM (halogen-free)
- Frequency/CAS latency
 - 0.625ns @ CL = 22 (DDR4-3200)

Marking

None

Z

-3G2

Table 1: Addressing

Parameter	16GB
Row address	128K A[16:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	16Gb (2 Gig x 8), 16 banks
Module rank address	CS0_n

Table 2: Part Numbers and Timing Parameters – 16GB Modules

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/Data Rate	Clock Cycles (CL _n RCD _n RP)
MTA9ADF2G72AZ-3G2__	16GB	2 Gig x 72	25.6 GB/s	0.625ns/3200 MT/s	22-22-22

- Notes: 1. The data sheet for the base device can be found at micron.com.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA9ADF2G72AZ-3G2E1.
3. Base device: MT40A2G8,¹ 16Gb DDR4 SDRAM



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DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	3	157	U2	0	11	168
	1	1	150		1	9	161
	2	2	12		2	10	23
	3	0	5		3	8	16
	4	7	155		4	15	166
	5	5	148		5	13	159
	6	6	10		6	14	21
	7	4	3		7	12	14
U3	0	19	179	U4	0	27	190
	1	17	172		1	25	183
	2	18	34		2	26	45
	3	16	27		3	24	38
	4	23	177		4	31	188
	5	21	170		5	29	181
	6	22	32		6	30	43
	7	20	28		7	28	36
U5	0	CB3	201	U7	0	35	249
	1	CB1	194		1	33	242
	2	CB2	56		2	34	104
	3	CB0	49		3	32	97
	4	CB7	199		4	39	247
	5	CB5	192		5	37	240
	6	CB6	54		6	38	102
	7	CB4	47		7	36	95
U8	0	43	260	U9	0	51	271
	1	41	253		1	49	264
	2	42	115		2	50	126
	3	40	108		3	48	119
	4	47	258		4	55	269
	5	45	251		5	53	262
	6	46	113		6	54	124
	7	44	106		7	52	117



Table 3: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U10	0	59	282				
	1	57	275				
	2	58	137				
	3	56	130				
	4	63	280				
	5	61	273				
	6	62	135				
	7	60	128				



I_{DD} Specifications

Table 4: DDR4 I_{DD} Specifications and Conditions – 16GB (Die Revision F)

Parameter	Symbol	3200	Units
One bank ACTIVATE-PRECHARGE current	I _{DD0}	540	mA
One bank ACTIVATE-PRECHARGE, word line boost, I _{pp} current	I _{PP0}	27	mA
One bank ACTIVATE-READ-PRECHARGE current	I _{DD1}	639	mA
Precharge standby current	I _{DD2N}	405	mA
Precharge standby ODT current	I _{DD2NT}	459	mA
Precharge power-down current	I _{DD2P}	342	mA
Precharge quiet standby current	I _{DD2Q}	378	mA
Active standby current	I _{DD3N}	549	mA
Active standby I _{pp} current	I _{PP3N}	18	mA
Active power-down current	I _{DD3P}	450	mA
Burst read current	I _{DD4R}	1260	mA
Burst write current	I _{DD4W}	1008	mA
Burst refresh current (1x REF)	I _{DD5R}	612	mA
Burst refresh I _{pp} current (1x REF)	I _{PP5R}	36	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I _{DD6N}	477	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I _{DD6E}	810	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I _{DD6R}	180	mA
Auto self refresh current (25°C)	I _{DD6A}	99	mA
Auto self refresh current (45°C)	I _{DD6A}	180	mA
Auto self refresh current (75°C)	I _{DD6A}	459	mA
Auto self refresh current (95°C)	I _{DD6A}	810	mA
Auto self refresh I _{pp} current	I _{PP6X}	54	mA
Bank interleave read current	I _{DD7}	1503	mA
Bank interleave read I _{pp} current	I _{PP7}	72	mA
Maximum power-down current	I _{DD8}	324	mA

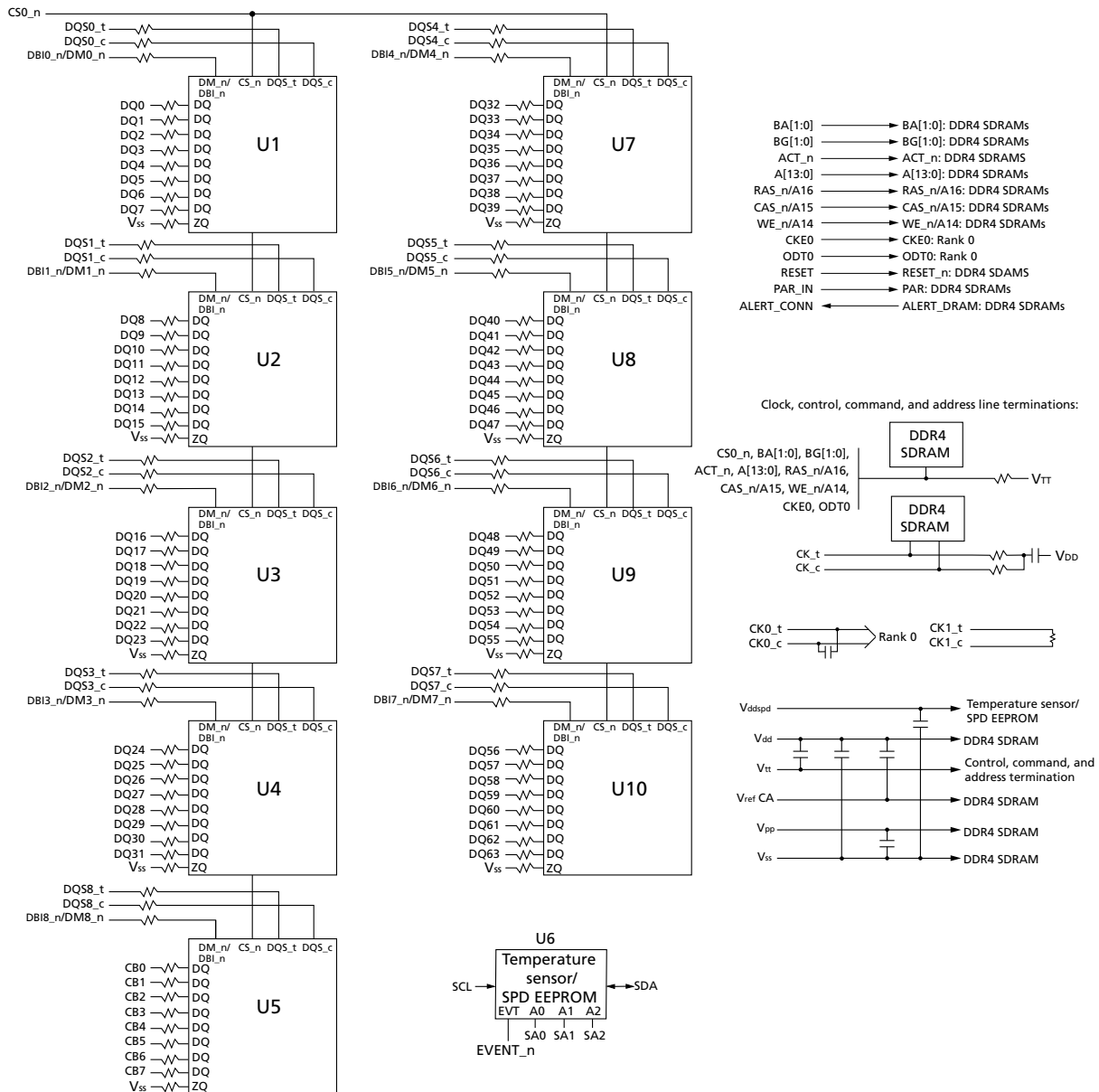
Notes: 1. Values are for the MT40A2G8 DDR4 SDRAM only and are computed from values specified in the 16Gb (2 Gig x 8) component data sheet



16GB (x72, ECC, SR) 288-Pin DDR4 VLP EUDIMM Functional Block Diagram

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external $240\Omega \pm 1\%$ resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.