

DDR5 SDRAM UDIMM Addendum

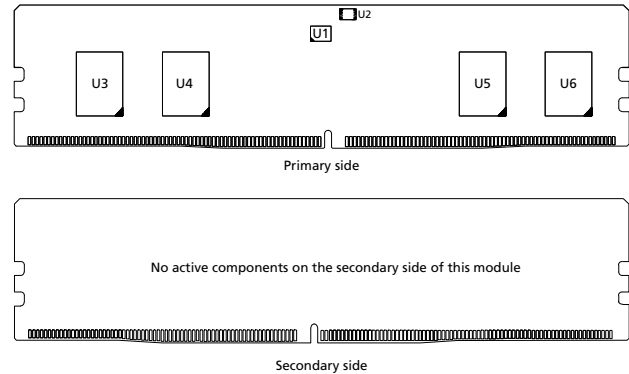
MTC4C10163S1UC – 8GB 16Gb Die Revision A

Features

Information provided here is in addition to or supersedes information provided in the Micron DDR5 UDIMM Core data sheet.

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR5 UDIMM core data sheet
- 288-pin, DDR5 unbuffered dual in-line memory module (DDR5 UDIMM)
- Fast data transfer rate: PC5-4800, PC5-5600
- 8GB (1Gig x 64)
- Single-rank
- 16 internal banks; 4 groups of 4 banks each

Figure 1: 288-Pin DDR5 UDIMM (R/C-C0)



Options

- Operating temperature
 - Commercial ($0^{\circ}\text{C} \leq T_{\text{OPER}} \leq 95^{\circ}\text{C}$)
- Frequency/CAS latency
 - 0.416ns @ CL = 40 (DDR5-4800)
 - 0.357ns @ CL = 46 (DDR5-5600)

Marking

C
48B
56B

Table 1: Addressing

Parameter	8GB
Row address ¹	64K (R0-R15)
Column address ¹	1K (C0-C9)
Device bank group address ¹	4 (BG0-BG1)
Device bank address per bank group ¹	4 (BA0-BA1)
Device configuration	16Gb (1Gb x 16), 16 banks
Module rank address	1 (CS0_n)

Notes: 1. These parameters represent the logical address state of the CA bus for different commands. Refer to the command truth table in the component data sheet.



Table 2: Part Numbers and Timing Parameters – 8GB Modules

Base device: MT60B1G16,¹ 16Gb DDR5 SDRAM Die Revision A

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-nRCD-nRP)
MTC4C10163S1UC48BA1	8GB	1Gb x 64	38.4 GB/s	0.416ns/4800 MT/s	40-39-39
MTC4C10163S1UC56BA1	8GB	1Gb x 64	44.8 GB/s	0.357ns/5600 MT/s	46-45-45

Notes: 1. The data sheet for the base device can be found on micron.com.

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DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U3	0	14A	171	U4	0	30A	192
	1	13A	28		1	29A	49
	2	15A	173		2	31A	194
	3	12A	26		3	28A	47
	4	11A	166		4	27A	187
	5	9A	22		5	24A	41
	6	10A	164		6	26A	185
	7	8A	20		7	25A	43
	8	7A	162		8	23A	183
	9	4A	16		9	20A	37
	10	6A	160		10	22A	181
	11	5A	18		11	21A	39
	12	3A	156		12	19A	177
	13	1A	11		13	16A	30
	14	0A	9		14	18A	175
15	2A	154	15	17A	32		
U5	0	7B	254	U6	0	23B	275
	1	4B	108		1	22B	273
	2	6B	252		2	20B	129
	3	5B	110		3	21B	131
	4	3B	248		4	17B	124
	5	0B	101		5	19B	269
	6	1B	103		6	18B	267
	7	2B	246		7	16B	122
	8	10B	256		8	26B	277
	9	9B	114		9	24B	133
	10	8B	112		10	27B	279
	11	11B	258		11	25B	135
	12	15B	265		12	30B	284
	13	12B	118		13	29B	141
	14	14B	263		14	28B	139
15	13B	120	15	31B	286		



I_{DD} Specifications

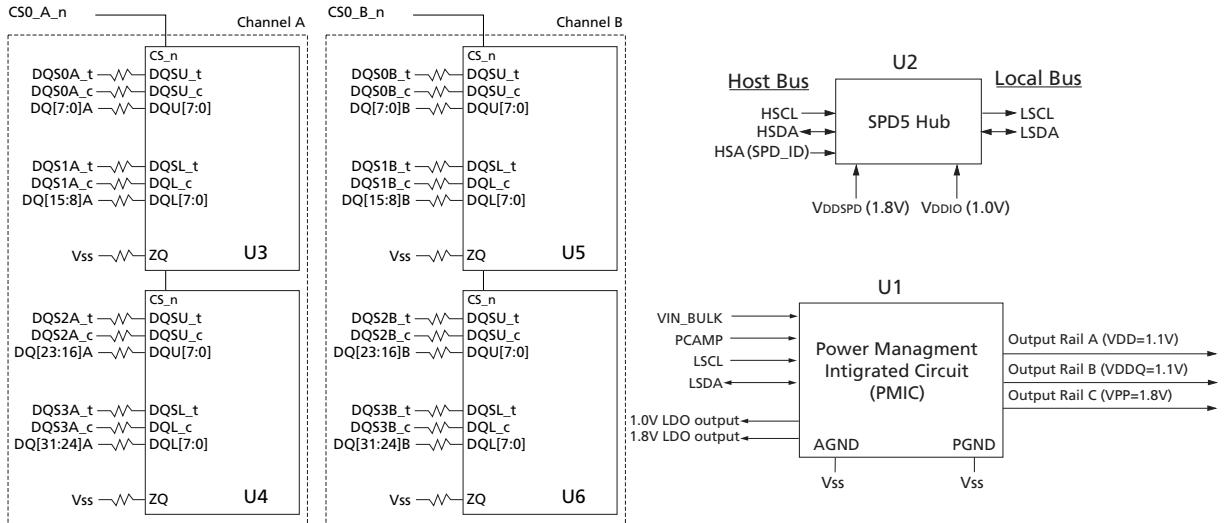
Table 4: DDR5 I_{DD} Specifications and Conditions – 16GB (Die Revision A)

Module I_{DD} is based on PMIC VIN_BULK 5V input current and typical operating range of temperature. Each I_{DD} parameter includes PMIC efficiency and all DRAM current on all supplies (V_{DD}, V_{DDQ}, and V_{PP}).

Parameter	Symbol	4800	5600	Units
Operating one bank ACTIVATE-PRECHARGE current	I _{DD0}	98	TBD	mA
Operating four bank ACTIVATE-PRECHARGE current	I _{DD0F}	172	TBD	mA
Precharge standby current	I _{DD2N}	74	TBD	mA
Precharge standby non-target command	I _{DD2NT}	166	TBD	mA
Precharge power-down current	I _{DD2P}	65	TBD	mA
Active standby current	I _{DD3N}	81	TBD	mA
Active power-down current	I _{DD3P}	75	TBD	mA
Operating burst read current	I _{DD4R}	537	TBD	mA
Operating burst write current	I _{DD4W}	778	TBD	mA
Operating burst write with write CRC current	I _{DD4WC}	695	TBD	mA
Burst refresh (normal refresh mode) current	I _{DD5B}	248	TBD	mA
Burst refresh (fine granularity refresh mode) current	I _{DD5F}	160	TBD	mA
Burst refresh (same bank refresh mode) current	I _{DD5C}	113	TBD	mA
Self refresh current	I _{DD6N}	31	TBD	mA
Operating bank interleave read current	I _{DD7}	634	TBD	mA
Maximum power saving deep power down mode current	I _{DD8}	23	TBD	mA

Functional Block Diagram

Figure 2: Functional Block Diagram



- Notes:
1. The ZQ ball on each DDR5 component is connected to an external $240\Omega \pm 1\%$ resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
 2. Functional block diagram is for reference only.



Revision History

Rev. F – 10/2021

- Add 5600 speed, IDD's are TBD
- Remove Micron Confidential marking

Rev. E – 08/2021

- Production Release

Rev. D – 02/2021

- Preliminary Release

Rev. C – 01/2021

- Preliminary Release

Rev. B – 06/2020

- Preliminary Release

Rev. A – 06/2020

- Preliminary Release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.