# DDR5 SDRAM UDIMM Addendum

MTC8C1084S1UC – 16GB
16Gb Die Revision A

Features

Information provided here is in addition to or super-sedes information provided in the Micron DDR5 UDIMM Core data sheet.

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR5 UDIMM core data sheet
- 288-pin, DDR5 unbuffered dual in-line memory module (DDR5 UDIMM)
- Fast data transfer rate: PC5-4800, PC5-5600
- 16GB (2Gig x 64)
- Single-rank
- 32 internal banks; 8 groups of 4 banks each

Figure 1: 288-Pin DDR5 UDIMM (R/C-B0)

Primary side

No components on the secondary side of this module

Secondary Side
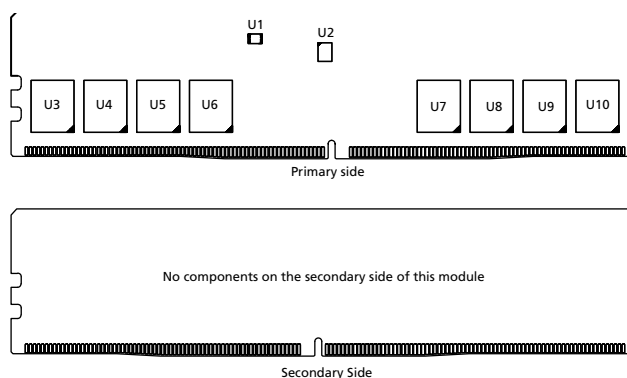
Options   Marking

- Operating temperature
  – Commercial (0°C ≤ T_{OPER} ≤ 95°C)   C
- Frequency/CAS latency
  – 0.416ns @ CL = 40 (DDR5-4800)   48B
  – 0.357ns @ CL = 46 (DDR5-5600)   56B

Table 1: Addressing

Parameter	16GB
Row address[1]	64K (R0-R15)
Column address[1]	1K (C0-C9)
Device bank group address[1]	8 (BG0-BG2)
Device bank address per bank group[1]	4 (BA0-BA1)
Device configuration	16Gb (2Gb x 8), 32 banks
Module rank address	1 (CS0_n)

Notes: 1. These parameters represent the logical address state of the CA bus for different commands. Refer to the command truth table in the component data sheet.

Table 2: Part Numbers and Timing Parameters – 16GB Modules

Base device: MT60B2G8,[1] 16Gb DDR5 SDRAM Die Revision A

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-$_n$RCD-$_n$RP)
MTC8C1084S1UC48BA1	16GB	2Gb x 64	38.4 GB/s	0.416ns/4800 MT/s	40-39-39
MTC8C1084S1UC56BA1	16GB	2Gb x 64	44.8 GB/s	0.357ns/5600 MT/s	46-45-45

Notes: 1. The data sheet for the base device can be found on micron.com.

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DQ Map

Table 3: Component-to-Module DQ Map

| Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U3	0	3A	156	U4	0	11A	166
	1	0A	9		1	8A	20
	2	1A	11		2	9A	22
	3	2A	154		3	10A	164
	4	7A	162		4	15A	173
	5	4A	16		5	12A	26
	6	5A	18		6	13A	28
	7	6A	160		7	14A	171
U5	0	19A	177	U6	0	27A	187
	1	16A	30		1	24A	41
	2	17A	32		2	25A	43
	3	18A	175		3	26A	185
	4	23A	183		4	31A	194
	5	20A	37		5	28A	47
	6	21A	39		6	29A	49
	7	22A	181		7	30A	192
U7	0	3B	248	U8	0	11B	258
	1	0B	101		1	8B	112
	2	1B	103		2	9B	114
	3	2B	246		3	10B	256
	4	7B	254		4	15B	265
	5	4B	108		5	12B	118
	6	5B	110		6	13B	120
	7	6B	252		7	14B	263
U9	0	19B	269	U10	0	27B	279
	1	16B	122		1	24B	133
	2	17B	124		2	25B	135
	3	18B	267		3	26B	277
	4	23B	275		4	31B	286
	5	20B	129		5	28B	139
	6	21B	131		6	29B	141
	7	22B	273		7	30B	284

I_{DD} Specifications

Table 4: DDR5 I_{DD} Specifications and Conditions – 16GB (Die Revision A)

Module I_{DD} is based on PMIC VIN_BULK 5V input current and typical operating range of temperature. Each I_{DD} parameter includes PMIC efficiency and all DRAM current on all supplies (V_{DD}, V_{DDQ}, and V_{PP}).

Parameter	Symbol	4800	5600	Units
Operating one bank ACTIVATE-PRECHARGE current	I_{DD0}	139	TBD	mA
Operating four bank ACTIVATE-PRECHARGE current	I_{DD0F}	220	TBD	mA
Precharge standby current	I_{DD2N}	109	TBD	mA
Precharge standby non-target command	I_{DD2NT}	244	TBD	mA
Precharge power-down current	I_{DD2P}	93	TBD	mA
Active standby current	I_{DD3N}	124	TBD	mA
Active power-down current	I_{DD3P}	110	TBD	mA
Operating burst read current	I_{DD4R}	652	TBD	mA
Operating burst write current	I_{DD4W}	890	TBD	mA
Operating burst write with write CRC current	I_{DD4WC}	803	TBD	mA
Burst refresh (normal refresh mode) current	I_{DD5B}	451	TBD	mA
Burst refresh (fine granularity refresh mode) current	I_{DD5F}	274	TBD	mA
Burst refresh (same bank refresh mode) current	I_{DD5C}	190	TBD	mA
Self refresh current	I_{DD6N}	60	TBD	mA
Operating bank interleave read current	I_{DD7}	722	TBD	mA
Maximum power saving deep power down mode current	I_{DD8}	43	TBD	mA

Functional Block Diagram

Figure 2: Functional Block Diagram
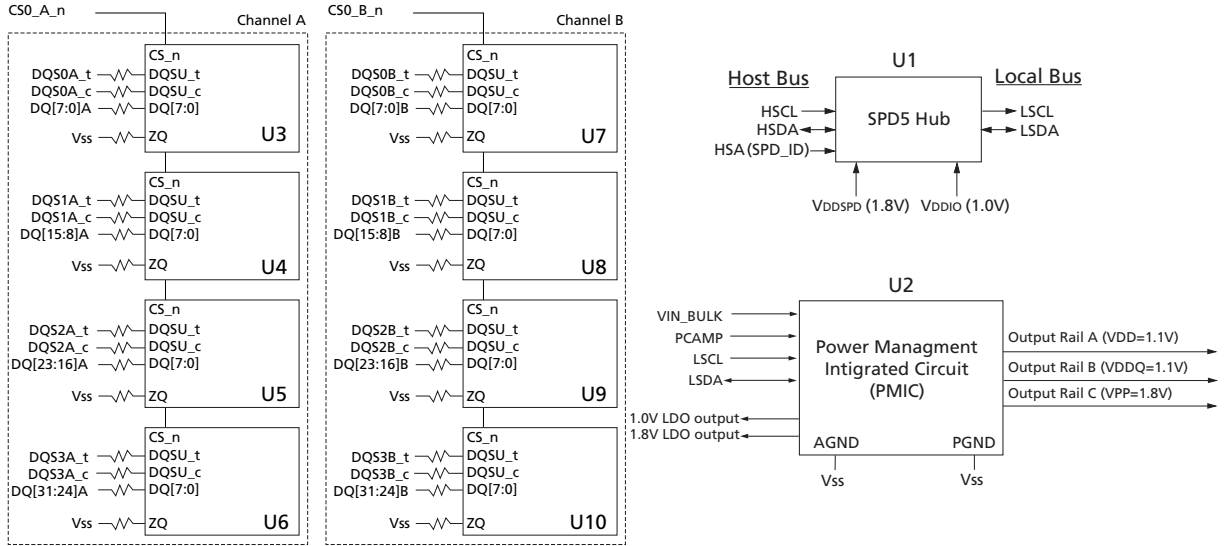
Notes: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
  2. Functional block diagram is for reference only.

Revision History

Rev. F – 10/2021

- Add 5600 speed, IDDs are TBD
- Remove Micron Confidential marking

Rev. E – 08/2021

- Production Release

Rev. D – 02/2021

- Preliminary Release

Rev. C – 01/2021

- Preliminary Release

Rev. B – 06/2020

- Preliminary Release

Rev. A – 06/2020

- Preliminary Release

This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.