

DDR4 SDRAM UDIMM

Addendum

MTA8ATF2G64AZ – 16GB

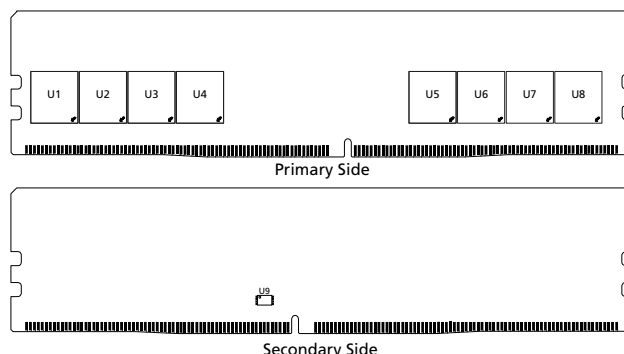
Introduction

Information provided here is in addition to or supercedes information provided in the Micron DDR4 UDIMM Core data sheet.

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- Features and specifications supported in the Micron DDR4 UDIMM core data sheet
- 288-pin, unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rate: PC4-2666, PC4-3200
- 16GB (2 Gig x 64)
- Data bus inversion (DBI) for data bus
- Single-rank
- On-board I² serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each

Figure 1: 288-Pin UDIMM (R/C A2)



Options

- Operating temperature
 - Commercial (0°C ≤ T_{OPER} ≤ 95°C)
- Package
 - 288-pin DIMM (halogen-free)
- Frequency/CAS latency
 - 0.625ns @ CL = 22 (DDR4-3200)
 - 0.75ns @ CL = 19 (DDR4-2666)

Marking

None
Z
-3G2
-2G6

Table 1: Addressing

Parameter	16GB
Row address	128K A[16:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	16Gb (2 Gig x 8), 16 banks
Module rank address	CS0_n

Table 2: Part Numbers and Timing Parameters – 16GB Modules

Base device: MT40A2G8,¹ 16Gb DDR4 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL _n RCD _n RP)
MTA8ATF2G64AZ-3G2__	16GB	2 Gig x 64	25.6 GB/s	0.625ns/3200 MT/s	22-22-22
MTA8ATF2G64AZ-2G6__	16GB	2 Gig x 64	21.3 GB/s	0.75ns/2666 MT/s	19-19-19

- Notes:
1. The data sheet for the base device can be found on micron.com.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA8ATF2G64AZ-3G2B1.

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DQ Map

Table 3: Component-to-Module DQ Map (R/C-A2)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	3	157	U2	0	11	168
	1	1	150		1	9	161
	2	2	12		2	10	23
	3	0	5		3	8	16
	4	7	155		4	15	166
	5	5	148		5	13	159
	6	6	10		6	14	21
	7	4	3		7	12	14
U3	0	19	179	U4	0	27	190
	1	17	172		1	25	183
	2	18	34		2	26	45
	3	16	27		3	24	38
	4	23	177		4	31	188
	5	21	170		5	29	181
	6	22	32		6	30	43
	7	20	25		7	28	36
U5	0	35	249	U6	0	43	260
	1	33	242		1	41	253
	2	34	104		2	42	115
	3	32	97		3	40	108
	4	39	247		4	47	258
	5	37	240		5	45	251
	6	38	102		6	46	113
	7	36	95		7	44	106
U7	0	51	271	U8	0	59	282
	1	49	264		1	57	275
	2	50	126		2	58	137
	3	48	119		3	56	130
	4	55	269		4	63	280
	5	53	262		5	61	273
	6	54	124		6	62	135
	7	52	117		7	60	128

I_{DD} Specifications

Table 4: DDR4 I_{DD} Specifications and Conditions (0° ≤ T_C ≤ 85°) – 16GB (Die Revision E)

Values are for the MT40A2G8 DDR4 SDRAM only and are computed from values specified in the 16Gb (2 Gig x 8) component data sheet

Parameter	Symbol	3200	2666	Units
One bank ACTIVATE-PRECHARGE current	I _{DD0}	480	464	mA
One bank ACTIVATE-PRECHARGE, Word Line Boost, I _{pp} current	I _{PP0}	24	24	mA
One bank ACTIVATE-READ-PRECHARGE current	I _{DD1}	568	552	mA
Precharge standby current	I _{DD2N}	360	344	mA
Precharge standby ODT current	I _{DD2NT}	408	392	mA
Precharge power-down current	I _{DD2P}	304	304	mA
Precharge quiet standby current	I _{DD2Q}	336	336	mA
Active standby current	I _{DD3N}	488	472	mA
Active standby I _{pp} current	I _{PP3N}	16	16	mA
Active power-down current	I _{DD3P}	400	384	mA
Burst read current	I _{DD4R}	1296	1168	mA
Burst write current	I _{DD4W}	1024	936	mA
Burst refresh current (1x REF)	I _{DD5R}	544	544	mA
Burst refresh I _{pp} current (1x REF)	I _{PP5R}	32	32	mA
Self refresh current: Normal temperature range (0°C to +85°C)	I _{DD6N}	424	424	mA
Self refresh current: Extended temperature range (0°C to +95°C)	I _{DD6E}	904	904	mA
Self refresh current: Reduced temperature range (0°C to +45°C)	I _{DD6R}	160	160	mA
Auto self refresh current (25°C)	I _{DD6A}	88	88	mA
Auto self refresh current (45°C)	I _{DD6A}	160	160	mA
Auto self refresh current (75°C)	I _{DD6A}	408	408	mA
Auto self refresh current (95°C)	I _{DD6A}	904	904	mA
Auto self refresh I _{pp} current	I _{PP6X}	48	48	mA
Bank interleaved read current	I _{DD7}	1480	1448	mA
Bank interleaved read I _{pp} current	I _{PP7}	64	64	mA
Maximum power-down current	I _{DD8}	288	288	mA

Note: 1. When T_C > 85°C, the I_{DD} and I_{pp} values must be derated. Refer to the base device data sheet I_{DD} and I_{pp} specification tables for derating values for the applicable die-revision.

Table 5: DDR4 I_{DD} Specifications and Conditions (0° ≤ T_C ≤ 85°) – 16GB (Die Revision B)

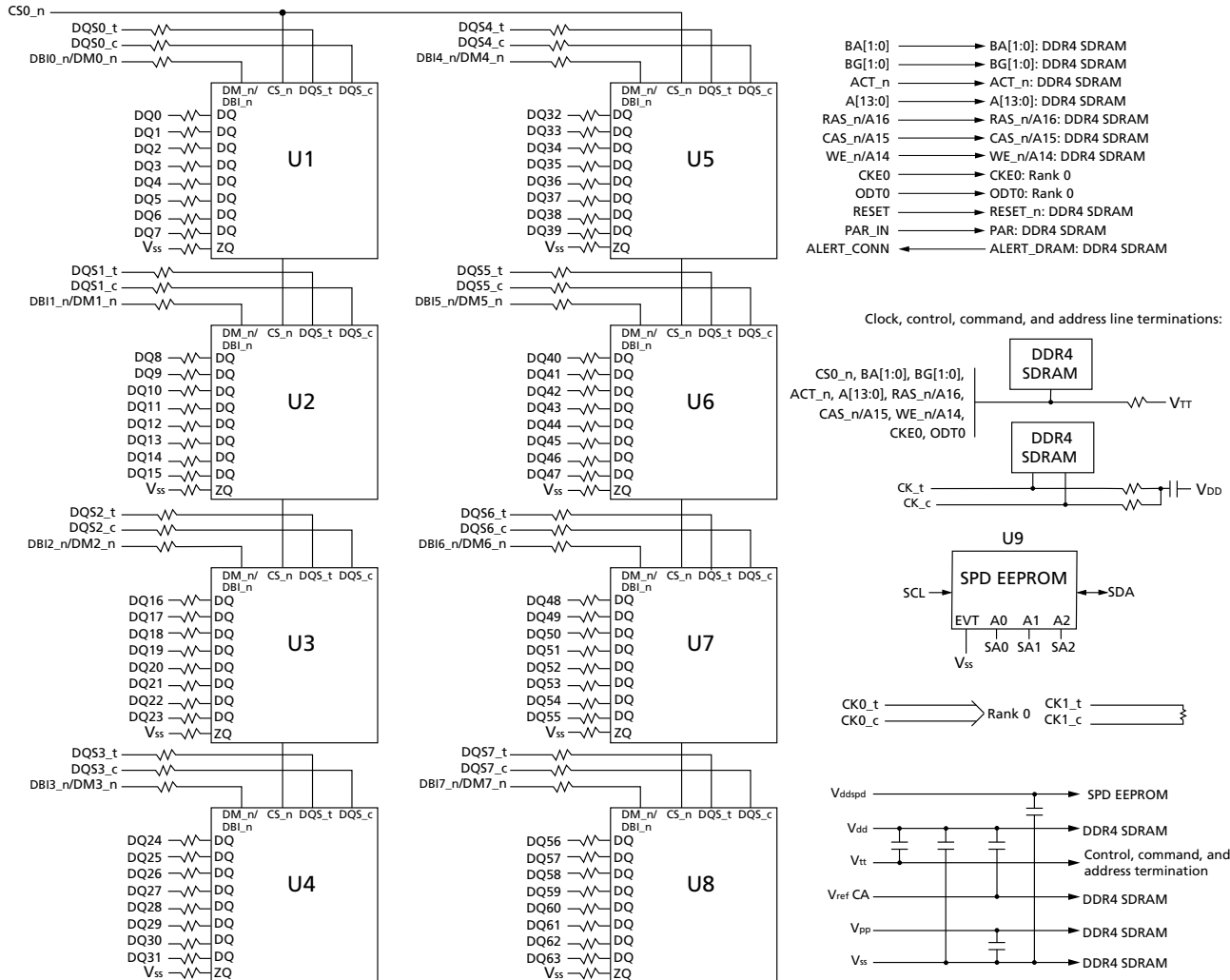
Values are for the MT40A2G8 DDR4 SDRAM only and are computed from values specified in the 16Gb (2 Gig x 8) component data sheet

Parameter	Symbol	3200	2666	Units
One bank ACTIVATE-PRECHARGE current	I _{DD0}	504	488	mA
One bank ACTIVATE-PRECHARGE, Word Line Boost, I _{PP} current	I _{PP0}	32	32	mA
One bank ACTIVATE-READ-PRECHARGE current	I _{DD1}	592	576	mA
Precharge standby current	I _{DD2N}	416	400	mA
Precharge standby ODT current	I _{DD2NT}	448	432	mA
Precharge power-down current	I _{DD2P}	344	344	mA
Precharge quiet standby current	I _{DD2Q}	376	376	mA
Active standby current	I _{DD3N}	640	624	mA
Active standby I _{PP} current	I _{PP3N}	24	24	mA
Active power-down current	I _{DD3P}	552	544	mA
Burst read current	I _{DD4R}	1616	1456	mA
Burst write current	I _{DD4W}	1464	1328	mA
Burst refresh current (1x REF)	I _{DD5R}	632	616	mA
Burst refresh I _{PP} current (1x REF)	I _{PP5R}	40	40	mA
Self refresh current: Normal temperature range (0°C to +85°C)	I _{DD6N}	536	536	mA
Self refresh current: Extended temperature range (0°C to +95°C)	I _{DD6E}	968	968	mA
Self refresh current: Reduced temperature range (0°C to +45°C)	I _{DD6R}	232	232	mA
Auto self refresh current (25°C)	I _{DD6A}	80	80	mA
Auto self refresh current (45°C)	I _{DD6A}	232	232	mA
Auto self refresh current (75°C)	I _{DD6A}	488	488	mA
Auto self refresh current (95°C)	I _{DD6A}	968	968	mA
Auto self refresh I _{PP} current	I _{PP6X}	88	88	mA
Bank interleave read current	I _{DD7}	1568	1520	mA
Bank interleave read I _{PP} current	I _{PP7}	80	80	mA
Maximum power-down current	I _{DD8}	320	320	mA

Note: 1. When T_C > 85°C, the I_{DD} and I_{PP} values must be derated. Refer to the base device data sheet I_{DD} and I_{PP} specification tables for derating values for the applicable die-revision.

Functional Block Diagram

Figure 2: Functional Block Diagram (R/C-A2)



Note: 1. The ZQ ball on each DDR4 component is connected to an external $240\Omega \pm 1\%$ resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

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