Automotive Asynchronous/Synchronous NAND Flash Memory

MT29F16G08ABABAWP-AIT:B, MT29F16G08ABCBBH1-12AIT:B

Features

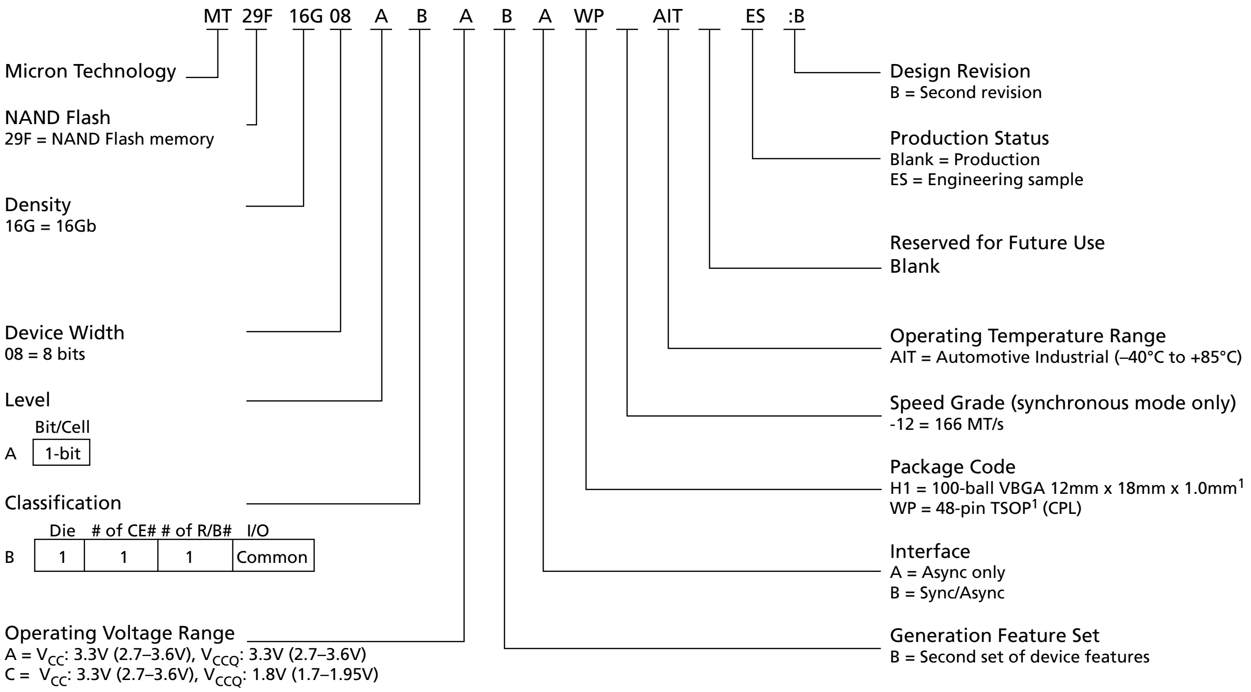
- Open NAND Flash Interface (ONFI) 2.1-compliant[1]
- Single-level cell (SLC) technology
- Organization
  - Page size x8: 4320 bytes (4096 + 224 bytes)
  - Block size: 128 pages (512K +28K bytes)
  - Plane size: 2 planes x 2048 blocks per plane
  - Device size: 16Gb: 4096 blocks;
    32Gb: 8192 blocks;
    64Gb: 16,384 blocks;
    128Gb: 32,768 blocks
- Synchronous I/O performance
  - Up to synchronous timing mode 4
  - Clock rate: 12ns (DDR)
  - Read/write throughput per pin: 166 MT/s
- Asynchronous I/O performance
  - Up to asynchronous timing mode 4
  - ^{t}RC/^{t}WC: 25ns (MIN)
- Array performance
  - Read page: 25µs (MAX)
  - Program page: 230µs (TYP)
  - Erase block: 700µs (TYP)
- Operating Voltage Range
  - V_{CC}: 2.7–3.6V
  - V_{CCQ}: 1.7–1.95V, 2.7–3.6V
- Command set: ONFI NAND Flash Protocol
- Advanced Command Set
  - Program cache
  - Read cache sequential
  - Read cache random
  - One-time programmable (OTP) mode
  - Multi-plane commands
  - Multi-LUN operations
  - Read unique ID
  - Copyback
- First block (block address 00h) is valid when shipped from factory. For minimum required ECC, see Error Management (page 115).
- RESET (FFh) required as first command after power-on
- Operation status byte provides software method for detecting
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Data strobe (DQS) signals provide a hardware method for synchronizing data DQ in the synchronous interface
- Copyback operations supported within the plane from which data is read
- Quality and reliability
  - Data retention: 10 years
  - Endurance: 100,000 PROGRAM/ERASE cycles
- Operating temperature:
  - Automotive Industrial (AIT): –40°C to +85°C
- Package
  - 52-pad LGA
  - 48-pin TSOP
  - 100-ball BGA

Note: 1. The ONFI 2.1 specification is available at www.onfi.org.

Part Numbering Information

Micron NAND Flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Numbering



Note: 1. Pb-free package.

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General Description

Micron NAND Flash devices include an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (DQx) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection (WP#) and monitor device status (R/B#).

This Micron NAND Flash device additionally includes a synchronous data interface for high-performance I/O operations. When the synchronous interface is active, WE# becomes CLK and RE# becomes W/R#. Data transfers include a bidirectional data strobe (DQS).

This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign.

A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). For further details, see Device and Array Organization.

Asynchronous and Synchronous Signal Descriptions

Table 1: Asynchronous and Synchronous Signal Definitions

Asynchronous Signal[1]	Synchronous Signal[1]	Type	Description[2]
ALE	ALE	Input	**Address latch enable:** Loads an address from DQx into the address register.
CE#	CE#	Input	**Chip enable:** Enables or disables one or more die (LUNs) in a target[1].
CLE	CLE	Input	**Command latch enable:** Loads a command from DQx into the command register.
DQx	DQx	I/O	**Data inputs/outputs:** The bidirectional I/Os transfer address, data, and command information.
–	DQS	I/O	**Data strobe:** Provides a synchronous reference for data input and output.
RE#	W/R#	Input	**Read enable and write/read:** RE# transfers serial data from the NAND Flash to the host system when the asynchronous interface is active. When the synchronous interface is active, W/R# controls the direction of DQx and DQS.
WE#	CLK	Input	**Write enable and clock:** WE# transfers commands, addresses, and serial data from the host system to the NAND Flash when the asynchronous interface is active. When the synchronous interface is active, CLK latches command and address cycles.
WP#	WP#	Input	**Write protect:** Enables or disables array PROGRAM and ERASE operations.
R/B#	R/B#	Output	**Ready/busy:** An open-drain, active-low output that requires an external pull-up resistor. This signal indicates target array activity.

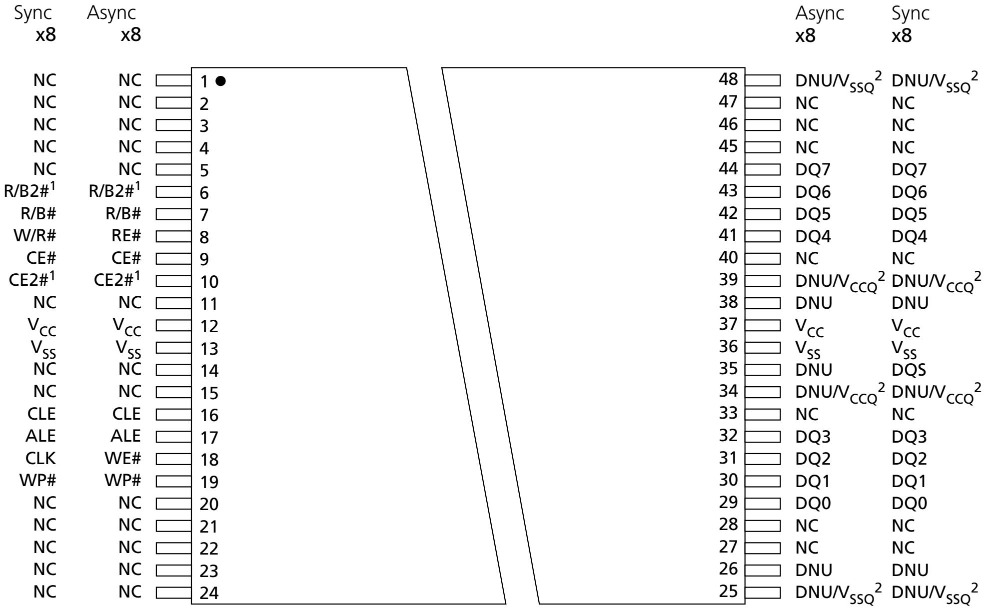
Table 1: Asynchronous and Synchronous Signal Definitions (Continued)

Asynchronous Signal[1]	Synchronous Signal[1]	Type	Description[2]
V_{CC}	V_{CC}	Supply	**V_{CC}:** Core power supply
V_{CCQ}	V_{CCQ}	Supply	**V_{CCQ}:** I/O power supply
V_{SS}	V_{SS}	Supply	**V_{SS}:** Core ground connection
V_{SSQ}	V_{SSQ}	Supply	**V_{SSQ}:** I/O ground connection
NC	NC	–	**No connect:** NCs are not internally connected. They can be driven or left unconnected.
DNU	DNU	–	**Do not use:** DNUs must be left unconnected.
RFU	RFU	–	**Reserved for future use:** RFUs must be left unconnected.

Notes:
1. See Device and Array Organization for detailed signal connections.
2. See Bus Operation – Asynchronous Interface (page 30) and Bus Operation – Synchronous Interface (page 40) for detailed asynchronous and synchronous interface signal descriptions.

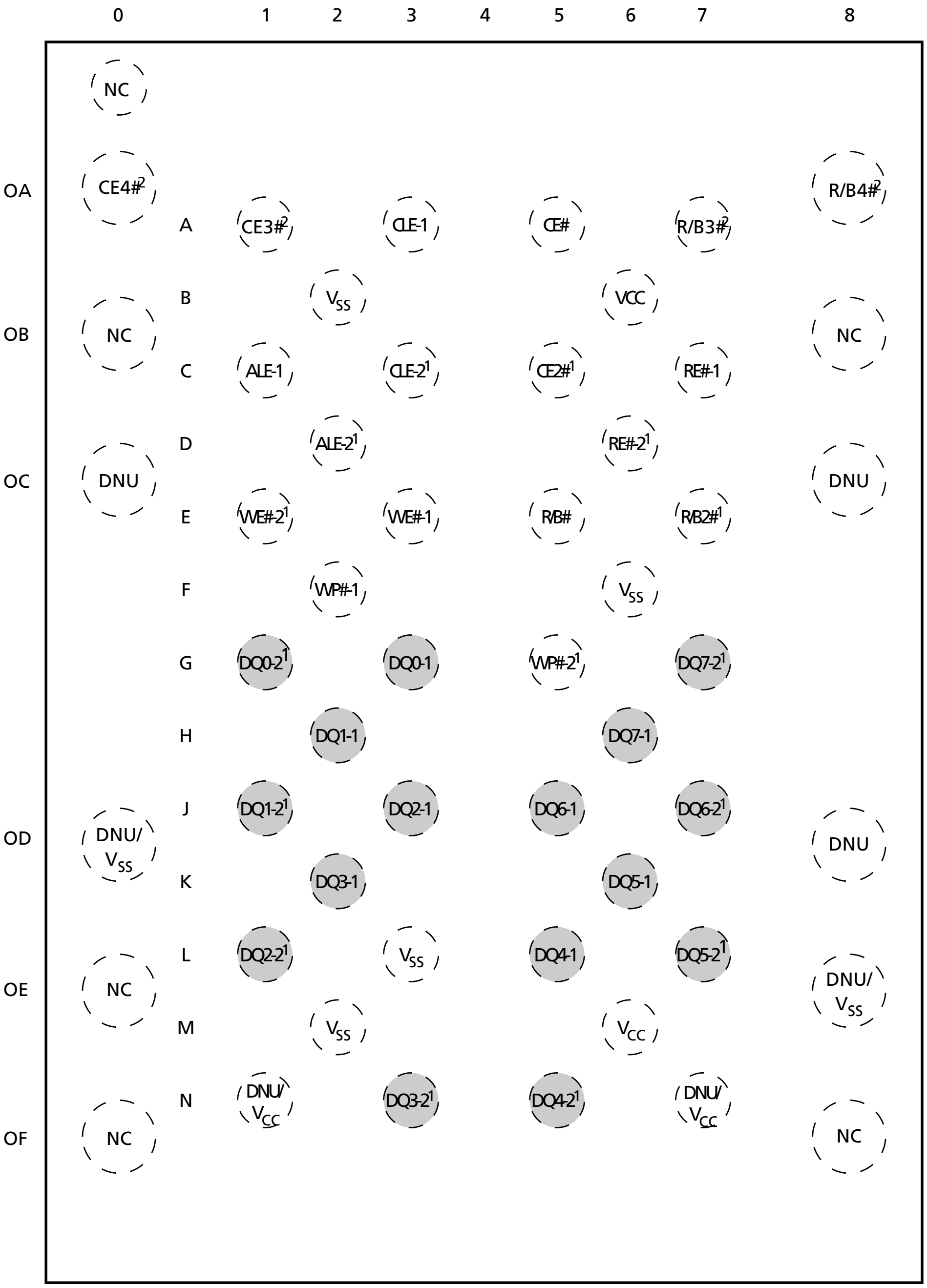
Signal Assignments

Figure 2: 48-Pin TSOP Type 1 (Top View)



Notes:
1. CE2# and R/B2# are available on dual die and quad die packages. They are NC for other configurations.
2. These V_{CCQ} and V_{SSQ} pins are for compatibility with ONFI 2.1. If not supplying V_{CCQ} or V_{SSQ} to these pins, do not use them.
3. TSOP devices do not support the synchronous interface.

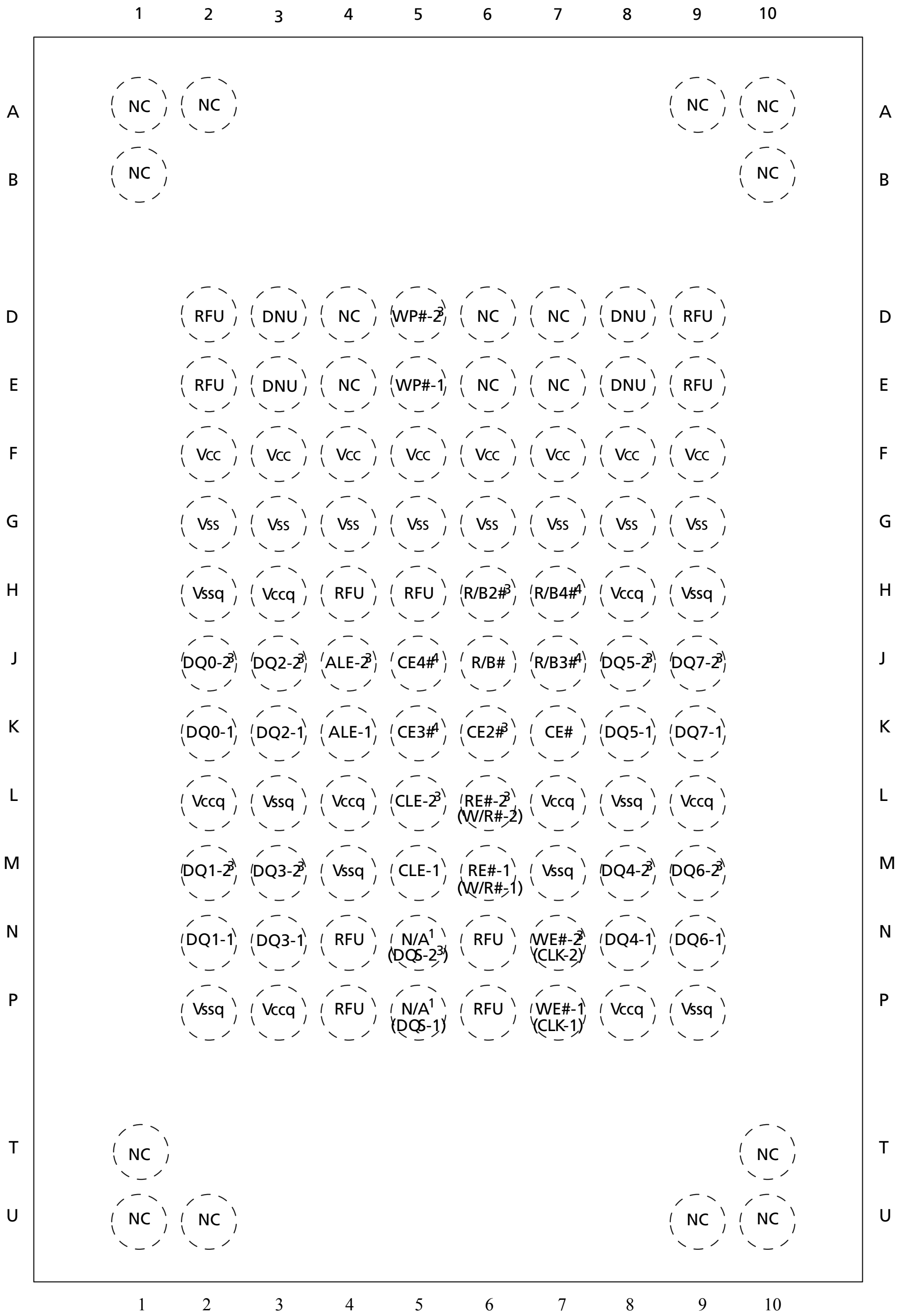
Figure 3: 52-Pad LGA (Top View)



Top View, Pads Down

Notes:
1. These signals are available on quad and octal die packages. They are NC for other configurations.
2. These signals are available on quad die four CE# or octal die packages. They are NC for other configurations.

Figure 4: 100-Ball BGA (Ball-Down, Top View)



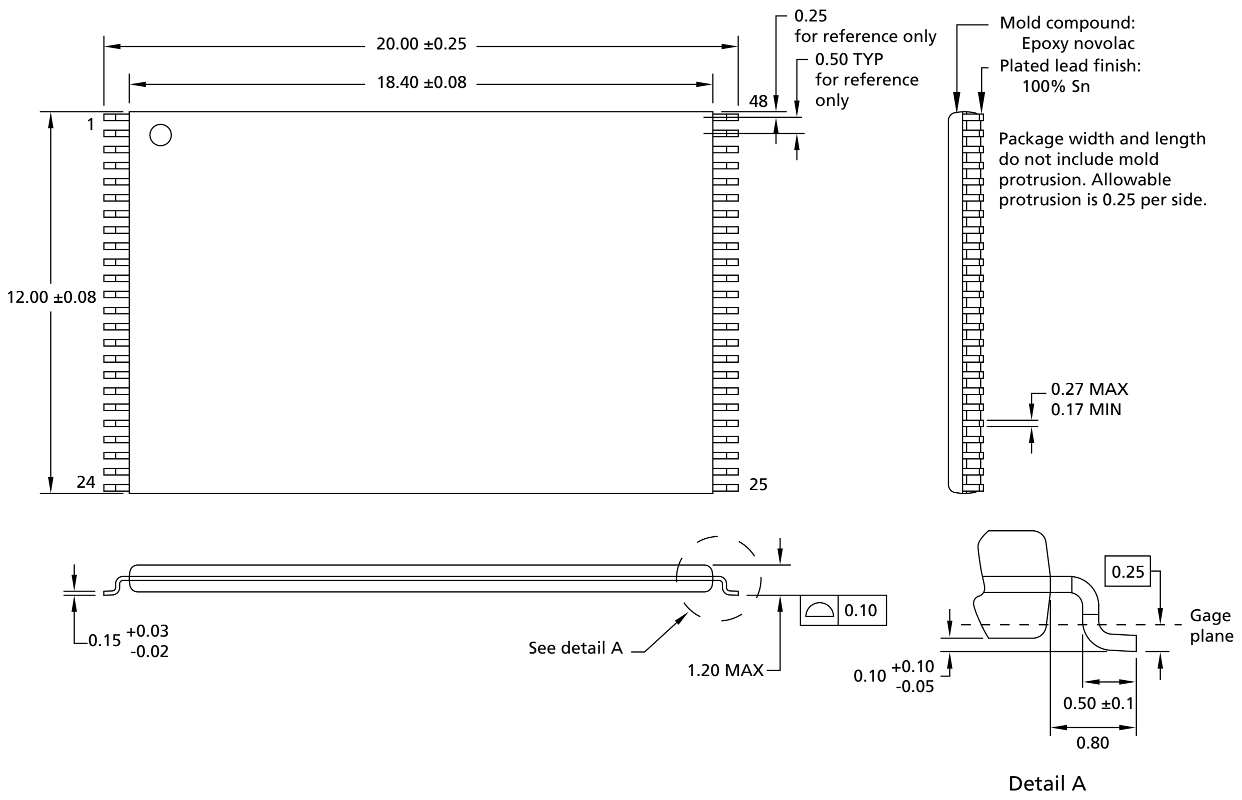
	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC									NC
D		RFU	DNU	NC	WP#-2[3]	NC	NC	DNU	RFU	
E		RFU	DNU	NC	WP#-1	NC	NC	DNU	RFU	
F		Vcc	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc	
G		Vss	Vss	Vss	Vss	Vss	Vss	Vss	Vss	
H		Vssq	Vccq	RFU	RFU	R/B2#[3]	R/B4#[4]	Vccq	Vssq	
J		DQ0-2[3]	DQ2-2[3]	ALE-2[3]	CE4#[4]	R/B#	R/B3#[4]	DQ5-2[3]	DQ7-2[3]	
K		DQ0-1	DQ2-1	ALE-1	CE3#[4]	CE2#[3]	CE#	DQ5-1	DQ7-1	
L		Vccq	Vssq	Vccq	CLE-2[3]	RE#-2[3] (W/R#-2)	Vccq	Vssq	Vccq	
M		DQ1-2[3]	DQ3-2[3]	Vssq	CLE-1	RE#-1 (W/R#-1)	Vssq	DQ4-2[3]	DQ6-2[3]	
N		DQ1-1	DQ3-1	RFU	N/A[1] (DQS-2[3])	RFU	WE#-2[3] (CLK-2)	DQ4-1	DQ6-1	
P		Vssq	Vccq	RFU	N/A[1] (DQS-1)	RFU	WE#-1 (CLK-1)	Vccq	Vssq	
T	NC									NC
U	NC	NC							NC	NC

Notes:
1. N/A: This signal is tri-stated when the asynchronous interface is active.
2. Signal names in parentheses are the signal names when the synchronous interface is active.
3. These signals are available on dual, quad, and octal die packages. They are NC for other configurations.

4. These signals are available on quad die four CE# or octal die packages. They are NC for other configurations.

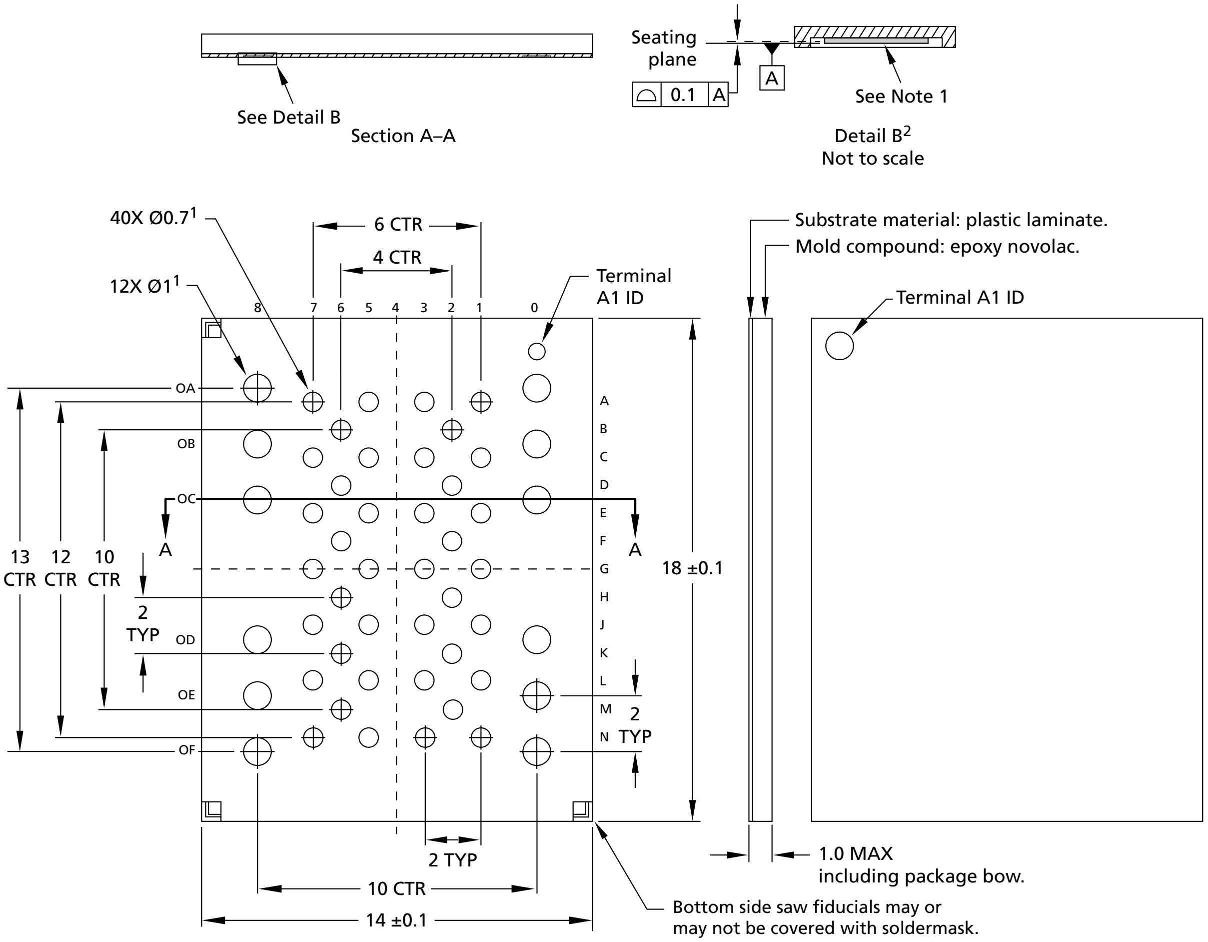
Package Dimensions

Figure 5: 48-Pin TSOP – Type 1 CPL (Package Code: WP)



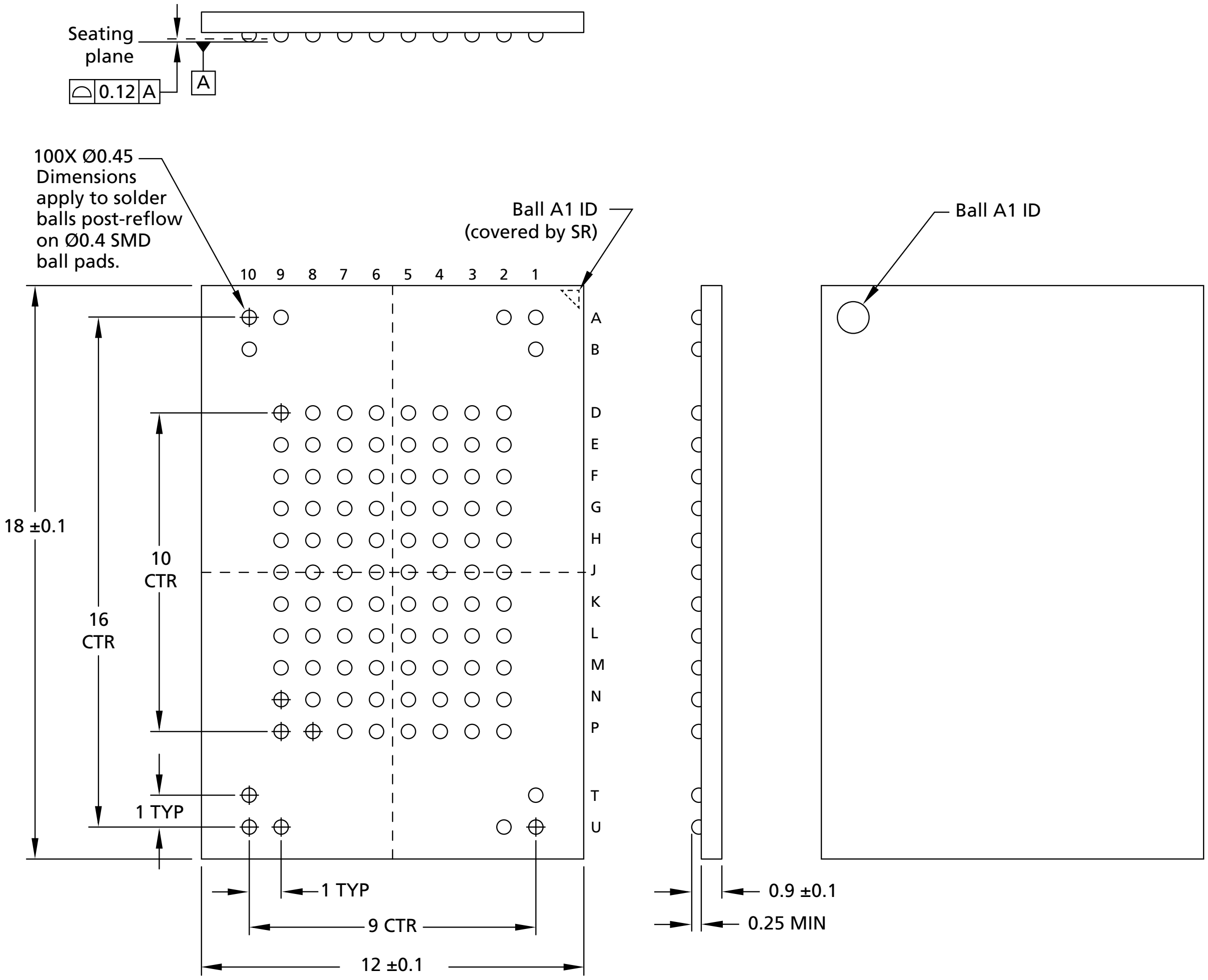
Note: 1. All dimensions are in millimeters.

Figure 6: 52-Pad VLGA



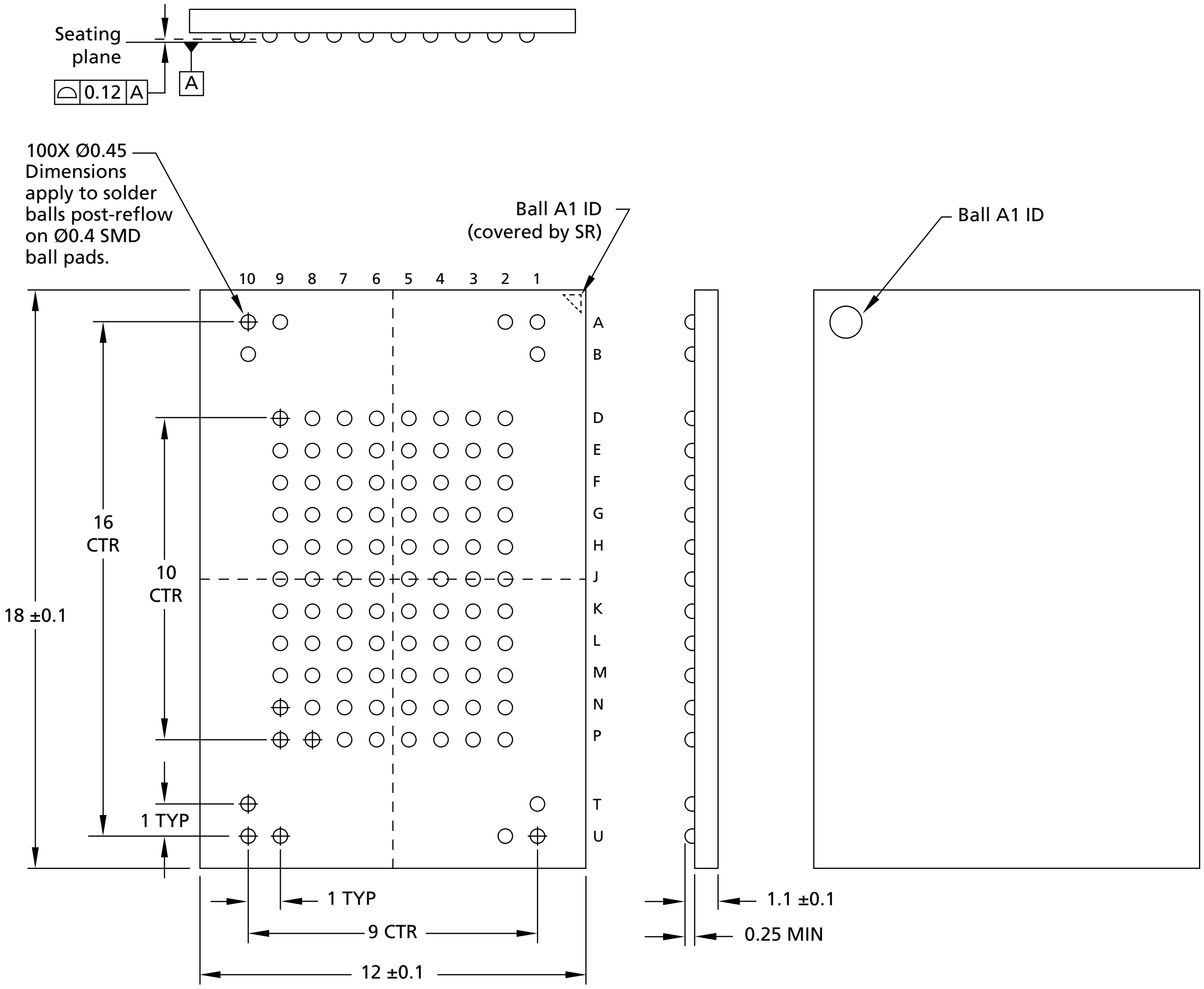
Note: 1. All dimensions are in millimeters.

Figure 7: 100-Ball VBGA – 12mm x 18mm (Package Code: H1)



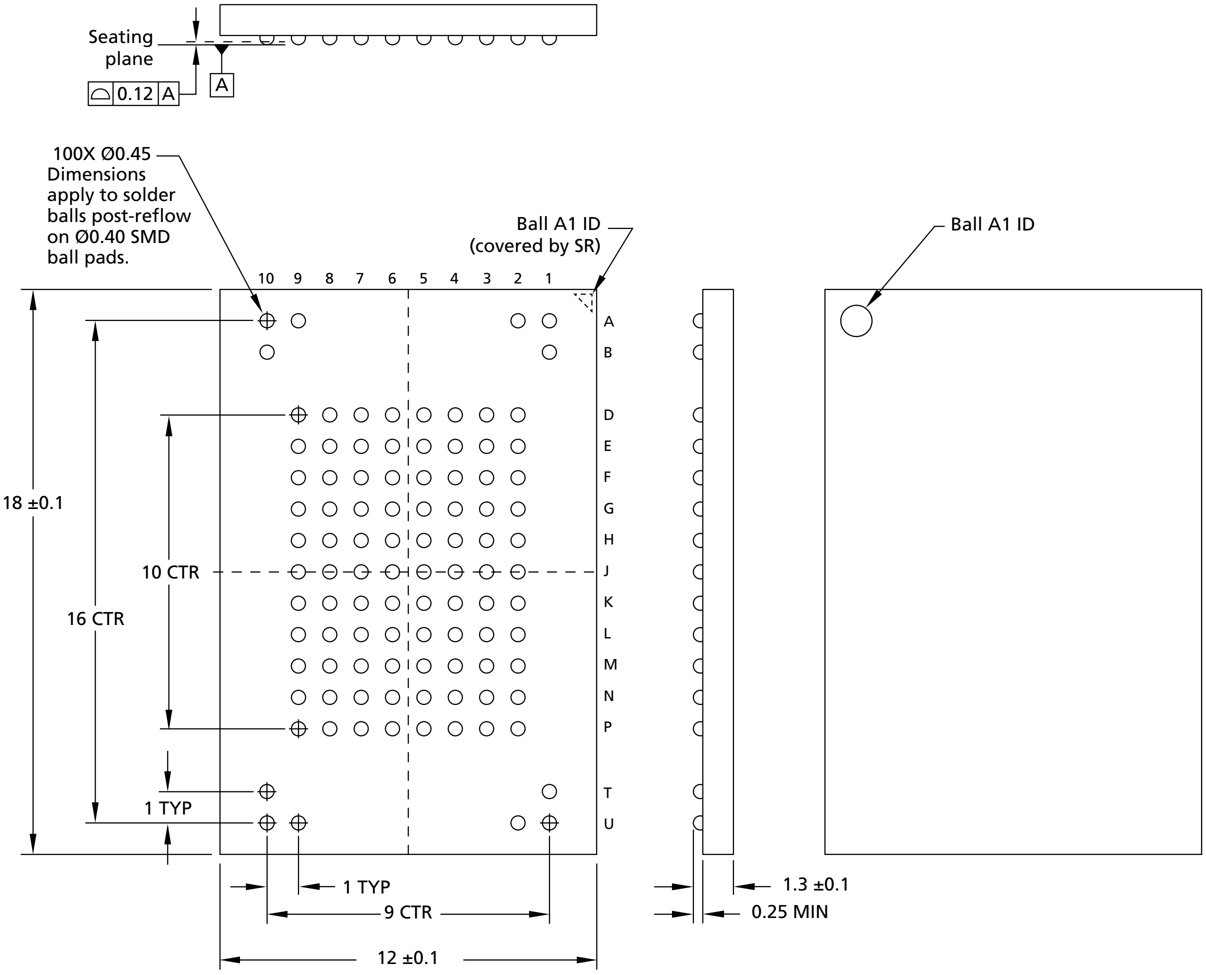
Note: 1. All dimensions are in millimeters.

Figure 8: 100-Ball TBGA – 12mm x 18mm (Package Code: H2)



Note: 1. All dimensions are in millimeters.

Figure 9: 100-Ball LBGA – 12mm x 18mm (Package Code: H3)



Note: 1. All dimensions are in millimeters.

Architecture

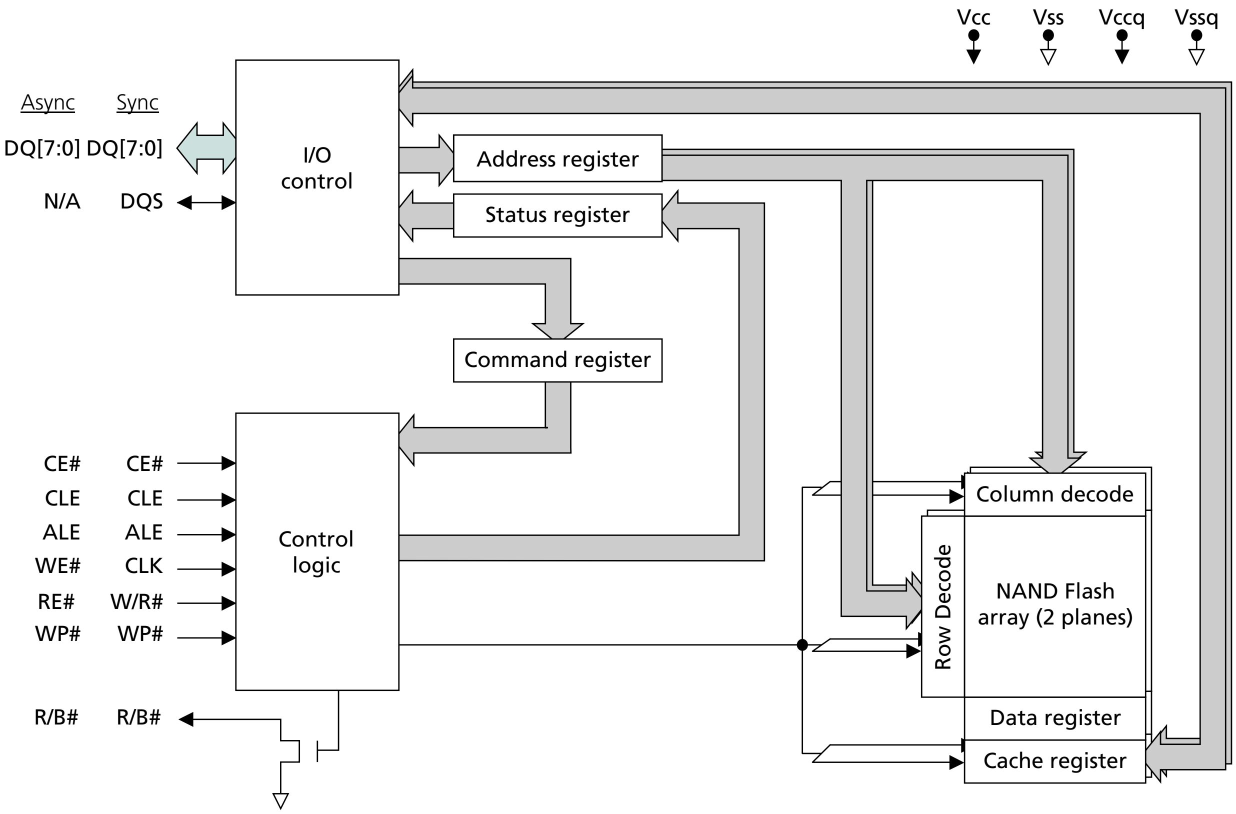
These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder to select a row address, or to a column decoder to select a column address.

Data is transferred to or from the NAND Flash memory array, byte by byte, through a data register and a cache register.

The NAND Flash memory array is programmed and read using page-based operations and is erased using block-based operations. During normal page operations, the data and cache registers act as a single register. During cache operations, the data and cache registers operate independently to increase data throughput.

The status register reports the status of die (LUN) operations.

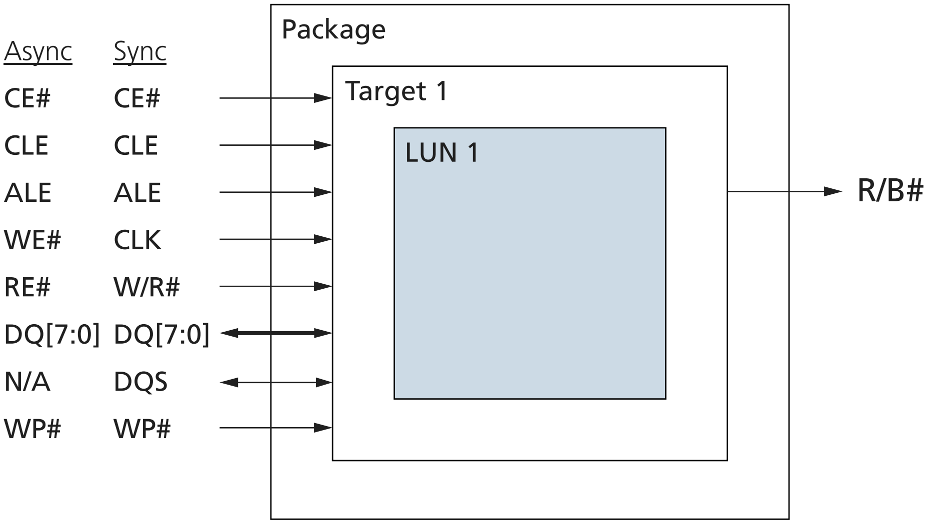
Figure 10: NAND Flash Die (LUN) Functional Block Diagram



Notes:
1. N/A: This signal is tri-stated when the asynchronous interface is active.
2. Some devices do not include the synchronous interface.

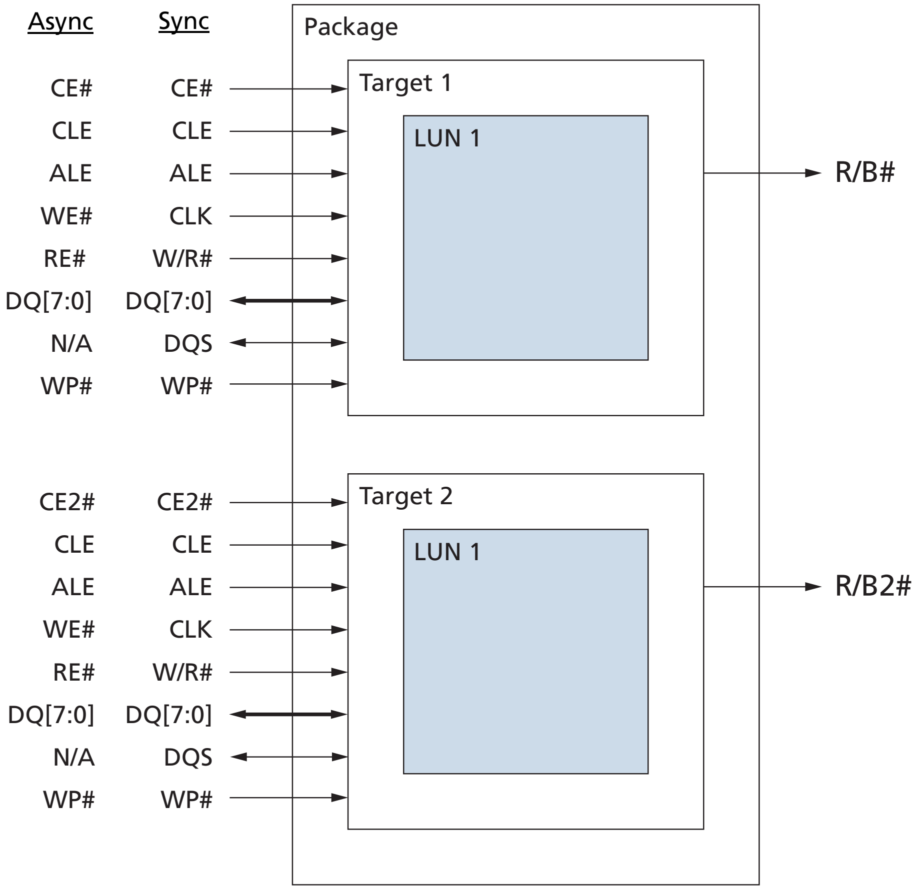
Device and Array Organization

Figure 11: Device Organization for Single-Die Package (TSOP/BGA)



Note: 1. TSOP devices do not support the synchronous interface.

Figure 12: Device Organization for Two-Die Package (TSOP)



Note: 1. TSOP devices do not support the synchronous interface.

Figure 13: Device Organization for Two-Die Package (BGA)

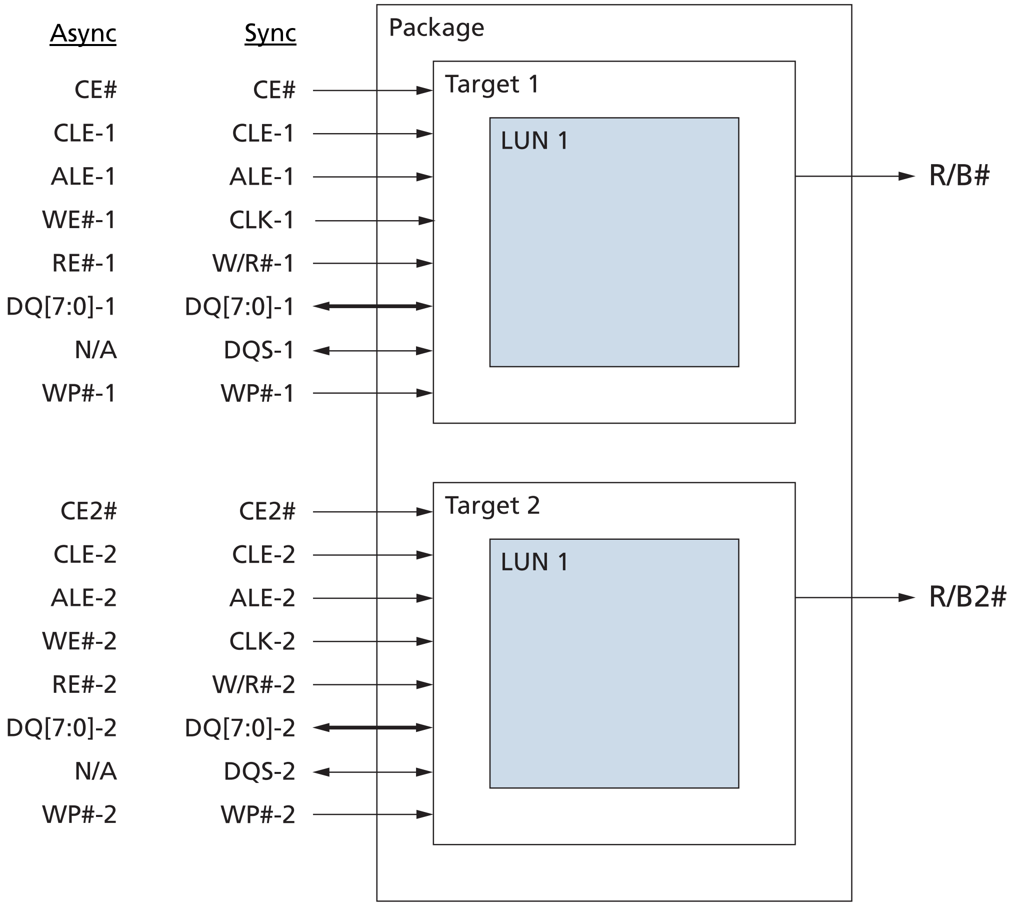
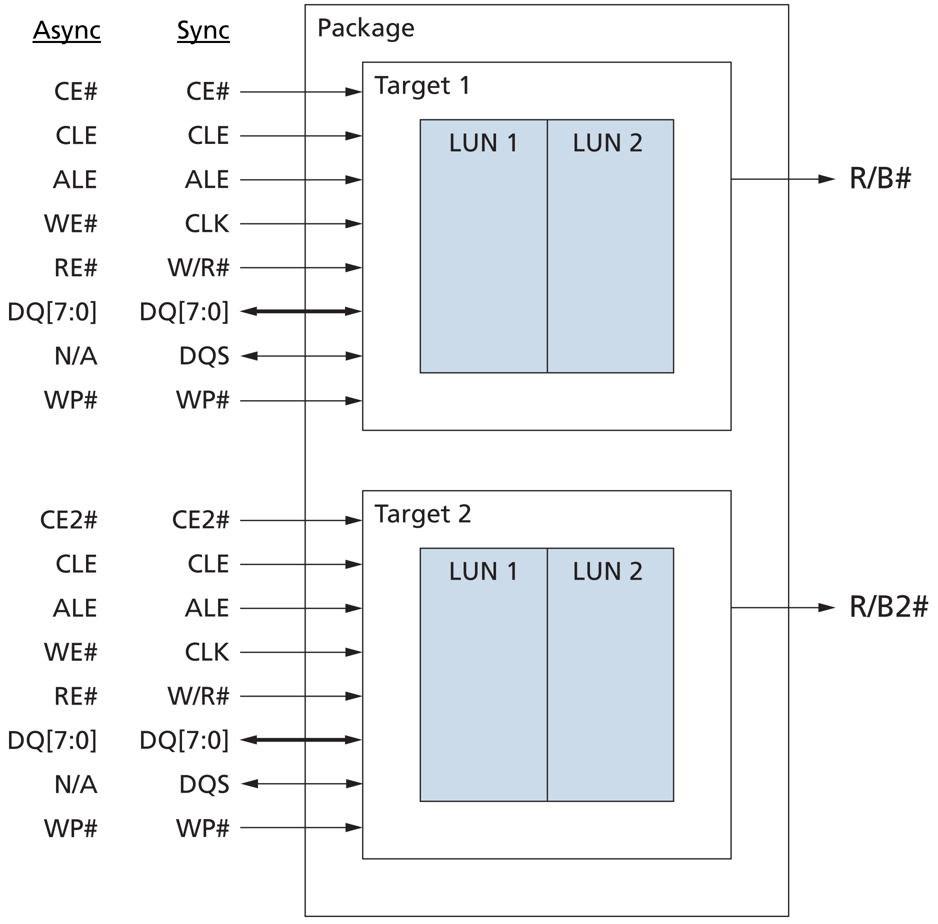
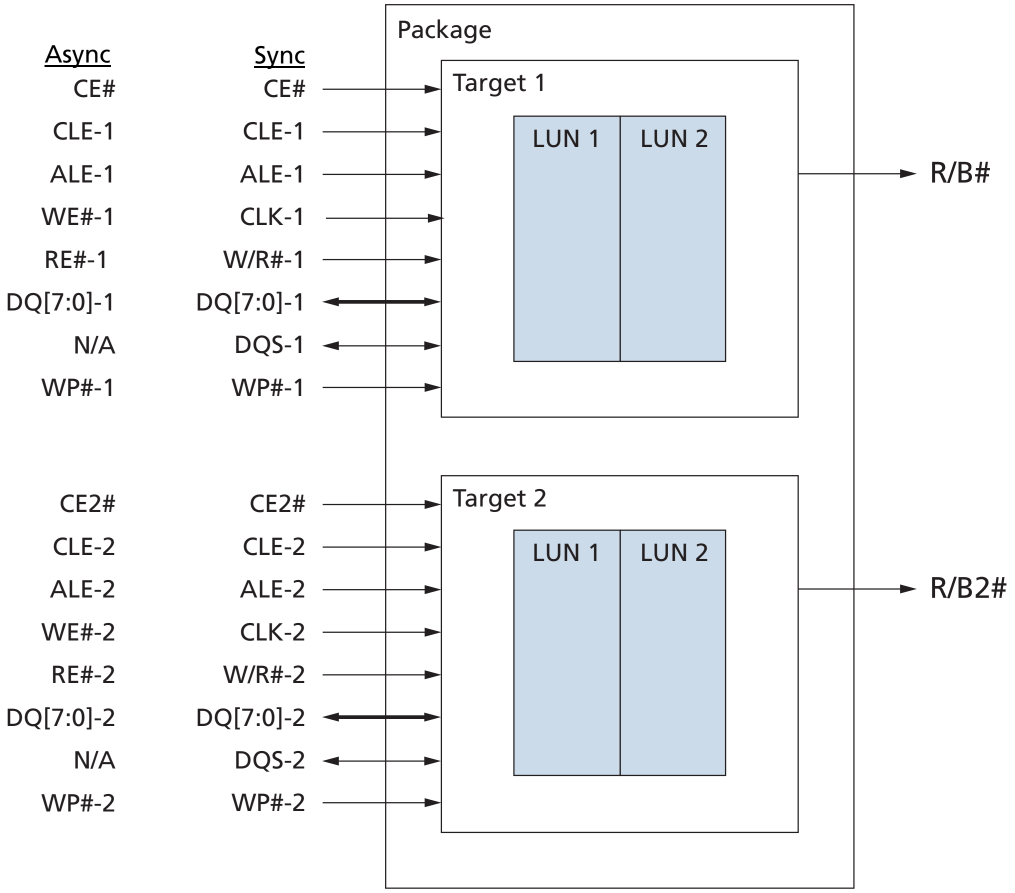


Figure 14: Device Organization for Four-Die Package (TSOP)



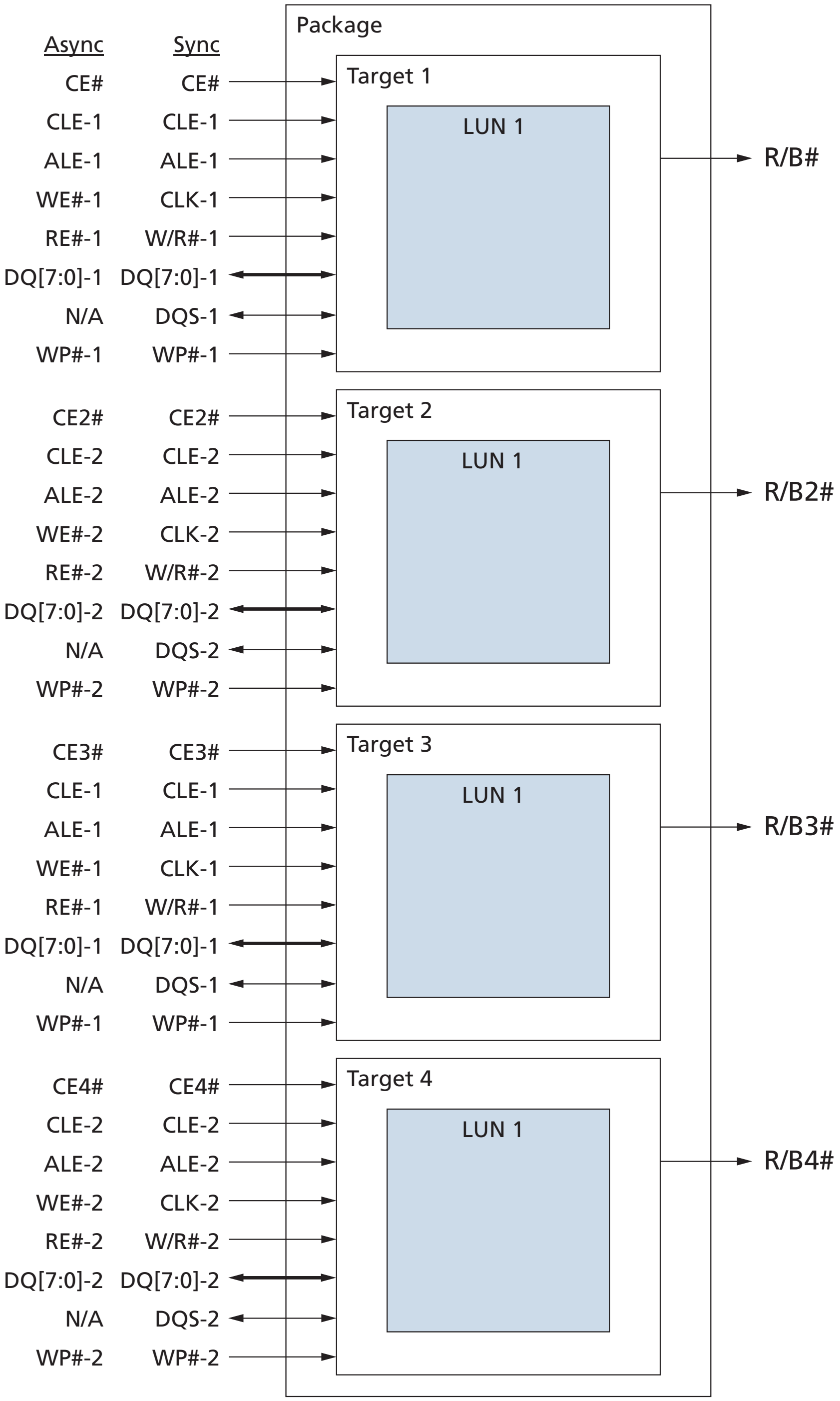
Note: 1. TSOP devices do not support the synchronous interface.

Figure 15: Device Organization for Four-Die Package with CE# and CE2# (BGA/LGA)



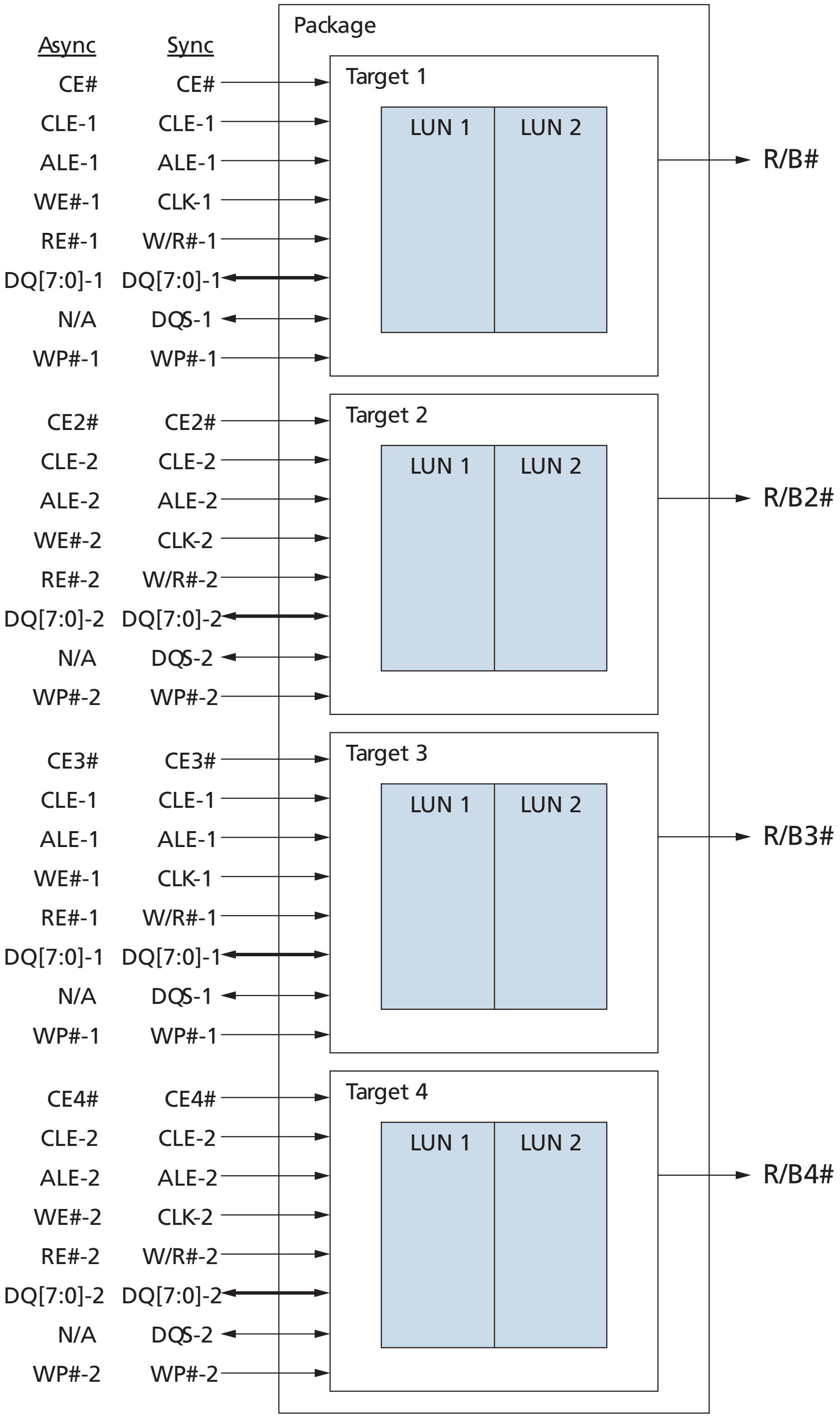
Note: 1. LGA devices do not support the synchronous interface.

Figure 16: Device Organization for Four-Die Package with CE#, CE2#, CE3#, and CE4# (BGA/LGA)



Note: 1. LGA devices do not support the synchronous interface.

Figure 17: Device Organization for Eight-Die Package (BGA/LGA)



Note: 1. LGA devices do not support the synchronous interface.

Figure 18: Array Organization per Logical Unit (LUN)

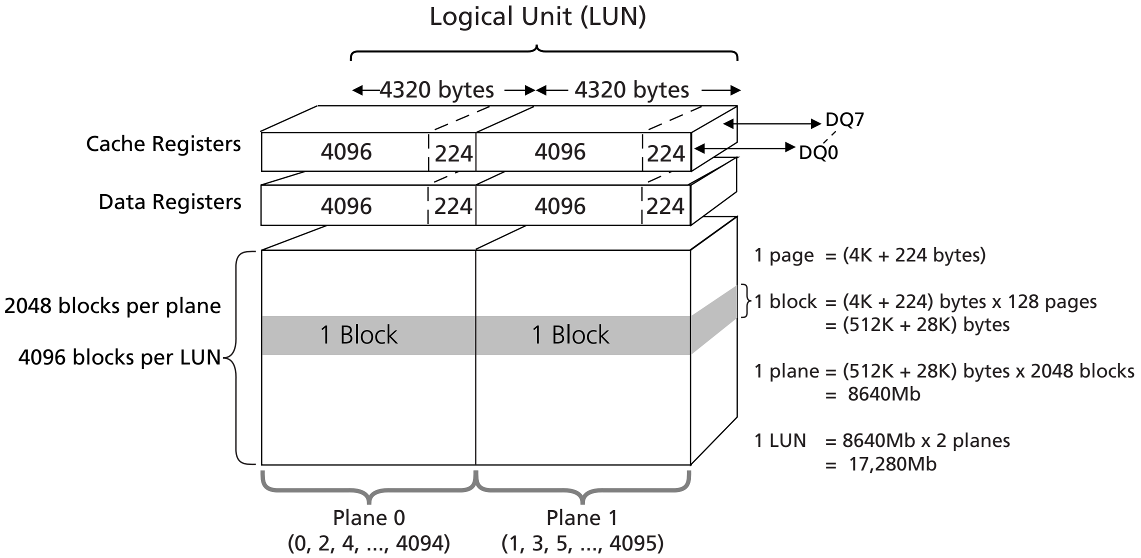


Table 2: Array Addressing for Logical Unit (LUN)

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0[2]
Second	LOW	LOW	LOW	CA12[3]	CA11	CA10	CA9	CA8
Third	BA7[4]	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LA0[5]	BA18	BA17	BA16

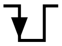
Notes:
1. CAx = column address, PAx = page address, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address.
2. When using the synchronous interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.
3. Column addresses 4320 (10E0h) through 8191 (1FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.
4. BA[7] is the plane-select bit:
   Plane 0: BA[7] = 0
   Plane 1: BA[7] = 1
5. LA0 is the LUN-select bit. It is present only when two LUNs are shared on the target; otherwise, it should be held LOW.
   LUN 0: LA0 = 0
   LUN 1: LA0 = 1

Bus Operation – Asynchronous Interface

The asynchronous interface is active when the NAND Flash device powers on. The I/O bus, DQ[7:0], is multiplexed sharing data I/O, addresses, and commands. The DQS signal, if present, is tri-stated when the asynchronous interface is active.

Asynchronous interface bus modes are summarized below.

Table 3: Asynchronous Interface Mode Selection

Mode	CE#	CLE	ALE	WE#	RE#	DQS	DQx	WP#	Notes
Standby	H	X	X	X	X	X	X	0V/V_{CCQ}[2]	2
Bus idle	L	X	X	H	H	X	X	X	
Command input	L	H	L		H	X	input	H	
Address input	L	L	H		H	X	input	H	
Data input	L	L	L		H	X	input	H	
Data output	L	L	L	H		X	output	X	
Write protect	X	X	X	X	X	X	X	L	

Notes:
1. DQS is tri-stated when the asynchronous interface is active.
2. WP# should be biased to CMOS LOW or HIGH for standby.
3. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

Asynchronous Enable/Standby

A chip enable (CE#) signal is used to enable or disable a target. When CE# is driven LOW, all of the signals for that target are enabled. With CE# LOW, the target can accept commands, addresses, and data I/O. There may be more than one target in a NAND Flash package. Each target is controlled by its own chip enable; the first target (Target 0) is controlled by CE#; the second target (if present) is controlled by CE2#, etc.

A target is disabled when CE# is driven HIGH, even when the target is busy. When disabled, all of the target's signals are disabled except CE#, WP#, and R/B#. This functionality is also known as CE# "Don't Care". While the target is disabled, other devices can utilize the disabled NAND signals that are shared with the NAND Flash.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the die (LUNs) complete their operations. Standby helps reduce power consumption.

Asynchronous Bus Idle

A target's bus is idle when CE# is LOW, WE# is HIGH, and RE# is HIGH.

During bus idle, all of the signals are enabled except DQS, which is not used when the asynchronous interface is active. No commands, addresses, and data are latched into the target; no data is output.

Asynchronous Pausing Data Input/Output

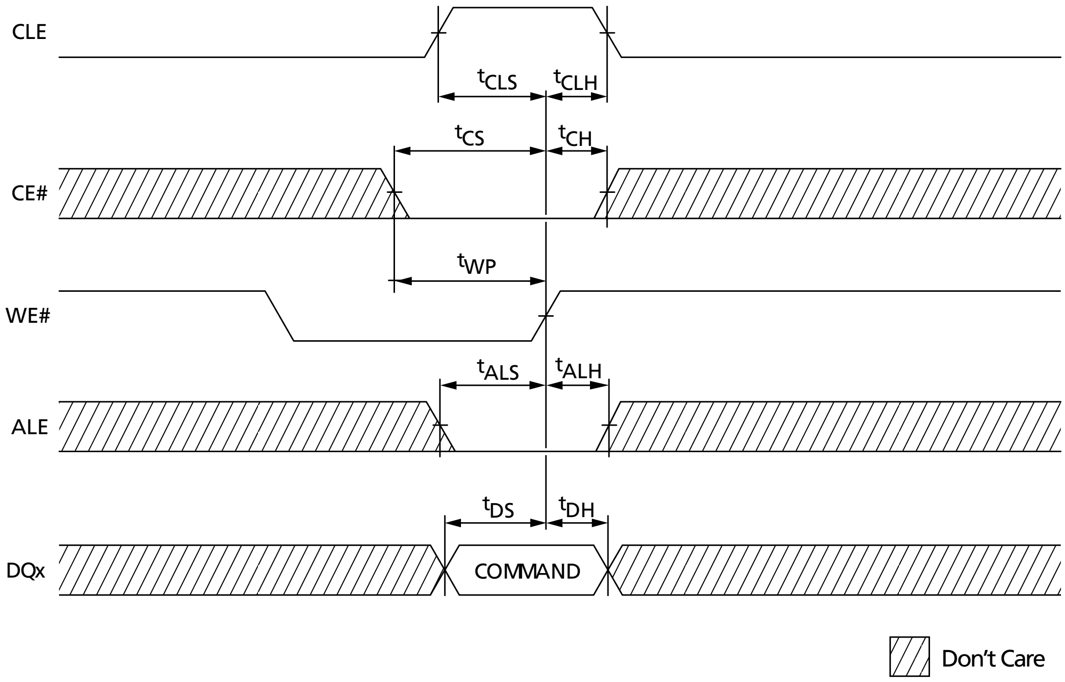
Pausing data input or data output is done by keeping WE# or RE# HIGH, respectively.

Asynchronous Commands

An asynchronous command is written from DQ[7:0] to the command register on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is HIGH, and RE# is HIGH.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, including READ STATUS (70h) and READ STATUS ENHANCED (78h), are accepted by die (LUNs) even when they are busy.

Figure 19: Asynchronous Command Latch Cycle



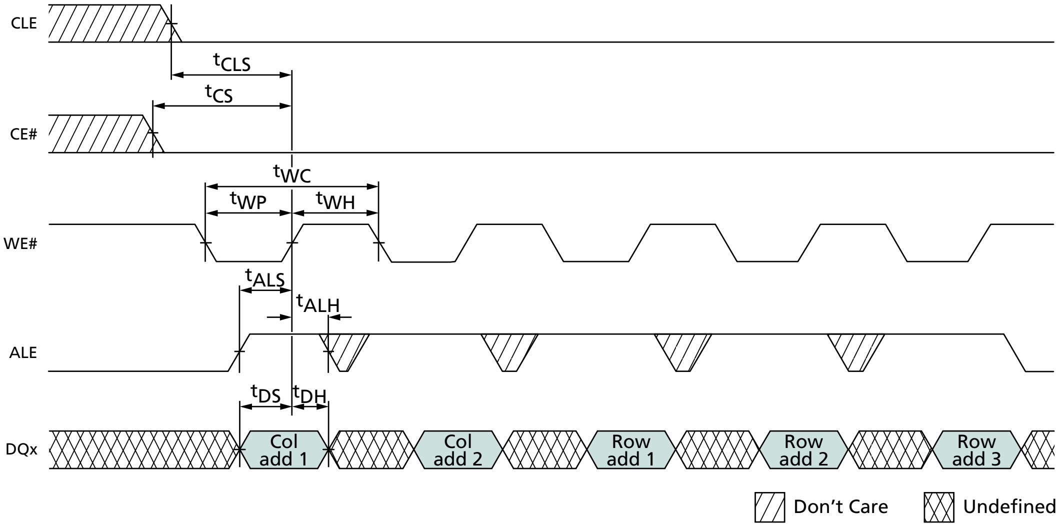
Asynchronous Addresses

An asynchronous address is written from DQ[7:0] to the address register on the rising edge of WE# when CE# is LOW, ALE is HIGH, CLE is LOW, and RE# is HIGH.

Bits that are not part of the address space must be LOW (see Device and Array Organization). The number of cycles required for each command varies. Refer to the command descriptions to determine addressing requirements (see Command Definitions).

Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses are accepted by die (LUNs) even when they are busy; for example, address cycles that follow the READ STATUS ENHANCED (78h) command.

Figure 20: Asynchronous Address Latch Cycle

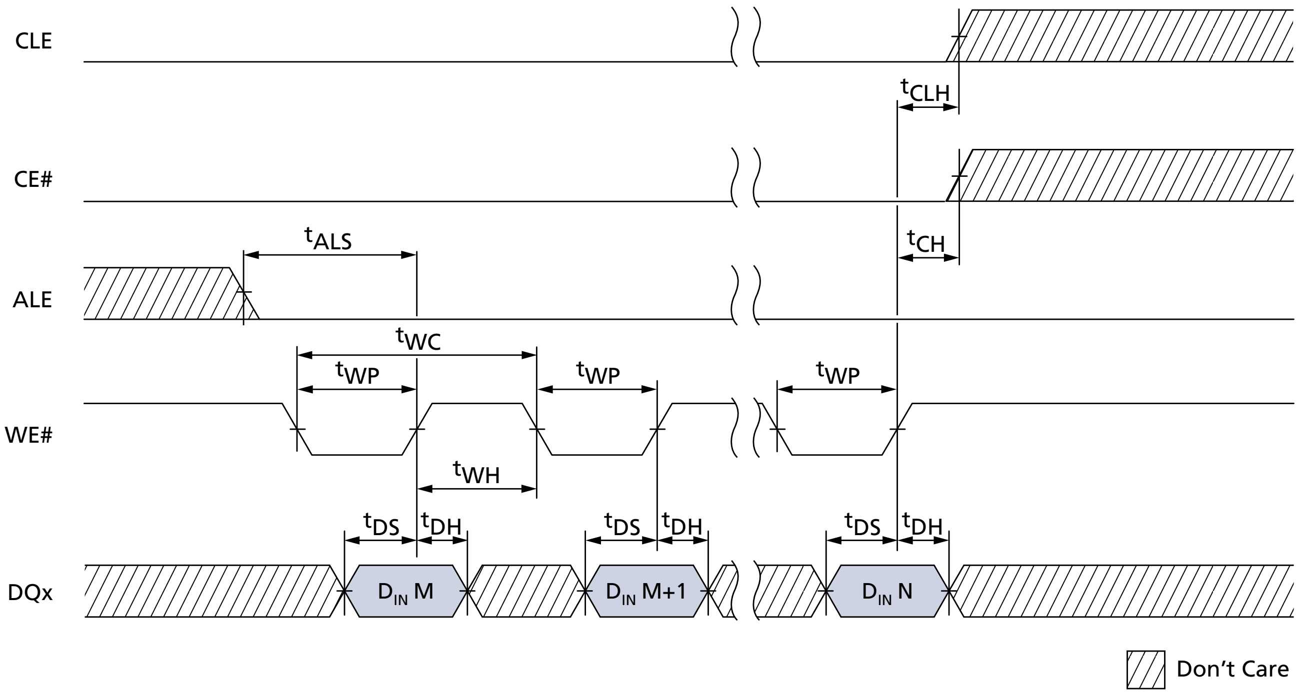


Asynchronous Data Input

Data is written from DQ[7:0] to the cache register of the selected die (LUN) on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is LOW, and RE# is HIGH.

Data input is ignored by die (LUNs) that are not selected or are busy (RDY = 0).

Figure 21: Asynchronous Data Input Cycles



Asynchronous Data Output

Data can be output from a die (LUN) if it is in a READY state. Data output is supported following a READ operation from the NAND Flash array. Data is output from the cache register of the selected die (LUN) to DQ[7:0] on the falling edge of RE# when CE# is LOW, ALE is LOW, CLE is LOW, and WE# is HIGH.

If the host controller is using a ^{t}RC of 30ns or greater, the host can latch the data on the rising edge of RE# (see Figure 22 for proper timing). If the host controller is using a ^{t}RC of less than 30ns, the host can latch the data on the next falling edge of RE# (see Figure 23 (page 35) for extended data output (EDO) timing).

Using the READ STATUS ENHANCED (78h) command prevents data contention following an interleaved die (multi-LUN) operation. After issuing the READ STATUS ENHANCED (78h) command, to enable data output, issue the READ MODE (00h) command.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by first issuing the READ STATUS (70h) or READ STATUS ENHANCED (78h) command.

Figure 22: Asynchronous Data Output Cycles

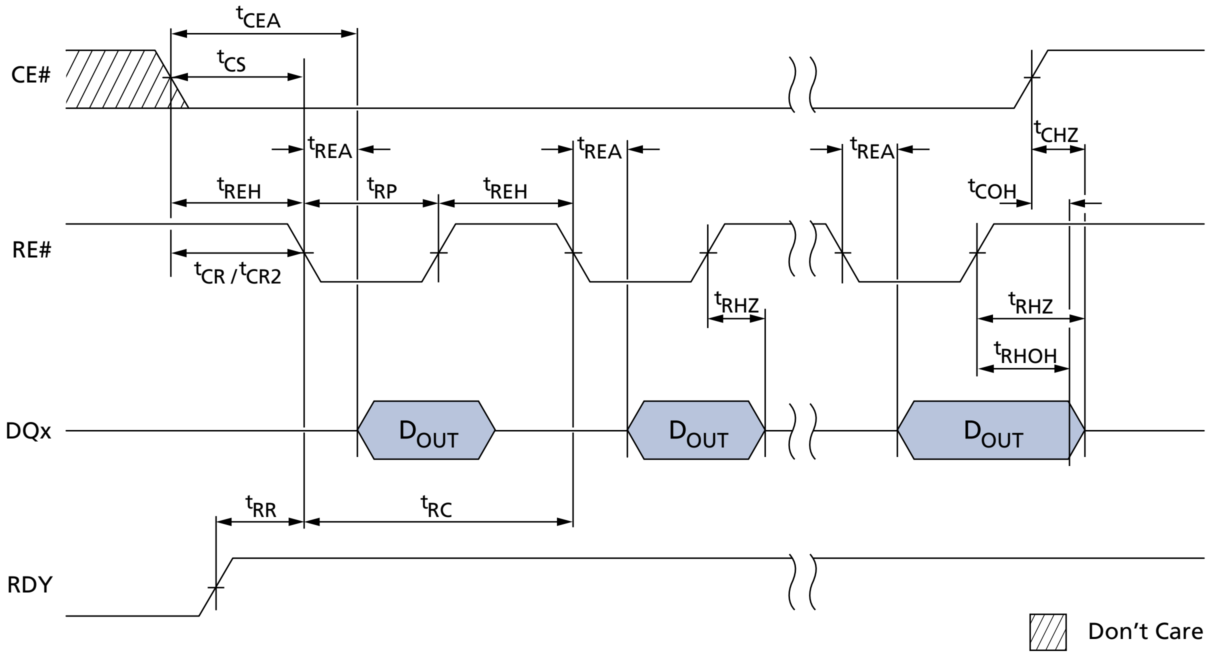
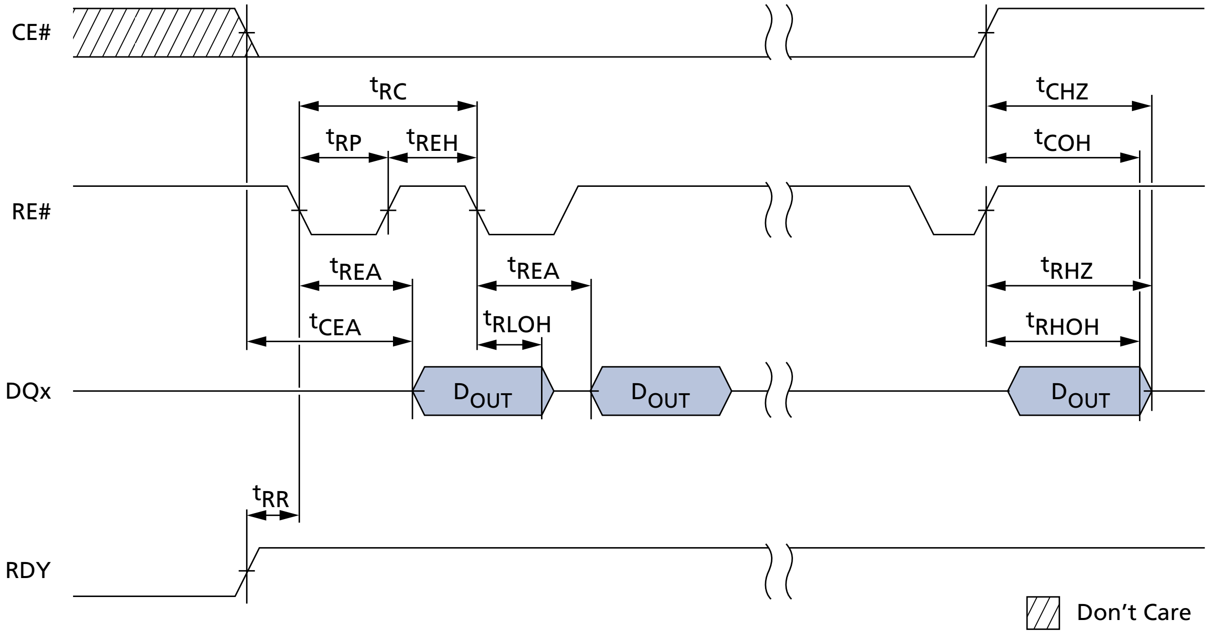


Figure 23: Asynchronous Data Output Cycles (EDO Mode)



Write Protect

The write protect# (WP#) signal enables or disables PROGRAM and ERASE operations to a target. When WP# is LOW, PROGRAM and ERASE operations are disabled. When WP# is HIGH, PROGRAM and ERASE operations are enabled.

It is recommended that the host drive WP# LOW during power-on until Vcc and Vccq are stable to prevent inadvertent PROGRAM and ERASE operations (see Device Initialization for additional details).

WP# must be transitioned only when the target is not busy and prior to beginning a command sequence. After a command sequence is complete and the target is ready, WP# can be transitioned. After WP# is transitioned, the host must wait ^{t}WW before issuing a new command.

The WP# signal is always an active input, even when CE# is HIGH. This signal should not be multiplexed with other signals.

Ready/Busy#

The ready/busy# (R/B#) signal provides a hardware method of indicating whether a target is ready or busy. A target is busy when one or more of its die (LUNs) are busy (RDY = 0). A target is ready when all of its die (LUNs) are ready (RDY = 1). Because each die (LUN) contains a status register, it is possible to determine the independent status of each die (LUN) by polling its status register instead of using the R/B# signal (see Status Operations for details regarding die (LUN) status).

This signal requires a pull-up resistor, Rp, for proper operation. R/B# is HIGH when the target is ready, and transitions LOW when the target is busy. The signal's open-drain driver enables multiple R/B# outputs to be OR-tied. Typically, R/B# is connected to an interrupt pin on the system controller (see Figure 24 (page 36)).

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# signal. The actual value used for Rp depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. Between the 10- to 90-percent points on the R/B# waveform, the rise time is approximately two time constants (TC).

$$TC = R \times C$$

Where R = Rp (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# signal and the total load capacitance. Approximate Rp values using a circuit load of 100pF are provided in Figure 29 (page 39).

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and Vccq.

$$Rp = \frac{Vccq\ (MAX) - Vol\ (MAX)}{IOL + \Sigma il}$$

Where Σil is the sum of the input currents of all devices tied to the R/B# pin.

Figure 24: READ/BUSY# Open Drain

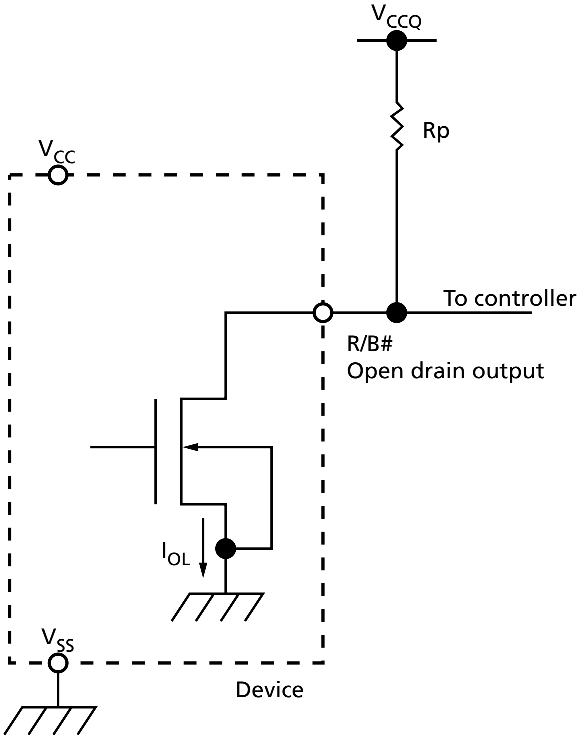
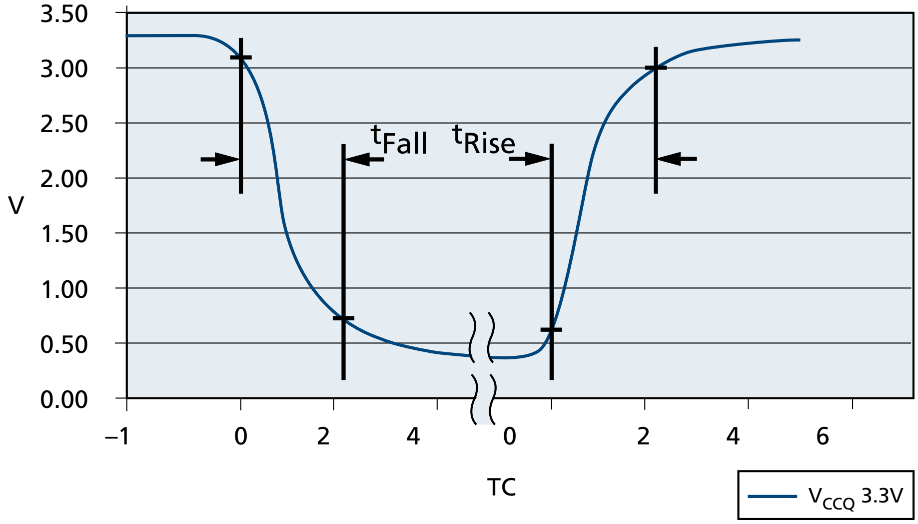
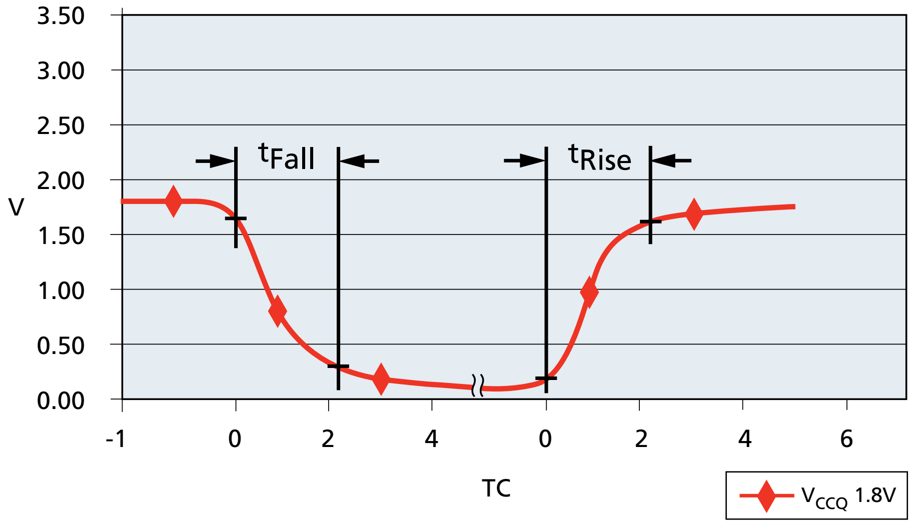


Figure 25: ^{t}Fall and ^{t}Rise (V_{CCQ} = 2.7-3.6V)



Notes:
1. ^{t}FALL is $V_{OH(DC)}$ to $V_{OL(AC)}$ and ^{t}RISE is $V_{OL(DC)}$ to $V_{OH(AC)}$.
2. ^{t}Rise dependent on external capacitance and resistive loading and output transistor impedance.
3. ^{t}Rise primarily dependent on external pull-up resistor and external capacitive loading.
4. ^{t}Fall = 10ns at 3.3V
5. See TC values in Figure 29 (page 39) for approximate Rp value and TC.

Figure 26: ^{t}Fall and ^{t}Rise (V_{CCQ} = 1.7-1.95V)



Notes:
1. ^{t}FALL is $V_{OH(DC)}$ to $V_{OL(AC)}$ and ^{t}RISE is $V_{OL(DC)}$ to $V_{OH(AC)}$.
2. ^{t}Rise is primarily dependent on external pull-up resistor and external capacitive loading.
3. ^{t}Fall ≈ 7ns at 1.8V.
4. See TC values in Figure 29 (page 39) for TC and approximate Rp value.

Figure 27: IOL vs Rp (V_{CCQ} = 2.7-3.6V)

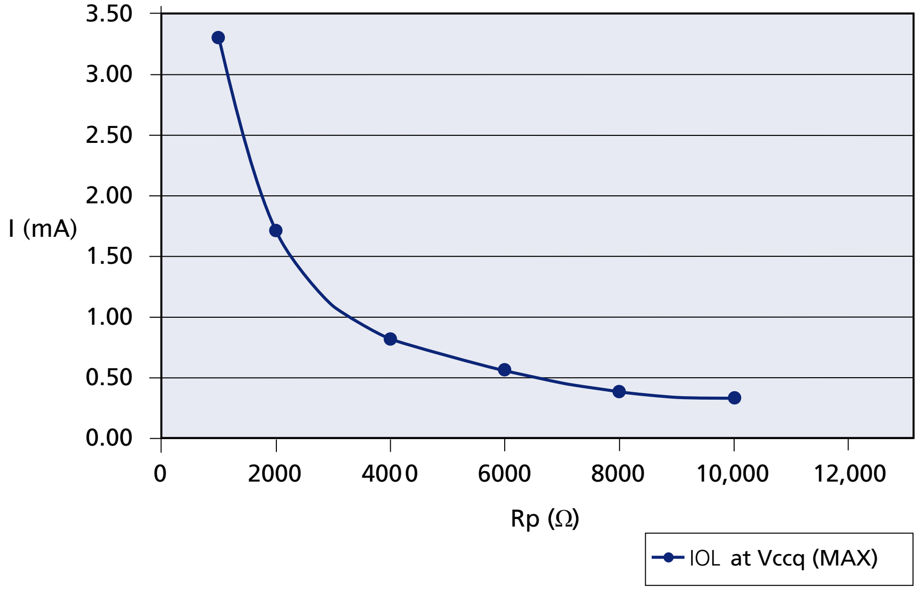


Figure 28: IOL vs Rp (V_{CCQ} = 1.7-1.95V)

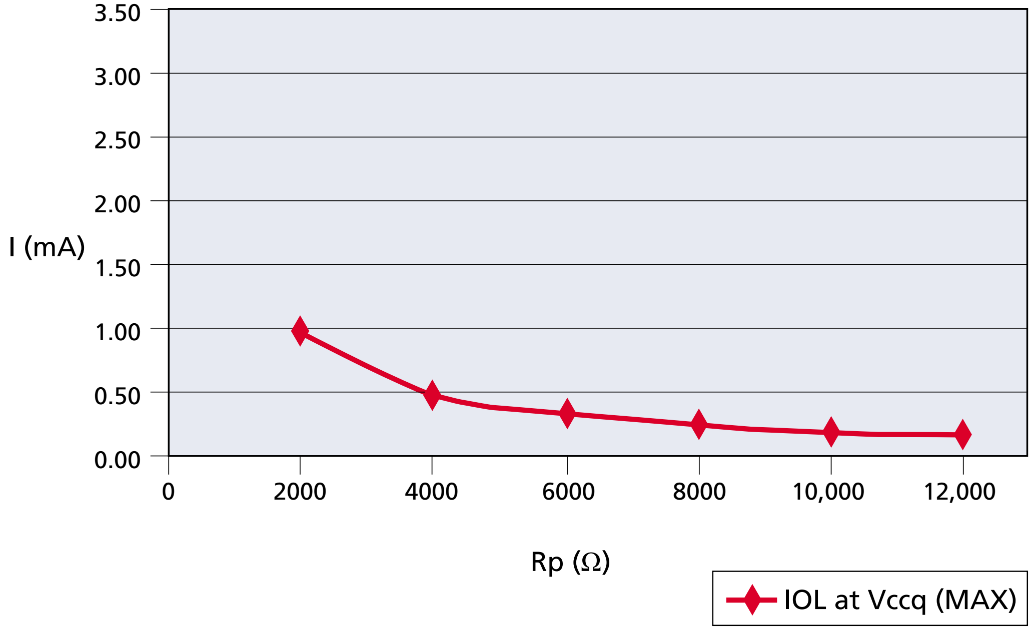
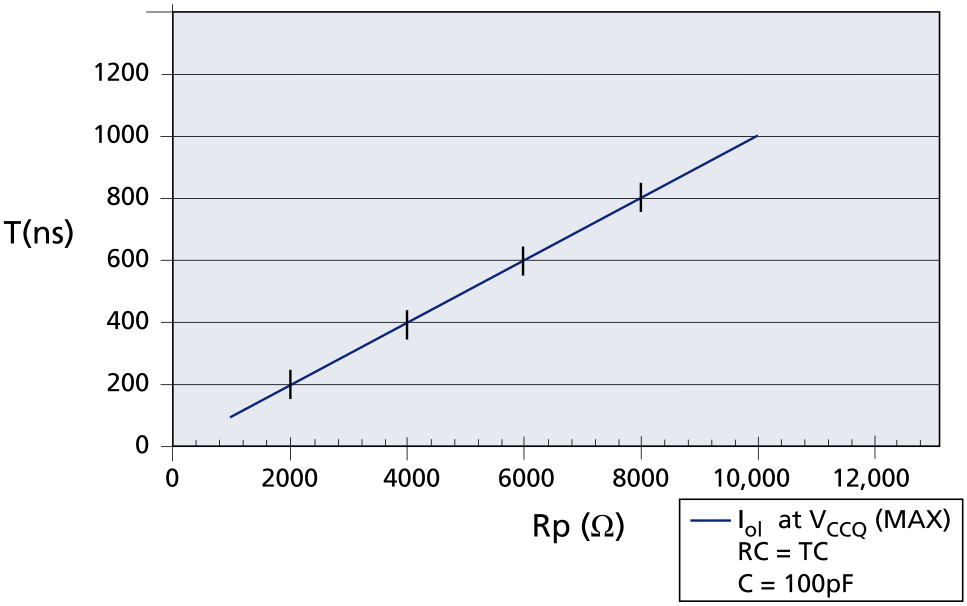


Figure 29: TC vs Rp



Bus Operation – Synchronous Interface

These NAND Flash devices have two interfaces—a synchronous interface for fast data I/O transfer and an asynchronous interface that is backward compatible with existing NAND Flash devices.

The NAND Flash command protocol for both the asynchronous and synchronous interfaces is identical. However, there are some differences between the asynchronous and synchronous interfaces when issuing command, address, and data I/O cycles using the NAND Flash signals.

When the synchronous interface is activated on a target (see Activating Interfaces), the target is capable of high-speed DDR data transfers. Existing signals are redefined for high-speed DDR I/O. The WE# signal becomes CLK. DQS is enabled. The RE# signal becomes W/R#. CLK provides a clock reference to the NAND Flash device.

DQS is a bidirectional data strobe. During data output, DQS is driven by the NAND Flash device. During data input, DQS is controlled by the host controller while inputting data on DQ[7:0].

The direction of DQS and DQ[7:0] is controlled by the W/R# signal. When the W/R# signal is latched HIGH, the controller is driving the DQ bus and DQS. When the W/R# is latched LOW, the NAND Flash is driving the DQ bus and DQS.

The synchronous interface bus modes are summarized below.

Table 4: Synchronous Interface Mode Selection

Mode	CE#	CLE	ALE	CLK	W/R#	DQS	DQ[7:0]	WP#	Notes
Standby	H	X	X	X	X	X	X	0V/V_{CCQ}	1, 2
Bus idle	L	L	L	↑	H	X	X	X	
Bus driving	L	L	L	↑	L	output	output	X	
Command input	L	H	L	↑	H	X	input	H	3
Address input	L	L	H	↑	H	X	input	H	3
Data input	L	H	H	↑↓	H	↑↓	input	H	4
Data output	L	H	H	↑↓	L	See Note 5	output	X	5
Write protect	X	X	X	X	X	X	X	L	
Undefined	L	L	H	↑	L	output	output	X	
Undefined	L	H	L	↑	L	output	output	X	

Notes:
1. CLK can be stopped when the target is disabled, even when R/B# is LOW.
2. WP# should be biased to CMOS LOW or HIGH for standby.
3. Commands and addresses are latched on the rising edge of CLK.

4. During data input to the device, DQS is the “clock” that latches the data in the cache register.
5. During data output from the NAND Flash device, DQS is an output generated from CLK after ^{t}DQSCK delay.
6. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

Synchronous Enable/Standby

In addition to the description found in Asynchronous Enable/Standby (page 30), the following requirements also apply when the synchronous interface is active.

Before enabling a target, CLK must be running and ALE and CLE must be LOW. When CE# is driven LOW, all of the signals for the selected target are enabled. The target is not enabled until ^{t}CS completes; the target's bus is then idle.

Prior to disabling a target, the target's bus must be idle. A target is disabled when CE# is driven HIGH, even when it is busy. All of the target's signals are disabled except CE#, WP#, and R/B#. After the target is disabled, CLK can be stopped.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the die (LUNs) complete their operations.

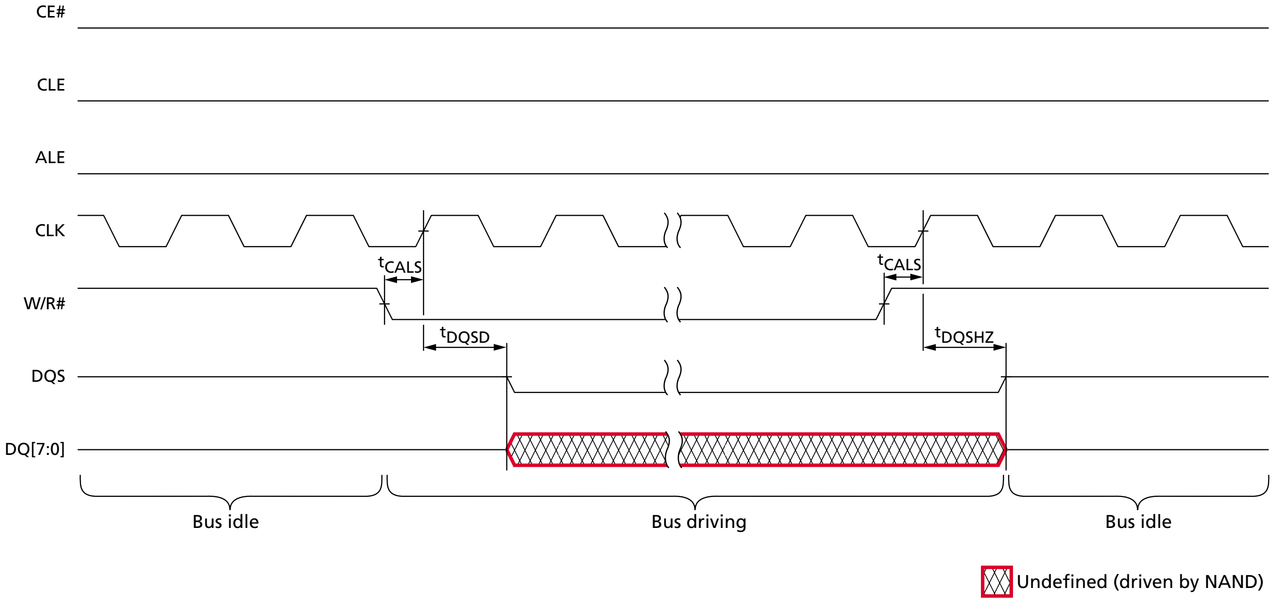
Synchronous Bus Idle/Driving

A target's bus is idle or driving when CLK is running, CE# is LOW, ALE is LOW, and CLE is LOW.

The bus is idle when W/R# transitions HIGH and is latched by CLK. During the bus idle mode, all signals are enabled; DQS and DQ[7:0] are inputs. No commands, addresses, or data are latched into the target; no data is output. When entering the bus idle mode, the host must wait a minimum of ^{t}CAD before changing the bus mode. In the bus idle mode, the only valid bus modes supported are: bus driving, command, address, and DDR data input.

The bus is driving when W/R# transitions LOW and is latched by CLK. During the bus driving mode, all signals are enabled; DQS is LOW and DQ[7:0] is driven LOW or HIGH, but no valid data is output. Following the bus driving mode, the only valid bus modes supported are bus idle and DDR data output.

Figure 30: Synchronous Bus Idle/Driving Behavior



Note: 1. Only the selected die (LUN) drives DQS and DQ[7:0]. During an interleaved die (multi-LUN) operation, the host must use the READ STATUS ENHANCED (78h) to prevent data output contention.

Synchronous Pausing Data Input/Output

Pausing data input or data output is done by setting ALE and CLE to LOW. The host may continue data transfer by setting ALE and CLE to HIGH after the applicable ^{t}CAD time has passed.

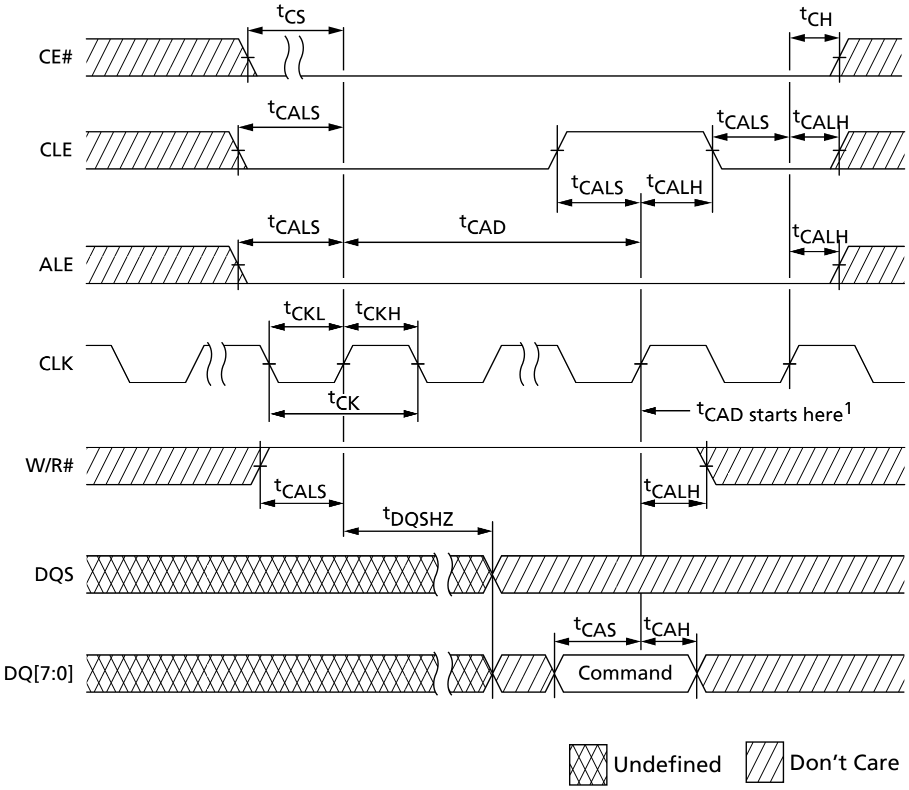
Synchronous Commands

A command is written from DQ[7:0] to the command register on the rising edge of CLK when CE# is LOW, ALE is LOW, CLE is HIGH, and W/R# is HIGH.

After a command is latched—and prior to issuing the next command, address, or data I/O—the bus must go to bus idle mode on the next rising edge of CLK, except when the clock period, ^{t}CK, is greater than ^{t}CAD.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, such as READ STATUS (70h) and READ STATUS ENHANCED (78h), are accepted by die (LUNs), even when they are busy.

Figure 31: Synchronous Command Cycle



Note: 1. When CE# remains LOW, tCAD begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

Synchronous Addresses

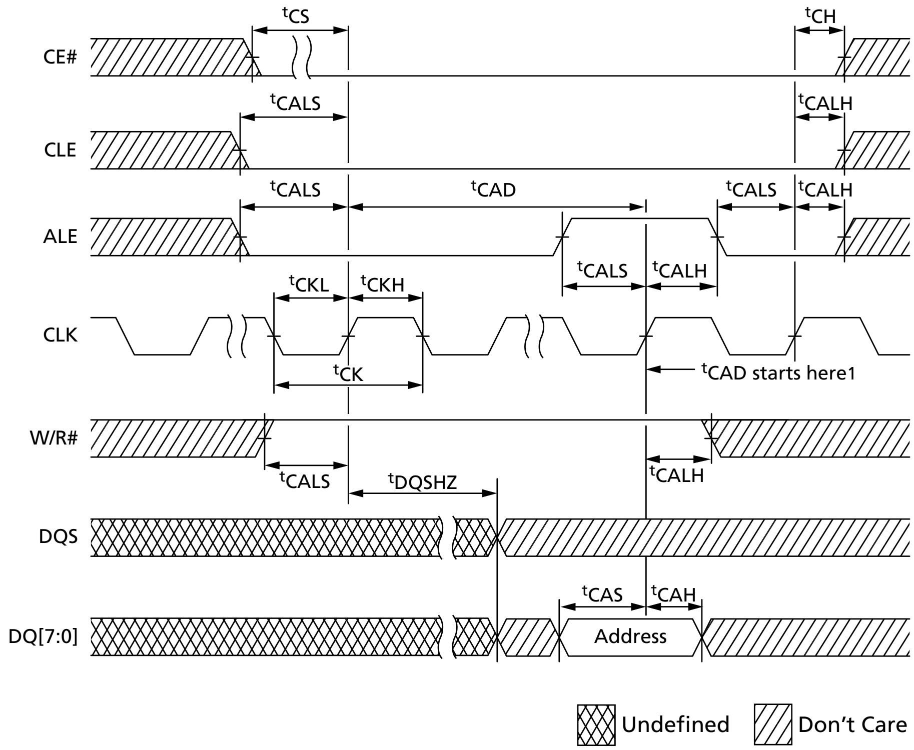
A synchronous address is written from DQ[7:0] to the address register on the rising edge of CLK when CE# is LOW, ALE is HIGH, CLE is LOW, and W/R# is HIGH.

After an address is latched—and prior to issuing the next command, address, or data I/O—the bus must go to bus idle mode on the next rising edge of CLK, except when the clock period, tCK, is greater than tCAD.

Bits not part of the address space must be LOW (see Device and Array Organization). The number of address cycles required for each command varies. Refer to the command descriptions to determine addressing requirements.

Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses such as address cycles that follow the READ STATUS ENHANCED (78h) command, are accepted by die (LUNs), even when they are busy.

Figure 32: Synchronous Address Cycle



Note: 1. When CE# remains LOW, ^{t}CAD begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

Synchronous DDR Data Input

To enter the DDR data input mode, the following conditions must be met:

- CLK is running
- CE# is LOW
- W/R# is HIGH
- ^{t}CAD is met
- DQS is LOW
- ALE and CLE are HIGH on the rising edge of CLK

Upon entering the DDR data input mode after ^{t}DQSS, data is written from DQ[7:0] to the cache register on each and every rising and falling edge of DQS (center-aligned) when CLK is running and the DQS to CLK skew meets ^{t}DSH and ^{t}DSS, CE# is LOW, W/R# is HIGH, and ALE and CLE are HIGH on the rising edge of CLK.

To exit DDR data input mode, the following conditions must be met:

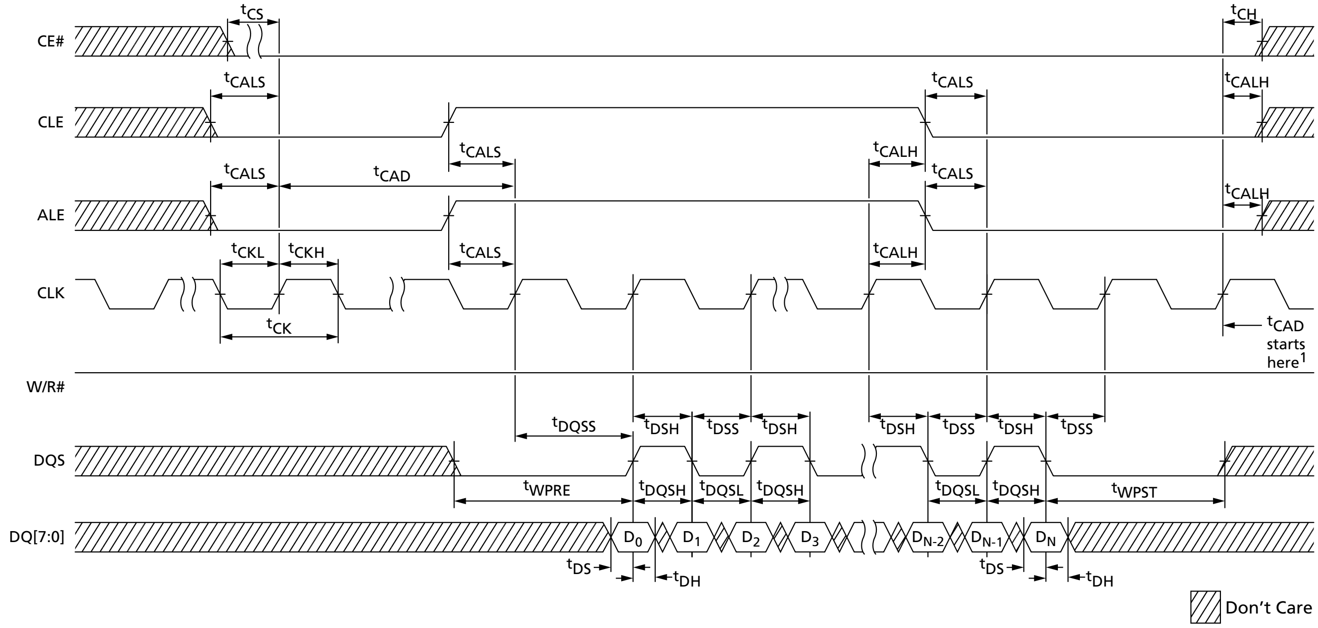
- CLK is running and the DQS to CLK skew meets ^{t}DSH and ^{t}DSS
- CE# is LOW
- W/R# is HIGH
- ALE and CLE are latched LOW on the rising edge of CLK

- The final two data bytes of the data input sequence are written to DQ[7:0] to the cache register on the rising and falling edges of DQS after the last cycle in the data input sequence in which ALE and CLE are latched HIGH.
- DQS is held LOW for ^{t}WPST (after the final falling edge of DQS)

Following ^{t}WPST, the bus enters bus idle mode and ^{t}CAD begins on the next rising edge of CLK. After ^{t}CAD starts, the host can disable the target if desired.

Data input is ignored by die (LUNs) that are not selected or are busy.

Figure 33: Synchronous DDR Data Input Cycles



Notes:
1. When CE# remains LOW, ^{t}CAD begins at the first rising edge of the clock after ^{t}WPST completes.
2. ^{t}DSH (MIN) generally occurs during ^{t}DQSS (MIN).
3. ^{t}DSS (MIN) generally occurs during ^{t}DQSS (MAX).

Synchronous DDR Data Output

Data can be output from a die (LUN) if it is ready. Data output is supported following a READ operation from the NAND Flash array.

To enter the DDR data output mode, the following conditions must be met:

- CLK is running
- CE# is LOW
- The host has released the DQ[7:0] bus and DQS
- W/R# is latched LOW on the rising edge of CLK to enable the selected die (LUN) to take ownership of the DQ[7:0] bus and DQS within ^{t}WRCK
- ^{t}CAD is met
- ALE and CLE are HIGH on the rising edge of CLK

Upon entering the DDR data output mode, DQS will toggle HIGH and LOW with a delay of ^{t}DQSCK from the respective rising and falling edges of CLK. DQ[7:0] will output data edge-aligned to the rising and falling edges of DQS, with the first transition delayed by no more than ^{t}AC.

DDR data output mode continues as long as CLK is running, CE# is LOW, W/R# is LOW, and ALE and CLE are HIGH on the rising edge of CLK.

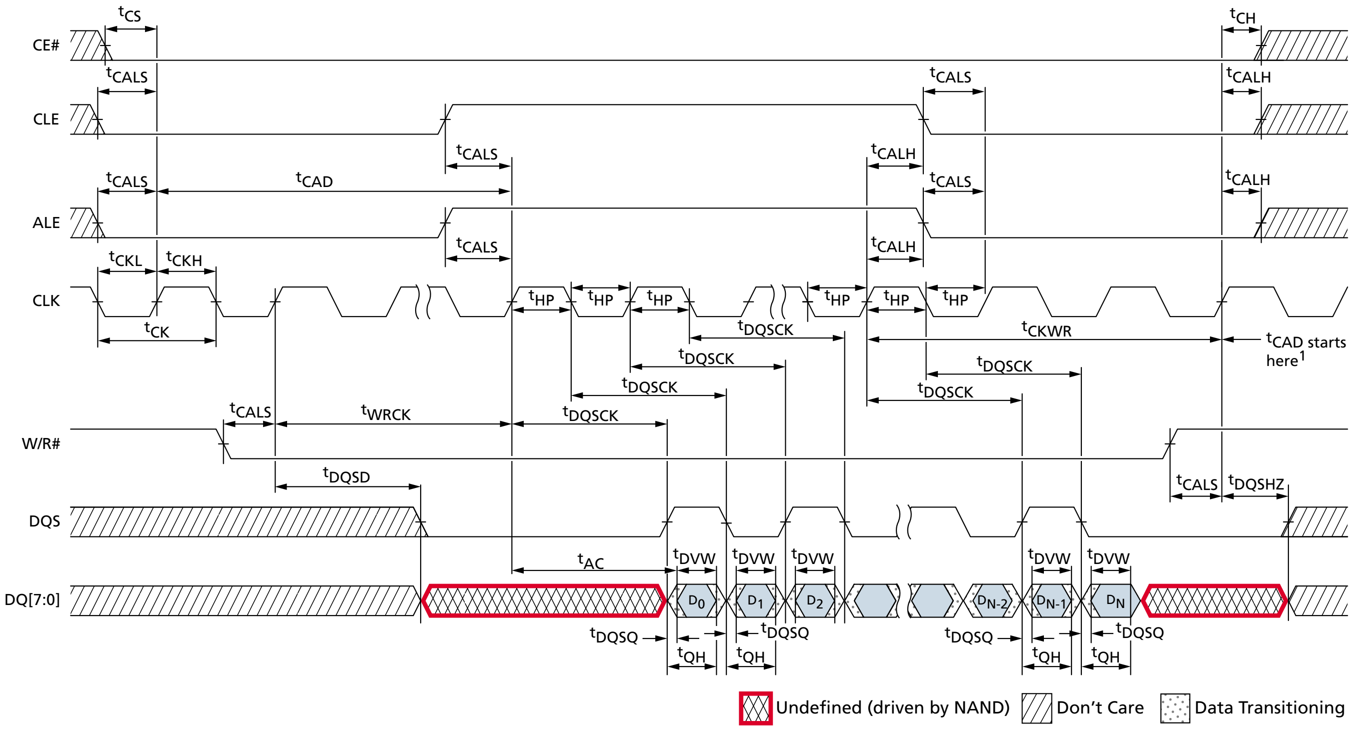
To exit DDR data output mode, the following conditions must be met:

- CLK is running
- CE# is LOW
- W/R# is LOW
- ALE and CLE are latched LOW on the rising edge of CLK

The final two data bytes are output on DQ[7:0] on the final rising and falling edges of DQS. The final rising and falling edges of DQS occur ^{t}DQSCK after the last cycle in the data output sequence in which ALE and CLE are latched HIGH. After ^{t}CKWR, the bus enters bus idle mode and ^{t}CAD begins on the next rising edge of CLK. Once ^{t}CAD starts the host can disable the target if desired.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by issuing the READ STATUS (70h) or READ STATUS ENHANCED (78h) command.

Figure 34: Synchronous DDR Data Output Cycles



Notes:
1. When CE# remains LOW, tCAD begins at the rising edge of the clock after tCKWR for subsequent command or data output cycle(s).
2. See Figure 31 (page 43) for details of W/R# behavior.
3. tAC is the DQ output window relative to CLK and is the long-term component of DQ skew.
4. For W/R# transitioning HIGH, DQ[7:0] and DQS go to tri-state.
5. For W/R# transitioning LOW, DQ[7:0] drives current state and DQS goes LOW.
6. After final data output, DQ[7:0] is driven until W/R# goes HIGH, but is not valid.

Write Protect

See Write Protect (page 35).

Ready/Busy#

See Ready/Busy# (page 35).

Device Initialization

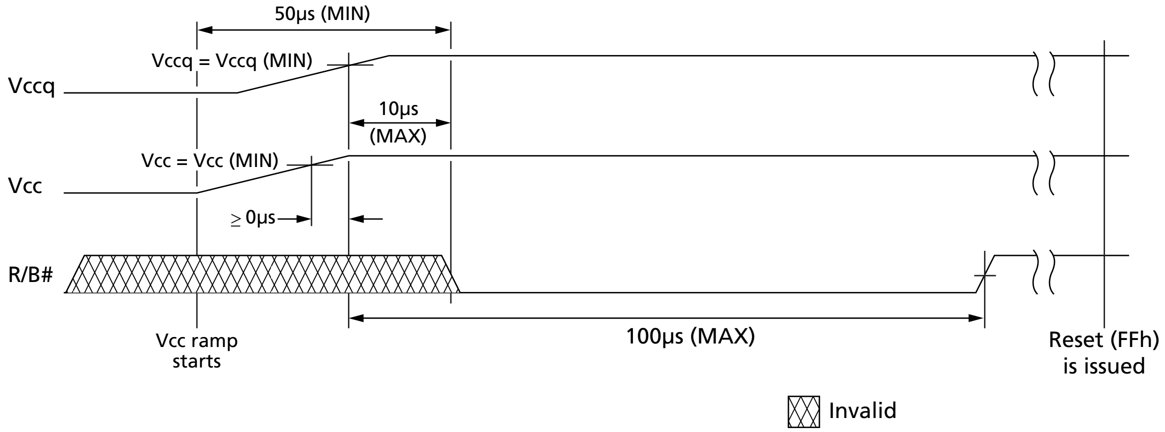
Some NAND Flash devices do not support V_{CCQ}. For these devices all references to V_{CCQ} are replaced with V_{CC}.

Micron NAND Flash devices are designed to prevent data corruption during power transitions. V_{CC} is internally monitored. (The WP# signal supports additional hardware protection during power transitions.) When ramping V_{CC} and V_{CCQ}, use the following procedure to initialize the device:

1. Ramp V_{CC}.
2. Ramp V_{CCQ}. V_{CCQ} must not exceed V_{CC}.
3. The host must wait for R/B# to be valid and HIGH before issuing RESET (FFh) to any target (see Figure 35). The R/B# signal becomes valid when 50µs has elapsed since the beginning the V_{CC} ramp, and 10µs has elapsed since V_{CCQ} reaches V_{CCQ} (MIN) and V_{CC} reaches V_{CC} (MIN).
4. If not monitoring R/B#, the host must wait at least 100µs after V_{CCQ} reaches V_{CCQ} (MIN) and V_{CC} reaches V_{CC} (MIN). If monitoring R/B#, the host must wait until R/B# is HIGH.
5. The asynchronous interface is active by default for each target. Each LUN draws less than an average of I_{ST} measured over intervals of 1ms until the RESET (FFh) command is issued.
6. The RESET (FFh) command must be the first command issued to all targets (CE#s) after the NAND Flash device is powered on. Each target will be busy for ^{t}POR after a RESET command is issued. The RESET busy time can be monitored by polling R/B# or issuing the READ STATUS (70h) command to poll the status register.
7. The device is now initialized and ready for normal operation.

At power-down, V_{CCQ} must go LOW, either before, or simultaneously with, V_{CC} going LOW.

Figure 35: R/B# Power-On Behavior



Note: 1. Disregard V_{CCQ} for devices that use only V_{CC}.

To initialize a discovered target, the following steps shall be taken. The initialization process should be followed for each connected CE# signal, including performing the READ PARAMETER PAGE (ECh) command for each target. Each chip enable corresponds to a unique target with its own independent properties that the host shall observe and subsequently use.

The host should issue the READ PARAMETET PAGE (ECh) command. This command returns information that includes the capabilities, features, and operating parameters of the device. When the information is read from the device, the host shall check the CRC to ensure that the data was received correctly and without error prior to taking action on that data.

If the CRC of the first parameter page read is not valid, the host should read redundant parameter page copies. The host can determine whether a redundant parameter page is present or not by checking if the first four bytes contain at least two bytes of the parameter page signature. If the parameter page signature is present, then the host should read the entirety of that redundant parameter page. The host should then check the CRC of that redundant parameter page. If the CRC is correct, the host may take action based on the contents of that redundant parameter page. If the CRC is incorrect, then the host should attempt to read the next redundant parameter page by the same procedure.

The host should continue reading redundant parameter pages until the host is able to accurately reconstruct the parameter page contents. The host may use bit-wise majority or other ECC techniques to recover the contents of the parameter page from the parameter page copies present. When the host determines that a parameter page signature is not present, then all parameter pages have been read.

After successfully retrieving the parameter page, the host has all information necessary to successfully communicate with that target. If the host has not previously mapped defective block information for this target, the host should next map out all defective blocks in the target. The host may then proceed to utilize the target, including erase and program operations.

Activating Interfaces

After performing the steps under Device Initialization (page 48), the asynchronous interface is active for all targets on the device.

Each target's interface is independent of other targets, so the host is responsible for changing the interface for each target.

If the host and NAND Flash device, through error, are no longer using the same interface, then steps under Activating the Asynchronous Interface are performed to resynchronize the interfaces.

Activating the Asynchronous Interface

To activate the asynchronous NAND interface, once the synchronous interface is active, the following steps are repeated for each target:

1. The host pulls CE# HIGH, disables its input to CLK, and enables its asynchronous interface.
2. The host pulls CE# LOW and issues the RESET (FFh) command, using an asynchronous command cycle.
3. R/B# goes LOW for ^{t}RST.
4. After ^{t}ITC, and during ^{t}RST, the device enters the asynchronous NAND interface. READ STATUS (70h) and READ STATUS ENHANCED (78h) are the only commands that can be issued.
5. After ^{t}RST, R/B# goes HIGH. Timing mode feature address (01h), subfeature parameter P1 is set to 00h, indicating that the asynchronous NAND interface is active and that the device is set to timing mode 0.

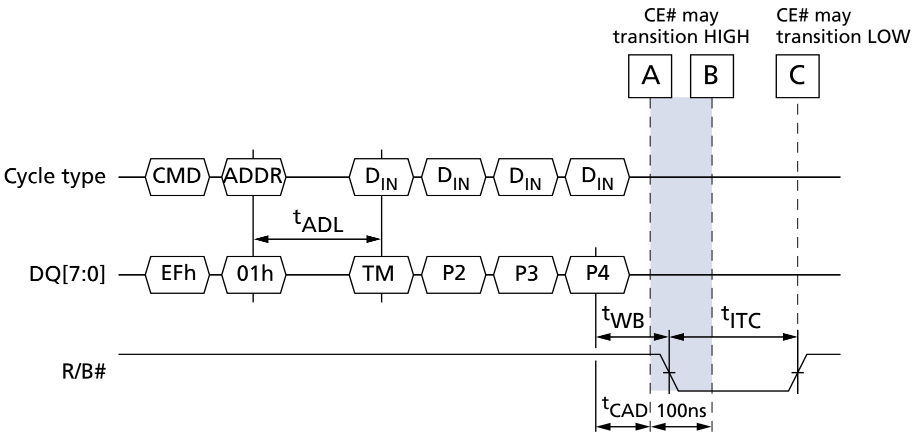
For further details, see Reset Operations.

Activating the Synchronous Interface

To activate the synchronous NAND Flash interface, the following steps are repeated for each target:

1. Issue the SET FEATURES (EFh) command.
2. Write address 01h, which selects the timing mode.
3. Write P1 with 1Xh, where "X" is the timing mode used in the synchronous interface (see Configuration Operations).
4. Write P2–P4 as 00h-00h-00h.
5. R/B# goes LOW for ^{t}ITC. The host should pull CE# HIGH. During ^{t}ITC, the host should not issue any type of command, including status commands, to the NAND Flash device.
6. After ^{t}ITC, R/B# goes HIGH and the synchronous interface is enabled. Before pulling CE# LOW, the host should enable the clock.

Figure 36: Activating the Synchronous Interface



Note: 1. TM = Timing mode.

Command Definitions

Table 5: Command Set

Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Valid While Selected LUN is Busy[1]	Valid While Other LUNs are Busy[2]	Notes
Reset Operations							
RESET	FFh	0	–	–	Yes	Yes	
SYNCHRONOUS RESET	FCh	0	–	–	Yes	Yes	
Identification Operations							
READ ID	90h	1	–	–			3
READ PARAMETER PAGE	ECh	1	–	–			
READ UNIQUE ID	EDh	1	–	–			
Configuration Operations							
GET FEATURES	EEh	1	–	–			3
SET FEATURES	EFh	1	4	–			4
Status Operations							
READ STATUS	70h	0	–	–	Yes		
READ STATUS ENHANCED	78h	3	–	–	Yes	Yes	
Column Address Operations							
CHANGE READ COLUMN	05h	2	–	E0h		Yes	
CHANGE READ COLUMN ENHANCED	06h	5	–	E0h		Yes	
CHANGE WRITE COLUMN	85h	2	Optional	–		Yes	
CHANGE ROW ADDRESS	85h	5	Optional	–		Yes	5
Read Operations							
READ MODE	00h	0	–	–		Yes	
READ PAGE	00h	5	–	30h		Yes	6
READ PAGE MULTI-PLANE	00h	5	–	32h		Yes	
READ PAGE CACHE SEQUENTIAL	31h	0	–	–		Yes	7
READ PAGE CACHE RANDOM	00h	5	–	31h		Yes	6,7
READ PAGE CACHE LAST	3Fh	0	–	–		Yes	7
Program Operations							
PROGRAM PAGE	80h	5	Yes	10h		Yes	
PROGRAM PAGE MULTI-PLANE	80h	5	Yes	11h		Yes	
PROGRAM PAGE CACHE	80h	5	Yes	15h		Yes	8

Table 5: Command Set (Continued)

Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Valid While Selected LUN is Busy[1]	Valid While Other LUNs are Busy[2]	Notes
Erase Operations							
ERASE BLOCK	60h	3	–	D0h		Yes	
ERASE BLOCK MULTI-PLANE	60h	3	–	D1h		Yes	
Copyback Operations							
COPYBACK READ	00h	5	–	35h		Yes	6
COPYBACK PROGRAM	85h	5	Optional	10h		Yes	
COPYBACK PROGRAM MULTI-PLANE	85h	5	Optional	11h		Yes	

Notes:
1. Busy means RDY = 0.
2. These commands can be used for interleaved die (multi-LUN) operations.
3. The READ ID (90h) and GET FEATURES (EEh) output identical data on rising and falling DQS edges.
4. The SET FEATURES (EFh) command requires data transition prior to the rising edge of CLK, with identical data for the rising and falling edges.
5. Command cycle #2 of 11h is conditional. See CHANGE ROW ADDRESS (85h) (page 85) for more details.
6. This command can be preceded by up to one READ PAGE MULTI-PLANE (00h-32h) command to accommodate a maximum simultaneous two-plane array operation.
7. Issuing a READ PAGE CACHE-series (31h, 00h-31h, 00h-32h, 3Fh) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a READ PAGE (00h-30h) or READ PAGE CACHE-series command; otherwise, it is prohibited.
8. Issuing a PROGRAM PAGE CACHE (80h-15h) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a PROGRAM PAGE CACHE (80h-15h) command; otherwise, it is prohibited.

Reset Operations

RESET (FFh)

The RESET (FFh) command is used to put a target into a known condition and to abort command sequences in progress. This command is accepted by all die (LUNs), even when they are busy.

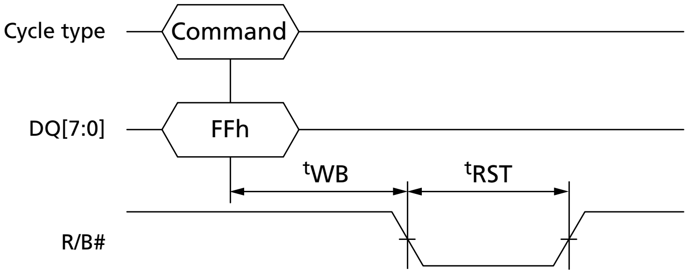
When FFh is written to the command register, the target goes busy for ^{t}RST. During ^{t}RST, the selected target (CE#) discontinues all array operations on all die (LUNs). All pending single- and multi-plane operations are cancelled. If this command is issued while a PROGRAM or ERASE operation is occurring on one or more die (LUNs), the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are invalid.

RESET must be issued as the first command to each target following power-up (see Device Initialization (page 48)). Use of the READ STATUS ENHANCED (78h) command is prohibited during the power-on RESET. To determine when the target is ready, use READ STATUS (70h).

If the RESET (FFh) command is issued when the synchronous interface is enabled, the target's interface is changed to the asynchronous interface and the timing mode is set to 0. The RESET (FFh) command can be issued asynchronously when the synchronous interface is active, meaning that CLK does not need to be continuously running when CE# is transitioned LOW and FFh is latched on the rising edge of CLK. After this command is latched, the host should not issue any commands during ^{t}ITC. After ^{t}ITC, and during or after ^{t}RST, the host can poll each LUN's status register.

If the RESET (FFh) command is issued when the asynchronous interface is active, the target's asynchronous timing mode remains unchanged. During or after ^{t}RST, the host can poll each LUN's status register.

Figure 37: RESET (FFh) Operation



SYNCHRONOUS RESET (FCh)

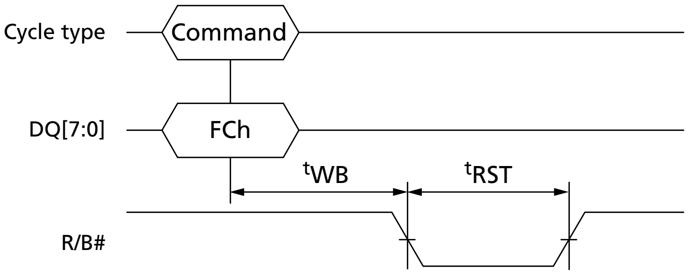
When the synchronous interface is active, the SYNCHRONOUS RESET (FCh) command is used to put a target into a known condition and to abort command sequences in progress. This command is accepted by all die (LUNs), even when they are BUSY.

When FCh is written to the command register, the target goes busy for ^tRST. During ^tRST, the selected target (CE#) discontinues all array operations on all die (LUNs). All pending single- and multi-plane operations are cancelled. If this command is issued while a PROGRAM or ERASE operation is occurring on one or more die (LUNs), the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are invalid and the synchronous interface remains active.

During or after ^tRST, the host can poll each LUN's status register.

SYNCHRONOUS RESET is only accepted while the synchronous interface is active. Its use is prohibited when the asynchronous interface is active.

Figure 38: SYNCHRONOUS RESET (FCh) Operation



Identification Operations

READ ID (90h)

The READ ID (90h) command is used to read identifier codes programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

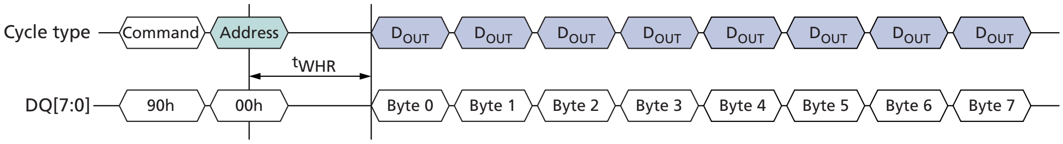
Writing 90h to the command register puts the target in read ID mode. The target stays in this mode until another valid command is issued.

When the 90h command is followed by a 00h address cycle, the target returns a 5-byte identifier code that includes the manufacturer ID, device configuration, and part-specific information.

When the 90h command is followed by a 20h address cycle, the target returns the 4-byte ONFI identifier code.

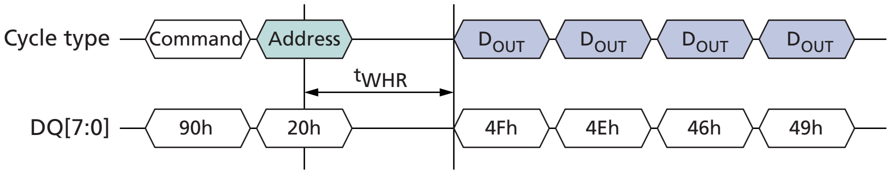
After the 90h and address cycle are written to the target, the host enables data output mode to read the identifier information. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, one data byte is output per rising edge of DQS when ALE and CLE are HIGH; the data byte on the falling edge of DQS is identical to the data byte output on the previous rising edge of DQS.

Figure 39: READ ID (90h) with 00h Address Operation



Note: 1. See the READ ID Parameter tables for byte definitions.

Figure 40: READ ID (90h) with 20h Address Operation



Note: 1. See the READ ID Parameter tables for byte definitions.

READ ID Parameter Tables

Table 6: Read ID Parameters for Address 00h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
MT29F16G08ABABA	2Ch	48h	00h	26h	89h	00h	00h	00h
MT29F16G08ABCBB	2Ch	48h	00h	26h	89h	00h	00h	00h
MT29F32G08AFABA	2Ch	48h	00h	26h	89h	00h	00h	00h
MT29F32G08AECBB	2Ch	48h	00h	26h	89h	00h	00h	00h
MT29F64G08AJABA	2Ch	68h	01h	A6h	89h	00h	00h	00h
MT29F64G08AKABA	2Ch	68h	01h	A6h	89h	00h	00h	00h
MT29F64G08AKCBB	2Ch	68h	01h	A6h	89h	00h	00h	00h
MT29F64G08AMABA	2Ch	48h	00h	26h	89h	00h	00h	00h
MT29F64G08AMCBB	2Ch	48h	00h	26h	89h	00h	00h	00h
MT29F128G08AUABA	2Ch	68h	01h	A6h	89h	00h	00h	00h
MT29F128G08AUCBB	2Ch	68h	01h	A6h	89h	00h	00h	00h

Note: 1. h = hexadecimal.

Table 7: Read ID Parameters for Address 20h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
All	4Fh	4Eh	46h	49h	XXh

Notes: 1. h = hexadecimal.
2. XXh = Undefined.

Configuration Operations

The SET FEATURES (EFh) and GET FEATURES (EEh) commands are used to modify the target's default power-on behavior. These commands use a one-byte feature address to determine which subfeature parameters will be read or modified. Each feature address (in the 00h to FFh range) is defined in Table 8. The SET FEATURES (EFh) command writes subfeature parameters (P1-P4) to the specified feature address. The GET FEATURES command reads the subfeature parameters (P1-P4) at the specified feature address.

Unless otherwise specifed, the values of the feature addresses do not change when RESET (FFh, FCh) is issued by the host.

Table 8: Feature Address Definitions

Feature Address	Definition
00h	Reserved
01h	Timing mode
02h–0Fh	Reserved
10h	Programmable output drive strength
11h–7Fh	Reserved
80h	Programmable output drive strength
81h	Programmable RB# pull-down strength
82h–8Fh	Reserved
90h	Array operation mode
91h–FFh	Reserved

SET FEATURES (EFh)

The SET FEATURES (EFh) command writes the subfeature parameters (P1-P4) to the specified feature address to enable or disable target-specific features. This command is accepted by the target only when all die (LUNs) on the target are idle.

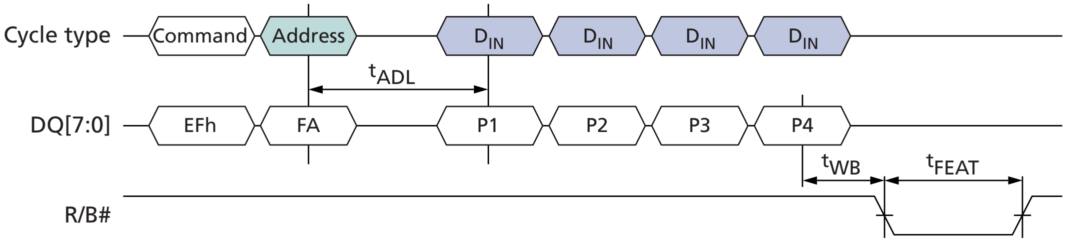
Writing EFh to the command register puts the target in the set features mode. The target stays in this mode until another command is issued.

The EFh command is followed by a valid feature address. The host waits for ^{t}ADL before the subfeature parameters are input. When the asynchronous interface is active, one subfeature parameter is latched per rising edge of WE#. When the synchronous interface is active, one subfeature parameter is latched per rising edge of DQS. The data on the falling edge of DQS should be identical to the subfeature parameter input on the previous rising edge of DQS. The device is not required to wait for the repeated data byte before beginning internal actions.

After all four subfeature parameters are input, the target goes busy for ^{t}FEAT. The READ STATUS (70h) command can be used to monitor for command completion.

Feature address 01h (timing mode) operation is unique. If SET FEATURES is used to modify the interface type, the target will be busy for ^{t}ITC.

Figure 41: SET FEATURES (EFh) Operation



GET FEATURES (EEh)

The GET FEATURES (EEh) command reads the subfeature parameters (P1-P4) from the specified feature address. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EEh to the command register puts the target in get features mode. The target stays in this mode until another valid command is issued.

When the EEh command is followed by a feature address, the target goes busy for ^{t}FEAT. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. During and prior to data output, use of the READ STATUS ENHANCED (78h) command is prohibited.

After ^{t}FEAT completes, the host enables data output mode to read the subfeature parameters. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, one subfeature parameter is output per DQS toggle on rising or falling edge of DQS.

Figure 42: GET FEATURES (EEh) Operation

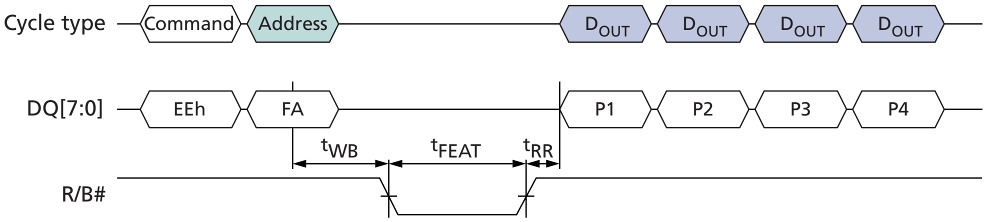


Table 9: Feature Address 01h: Timing Mode

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Timing mode	Mode 0 (default)					0	0	0	0	x0h	1, 2
	Mode 1					0	0	0	1	x1h	
	Mode 2					0	0	1	0	x2h	
	Mode 3					0	0	1	1	x3h	
	Mode 4					0	1	0	0	x4h	
	Mode 5					0	1	0	1	x5h	
Data interface	Asynchronous (default)			0	0					0xh	1
	Synchronous DDR			0	1					1xh	
	Reserved			1	x					2xh	
Reserved		0	0							00b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes:
1. Asynchronous timing mode 0 is the default, power-on value.
2. If the synchronous interface is active, a RESET (FFh) command will change the timing mode and data interface bits of feature address 01h to their default values. If the asynchronous interface is active, a RESET (FFh) command will not change the values of the timing mode or data interface bits to their default valued.

Table 10: Feature Addresses 10h and 80h: Programmable Output Drive Strength

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Output drive strength	Overdrive 2							0	0	00h	1
	Overdrive 1							0	1	01h	
	Nominal (default)							1	0	02h	
	Underdrive							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	

Table 10: Feature Addresses 10h and 80h: Programmable Output Drive Strength (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. See Output Drive Impedance for details.

Table 11: Feature Addresses 81h: Programmable R/B# Pull-Down Strength

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
R/B# pull-down strength	Full (default)							0	0	00h	1
	Three-quarter							0	1	01h	
	One-half							1	0	02h	
	One-quarter							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. This feature address is used to change the default R/B# pull-down strength. Its strength should be selected based on the expected loading of R/B#. Full strength is the default, power-on value.

Table 12: Feature Addresses 90h: Array Operation Mode

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Array Operation Mode	Normal (default)								0	00h	
	OTP Block								1	01h	1
Reserved		0	0	0	0	0	0	0		00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											

Table 12: Feature Addresses 90h: Array Operation Mode (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Reserved		0	0	0	0	0	0	0	0	00h	

Notes:
1. See One-Time Programmable (OTP) Operations for details.
2. A RESET (FFh) command will cause the bits of the array operation mode to change to their default values.

READ PARAMETER PAGE (ECh)

The READ PARAMETER PAGE (ECh) command is used to read the ONFI parameter page programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing ECh to the command register puts the target in read parameter page mode. The target stays in this mode until another valid command is issued.

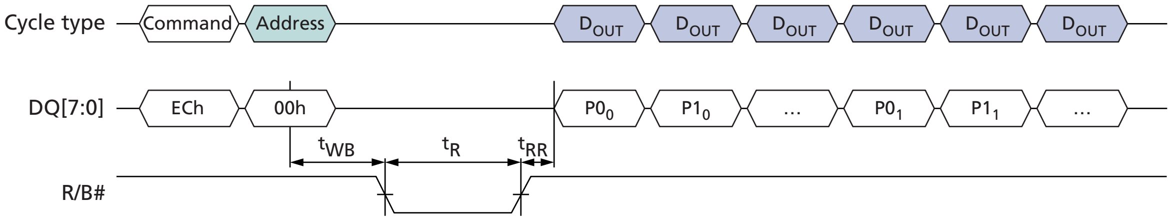
When the ECh command is followed by an 00h address cycle, the target goes busy for ^{t}R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. Use of the READ STATUS ENHANCED (78h) command is prohibited while the target is busy and during data output.

After ^{t}R completes, the host enables data output mode to read the parameter page. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, one data byte is output for each rising or falling edge of DQS.

A minimum of three copies of the parameter page are stored in the device. Each parameter page is 256 bytes. If desired, the CHANGE READ COLUMN (05h-E0h) command can be used to change the location of data output. Use of the CHANGE READ COLUMN ENHANCED (06h-E0h) command is prohibited.

The READ PARAMETER PAGE (ECh) output data can be used by the host to configure its internal settings to properly use the NAND Flash device. Parameter page data is static per part, however the value can be changed through the product cycle of NAND Flash. The host should interpret the data and configure itself accordingly.

Figure 43: READ PARAMETER (ECh) Operation



Parameter Page Data Structure Tables

Table 13: Parameter Page Data Structure

Byte	Description	Device	Values
Revision information and features block			
0–3	Parameter page signature Byte 0: 4Fh, “O” Byte 1: 4Eh, “N” Byte 2: 46h, “F” Byte 3: 49h, “I”	–	4Fh, 4Eh, 46h, 49h
4–5	Revision number Bit[15:4]: Reserved (0) Bit 3: 1 = supports ONFI verion 2.1 Bit 2: 1 = supports ONFI version 2.0 Bit 1: 1 = supports ONFI version 1.0 Bit 0: Reserved (0)	–	0Eh, 00h
6–7	Features supported Bit[15:8]: Reserved (0) Bit 7: 1 = supports extended parameter page Bit 6: 1 = supports interleaved (multi-plane) read operations Bit 5: 1 = supports synchronous interface Bit 4: 1 = supports odd-to-even page copyback Bit 3: 1 = supports interleaved (multi-plane) program and erase operations Bit 2: 1 = supports non-sequential page programming Bit 1: 1 = supports multiple LUN operations Bit 0: 1 = supports 16-bit data bus width	MT29F16G08ABABA	58h, 00h
		MT29F32G08AFABA	
		MT29F64G08AMABA	
		MT29F64G08AJABA	5Ah, 00h
		MT29F64G08AKABA	
		MT29F128G08AUABA	
		MT29F16G08ABCBB	78h, 00h
		MT29F32G08AECBB	
		MT29F64G08AMCBB	
		MT29F64G08AKCBB	7Ah, 00h
		MT29F128G08AUCBB	
8–9	Optional commands supported Bit[15:9]: Reserved (0) Bit 8: 1 = supports small data move Bit 7: 1 = supports CHANGE ROW ADDRESS Bit 6: 1 = supports CHANGE READ COLUMN ENHANCED Bit 5: 1 = supports READ UNIQUE ID Bit 4: 1 = supports COPYBACK Bit 3: 1 = supports READ STATUS ENHANCED Bit 2: 1 = supports GET FEATURES and SET FEATURES Bit 1: 1 = supports read cache commands Bit 0: 1 = supports PROGRAM PAGE CACHE	–	FFh, 01h
10–11	Reserved (0)	–	All 00h
12–13	Reserved (0)	–	All 00h
14	Number of parameter pages	–	03h
15–31	Reserved (0)	–	All 00h
Manufacturer information block			

Table 13: Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
32–43	Device manufacturer (12 ASCII characters) Micron	–	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h
44–63	Device model (20 ASCII characters)	MT29F16G08ABABAWP	4Dh, 54h, 32h, 39h, 46h, 31h, 36h, 47h, 30h, 38h, 41h, 42h, 41h, 42h, 41h, 57h, 50h, 20h, 20h, 20h
		MT29F32G08AFABAWP	4Dh, 54h, 32h, 39h, 46h, 33h, 32h, 47h, 30h, 38h, 41h, 46h, 41h, 42h, 41h, 57h, 50h, 20h, 20h, 20h
		MT29F64G08AJABAWP	4Dh, 54h, 32h, 39h, 46h, 36h, 34h, 47h, 30h, 38h, 41h, 4Ah, 41h, 42h, 41h, 57h, 50h, 20h, 20h, 20h
		MT29F64G08AKABAC5	4Dh, 54h, 32h, 39h, 46h, 36h, 34h, 47h, 30h, 38h, 41h, 4Bh, 41h, 42h, 41h, 43h, 35h, 20h, 20h, 20h
		MT29F64G08AMABAC5	4Dh, 54h, 32h, 39h, 46h, 36h, 34h, 47h, 30h, 38h, 41h, 4Dh, 41h, 42h, 41h, 43h, 35h, 20h, 20h, 20h
		MT29F128G08AUABAC5	4Dh, 54h, 32h, 39h, 46h, 31h, 32h, 38h, 47h, 30h, 38h, 41h, 55h, 41h, 42h, 41h, 43h, 35h, 20h, 20h

Table 13: Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
		MT29F16G08ABCBBH1	4Dh, 54h, 32h, 39h, 46h, 31h, 36h, 47h, 30h, 38h, 41h, 42h, 43h, 42h, 42h, 48h, 31h, 20h, 20h, 20h
		MT29F32G08AECBBH1	4Dh, 54h, 32h, 39h, 46h, 33h, 32h, 47h, 30h, 38h, 41h, 45h, 43h, 42h, 42h, 48h, 31h, 20h, 20h, 20h
		MT29F64G08AKCBBH2	4Dh, 54h, 32h, 39h, 46h, 36h, 34h, 47h, 30h, 38h, 41h, 4Bh, 43h, 42h, 42h, 48h, 32h, 20h, 20h, 20h
		MT29F64G08AMCBBH2	4Dh, 54h, 32h, 39h, 46h, 36h, 34h, 47h, 30h, 38h, 41h, 4Dh, 43h, 42h, 42h, 48h, 32h, 20h, 20h, 20h
		MT29F128G08AUCBBH3	4Dh, 54h, 32h, 39h, 46h, 31h, 32h, 38h, 47h, 30h, 38h, 41h, 55h, 43h, 42h, 42h, 48h, 33h, 20h, 20h
64	JEDEC manufacturer ID	–	2Ch
65–66	Date code	–	00h, 00h
67–79	Reserved (0)	–	All 00h
Memory organization block			
80–83	Number of data bytes per page	–	00h, 10h, 00h, 00h
84–85	Number of spare bytes per page	–	E0h, 00h
86–89	Number of data bytes per partial page	–	00h, 02h, 00h, 00h
90–91	Number of spare bytes per partial page	–	1Ch, 00h
92–95	Number of pages per block	–	80h, 00h, 00h, 00h
96–99	Number of blocks per LUN	–	00h, 10h, 00h, 00h

Table 13: Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
100	Number of LUNs per chip enable	MT29F16G08ABABA	01h
		MT29F16G08ABCBB	
		MT29F32G08AFABA	
		MT29F32G08AECBB	
		MT29F64G08AMABA	
		MT29F64G08AMCBB	
		MT29F64G08AJABA	02h
		MT29F64G08AKABA	
		MT29F64G08AKCBB	
		MT29F128G08AUABA	
		MT29F128G08AUCBB	
101	Number of address cycles Bit[7:4]: Column address cycles Bit[3:0]: Row address cycles	–	23h
102	Number of bits per cell	–	01h
103–104	Bad blocks maximum per LUN	–	50h, 00h
105–106	Block endurance	–	01h, 05h
107	Guaranteed valid blocks at beginning of target	–	01h
108–109	Block endurance for guaranteed valid blocks	–	00h, 00h
110	Number of programs per page	–	04h
111	Partial programming attributes Bit[7:5]: Reserved Bit 4: 1 = partial page layout is partial page data followed by partial page spare Bit[3:1]: Reserved Bit 0: 1 = partial page programming has constraints	–	00h
112	Number of bits ECC correctability	–	04h
113	Number of interleaved address bits Bit[7:4]: Reserved (0) Bit[3:0]: Number of interleaved address bits	–	01h
114	Interleaved operation attributes Bit[7:5]: Reserved (0) Bit 4: 1 = supports read cache Bit 3: Address restrictions for cache operations Bit 2: 1 = supports program cache Bit 1: 1 = no block address restrictions Bit 0: Overlapped/concurrent interleaving support	–	1Eh
115–127	Reserved (0)	–	All 00h
Electrical parameters block			

Table 13: Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
128	I/O pin capacitance per chip enable	MT29F16G08ABABAWP	05h
		MT29F32G08AFABAWP	05h
		MT29F64G08AJABAWP	09h
		MT29F64G08AKABAC5	0Eh
		MT29F64G08AMABAC5	07h
		MT29F128G08AUABAC5	0Ah
		MT29F16G08ABCBBH1	05h
		MT29F32G08AECBBH1	05h
		MT29F64G08AKCBBH2	09h
		MT29F64G08AMCBBH2	05h
		MT29F128G08AUCBBH3	09h
129–130	Timing mode support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	–	1Fh, 00h
131–132	Program cache timing mode support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	–	1Fh, 00h
133–134	^{t}PROG Maximum PROGRAM PAGE time (µs)	–	F4h, 01h
135–136	^{t}BERS Maximum BLOCK ERASE time (µs)	–	ACh, 0Dh
137–138	^{t}R Maximum PAGE READ time (µs)	–	19h, 00h
139–140	^{t}CCS Minimum change column setup time (ns)	–	C8h, 00h

Table 13: Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
141–142	Source synchronous timing mode support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	MT29F16G08ABABAWP	00h, 00h
		MT29F32G08AFABAWP	
		MT29F64G08AJABAWP	
		MT29F64G08AKABAC5	
		MT29F64G08AMABAC5	
		MT29F128G08AUABAC5	
		MT29F16G08ABCBBH1	1Fh, 00h
		MT29F32G08AECBBH1	
		MT29F64G08AKCBBH2	
		MT29F64G08AMCBBH2	
		MT29F128G08AUCBBH3	
143	Source synchronous features Bit[7:3]: Reserved (0) Bit 2: 1 = devices support CLK stopped for data input Bit 1: 1 = typical capacitance values present Bit 0: 0 = use ^{t}CAD MIN value	MT29F16G08ABABAWP	00h
		MT29F32G08AFABAWP	
		MT29F64G08AJABAWP	
		MT29F64G08AKABAC5	
		MT29F64G08AMABAC5	
		MT29F128G08AUABAC5	
		MT29F16G08ABCBBH1	02h
		MT29F32G08AECBBH1	
		MT29F64G08AKCBBH2	
		MT29F64G08AMCBBH2	
		MT29F128G08AUCBBH3	
144–145	CLK input pin capacitance, typical	MT29F16G08ABABAWP	00h, 00h
		MT29F32G08AFABAWP	
		MT29F64G08AJABAWP	
		MT29F64G08AKABAC5	
		MT29F64G08AMABAC5	
		MT29F128G08AUABAC5	
		MT29F16G08ABCBBH1	24h, 00h
		MT29F32G08AECBBH1	
		MT29F64G08AKCBBH2	3Eh, 00h
		MT29F64G08AMCBBH2	1Fh, 00h
		MT29F128G08AUCBBH3	35h, 00h

Table 13: Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
146–147	I/O pin capacitance, typical	MT29F16G08ABABAWP	00h, 00h
		MT29F32G08AFABAWP	
		MT29F64G08AJABAWP	
		MT29F64G08AKABAC5	
		MT29F64G08AMABAC5	
		MT29F128G08AUABAC5	
		MT29F16G08ABCBBH1	2Dh, 00h
		MT29F32G08AECBBH1	
		MT29F64G08AKCBBH2	50h, 00h
		MT29F64G08AMCBBH2	28h, 00h
		MT29F128G08AUCBBH3	49h, 00h
148–149	Input capacitance, typical	MT29F16G08ABABAWP	00h, 00h
		MT29F32G08AFABAWP	
		MT29F64G08AJABAWP	
		MT29F64G08AKABAC5	
		MT29F64G08AMABAC5	
		MT29F128G08AUABAC5	
		MT29F16G08ABCBBH1	28h, 00h
		MT29F32G08AECBBH1	
		MT29F64G08AKCBBH2	44h, 00h
		MT29F64G08AMCBBH2	22h, 00h
		MT29F128G08AUCBBH3	35h, 00h
150	Input pin capacitance, maximum	MT29F16G08ABABAWP	0Ah
		MT29F32G08AFABAWP	07h
		MT29F64G08AJABAWP	09h
		MT29F64G08AKABAC5	0Ah
		MT29F64G08AMABAC5	05h
		MT29F128G08AUABAC5	0Ah
		MT29F16G08ABCBBH1	05h
		MT29F32G08AECBBH1	
		MT29F64G08AKCBBH2	08h
		MT29F64G08AMCBBH2	04h
		MT29F128G08AUCBBH3	07h
151	Driver strength support Bit[7:3]: Reserved (0) Bit 2: 1 = Supports overdrive (2 drive strength) Bit 1: 1 = Supports overdrive (1 drive strength) Bit 0: 1 = Supports driver strength settings	–	07h

Table 13: Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
152–153	^{t}R maximum interleaved (multi-plane) page read time (μs)	–	19h, 00h
154–163	Reserved (0)	–	All 00h
Vendor block			
164–165	Vendor-specific revision number	–	01h, 00h
166	TWO-PLANE PAGE READ support Bit[7:1]: Reserved (0) Bit 0: 1 = Support for TWO-PLANE PAGE READ	–	01h
167	Read cache support Bit[7:1]: Reserved (0) Bit 0: 0 = Does not support Micron-specific read cache function	–	00h
168	READ UNIQUE ID support Bit[7:1]: Reserved (0) Bit 0: 0 = Does not support Micron-specific READ UNIQUE ID	–	00h
169	Programmable DQ output impedance support Bit[7:1]: Reserved (0) Bit 0: 0 = No support for programmable DQ output impedance by B8h command	–	00h
170	Number of programmable DQ output impedance settings Bit[7:3]: Reserved (0) Bit [2:0] = Number of programmable DQ output impedance settings	–	04h
171	Programmable DQ output impedance feature address Bit[7:0] = Programmable DQ output impedance feature address	–	10h
172	Programmable R/B# pull-down strength support Bit[7:1]: Reserved (0) Bit 0: 1 = Support programmable R/B# pull-down strength	–	01h
173	Programmable R/B# pull-down strength feature address Bit[7:0] = Feature address used with programmable R/B# pull-down strength	–	81h
174	Number of programmable R/B# pull-down strength settings Bit[7:3]: Reserved (0) Bit[2:0] = Number of programmable R/B# pull-down strength settings	–	04h

Table 13: Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
175	OTP mode support Bit[7:2]: Reserved (0) Bit 1: 1 = Supports Get/Set Features command set Bit 0: 0 = Does not support A5h/A0h/AFh OTP command set	–	02h
176	OTP page start Bit[7:0] = Page where OTP page space begins	–	02h
177	OTP DATA PROTECT address Bit[7:0] = Page address to use when issuing OTP DATA PROTECT command	–	01h
178	Number of OTP pages Bit[15:5]: Reserved (0) Bit[4:0] = Number of OTP pages	–	1Eh
179	OTP Feature Address	–	90h
180–252	Reserved (0)	–	All 00h
253	Parameter page revision	–	03h
254–255	Integrity CRC	MT29F16G08ABABAWP	B4h, ADh
		MT29F32G08AFABAWP	BBh, A8h
		MT29F64G08AJABAWP	F7h, D2h
		MT29F64G08AKABAC5	20h, 7Dh
		MT29F64G08AMABAC5	2Ch, 10h
		MT29F128G08AUABAC5	AEh, E7h
		MT29F16G08ABCBBH1	D9h, AAh
		MT29F32G08AECBBH1	53h, 74h
		MT29F64G08AKCBBH2	3Fh, CCh
		MT29F64G08AMCBBH2	30h, 75h
		MT29F128G08AUCBBH3	EBh, C5h
Redundant parameter pages			
256–511	Value of bytes 0–255	–	See bytes 0–255
512–767	Value of bytes 0–255	–	See bytes 0–255
768–4319	Reserved (FFh)	–	All FFh

READ UNIQUE ID (EDh)

The READ UNIQUE ID (EDh) command is used to read a unique identifier programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

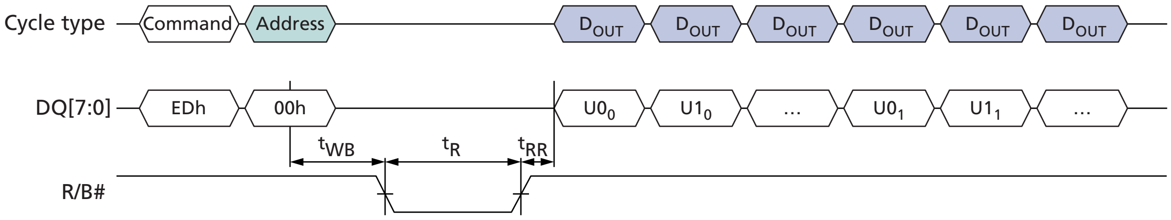
Writing EDh to the command register puts the target in read unique ID mode. The target stays in this mode until another valid command is issued.

When the EDh command is followed by a 00h address cycle, the target goes busy for ${}^{t}R$. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode.

After ${}^{t}R$ completes, the host enables data output mode to read the unique ID. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, two data bytes are output, one byte for each rising or falling edge of DQS.

Sixteen copies of the unique ID data are stored in the device. Each copy is 32 bytes. The first 16 bytes of a 32-byte copy are unique data, and the second 16 bytes are the complement of the first 16 bytes. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, then that copy of the unique ID data is correct. In the event that a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data. If desired, the CHANGE READ COLUMN (05h-E0h) command can be used to change the data output location. Use of the CHANGE READ COLUMN ENHANCED (06h-E0h) command is prohibited.

Figure 44: READ UNIQUE ID (EDh) Operation



Configuration Operations

The SET FEATURES (EFh) and GET FEATURES (EEh) commands are used to modify the target's default power-on behavior. These commands use a one-byte feature address to determine which subfeature parameters will be read or modified. Each feature address (in the 00h to FFh range) is defined in Table 14. The SET FEATURES (EFh) command writes subfeature parameters (P1-P4) to the specified feature address. The GET FEATURES command reads the subfeature parameters (P1-P4) at the specified feature address.

Unless otherwise specifed, the values of the feature addresses do not change when RESET (FFh, FCh) is issued by the host.

Table 14: Feature Address Definitions

Feature Address	Definition
00h	Reserved
01h	Timing mode
02h–0Fh	Reserved
10h	Programmable output drive strength
11h–7Fh	Reserved
80h	Programmable output drive strength
81h	Programmable RB# pull-down strength
82h–8Fh	Reserved
90h	Array operation mode
91h–FFh	Reserved

SET FEATURES (EFh)

The SET FEATURES (EFh) command writes the subfeature parameters (P1-P4) to the specified feature address to enable or disable target-specific features. This command is accepted by the target only when all die (LUNs) on the target are idle.

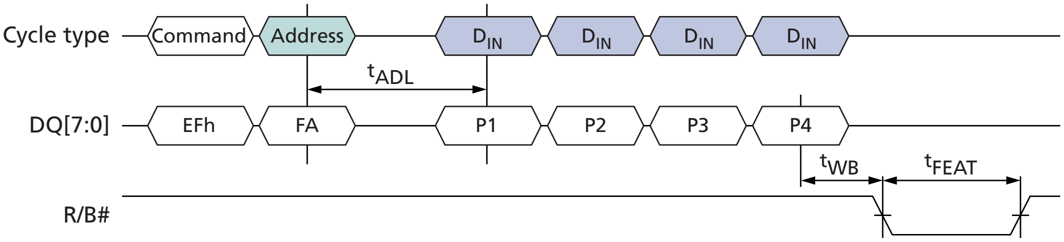
Writing EFh to the command register puts the target in the set features mode. The target stays in this mode until another command is issued.

The EFh command is followed by a valid feature address. The host waits for ^{t}ADL before the subfeature parameters are input. When the asynchronous interface is active, one subfeature parameter is latched per rising edge of WE#. When the synchronous interface is active, one subfeature parameter is latched per rising edge of DQS. The data on the falling edge of DQS should be identical to the subfeature parameter input on the previous rising edge of DQS. The device is not required to wait for the repeated data byte before beginning internal actions.

After all four subfeature parameters are input, the target goes busy for ^{t}FEAT. The READ STATUS (70h) command can be used to monitor for command completion.

Feature address 01h (timing mode) operation is unique. If SET FEATURES is used to modify the interface type, the target will be busy for ^{t}ITC.

Figure 45: SET FEATURES (EFh) Operation



GET FEATURES (EEh)

The GET FEATURES (EEh) command reads the subfeature parameters (P1-P4) from the specified feature address. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EEh to the command register puts the target in get features mode. The target stays in this mode until another valid command is issued.

When the EEh command is followed by a feature address, the target goes busy for ^{t}FEAT. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. During and prior to data output, use of the READ STATUS ENHANCED (78h) command is prohibited.

After ^{t}FEAT completes, the host enables data output mode to read the subfeature parameters. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, one subfeature parameter is output per DQS toggle on rising or falling edge of DQS.

Figure 46: GET FEATURES (EEh) Operation

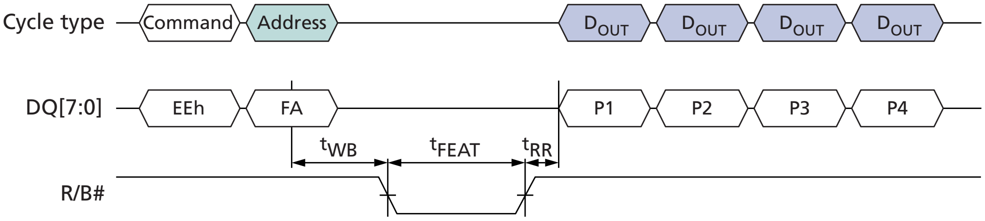


Table 15: Feature Address 01h: Timing Mode

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Timing mode	Mode 0 (default)					0	0	0	0	x0h	1, 2
	Mode 1					0	0	0	1	x1h	
	Mode 2					0	0	1	0	x2h	
	Mode 3					0	0	1	1	x3h	
	Mode 4					0	1	0	0	x4h	
	Mode 5					0	1	0	1	x5h	
Data interface	Asynchronous (default)			0	0					0xh	1
	Synchronous DDR			0	1					1xh	
	Reserved			1	x					2xh	
Reserved		0	0							00b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes:
1. Asynchronous timing mode 0 is the default, power-on value.
2. If the synchronous interface is active, a RESET (FFh) command will change the timing mode and data interface bits of feature address 01h to their default values. If the asynchronous interface is active, a RESET (FFh) command will not change the values of the timing mode or data interface bits to their default valued.

Table 16: Feature Addresses 10h and 80h: Programmable Output Drive Strength

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Output drive strength	Overdrive 2							0	0	00h	1
	Overdrive 1							0	1	01h	
	Nominal (default)							1	0	02h	
	Underdrive							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	

Table 16: Feature Addresses 10h and 80h: Programmable Output Drive Strength (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. See Output Drive Impedance for details.

Table 17: Feature Addresses 81h: Programmable R/B# Pull-Down Strength

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
R/B# pull-down strength	Full (default)							0	0	00h	1
	Three-quarter							0	1	01h	
	One-half							1	0	02h	
	One-quarter							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. This feature address is used to change the default R/B# pull-down strength. Its strength should be selected based on the expected loading of R/B#. Full strength is the default, power-on value.

Table 18: Feature Addresses 90h: Array Operation Mode

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Array Operation Mode	Normal (default)								0	00h	
	OTP Block								1	01h	1
Reserved		0	0	0	0	0	0	0		00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											

Table 18: Feature Addresses 90h: Array Operation Mode (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Reserved		0	0	0	0	0	0	0	0	00h	

Notes:
1. See One-Time Programmable (OTP) Operations for details.
2. A RESET (FFh) command will cause the bits of the array operation mode to change to their default values.

Status Operations

Each die (LUN) provides its status independently of other die (LUNs) on the same target through its 8-bit status register.

After the READ STATUS (70h) or READ STATUS ENHANCED (78h) command is issued, status register output is enabled. The contents of the status register are returned on DQ[7:0] for each data output request.

When the asynchronous interface is active and status register output is enabled, changes in the status register are seen on DQ[7:0] as long as CE# and RE# are LOW; it is not necessary to toggle RE# to see the status register update.

When the synchronous interface is active and status register output is enabled, changes in the status register are seen on DQ[7:0] as long as CE# and W/R# are LOW and ALE and CLE are HIGH. DQS also toggles (with ^{t}DQSCK delay) while ALE and CLE are captured HIGH. If status register output is enabled and CE# and W/R# are LOW and ALE and CLE are also captured LOW, changes in the status register are still seen asynchronously on DQ[7:0] but DQS does not toggle.

While monitoring the status register to determine when a data transfer from the Flash array to the data register (^{t}R) is complete, the host must issue the READ MODE (00h) command to disable the status register and enable data output (see READ MODE (00h) (page 89)).

The READ STATUS (70h) command returns the status of the most recently selected die (LUN). To prevent data contention during or following an interleaved die (multi-LUN) operation, the host must enable only one die (LUN) for status output by using the READ STATUS ENHANCED (78h) command (see Interleaved Die (Multi-LUN) Operations (page 113)).

Table 19: Status Register Definition

SR Bit	Definition	Independent per Plane[1]	Description
7	WP#	–	Write Protect: 0 = Protected 1 = Not protected In the normal array mode, this bit indicates the value of the WP# signal. In OTP mode this bit is set to 0 if a PROGRAM OTP PAGE operation is attempted and the OTP area is protected.
6	RDY	–	Ready/Busy I/O: 0 = Busy 1 = Ready This bit indicates that the selected die (LUN) is not available to accept new commands, address, or data I/O cycles with the exception of RESET (FFh), SYNCHRONOUS RESET (FCh), READ STATUS (70h), and READ STATUS ENHANCED (78h). This bit applies only to the selected die (LUN).

Table 19: Status Register Definition (Continued)

SR Bit	Definition	Independent per Plane[1]	Description
5	ARDY	–	Ready/Busy Array: 0 = Busy 1 = Ready This bit goes LOW (busy) when an array operation is occurring on any plane of the selected die (LUN). It goes HIGH when all array operations on the selected die (LUN) finish. This bit applies only to the selected die (LUN).
4	–	–	Reserved (0)
3	–	–	Reserved (0)
2	–	–	Reserved (0)
1	FAILC	Yes	Pass/Fail (N–1): 0 = Pass 1 = Fail This bit is set if the previous operation on the selected die (LUN) failed. This bit is valid only when RDY (SR bit 6) is 1. It applies to PROGRAM-, and COPYBACK PROGRAM-series operations (80h-10h, 80h-15h, 85h-10h). This bit is not valid following an ERASE-series or READ-series operation.
0	FAIL	Yes	Pass/Fail (N): 0 = Pass 1 = Fail This bit is set if the most recently finished operation on the selected die (LUN) failed. This bit is valid only when ARDY (SR bit 5) is 1. It applies to PROGRAM-, ERASE-, and COPYBACK PROGRAM-series operations (80h-10h, 80h-15h, 60h-D0h, 85h-10h). This bit is not valid following a READ-series operation.

Note: 1. After a multi-plane operation begins, the FAILC and FAIL bits are ORed together for the active planes when the READ STATUS (70h) command is issued. After the READ STATUS ENHANCED (78h) command is issued, the FAILC and FAIL bits reflect the status of the plane selected.

READ STATUS (70h)

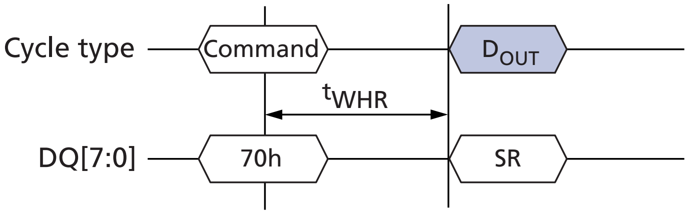
The READ STATUS (70h) command returns the status of the last-selected die (LUN) on a target. This command is accepted by the last-selected die (LUN) even when it is busy (RDY = 0).

If there is only one die (LUN) per target, the READ STATUS (70h) command can be used to return status following any NAND command.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select the die (LUN) that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as two or more die (LUNs) could respond until the next operation is issued. The READ STATUS (70h) command can be used following all single die (LUN) operations.

If following a multi-plane operation, regardless of the number of LUNs per target, the READ STATUS (70h) command indicates an error occurred (FAIL = 1), use the READ STATUS ENHANCED (78h) command—once for each plane—to determine which plane operation failed.

Figure 47: READ STATUS (70h) Operation



READ STATUS ENHANCED (78h)

The READ STATUS ENHANCED (78h) command returns the status of the addressed die (LUN) on a target even when it is busy (RDY = 0). This command is accepted by all die (LUNs), even when they are BUSY (RDY = 0).

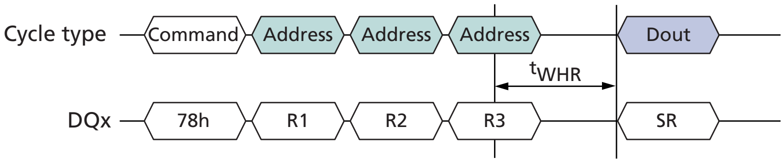
Writing 78h to the command register, followed by three row address cycles containing the page, block, and LUN addresses, puts the selected die (LUN) into read status mode. The selected die (LUN) stays in this mode until another valid command is issued. Die (LUNs) that are not addressed are deselected to avoid bus contention.

The selected LUN's status is returned when the host requests data output. The RDY and ARDY bits of the status register are shared for all of the planes of the selected die (LUN). The FAILC and FAIL bits are specific to the plane specified in the row address.

The READ STATUS ENHANCED (78h) command also enables the selected die (LUN) for data output. To begin data output following a READ-series operation after the selected die (LUN) is ready (RDY = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the cache register that will output data, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command after the die (LUN) is ready (see CHANGE READ COLUMN ENHANCED (06h-E0h)).

Use of the READ STATUS ENHANCED (78h) command is prohibited during the power-on RESET (FFh) command and when OTP mode is enabled. It is also prohibited following some of the other reset, identification, and configuration operations. See individual operations for specific details.

Figure 48: READ STATUS ENHANCED (78h) Operation



Column Address Operations

The column address operations affect how data is input to and output from the cache registers within the selected die (LUNs). These features provide host flexibility for managing data, especially when the host internal buffer is smaller than the number of data bytes or words in the cache register.

When the asynchronous interface is active, column address operations can address any byte in the selected cache register.

When the synchronous interface is active, column address operations are aligned to word boundaries (CA0 is forced to 0), because as data is transferred on DQ[7:0] in two-byte units.

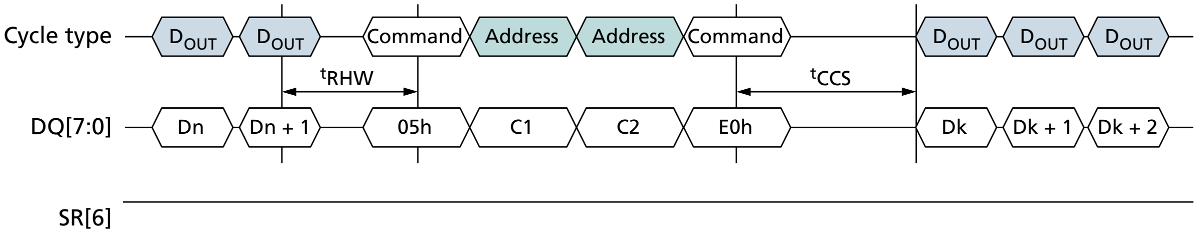
CHANGE READ COLUMN (05h-E0h)

The CHANGE READ COLUMN (05h-E0h) command changes the column address of the selected cache register and enables data output from the last selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during CACHE READ operations (RDY = 1; ARDY = 0).

Writing 05h to the command register, followed by two column address cycles containing the column address, followed by the E0h command, puts the selected die (LUN) into data output mode. After the E0h command cycle is issued, the host must wait at least ^{t}CCS before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be issued prior to issuing the CHANGE READ COLUMN (05h-E0h). In this situation, using the CHANGE READ COLUMN (05h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention, as two or more die (LUNs) could output data.

Figure 49: CHANGE READ COLUMN (05h-E0h) Operation



CHANGE READ COLUMN ENHANCED (06h-E0h)

The CHANGE READ COLUMN ENHANCED (06h-E0h) command enables data output on the addressed die's (LUN's) cache register at the specified column address. This command is accepted by a die (LUN) when it is ready (RDY = 1; ARDY = 1).

Writing 06h to the command register, followed by two column address cycles and three row address cycles, followed by E0h, enables data output mode on the address LUN's cache register at the specified column address. Only the column, plane and LUN addresses are valid; the page and block addresses are ignored. After the E0h command cycle is issued, the host must wait at least ^{t}CCS before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

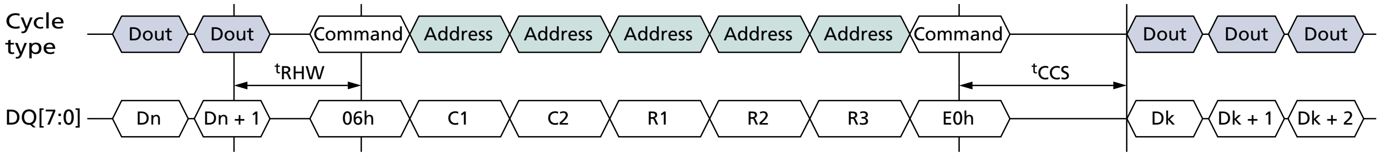
Following a multi-plane read page operation, the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select the cache register to be enabled for data output. After data output is complete on the selected plane, the command can be issued again to begin data output on another plane.

In devices with more than one die (LUN) per target, after all of the die (LUNs) on the target are ready (RDY = 1), the CHANGE READ COLUMN ENHANCED (06h-E0h) command can be used following an interleaved die (multi-LUN) read operation. Die (LUNs) that are not addressed are deselected to avoid bus contention.

In devices with more than one die (LUN) per target, during interleaved die (multi-LUN) operations where more than one or more die (LUNs) are busy (RDY = 1; ARDY = 0 or RDY = 0; ARDY = 0), the READ STATUS ENHANCED (78h) command must be issued to the die (LUN) to be selected prior to issuing the CHANGE READ COLUMN ENHANCED (06h-E0h). In this situation, using the CHANGE READ COLUMN ENHANCED (06h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention, as two or more die (LUNs) could output data.

If there is a need to update the column address without selecting a new cache register or LUN, the CHANGE READ COLUMN (05h-E0h) command can be used instead.

Figure 50: CHANGE READ COLUMN ENHANCED (06h-E0h) Operation



CHANGE WRITE COLUMN (85h)

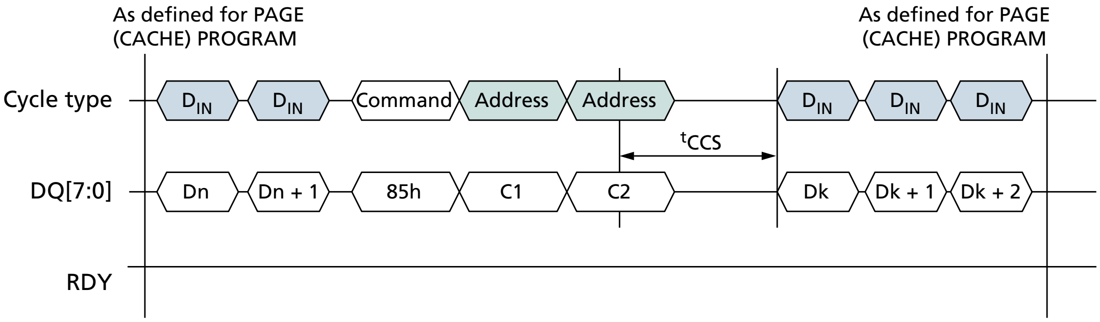
The CHANGE WRITE COLUMN (85h) command changes the column address of the selected cache register and enables data input on the last-selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during cache program operations (RDY = 1; ARDY = 0).

Writing 85h to the command register, followed by two column address cycles containing the column address, puts the selected die (LUN) into data input mode. After the second address cycle is issued, the host must wait at least ^{t}CCS before inputting data. The selected die (LUN) stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE WRITE COLUMN (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE CACHE (80h-15h), COPYBACK PROGRAM (85h-10h), and COPYBACK PROGRAM MULTI-PLANE (85h-11h).

In devices that have more than one die (LUN) per target, the CHANGE WRITE COLUMN (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

Figure 51: CHANGE WRITE COLUMN (85h) Operation



CHANGE ROW ADDRESS (85h)

The CHANGE ROW ADDRESS (85h) command changes the row address (block and page) where the cache register contents will be programmed in the NAND Flash array. It also changes the column address of the selected cache register and enables data input on the specified die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during cache programming operations (RDY = 1; ARDY = 0).

Write 85h to the command register. Then write two column address cycles and three row address cycles. This updates the page and block destination of the selected plane for the addressed LUN and puts the cache register into data input mode. After the fifth address cycle is issued the host must wait at least ^{t}CCS before inputting data. The selected LUN stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE ROW ADDRESS (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE CACHE (80h-15h), COPYBACK PROGRAM (85h-10h), and COPYBACK PROGRAM MULTI-PLANE (85h-11h). When used with these commands, the LUN address and plane select bits are required to be identical to the LUN address and plane select bits originally specified.

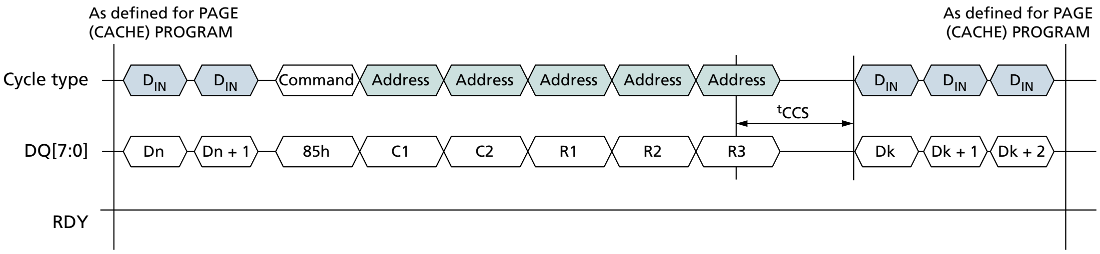
The CHANGE ROW ADDRESS (85h) command enables the host to modify the original page and block address for the data in the cache register to a new page and block address.

In devices that have more than one die (LUN) per target, the CHANGE ROW ADDRESS (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

The CHANGE ROW ADDRESS (85h) command can be used with the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) commands to read and modify cache register contents in small sections prior to programming cache register contents to the NAND Flash array. This capability can reduce the amount of buffer memory used in the host controller.

To modify the cache register contents in small sections, first issue a PAGE READ (00h-30h) or COPYBACK READ (00h-35h) operation. When data output is enabled, the host can output a portion of the cache register contents. To modify the cache register contents, issue the 85h command, the column and row addresses, and input the new data. The host can re-enable data output by issuing the 11h command, waiting ^{t}DBSY, and then issuing the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) command. It is possible toggle between data output and data input multiple times. After the final CHANGE ROW ADDRESS (85h) operation is complete, issue the 10h command to program the cache register to the NAND Flash array.

Figure 52: CHANGE ROW ADDRESS (85h) Operation



Read Operations

Read operations are used to copy data from the NAND Flash array of one or more of the planes to their respective cache registers and to enable data output from the cache registers to the host through the DQ bus.

Read Operations

The READ PAGE (00h-30h) command, when issued by itself, reads one page from the NAND Flash array to its cache register and enables data output for that cache register.

During data output the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h) and CHANGE ROW ADDRESS (85h).

Read Cache Operations

To increase data throughput, the READ PAGE CACHE-series (31h, 00h-31h) commands can be used to output data from the cache register while concurrently copying a page from the NAND Flash array to the data register.

To begin a read page cache sequence, begin by reading a page from the NAND Flash array to its corresponding cache register using the READ PAGE (00h-30h) command. R/B# goes LOW during ^{t}R and the selected die (LUN) is busy (RDY = 0, ARDY = 0). After ^{t}R (R/B# is HIGH and RDY = 1, ARDY = 1), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h)—copies the next sequential page from the NAND Flash array to the data register
- READ PAGE CACHE RANDOM (00h-31h)—copies the page specified in this command from the NAND Flash array (any plane) to its corresponding data register

After the READ PAGE CACHE-series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the next page begins copying data from the array to the data register. After ^{t}RCBSY, R/B# goes HIGH and the die's (LUN's) status register bits indicate the device is busy with a cache operation (RDY = 1, ARDY = 0). The cache register becomes available and the page requested in the READ PAGE CACHE operation is transferred to the data register. At this point, data can be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data output by the die (LUN).

After outputting the desired number of bytes from the cache register, either an additional READ PAGE CACHE-series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the data register is copied into the cache register. After ^{t}RCBSY, R/B# goes HIGH and RDY = 1 and ARDY = 1, indicating that the cache register is available and that the die (LUN) is ready. Data can then be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output.

For READ PAGE CACHE-series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, ^{t}RCBSY, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and RESET (FFh, FCh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE-series (31h, 00h-31h) operations are status operations (70h, 78h), READ MODE (00h), READ PAGE CACHE-series (31h, 00h-31h), CHANGE READ COLUMN (05h-E0h), and RESET (FFh, FCh).

Multi-Plane Read Operations

Multi-plane read page operations improve data throughput by copying data from more than one plane simultaneously to the specified cache registers. This is done by prepending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the READ PAGE (00h-30h) command.

When the die (LUN) is ready, the CHANGE READ COLUMN ENHANCED (06h-E0h) command determines which plane outputs data. During data output, the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h) and CHANGE ROW ADDRESS (85h). See Multi-Plane Operations for details.

Multi-Plane Read Cache Operations

Multi-plane read cache operations can be used to output data from more than one cache register while concurrently copying one or more pages from the NAND Flash array to the data register. This is done by prepending READ PAGE MULTI-PLANE (00h-32h) commands in front of the PAGE READ CACHE RANDOM (00h-31h) command.

To begin a multi-plane read page cache sequence, begin by issuing a MULTI-PLANE READ PAGE operation using the READ PAGE MULTI-PLANE (00h-32h) and READ PAGE (00h-30h) commands. R/B# goes LOW during ^{t}R and the selected die (LUN) is busy (RDY = 0, ARDY = 0). After ^{t}R (R/B# is HIGH and RDY = 1, ARDY = 1), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h)—copies the next sequential page from the previously addressed planes from the NAND Flash array to the data registers.
- READ PAGE MULTI-PLANE (00h-32h) commands, if desired, followed by the READ PAGE CACHE RANDOM (00h-31h) command—copies the pages specified from the NAND Flash array to the corresponding data registers.

After the READ PAGE CACHE-series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the next pages begin copying data from the array to the data registers. After ^{t}RCBSY, R/B# goes HIGH and the LUN’s status register bits indicate the device is busy with a cache operation (RDY = 1, ARDY = 0). The cache registers become available and the pages requested in the READ PAGE CACHE operation are transferred to the data registers. Issue the CHANGE READ COLUMN ENHANCED (06h-E0h) command to determine which cache register will output data. After data is output, the CHANGE READ COLUMN ENHANCED (06h-E0h) command can be used to output data from other cache registers. After a cache register has been selected, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data output.

After outputting data from the cache registers, either an additional MULTI-PLANE READ CACHE-series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the data registers are copied into the cache registers. After ^{t}RCBSY, R/B# goes HIGH and RDY = 1 and ARDY = 1, indicating that the cache registers are available and that the die (LUN) is ready. Issue the

CHANGE READ COLUMN ENHANCED (06h-E0h) command to determine which cache register will output data. After data is output, the CHANGE READ COLUMN ENHANCED (06h-E0h) command can be used to output data from other cache registers. After a cache register has been selected, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data output.

For READ PAGE CACHE-series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, ^{t}RCBSY, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and RESET (FFh, FCh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE-series (31h, 00h-31h) operations are status operations (70h, 78h), READ MODE (00h), multi-plane read cache-series (31h, 00h-32h, 00h-31h), CHANGE READ COLUMN (05h-E0h, 06h-E0h), and RESET (FFh, FCh).

See Multi-Plane Operations for additional multi-plane addressing requirements.

READ MODE (00h)

The READ MODE (00h) command disables status output and enables data output for the last-selected die (LUN) and cache register after a READ operation (00h-30h, 00h-35h) has been monitored with a status operation (70h, 78h). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 3Fh, 00h-31h) operations (RDY = 1 and ARDY = 0).

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to issuing the READ MODE (00h) command. This prevents bus contention.

READ PAGE (00h-30h)

The READ PAGE (00h–30h) command copies a page from the NAND Flash array to its respective cache register and enables data output. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To read a page from the NAND Flash array, write the 00h command to the command register, the write five address cycles to the address registers, and conclude with the 30h command. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^tR as data is transferred.

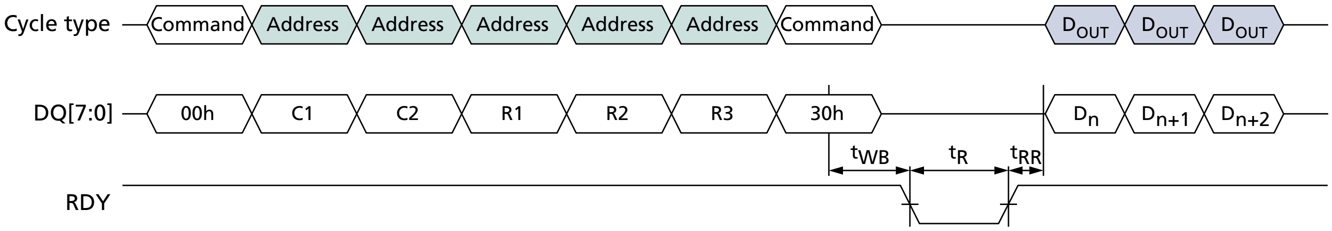
To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. If the status operations are used to monitor the LUN's status, when the die (LUN) is ready (RDY = 1, ARDY = 1), the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, output begins at the column address specified.

During data output the CHANGE READ COLUMN (05h-E0h) command can be issued.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to the issue of the READ MODE (00h) command. This prevents bus contention.

The READ PAGE (00h-30h) command is used as the final command of a multi-plane read operation. It is preceded by one or more READ PAGE MULTI-PLANE (00h-32h) commands. Data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the die (LUN) is ready (RDY = 1, ARDY = 1), data output is enabled for the cache register linked to the last even plane addressed. When the host requests data output, output begins at the column address last specified in the READ PAGE (00h-30h) command. The CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to enable data output in the other cache registers. See Multi-Plane Operations for additional multi-plane addressing requirements.

Figure 53: READ PAGE (00h-30h) Operation



READ PAGE CACHE SEQUENTIAL (31h)

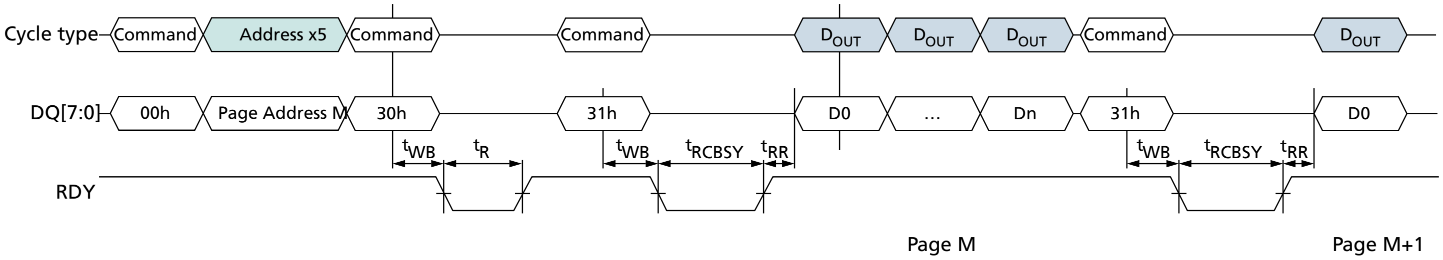
The READ PAGE CACHE SEQUENTIAL (31h) command reads the next sequential page within a block into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue this command, write 31h to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

The READ PAGE CACHE SEQUENTIAL (31h) command can be used to cross block boundaries. If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after the last page of a block is read into the data register, the next page read will be the next logical block in the plane which the 31h command was issued. Do not issue the READ PAGE CACHE SEQUENTIAL (31h) to cross die (LUN) boundaries. Instead, issue the READ PAGE CACHE LAST (3Fh) command.

If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after a MULTI-PLANE READ PAGE operation (00h-32h, 00h-30h), the next sequential pages are read into the data registers while the previous pages can be output from the cache registers. After the die (LUN) is ready (RDY = 1, ARDY = 0), the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select which cache register outputs data.

Figure 54: READ PAGE CACHE SEQUENTIAL (31h) Operation



READ PAGE CACHE RANDOM (00h-31h)

The READ PAGE CACHE RANDOM (00h-31h) command reads the specified block and page into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

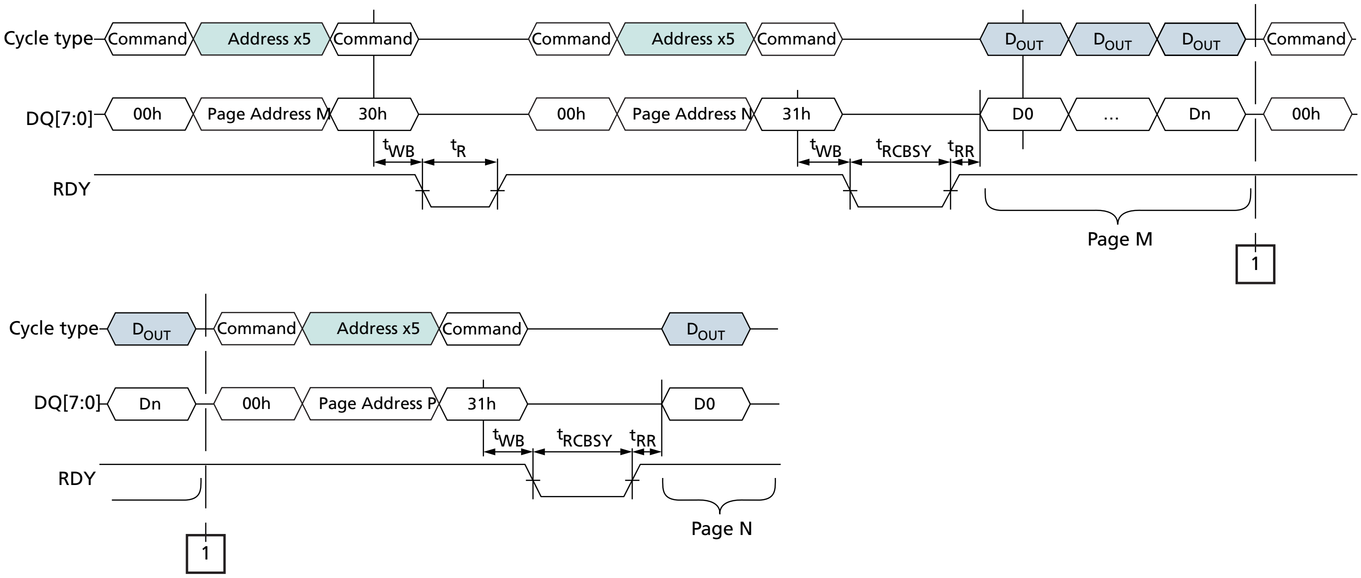
To issue this command, write 00h to the command register, then write five address cycles to the address register, and conclude by writing 31h to the command register. The column address in the address specified is ignored. The die (LUN) address must match the same die (LUN) address as the previous READ PAGE (00h-30h) command or, if applicable, the previous READ PAGE CACHE RANDOM (00h-31h) command. There is no restriction on the plane address.

After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command followed by the READ MODE (00h) command must be used to select only one die (LUN) and prevent bus contention.

If a MULTI-PLANE CACHE RANDOM (00h-32h, 00h-31h) command is issued after a MULTI-PLANE READ PAGE operation (00h-32h, 00h-30h), then the addressed pages are read into the data registers while the previous pages can be output from the cache registers. After the die (LUN) is ready (RDY = 1, ARDY = 0), the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select which cache register outputs data.

Figure 55: READ PAGE CACHE RANDOM (00h-31h) Operation



READ PAGE CACHE LAST (3Fh)

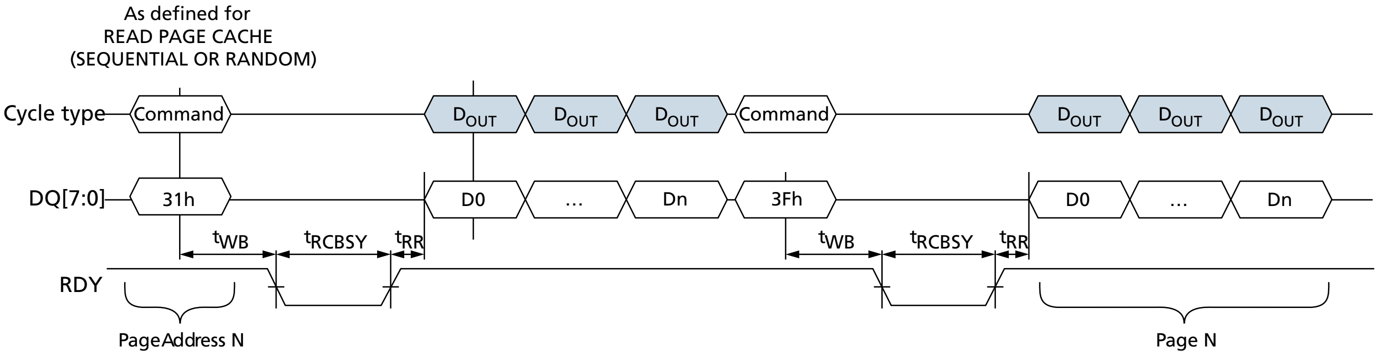
The READ PAGE CACHE LAST (3Fh) command ends the read page cache sequence and copies a page from the data register to the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue the READ PAGE CACHE LAST (3Fh) command, write 3Fh to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and the die (LUN) is ready (RDY = 1, ARDY = 1). At this point, data can be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one LUN per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command followed by the READ MODE (00h) command must be used to select only one die (LUN) and prevent bus contention.

If the READ PAGE CACHE LAST (3Fh) command is issued after a MULTI-PLANE READ PAGE CACHE operation (31h; 00h-32h, 00h-30h), the die (LUN) goes busy until the pages are copied from the data registers to the cache registers. After the die (LUN) is ready (RDY = 1, ARDY = 1), the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select which cache register outputs data.

Figure 56: READ PAGE CACHE LAST (3Fh) Operation



READ PAGE MULTI-PLANE (00h-32h)

The READ PAGE MULTI-PLANE (00h-32h) command queues a plane to transfer data from the NAND flash array to its cache register. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for data transfer. The READ PAGE (00h-30h) command is issued to select the final plane and to begin the read operation for all previously queued planes. All queued planes will transfer data from the NAND Flash array to their cache registers.

To issue the READ PAGE MULTI-PLANE (00h-32h) command, write 00h to the command register, then write five address cycles to the address register, and conclude by writing 32h to the command register. The column address in the address specified is ignored.

After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}DBSY. After ^{t}DBSY, R/B# goes HIGH and the die (LUN) is ready (RDY = 1, ARDY = 1). At this point, the die (LUN) and block are queued for data transfer from the array to the cache register for the addressed plane. During ^{t}DBSY, the only valid commands are status operations (70h, 78h) and reset commands (FFh, FCh). Following ^{t}DBSY, to continue the MULTI-PLANE READ operation, the only valid commands are status operations (70h, 78h), READ PAGE MULTI-PLANE (00h-32h), READ PAGE (00h-30h), and READ PAGE CACHE RANDOM (00h-31h).

Additional READ PAGE MULTI-PLANE (00h-32h) commands can be issued to queue additional planes for data transfer.

If the READ PAGE (00h-30h) command is used as the final command of a MULTI-PLANE READ operation, data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the die (LUN) is ready (RDY = 1, ARDY = 1), data output is enabled for the cache register linked to the last even plane addressed. When the host requests data output, it begins at the column address specified in the READ PAGE (00h-30h) command. To enable data output in the other cache registers, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command. Additionally, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

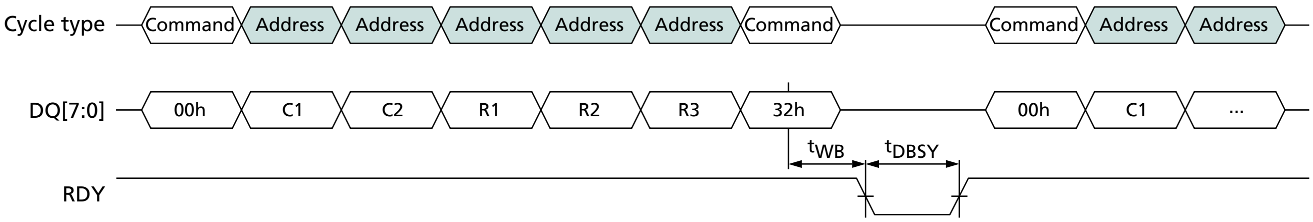
If the READ PAGE CACHE SEQUENTIAL (31h) is used as the final command of a MULTI-PLANE READ CACHE operation, data is copied from the previously read operation from each plane to each cache register and then data is transferred from the NAND Flash array for all previously addressed planes to their respective data registers. When the die (LUN) is ready (RDY = 1, ARDY = 0), data output is enabled. The CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to determine which cache register outputs data first. To enable data output in the other cache registers, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command. Additionally, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

If the READ PAGE CACHE RANDOM (00h-31h) command is used as the final command of a MULTI-PLANE READ CACHE operation, data is copied from the previously read operation from the data register to the cache register and then data is transferred from the NAND Flash array for all of the addressed planes to their respective data registers. When the die (LUN) is ready (RDY = 1, ARDY = 0), data output is enabled. The CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to determine which cache register outputs data first. To enable data output in the other cache registers, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command. Additionally, the CHANGE READ

COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

See Multi-Plane Operations for additional multi-plane addressing requirements.

Figure 57: READ PAGE MULTI-PLANE (00h-32h) Operation



Program Operations

Program operations are used to move data from the cache or data registers to the NAND array of one or more planes. During a program operation the contents of the cache and/or data registers are modified by the internal control logic.

Within a block, pages must be programmed sequentially from the least significant page address to the most significant page address (i.e. 0, 1, 2, 3, …). Programming pages out of order within a block is prohibited.

Program Operations

The PROGRAM PAGE (80h-10h) command, when not preceded by the PROGRAM PAGE MULTI-PLANE (80h-11h) command, programs one page from the cache register to the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that the operation has completed successfully.

Program Cache Operations

The PROGRAM PAGE CACHE (80h-15h) command can be used to improve program operation system performance. When this command is issued, the die (LUN) goes busy (RDY = 0, ARDY = 0) while the cache register contents are copied to the data register, and the die (LUN) is busy with a program cache operation (RDY = 1, ARDY = 0). While the contents of the data register are moved to the NAND Flash array, the cache register is available for an additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) command.

For PROGRAM PAGE CACHE-series (80h-15h) operations, during the die (LUN) busy times, ^{t}CBSY and ^{t}LPROG, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and reset (FFh, FCh). When RDY = 1 and ARDY = 0, the only valid commands during PROGRAM PAGE CACHE-series (80h-15h) operations are status operations (70h, 78h), PROGRAM PAGE CACHE (80h-15h), PROGRAM PAGE (80h-10h), CHANGE WRITE COLUMN (85h), CHANGE ROW ADDRESS (85h), and reset (FFh, FCh).

Multi-Plane Program Operations

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can be used to improve program operation system performance by enabling multiple pages to be moved from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands in front of the PROGRAM PAGE (80h-10h) command. See Multi-Plane Operations for details.

Multi-Plane Program Cache Operations

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can be used to improve program cache operation system performance by enabling multiple pages to be moved from the cache registers to the data registers and, while the pages are being transferred from the data registers to different planes of the NAND Flash array, free the cache registers to receive data input from the host. This is done by prepending one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands in front of the PROGRAM PAGE CACHE (80h-15h) command. See Multi-Plane Operations for details.

PROGRAM PAGE (80h-10h)

The PROGRAM PAGE (80h-10h) command enables the host to input data to a cache register, and moves the data from the cache register to the specified block and page address in the array of the selected die (LUN). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) when it is busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

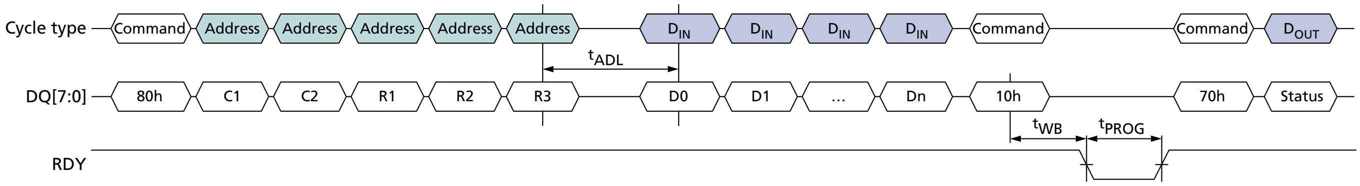
To input a page to the cache register and move it to the NAND array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write five address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 10h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}PROG as data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) may be used. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The PROGRAM PAGE (80h-10h) command is used as the final command of a multi-plane program operation. It is preceded by one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands. Data is transferred from the cache registers for all of the addressed planes to the NAND array. The host should check the status of the operation by using the status operations (70h, 78h). See Multi-Plane Operations for multi-plane addressing requirements.

Figure 58: PROGRAM PAGE (80h-10h) Operation



PROGRAM PAGE CACHE (80h-15h)

The PROGRAM PAGE CACHE (80h-15h) command enables the host to input data to a cache register; copies the data from the cache register to the data register; then moves the data register contents to the specified block and page address in the array of the selected die (LUN). After the data is copied to the data register, the cache register is available for additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) commands. The PROGRAM PAGE CACHE (80h-15h) command is accepted by the die (LUN) when it is ready (RDY =1, ARDY = 1). It is also accepted by the die (LUN) when busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

To input a page to the cache register to move it to the NAND array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write five address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 15h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}CBSY to allow the data register to become available from a previous program cache operation, to copy data from the cache register to the data register, and then to begin moving the data register contents to the specified page and block address.

To determine the progress of ^{t}CBSY, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. When the LUN’s status shows that it is busy with a PROGRAM CACHE operation (RDY = 1, ARDY = 0), the host should check the status of the FAILC bit to see if a previous cache operation was successful.

If, after ^{t}CBSY, the host wants to wait for the program cache operation to complete, without issuing the PROGRAM PAGE (80h-10h) command, the host should monitor ARDY until it is 1. The host should then check the status of the FAIL and FAILC bits.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The PROGRAM PAGE CACHE (80h-15h) command is used as the final command of a multi-plane program cache operation. It is preceded by one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands. Data for all of the addressed planes is transferred from the cache registers to the corresponding data registers, then moved to the NAND Flash array. The host should check the status of the operation by using the status operations (70h, 78h). See Multi-Plane Operations for multi-plane addressing requirements.

Figure 59: PROGRAM PAGE CACHE (80h–15h) Operation (Start)

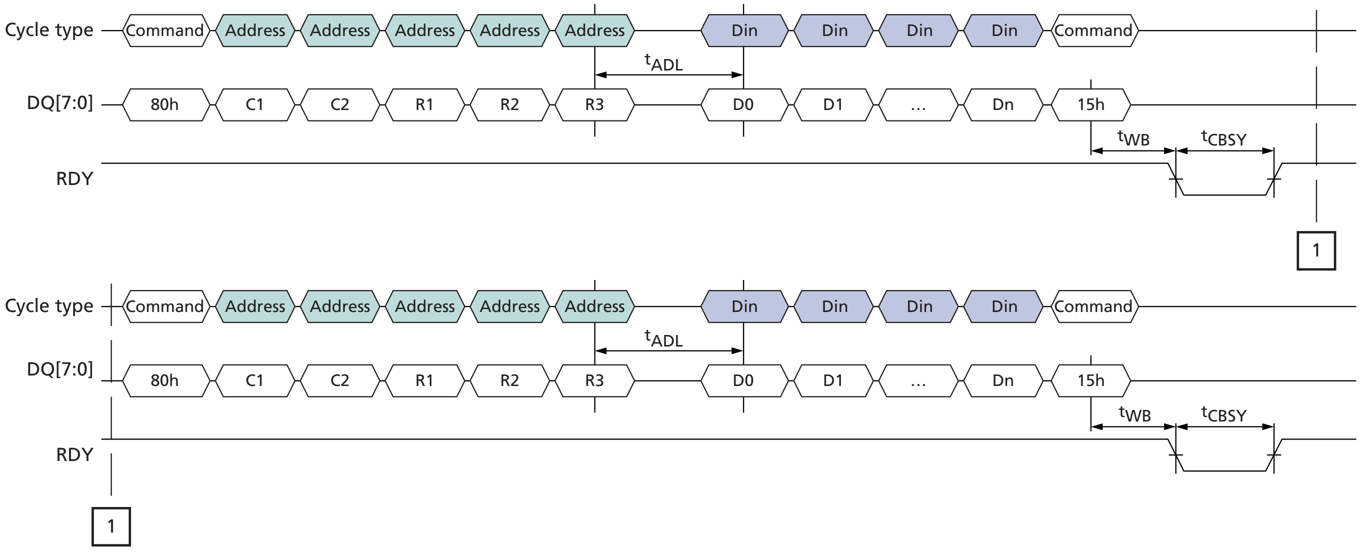
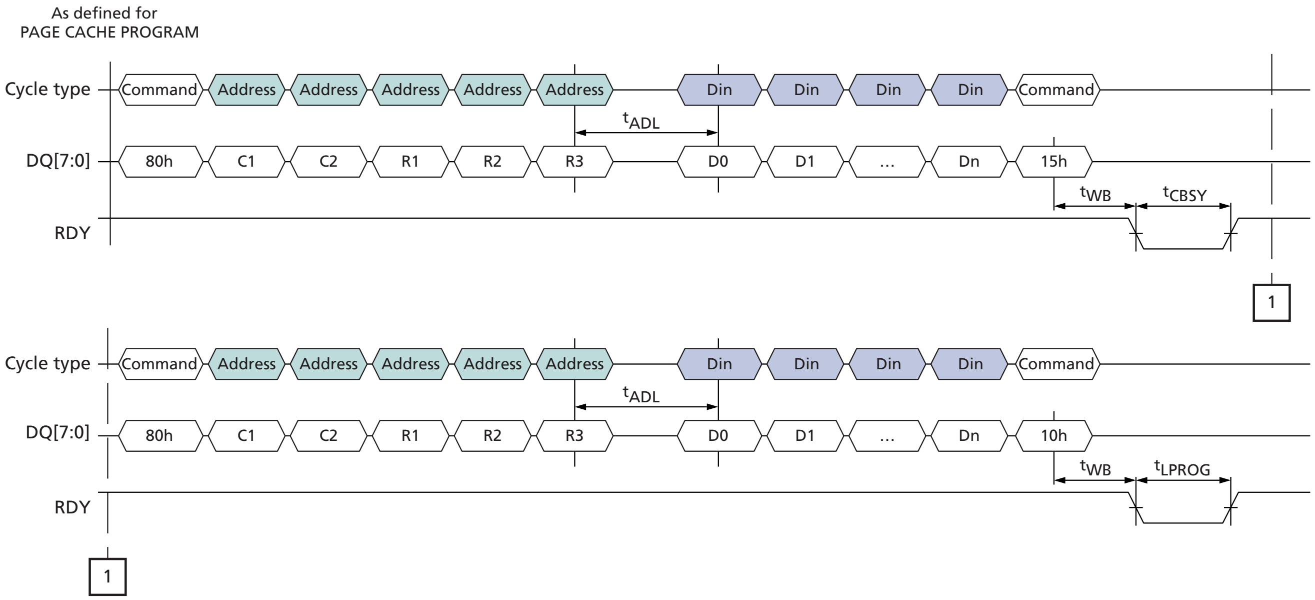


Figure 60: PROGRAM PAGE CACHE (80h–15h) Operation (End)



PROGRAM PAGE MULTI-PLANE (80h-11h)

The PROGRAM PAGE MULTI-PLANE (80h-11h) command enables the host to input data to the addressed plane's cache register and queue the cache register to ultimately be moved to the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified that plane is also queued for data transfer. To input data for the final plane and to begin the program operation for all previously queued planes, issue either the PROGRAM PAGE (80h-10h) command or the PROGRAM PAGE CACHE (80h-15h) command. All of the queued planes will move the data to the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1).

To input a page to the cache register and queue it to be moved to the NAND Flash array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by an 11h command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Write five address cycles containing the column address and row address; data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle, the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands can be issued. When data input is complete, write 11h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}DBSY.

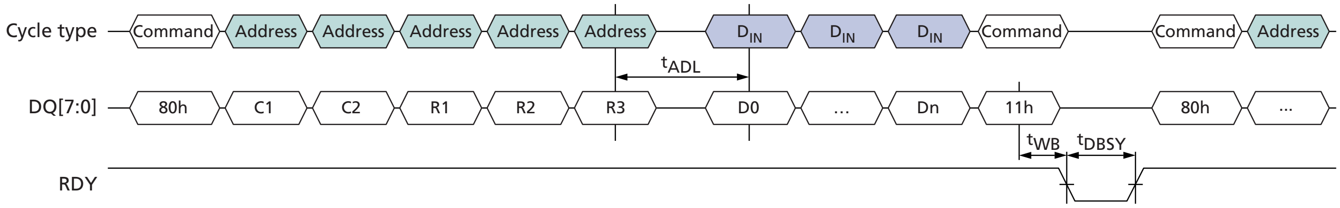
To determine the progress of ^{t}DBSY, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is ready (RDY = 1), additional PROGRAM PAGE MULTI-PLANE (80h-11h) commands can be issued to queue additional planes for data transfer. Alternatively, the PROGRAM PAGE (80h-10h) or PROGRAM PAGE CACHE (80h-15h) commands can be issued.

When the PROGRAM PAGE (80h-10h) command is used as the final command of a multi-plane program operation, data is transferred from the cache registers to the NAND Flash array for all of the addressed planes during ^{t}PROG. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit for each of the planes to verify that programming completed successfully.

When the PROGRAM PAGE CACHE (80h-15h) command is used as the final command of a MULTI-PLANE PROGRAM CACHE operation, data is transferred from the cache registers to the data registers after the previous array operations finish. The data is then moved from the data registers to the NAND Flash array for all of the addressed planes. This occurs during ^{t}CBSY. After ^{t}CBSY, the host should check the status of the FAILC bit for each of the planes from the previous program cache operation, if any, to verify that programming completed successfully.

For the PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE (80h-10h), and PROGRAM PAGE CACHE (80h-15h) commands, see Multi-Plane Operations for multi-plane addressing requirements.

Figure 61: PROGRAM PAGE MULTI-PLANE (80h–11h) Operation



Erase Operations

Erase operations are used to clear the contents of a block in the NAND Flash array to prepare its pages for program operations.

Erase Operations

The ERASE BLOCK (60h-D0h) command, when not preceded by the ERASE BLOCK MULTI-PLANE (60h-D1h) command, erases one block in the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

MULTI-PLANE ERASE Operations

The ERASE BLOCK MULTI-PLANE (60h-D1h) command can be used to further system performance of erase operations by allowing more than one block to be erased in the NAND array. This is done by prepending one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands in front of the ERASE BLOCK (60h-D0h) command. See Multi-Plane Operations for details.

ERASE BLOCK (60h-D0h)

The ERASE BLOCK (60h-D0h) command erases the specified block in the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

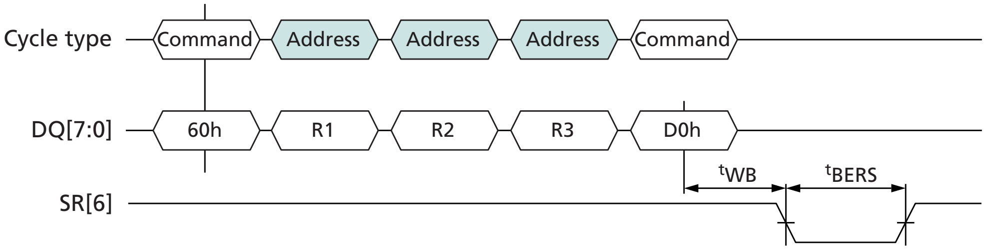
To erase a block, write 60h to the command register. Then write three address cycles containing the row address; the page address is ignored. Conclude by writing D0h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}BERS while the block is erased.

To determine the progress of an ERASE operation, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the die (LUN) is ready (RDY = 1, ARDY = 1) the host should check the status of the FAIL bit.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The ERASE BLOCK (60h-D0h) command is used as the final command of a MULTI-PLANE ERASE operation. It is preceded by one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands. All of blocks in the addressed planes are erased. The host should check the status of the operation by using the status operations (70h, 78h). See Multi-Plane Operations for multi-plane addressing requirements.

Figure 62: ERASE BLOCK (60h-D0h) Operation



ERASE BLOCK MULTI-PLANE (60h-D1h)

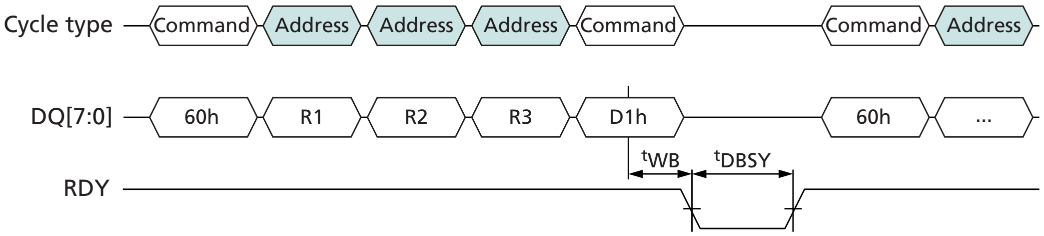
The ERASE BLOCK MULTI-PLANE (60h-D1h) command queues a block in the specified plane to be erased in the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for a block to be erased. To specify the final block to be erased and to begin the ERASE operation for all previously queued planes, issue the ERASE BLOCK (60h-D0h) command. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To queue a block to be erased, write 60h to the command register, then write three address cycles containing the row address; the page address is ignored. Conclude by writing D1h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}DBSY.

To determine the progress of ^{t}DBSY, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is ready (RDY = 1, ARDY = 1), additional ERASE BLOCK MULTI-PLANE (60h-D1h) commands can be issued to queue additional planes for erase. Alternatively, the ERASE BLOCK (60h-D0h) command can be issued to erase all of the queued blocks.

For multi-plane addressing requirements for the ERASE BLOCK MULTI-PLANE (60h-D1h) and ERASE BLOCK (60h-D0h) commands, see Multi-Plane Operations.

Figure 63: ERASE BLOCK MULTI-PLANE (60h–D1h) Operation



Copyback Operations

COPYBACK operations make it possible to transfer data within a plane from one page to another using the cache register. This is particularly useful for block management and wear leveling.

The COPYBACK operation is a two-step process consisting of a COPYBACK READ (00h-35h) and a COPYBACK PROGRAM (85h-10h) command. To move data from one page to another on the same plane, first issue the COPYBACK READ (00h-35h) command. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host can transfer the data to a new page by issuing the COPYBACK PROGRAM (85h-10h) command. When the die (LUN) is again ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

To prevent bit errors from accumulating over multiple COPYBACK operations, it is recommended that the host read the data out of the cache register after the COPYBACK READ (00h-35h) completes prior to issuing the COPYBACK PROGRAM (85h-10h) command. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address. The host should check the data for ECC errors and correct them. When the COPYBACK PROGRAM (85h-10h) command is issued, any corrected data can be input. The CHANGE ROW ADDRESS (85h) command can be used to change the column address.

It is not possible to use the COPYBACK operation to move data from one plane to another or from one die (LUN) to another. Instead, use a READ PAGE (00h-30h) or COPYBACK READ (00h-35h) command to read the data out of the NAND, and then use a PROGRAM PAGE (80h-10h) command with data input to program the data to a new plane or die (LUN).

Between the COPYBACK READ (00h-35h) and COPYBACK PROGRAM (85h-10h) commands, the following commands are supported: status operations (70h, 78h), and column address operations (05h-E0h, 06h-E0h, 85h). Reset operations (FFh, FCh) can be issued after COPYBACK READ (00h-35h), but the contents of the cache registers on the target are not valid.

In devices which have more than one die (LUN) per target, once the COPYBACK READ (00h-35h) is issued, interleaved die (multi-LUN) operations are prohibited until after the COPYBACK PROGRAM (85h-10h) command is issued.

Multi-Plane Copyback Operations

Multi-plane copyback read operations improve read data throughput by copying data simultaneously from more than one plane to the specified cache registers. This is done by prepending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the COPYBACK READ (00h-35h) command.

The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command can be used to further system performance of COPYBACK PROGRAM operations by enabling movement of multiple pages from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more COPYBACK PROGRAM (85h-11h) commands in front of the COPYBACK PROGRAM (85h-10h) command. See Multi-Plane Operations for details.

COPYBACK READ (00h-35h)

The COPYBACK READ (00h-35h) command is functionally identical to the READ PAGE (00h-30h) command, except that 35h is written to the command register instead of 30h. See READ PAGE (00h-30h) (page 90) for further details.

Though it is not required, it is recommended that the host read the data out of the device to verify the data prior to issuing the COPYBACK PROGRAM (85h-10h) command to prevent the propagation of data errors.

Figure 64: COPYBACK READ (00h-35h) Operation

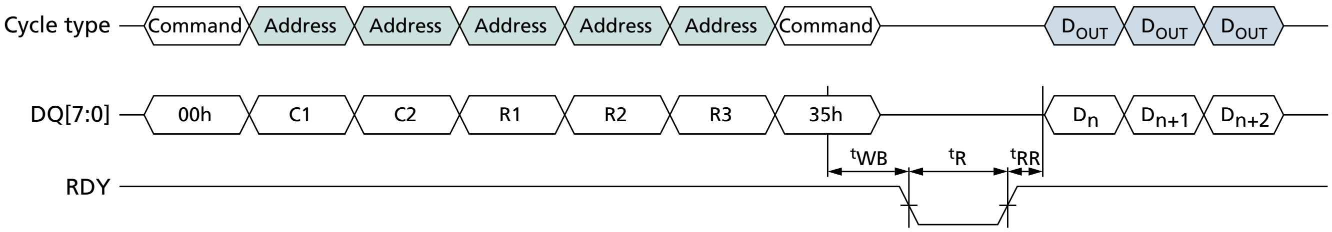
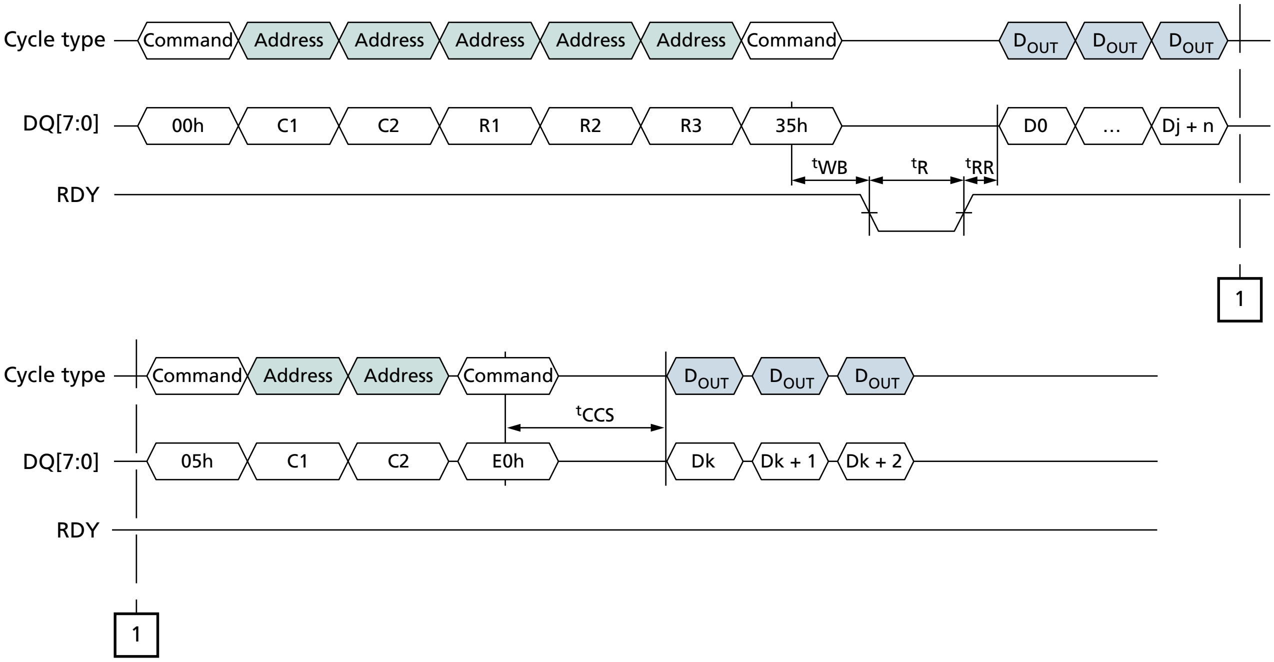


Figure 65: COPYBACK READ (00h–35h) with CHANGE READ COLUMN (05h–E0h) Operation



COPYBACK PROGRAM (85h–10h)

The COPYBACK PROGRAM (85h-10h) command is functionally identical to the PROGRAM PAGE (80h-10h) command, except that when 85h is written to the command register, cache register contents are not cleared. See PROGRAM PAGE (80h-10h) for further details.

Figure 66: COPYBACK PROGRAM (85h–10h) Operation

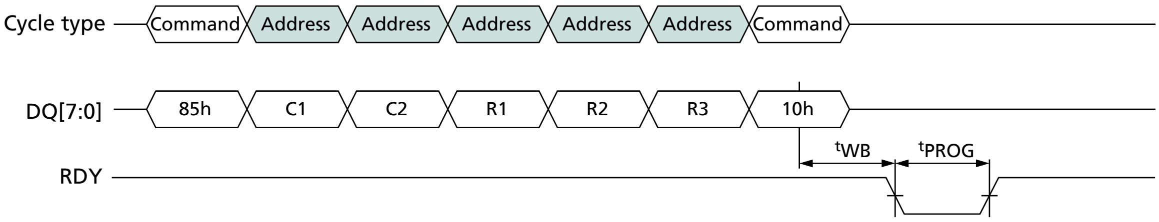
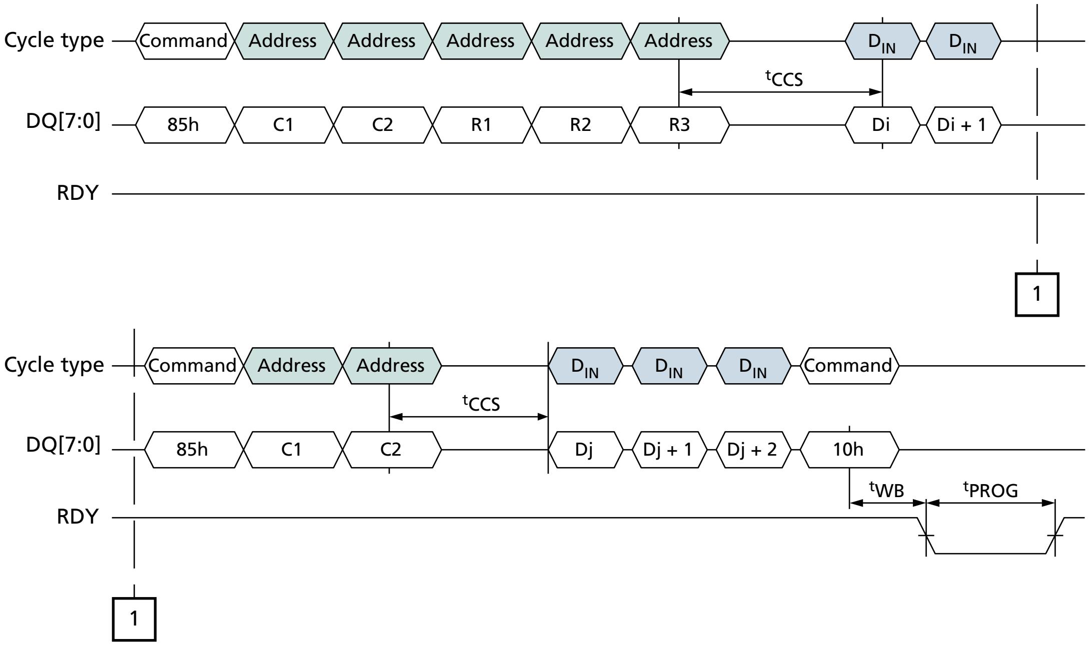


Figure 67: COPYBACK PROGRAM (85h-10h) with CHANGE WRITE COLUMN (85h) Operation



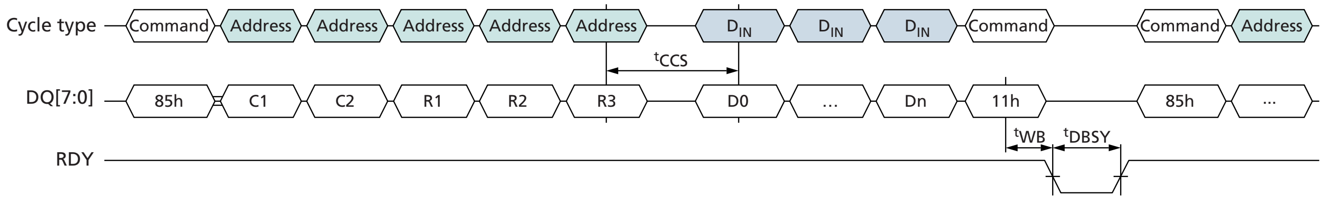
COPYBACK READ MULTI-PLANE (00h-32h)

The COPYBACK READ MULTI-PLANE (00h-32h) command is functionally identical to the READ PAGE MULTI-PLANE (00h-32h) command, except that the 35h command is written as the final command. The complete command sequence for the COPYBACK READ PAGE MULTI-PLANE is 00h-32h-00h-35h. See READ PAGE MULTI-PLANE (00h-32h) (page 95) for further details.

COPYBACK PROGRAM MULTI-PLANE (85h-11h)

The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command is functionally identical to the PROGRAM PAGE MULTI-PLANE (80h-11h) command, except that when 85h is written to the command register, cache register contents are not cleared. See PROGRAM PAGE MULTI-PLANE (80h-11h) for further details.

Figure 68: COPYBACK PROGRAM MULTI-PLANE (85h-11h) Operation



One-Time Programmable (OTP) Operations

This Micron NAND Flash device offers a protected, one-time programmable NAND Flash memory area. Each target has a an OTP area with a range of OTP pages (see Table 20 (page 110)); the entire range is guaranteed to be good. Customers can use the OTP area in any way they desire; typical uses include programming serial numbers or other data for permanent storage.

The OTP area leaves the factory in an erased state (all bits are 1). Programming an OTP page changes bits that are 1 to 0, but cannot change bits that are 0 to 1. The OTP area cannot be erased, even if it is not protected. Protecting the OTP area prevents further programming of the pages in the OTP area.

Enabling the OTP Operation Mode

The OTP area is accessible while the OTP operation mode is enabled. To enable OTP operation mode, issue the SET FEATURES (EFh) command to feature address 90h and write 01h to P1, followed by three cycles of 00h to P2 through P4.

When the target is in OTP operation mode, all subsequent PAGE READ (00h-30h) and PROGRAM PAGE (80h-10h) commands are applied to the OTP area.

ERASE commands are not valid while the target is in OTP operation mode.

Programming OTP Pages

Each page in the OTP area is programming using the PROGRAM OTP PAGE (80h-10h) command. Each page can be programmed more than once, in sections, up to the maximum number allowed (see NOP in Table 20 (page 110)). The pages in the OTP area must be programmed in ascending order.

If the host issues a PAGE PROGRAM (80h-10h) command to an address beyond the maximum page-address range, the target will be busy for ^{t}OBSY and the WP# status register bit will be 0, meaning that the page is write-protected.

Protecting the OTP Area

To protect the OTP area, issue the OTP PROTECT (80h-10h) command to the OTP Protect Page. When the OTP area is protected it cannot be programmed further. It is not possible to unprotect the OTP area after it has been protected.

Reading OTP Pages

To read pages in the OTP area, whether the OTP area is protected or not, issue the PAGE READ (00h-30h) command.

If the host issues the PAGE READ (00h-30h) command to an address beyond the maximum page-address range, the data output will not be valid. To determine whether the target is busy during an OTP operation, either monitor R/B# or use the READ STATUS (70h) command. Use of the READ STATUS ENHANCED (78h) command is prohibited while the OTP operation is in progress.

Returning to Normal Array Operation Mode

To exit OTP operation mode and return to normal array operation mode, issue the SET FEATURES (EFh) command to feature address 90h and write 00h to P1 through P4.

If the RESET (FFh) command is issued while in OTP operation mode, the target will exit OTP operation mode and enter normal operating mode. If the synchronous interface is active, the target will exit OTP operation and enable the asynchronous interface.

If the SYNCHRONOUS RESET (FCh) command is issued while in the OTP operation mode, the target will exit OTP operation mode and the synchronous interface remains active.

Table 20: OTP Area Details

Description	Value
Number of OTP pages	30
OTP protect page address	01h
OTP start page address	02h
Number of partial page programs (NOP) to each OTP page	8

PROGRAM OTP PAGE (80h-10h)

The PROGRAM OTP PAGE (80h-10h) command is used to write data to the pages within the OTP area. To program data in the OTP area, the target must be in OTP operation mode.

To use the PROGRAM OTP PAGE (80h-10h) command, issue the 80h command. Issue five address cycles including the column address, the page address within the OTP page range, and a block address of 0. Next, write the data to the cache register using data input cycles. After data input is complete, issue the 10h command.

R/B# goes LOW for the duration of the array programming time, ^{t}PROG. The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. The RDY bit of the status register will reflect the state of R/B#. Use of the READ STATUS ENHANCED (78h) command is prohibited.

When the target is ready, read the FAIL bit of the status register to determine whether the operation passed or failed (see Status Operations).

The PROGRAM OTP PAGE (80h-10h) command also accepts the CHANGE WRITE COLUMN (85h) command during data input.

If a PROGRAM PAGE command is issued to the OTP area after the area has been protected, then R/B# goes LOW for ^{t}OBSY. After ^{t}OBSY, the status register is set to 60h.

Figure 69: PROGRAM OTP PAGE (80h-10h) Operation

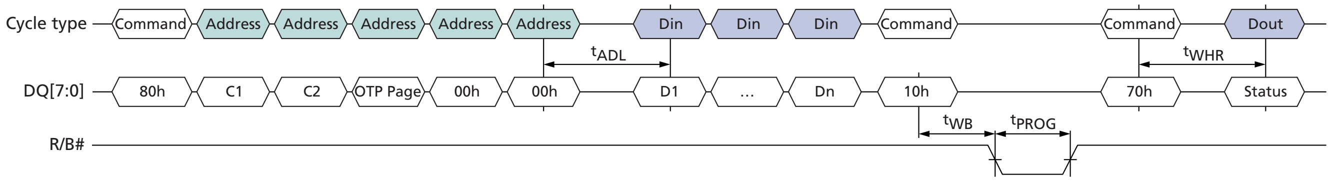
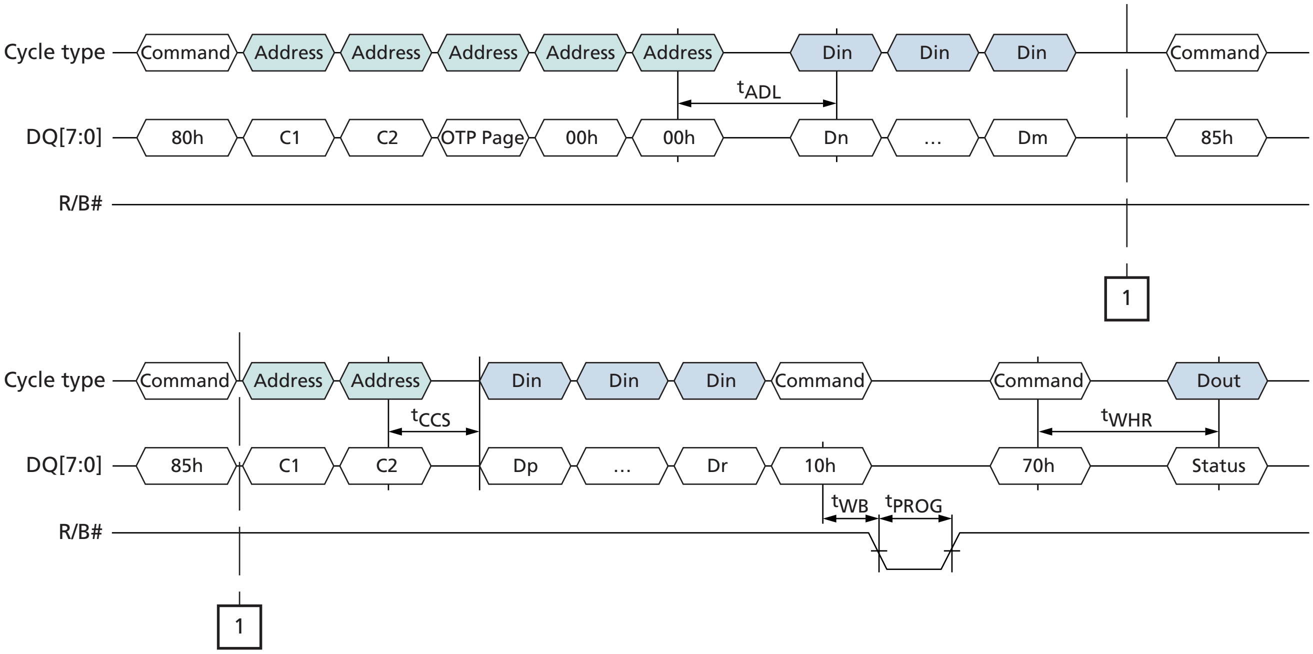


Figure 70: PROGRAM OTP PAGE (80h-10h) with CHANGE WRITE COLUMN (85h) Operation



PROTECT OTP AREA (80h-10h)

The PROTECT OTP AREA (80h-10h) command is used to prevent further programming of the pages in the OTP area. The protect the OTP area, the target must be in OTP operation mode.

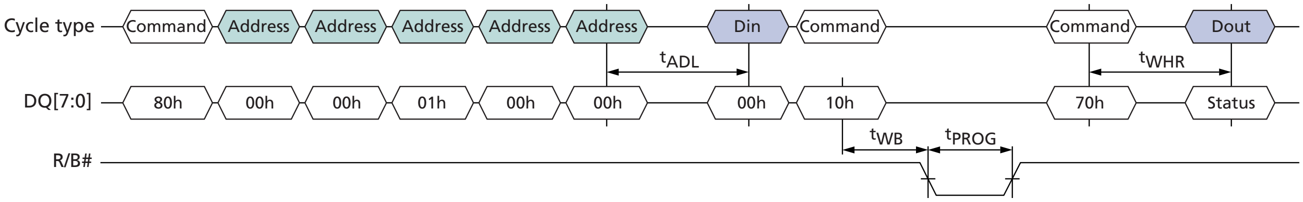
To protect all data in the OTP area, issue the 80h command. Issue five address cycles including the column address, OTP protect page address and block address; the column and block addresses are fixed to 0. Next, write 00h data for the first byte location and issue the 10h command.

R/B# goes LOW for the duration of the array programming time, ^{t}PROG. The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. The RDY bit of the status register will reflect the state of R/B#. Use of the READ STATUS ENHANCED (78h) command is prohibited.

When the target is ready, read the FAIL bit of the status register to determine if the operation passed or failed (see Status Operations).

If the PROTECT OTP AREA (80h-10h) command is issued after the OTP area has already been protected, R/B# goes LOW for ^{t}OBSY. After ^{t}OBSY, the status register is set to 60h.

Figure 71: PROTECT OTP AREA (80h-10h) Operation



Note: 1. OTP data is protected following a status confirmation.

READ OTP PAGE (00h-30h)

The READ OTP PAGE (00h-30h) command is used to read data from the pages in the OTP area. To read data in the OTP area, the target must be in OTP operation mode.

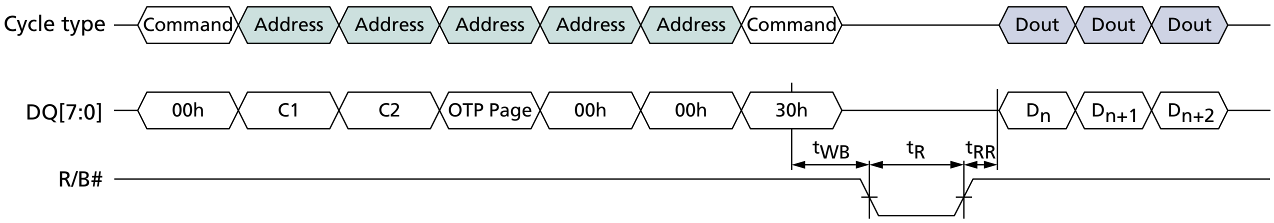
To use the READ OTP PAGE (00h-30h) command, issue the 00h command. Issue five address cycles including the column address, the page address within the OTP page range, and a block address of 0. Next, issue the 30h command. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^tR as data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal, or alternatively the READ STATUS (70h) command can be used. If the status operations are used to monitor the die's (LUN's) status, when the die (LUN) is ready (RDY = 1, ARDY = 1) the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, it begins at the column address specified.

Additional pages within the OTP area can be read by repeating the READ OTP PAGE (00h-30h) command.

The READ OTP PAGE (00h-30h) command is compatible with the CHANGE READ COLUMN (05h-E0h) command. Use of the READ STATUS ENHANCED (78h) and CHANGE READ COLUMN ENHANCED (06h-E0h) commands are prohibited.

Figure 72: READ OTP PAGE (00h-30h) Operation



Multi-Plane Operations

Each NAND Flash logical unit (LUN) is divided into multiple physical planes. Each plane contains a cache register and a data register independent of the other planes. The planes are addressed via the low-order block address bits. Specific details are provided in Device and Array Organization.

Multi-plane operations make better use of the NAND Flash arrays on these physical planes by performing concurrent READ, PROGRAM, or ERASE operations on multiple planes, significantly improving system performance. Multi-plane operations must be of the same type across the planes; for example, it is not possible to perform a PROGRAM operation on one plane with an ERASE operation on another.

When issuing MULTI-PLANE PROGRAM or ERASE operations, use the READ STATUS (70h) command and check whether the previous operation(s) failed. If the READ STATUS (70h) command indicates that an error occurred (FAIL = 1 and/or FAILC = 1), use the READ STATUS ENHANCED (78h) command—time for each plane—to determine which plane operation failed.

Multi-Plane Addressing

Multi-plane commands require an address per operational plane. For a given multi-plane operation, these addresses are subject to the following requirements:

- The LUN address bit(s) must be identical for all of the issued addresses.
- The plane select bit, BA[7], must be different for each issued address.
- The page address bits, PA[6:0], must be identical for each issued address.

The READ STATUS (70h) command should be used following MULTI-PLANE PROGRAM PAGE and ERASE BLOCK operations on a single die (LUN).

Interleaved Die (Multi-LUN) Operations

In devices that have more than one die (LUN) per target, it is possible to improve performance by interleaving operations between the die (LUNs). An interleaved die (multi-LUN) operation is one that individual die (LUNs) involved may be in any combination of busy or ready status during operations.

Interleaved die (multi-LUN) operations are prohibited following RESET (FFh, FCh), identification (90h, ECh, EDh), and configuration (EEh, EFh) operations until ARDY = 1 for all of the die (LUNs) on the target.

During an interleaved die (multi-LUN) operation, there are two methods to determine operation completion. The R/B# signal indicates when all of the die (LUNs) have finished their operations. R/B# remains LOW while any die (LUN) is busy. When R/B# goes HIGH, all of the die (LUNs) are idle and the operations are complete. Alternatively, the READ STATUS ENHANCED (78h) command can report the status of each die (LUN) individually.

If a die (LUN) is performing a cache operation, like PROGRAM PAGE CACHE (80h-15h), then the die (LUN) is able to accept the data for another cache operation when status register bit 6 is 1. All operations, including cache operations, are complete on a die when status register bit 5 is 1.

Use the READ STATUS ENHANCED (78h) command to monitor status for the addressed die (LUN). When multi-plane commands are used with interleaved die (multi-LUN) operations, the multi-plane commands must also meet the requirements, see Multi-Plane Operations for details. After the READ STATUS ENHANCED (78h) command has been issued, the READ STATUS (70h) command may be issued for the previously addressed die (LUN).

See Command Definitions for the list of commands that can be issued while other die (LUNs) are busy.

During an interleaved die (multi-LUN) operation that involves a PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation and a READ operation, the PROGRAM-series operation must be issued before the READ-series operation. The data from the READ-series operation must be output to the host before the next PROGRAM-series operation is issued. This is because the 80h command clears the cache register contents of all cache registers on all planes.

During a interleaved die (multi-LUN) operation that involves PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operations between multiple die (LUNs) on the same target, after data is inputted to the first die (LUN) addressed in that interleaved die (multi-LUN) sequence, before addressing the next die (LUN) with a PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation a program confirm command (via 80h-10h, 80-15h) must be issued to begin the array programming of the pervious die (LUN). If this is not done by the host prior to addressing the next die (LUN), data in all the cache registers of the previously die (LUNs) will be cleared by the PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation to the next die (LUN) in the interleaved die (multi-LUN) sequence. Utilizing the Program Clear functionality in feature address 01h can be utilized to avoid a PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation from clearing the contents of non-addressed NAND planes.

When issuing combinations of commands to multiple die (LUNs) (for example, Reads to one die (LUN) and Programs to another die (LUN)) or Reads to one die (LUN) and Reads to another die (LUN)), the host shall issue the READ STATUS ENHANCED (78h) command before reading data from any LUN. This ensures that only the LUN selected by the READ STATUS ENHANCED (78h) command responds to a data output cycle after being put into data output mode, and thus avoiding bus contention. After the READ STATUS ENHANCED (78h) command is issued to the selected die (LUN) a CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) command shall be issued prior to any data output from the selected die (LUN).

Error Management

Each NAND Flash die (LUN) is specified to have a minimum number of valid blocks (NVB) of the total available blocks. This means the die (LUNs) could have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional blocks can develop with use. However, the total number of available blocks per die (LUN) will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices could contain bad blocks, they can be used quite reliably in systems that provide bad-block management and error-correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the first spare area location and the bad-block mark.

System software should check the first spare area location on the first page of each block prior to performing any PROGRAM or ERASE operations on the NAND Flash device. A bad block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks could be marginal, it may not be possible to recover this information if the block is erased.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Always check status after a PROGRAM or ERASE operation
- Under typical conditions, use the minimum required ECC (see table below)
- Use bad-block management and wear-leveling algorithms

The first block (physical block address 00h) for each CE# is guaranteed to be valid with ECC when shipped from the factory.

Table 21: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB) per LUN	4016
Total available blocks per LUN	4096
First spare area location	Byte 4096
Bad-block mark	00h
Minimum required ECC	4-bit ECC per 540 bytes of data

Output Drive Impedance

Because NAND Flash is designed for use in systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength should be selected based on the expected loading of the memory bus. There are four supported settings for the output drivers: overdrive 2, overdrive 1, nominal, and underdrive.

The nominal output drive strength setting is the power-on default value. The host can select a different drive strength setting using the SET FEATURES (EFh) command.

The output impedance range from minimum to maximum covers process, voltage, and temperature variations. Devices are not guaranteed to be at the nominal line.

Table 22: Output Drive Strength Conditions (V_{CCQ} = 1.7–1.95V)

Range	Process	Voltage	Temperature
Minimum	Fast-Fast	1.95V	T_A (MIN)
Nominal	Typical-Typical	1.8V	+25°C
Maximum	Slow-Slow	1.7V	T_A (MAX)

Table 23: Output Drive Strength Impedance Values (V_{CCQ} = 1.7–1.95V)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
Overdrive 2	Rpd	V_{CCQ} × 0.2	7.5	13.5	34	ohms
		V_{CCQ} × 0.5	9	18	31	ohms
		V_{CCQ} × 0.8	11	23.5	44	ohms
	Rpu	V_{CCQ} × 0.2	11	23.5	44	ohms
		V_{CCQ} × 0.5	9	18	31	ohms
		V_{CCQ} × 0.8	7.5	13.5	34	ohms
Overdrive 1	Rpd	V_{CCQ} × 0.2	10.5	19	47	ohms
		V_{CCQ} × 0.5	13	25	44	ohms
		V_{CCQ} × 0.8	16	32.5	61.5	ohms
	Rpu	V_{CCQ} × 0.2	16	32.5	61.5	ohms
		V_{CCQ} × 0.5	13	25	44	ohms
		V_{CCQ} × 0.8	10.5	19	47	ohms
Nominal	Rpd	V_{CCQ} × 0.2	15	27	66.5	ohms
		V_{CCQ} × 0.5	18	35	62.5	ohms
		V_{CCQ} × 0.8	22	52	88	ohms
	Rpu	V_{CCQ} × 0.2	22	52	88	ohms
		V_{CCQ} × 0.5	18	35	62.5	ohms
		V_{CCQ} × 0.8	15	27	66.5	ohms

Table 23: Output Drive Strength Impedance Values (V_{CCQ} = 1.7–1.95V) (Continued)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
Underdrive	Rpd	V_{CCQ} × 0.2	21.5	39	95	ohms
		V_{CCQ} × 0.5	26	50	90	ohms
		V_{CCQ} × 0.8	31.5	66.5	126.5	ohms
	Rpu	V_{CCQ} × 0.2	31.5	66.5	126.5	ohms
		V_{CCQ} × 0.5	26	50	90	ohms
		V_{CCQ} × 0.8	21.5	39	95	ohms

Table 24: Output Drive Strength Conditions (V_{CCQ} = 2.7–3.6V)

Range	Process	Voltage	Temperature
Minimum	Fast-Fast	3.6V	T_A (MIN)
Nominal	Typical-Typical	3.3V	+25°C
Maximum	Slow-Slow	2.7V	T_A (MAX)

Table 25: Output Drive Strength Impedance Values (V_{CCQ} = 2.7–3.6V)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
Overdrive 2	Rpd	V_{CCQ} X 0.2	7.0	16.2	28.7	ohms
		V_{CCQ} X 0.5	9.0	18.0	36.0	ohms
		V_{CCQ} X 0.8	11.8	21.0	50.0	ohms
	Rpu	V_{CCQ} X 0.2	11.8	21.0	50.0	ohms
		V_{CCQ} X 0.5	9.0	18.0	36.0	ohms
		V_{CCQ} X 0.8	7.0	14.0	28.7	ohms
Overdrive 1	Rpd	V_{CCQ} X 0.2	9.3	22.3	40.0	ohms
		V_{CCQ} X 0.5	12.6	25.0	50.0	ohms
		V_{CCQ} X 0.8	16.3	29.0	68.0	ohms
	Rpu	V_{CCQ} X 0.2	16.3	29.0	68.0	ohms
		V_{CCQ} X 0.5	12.6	25.0	50.0	ohms
		V_{CCQ} X 0.8	9.3	19.0	40.0	ohms
Nominal	Rpd	V_{CCQ} X 0.2	12.8	32.0	58.0	ohms
		V_{CCQ} X 0.5	18.0	35.0	70.0	ohms
		V_{CCQ} X 0.8	23.0	40.0	95.0	ohms
	Rpu	V_{CCQ} X 0.2	23.0	40.0	95.0	ohms
		V_{CCQ} X 0.5	18.0	35.0	70.0	ohms
		V_{CCQ} X 0.8	12.8	32.0	58.0	ohms

Table 25: Output Drive Strength Impedance Values (V_{CCQ} = 2.7–3.6V) (Continued)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
Underdrive	Rpd	V_{CCQ} X 0.2	18.4	45.0	80.0	ohms
		V_{CCQ} X 0.5	25.0	50.0	100.0	ohms
		V_{CCQ} X 0.8	32.0	57.0	136.0	ohms
	Rpu	V_{CCQ} X 0.2	32.0	57.0	136.0	ohms
		V_{CCQ} X 0.5	25.0	50.0	100.0	ohms
		V_{CCQ} X 0.8	18.4	45.0	80.0	ohms

Table 26: Pull-Up and Pull-Down Output Impedance Mismatch

Drive Strength	Minimum	Maximum	Unit	Notes
Overdrive 2	0	6.3	ohms	1, 2
Overdrive 1	0	8.8	ohms	1, 2
Nominal	0	12.3	ohms	1, 2
Underdrive	0	17.5	ohms	1, 2

Notes:
1. Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
2. Test conditions: $V_{CCQ} = V_{CCQ}$ (MIN), $V_{OUT} = V_{CCQ} \times 0.5$, $T_A = T_{OPER}$.

AC Overshoot/Undershoot Specifications

The supported AC overshoot and undershoot area depends on the timing mode selected by the host.

Table 27: Asynchronous Overshoot/Undershoot Parameters

Parameter	Timing Mode						Unit
	0	1	2	3	4	5	
Maximum peak amplitude provided for overshoot area	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	1	1	1	1	1	1	V
Maximum overshoot area above V_{CCQ}	3	3	3	3	3	3	V-ns
Maximum undershoot area below V_{SSQ}	3	3	3	3	3	3	V-ns

Table 28: Synchronous Overshoot/Undershoot Parameters

Parameter	Timing Mode						Unit
	0	1	2	3	4	5	
Maximum peak amplitude provided for overshoot area	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	1	1	1	1	1	1	V
Maximum overshoot area above V_{CCQ}	3	3	3	2.25	1.8	1.5	V-ns
Maximum undershoot area below V_{SSQ}	3	3	3	2.25	1.8	1.5	V-ns

Figure 73: Overshoot

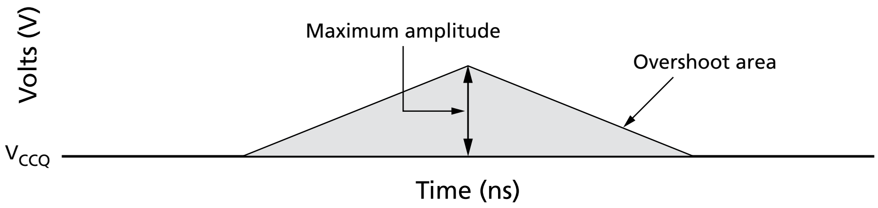
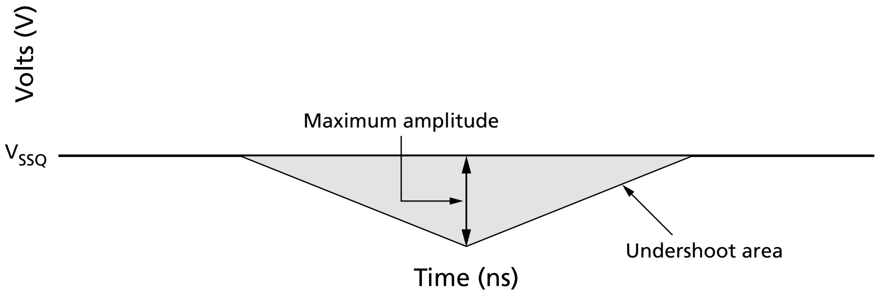


Figure 74: Undershoot



Synchronous Input Slew Rate

Though all AC timing parameters are tested with a nominal input slew rate of 1 V/ns, it is possible to run the device at a slower slew rate. The input slew rates shown below are sampled, and not 100% tested. When using slew rates slower than the minimum values, timing must be derated by the host.

Table 29: Test Conditions for Input Slew Rate

Parameter	Value
Rising edge	$V_{IL(DC)}$ To $V_{IH(AC)}$
Falling edge	$V_{IH(DC)}$ To $V_{IL(AC)}$
Temperature range	T_A

Table 30: Input Slew Rate (V_{CCQ} = 1.7–1.95V)

Command/ Address and DQ V/ns	CLK/DQS Slew Rate Derating $V_{IH(AC)}/V_{IL(AC)}$= 540mV, $V_{IH(DC)}/V_{IL(DC)}$= 360mV																Unit
	1		0.9		0.8		0.7		0.6		0.5		0.4		0.3		
	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	
1	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	ps
0.9	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	ps
0.8	-	-	0	0	0	0	0	0	-	-	-	-	-	-	-	-	ps
0.7	-	-	-	-	0	0	0	0	0	0	-	-	-	-	-	-	ps
0.6	-	-	-	-	-	-	0	0	0	0	0	0	-	-	-	-	ps
0.5	-	-	-	-	-	-	-	-	0	0	0	0	180	180	-	-	ps
0.4	-	-	-	-	-	-	-	-	-	-	180	180	360	360	660	660	ps
0.3	-	-	-	-	-	-	-	-	-	-	-	-	660	660	920	920	ps

Output Slew Rate

The output slew rate is tested using the following setup with only one die per DQ channel.

Table 31: Test Conditions for Output Slew Rate

Parameter	Value
$V_{OL(DC)}$	0.3 × V_{CCQ}
$V_{OH(DC)}$	0.7 × V_{CCQ}
$V_{OL(AC)}$	0.2 × V_{CCQ}
$V_{OH(AC)}$	0.8 × V_{CCQ}
Rising edge (^{t}RISE)	$V_{OL(DC)}$ to $V_{OH(AC)}$
Falling edge (^{t}FALL)	$V_{OH(DC)}$ to $V_{OL(AC)}$
Output capacitive load (C_{LOAD})	5pF
Temperature range	T_A

Table 32: Output Slew Rate (V_{CCQ} = 1.7–1.95V)

Output Drive Strength	Min	Max	Unit
Overdrive 2	1	5.5	V/ns
Overdrive 1	0.85	5	V/ns
Nominal	0.75	4	V/ns
Underdrive	0.6	4	V/ns

Table 33: Output Slew Rate (V_{CCQ} = 2.7–3.6V)

Output Drive Strength	Min	Max	Unit
Overdrive 2	1.5	10.0	V/ns
Overdrive 1	1.5	9.0	V/ns
Nominal	1.2	7.0	V/ns
Underdrive	1.0	5.5	V/ns

Electrical Specifications

Stresses greater than those listed can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

Table 34: Absolute Maximum Ratings by Device

Parameter	Symbol	Min[1]	Max[1]	Unit
Voltage input	V_{IN}	-0.6	4.6	V
V_{CC} supply voltage	V_{CC}	-0.6	4.6	V
V_{CCQ} supply voltage	V_{CCQ}	-0.6	4.6	V
Storage temperature	T_{STG}	-65	150	°C

Note: 1. Voltage on any pin relative to V_{SS}.

Table 35: Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit
Operating temperature	Automotive	T_A	–40	–	+85	°C
V_{CC} supply voltage		V_{CC}	2.7	3.3	3.6	V
V_{CCQ} supply voltage (1.8V)		V_{CCQ}	1.7	1.8	1.95	V
V_{CCQ} supply voltage (3.3V)			2.7	3.3	3.6	V
V_{SS} ground voltage		V_{SS}	0	0	0	V

Table 36: Valid Blocks per LUN

Parameter	Symbol	Min	Max	Unit	Notes
Valid block number	NVB	4016	4096	Blocks	1

Note: 1. Invalid blocks are block that contain one or more bad bits beyond ECC. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid from the factory.

Table 37: Capacitance: 100-Ball BGA Package

Notes 1 and 2 apply to entire table

		Single Die/Dual Die Package			Quad Die Package			Octal Die Package				
Description	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (CLK)	C_{CK}	3.0	3.5	4.0	5.2	6.2	7.2	8.5	10.5	12.5	pF	3
Input capacitance (ALE, CLE, W/R#)	C_{IN}	3.5	4	4.5	5.8	6.8	7.8	8.5	10.5	12.5	pF	3
Input/output capacitance (DQ[7:0], DQS)	C_{IO}	4	4.5	5	7	8	9	12.5	14.5	16.5	pF	3
Input capacitance (CE#, WP#)	C_{OTHER}	–	–	5	–	–	10	–	–	13	pF	
Delta clock capacitance	DC_{CK}	–	–	0.25	–	–	0.5	–	–	1	pF	
Delta input capacitance	DC_{IN}	–	–	0.5	–	–	1	–	–	2	pF	
Delta input/output capacitance	DC_{IO}	–	–	0.5	–	–	1	–	–	2	pF	

Notes:
1. Verified in device characterization; not 100% tested.
2. Test conditions: $T_A = 25°C$, $f = 100$ MHz, $V_{IN} = 0V$.
3. Values for C_{CK}, C_{IN} and C_{IO} (TYP) are estimates.

Table 38: Capacitance: 48-Pin TSOP Package

Description	Symbol	Device	Max	Unit	Notes
Input capacitance – ALE, CE#, CLE, RE# (W/R#), WE# (CLK), WP#	C_{IN}	Single die package	10	pF	1
		Dual die package	14		
		Quad die package	18		
Input/output capacitance – DQ[7:0], DQS	C_{IO}	Single die package	5	pF	1
		Dual die package	10		
		Quad die package	18		

Note:
1. These parameters are verified in device characterization and are not 100% tested. Test conditions: $T_C = 25°C$; f = 1 MHz; Vin = 0V.

Table 39: Capacitance: 52-Pad LGA Package

Description	Symbol	Device	Max	Unit	Notes
Input capacitance – ALE, CE#, CLE, RE#, WE#, WP#	C_{IN}	Quad die package	10	pF	1
		Octal die package	20		

Table 39: Capacitance: 52-Pad LGA Package (Continued)

Description	Symbol	Device	Max	Unit	Notes
Input/output capacitance – DQ[7:0]	C_{IO}	Quad die package	14	pF	1
		Octal die package	20		

Note: 1. These parameters are verified in device characterization and are not 100% tested. Test conditions: T_C = 25°C; f = 1 MHz; Vin = 0V.

Table 40: Test Conditions

Parameter	Value	Notes
Rising input transition	$V_{IL(DC)}$ to $V_{IH(AC)}$	1
Falling input transition	$V_{IH(DC)}$ to $V_{IL(AC)}$	1
Input rise and fall slew rates	1 V/ns	–
Input and output timing levels	$V_{CCQ}/2$	–
Output load: Nominal output drive strength	C_L = 5pF	2, 3

Notes:
1. The receiver will effectively switch as a result of the signal crossing the AC input level; it will remain in that status as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
2. Transmission line delay is assumed to be very small.
3. This test setup applies to all package configurations.

Electrical Specifications – DC Characteristics and Operating Conditions (Asynchronous)

Table 41: DC Characteristics and Operating Conditions (Asynchronous Interface)

Parameter	Conditions	Symbol	Min[1]	Typ[1]	Max[1]	Unit
Array read current (active)	–	I_{CC1_A}	–	20	50	mA
Array program current (active)	–	I_{CC2_A}	–	20	50	mA
Erase current (active)	–	I_{CC3_A}	–	20	50	mA
I/O burst read current	$^tRC = {}^tRC$ (MIN); I_{OUT}= 0mA	I_{CC4R_A}	–	5	10	mA
I/O burst write current	$^tWC = {}^tWC$ (MIN)	I_{CC4w_A}	–	5	10	mA
Bus idle current	–	I_{CC5_A}	–	3	5	mA
Current during first RESET command after power-on	–	I_{CC6}	–	–	10	mA
Standby current - V_{CC}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SB}	–	10	50	µA
Standby current - V_{CCQ}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SBQ}	–	3	10	µA

Table 41: DC Characteristics and Operating Conditions (Asynchronous Interface) (Continued)

Parameter	Conditions	Symbol	Min[1]	Typ[1]	Max[1]	Unit
Staggered power-up current	^{t}RISE = 1ms; C_{LINE} = 0.1uF	I_{ST}	–	–	10	mA

Note: 1. All values are per die (LUN) unless otherwise specified.

Electrical Specifications – DC Characteristics and Operating Conditions (Synchronous)

Table 42: DC Characteristics and Operating Conditions (Synchronous Interface)

Parameter	Conditions	Symbol	Min[1]	Typ[1]	Max[1]	Unit
Array read current (active)	CE# = V_{IL}; ^{t}CK = ^{t}CK (MIN)	I_{CC1_S}	–	20	50	mA
Array program current (active)	^{t}CK = ^{t}CK (MIN)	I_{CC2_S}	–	20	50	mA
Erase current (active)	^{t}CK = ^{t}CK (MIN)	I_{CC3_S}	–	20	50	mA
I/O burst read current	^{t}CK = ^{t}CK (MIN)	I_{CC4R_S}; I_{OUT}= 0mA	–	10	20	mA
I/O burst write current	^{t}CK = ^{t}CK (MIN)	I_{CC4W_S}	–	10	20	mA
Bus idle current	^{t}CK = ^{t}CK (MIN)	I_{CC5_S}	–	5	10	mA
Standby current - V_{CC}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SB}	–	10	50	µA
Standby Current - V_{CCQ}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SBQ}	–	3	10	µA

Note: 1. All values are per die (LUN) unless otherwise specified.

Electrical Specifications – DC Characteristics and Operating Conditions (V_{CCQ})

Table 43: DC Characteristics and Operating Conditions (3.3V V_{CCQ})

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
AC input high voltage	CE#, DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (RE#), WP#	$V_{IH(AC)}$	0.8 × V_{CCQ}	–	V_{CCQ} + 0.3	V	
AC input low voltage		$V_{IL(AC)}$	–0.3	–	0.2 × V_{CCQ}	V	
DC input high voltage	DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (RE#)	$V_{IH(DC)}$	0.7 × V_{CCQ}	–	V_{CCQ} + 0.3	V	
DC input low voltage		$V_{IL(DC)}$	–0.3	–	0.3 × V_{CCQ}	V	
Input leakage current	Any input V_{IN} = 0V to V_{CCQ} (all other pins under test = 0V)	I_{LI}	–	–	±10	µA	
Output leakage current	DQ are disabled; V_{OUT} = 0V to V_{CCQ}	I_{LO}	–	–	±10	µA	1

Table 43: DC Characteristics and Operating Conditions (3.3V V_{CCQ}) (Continued)

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
Output low current (R/B#)	V_{OL} = 0.4V	I_{OL} (R/B#)	8	10	–	mA	2

Notes:
1. All leakage currents are per die (LUN). Two die (LUNs) have a maximum leakage current of ±20µA and four die (LUNs) have a maximum leakage current of ±40µA in the asynchronous interface.
2. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See Table 19 (page 79) for additional details.

Table 44: DC Characteristics and Operating Conditions (1.8V V_{CCQ})

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
AC input high voltage	CE#, DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (R/E#), WP#	$V_{IH(AC)}$	0.8 × V_{CCQ}	–	V_{CCQ} + 0.3	V	
AC input low voltage		$V_{IL(AC)}$	–0.3	–	0.2 × V_{CCQ}	V	
DC input high voltage	DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (R/E#)	$V_{IH(DC)}$	0.7 × V_{CCQ}	–	V_{CCQ} + 0.3	V	
DC input low voltage		$V_{IL(DC)}$	-0.3	–	0.3 × V_{CCQ}	V	
Input leakage current	Any input V_{IN} = 0V to V_{CCQ} (all other pins under test = 0V)	I_{LI}	–	–	±10	µA	1
Output leakage current	DQ are disabled; Vout = 0V to V_{CCQ}	I_{LO}	–	–	±10	µA	1
Output low current (R/B#)	V_{OL} = 0.2V	I_{OL} (R/B#)	3	4	–	mA	

Note: 1. All leakage currents are per die (LUN). Two die (LUNs) have a maximum leakage current of ±20µA and four die (LUNs) have a maximum leakage current of ±40µA in the asynchronous interface.

Electrical Specifications – AC Characteristics and Operating Conditions (Asynchronous)

Table 45: AC Characteristics: Asynchronous Command, Address, and Data

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock period		100		50		35		30		25		20		ns	
Frequency		≈10		≈20		≈28		≈33		≈40		≈50		MHz	
ALE to data start	^{t}ADL	200	–	100	–	100	–	100	–	70	–	70	–	ns	1
ALE hold time	^{t}ALH	20	–	10	–	10	–	5	–	5	–	5	–	ns	
ALE setup time	^{t}ALS	50	–	25	–	15	–	10	–	10	–	10	–	ns	
ALE to RE# delay	^{t}AR	25	–	10	–	10	–	10	–	10	–	10	–	ns	
CE# access time	^{t}CEA	–	100	–	45	–	30	–	25	–	25	–	25	ns	
CE# hold time	^{t}CH	20	–	10	–	10	–	5	–	5	–	5	–	ns	
CE# HIGH to output High-Z	^{t}CHZ	–	100	–	50	–	50	–	50	–	30	–	30	ns	2
CLE hold time	^{t}CLH	20	–	10	–	10	–	5	–	5	–	5	–	ns	
CLE to RE# delay	^{t}CLR	20	–	10	–	10	–	10	–	10	–	10	–	ns	
CLE setup time	^{t}CLS	50	–	25	–	15	–	10	–	10	–	10	–	ns	
CE# HIGH to output hold	^{t}COH	0	–	15	–	15	–	15	–	15	–	15	–	ns	
CE# setup time	^{t}CS	70	–	35	–	25	–	25	–	20	–	15	–	ns	
Data hold time	^{t}DH	20	–	10	–	5	–	5	–	5	–	5	–	ns	
Data setup time	^{t}DS	40	–	20	–	15	–	10	–	10	–	7	–	ns	
Output High-Z to RE# LOW	^{t}IR	10	–	0	–	0	–	0	–	0	–	0	–	ns	
RE# cycle time	^{t}RC	100	–	50	–	35	–	30	–	25	–	20	–	ns	
RE# access time	^{t}REA	–	40	–	30	–	25	–	20	–	20	–	16	ns	3
RE# HIGH hold time	^{t}REH	30	–	15	–	15	–	10	–	10	–	7	–	ns	3
RE# HIGH to output hold	^{t}RHOH	0	–	15	–	15	–	15	–	15	–	15	–	ns	3
RE# HIGH to WE# LOW	^{t}RHW	200	–	100	–	100	–	100	–	100	–	100	–	ns	
RE# HIGH to output High-Z	^{t}RHZ	–	200	–	100	–	100	–	100	–	100	–	100	ns	2, 3
RE# LOW to output hold	^{t}RLOH	0	–	0	–	0	–	0	–	5	–	5	–	ns	3
RE# pulse width	^{t}RP	50	–	25	–	17	–	15	–	12	–	10	–	ns	
Ready to RE# LOW	^{t}RR	40	–	20	–	20	–	20	–	20	–	20	–	ns	
WE# HIGH to R/B# LOW	^{t}WB	–	200	–	100	–	100	–	100	–	100	–	100	ns	4
WE# cycle time	^{t}WC	100	–	45	–	35	–	30	–	25	–	20	–	ns	

Table 45: AC Characteristics: Asynchronous Command, Address, and Data (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
WE# HIGH hold time	^tWH	30	–	15	–	15	–	10	–	10	–	7	–	ns	
WE# HIGH to RE# LOW	^tWHR	120	–	80	–	80	–	60	–	60	–	60	–	ns	
WE# pulse width	^tWP	50	–	25	–	17	–	15	–	12	–	10	–	ns	
WP# transition to WE# LOW	^tWW	100	–	100	–	100	–	100	–	100	–	100	–	ns	

Notes:
1. Timing for ^tADL begins in the address cycle, on the final rising edge of WE# and ends with the first rising edge of WE# for data input.
2. Data transition is measured ±200mV from steady-steady voltage with load. This parameter is sampled and not 100 percent tested.
3. AC characteristics may need to be relaxed if output drive strength is not set to at least nominal.
4. Do not issue a new command during ^tWB, even if R/B# or RDY is ready.

Electrical Specifications – AC Characteristics and Operating Conditions (Synchronous)

Table 46: AC Characteristics: Synchronous Command, Address, and Data

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock period		50		30		20		15		12		10		ns	
Frequency		≈20		≈33		≈50		≈67		≈83		≈100		MHz	
Access window of DQ[7:0] from CLK	^{t}AC	3	20	3	20	3	20	3	20	3	20	3	20	ns	
ALE to data loading time	^{t}ADL	100	–	100	–	70	–	70	–	70	–	70	–	ns	
Command, address data delay	^{t}CAD	25	–	25	–	25	–	25	–	25	–	25	–	ns	1
ALE, CLE, W/R# hold	^{t}CALH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
ALE, CLE, W/R# setup	^{t}CALS	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
DQ hold – command, address	^{t}CAH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
DQ setup – command, address	^{t}CAS	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
CE# hold	^{t}CH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
Average CLK cycle time	^{t}CK (avg)	50	100	30	50	20	30	15	20	12	15	10	12	ns	3
Absolute CLK cycle time, from rising edge to rising edge	^{t}CK (abs)	^{t}CK (abs) MIN = ^{t}CK (avg) + ^{t}JIT (per) MIN ^{t}CK (abs) MAX = ^{t}CK (avg) + ^{t}JIT (per) MAX												ns	
CLK cycle HIGH	^{t}CKH (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^{t}CK	4
CLK cycle LOW	^{t}CKL (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^{t}CK	4
Data output end to W/R# HIGH	^{t}CKWR	^{t}CKWR(MIN) = RoundUp[(^{t}DQSCK(MAX) + ^{t}CK)/^{t}CK]												^{t}CK	
CE# setup	^{t}CS	35	–	25	–	15	–	15	–	15	–	15	–	ns	
Data In hold	^{t}DH	5	–	2.5	–	1.7	–	1.3	–	1.1	–	0.8	–	ns	
Access window of DQS from CLK	^{t}DQSCK	–	20	–	20	–	20	–	20	–	20	–	20	ns	

Table 46: AC Characteristics: Synchronous Command, Address, and Data (Continued)

		Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
DQS, DQ[7:0] Driven by NAND	^{t}DQSD	–	18	–	18	–	18	–	18	–	18	–	18	ns	
DQS, DQ[7:0] to tri-state	^{t}DQSHZ	–	20	–	20	–	20	–	20	–	20	–	20	ns	5
DQS input high pulse width	^{t}DQSH	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK	
DQS input low pulse width	^{t}DQSL	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK	
DQS-DQ skew	^{t}DQSQ	–	5	–	2.5	–	1.7	–	1.3	–	1.0	–	0.85	ns	
Data input	^{t}DQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	^{t}CK	
Data In setup	^{t}DS	5	–	3	–	2	–	1.5	–	1.1	–	0.8	–	ns	
DQS falling edge from CLK rising – hold	^{t}DSH	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	^{t}CK	
DQS falling to CLK rising – setup	^{t}DSS	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	^{t}CK	
Data valid window	^{t}DVW	^{t}DVW = ^{t}QH - ^{t}DQSQ												ns	
Half clock period	^{t}HP	^{t}HP = Min(^{t}CKH, ^{t}CKL)												ns	
The deviation of a given ^{t}CK (abs) from a ^{t}CK (avg)	^{t}JIT (per)	–0.7	0.7	–0.7	0.7	–0.7	0.7	–0.6	0.6	–0.6	0.6	–0.5	0.5	ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	^{t}QH	^{t}QH = ^{t}HP - ^{t}QHS												ns	
Data hold skew factor	^{t}QHS	–	6	–	3	–	2	–	1.5	–	1.2	–	1	ns	
Data output to command, address, or data input	^{t}RHW	100	–	100	–	100	–	100	–	100	–	100		ns	
Ready to data output	^{t}RR	20	–	20	–	20	–	20	–	20	–	20	–	ns	
CLK HIGH to R/B# LOW	^{t}WB	–	100	–	100	–	100	–	100	–	100	–	100	ns	
Command cycle to data output	^{t}WHR	80	–	80	–	80	–	80	–	80	–	80	–	ns	

Table 46: AC Characteristics: Synchronous Command, Address, and Data (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS write preamble	^{t}WPRE	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	^{t}CK	
DQS write postamble	^{t}WPST	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	^{t}CK	
W/R# LOW to data output cycle	^{t}WRCK	20	–	20	–	20	–	20	–	20	–	20	–	ns	
WP# transition to command cycle	^{t}WW	100	–	100	–	100	–	100	–	100	–	100	–	ns	

Notes:
1. Delay is from start of command to next command, address, or data cycle; start of address to next command, address, or data cycle; and end of data to start of next command, address, or data cycle.
2. This value is specified in the parameter page.
3. ^{t}CK(avg) is the average clock period over any consecutive 200-cycle window.
4. ^{t}CKH(abs) and ^{t}CKL(abs) include static offset and duty cycle jitter.
5. ^{t}DQSHZ begins when W/R# is latched HIGH by CLK. This parameter is not referenced to a specific voltage level; it specifies when the device outputs are no longer driving.

Electrical Specifications – Array Characteristics

Table 47: Array Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial page programs	NOP	–	4	Cycles	1
ERASE BLOCK operation time	^{t}BERS	0.7	3.5	ms	
Cache busy	^{t}CBSY	3	500	µs	
Dummy busy time	^{t}DBSY	0.5	1	µs	
Cache read busy time	^{t}RCBSY	3	25	µs	
Busy time for SET FEATURES and GET FEATURES operations	^{t}FEAT	–	1	µs	
Busy time for interface change	^{t}ITC	–	1	µs	2
LAST PAGE PROGRAM operation time	^{t}LPROG	–	–	µs	3
Busy time for OTP DATA PROGRAM operation if OTP is protected	^{t}OBSY	–	30	µs	
Power-on reset time	^{t}POR	–	1	ms	
PROGRAM PAGE operation time	^{t}PROG	230	500	µs	
READ PAGE operation time	^{t}R	–	25	µs	

Notes:
1. The pages in the OTP Block have an NOP of 8.
2. ^{t}ITC (MAX) is the busy time when the interface changes from asynchronous to synchronous using the SET FEATURES (EFh) command or synchronous to asynchronous using the RESET (FFh) command. During the ^{t}ITC time, any command, including READ STATUS (70h) and READ STATUS ENHANCED (78h), is prohibited.
3. ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last page - 1) - command load time (last page) - address load time (last page) - data load time (last page).

Asynchronous Interface Timing Diagrams

Figure 75: RESET Operation

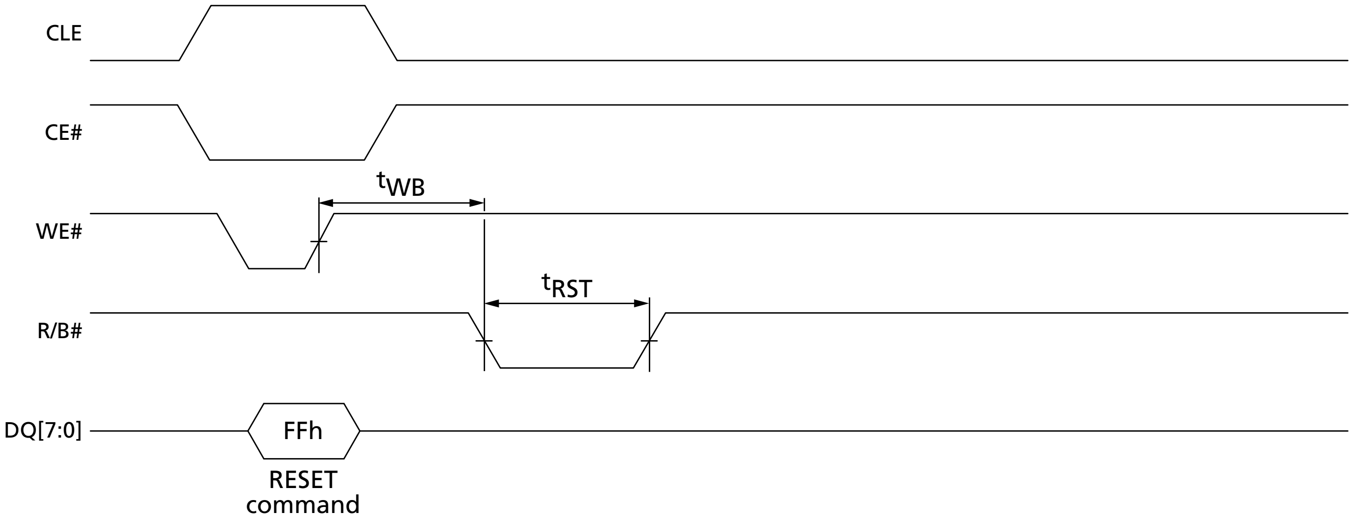


Figure 76: READ STATUS Cycle

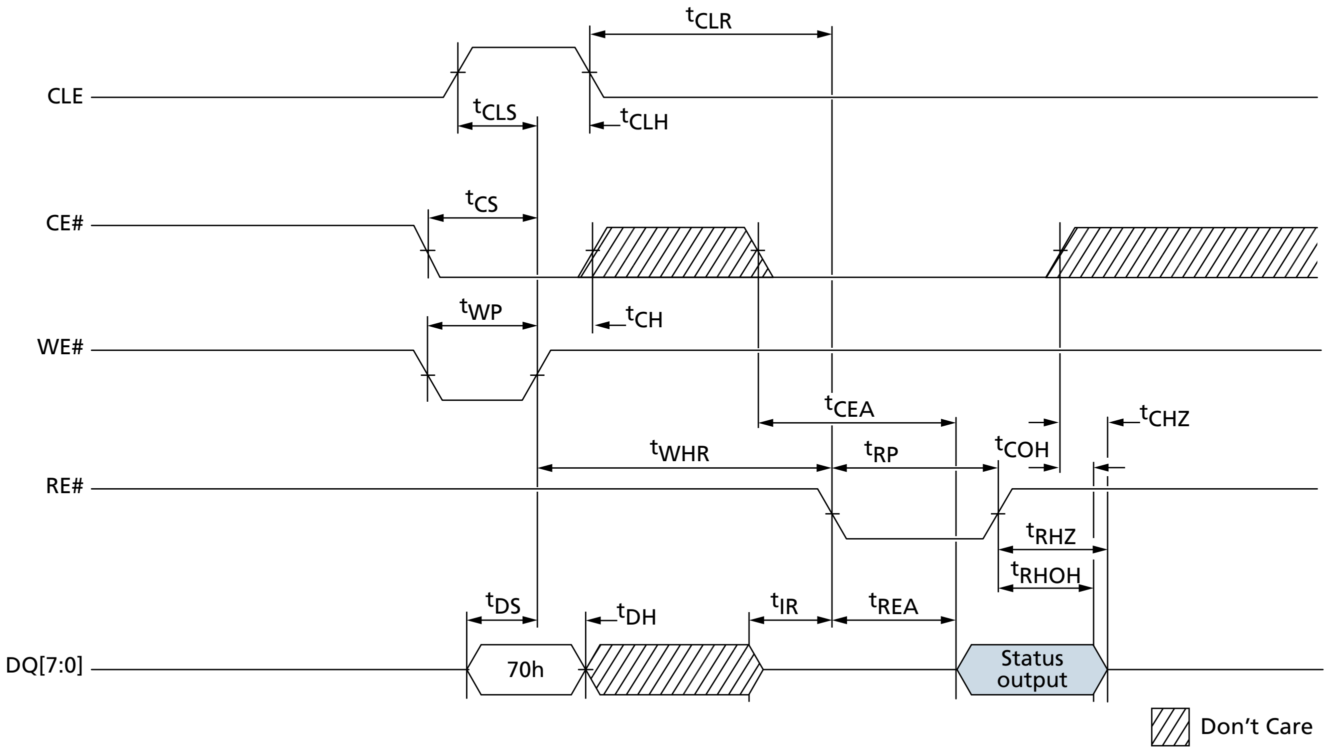


Figure 77: READ STATUS ENHANCED Cycle

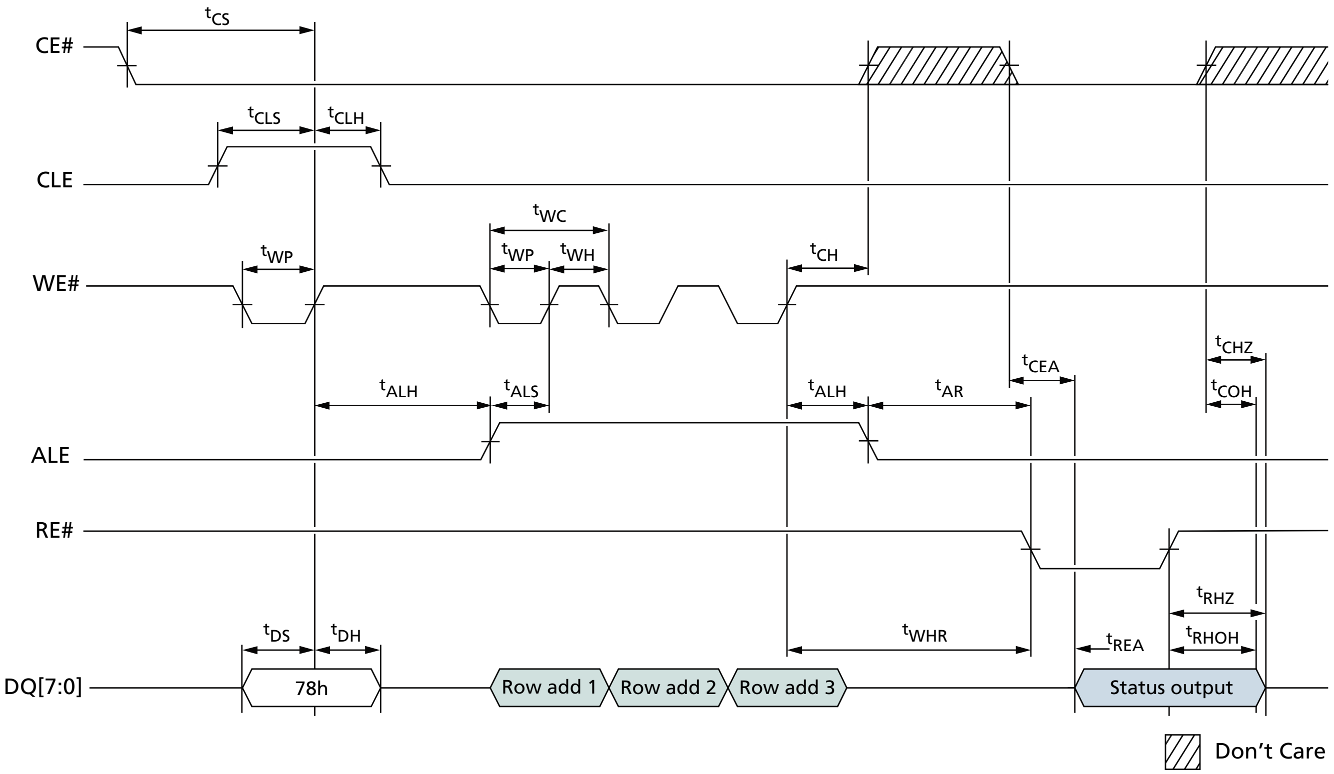


Figure 78: READ PARAMETER PAGE

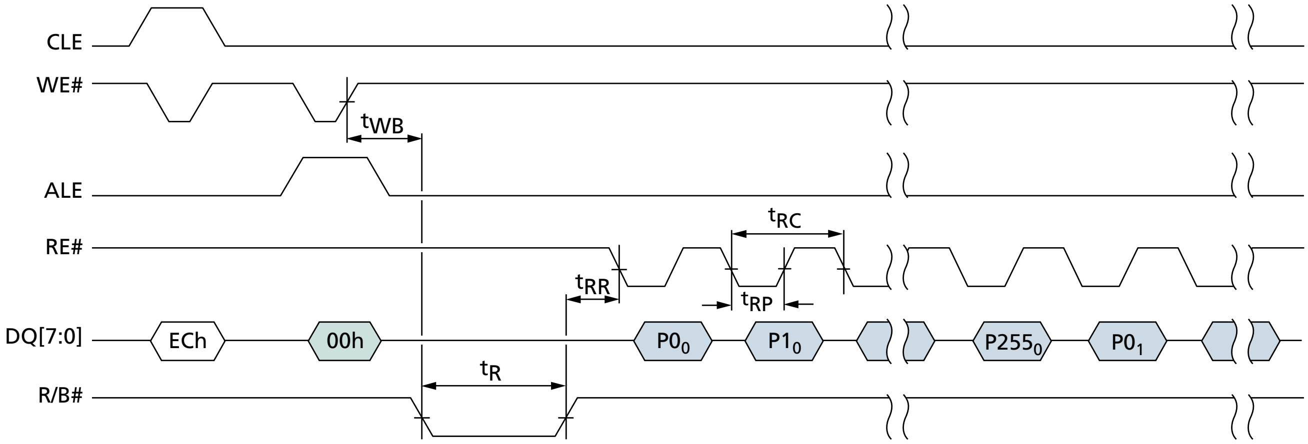


Figure 79: READ PAGE

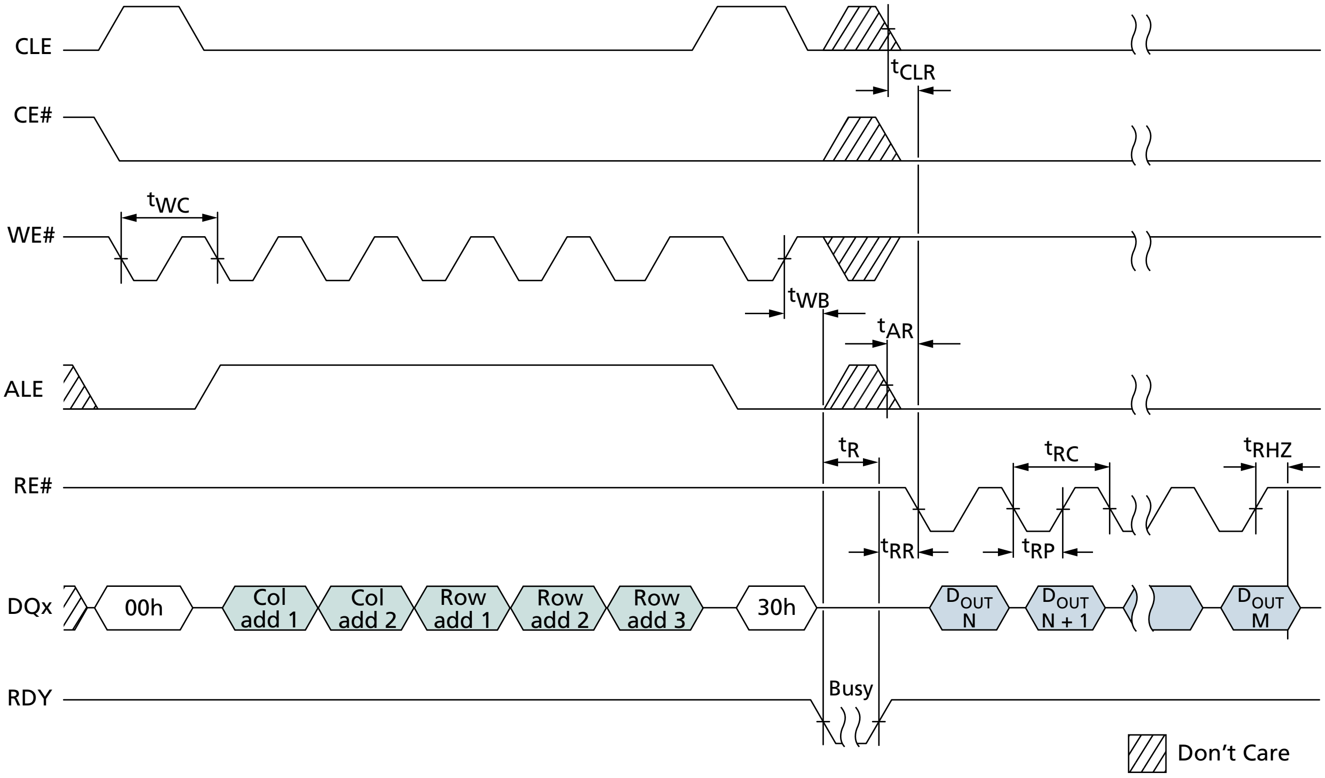


Figure 80: READ PAGE Operation with CE# "Don't Care"

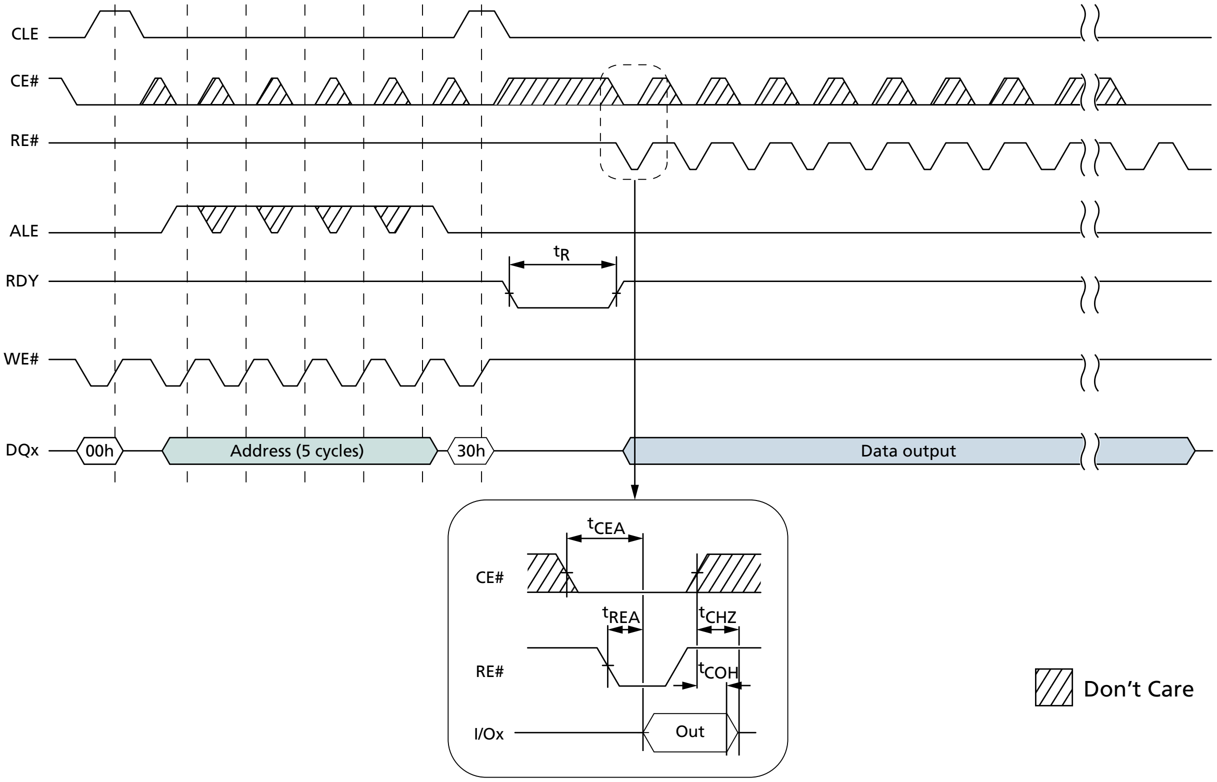


Figure 81: CHANGE READ COLUMN

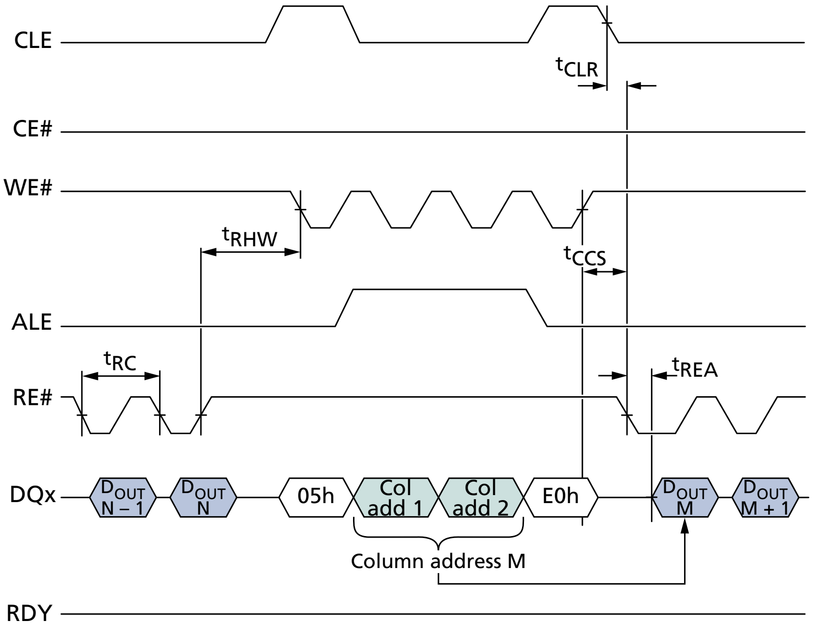


Figure 82: READ PAGE CACHE SEQUENTIAL

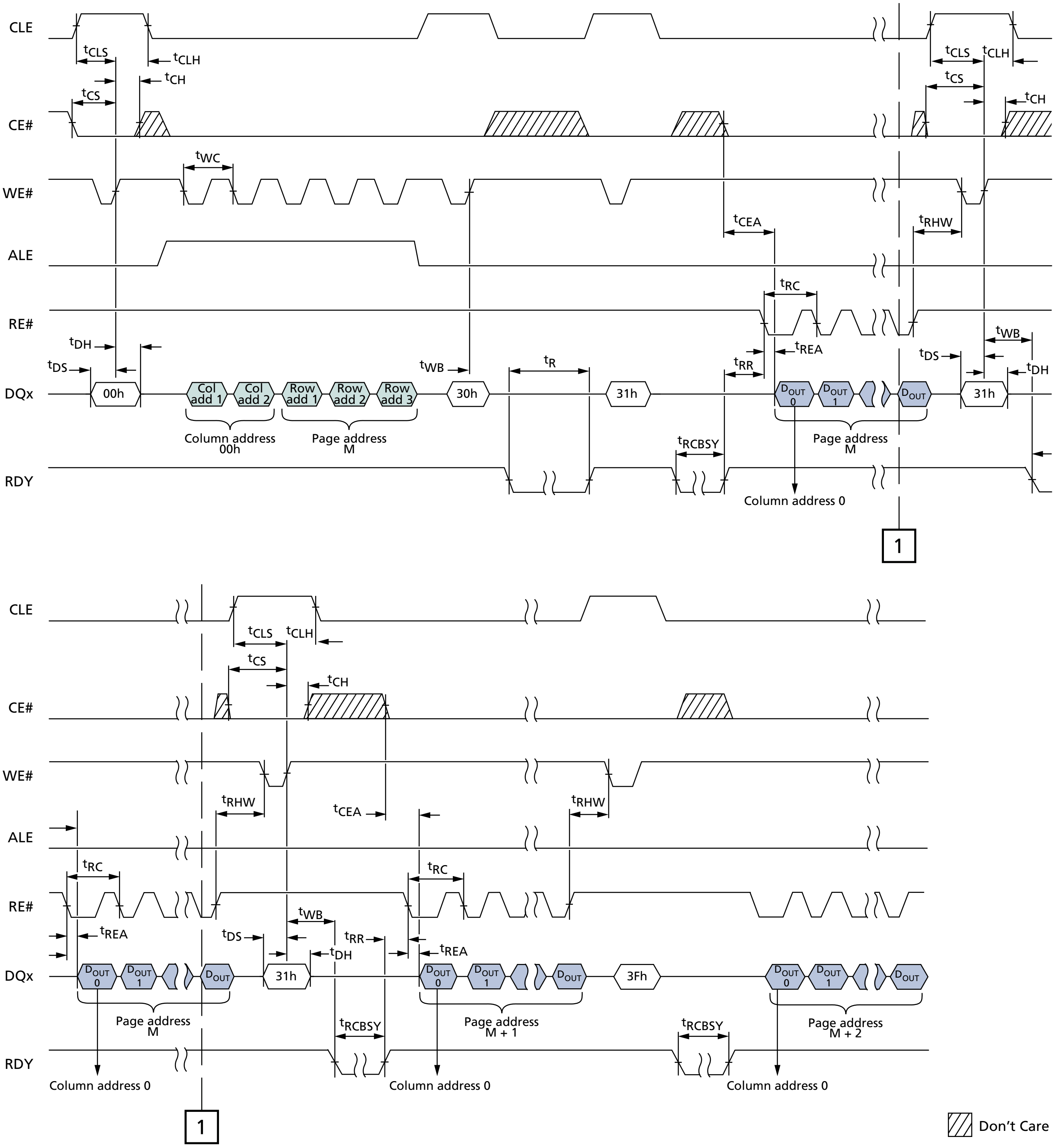


Figure 83: READ PAGE CACHE RANDOM

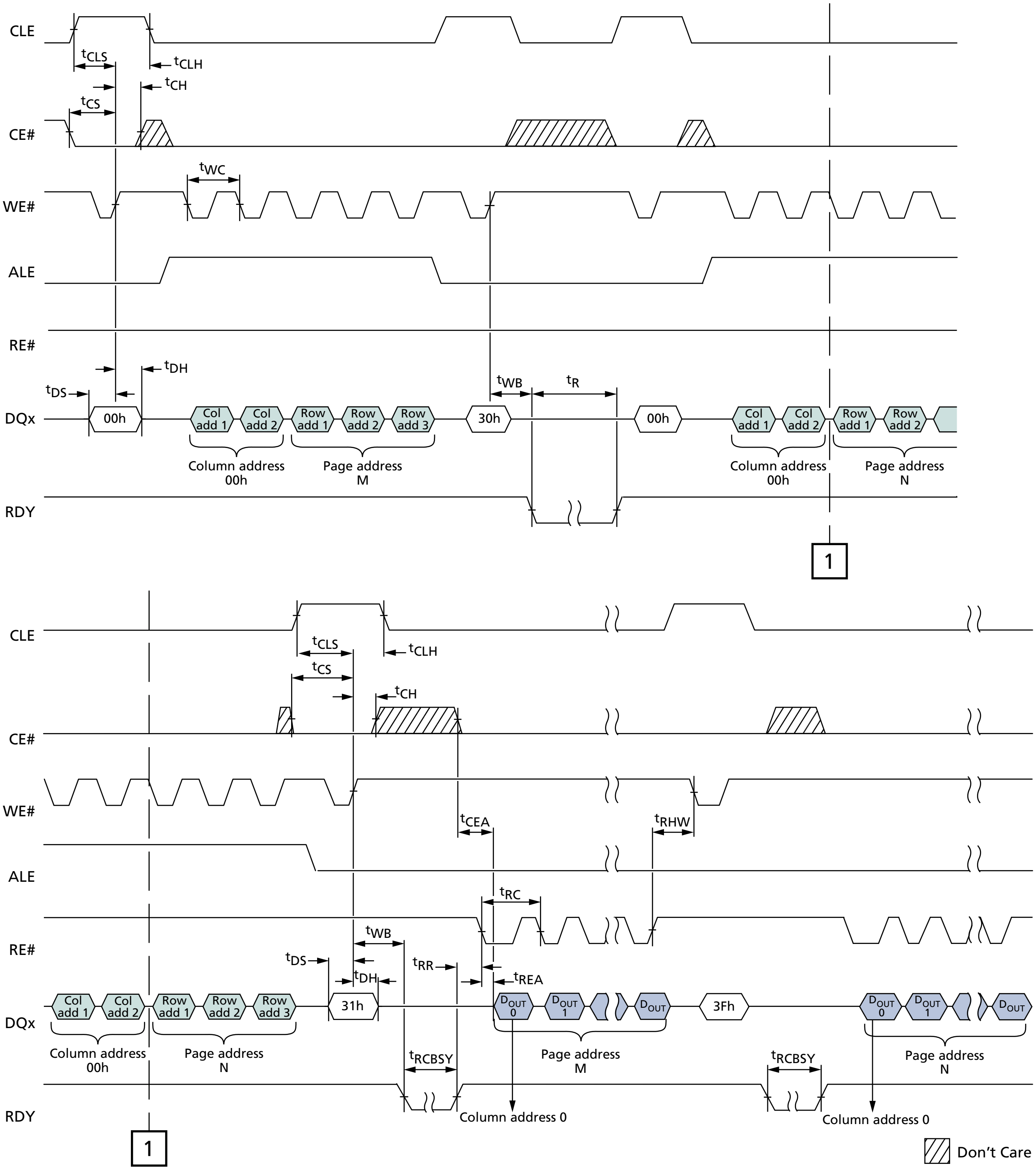


Figure 84: READ ID Operation

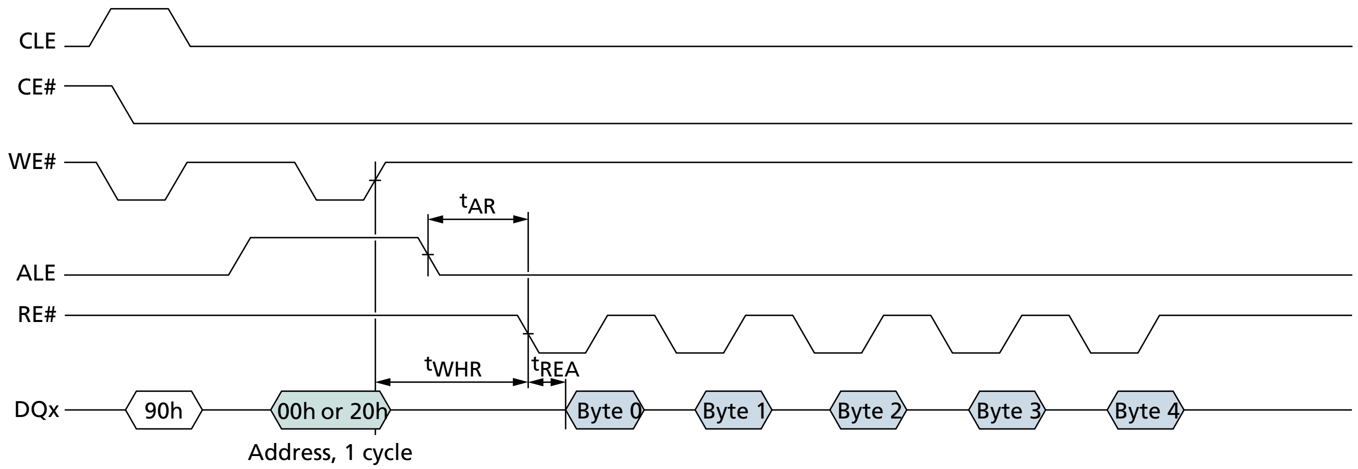


Figure 85: PROGRAM PAGE Operation

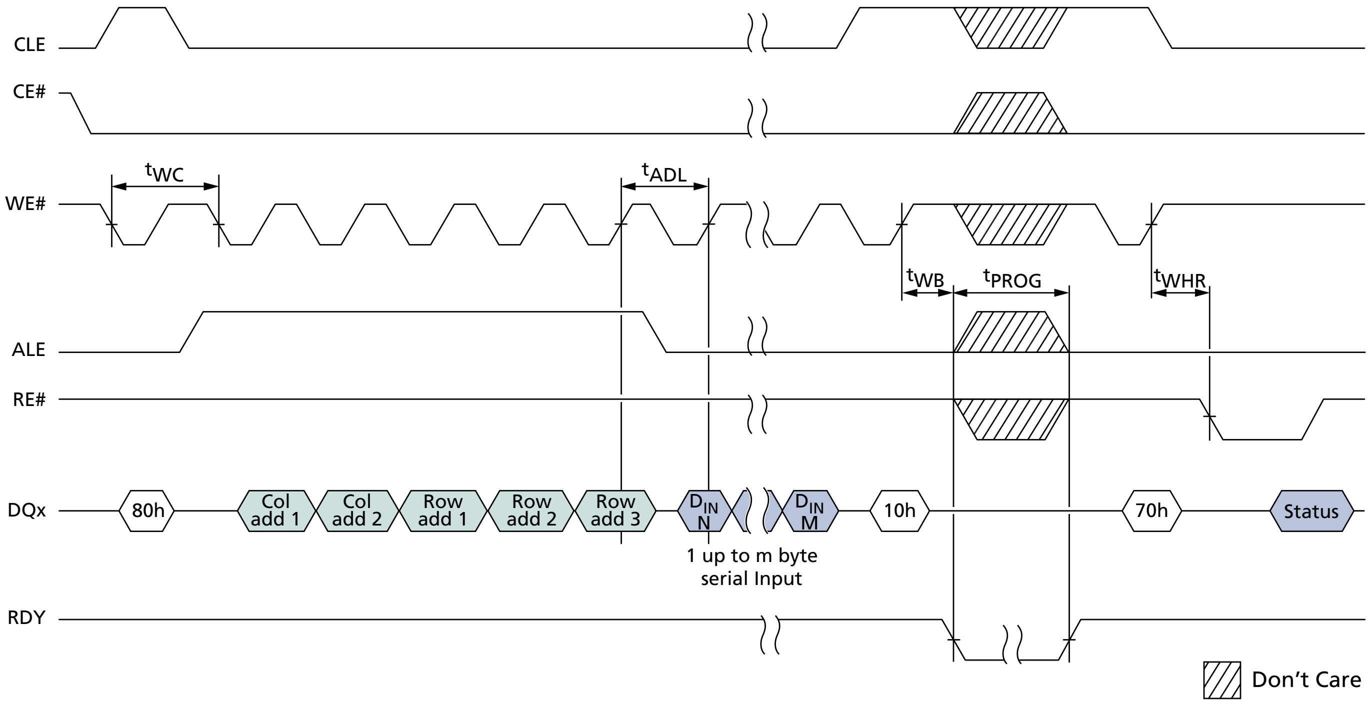


Figure 86: PROGRAM PAGE Operation with CE# “Don’t Care”

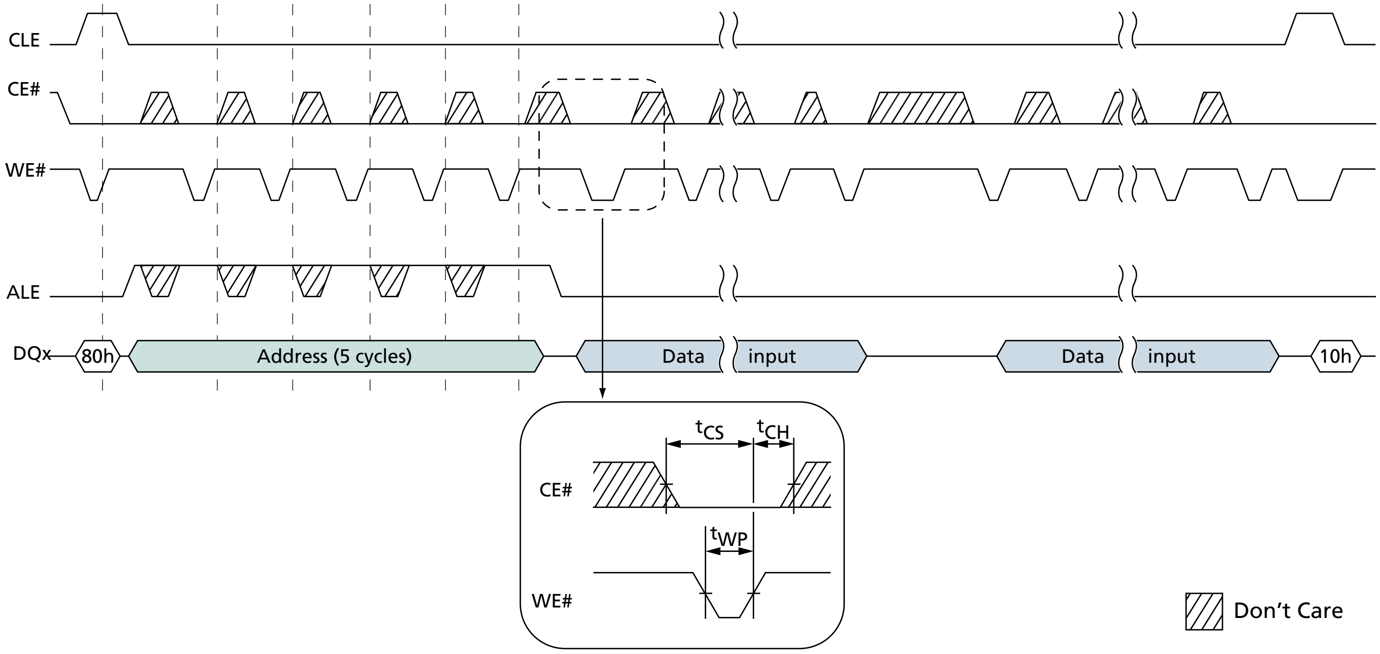


Figure 87: PROGRAM PAGE Operation with CHANGE WRITE COLUMN

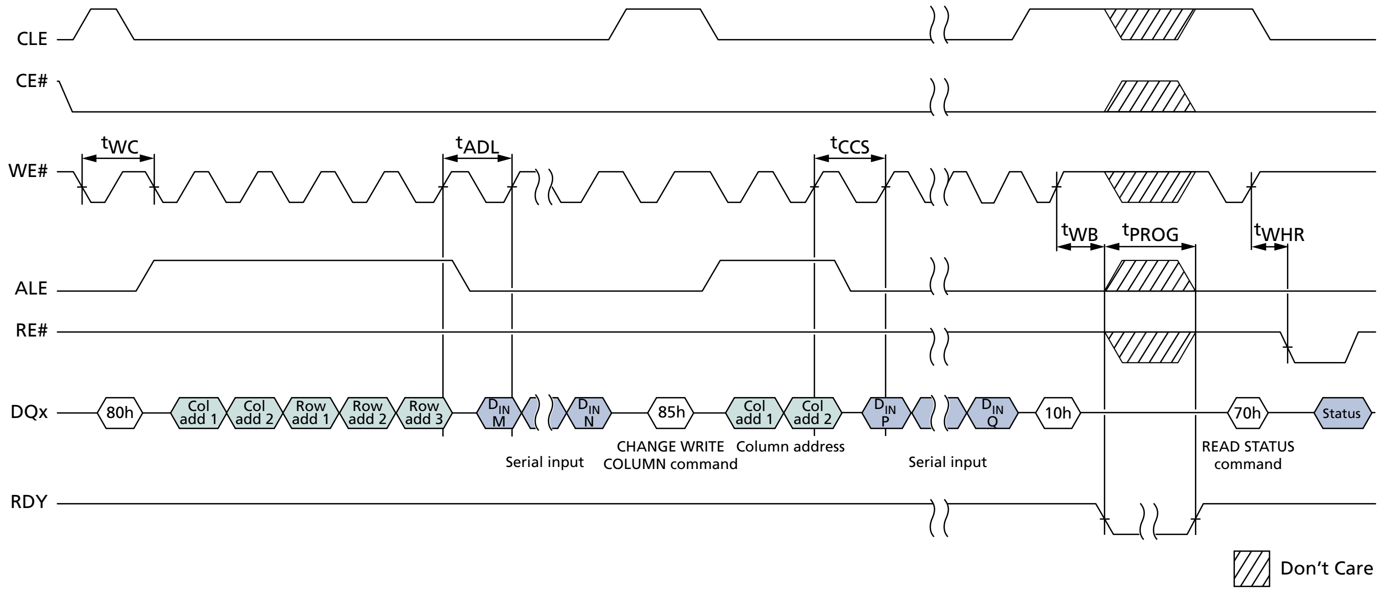


Figure 88: PROGRAM PAGE CACHE

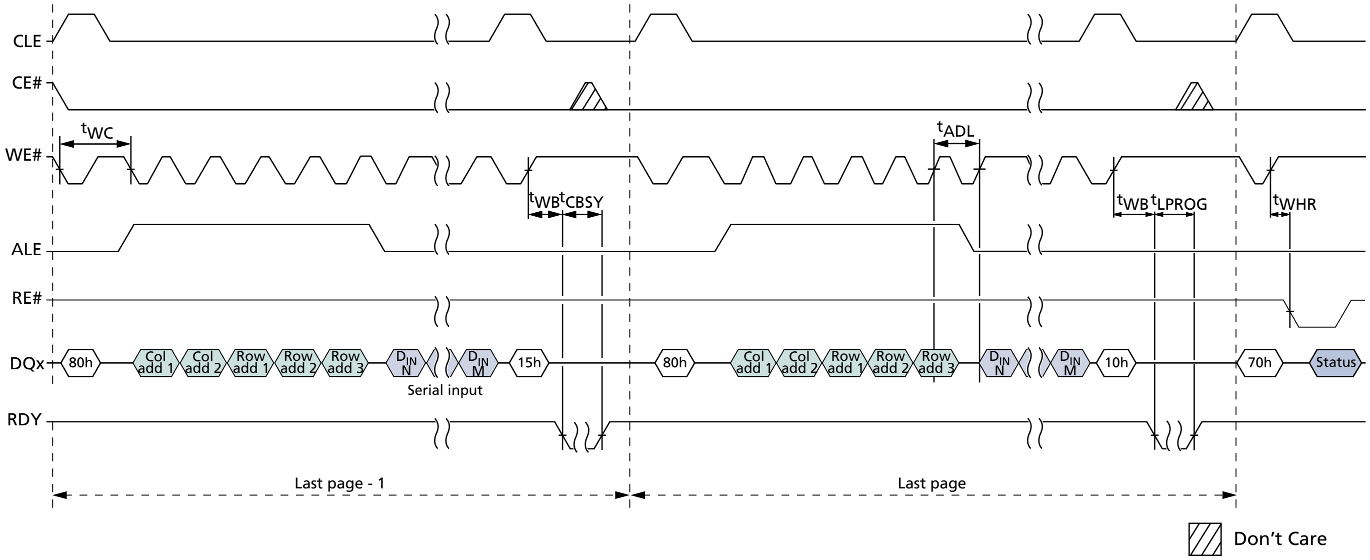
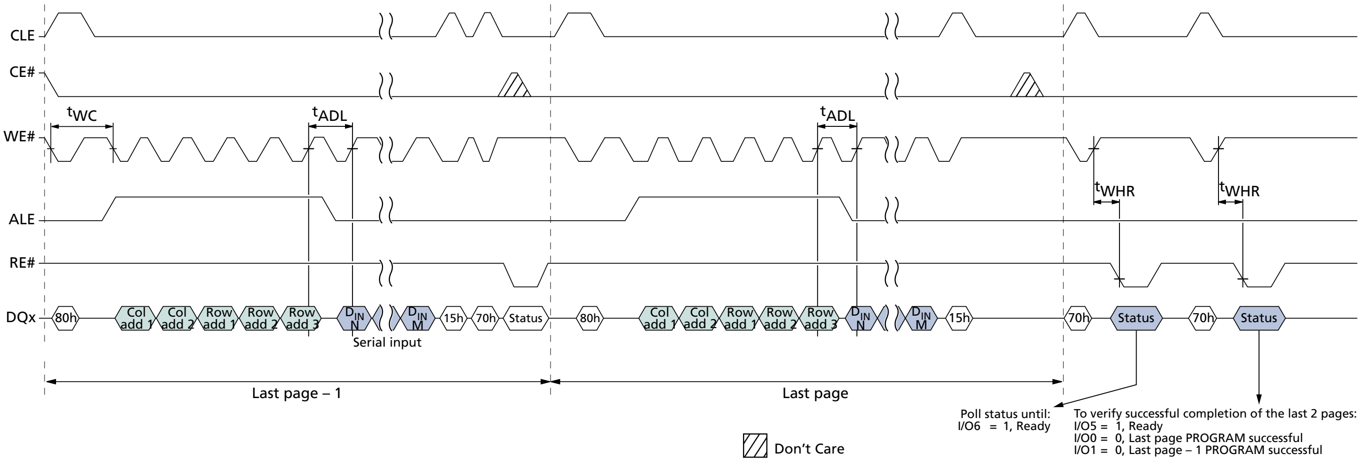


Figure 89: PROGRAM PAGE CACHE Ending on 15h



Poll status until:
I/O6 = 1, Ready

To verify successful completion of the last 2 pages:
I/O5 = 1, Ready
I/O0 = 0, Last page PROGRAM successful
I/O1 = 0, Last page – 1 PROGRAM successful

Figure 90: COPYBACK

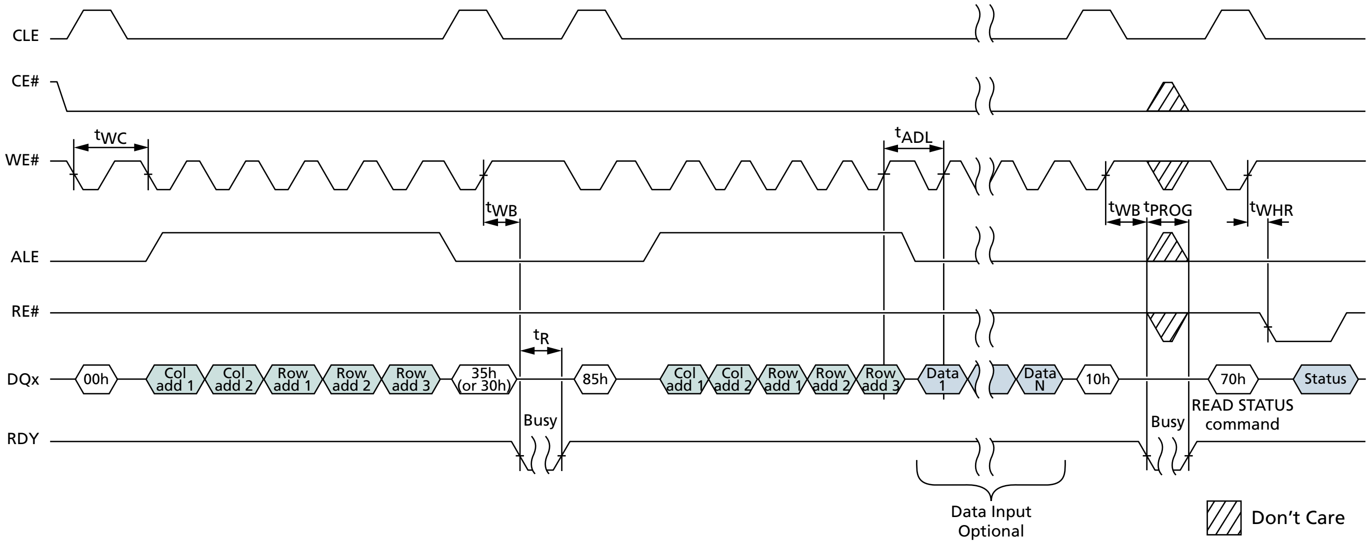
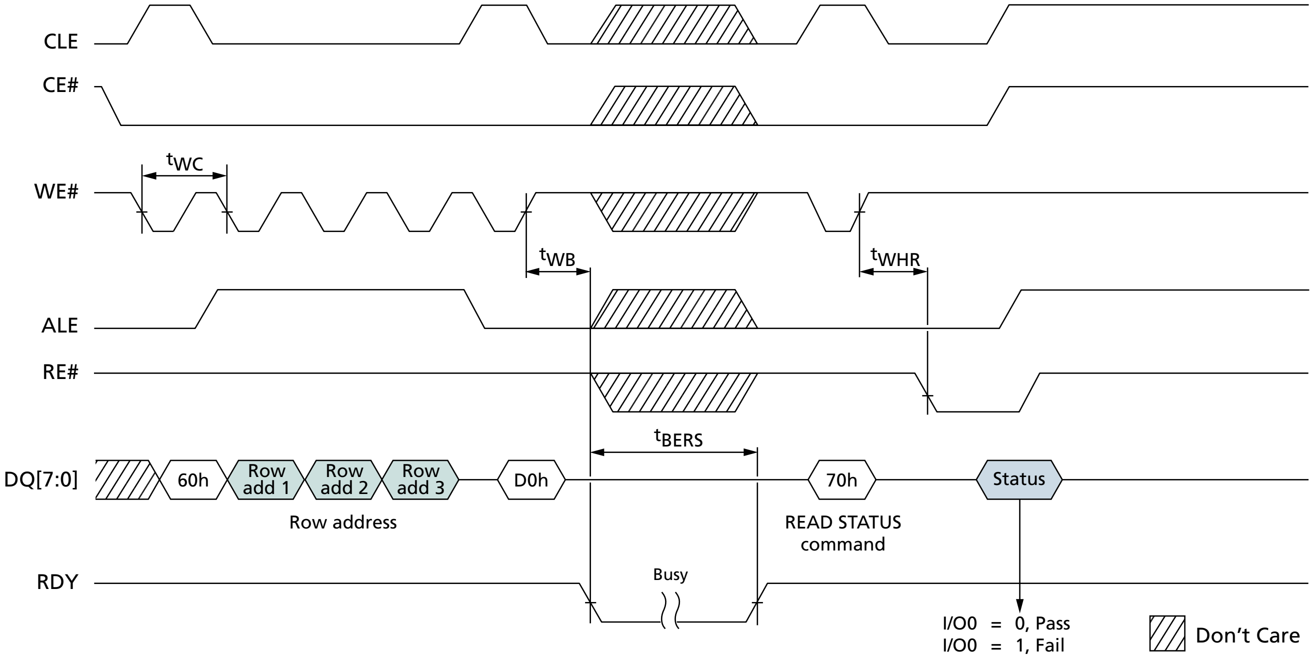
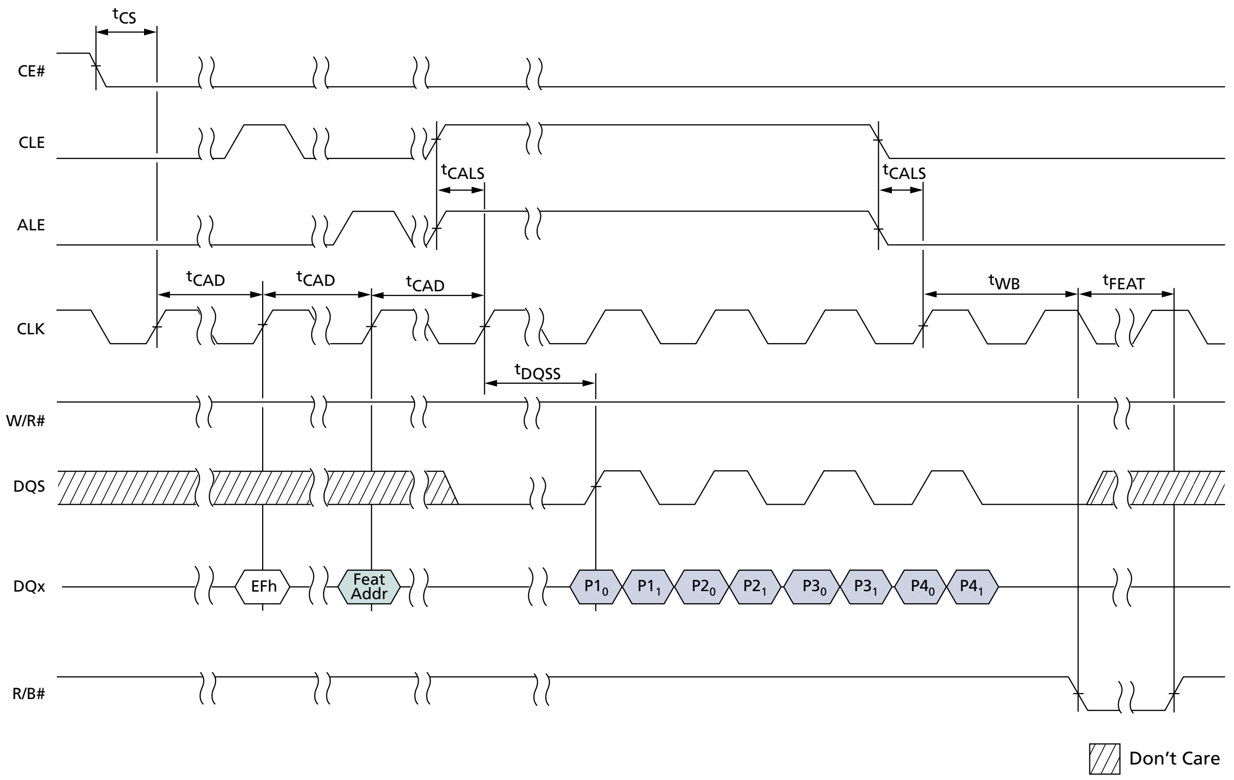


Figure 91: ERASE BLOCK Operation



Synchronous Interface Timing Diagrams

Figure 92: SET FEATURES Operation



Notes:

1. When CE# remains LOW, ^{t}CAD begins at the rising edge of the clock from which the last data byte is input for the subsequent command or data input cycle(s).
2. ^{t}DSH (MIN) generally occurs during ^{t}DQSS (MIN).
3. ^{t}DSS (MIN) generally occurs during ^{t}DQSS (MAX).
4. The cycle that ^{t}CAD is measured from may be an idle cycle (as shown), another command cycle, an address cycle, or a data cycle. The idle cycle is shown in this diagram for simplicity.

Figure 93: READ ID Operation

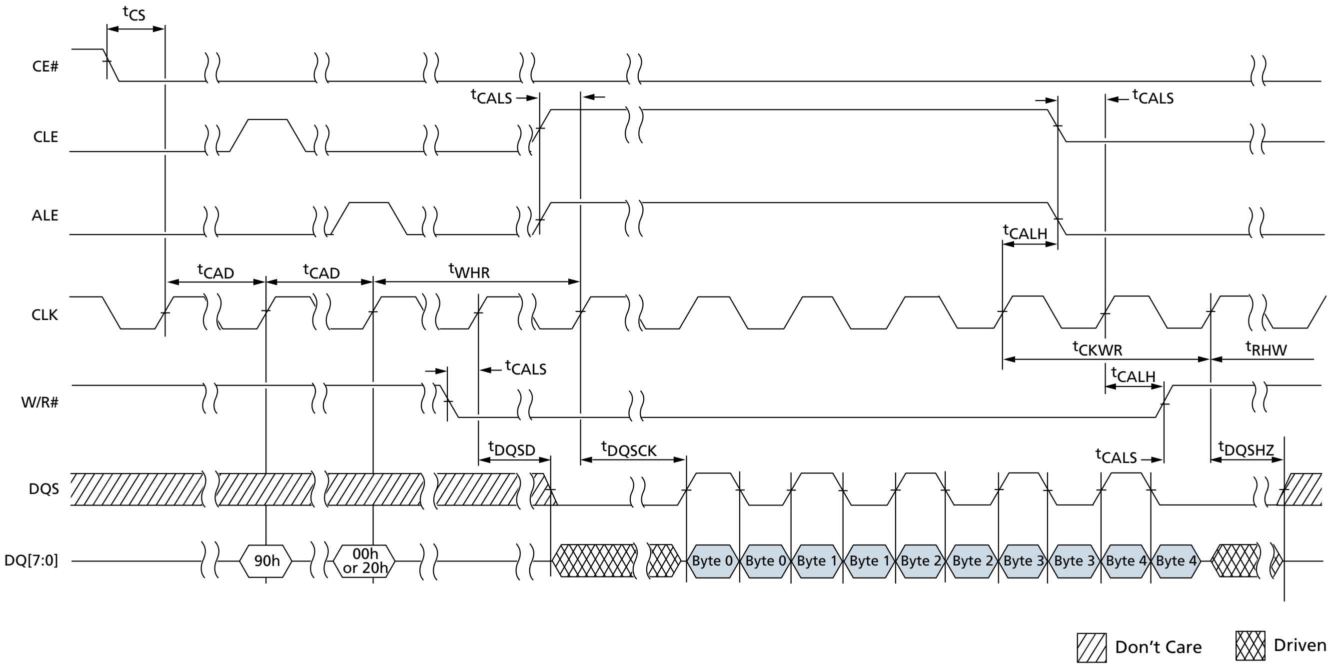


Figure 94: GET FEATURES Operation

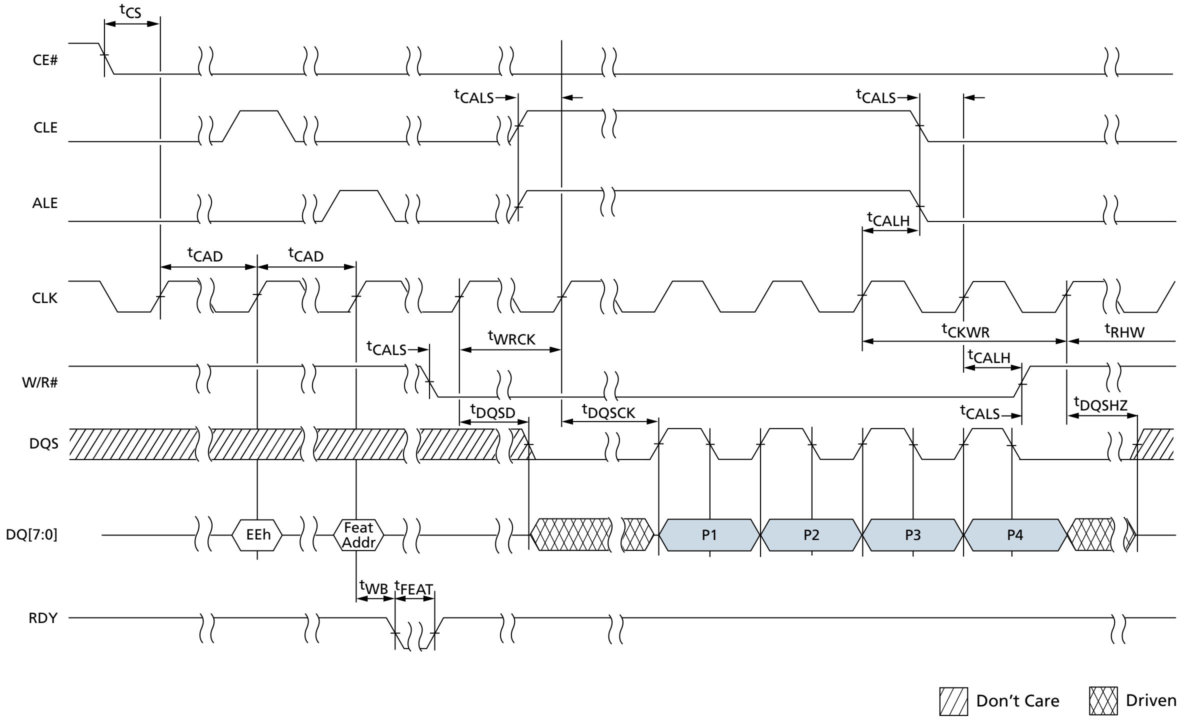


Figure 95: RESET (FCh) Operation

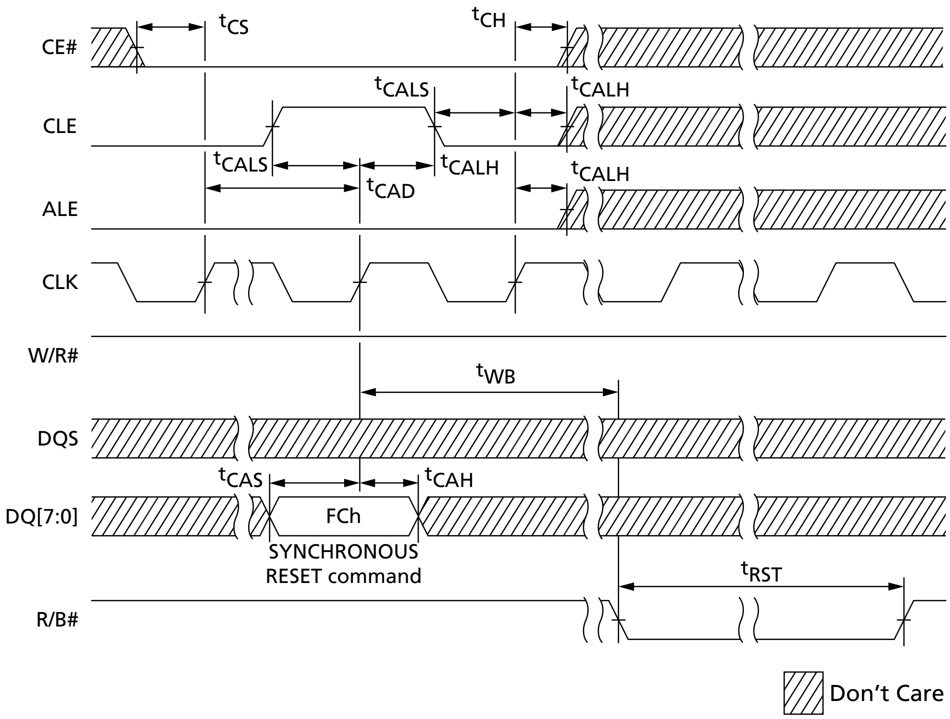


Figure 96: READ STATUS Cycle

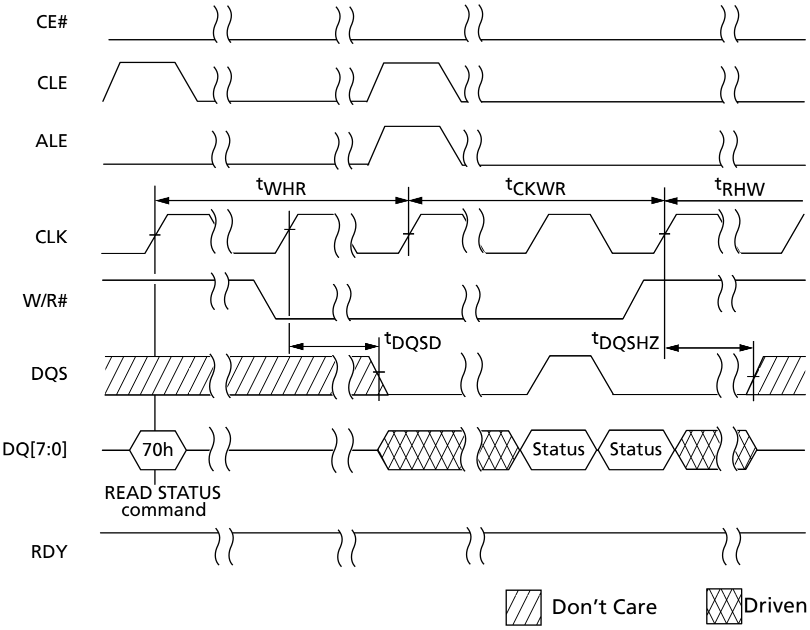


Figure 97: READ STATUS ENHANCED Operation

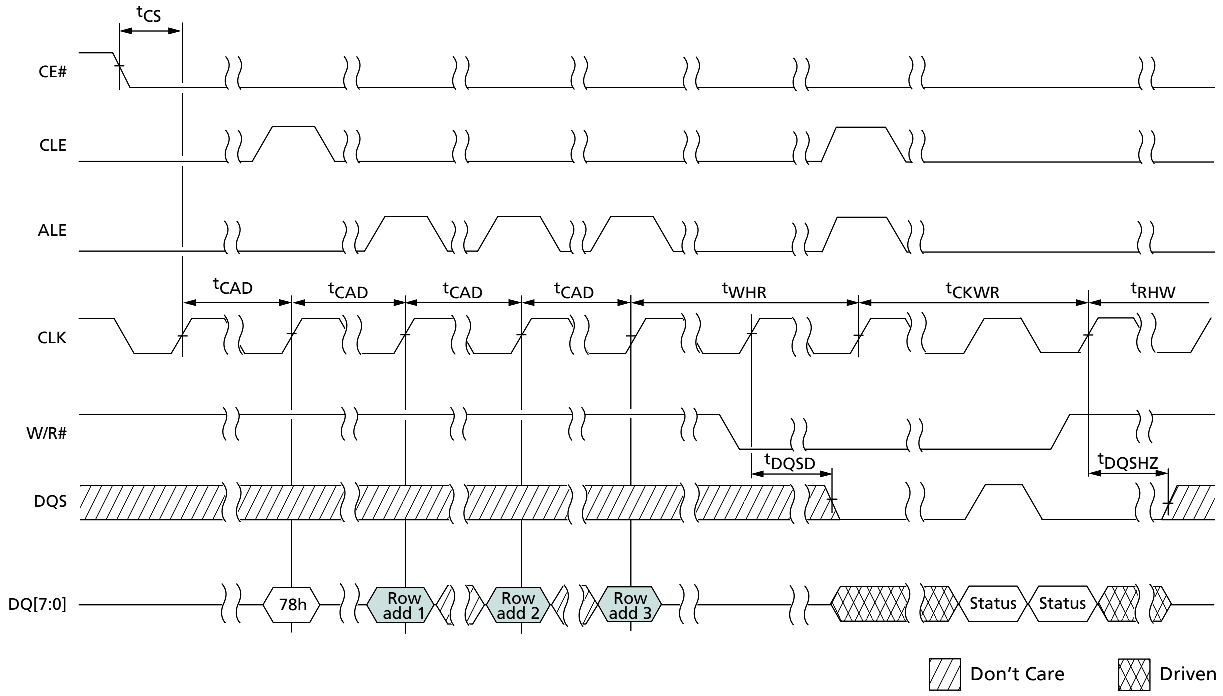


Figure 98: READ PARAMETER PAGE Operation

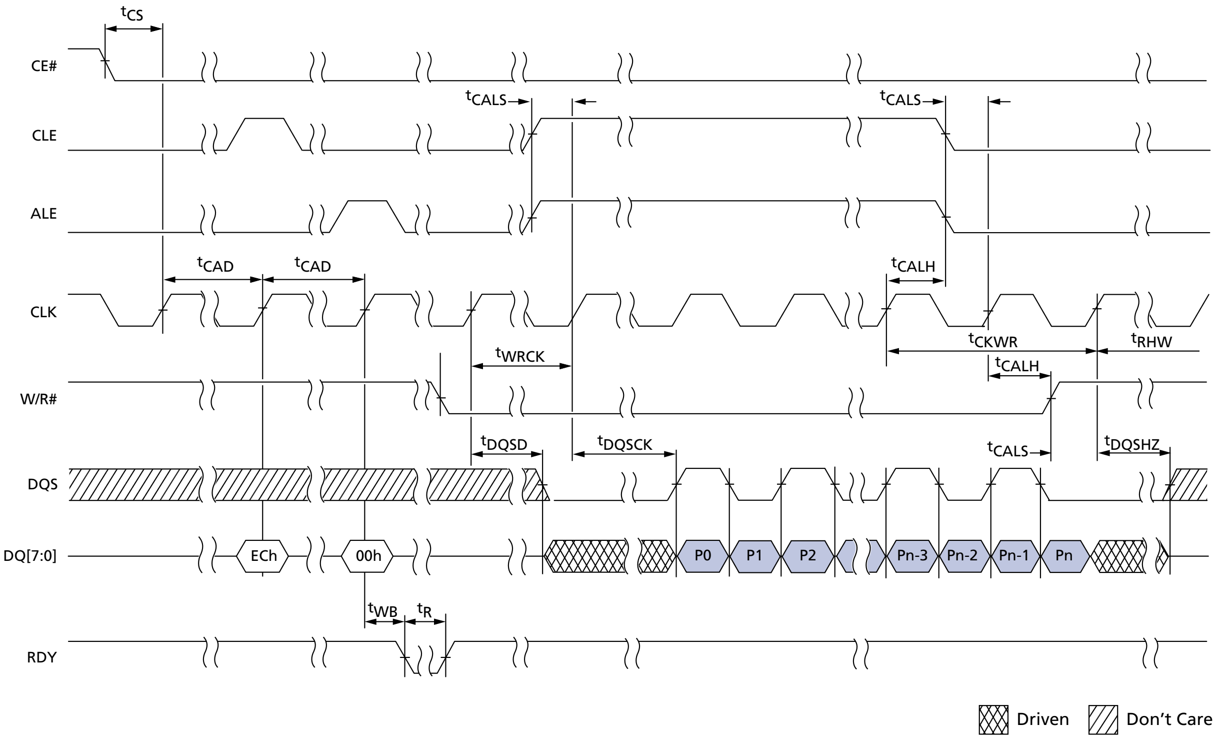


Figure 99: READ PAGE Operation

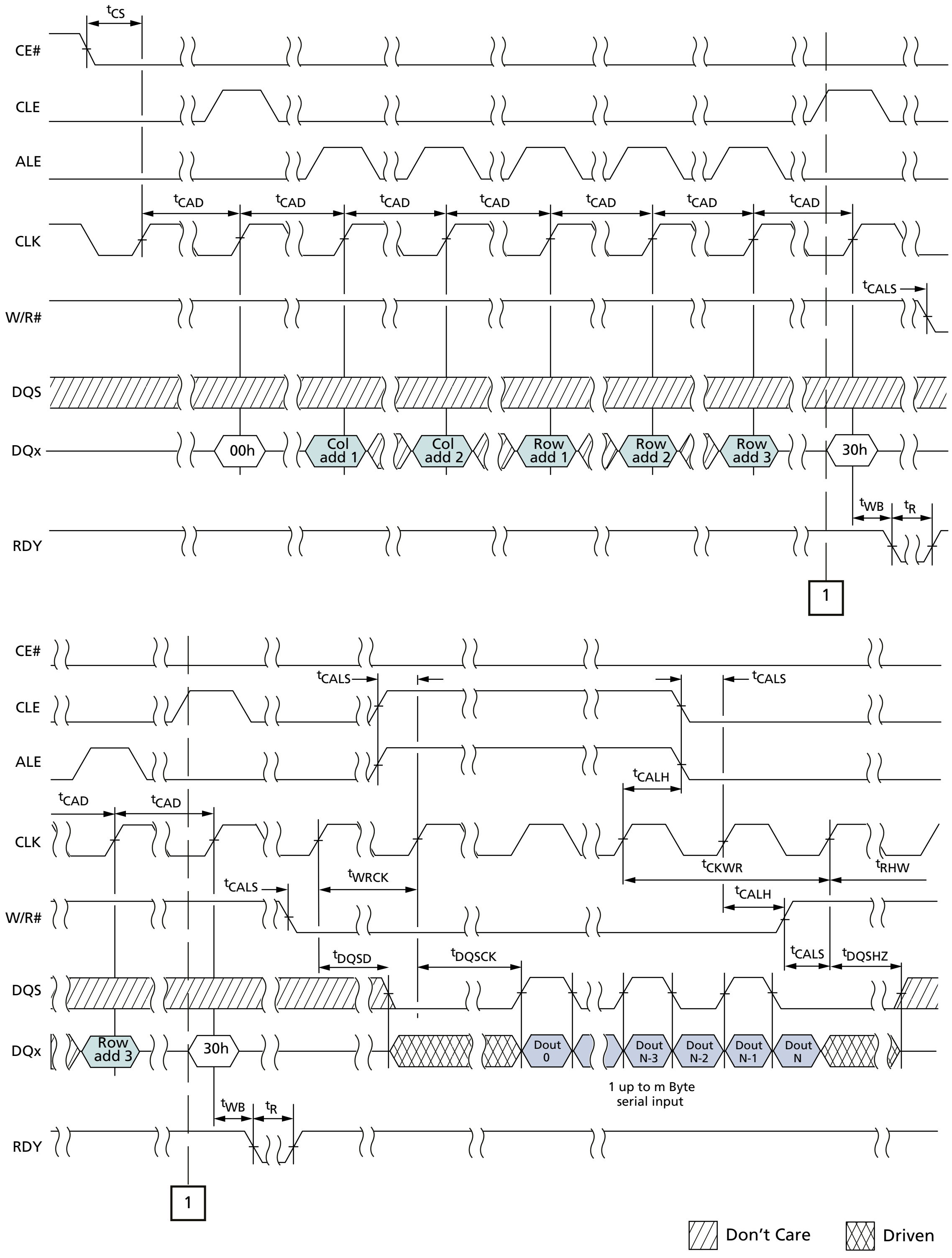


Figure 100: CHANGE READ COLUMN

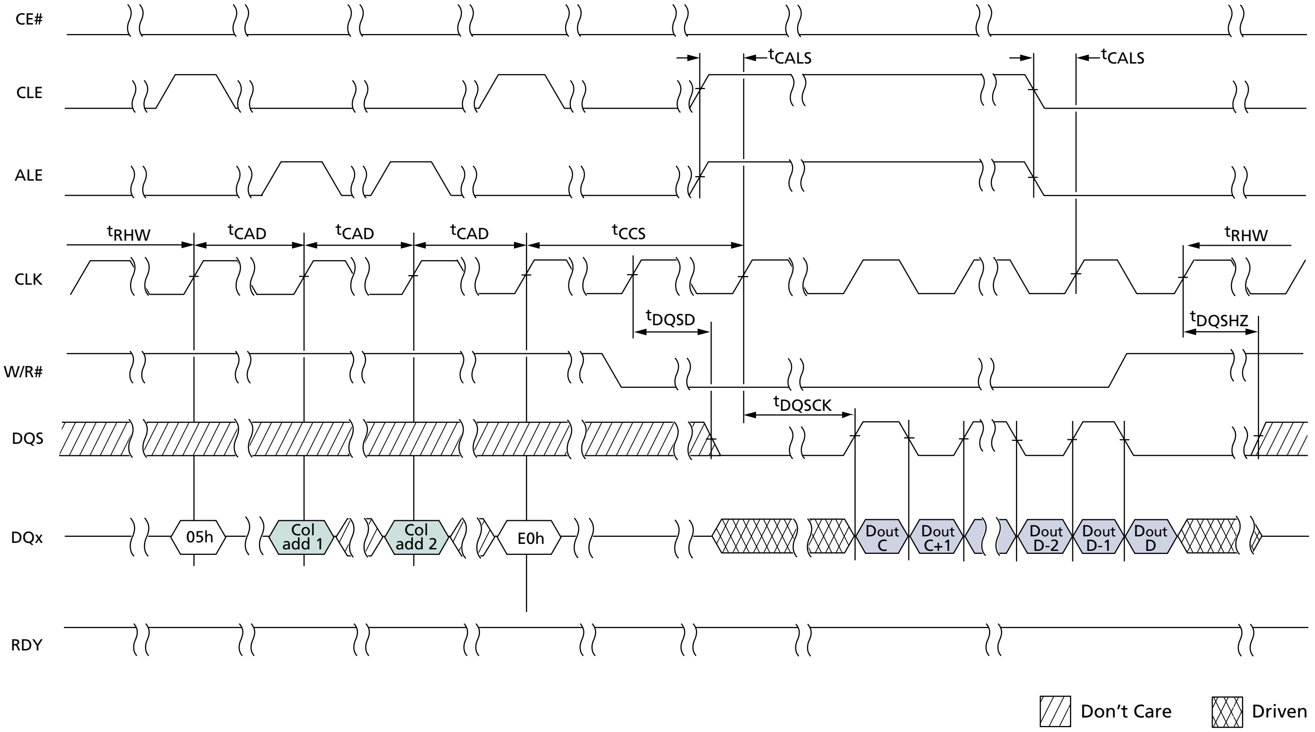


Figure 101: READ PAGE CACHE SEQUENTIAL (1 of 2)

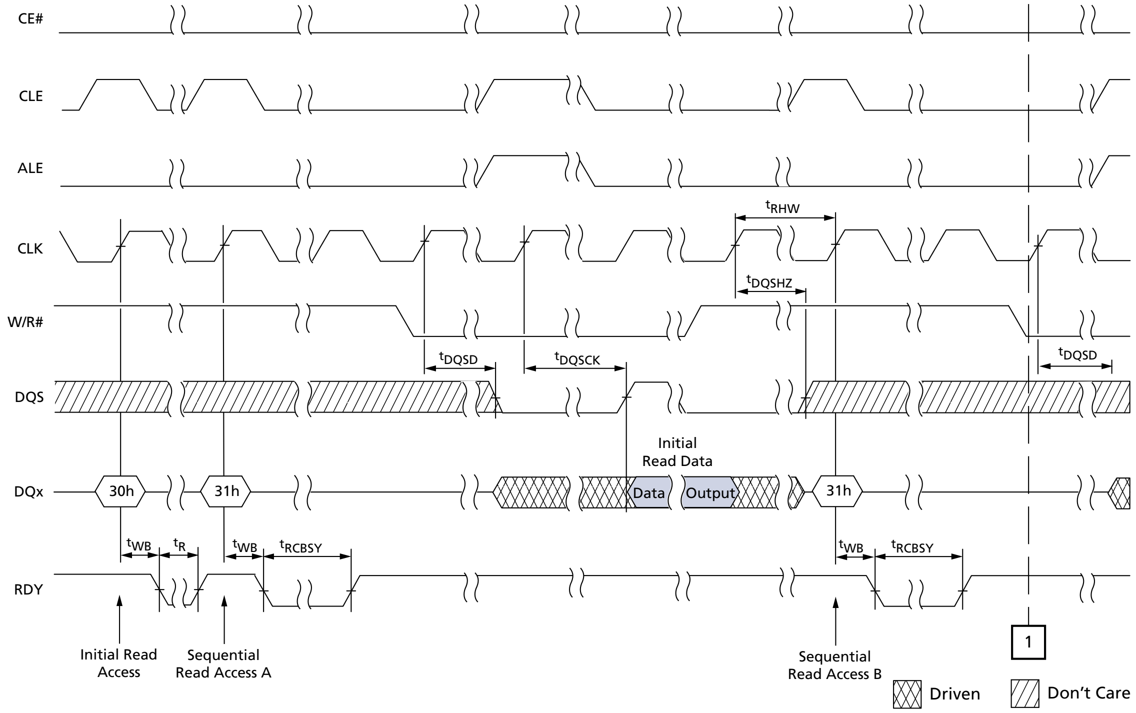


Figure 102: READ PAGE CACHE SEQUENTIAL (2 of 2)

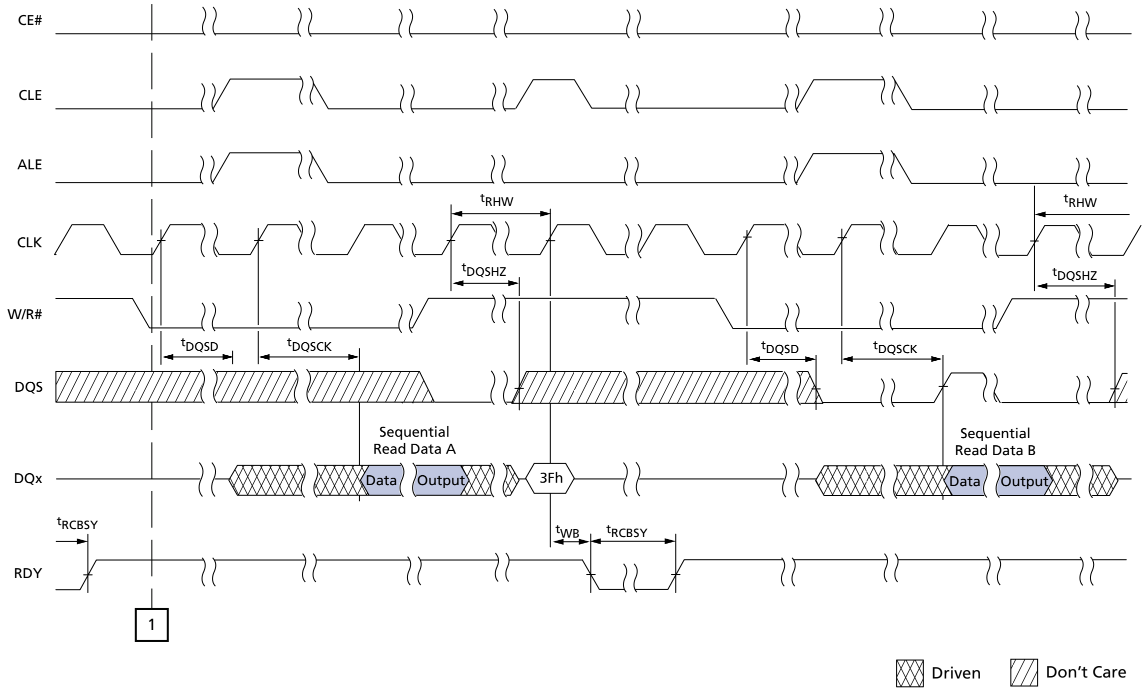


Figure 103: READ PAGE CACHE RANDOM (1 of 2)

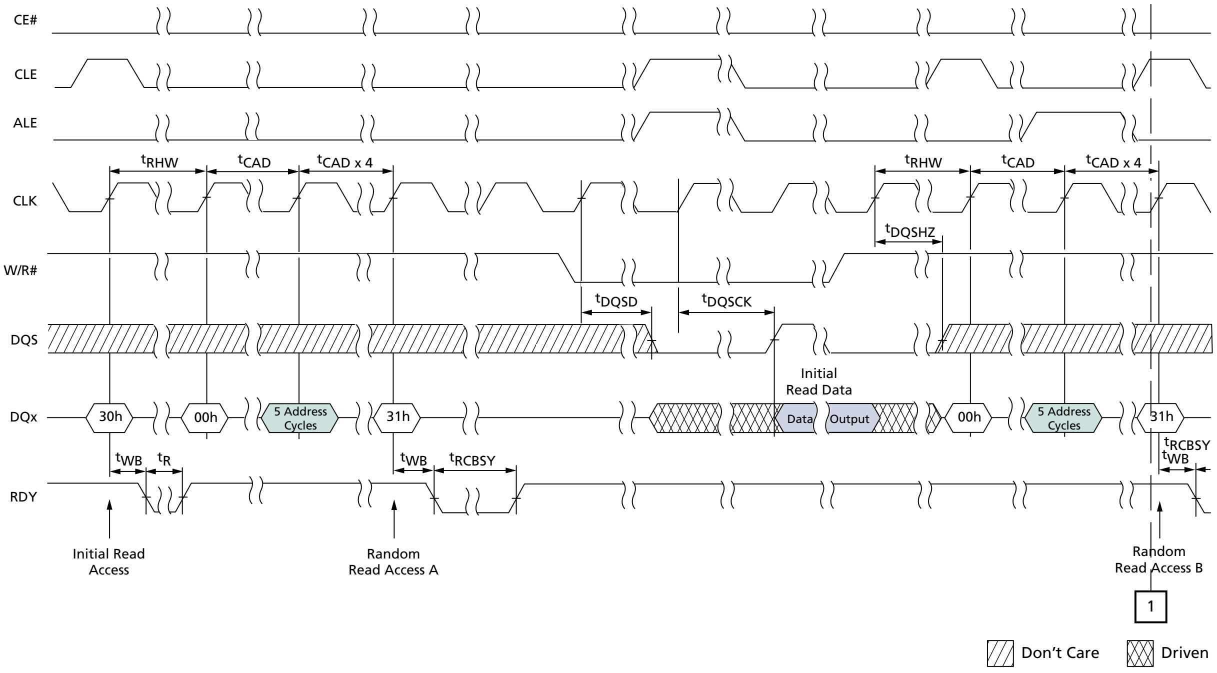


Figure 104: READ PAGE CACHE RANDOM (2 of 2)

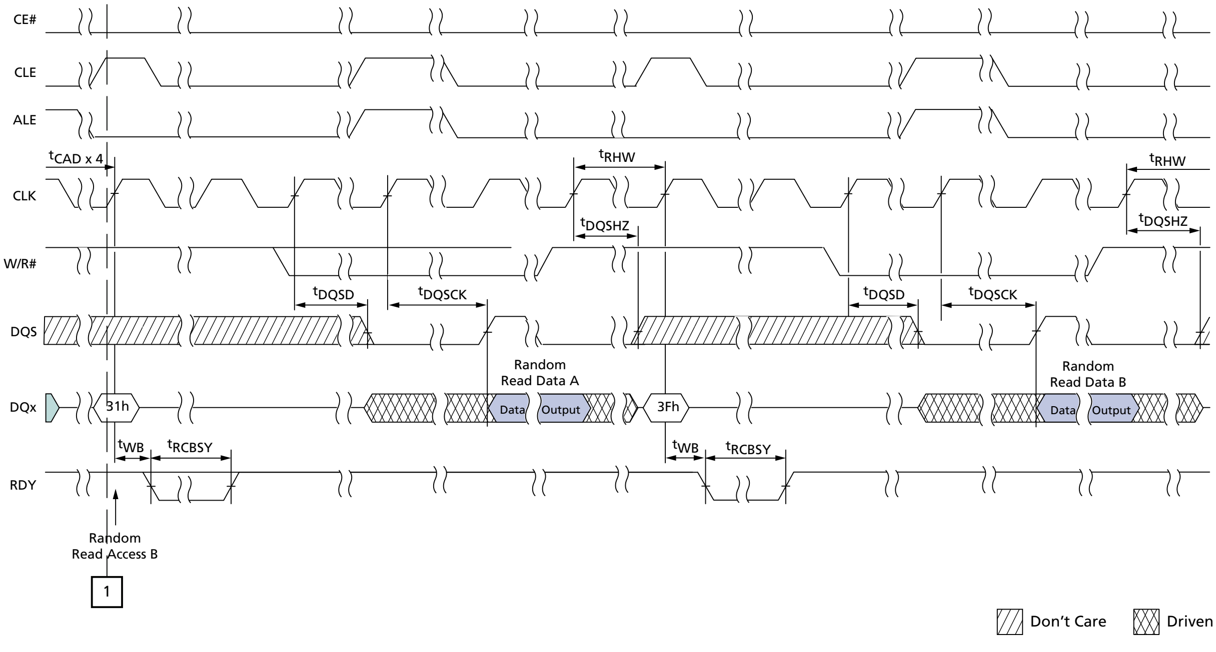
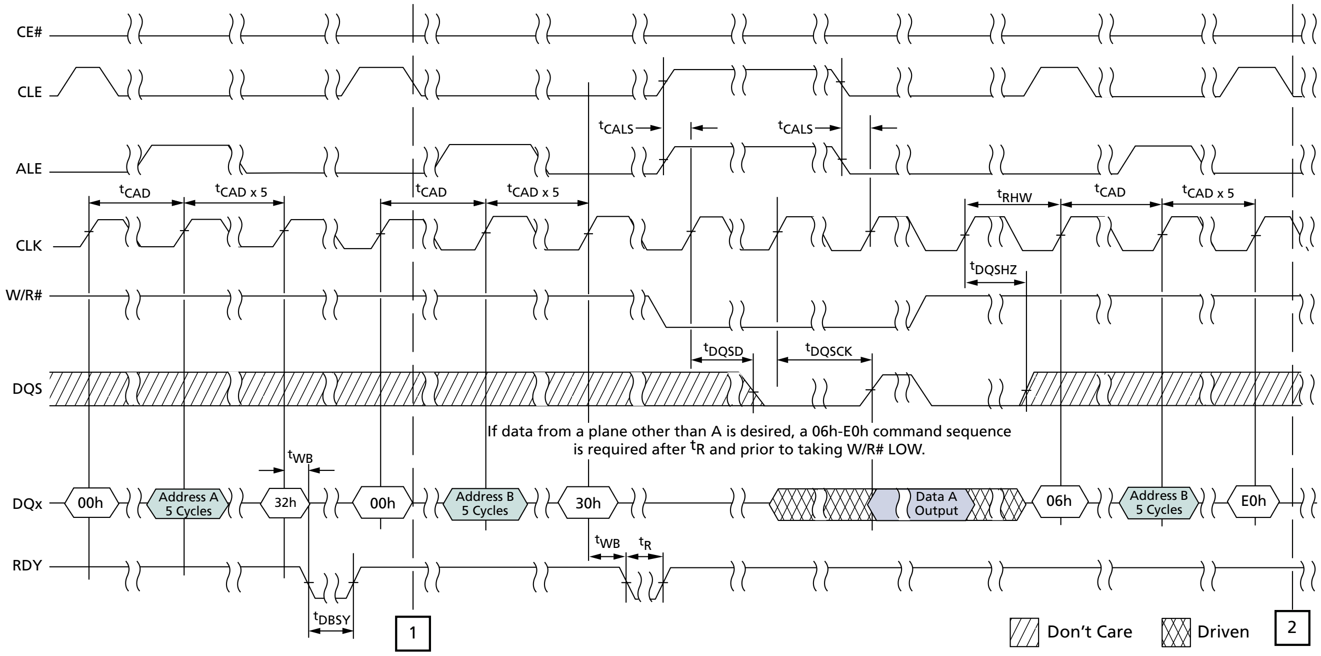


Figure 105: Multi-Plane Read Page (1 of 2)



If data from a plane other than A is desired, a 06h-E0h command sequence is required after tR and prior to taking W/R# LOW.

Figure 106: Multi-Plane Read Page (2 of 2)

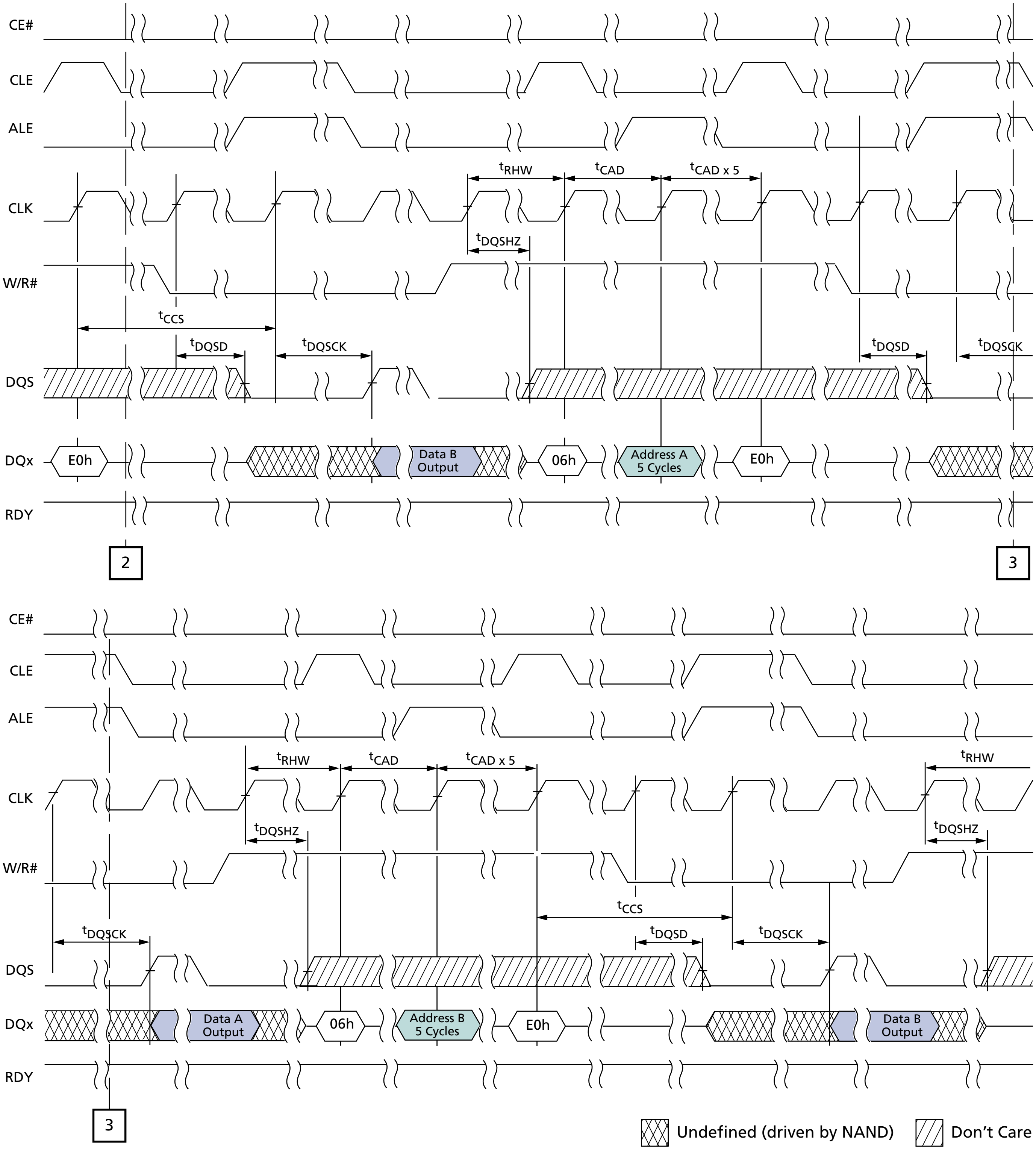


Figure 107: PROGRAM PAGE Operation (1 of 2)

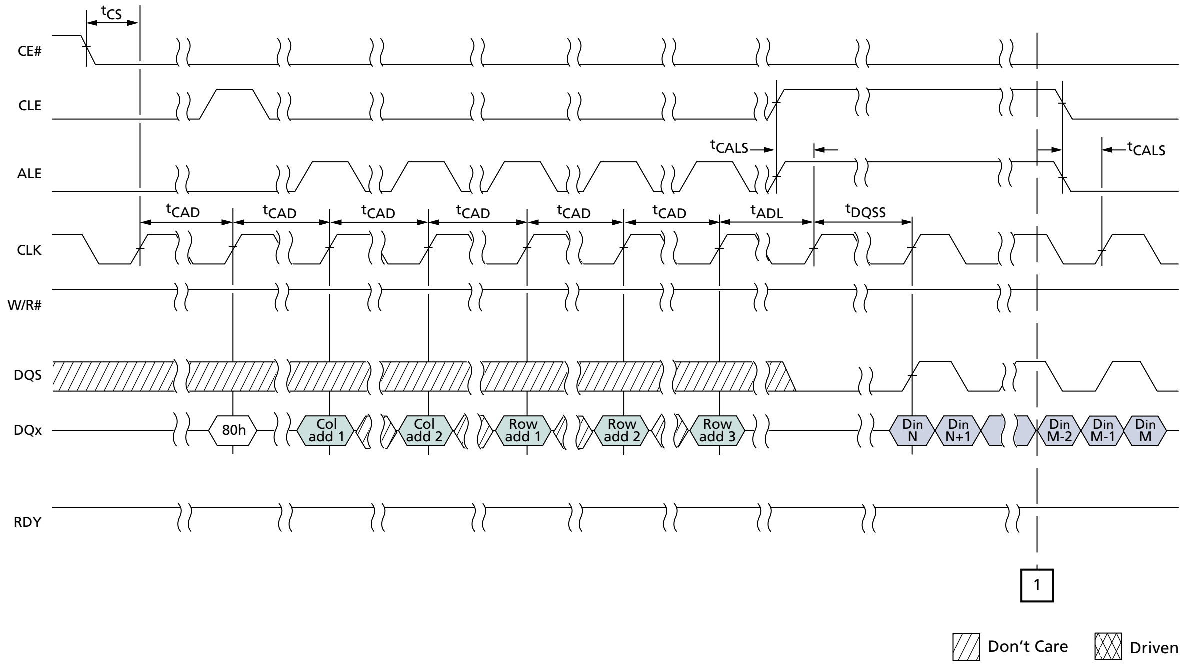


Figure 108: PROGRAM PAGE Operation (2 of 2)

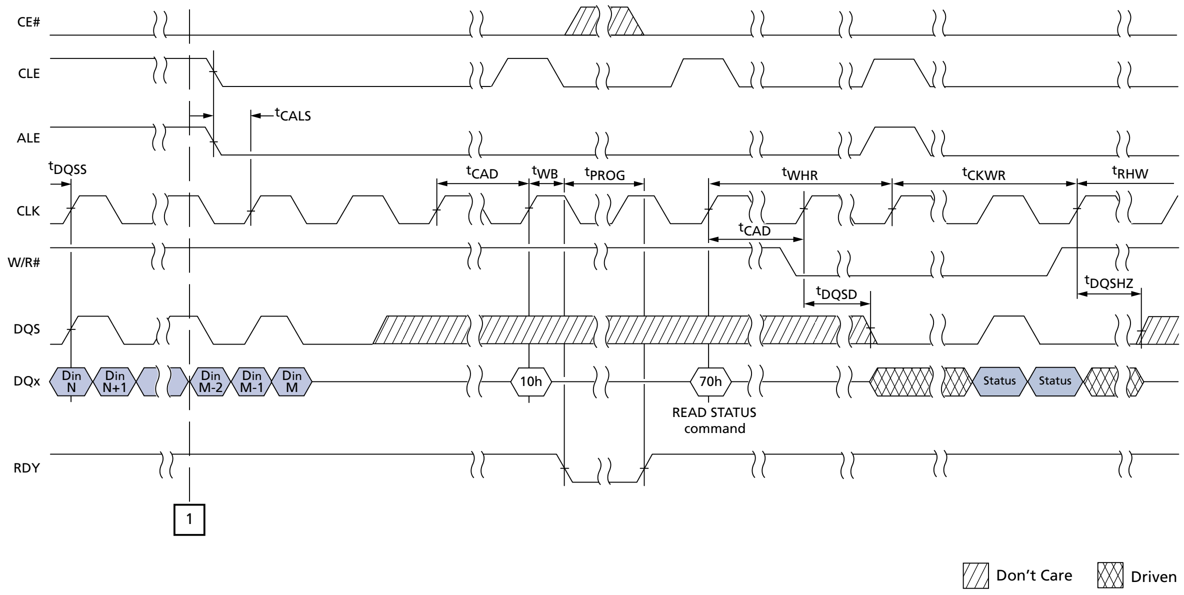


Figure 109: CHANGE WRITE COLUMN

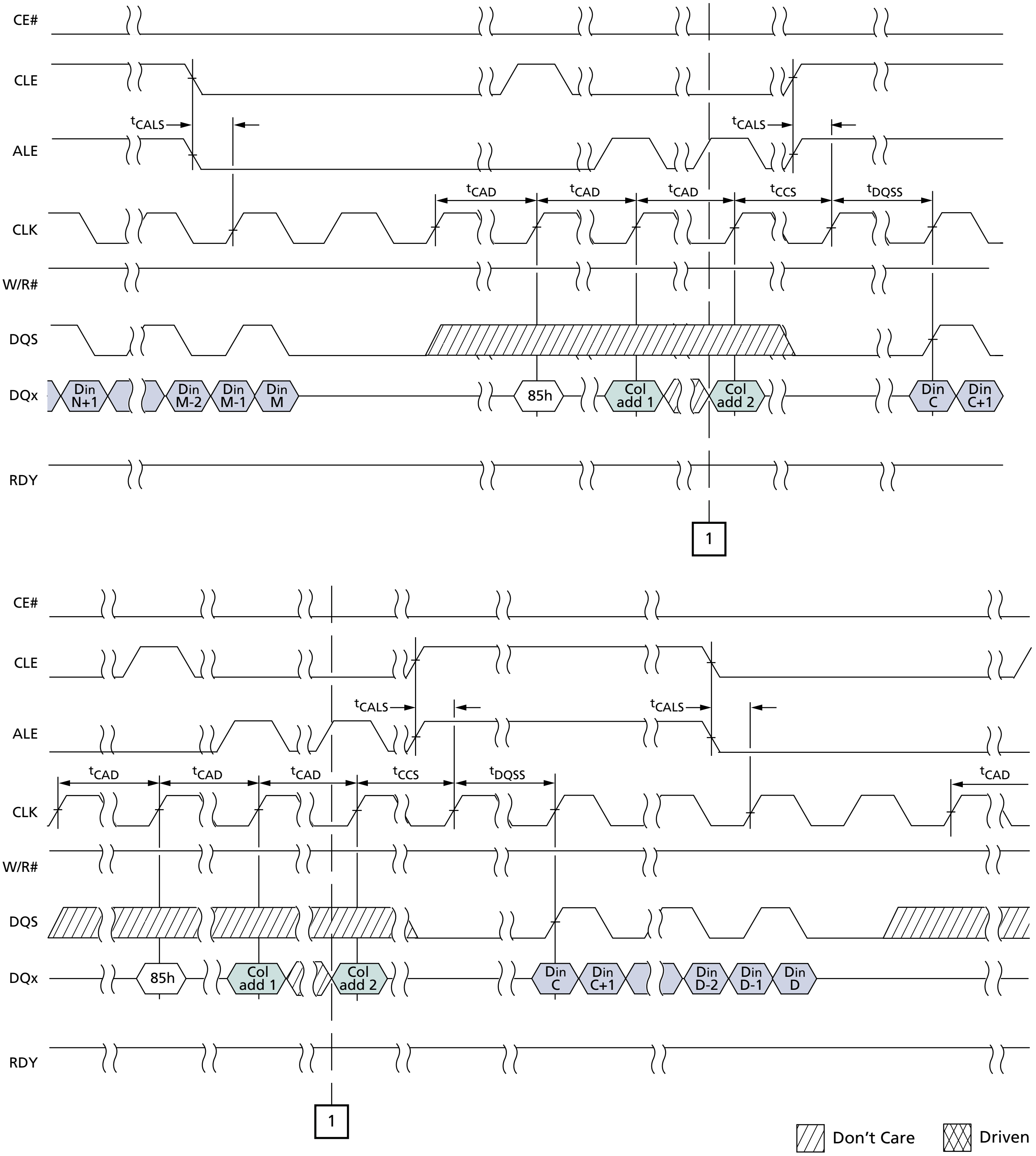


Figure 110: Multi-Plane Program Page

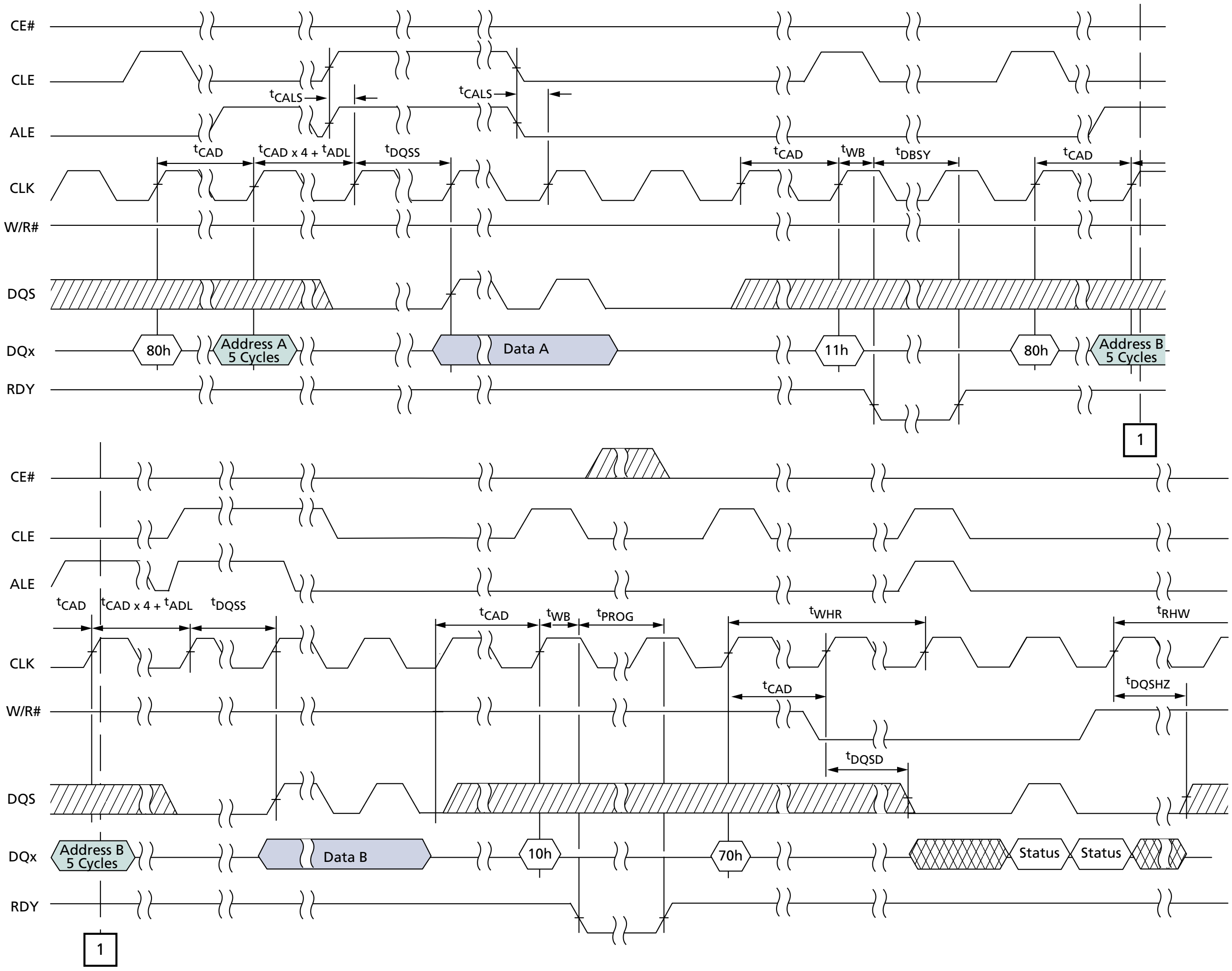


Figure 111: ERASE BLOCK

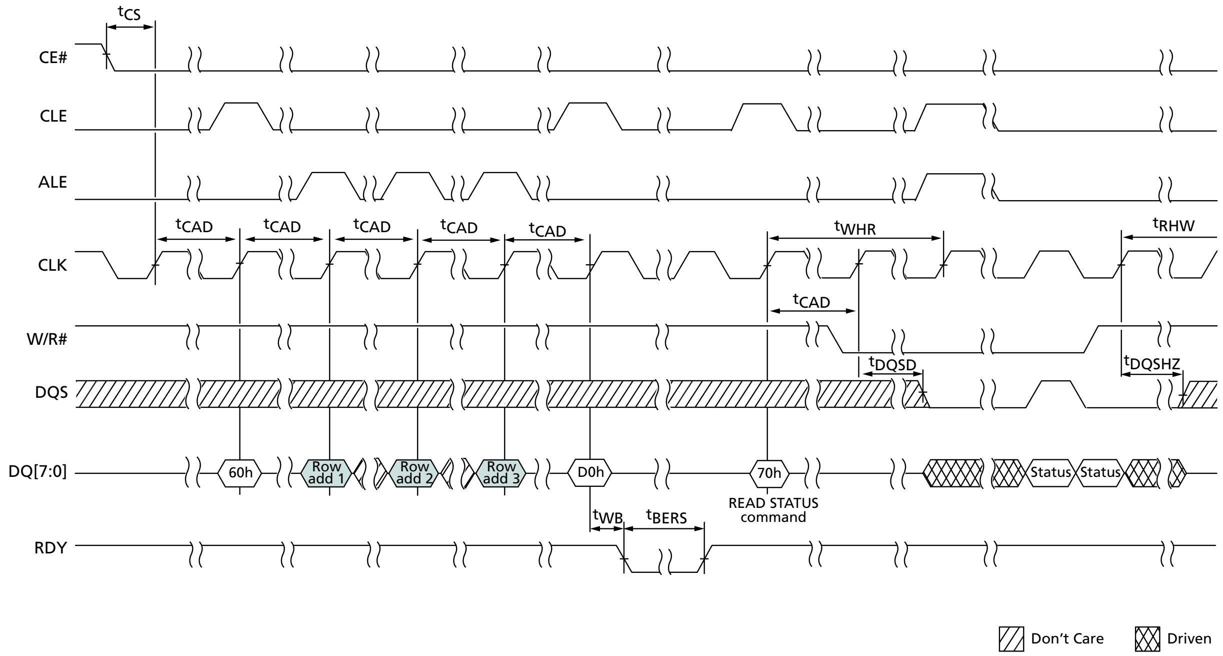


Figure 112: COPYBACK (1 of 3)

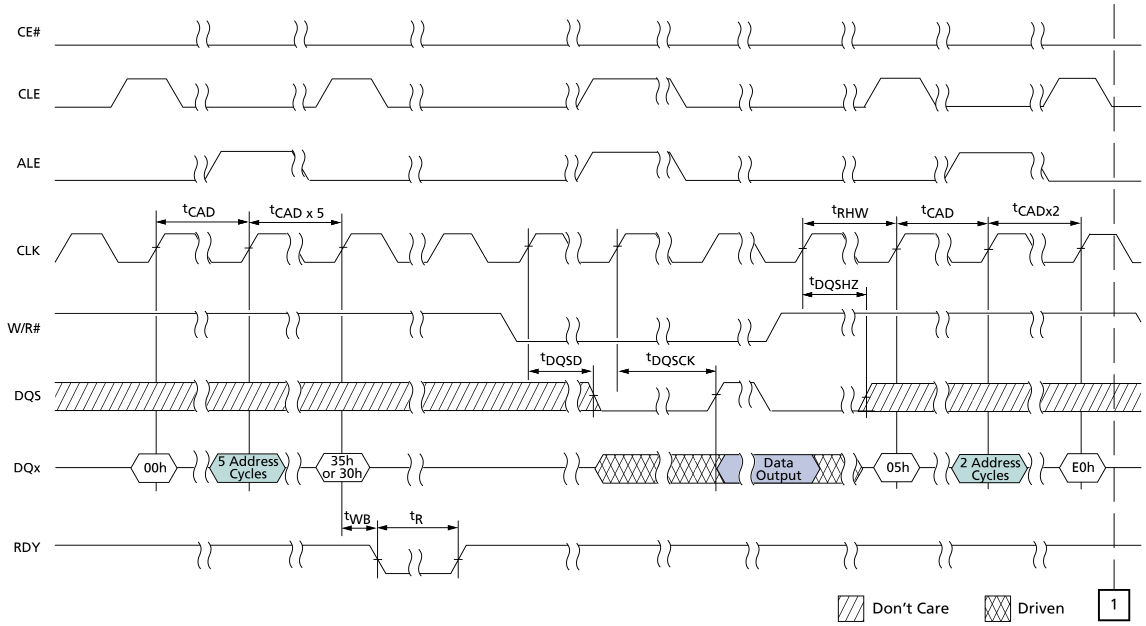


Figure 113: COPYBACK (2 of 3)

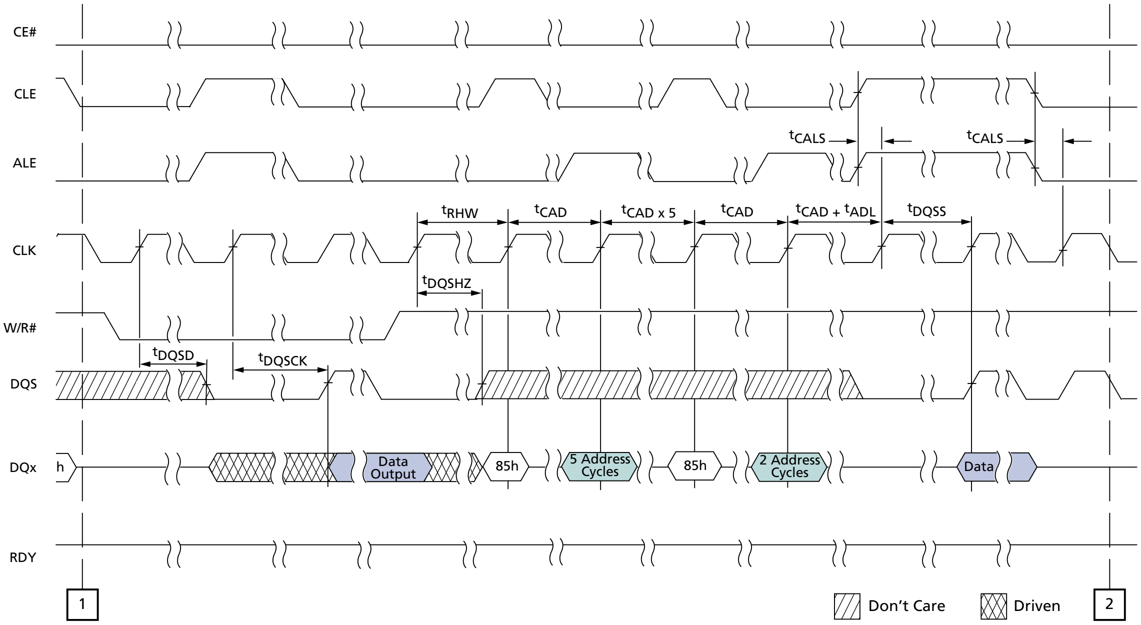


Figure 114: COPYBACK (3 of 3)

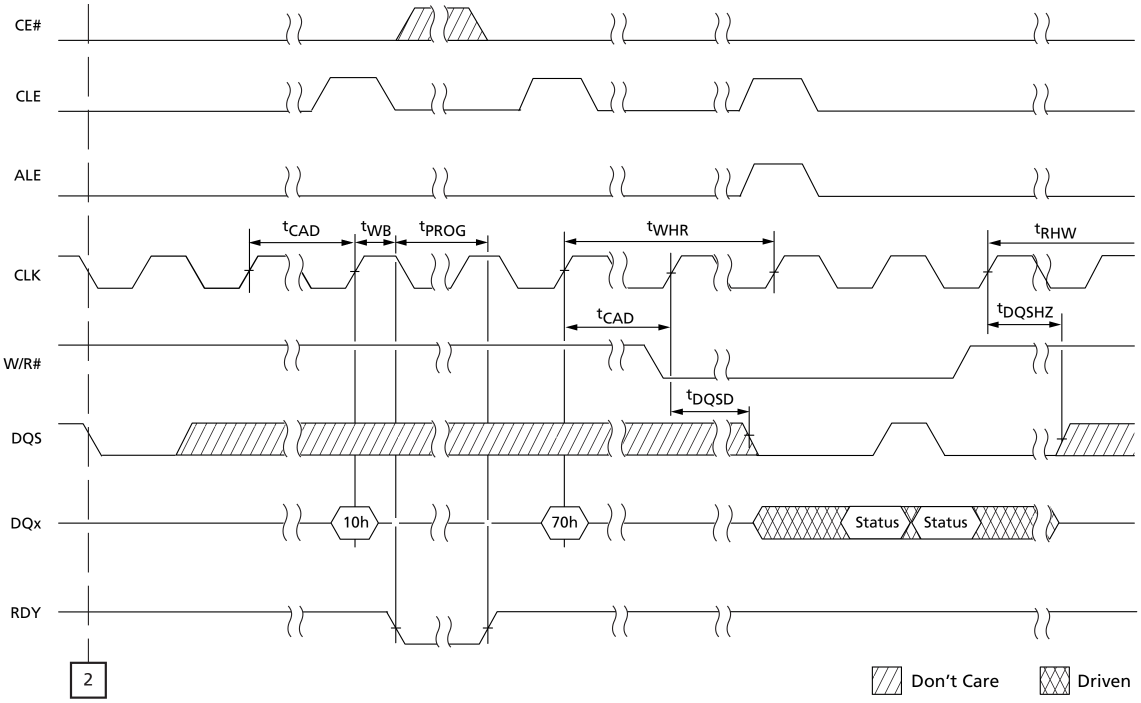


Figure 115: READ OTP PAGE

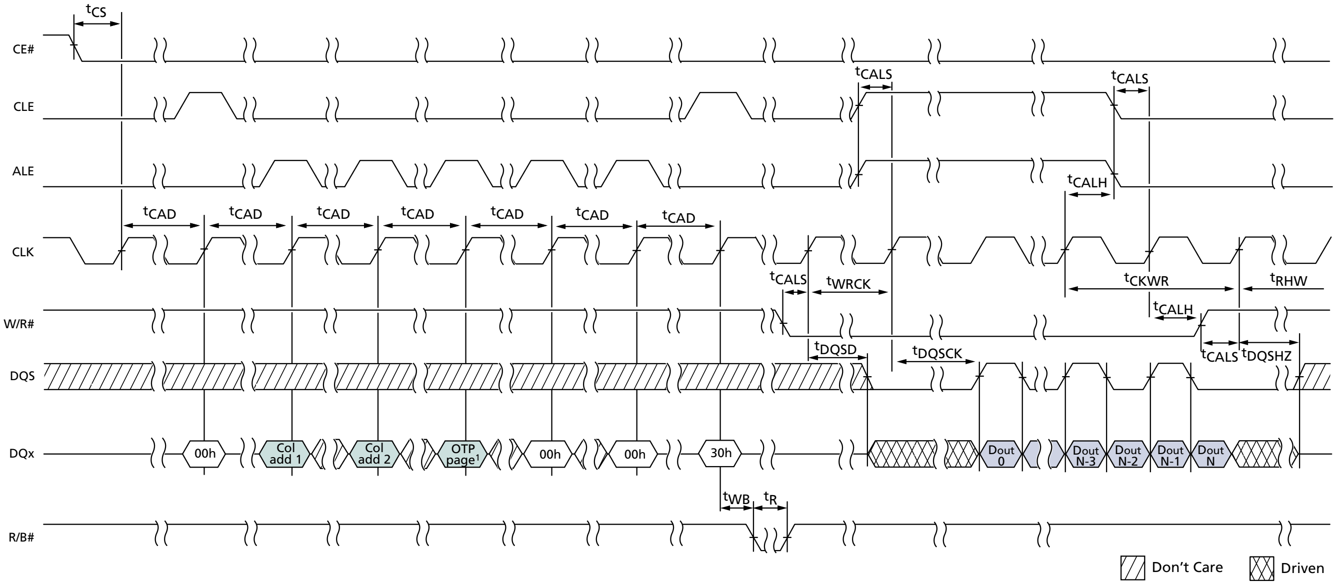


Figure 116: PROGRAM OTP PAGE (1 of 2)

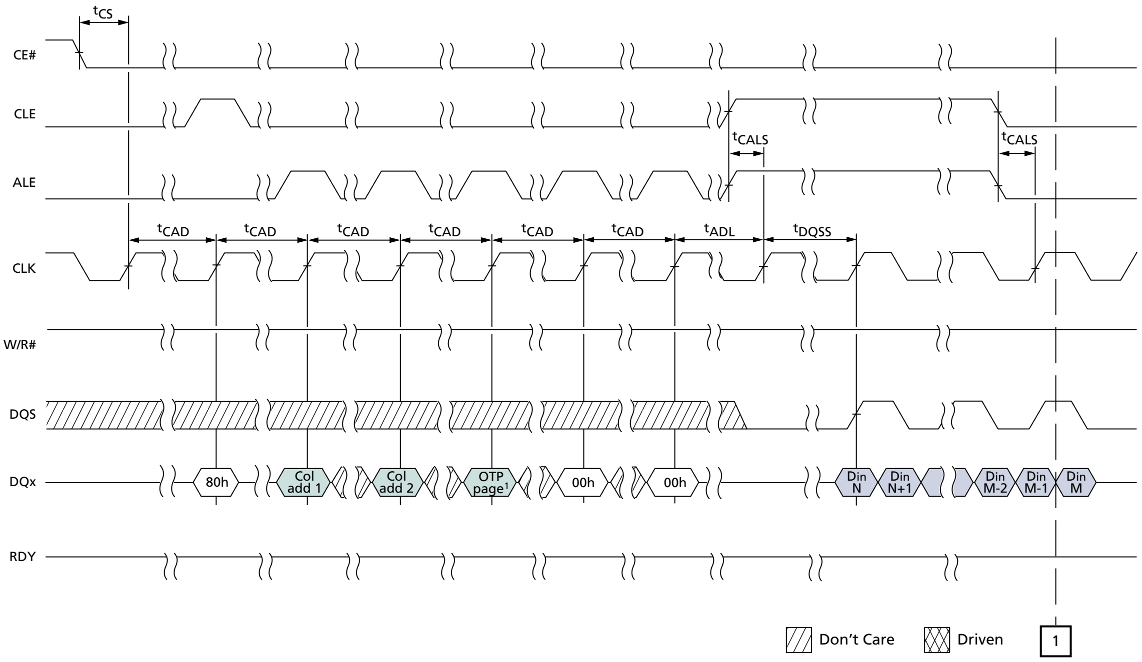


Figure 117: PROGRAM OTP PAGE (2 of 2)

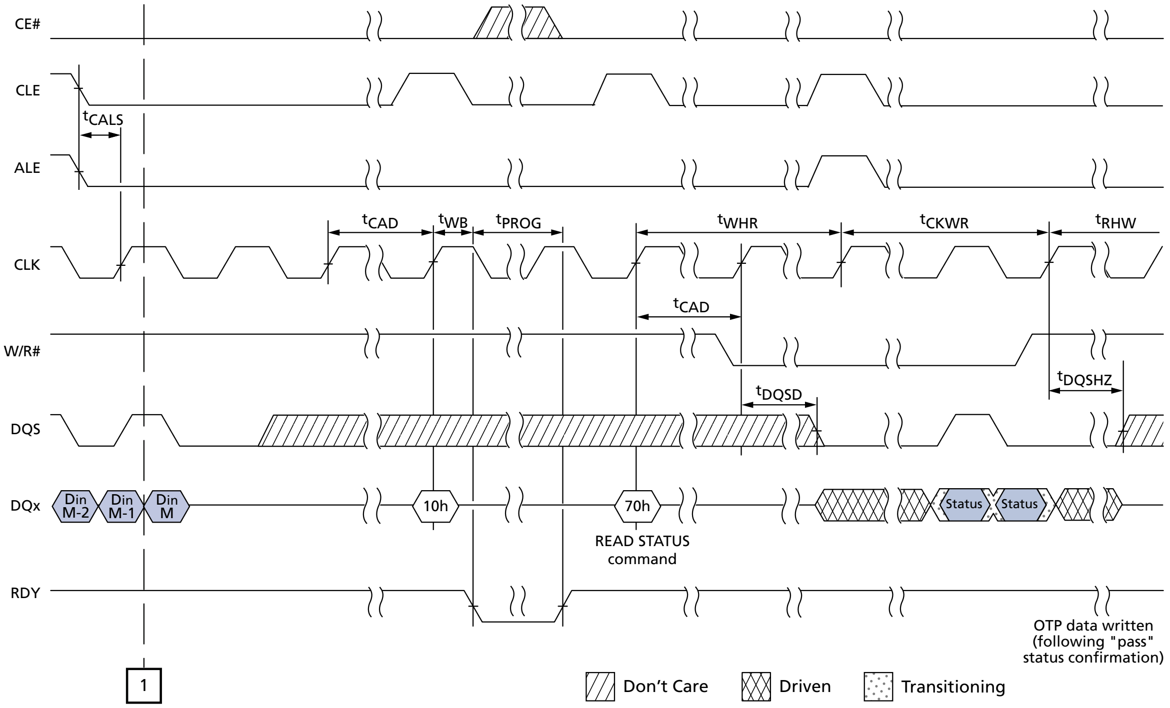
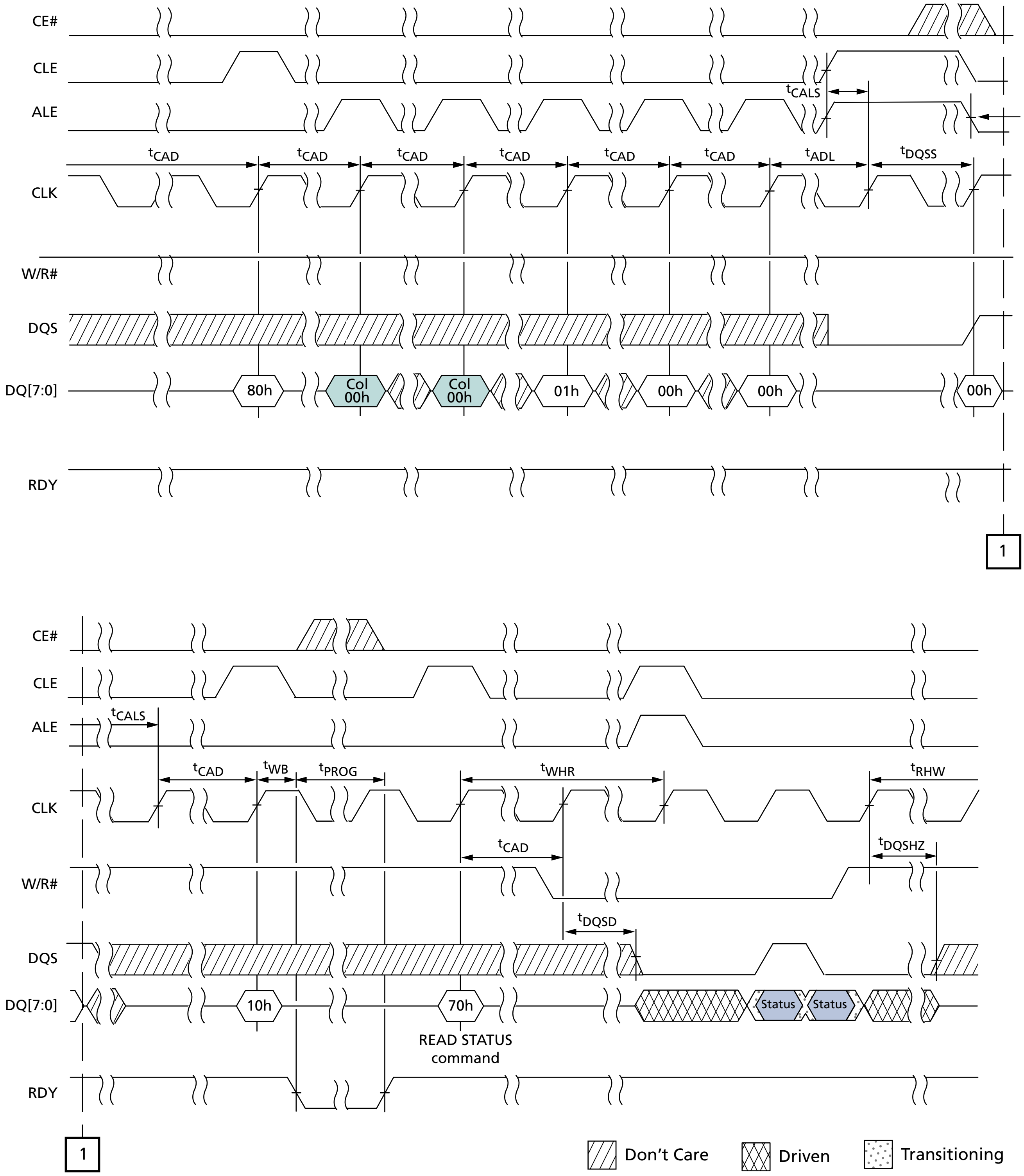


Figure 118: PROTECT OTP AREA



Revision History

Rev. C – 09/18

- Added Important Notes and Warnings section for further clarification aligning to industry standards

Rev. B – 03/15

- Updated part numbers

Rev. A – 03/14

- Initial release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.