

DDR4 SDRAM SODIMM

Addendum

MTA9ASF1G72HBZ – 8GB

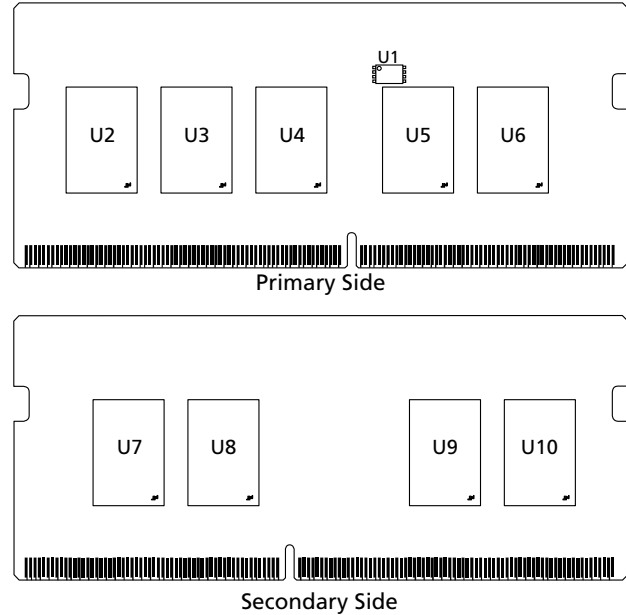
Introduction

Information provided here is in addition to or supersedes information provided in the Micron DDR4 SODIMM Core data sheet.

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- Features and specifications supported in the Micron DDR4 SODIMM Core data sheet
- 260-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rate: PC4-3200
- 8GB (1 Gig x 72)
- Data bus inversion (DBI) for data bus
- Supports ECC error detection and correction
- Single-rank
- On-board I²C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each

Figure 1: 260-Pin SODIMM



Options

- Operating temperature
 - Extended ($-40^{\circ}\text{C} \leq T_{\text{OPER}} \leq 105^{\circ}\text{C}$)
- Package
 - 260-pin DIMM (Green)
- Frequency/CAS latency
 - 0.625ns @ CL = 22 (DDR4-3200)

Marking

B
Z
-3G2

Table 1: Addressing

Parameter	8GB
Row address	64K A[15:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	8Gb (1 Gig x 8), 16 banks
Module rank address	CS0_n



Table 2: Part Numbers and Timing Parameters – 8GB Modules

Base device: MT40A1G8,¹ 8Gb DDR4 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-nRCD-nRP)
MTA9ASF1G72HBZ-3G2__	8GB	1 Gig x 72	25.6 GB/s	0.625ns/3200 MT/s	22-22-22

- Notes:
1. The data sheet for the base device can be found at micron.com.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA9ASF1G72HBZ-3G2E1.

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DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U2	0	3	21	U3	0	19	63
	1	0	8		1	17	49
	2	2	20		2	18	62
	3	1	7		3	16	50
	4	6	16		4	22	58
	5	4	4		5	21	45
	6	7	17		6	23	59
	7	5	3		7	20	46
U4	0	CB7	104	U5	0	38	183
	1	CB4	88		1	36	170
	2	CB6	100		2	39	182
	3	CB5	87		3	37	169
	4	CB3	105		4	35	186
	5	CB1	91		5	32	174
	6	CB2	104		6	34	187
	7	CB0	92		7	33	173
U6	0	55	225	U7	0	56	237
	1	52	211		1	58	249
	2	54	224		2	57	236
	3	53	212		3	59	250
	4	50	228		4	61	233
	5	49	215		5	62	245
	6	51	229		6	60	232
	7	48	216		7	63	246
U8	0	40	195	U9	0	29	67
	1	42	207		1	30	79
	2	41	194		2	28	66
	3	43	208		3	31	80
	4	44	191		4	24	70
	5	47	204		5	26	83
	6	45	190		6	25	71
	7	46	203		7	27	84



Table 3: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U10	0	12	24				
	1	15	37				
	2	13	25				
	3	14	38				
	4	9	29				
	5	10	41				
	6	8	28				
	7	11	42				



I_{DD} Specifications

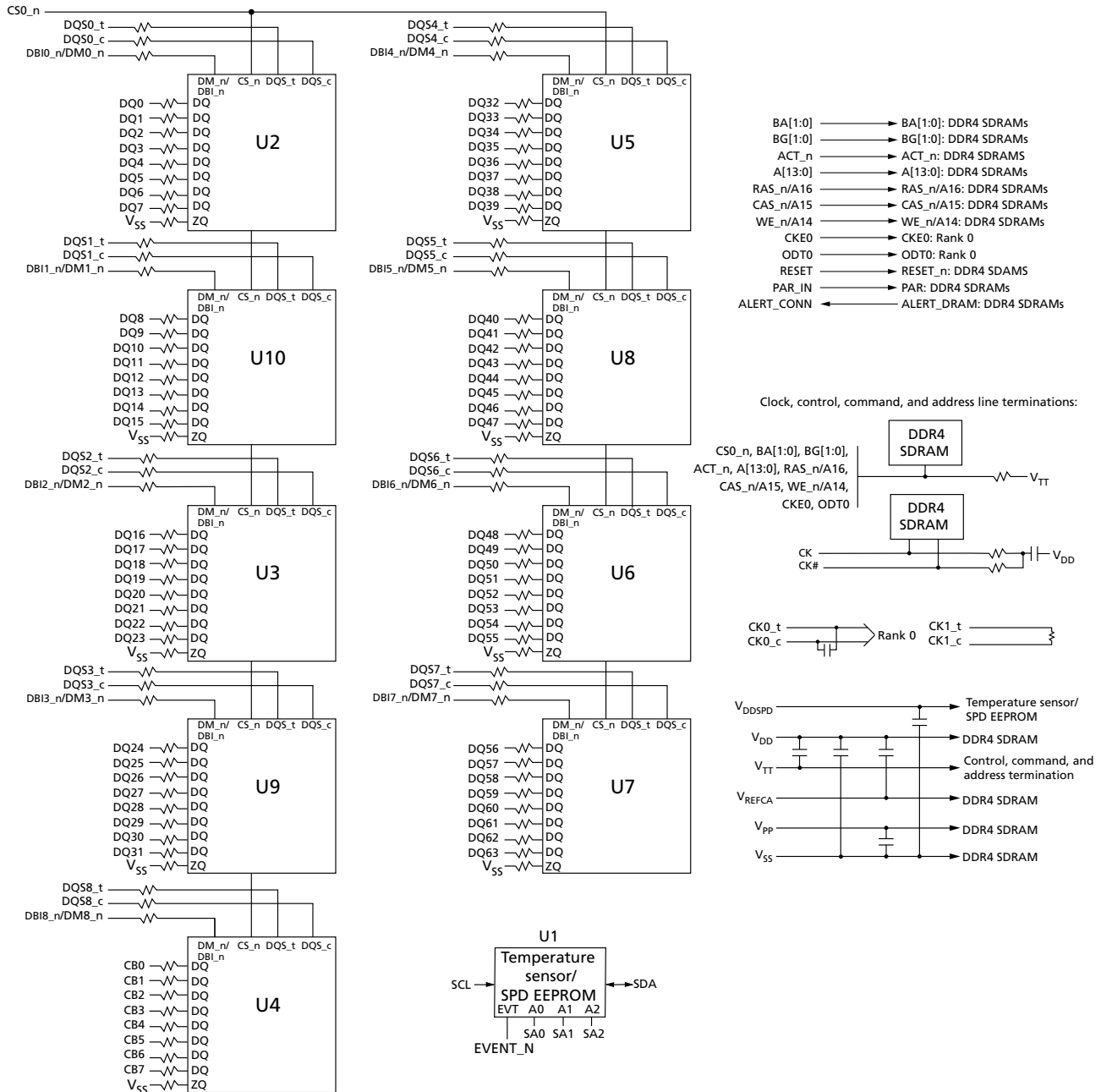
Table 4: DDR4 I_{DD} Specifications and Conditions – 8GB (Die Revision E)

Values are for the MT40A1G8 DDR4 SDRAM only and are computed from values specified in the 8Gb (1 Gig x 8) component data sheet

Parameter	Symbol	3200	Units
One bank ACTIVATE-PRECHARGE current	I _{DD0}	459	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I _{pp} current	I _{PP0}	27	mA
One bank ACTIVATE-READ-PRECHARGE current	I _{DD1}	603	mA
Precharge standby current	I _{DD2N}	324	mA
Precharge standby ODT current	I _{DD2NT}	432	mA
Precharge power-down current	I _{DD2P}	234	mA
Precharge quiet standby current	I _{DD2Q}	261	mA
Active standby current	I _{DD3N}	423	mA
Active standby I _{pp} current	I _{PP3N}	27	mA
Active power-down current	I _{DD3P}	333	mA
Burst read current	I _{DD4R}	1701	mA
Burst write current	I _{DD4W}	1440	mA
Burst refresh current (1x REF)	I _{DD5R}	900	mA
Burst refresh I _{pp} current (1x REF)	I _{PP5R}	45	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I _{DD6N} (0–85°C)	306	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I _{DD6E} (0–95°C)	855	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I _{DD6R} (0–45°C)	189	mA
Auto self refresh current (25°C)	I _{DD6A} (25°C)	78	mA
Auto self refresh current (45°C)	I _{DD6A} (45°C)	189	mA
Auto self refresh current (75°C)	I _{DD6A} (75°C)	279	mA
Auto self refresh current (95°C)	I _{DD6A} (95°C)	855	mA
Auto self refresh I _{pp} current	I _{PP6X}	54	mA
Bank interleave read current	I _{DD7}	1755	mA
Bank interleave read I _{pp} current	I _{PP7}	117	mA
Maximum power-down current	I _{DD8}	180	mA

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.



8GB (x72, ECC, SR) 260-Pin DDR4 SODIMM Functional Block Diagram

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization some-
times occur.