

DDR4 SDRAM UDIMM

Addendum

MTA16ATF4G64AZ – 32GB

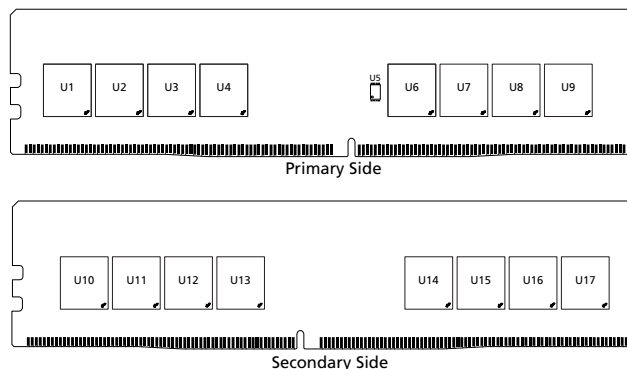
Introduction

Information provided here is in addition to or supersedes information provided in the Micron DDR4 UDIMM Core data sheet.

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- Features and specifications supported in the Micron DDR4 UDIMM core data sheet
- 288-pin, unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rates: PC4-3200, PC4-2666
- 32GB (4 Gig x 64)
- Data bus inversion (DBI) for data bus
- On-board serial presence-detect (SPD) EEPROM
- Dual-rank
- 16 internal banks; 4 groups of 4 banks each

Figure 1: 288-Pin UDIMM (MO-309, R/C-B2)



Options

- Operating temperature
 - Commercial (0°C ≤ T_{OPER} ≤ 95°C)
- Package
 - 288-pin DIMM (halogen-free)
- Frequency/CAS latency
 - 0.625ns @ CL = 22 (DDR4-3200)
 - 0.75ns @ CL = 19 (DDR4-2666)

Marking

None

Z

-3G2

-2G6

Table 1: Addressing

Parameter	32GB
Row address	128K A[16:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	16Gb (2 Gig x 8), 16 banks
Module rank address	2 CS _n [1:0]

Table 2: Part Numbers and Timing Parameters – 32GB Modules

Base device: MT40A2G8,¹ 16Gb DDR4 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL _n RCD _n RP)
MTA16ATF4G64AZ-3G2__	32GB	4 Gig x 64	25.6 GB/s	0.625ns/3200 MT/s	22-22-22
MTA16ATF4G64AZ-2G6__	32GB	4 Gig x 64	21.3 GB/s	0.75ns/2666 MT/s	19-19-19

- Notes:
1. The data sheet for the base device can be found on micron.com.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA16ATF4G64AZ-3G2B1.

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DQ Map

Table 3: Component-to-Module DQ Map

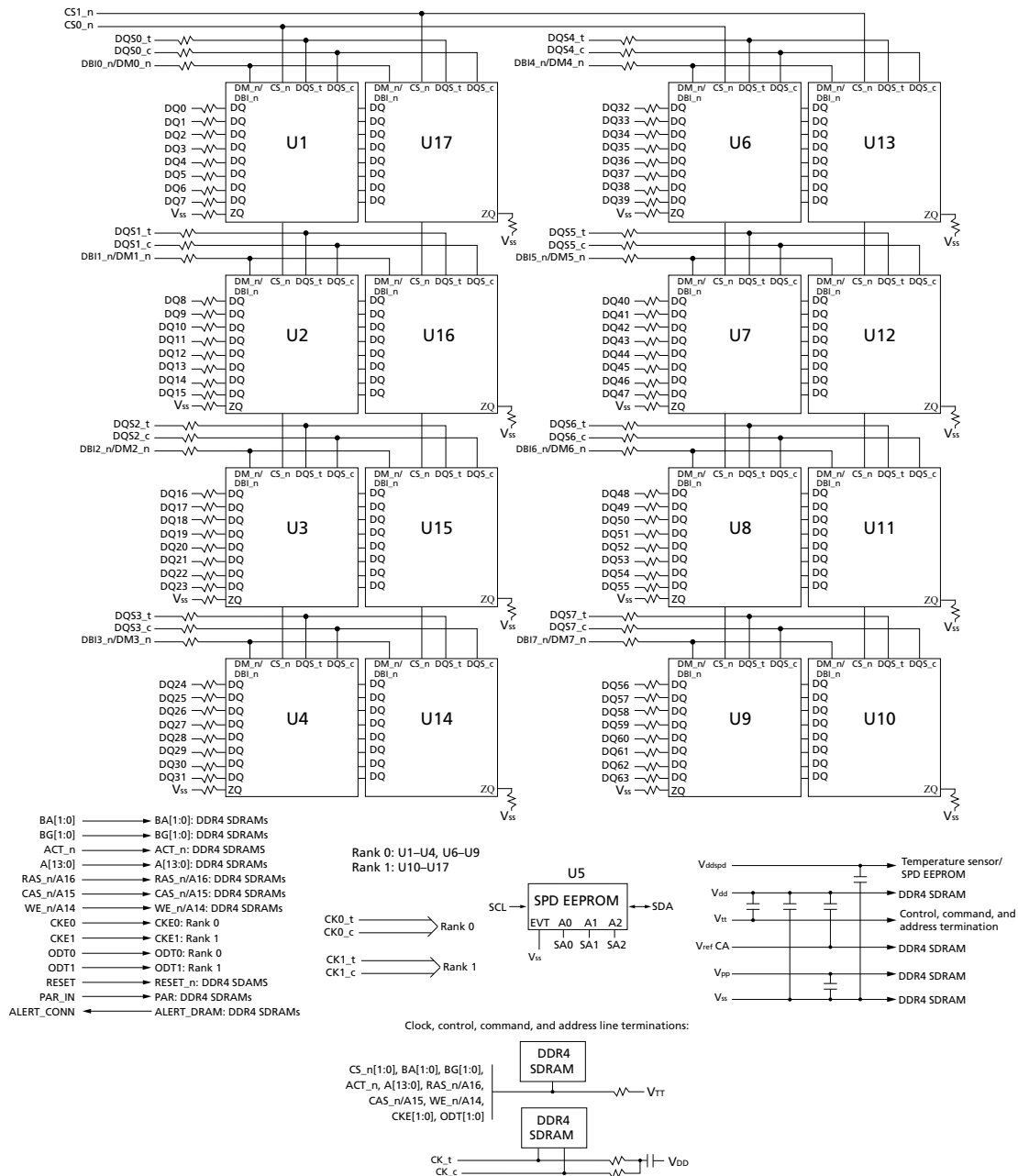
Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	2	12	U2	0	11	168
	1	1	150		1	9	161
	2	3	157		2	10	23
	3	0	5		3	8	16
	4	6	10		4	15	166
	5	4	3		5	13	159
	6	7	155		6	14	21
	7	5	148		7	12	14
U3	0	18	34	U4	0	27	190
	1	16	27		1	24	38
	2	19	179		2	26	45
	3	17	172		3	25	183
	4	22	32		4	31	188
	5	20	25		5	29	181
	6	23	177		6	30	43
	7	21	170		7	28	36
U6	0	38	102	U7	0	47	258
	1	37	240		1	44	106
	2	39	247		2	46	113
	3	36	95		3	45	251
	4	35	249		4	42	115
	5	33	242		5	40	108
	6	34	104		6	43	260
	7	32	97		7	41	253
U8	0	55	269	U9	0	63	280
	1	53	262		1	60	128
	2	54	124		2	62	135
	3	52	117		3	61	273
	4	51	271		4	58	137
	5	48	119		5	56	130
	6	50	126		6	59	260
	7	47	264		7	57	275

Table 3: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U10	0	60	128	U11	0	53	262
	1	63	280		1	55	269
	2	61	273		2	52	117
	3	62	135		3	54	124
	4	56	130		4	48	119
	5	58	137		5	51	271
	6	57	275		6	49	264
	7	59	282		7	50	126
U12	0	44	106	U13	0	37	240
	1	47	258		1	38	102
	2	45	251		2	36	95
	3	46	113		3	39	247
	4	40	108		4	33	242
	5	42	115		5	35	249
	6	41	253		6	32	97
	7	43	260		7	34	104
U14	0	24	38	U15	0	16	27
	1	27	190		1	18	34
	2	25	183		2	17	172
	3	26	45		3	19	179
	4	29	181		4	20	25
	5	31	188		5	22	32
	6	28	36		6	21	170
	7	30	43		7	23	177
U16	0	9	161	U17	0	1	150
	1	11	168		1	2	12
	2	8	16		2	0	5
	3	10	23		3	3	157
	4	13	159		4	4	3
	5	15	166		5	6	10
	6	12	14		6	5	148
	7	14	21		7	7	155

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.



32GB (x64, DR) 288-Pin DDR4 UDIMM Functional Block Diagram

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