Parallel NOR and PSRAM 88-Ball MCP Combination Memory

MT38L4031A502ZQXZI.XCA

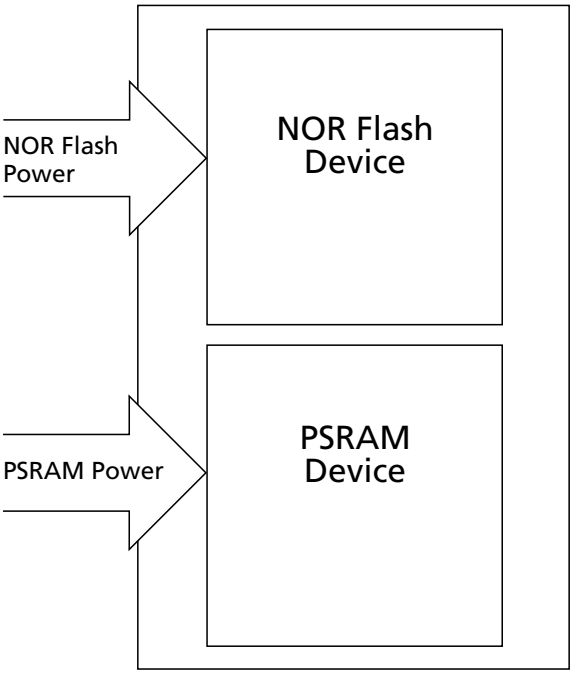
Features

- Micron® Parallel NOR Flash and PSRAM components
- RoHS-compliant, "green" package
- Space-saving multichip package (MCP)
- Low-voltage operation (1.70–1.95V)
- Industrial temperature range: –40°C to +85°C

NOR Flash-Specific Features

- Multiple-bank, Parallel NOR Flash memory
- Synchronous/asynchronous read
  - Synchronous burst read mode: 66 MHz
  - Random access times: 70ns
  - Asynchronous page read mode: 20ns
- Programming times
  - 2.5µs typical word program time using buffer enhanced factory program command
  - Fast program with 9V V_{PP}
- Memory blocks
  - Multiple bank memory array: 8Mb banks
  - Top or bottom location parameter blocks[1]
- Dual operations
  - Program erase in 1 bank, read in others
  - No delay between READ and WRITE operations
- Block locking
  - All blocks locked at power-up
  - Any combination of blocks can be locked
  - WP# for block lock-down
- Security
  - 2112-bit user programmable OTP cells
  - 64-bit unique device number
- Common Flash interface
- 100,000 PROGRAM/ERASE cycles per block
- Electronic signature
  - Manufacturer code: 20h
  - 256Mb Flash code: 880Eh (bottom boot)

Figure 1: MCP Block Diagram



PSRAM-Specific Features

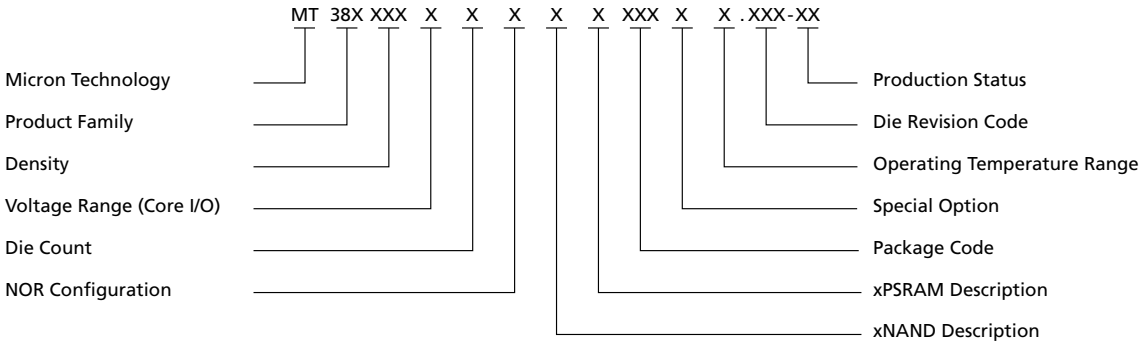
- Synchronous/asynchronous read
  - Synchronous burst read mode: 83 MHz
  - Random access times: 70ns
  - Asynchronous page read mode: 20ns
- Partial-array self refresh (PAR)
- Deep power-down (DPD) mode
- Automatic temperature-compensated self-refresh (TCR)

Notes: 1. Contact factory for availability of version.
2. For physical part markings, see Part Numbering Information (page 2).

Part Numbering Information

Micron NOR MCP devices are available in different configurations and densities. The NOR MCP part numbering system is available at www.micron.com/numbering.

Figure 2: Part Number Chart



Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: www.micron.com/decoder. To view the location of the abbreviated mark on the device, refer to customer service note CSN-11, "Product Mark/Label," at www.micron.com/csn.

MCP General Description

Micron MCP products combine NOR Flash and PSRAM devices in a single MCP.

Operational characteristics for the NOR Flash and PSRAM devices are found in the standard data sheets for each of the discrete devices.

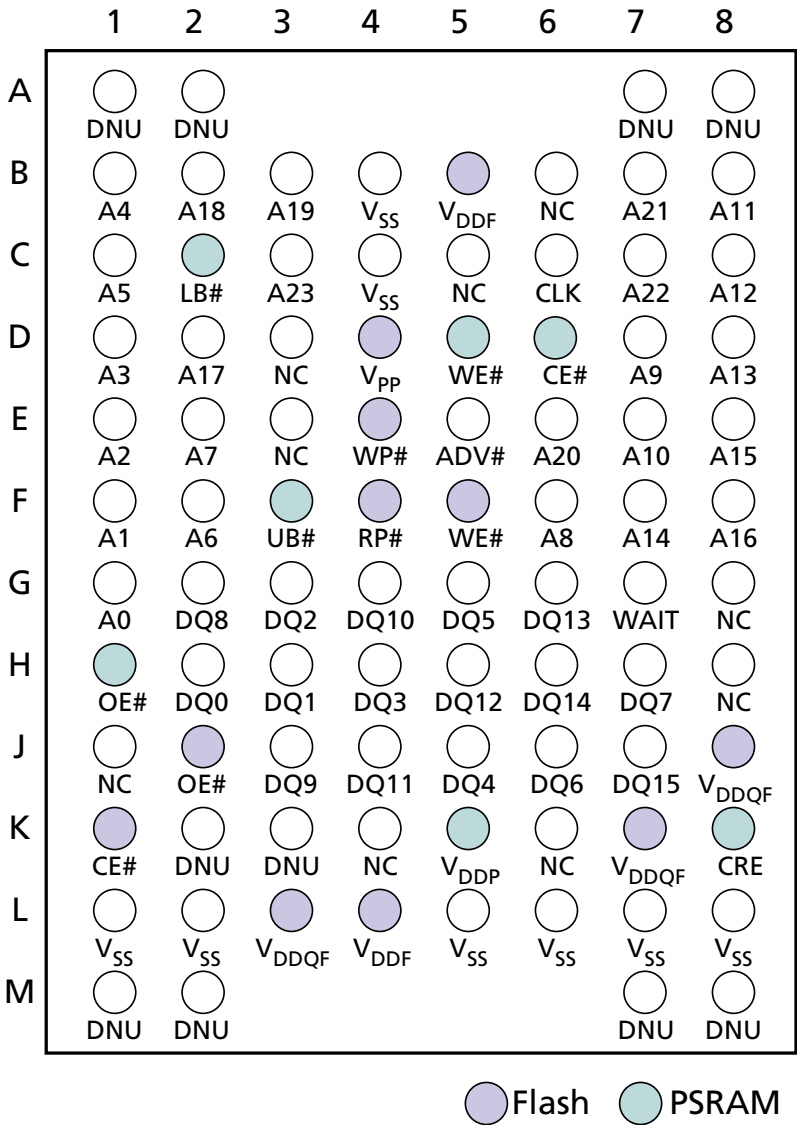
Recommended operating conditions do not allow more than one device to be active at a time. A common example of this scenario is running simultaneous READ operations on the NOR device and on the PSRAM device. Doing this results in data bus contention. To prevent this, one device must be High-Z when reading the selected device.

NOR Flash device is the with M58LR256KB. For device specifications and complete Micron NOR Flash features documentation, contact your local Micron sales office.

PSRAM device is the W966D6H. For device specifications and complete PSRAM features documentation, contact your local Micron sales office.

Ball Assignments and Descriptions

Figure 3: 88-Ball TFBGA (NOR x16; PSRAM x16) Ball Assignments



Notes:
1. A23 is valid for 256Mb and above; otherwise, it is RFU.
2. A22 is valid for 128Mb and above; otherwise, it is RFU.
3. A21 is valid for 64Mb and above; otherwise, it is RFU.

Table 1: x16 NOR Ball Descriptions

Symbol	Alternate Symbol	Type	Description
CE#	E#	Input	Chip enable: Activates the memory control logics, input buffers, decoders, and sense amplifiers. When CE# is LOW and RESET is HIGH, the device is in active mode. When HIGH, the NOR device is deselected, the outputs are High-Z, and the power consumption is reduced to the standby level.
OE#	G#	Input	Output enable: Controls data outputs during NOR bus READ operations.
WE#	W#	Input	Write enable: Controls the bus WRITE operation of the NOR command interface. The data and address inputs are latched on the rising edge of CE# or WE#, whichever occurs first.
WP#	WP#	Input	Write protect: Provides additional hardware protection for each block. When WP# is LOW, lock-down is enabled and the protection status of the locked-down blocks cannot be changed. When WP# is HIGH, lock-down is disabled and the locked-down blocks can be locked or unlocked.
RP#	RP#	Input	Reset: Provides a hardware reset of the memory. When RP# is LOW, the device is in reset mode; the outputs are High-Z and the current consumption is reduced to $_{IDD2}$. After RP#, all blocks are in the locked state and the configuration register is reset. When RP# is HIGH, the device is in normal operation. Upon exiting reset mode, the device enters asynchronous read mode, but a negative transition of CE# or L# is required to ensure valid data outputs.
V_{PP}		Supply	Both a NOR control input and power supply pin. The two functions are selected by the voltage range applied to the pin. When V_{PP} = 0V - V_{DDQF}, it functions as a control input. In this case, a voltage lower than V_{PPLKF} provides absolute protection against program or erase, while V_{PP} > V_{PP1F} enables these functions. V_{PP} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect, and PROGRAM or ERASE operations continue. When V_{PP} is in the range of V_{PPH}, it acts as a power supply pin. In this condition, V_{PP} must be stable until the program/erase algorithm is completed.
V_{DDF}		Supply	Flash core power supply
V_{DDQF}		Supply	Flash I/O power supply

Table 2: x16 PSRAM Ball Descriptions

Symbol	Alternate Symbol	Type	Description
CE#	E#	Input	Chip enable: When LOW, CE# activates the memory state machine, address buffers and decoders, enabling READ and WRITE operations. When HIGH, all other pins are ignored and the device is automatically put in low-power standby mode.
OE#	G#	Input	Output enable: Provides high-speed, tri-state control, enabling fast READ and WRITE cycles to be achieved with the common I/O data bus.
WE#	W#	Input	Write enable: Controls the bus WRITE operation.
CRE	CR	Input	Configuration register enable: When HIGH, bus READ or WRITE operations access either the value of the refresh configuration register or the bus configuration register, according to the value of A19.
UB#		Input	Upper byte enable: Gates the data on the upper byte data I/Os (DQ[15:8]) to or from the upper part of the selected address during a WRITE or READ operation.
LB#		Input	Lower byte enable: Gates the data on the lower byte data I/Os (DQ[7:0]) to or from the lower part of the selected address during a WRITE or READ operation.
V_{DDP}		Supply	PSRAM power supply.

Table 3: NOR/PSRAM Shared Ball Descriptions

Symbol	Type	Description
A[MAX:0]	Input	Address: Select the cells in the memory array to access during bus READ operations. During bus WRITE operations they control the commands sent to the command interface of NOR memory program/erase controller, and they select the cells to access in the PSRAM.
DQ[15:0]	Input/ Output	Data inputs/outputs: The bidirectional I/Os output the data stored at the selected address during a NOR bus READ operation or inputs a command or the data to be programmed during a bus WRITE operation. The upper byte data inputs/outputs carry the data to or from the upper part of the selected address during a PSRAM WRITE or READ operation, when UB# is driven LOW. Likewise, the lower byte data I/Os carry the data to or from the lower part of the selected address during a WRITE or READ operation, when LB# is driven LOW.
CLK	Input	Clock
ADV#	Input	Latch enable input
WAIT	Output	WAIT data in burst mode
Symbol	**Type**	**Description**
V_{SS}	Supply	Shared ground.
Symbol	**Type**	**Description**
NC	–	Not connected.
DNU	–	Do not use.

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4: Absolute Maximum Ratings

Parameters/Conditions	Symbol	Min	Max	Unit
Ambient operating temperature	T_A	–40	85	°C
	T_{BIAS}	–40	85	°C
Storage temperature range	T_{STG}	–55	125	°C
Input voltage	V_{IN}	–0.2	2.45	V
PSRAM core & I/O supply voltage	V_{DDP}	–0.2	2.45	V
Flash core supply voltage	V_{DDF}	–0.2	2.45	V
Flash I/O supply voltage	V_{DDQF}	–0.2	2.45	V
Flash V_{PP} program voltage	V_{PP}	–0.2	10	V
Output short circuit current	I_O	–	100	mA
Time for V_{PP} at V_{PPH}	^tVPPH	–	100	hours

Table 5: Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
PSRAM core & I/O supply voltage	V_{DDP}	1.70	1.95	V
Flash core supply voltage	V_{DDF}	1.70	1.95	V
Flash I/O supply voltage	V_{DDQF}	1.70	1.95	V
Flash V_{PP} supply voltage (application environment)	V_{PP}	–0.4	V_{DDQF} + 0.4	V
Flash V_{PP} supply voltage (factory environment)	V_{PP}	8.5	9.5	V
Operating temperature range	–	–40	+85	°C

Table 6: Operating Modes – Standard Asynchronous Operation

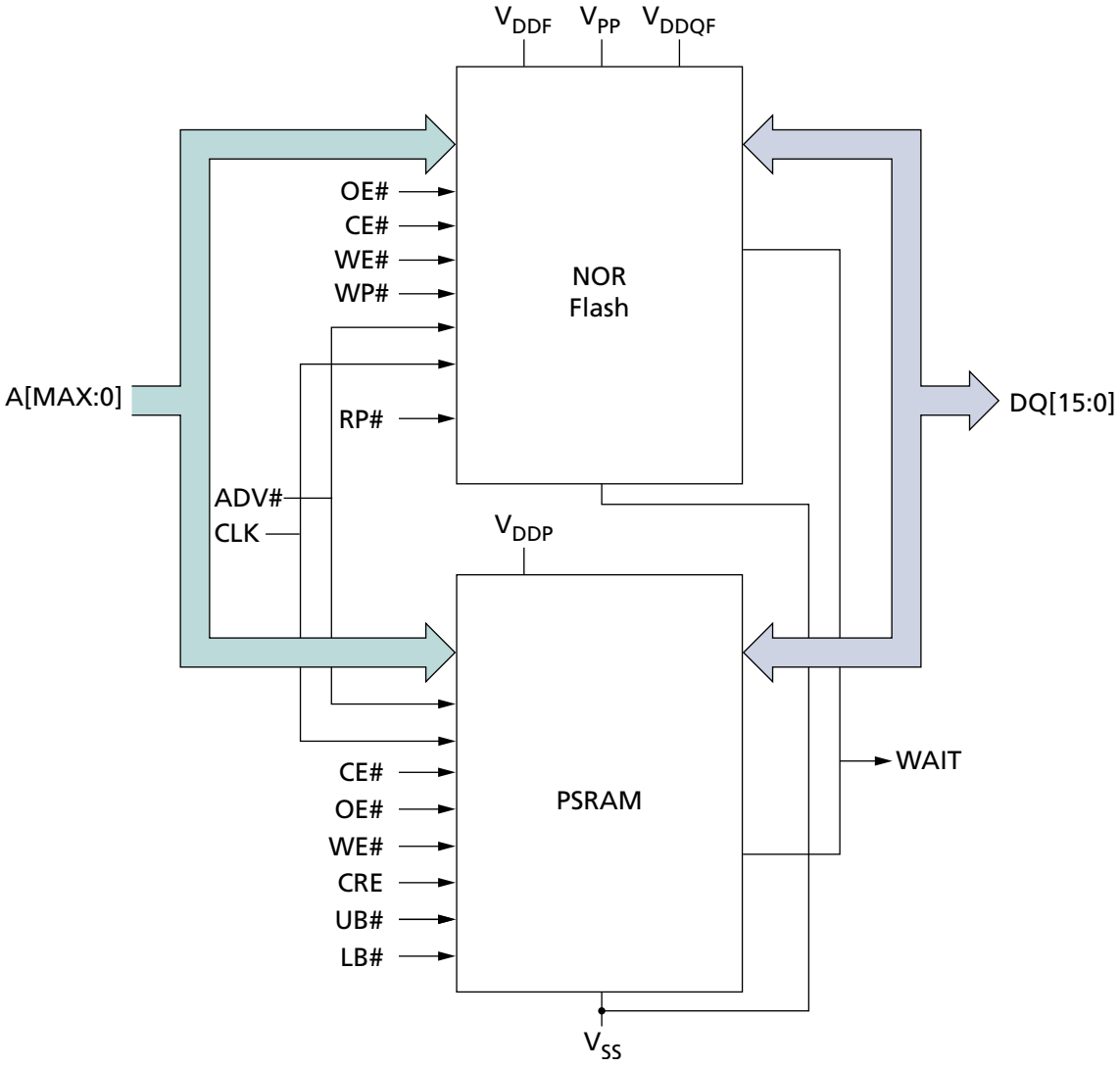
X = "Don't Care"

	Flash				PSRAM						Shared			
Operation	**RP#**	**CE#**	**OE#**	**WE#**	**CE#**	**OE#**	**WE#**	**CRE**	**UB#**	**LB#**	**ADV#**	**CLK[1]**	**ADQ[15:0]**	**WAIT[2]**
Flash														
READ	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	X	X	V_{IH}	V_{IL}	Address in/ data out	Low-Z
WRITE	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	X	X	X	V_{IH}	V_{IL}	Address in/ data in	Low-Z
ADDRESS LATCH	V_{IH}	V_{IL}	V_{IH}	X	V_{IH}	X	X	X	X	X	V_{IL}	V_{IL}	Data out or High-Z[3]	Low-Z
OUTPUT DISABLE	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	X	X	V_{IH}	V_{IL}	High-Z	Low-Z
STANDBY	V_{IH}	V_{IH}	X	X	Any PSRAM mode allowed						X	V_{IL}	High-Z	High-Z
RESET	V_{IL}	X	X	X							X	V_{IL}	High-Z	High-Z
PSRAM														
READ	X	V_{IH}	X	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	_/	V_{IL}	Address in/ data out	Low-Z
WRITE	X	V_{IH}	X	X	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	_/	V_{IL}	Address in/ data in	High-Z
READ CONFIGURATION REGISTER (CRE controlled)	X	V_{IH}	X	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	_/	V_{IL}	Address in/ BCR, RCR, or DIDR content	Low-Z
SET CONFIGURATION REGISTER (CRE controlled)[4]	X	V_{IH}	X	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	_/	V_{IL}	BCR/RCR data	Low-Z
OUTPUT DISABLE (No operation)	X	V_{IH}	X	X	V_{IL}	V_{IH}	X	V_{IL}	X	X	X	X	High-Z	Low-Z
DEEP POWER DOWN[5]	Any Flash mode allowed				V_{IH}	X	X	X	X	X	X	V_{IL}	High-Z	High-Z
STANDBY					V_{IH}	X	X	X	X	X	X	V_{IL}	High-Z	High-Z

Notes:
1. CLK must remain LOW when the PSRAM device is operating in asynchronous mode.
2. For the Flash device, WAIT polarity is configured using the SET CONFIGURATION REGISTER command.
3. See the NOR data sheet for more information.
4. BCR and RCR only.
5. The device enters deep power-down mode by driving the CE# from LOW to HIGH, with bit 4 of the RCR set to 0. The device remains in deep power-down mode until CE# goes LOW again and is held LOW for ^{t}DPDX.

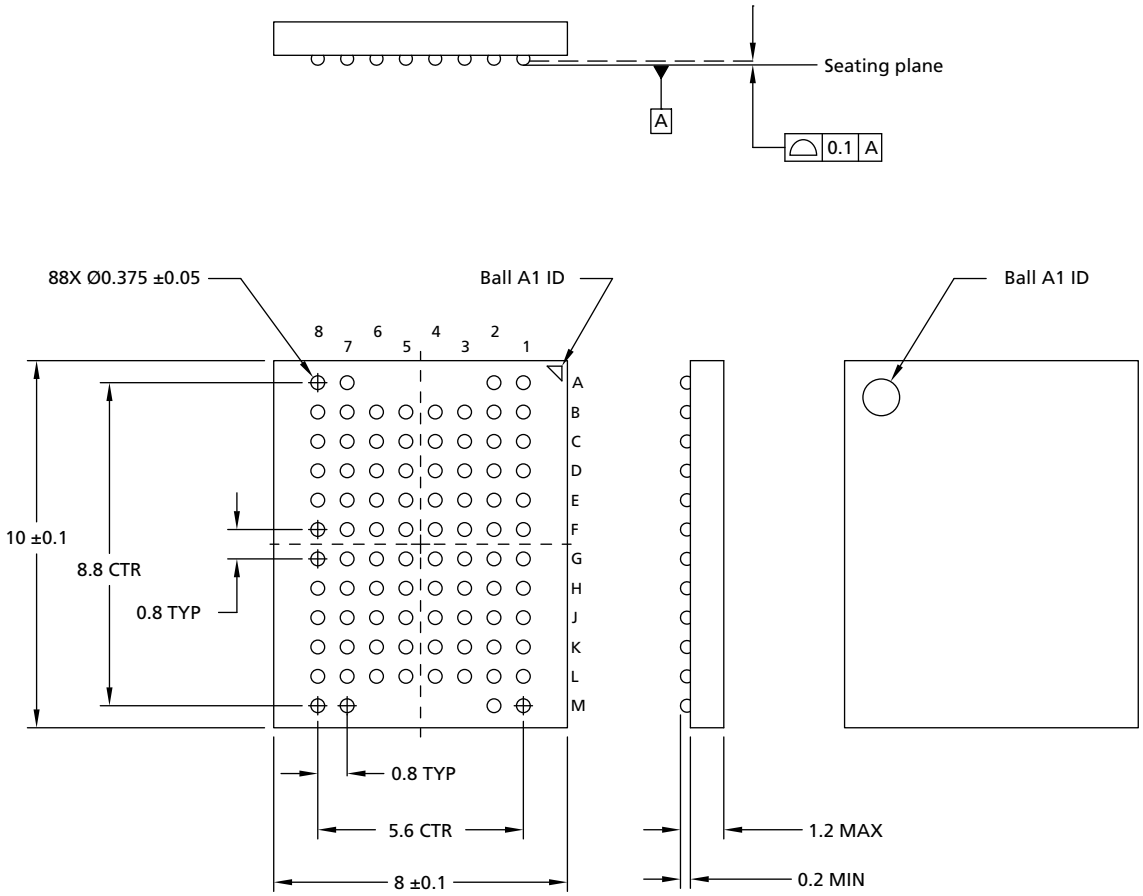
Device Diagrams

Figure 4: 88-Ball Functional Block Diagram (NOR with PSRAM)



Package Dimensions

Figure 5: 88-Ball TFBGA (Package Code: ZQ)



Note: 1. All dimensions are in millimeters.

Revision History

Rev. C – 11/14

- Production

Rev. B – 09/14

- Corrected part number

Rev. A – 08/14

- Initial release

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