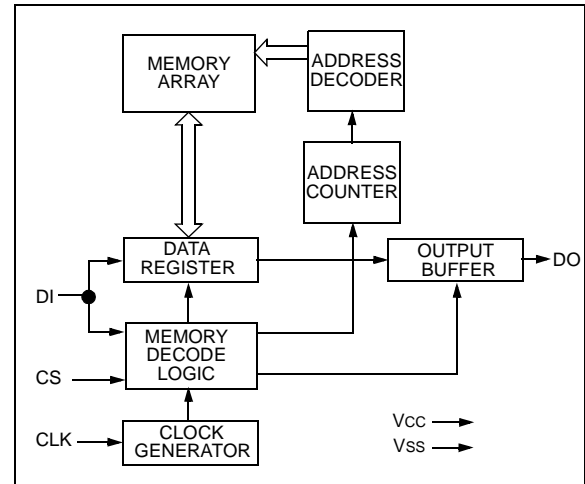


1K 5.0V Microwire® Serial EEPROM

FEATURES

- Single supply 5.0V operation
- Low power CMOS technology
 - 1 mA active current (typical)
 - 1 µA standby current (maximum)
- 64 x 16 bit organization
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial interface
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 E/W cycles ensured
- Data retention > 200 years
- 8-pin PDIP/SOIC and 8-pin TSSOP packages
- Available for the following temperature ranges:
 - Commercial (C): 0°C to +70°C
 - Industrial (I): -40°C to +85°C
 - Automotive (E): -40°C to +125°C

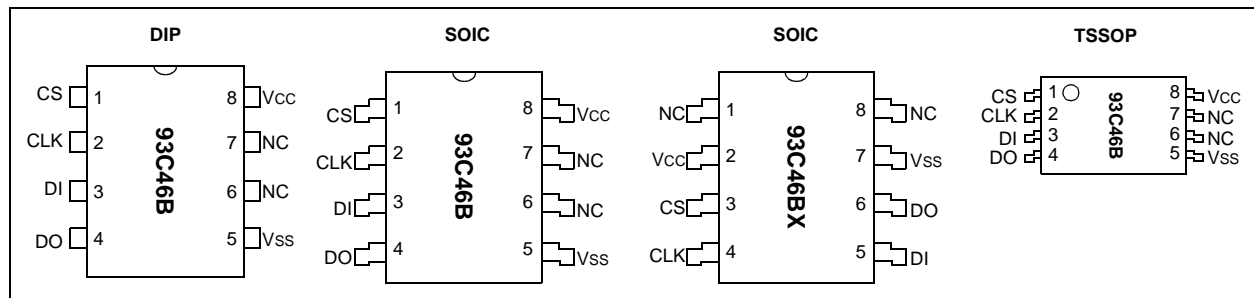
BLOCK DIAGRAM



DESCRIPTION

The Microchip Technology Inc. 93C46B is a 1 Kbit, low-voltage serial Electrically Erasable PROM. The device memory is configured as 64 x 16 bits. Advanced CMOS technology makes this device ideal for low-power, nonvolatile memory applications. The 93C46B is available in standard 8-pin DIP, surface mount SOIC, and TSSOP packages. The 93C46BX are only offered in a 150 mil SOIC package.

PACKAGE TYPE



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC}.....7.0V
 All inputs and outputs w.r.t. V_{SS} -0.6V to V_{CC} +1.0V
 Storage temperature-65°C to +150°C
 Ambient temp. with power applied-65°C to +125°C
 Soldering temperature of leads (10 seconds)+300°C
 ESD protection on all pins..... 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1 PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VSS	Ground
NC	No Connect
VCC	Power Supply

TABLE 1-2 DC AND AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Max.	Units	Conditions
High level input voltage	V _{IH}	2.0	V _{CC} +1	V	(Note 2)
Low level input voltage	V _{IL}	-0.3	0.8	V	—
Low level output voltage	V _{OL}	—	0.4	V	I _{OL} = 2.1 mA; V _{CC} = 4.5V
High level output voltage	V _{OH}	2.4	—	V	I _{OH} = -400 μA; V _{CC} = 4.5V
Input leakage current	I _{LI}	-10	10	μA	V _{IN} = V _{SS} to V _{CC}
Output leakage current	I _{LO}	-10	10	μA	V _{OUT} = V _{SS} to V _{CC}
Pin capacitance (all inputs/outputs)	C _{IN} , C _{OUT}	—	7	pF	V _{IN} /V _{OUT} = 0 V (Notes 1 & 2) T _{AMB} = +25°C, F _{CLK} = 1 MHz
Operating current	I _{CC} read	—	1	mA	—
	I _{CC} write	—	1.5	mA	—
Standby current	I _{CCS}	—	1	μA	CS = V _{SS} ; DI = V _{SS}
Clock frequency	F _{CLK}	—	2	MHz	V _{CC} = 4.5V
Clock high time	T _{CKH}	250	—	ns	—
Clock low time	T _{CKL}	250	—	ns	—
Chip select setup time	T _{CSS}	50	—	ns	Relative to CLK
Chip select hold time	T _{CSh}	0	—	ns	Relative to CLK
Chip select low time	T _{CsL}	250	—	ns	—
Data input setup time	T _{DIS}	100	—	ns	Relative to CLK
Data input hold time	T _{DIH}	100	—	ns	Relative to CLK
Data output delay time	T _{PD}	—	400	ns	C _L = 100 pF
Data output disable time	T _{CZ}	—	100	ns	C _L = 100 pF (Note 2)
Status valid time	T _{SV}	—	500	ns	C _L = 100 pF
Program cycle time	T _{WC}	—	2	ms	ERASE/WRITE mode
	T _{EC}	—	6	ms	ERAL mode
	T _{WL}	—	15	ms	WRAL mode
Endurance	—	1M	—	cycles	25°C, V _{CC} = 5.0V, Block Mode (Note 3)

Note 1: This parameter is tested at T_{AMB} = 25°C and F_{CLK} = 1 MHz.

2: This parameter is periodically sampled and not 100% tested.

3: This application is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which may be obtained on our website: www.microchip.com

2.0 PIN DESCRIPTION

2.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into standby mode. However, a programming cycle which is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (T_{CSL}) between consecutive instructions. If CS is low, the internal control logic is held in a RESET status.

2.2 Serial Clock (CLK)

The Serial Clock (CLK) is used to synchronize the communication between a master device and the 93C46B. Opcodes, addresses, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (T_{CKH}) and clock low time (T_{CKL}). This gives the controlling master freedom in preparing the opcode, address, and data.

CLK is a "Don't Care" if CS is low (device deselected). If CS is high, but START condition has not been detected, any number of clock cycles can be received by the device, without changing its status (i.e., waiting for a START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

TABLE 2-1 INSTRUCTION SET FOR 93C46B

Instruction	SB	Opcode	Address							Data In	Data Out	Req. CLK Cycles
ERASE	1	11	A5	A4	A3	A2	A1	A0	—	(RDY/BSY)	9	
ERAL	1	00	1	0	X	X	X	X	—	(RDY/BSY)	9	
EWDS	1	00	0	0	X	X	X	X	—	HIGH-Z	9	
EWEN	1	00	1	1	X	X	X	X	—	HIGH-Z	9	
READ	1	10	A5	A4	A3	A2	A1	A0	—	D15 - D0	25	
WRITE	1	01	A5	A4	A3	A2	A1	A0	D15 - D0	(RDY/BSY)	25	
WRAL	1	00	0	1	X	X	X	X	D15 - D0	(RDY/BSY)	25	

After detecting a START condition, the specified number of clock cycles (respectively low to high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcodes, addresses, and data bits before an instruction is executed (Table 2-1). CLK and DI then become don't care inputs waiting for a new START condition to be detected.

Note: CS must go low between consecutive instructions.

2.3 Data In (DI)

Data In (DI) is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

2.4 Data Out (DO)

Data Out (DO) is used in the READ mode to output data synchronously with the CLK input (T_{PD} after the positive edge of CLK).

This pin also provides READY/ $\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/ $\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought high after being low for minimum chip select low time (T_{CSL}) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held low during the entire ERASE or WRITE cycle. In this case, DO is in the HIGH-Z mode. If status is checked after the ERASE/WRITE cycle, the data line will be high to indicate the device is ready.

3.0 FUNCTIONAL DESCRIPTION

Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a HIGH-Z state except when reading data from the device, or when checking the READY/BUSY status during a programming operation. The READY/BUSY status can be verified during an ERASE/WRITE operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the HIGH-Z state on the falling edge of the CS.

3.1 START Condition

The START bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (ERASE, ERAL, EWDS, EWEN, READ, WRITE, and WRAL). As soon as CS is high, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcodes, addresses, and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new START condition is detected.

3.2 Data In (DI) and Data Out (DO)

It is possible to connect the Data In (DI) and Data Out (DO) pins together. However, with this configuration, if A0 is a logic-high level, it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation. Under such a condition, the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

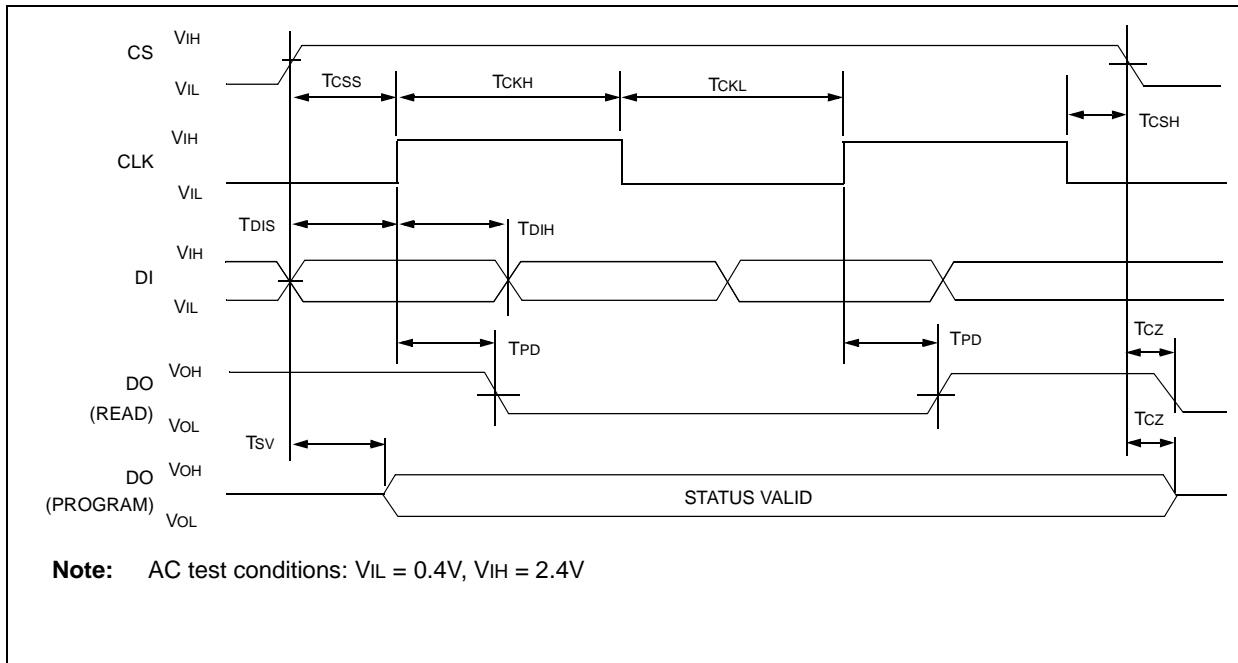
3.3 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 3.8V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 3.8V at nominal conditions.

The ERASE/SRITe Disable (EWDS) and ERASE/WRITE Enable (EWEN) commands give additional protection against accidental programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

FIGURE 3-1: SYNCHRONOUS DATA TIMING



3.4 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. This cycle begins on the rising clock edge of the last address bit.

The DO pin indicates the READY/ $\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

3.5 Erase All (ERAL)

The Erase All (ERAL) instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle, except for the different opcode. The ERAL cycle is completely self-timed and commences at the rising clock edge of the last address bit. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the READY/ $\overline{\text{BUSY}}$ status of the device, if CS is brought high after a minimum of 250 ns low (T_{CSL}) and before the entire ERAL cycle is complete.

FIGURE 3-2: ERASE TIMING

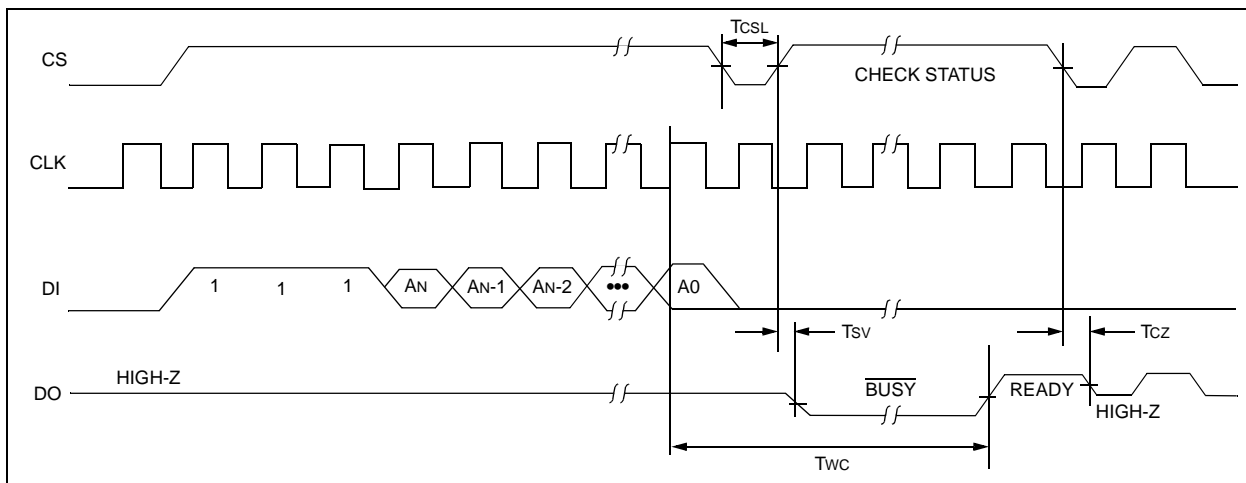
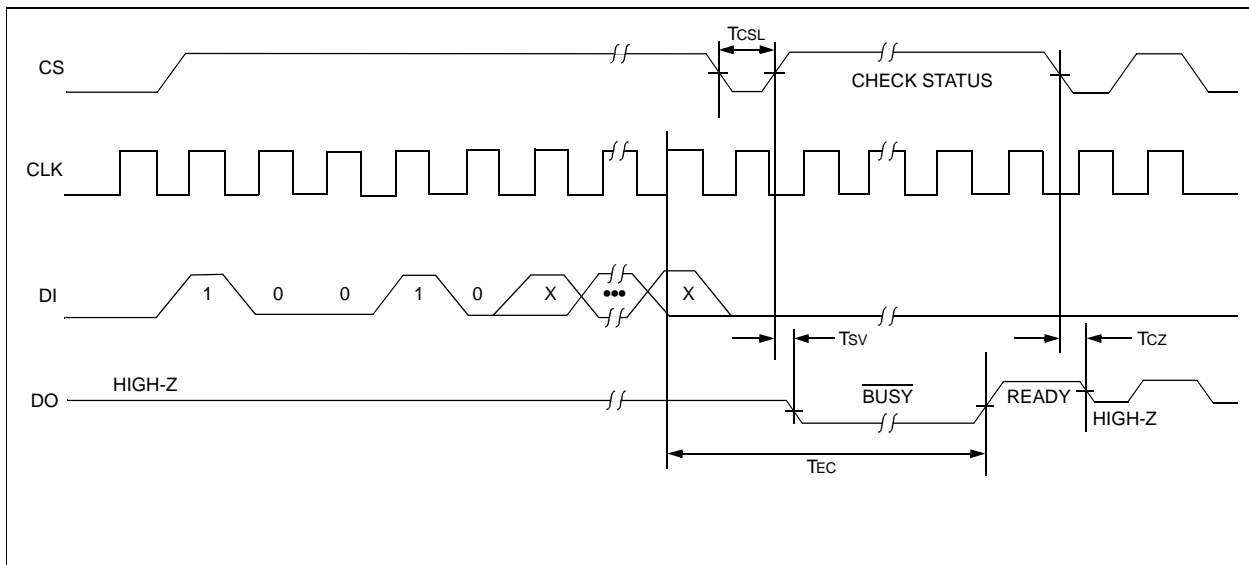


FIGURE 3-3: ERAL TIMING



3.6 ERASE/WRITE Disable and Enable (EWDS/EWEN)

The device powers up in the ERASE/WRITE Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturbance, the EWDS instruction can be used to disable all ERASE/WRITE functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWDS and EWEN instructions.

3.7 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16-bit output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 3-4: EWDS TIMING

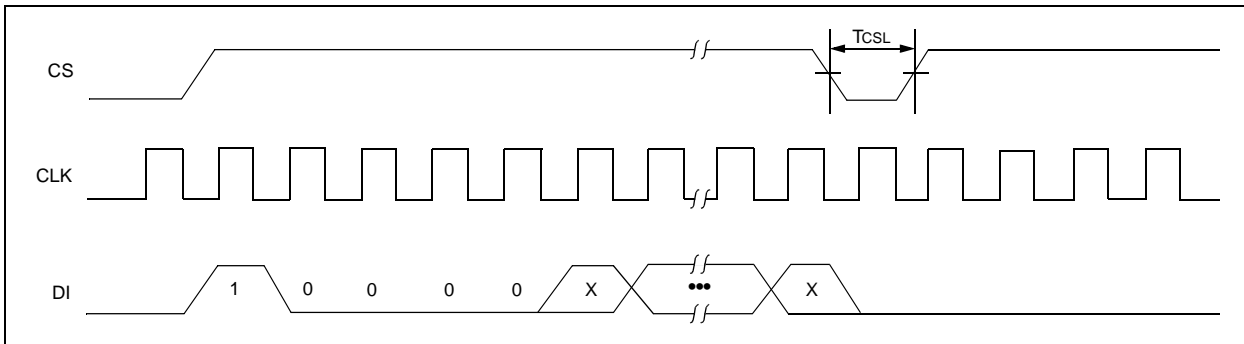


FIGURE 3-5: EWEN TIMING

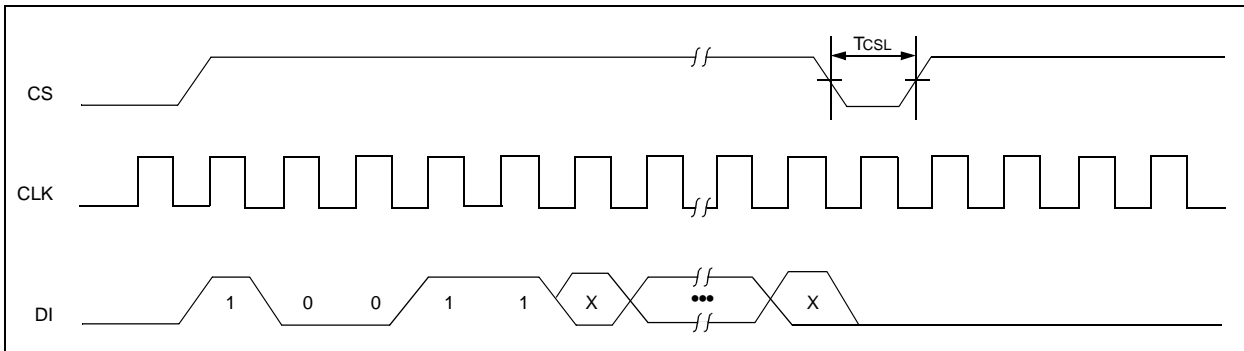
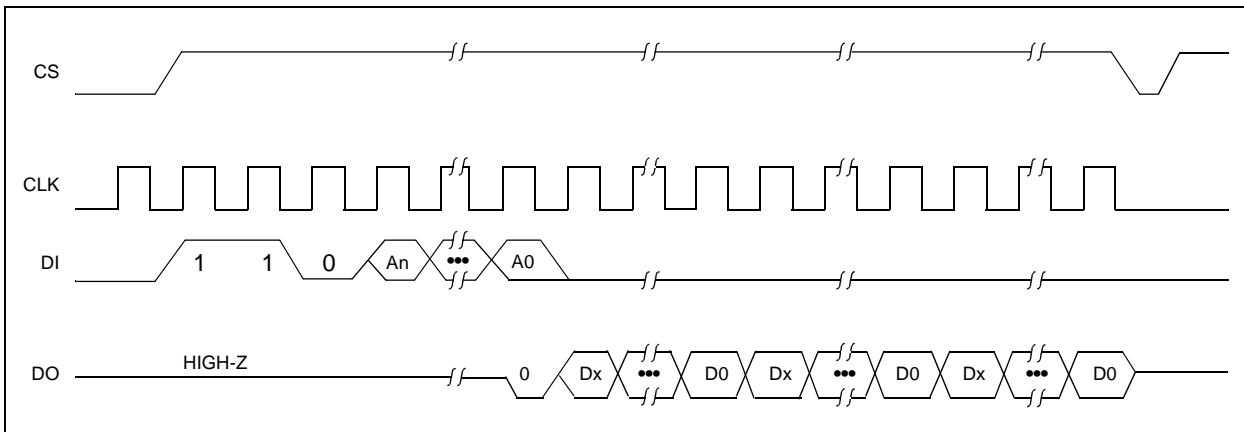


FIGURE 3-6: READ TIMING



3.8 WRITE

The WRITE instruction is followed by 16 bits of data, which are written into the specified address. After the last data bit is clocked into the DI pin, the self-timed auto-erase and programming cycle begins.

The DO pin indicates the $\overline{\text{READY}}/\overline{\text{BUSY}}$ status of the device, if CS is brought high after a minimum of 250 ns low (T_{CSL}) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

3.9 Write All (WRAL)

The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the rising clock edge of the last data bit. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction, but the chip must be in the EWEN status.

The DO pin indicates the $\overline{\text{READY}}/\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}).

FIGURE 3-7: WRITE TIMING

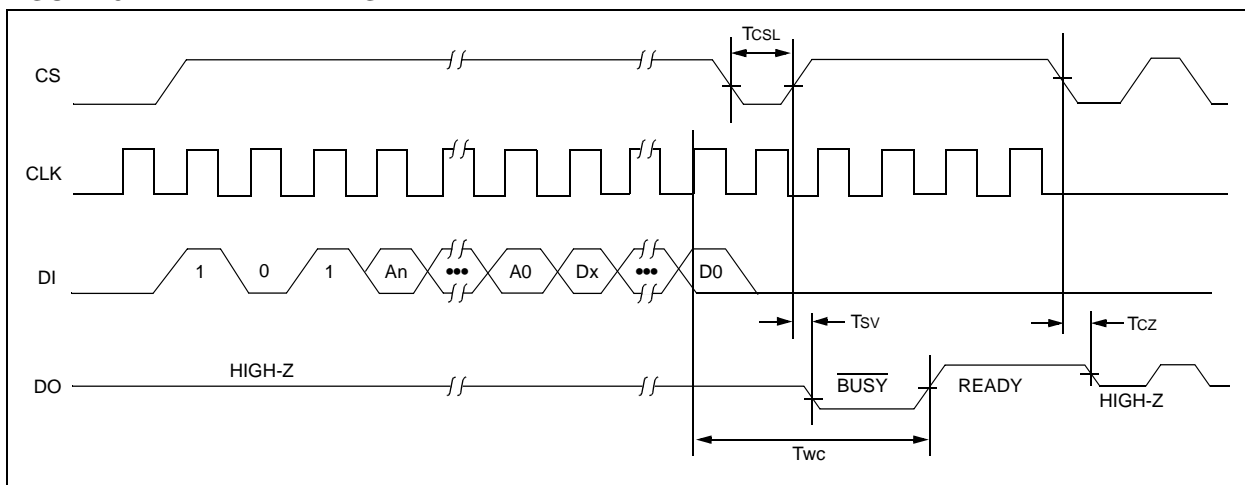
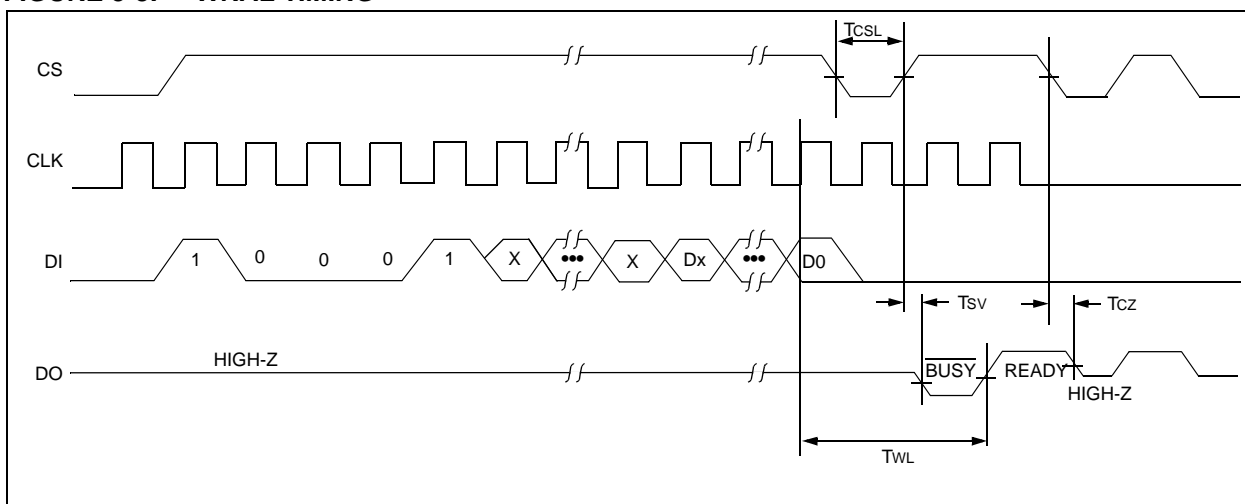


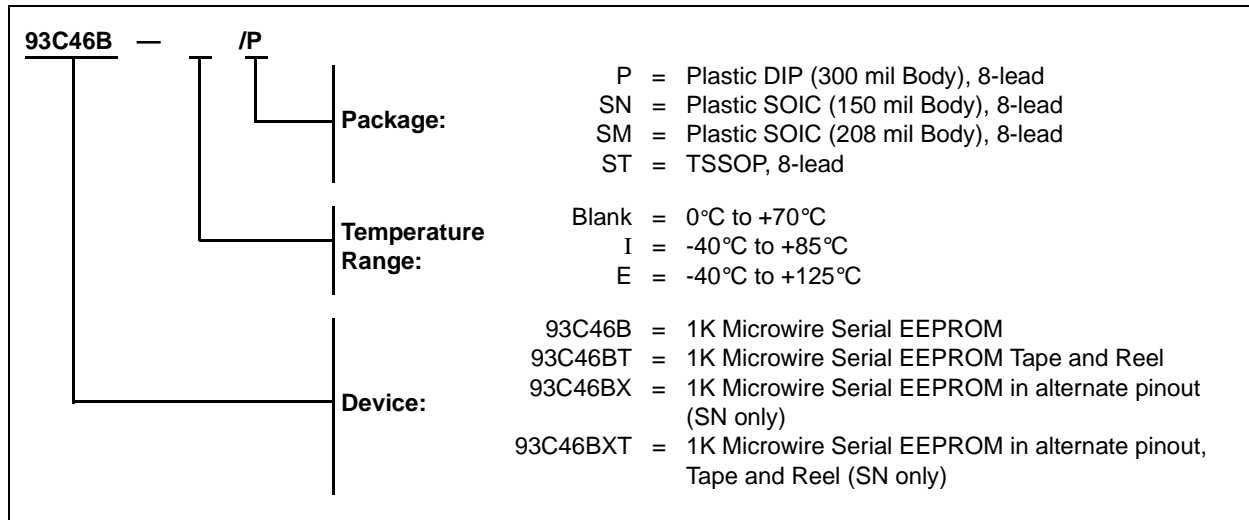
FIGURE 3-8: WRAL TIMING



93C46B

93C46B PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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NOTES:

93C46B

NOTES:

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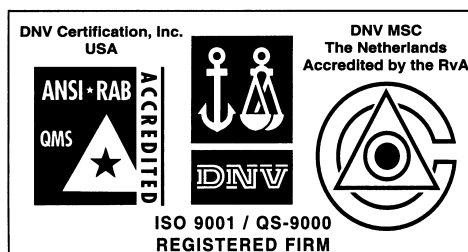
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New York

150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing

Microchip Technology Beijing Office
Unit 915
New China Hong Kong Manhattan Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Shanghai

Microchip Technology Shanghai Office
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

Hong Kong

Microchip Asia Pacific
RM 2101, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India

Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaughnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

ASIA/PACIFIC (continued)

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan

Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark

Microchip Technology Denmark ApS
Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Arizona Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Arizona Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Germany

Analog Product Sales
Lochhamer Strasse 13
D-82152 Martinsried, Germany
Tel: 49-89-895650-0 Fax: 49-89-895650-22

Italy

Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

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