

Product Change Notification - CYER-15MFPN252

Date: 23 Aug 2013

Product Category: 8-bit Microcontrollers; Analog (Linear & Mixed Signal) AND Interface; 16-bit Microcontrollers and Digital Signal Controllers

Notification subject: CCB 1326 Initial Notice: Qualification of 28L PDIP and 40L PDIP packages at MMT (ALPH) assembly site.

Notification text:

PCN Status:

Initial notification

Microchip Parts Affected:

See attachments of affected catalog part numbers (CPN) labeled as...

PCN_CYER-15MFPN252_Affected_CPN.xls

PCN_CYER-15MFPN252_Affected_CPN.pdf

Description of Change:

Qualification of 28L PDIP and 40L PDIP packages at MMT (ALPH) assembly site.

Impacts to Data Sheet:

None

Reason for Change:

To improve productivity

Change Implementation Status:

In Progress

Estimated First Ship Date:

October 10, 2013 (date code: 1341)

NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Markings to Distinguish Revised from Unrevised Devices:

Traceability code

Revision History:

August 23, 2013: Issued initial notification.

The change described in this PCN does not alter Microchip's current regulatory compliance regarding the material content of the applicable products.

Attachment(s):

[PCN_CYER-15MFPN252_Affected CPN.pdf](#) [PCN_CYER-15MFPN252_Qual Plan.pdf](#) [PCN_CYER-15MFPN252_Affected CPN.xlsx](#)

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PCN_CYER-15MFPN252
CATALOG_PART_NBR
AY0438/P
AY0438-I/P
CF775-04/P
DSPIC30F3011-20E/P
DSPIC30F3011-20I/P
DSPIC30F3011-30I/P
DSPIC30F3014-20E/P
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DSPIC30F4011-20I/P
DSPIC30F4011-30I/P
DSPIC30F4013-20E/P
DSPIC30F4013-20I/P
DSPIC30F4013-30I/P
PIC16C55-10/P
PIC16C55-10I/P
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SST89E54RDA-40-C-PIE
SST89E54RDA-40-I-PIE-ZZ131
SST89E58RDA-40-C-PIE
SST89E58RDA-40-C-PIE-ZZ132
SST89E58RDA-40-I-PIE-ZZ132
TC7106ACPL
TC7106AIPL
TC7106ARCPL
TC7106CPL
TC7106IPL
TC7106RCPL
TC7107ACPL
TC7107AIPL
TC7107ARCPL
TC7107CPL
TC7107IPL
TC7107RCPL
TC7109ACPL
TC7109ACPL514
TC7109CPL
TC7116ACPL
TC7116CPL
TC7117ACPL
TC7117CPL
TC7117RCPL
TC7126ACPL
TC7126ARCPL
TC7126CPL
TC7126IPL
TC7126RCPL
TC7129CPL
TC7135CPI
TC835CPI
TC850CPL



MICROCHIP

QUALIFICATION PLAN

PCN #: CYER-15MFPN252

**Date:
August 14, 2013**

**Qualification of 28L PDIP and 40L PDIP packages at MMT
(ALPH) assembly site.**

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Purpose: _____ Qualification of 28L PDIP and 40L PDIP packages at MMT (ALPH) assembly site.

MP code: _____ C5AF14S2XAXF

Part No.: _____ PIC18F452-E/P

BD No: _____ BDM-000375 rev. A

CCB No: _____ 1326

Package:

Type _____ 40L PDIP

Width or Size _____ 0.600 in.

Die thickness: _____ 15 mils

Die size: _____ 82.5 x 68 mils

Lead frame:

Paddle size: _____ 260 x 266 mils (Shinko-Malaysia)

Material _____ CDA194

Surface _____ Ag Spot plated

Process _____ Stamped

Lead Lock _____ No

Part Number _____ 144040004

Wire:

Material _____ Au (MKE-Korea)

Die Attach Epoxy:

Part Number _____ CRM-1064L (Sumitomo-Singapore)

Conductive _____ Yes

Mold Compound: _____ GE800 (Hitachi-Malaysia)

Reliability Test plan: _____ See attached, STD Package Reliability Test plan on each package.

Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Qty of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
Standard Pb-free Solderability	JESD22B-102E; Perform 8 hour steam aging for Matte tin finish and 1 hour steam aging for NiPdAu finish prior to testing. Standard Pb-free: Matte tin/ NiPdAu finish, SAC solder, wetting temp 245°C for both SMD & through hole packages.	22	5	1	27	> 95% lead coverage	5	Standard Pb-free solderability is the requirement. SnPb solderability (backward solderability—SMD reflow soldering) is required for any plating related changes and highly recommended for other package BOM changes.
Standard SnPb Solderability	JESD22B-102E; Perform 8 hour steam aging prior to testing. Standard SnPb: SnPb finish, SnPb solder, wetting temp 215°C for SMD & 245°C for through hole packages.	22	5	1	27	> 95% lead coverage	5	
Wire Bond Pull - WBP	Mil. Std. 883-2011	5	0	1	5	0 fails after TC	5	30 bonds from a minimum of 5 devices.
Wire Bond Shear - WBS	CDF-AEC-Q100-001	5	0	1	5	0	5	30 bonds from a minimum of 5 devices.
Physical Dimensions	Measure per JESD22 B100 and B108	10	0	3	30	0	5	
Lead Integrity	JESD22 B105	5	0	1	5	0 (No lead breakage or cracks)	5	10 leads from each of 5 parts. Not required for SMD, only required for through-hole.
External Visual	Mil. Std. 883-2009/2010	All devices prior to submission for qualification testing	0	3	ALL	0	5	
HTSL (High Temp Storage Life)	+175 C for 504 hours or 150°C for 1008 hrs. Electrical test pre and post stress at +25°C and hot temp. 1 lot to be tested at 85C and 125C	45	5	1	50	0	10	Must be in progress at time of package release to production, but completion is not required for release to production. For hot temp testing, pre/post test 1 lot at 85°C and 125°C (if applicable)
HAST	+130°C/85% RH for 96 hours. Electrical test pre and post stress at +25°C and hot temp. 1 lot to be tested at 85C and 125C	77	5	3	246	0	10	Spares should be properly identified. Use the parts which have gone through Pre-conditioning. For hot temp testing, pre/post test 1 lot at 85°C and 125°C (if applicable)

Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Qty of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
Unbiased HAST	+130°C/85% RH for 96 hrs or +110°C/85% RH for 264 hrs. Electrical Test pre and post stress at +25°C	77	5	3	246	0	10	Spares should be properly identified. Use the parts which have gone through Pre-conditioning. Please decap/ inspect 5 units for anomalies.
Temp Cycle	-65°C to +150°C for 500 cycles. Electrical test pre and post stress at hot temp; 3 gram force WBP, on 5 devices from 1 lot, test following Temp Cycle stress. 1 lot to be tested at 85C and 125C	77	5	3	246	0	15	Spares should be properly identified. Use the parts which have gone through Pre-conditioning. For hot temp testing, pre/post test 1 lot at 85°C and 125°C (if applicable).