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Product Change Notification - CYER-19YRIY190

Date: 19 Apr 2010

Product Category: Touch Sensing Technologies; 16-bit Microcontrollers and Digital Signal Controllers; Analog (Thermal, Power Management & Safety); 8-bit Microcontrollers; All 16-bit Microcontrollers; Analog (Linear & Mixed Signal) AND Interface

Device Family:  

Notification subject: CCB 957: Qualification of 16L & 20L SOIC (.300) at GTK (GRTK) assembly site.

Notification text:

PCN Status:
Initial notification

Microchip Part#s Affected:
See attachments of Affected Part Numbers Labeled as...
PCN_CYER-19YRIY190_Affected_CPN.xls
PCN_CYER-19YRIY190_Affected_CPN.pdf

Description of Change:
Qualification of 16L & 20L SOIC (.300) at GTK (GRTK) assembly site.

Impacts to Data Sheet:
None

Reason for Change:
To improve on-time delivery performance

Change Implementation Status:
In Progress

Estimated First Ship Date:
July 30, 2010 (1031)

NOTE: Please be advised that during the transition period customers may receive pre and post change parts, due to existing inventory of the pre changed parts.

Markings to Distinguish Revised from Unrevised Devices: (e.g.: Date Code, Device Marking, Ship Container Marking)
Traceability code

Attachment(s): [PCN_CYER-19YRIY190_Affected_CPN.pdf](#)
[PCN_CYER-19YRIY190_Affected_CPN.xls](#)
[PCN_CYER-19YRIY190_Qual Plan.pdf](#)

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Parts Affected

AR1010
AR1020
dsPIC33FJ12MC201
HC12-100S0s/12ST42
HE12-100S0s/12SE30
HI12-100S0s/12SI30
HP12-100S0s/TE082703
HS12-100S0s/12SS30
HS12-100SAs/12SS30
HS12-100SIs/12SS30
HT12-100S0s/12ST25
HT12-100S0s/12ST30
HT12-100S0s/12ST49
HT12-100S0s/TE08030502
HT12-100SAs/12ST25
HT12-100SAs/12ST30
HT12-100SAs/12ST49
HT12-100SCs/12SA49
HT12-100SIs/12ST30
HT12-100SIs/12ST49
MCP1403
MCP1404
MCP1405
PIC16C770
PIC16C771
PIC16C781
PIC16C782
PIC16F631
PIC16F677
PIC16F685
PIC16F687
PIC16F689
PIC16F690
PIC16F785
PIC18F13K22
PIC18F13K50
PIC18F14K22
PIC18F14K50
PIC24F04KA201
PIC24F08KA101
PIC24F16KA101
RE46C140
RE46C141
RE46C143

RE46C144

RE46C145

TC1027

TC1232

TC4423

TC4423A

TC4424

TC4424A

TC4425

TC4425A

TC4467

TC4468

TC4469

TC4626

TC4627

TC500

TC500A

TC520A

TC962



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QUALIFICATION PLAN

PCN#: CYER-19YRIY190

**Date:
July 22, 2009**

**Qualification of 20L SOIC (.300) at GTK (GRTK)
assembly site and the 16L SOIC (.300) will qualify by
similarity**

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Purpose: _____ Qualification of 20L SOIC (.300) at GTK (GRTK) assembly site. The 16L SOIC (.300) will qualify by similarity.

Mask: _____ A7BE37G5XA20

Part No.: _____ PIC16C771-I/SO

CCB#: _____ 957

Package:

Type _____ 20L SOIC (.300")

Die thickness: _____ 15 mils

Die size: _____ 134.2 x 172.5

Lead frame:

Paddle size: _____ 160x200 mils

Material _____ C194 /Poongsan (China)

Surface _____ Bare Cu

Process _____ Stamped

Lead Lock _____ No

Part Number _____ 11-0220W-003

Wire:

Material _____ Au / Sumitomo (Japan)

Die Attach Epoxy:

Part Number _____ CRM 1076DJ-G / Sumitomo (Japan)

Conductive _____ Yes

Mold Compound: _____ G600F / Sumitomo (Taiwan)

Package Reliability Tests

Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Quantity of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
Standard Pb-free Solderability	JESD22B-102E; Perform 8 hour steam aging for Matte tin finish and 1 hr steam aging for NiPdAu finish prior to testing.	22	5	1	27	> 95% lead coverage	5	
Backward Solderability	JESD22B-102E; Perform 8 hour steam aging for Matte tin finish and 1 hr steam aging for NiPdAu finish prior to testing. Backward: Matte tin/ NiPdAu finish, SnPb solder, wetting temp 215°C for SMD.	22	5	1	27	> 95% lead coverage	5	

Package Reliability Tests

Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Quantity of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
Wire Bond Pull - WBP	Mil. Std. 883-2011	5	0	1	5	0 fails after TC	5	30 bonds from a min. 5 devices.
Wire Bond Shear - WBS	CDF-AEC-Q100-001	5	0	1	5		5	30 bonds from a min. 5 devices.
Bond Line Thickness (BLT) robustness assessment						>0.5 mils		
Physical Dimensions	Measure per JESD22 B100 and B108	10	0	3	30	0	5	
External Visual	Mil. Std. 883-2009/2010	ALL	0	3	ALL	0	5	

Package Reliability Tests

Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Quantity of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
HTSL (High Temp Storage Life)	+175°C for 504 hours or 150°C for 1008 hrs. Electrical test pre and post stress at +25C and hot temp.	45	5	3	150	0	10	
Preconditioning - * Required for surface mount devices	+150°C Bake for 24 hours, moisture loading requirements per MSL level + 3X reflow at peak reflow temperature per Jedec-STD-020C for package type; Electrical test pre and post stress at +25°C. Perform SAM analysis using the standard sample size. MSL1 @ 260°C	231	15	3	738	0	15	Spares should be properly identified. 77 parts from each lot to be used for HAST, Autoclave, Temp Cycle test.

Package Reliability Tests

Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Quantity of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
HAST *	+130°C/85% RH for 96 hours. Electrical test pre and post stress at +25 and hot temp.	77	5	3	246	0	10	Spares should be properly identified. Use the parts which have gone through Pre-conditioning.
Autoclave *	+121°C/15 psig for 96 hours. Electrical test pre and post stress at +25°C	77	5	3	246	0	10	Spares should be properly identified. Use the parts which have gone through Pre-conditioning.
Temp Cycle*	-65°C to +150°C for 500 cycles. Electrical test pre and post stress at hot temp; 3 gram force WBP, on 5 devices from 1 lot, test following Temp Cycle stress.	77	5	3	246	0	15	Spares should be properly identified. Use the parts which have gone through Pre-conditioning. For hot temp testing, pre/post test 1 lot at 85°C.