Product / Process Change Notification JLIO-7NGMXY

The information below reflects a change that is being implemented.

Notice Date:	11/17/2009
Product Category:	Power Management; CAN Communication
Notification Subject:	CCB#858: QUALIFICATION OF NEW WAFER FAB FOUNDRY FOR MCP1790, MCP1791, AND MCP2551 PRODUCTS

Notification Body:

PCN Status:
Final notification

Microchip Part#s Affected (please see the link for these files at the end of this PCN):
See attachment of Affected package/device in Qualification plan.
CCB#858_Microchip_Catalog_Part#s_Affected.xls
CCB#858_Microchip_Catalog_Part#s_Affected.pdf

Description of Change:
New Wafer Fab Foundry

Impacts to Data Sheet:
None

Reason for Change:
To improve production cycle time and on-time delivery performance

Change Implementation Status:
In Progress

Estimated Change Implementation Date(s):
September 9, 2009 (Date Code: 0937)

Markings to Distinguish Revised from Unrevised Devices: (e.g.: Date Code, Device Marking, Ship Container Marking)
Traceability code

Attachment(s):

PCN JLIO-7NGMXY_VKABx_Qual Report.pdf PCN JLIO-7NGMXY_VK001_Qual Report.pdf

CCB#858_Microchip_Catalog_Part#s_Affected.xls CCB#858_Microchip_Catalog_Part#s_Affected.pdf

Close

Microchip_Catalog_Part#s
MCP1790T-5002E/EB
MCP1790-5002E/EB
MCP1790T-3302E/DB
MCP1790-3302E/DB
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MCP2551-I/P
MCP2551-E/SN
MCP2551-E/P

MCP2551
PRODUCT QUALIFICATION REPORT

Document Control # C-1109868

November 10, 2009

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SUMMARY PRODUCT QUALIFICATION REPORT

Document Control #: C-1109868

Document Revision: A

Purpose: WAFER FAB FOUNDRY CX08HI PROCESS QUALIFICATION

Device(s): MCP2551

Mask Identification #: VK001

Process: CX08HI Process

MSL: 593

Date: November 10, 2009

	Name	Title	Date
Author	C. Desai	Reliability Engineer	November 10, 2009
Approved by	C.K. Barlingay	Reliability Manager	November 10, 2009
Approved by	P. Jaconelli	Product Engineer	November 10, 2009

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Overview

The purpose of this report is to verify that qualification testing was performed in accordance with Microchip specification QCI-39000, “Worldwide Quality Conformance Requirements”.

Qualification Plan and Descriptions

In keeping with guidelines established in Microchip specification QCI-39000, a minimum of one production lots were used for qualification testing of the MCP2551. This qualification will release the MCP2551 to production. A detailed qualification plan is listed below along with descriptions of each test.

Early Life Failure Rate (ELFR) Test
This test is designed to accelerate random failure modes that may occur during initial operation. Devices were programmed with a burn-in pattern and were exercised at a high ambient temperature to simulate field life.

One lot of MCP2551 was subjected to 24 hours of ELFR testing at 150^{o}C.

High Temperature Operating Life (HTOL) / Dynamic Life Testing (DLT)
This test is designed to accelerate random failure modes which may occur during normal operation. Devices are programmed with a burn-in program and exercised at a high ambient temperature to simulate field life.

One lot of MCP2551 was subjected to 1008 hours of dynamic life burn-in at 150^{o}C.

Electrostatic Discharge (ESD) Test Using Human Body Model (HBM) and Machine Model (MM)
This test is conducted to determine the sensitivity of the input protection circuitry to electrostatic discharge. Human Body Model tests are conducted according to EIA/JESD22-A114 and Machine Model tests are performed in accordance with EIA/JESD22-A115 (Microchip Specification QCI-30510).

One lot of MCP2551 was tested to determine susceptibility to ESD.

Latch-Up (LU) Over Current Testing
This test is employed to determine the sensitivity of a device to overshoots in input and output signals (also called transients) with respect to V_{dd} and Ground. The current injection method is used per Microchip standard QCI-30521. This test is performed at 25^{o}C and 125^{o}C.

One lot of MCP2551 was tested to determine latch up susceptibility.

Test Conditions

Tests are performed in accordance with Microchip specification QCI-39000, “Worldwide Quality Conformance Requirements”. The various conditions are listed below.

TEST	METHOD	CONDITION	SAMPLE SIZE RUN	CRITERIA
Early Life Failure Rate (ELFR)	AEC-Q100	150°C, 24 Hrs. Electrical Test at +25°C and +125°C	876	0/800 per lot
High Temperature Operating Life / Dynamic Life Test	MIL-STD 883 Method 1005	150°C, 408 Hrs Electrical Test at -40°C, +25°C and +125°C.	873	0/600 per lot
ESD Human Body Model	EIA/JESD22 -A114	1.5K Ohm, 100 pF Electrical Test at +25°C and +125°C.	12	2000 V 1 Lot
ESD Machine Model	EIA/JESD22 -A115	0 Ohm, 200 pF Electrical Test at +25°C and +125°C.	12	200 V 1 Lot
Latch-up Testing	QCI-30521	Trigger Voltage Limit = $1.5*V_{max}$ (not to exceed V_{abs}) Pulse Width = 5 ms Rise/Fall Time = 500 us Test at +25°C and +125°C	 6 6	1 Lot 100 mA (0/6) 100 mA (0/6)

Reliability Results

The results of the tests performed are presented below.

Qualification Material

Information regarding the devices that were used in this qualification is shown in the table below.

LOT	LOT 1	LOT 2
DEVICE	MCP2551	MCP2551
MASK, REV	VK001, A0	VK001, A0
WAFER PROCESS	Foundry CX08HI	Foundry CX08HI
WAFER LOT	XFGM909461547.100	XFGM909461547.100
ASSEMBLY LOT	MTAI094900489.000	N/A
PACKAGE	8L SOIC	8L Side Brazed
ASSEMBLY SITE	MTAI	N/A
FINAL TEST	MICROCHIP THAILAND	MICROCHIP CHANDLER
QUAL #	R09075	N/A
CN #	C122087	N/A
QUAL TESTS	ELFR / DLT	ESD/ LATCH- UP

Die Level Results

The results of die level testing are shown below.

EARLY LIFE FAILURE RATE (ELFR) AT 150°C	
	24 Hours
Lot 1	0/879[b]

[b] One failed unit was discounted due to test margin issue, FA # T090325 an additional two good units were removed to aid Failure analysis. A CAPA #090055 was issued for the test marginality.

DYNAMIC LIFE TESTING AT 150°C	
	408 Hours
Lot 1	0/876[e]

e Three device failed due to EOS were discounted, FA R09160.

ELECTROSTATIC DISCHARGE TEST		
	Human Body Model	Machine Model
Lot 2	4000V	400V

LATCH-UP OVER CURRENT TEST		
	@ 25^{O}C	@ 125^{O}C
Lot 2	Passed	Passed

Note: All pins meet or exceed QCI-39000 guidelines.

Package Reliability

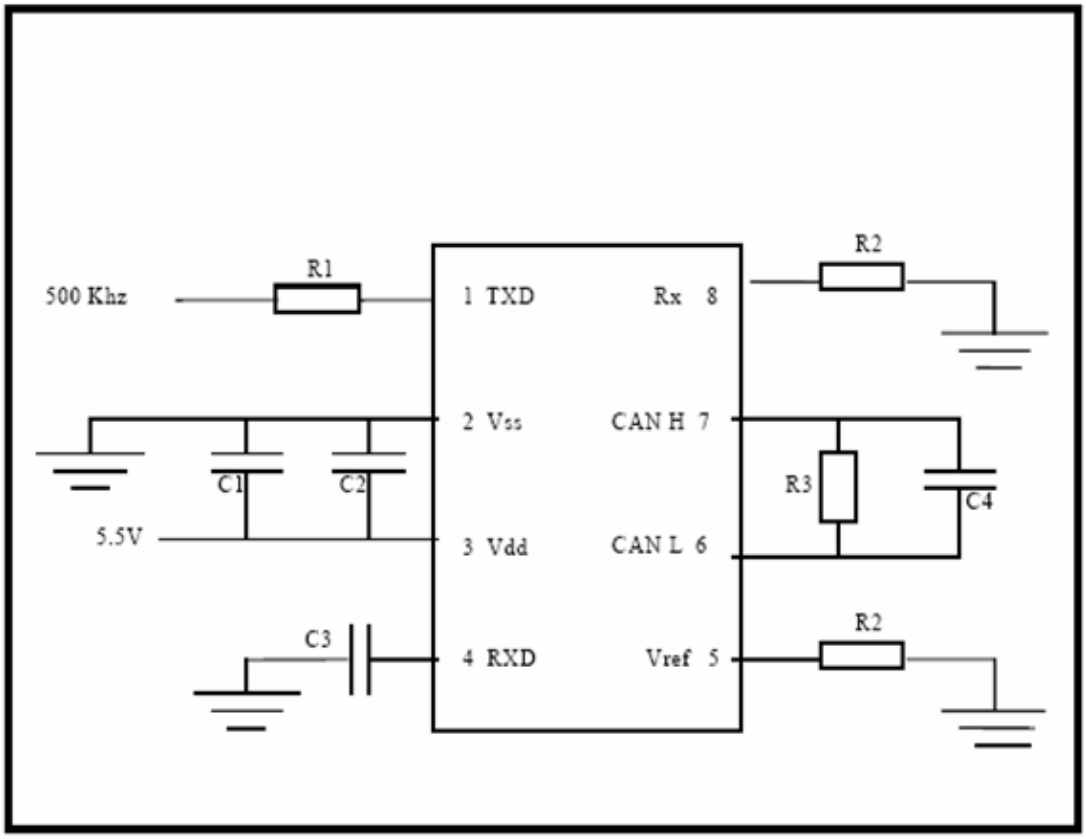
Visit the Microchip Technology Inc. website at www.microchip.com for the most recent package reliability data.

Conclusion

Based on the results, the MCP2551 complies with the reliability guidelines specified in Microchip specification QCI-39000, “Worldwide Quality Conformance Requirements”. Therefore, this qualification will release the MCP2551 to production.

Appendix A – Dynamic Life Burn-In Schematic

VK001 HIGH TEMPERATURE DYNAMIC LIFE TEST
BURN-IN SCHEMATIC FOR 8LD SOIC



Vdd = 5.5V	Vss = 0V
R1 = 1.0K Ohms	C1 = 0.1 uF
R2 = 47K Ohms	C2 = 1 uF
R3 = 60K Ohms	C3 = 30 uF
	C4 = 100 pF

NOTES:

MCP1791, MCP1790
PRODUCT QUALIFICATION REPORT

Document Control # C-1109270
NOVEMBER 10, 2009

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SUMMARY PRODUCT QUALIFICATION REPORT

Document Control #: C-1109270

Document Revision: A

Purpose: WAFER FAB FOUNDRY CX08HI PROCESS QUALIFICATION

Device(s): MCP1791, MCP1790

Mask Identification #: VKAB1

Process: CX08HI Process

MSL: 593

Date: November 10, 2009

	Name	Title	Date
Author	C. Desai	Reliability Engineer	November 10, 2009
Approved by	C.K. Barlingay	Reliability Manager	November 10, 2009
Approved by	P. Jaconelli	Product Engineer	November 10, 2009

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Overview

The purpose of this report is to verify that qualification testing was performed in accordance with Microchip specification QCI-39000, “Worldwide Quality Conformance Requirements”.

Qualification Plan and Descriptions

In keeping with guidelines established in Microchip specification QCI-39000, a minimum of one production lots were used for qualification testing of the MCP1790. This qualification will release the MCP1791 and MCP1790 by similarity to production. A detailed qualification plan is listed below along with descriptions of each test.

Early Life Failure Rate (ELFR) Test
This test is designed to accelerate random failure modes that may occur during initial operation. Devices were programmed with a burn-in pattern and were exercised at a high ambient temperature to simulate field life.

One lot of MCP1791 was subjected to 48 hours of ELFR testing at 125^{o}C.

High Temperature Operating Life (HTOL) / Dynamic Life Testing (DLT)
This test is designed to accelerate random failure modes which may occur during normal operation. Devices are programmed with a burn-in program and exercised at a high ambient temperature to simulate field life.

One lot of MCP1791 was subjected to 1008 hours of dynamic life burn-in at 125^{o}C.

Electrostatic Discharge (ESD) Test Using Human Body Model (HBM) and Machine Model (MM)
This test is conducted to determine the sensitivity of the input protection circuitry to electrostatic discharge. Human Body Model tests are conducted according to EIA/JESD22-A114 and Machine Model tests are performed in accordance with EIA/JESD22-A115 (Microchip Specification QCI-30510).

One lot of MCP1791 was tested to determine susceptibility to ESD.

Latch-Up (LU) Over Current Testing
This test is employed to determine the sensitivity of a device to overshoots in input and output signals (also called transients) with respect to V_{dd} and Ground. The current injection method is used per Microchip standard QCI-30521. This test is performed at 25^{o}C and 125^{o}C.

One lot of MCP1791 was tested to determine latch up susceptibility.

Test Conditions

Tests are performed in accordance with Microchip specification QCI-39000, “Worldwide Quality Conformance Requirements”. The various conditions are listed below.

TEST	METHOD	CONDITION	SAMPLE SIZE RUN	CRITERIA
Early Life Failure Rate (ELFR)	AEC-Q100	125°C, 48 Hrs. Electrical Test at +25°C and +125°C	898	0/800 per lot
High Temperature Operating Life / Dynamic Life Test	MIL-STD 883 Method 1005	125°C, 1008 Hrs Electrical Test at -40°C, +25°C and +125°C.	610	0/600 per lot
ESD Human Body Model	EIA/JESD22 -A114	1.5K Ohm, 100 pF Electrical Test at +25°C and +125°C.	12	2000 V 1 Lot
ESD Machine Model	EIA/JESD22 -A115	0 Ohm, 200 pF Electrical Test at +25°C and +125°C.	12	200 V 1 Lot
Latch-up Testing	QCI-30521	Trigger Voltage Limit = $1.5*V_{max}$ (not to exceed V_{abs}) Pulse Width = 5 ms Rise/Fall Time = 500 us Test at +25°C and +125°C	 6 6	1 Lot 100 mA (0/6) 100 mA (0/6)

Reliability Results

The results of the tests performed are presented below.

Qualification Material

Information regarding the devices that were used in this qualification is shown in the table below.

LOT	LOT 1	LOT 2
DEVICE	MCP1791	MCP1790
MASK, REV	VKAB1, A1	VKAB0, A1
WAFER PROCESS	Foundry CX08HI	Foundry CX08HI
WAFER LOT	XFGM909339684.200	XFGM909339685.000
ASSEMBLY LOT	MTAI093901479.000	N/A
PACKAGE	8L SOIC	8L Side Brazed
ASSEMBLY SITE	MTAI	N/A
FINAL TEST	MICROCHIP THAILAND	MICROCHIP CHANDLER
QUAL #	R09002	N/A
CN #	C119530	N/A
QUAL TESTS	ELFR / DLT	ESD/ LATCH- UP

Die Level Results

The results of die level testing are shown below.

EARLY LIFE FAILURE RATE (ELFR) AT 125°C	
	48 Hours
Lot 1	0/901[a]

[a] Three devices were discounted due to visual/mechanical damage

DYNAMIC LIFE TESTING AT 125°C		
	168 Hours	1008 Hours
Lot 1	0/620[c]	0/614[d]

[c] Six devices were removed due to visual/mechanical damage.

[d] Four devices were removed due to visual/mechanical damage and one device failed due to EOS was discounted, FA T09023.

ELECTROSTATIC DISCHARGE TEST		
	Human Body Model	Machine Model
Lot 2	6000V	400V

LATCH-UP OVER CURRENT TEST		
	@ 25^{O}C	@ 125^{O}C
Lot 2	Passed	Passed

Note: All pins meet or exceed QCI-39000 guidelines.

Package Reliability

Visit the Microchip Technology Inc. website at www.microchip.com for the most recent package reliability data.

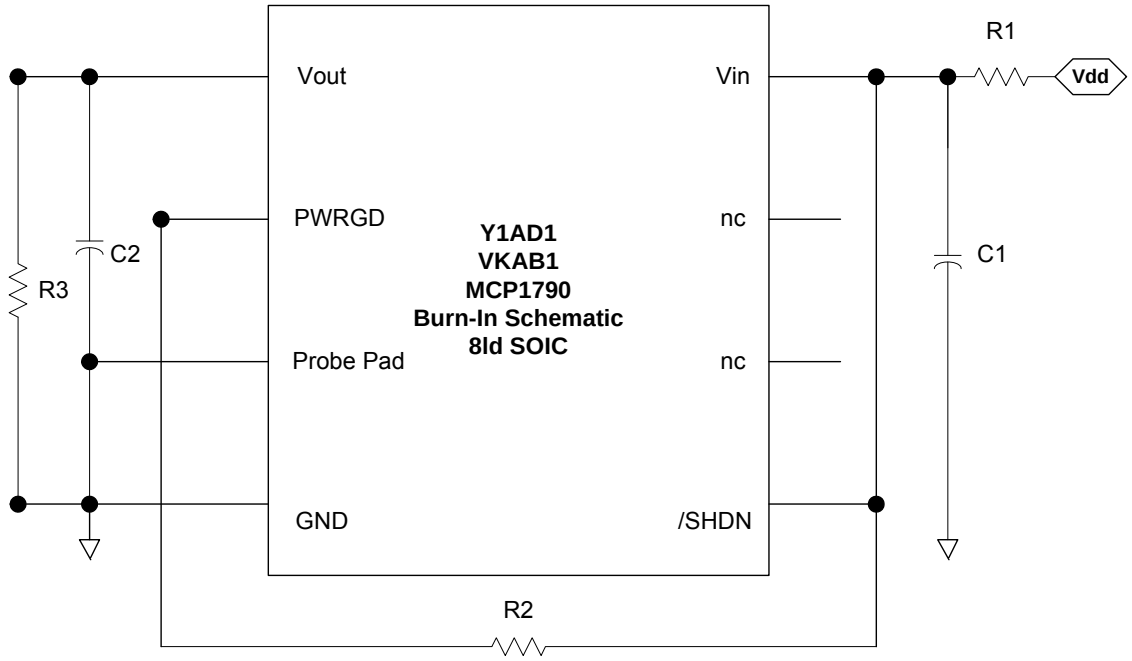
Conclusion

Based on the results, the MCP1791 complies with the reliability guidelines specified in Microchip specification QCI-39000, “Worldwide Quality Conformance Requirements”. Therefore, this qualification will release the MCP1791 and MCP1790 by similarity to production.

Appendix A – Dynamic Life Burn-In Schematic

**VKAB1 HIGH TEMPERATURE DYNAMIC LIFE TEST
BURN-IN SCHEMATIC FOR 8LD SOIC**

Y1AD1/VKAB1 Burn-In Schematic
8LD SOIC



Special Instructions:
R1=100Ω
R2=20KΩ
R3=1KΩ
C1=10µF
C2=4.7 µF

NOTES: