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Product Change Notification - CYER-19JIVU491

Date: 19 Apr 2010

Product Category: RF and Security; Analog (Linear & Mixed Signal) AND Interface; Touch Sensing Technologies; Analog (Thermal, Power Management & Safety); 8-bit Microcontrollers

Device Family:  

Notification subject: CCB 958: Qualification of the 14L & 16L SOIC (.150) at GTK (GRTK) assembly site.

Notification text:

PCN Status:
Initial notification

Microchip Part#s Affected:
See attachments of Affected Part Numbers Labeled as...
PCN_CYER-19JIVU491_Affected_CPN.xls
PCN_CYER-19JIVU491_Affected_CPN.pdf

Description of Change:
Qualification of the 14L & 16L SOIC (.150) at GTK (GRTK) assembly site.

Impacts to Data Sheet:
None

Reason for Change:
To improve on-time delivery performance

Change Implementation Status:
In Progress

Estimated First Ship Date:
July 30, 2010 (1031)

NOTE: Please be advised that during the transition period customers may receive pre and post change parts, due to existing inventory of the pre changed parts.

Markings to Distinguish Revised from Unrevised Devices: (e.g.: Date Code, Device Marking, Ship Container Marking)
Traceability code

Attachment(s): [PCN_CYER-19JIVU491_Affected_CPN.pdf](#)
[PCN_CYER-19JIVU491_Affected_CPN.xls](#)
[PCN_CYER-19JIVU491_Qual Plan.pdf](#)

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PCN_CYER-19JIVU491
CATALOG_PART_NBR
91001BS16TF
HA1504-I/SL
HA1504T-I/SL
HA1508-I/SL
HA1508-I/SL023
HA1508T-I/SL
HA1508T-I/SL023
HA2038-I/SL
HA2038T-I/SL
HA2089-I/SL
HA2089T-I/SL
HA2089T-I/SL040
HA2089T-I/SL043
HA2089T-I/SL054
HA2089T-I/SL057
HA2089T-I/SL077
HA5501-I/SL
HA5501T-I/SL
HA9698-I/SL044
HCS370/SL
HCS370-I/SL
HCS370T/SL
HCS370T-I/SL
HCS370T-I/SL076
HCS515/SL
HCS515-I/SL
HCS515-I/SLA56
HCS515T/SL
HCS515T-I/SL
HCS515T-I/SL022
HCS515T-I/SL024
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MCP2022-500E/SL
MCP2022T-330E/SL
MCP2022T-500E/SL
MCP2030A-I/SL
MCP2030AT-I/SL
MCP2030-I/SL
MCP2030T-I/SL
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PIC16F684T-I/SLC15
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PIC16LC505-04I/SL
PIC16LC505-04I/SLGD83
PIC16LC505T-04/SL
PIC16LC505T-04I/SL
PIC16LC505T-04I/SL120
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TC1021CEOR
TC1021CEORTR
TC1027CEOR
TC1027CEORTR
TC9400COD
TC9400COD713
TC9400EOD
TC9400IOD



MICROCHIP

QUALIFICATION PLAN

PCN#: CYER-19JIVU491

**Date:
March 12, 2010**

**Qualification of 16L SOIC (.150) at GTK (GRTK)
assembly site and the 14L SOIC (.150) will qualify by
similarity.**

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Purpose: _____ Qualification of 16L SOIC (.150) at GTK (GRTK) assembly site. The 14L SOIC (.150) will qualify by similarity.

Mask: _____ VQAA27D7XA00

Part No.: _____ RE46C119

CCB#: _____ 958

Package:

Type _____ 16L SOIC .150"

Die thickness: _____ 15 mils

Die size: _____ 81.1 x 87.4 mils

Lead frame:

Paddle size: _____ 95x110 mils

Material _____ C194 /Fu Sheng (Taiwan)

Surface _____ Bare Cu

Process _____ Stamped

Lead Lock _____ No

Part Number _____ 11-0216N-004

Wire:

Material _____ Au / Sumitomo (Japan)

Die Attach Epoxy:

Part Number _____ CRM 1076DJ-G / Sumitomo (Japan)

Conductive _____ Yes

Mold Compound: _____ G600F / Sumitomo (Taiwan)

Package Reliability Tests

Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Quantity of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
Standard Pb-free Solderability	JESD22B-102E; Perform 8 hour steam aging for Matte tin finish and 1 hr steam aging for NiPdAu finish prior to testing.	22	5	1	27	> 95% lead coverage	5	
Backward Solderability	JESD22B-102E; Perform 8 hour steam aging for Matte tin finish and 1 hr steam aging for NiPdAu finish prior to testing. Backward: Matte tin/ NiPdAu finish, SnPb solder, wetting temp 215°C for SMD.	22	5	1	27	> 95% lead coverage	5	

Package Reliability Tests

Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Quantity of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
Wire Bond Pull - WBP	Mil. Std. 883-2011	5	0	1	5	0 fails after TC	5	30 bonds from a min. 5 devices.
Wire Bond Shear - WBS	CDF-AEC-Q100-001	5	0	1	5		5	30 bonds from a min. 5 devices.
Bond Line Thickness (BLT) robustness assessment						>0.5 mils		
Wire Sweep								Required for any reduction in wire bond thickness.
Physical Dimensions	Measure per JESD22 B100 and B108	10	0	3	30	0	5	
External Visual	Mil. Std. 883-2009/2010	ALL	0	3	ALL	0	5	

Package Reliability Tests

Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Quantity of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
HTSL (High Temp Storage Life)	+175°C for 504 hours or 150°C for 1008 hrs. Electrical test pre and post stress at +25C	45	5	3	150	0	10	
Preconditioning - * Required for surface mount devices	+150°C Bake for 24 hours, moisture loading requirements per MSL level + 3X reflow at peak reflow temperature per Jedec-STD-020C for package type; Electrical test pre and post stress at +25°C. Perform SAM analysis using the standard sample size. MSL1 @ 260°C	231	15	3	738	0	15	Spares should be properly identified. 77 parts from each lot to be used for HAST, Autoclave, Temp Cycle test.

Package Reliability Tests

Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Quantity of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
HAST *	+130° C/85% RH for 96 hours. Electrical test pre and post stress at +25	77	5	3	246	0	10	Spares should be properly identified. Use the parts which have gone through Pre-conditioning.
Autoclave *	+121° C/15 psig for 96 hours. Electrical test pre and post stress at +25° C	77	5	3	246	0	10	Spares should be properly identified. Use the parts which have gone through Pre-conditioning.
Temp Cycle*	-65°C to +150°C for 500 cycles. Electrical test pre and post stress at hot temp; 3 gram force WBP, on 5 devices from 1 lot, test following Temp Cycle stress.	77	5	3	246	0	15	Spares should be properly identified. Use the parts which have gone through Pre-conditioning. For hot temp testing, pre/post test 1 lot at 85° C.