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Product Change Notification - SYST-03BQQP739

Date: 03 Aug 2011

Product Category: 8-bit Microcontrollers

Device Family:

Notification subject: Data Sheet - dsPIC33EPXXXMU806/810/814 and PIC24EPXXXGU810/814 Data Sheet Data Sheet Document Revision

Notification text:

SYST-03BQQP739

Microchip has released a new DeviceDoc for the dsPIC33EPXXXMU806/810/814 and PIC24EPXXXGU810/814 Data Sheet of devices. If you are using one of these devices please read the document located at dsPIC33EPXXXMU806/810/814 and PIC24EPXXXGU810/814 Data Sheet.

Notification Status: Final

Description of Change: The Data Converter Interface (DCI) module is available on all dsPIC33EPXXXMU806/810/814 and PIC24EPXXXGU810/814 devices. References throughout the document have been updated accordingly. The following pin name changes were implemented throughout the document: C1INA renamed to C1IN1+ C1INB renamed to C1IN2- C1INC renamed to C1IN1- C1IND renamed to C1IN3- C2INA renamed to C2IN1+ C2INB renamed to C2IN2- C2INC renamed to C2IN1- C2IND renamed to C2IN3- C3INA renamed to C3IN1+ C3INB renamed to C3IN2- C3INC renamed to C3IN1- C3IND renamed to C3IN3- Section 1.0 “Device Overview" Added Section 1.1 “Referenced Sources”. Section 2.0 “Guidelines for Getting Started with 16-bit Digital Signal Controllers and Microcontrollers” Updated the Note in Section 2.1 “Basic Connection Requirements”. Section 3.0 “CPU” Updated Section 3.1 “Registers”. Section 4.0 “Memory Organization” Updated FIGURE 4-3: “Data Memory Map for dsPIC33EP512MU810/814 Devices with 52 Kb RAM” and FIGURE 4-5: “Data Memory Map for dsPIC33EP256MU806/810/814 Devices with 28 Kb RAM”. Updated the IFS3, IEC3, IPC14, and IPC15 SFRs in the Interrupt Controller Register Map (see Table 4-6). Updated the SMPI bits for the AD1CON2 and AD2CON2 SFRs in the ADC1 and ADC2 Register Map (see Table 4-23). Updated the All Resets values for the CLKDIV and PLLFBD SFRs and removed the SBOREN bit in the System Control Register Map(see Table 4-43). Section 6.0 “Resets” Removed the SBOREN bit and Notes 3 and 4 from the Reset Control Register (see Register 6-1). Section 8.0 “Direct Memory Access (DMA)” Removed Note 2 from the DMA Channel x IRQ Select Register (see Register 8-2). Section 9.0 “Oscillator Configuration” Updated the PLL Block Diagram (see Figure 9-2). Updated the value at PORT and the default designations for the DOZE<2:0>, FRCDIV<2:0>, and PLLPOST<1:0> bits in the Clock Divisor Register and the PLLDIV<8:0> bits in the PLLFBD register (see Register 9-2 and Register 9-3). Section 23.0 “10-bit/12-bit Analog-to-Digital Converter (ADC)” Added Note 4 and updated the ADC Buffer names in the ADCx Module Block Diagram (see Figure 23-1). Added Note 3 to the ADCx Control Register 1 (see Register 23-1). Added the new ADC2 Control Register 2 (see Register 23-2). Updated the SMPI<4:0> bit value definitions in the ADC1 Control Register 2 (see Register 23-3). Section 25.0 “Comparator Module” Updated the Comparator I/O Operating Modes diagram (see Figure 25-1). Added Note 2 to the Comparator Voltage Reference Control Register (see Register 25-6). Section 29.0 “Special Features” Added Note 3 to the Connections for the On-chip Voltage Regulator (see Figure 29-1). Section 32.0 “Electrical Characteristics” Removed the Voltage on Vcap with respect to Vss from the Absolute Maximum Ratings(1). Removed Note 3 and parameter DC18 from the DC Temperature and Voltage Specifications (see Table 32-4). Updated the notes in the DC Characteristics: Operating Current (Idd)(see Table 32-5). Updated the notes in the DC Characteristics: Idle Current (Iidle)(see Table 32-6). Updated the Typical and Maximum values for parameter DC60c and the notes in the DC Characteristics: Power-down Current (Ipd) (see Table 32-7). Updated the notes in the DC Characteristics: Doze Current (Idoze)(see Table 32-8). Updated the conditions for parameters DI60a and DI60b (see Table 32-9). Updated the conditions for parameter BO10 in the BOR Electrical Characteristics (see Table 32-10). Added Note 1 to the Internal Voltage Regulator Specifications(see Table 32-13). Updated the Minimum and Maximum values for parameter OS53 in the PLL Clock Timing Specifications (see Table 32-17). Updated the Minimum and Maximum values for parameter F21b in the Internal LPRC Accuracy specifications (see Table 32-20). Added Note 2 to the ADC Module Specifications (see Table 32-54).

Pre Change: N/A

Post Change: N/A

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 03 Aug 2011

NOTE: Please be advised that this is a change to the document only the product has not been changed..

Markings to Distinguish Revised from Unrevised Devices:N/A

Attachment(s): dsPIC33EPXXXMU806/810/814 and PIC24EPXXXGU810/814 Data Sheet

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Parts Affected

PIC24EP512GU814
dsPIC33EP256MU814
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