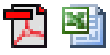
MICROCHIP — A Leading Provider of Microcontrollers & Analog Semiconductors

Date:	10 Oct 2012
Product Category:	Memory
Device Family:	
Notification subject:	CCB 1175 New Fabrication Site Initial Notice: Qualification of the SST39VF3201C and SST39VF3202C device families at a new wafer fabrication site.
Notification text:	PCN Status: Initial notification Microchip Parts Affected: See attachments of affected catalog part numbers (CPN) labeled as… PCN_CYER-01SVUF279_Affected_CPN.xls PCN_CYER-01SVUF279_Affected_CPN.pdf Description of Change: Qualification of the SST39VF3201C and SST39VF3202C device families at a new wafer fabrication site. Impacts to Data Sheet: None Reason for Change: To improve productivity Change Implementation Status: In Progress Estimated First Ship Date: January 31, 2013 (date code: 1305) NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts. Markings to Distinguish Revised from Unrevised Devices: Traceability code Revision History: October 10, 2012: Issued initial notification. The change described in this PCN does not alter Microchip's current regulatory compliance regarding the material content of the applicable

products.

Attachment(s): PCN_CYER-01SVUF279_Affected_CPN.xls PCN_CYER-01SVUF279_Affected_CPN.pdf PCN_CYER-01SVUF279_Qual Plan.pdf

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to change your product/process change notification (PCN) profile please log on to our website at http://www.microchip.com/PCN sign into myMICROCHIP to open the myMICROCHIP home page, then select a profile option from the left navigation bar.

To opt out of future offer or information emails (other than product change notification emails), click here to go to microchipDIRECT and login, then click on the "My account" link, click on "Update profile" and un-check the box that states "Future offers or information about Microchip's products or services."

Product Change Notification - CYER-01SVUF279

CYER-01SVUF279 - CCB 1175 New Fabrication Site Initial Notice: Qualification of the SST39VF3201C and SST39VF3202C device families at a new wafer fabrication site.

Parts Affected

SST39VF3201C
SST39VF3202C

Date: Wednesday, October 10, 2012

PCN_CYER-01SVUF279
CATALOG_PART_NBR
SST39VF3201C-70-4I-B3KE
SST39VF3201C-70-4I-B3KE-T
SST39VF3201C-70-4I-EKE
SST39VF3201C-70-4I-EKE-T
SST39VF3202C-70-4I-B3KE
SST39VF3202C-70-4I-B3KE-T
SST39VF3202C-70-4I-EKE
SST39VF3202C-70-4I-EKE-T

QUALIFICATION PLAN

PCN#: CYER-01SVUF279

Date:
10/05/2012

Qualification of the SST39VF3201C and SST39VF3202C device families at an additional wafer fabrication site.

Distribution

Microchip Technology (Thailand) Co., Ltd.
14 Moo 1 T. Wangtakien A. Muangchacherngsao,
Chacherngsao, Thailand, 24000
Tel. (6638) 857119-45, 857311-19 ext. 1231
Fax (6638) 857149-50

Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Qty of Lots	Total Units	Fail Accept Qty	Est. Dur. Days
ELFR	+150°C for 24 hour; Electrical test pre and post stress at -40°C, +25°C and +85°C temp.	800	5	3	2415	0	15
DLT	+150°C for 408 hours; Electrical test pre and post stress at -40°C, +25°C, and +85°C temp. Readout at 408 hours (samples from ELFR)	600	5	3	1815	0	35
EDR	10K CE/P whole array at +25°C; Electrical test pre stress at -40°C, +25°C, and +85°C temp. Electrical test post stress at +25°C, and +85°C temp.	400	5	3	1215	0	14
EDR+HTOL	+125°C for 1008 hours; Electrical test pre stress at -40°C, +25°C, and +85°C temp. Electrical test post stress at +25°C, and +85°C temp. Readout at 168, 504 and 1008hours if fresh samples used.	77	5	3	246	0	70
EDR+DRSL	+150°C for 1008 hours; Electrical test pre stress at -40°C, +25°C, and +85°C temp. Electrical test post stress at +25°C, and +85°C temp. Readout at 168, 504 and 1008hours if fresh samples used.	231	5	3	738	0	70
ESD - HBM	Electrical test pre and post stress at 25°C and hot temp. Test at each voltage: 500V, 1KV, 2KV, 4KV	12	0	1	12	0	7

Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Qty of Lots	Total Units	Fail Accept Qty	Est. Dur. Days
ESD - MM	Electrical test pre and post stress at 25°C and hot temp. Test at each voltage: 100V, 200V, 300V, 400V	12	0	1	12	0	7
ESD-CDM	Tested per ESDA STM 5.3.1-1999 spec at 250V, 500V, 750V, 1000V, 1500V, 2000V at 25°C and 85°C.	18	0	1	18	0	7
Latch up	Over voltage and over current. Latch-up stress testing should be performed at room and max operating temperature. Electrical test pre and post stress at 25°C and hot temp per Q100-004.	12	0	1	12	0	7