Date: 09 Mar 2011

Product Category: 8-bit Microcontrollers

Device Family:

Notification subject: ERRATA - PIC12(L)F1822/PIC16(L)F1823 Silicon Errata and Data Sheet Clarification

Notification text:

SYST-09KEQX557

Microchip has released a new DeviceDoc for the PIC12(L)F1822/PIC16(L)F1823 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC12(L)F1822/PIC16(L)F1823 Silicon Errata and Data Sheet Clarification.

Attachment(s): PIC12(L)F1822/PIC16(L)F1823 Silicon Errata and Data Sheet Clarification

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Product Change Notification - SYST-09KEQX557 (Printer Friendly)

Parts Affected

PIC16F1823
PIC12F1822

PIC12(L)F1822/PIC16(L)F1823

PIC12(L)F1822/PIC16(L)F1823 Family Silicon Errata and Data Sheet Clarification

The PIC12(L)F1822/PIC16(L)F1823 family devices that you have received conform functionally to the current Device Data Sheet (DS41413**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC12(L)F1822/PIC16(L)F1823 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A8**).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC12(L)F1822/ PIC16(L)F1823 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A6	A8
PIC12F1822	10 0111 000x xxxx	06h	08h
PIC12LF1822	10 1000 000x xxxx	06h	08h
PIC16F1823	10 0111 001x xxxx	06h	08h
PIC16LF1823	10 1000 001x xxxx	06h	08h

Note 1: The Device ID is located in the last configuration memory space.

2: Refer to the *"PIC16F/LF182X/PIC16F/LF1822 Memory Programming Specification"* (DS41390) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				A6	A8
Oscillator	HS Oscillator	1.1	HS Oscillator min. VDD.	X	
ADC	Analog-to-Digital Converter	2.1	ADC conversion does not complete.	X	
APFCON	Remappable T1Gate	3.1	T1Gate is not remappable.	X	
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	4.1	PWM 0% duty cycle direction change.	X	
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	4.2	PWM 0% duty cycle port steering.	X	
Clock Switching	OSTS Status Bit	5.1	Remains clear when 4xPLL enabled.	X	X
Timer1 Gate	T1Gate Toggle mode	6.1	T1Gate Flip-Flop does not clear.	X	X
In-Circuit Serial Program-ming™ (ICSP™)	Low-Voltage Programming	7.1	Bulk Erase not available with LVP.	X	
BOR	Wake-up from Sleep	8.1	Device may BOR Reset when waking-up from Sleep.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A8**).

1. Module: Oscillator

1.1 HS Oscillator

The HS oscillator requires a minimum voltage of 3.0 volts (at 65°C or less) to operate at 20 MHz.

Work around

None.

Affected Silicon Revisions

A6	A8						
X							

2. Module: ADC

2.1 Analog-to-Digital Converter (ADC)

Under certain device operating conditions, the ADC conversion may not complete properly. When this occurs, the ADC Interrupt Flag (ADIF) does not get set, the GO/$\overline{\text{DONE}}$ bit does not get cleared and the conversion result does not get loaded into the ADRESH and ADRESL result registers.

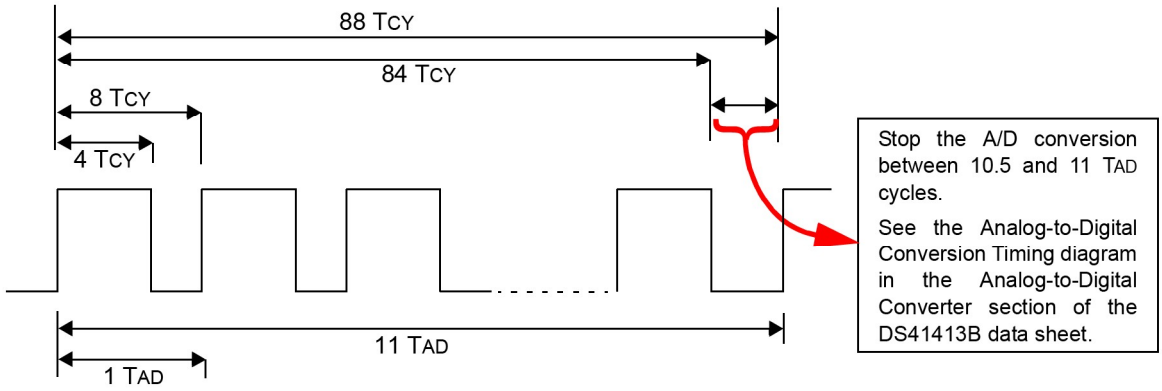
Work around

Method 1: Select the dedicated RC oscillator as the ADC conversion clock source, and perform all conversions with the device in Sleep.

Method 2: Provide a fixed delay in software to stop the A-to-D conversion manually, after all 10 bits are converted, but before the conversion would complete automatically. The conversion is stopped by clearing the GO/$\overline{\text{DONE}}$ bit in software. The GO/$\overline{\text{DONE}}$ bit must be cleared during the last ½ TAD cycle, before the conversion would have completed automatically. Refer to Figure 1 for details.

FIGURE 1: INSTRUCTION CYCLE DELAY CALCULATION EXAMPLE

FOSC = 32 MHz
TCY = 4/32 MHz = 125 nsec
TAD = 1 µsec, ADCS = FOSC/32



See the ADC Clock Period (TAD) vs. Device Operating Frequencies table, in the Analog-to-Digital Converter section of the DS41413B data sheet.

In Figure 1, 88 instruction cycles (TCY) will be required to complete the full conversion. Each TAD cycle consists of 8 TCY periods. A fixed delay is provided to stop the A/D conversion after 86 instruction cycles and terminate the conversion at the correct time as shown in the figure above.

Note: The exact delay time will depend on the choice of FOSC and the TAD divisor (ADCS) selection. The TCY counts shown in the timing diagram above apply to this example only. Refer to Table 3 for the required delay counts for other configurations.

EXAMPLE 1: CODE EXAMPLE OF INSTRUCTION CYCLE DELAY

```
BSF    ADCON0, GO/DONE; Start ADC conversion
                      ; Provide 86
                        instruction cycle
                        delay here
BCF    ADCON0, GO/DONE; Terminate the
                        conversion manually
MOVF   ADRESH, W      ; Read conversion
                        result
```

For other combinations of FOSC, TAD values and instruction cycle delay counts, refer to Table 3.

TABLE 3: INSTRUCTION CYCLE DELAY COUNTS FOR OTHER FOSC AND TAD COMBINATIONS

FOSC	TAD	Instruction Cycle Delay Counts
32 MHz	FOSC/64	172
	FOSC/32	86
16 MHz	FOSC/64	172
	FOSC/32	86
	FOSC/16	43
8 MHz	FOSC/32	86
	FOSC/16	43

Affected Silicon Revisions

A6	A8						
X							

3. Module: APFCON

3.1 Timer1 Gate

The APFCON register is normally used to remap the T1 Gate to an alternate pin. The T1GSEL bit of the APFCON register is found to be not writable and therefore the T1Gate pin cannot be remapped. The default value for the T1GSEL bit is 0 and, therefore, the T1Gate will be found on RA4. This affects the PIC16(L)F1823 devices only.

Work around

None.

Affected Silicon Revisions

A6	A8						
X							

4. Module: Enhanced Capture Compare PWM (ECCP)

4.1 Enhanced PWM

When the PWM is configured for Full-Bridge mode and the duty cycle is set to 0%, writing the PxM<1:0> bits to change the direction has no effect on PxA and PxC outputs.

Work around

Increase the duty cycle to a value greater than 0% before changing directions.

Affected Silicon Revisions

A6	A8						
X							

4.2 Enhanced PWM

In PWM mode, when the duty cycle is set to 0% and the STRxSYNC bit is set, writing the STRxA, STRxB, STRxC and the STRxD bits to enable/disable steering to port pins has no effect on the outputs.

Work around

Increase the duty cycle to a value greater than 0% before enabling/disabling steering to port pins.

Affected Silicon Revisions

A6	A8						
X							

5. Module: Clock Switching

5.1 OSTS Status Bit

When the 4xPLL is enabled, the Oscillator Start-up Time-out Status (OSTS) bit always remains clear.

Work around

None.

Affected Silicon Revisions

A6	A8						
X	X						

6. Module: Timer1 Gate

6.1 Timer1 Gate Toggle mode

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 Gate signal. To perform this function, the Timer1 Gate source is routed through a flip-flop that changes state on every incrementing edge of the gate signal. Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When working properly, clearing either the T1GTM bit or the TMR1ON bit would also clear the output value of this flip-flop, and hold it clear. This is done in order to control which edge is being measured. The issue that exists is that clearing the TMR1ON bit does not clear the output value of the flip-flop and hold it clear.

Work around

Clear the T1GTM bit in the T1GCON register to clear and hold clear the output value of the flip-flop.

Affected Silicon Revisions

A6	A8						
X	X						

7. Module: In-Circuit Serial Programming™ (ICSP™)

7.1 Low-Voltage Programming

The Bulk Erase feature is not available with Low-Voltage Programming mode.

A Bulk Erase of the program Flash memory or data memory cannot be executed in Low-Voltage Programming mode.

Work around

Method 1: If ICSP Low-Voltage Programming mode is required, use row erases to erase the program memory, as described in the Program/Verify mode section of the Programming Specification. Data memory must be overwritten with the desired values.

Method 2: Use the ICSP High-Voltage Programming mode if a Bulk Erase is required.

Note: Only the Bulk Erase feature will erase the program or data memory if the code or data protection is enabled. Method 2 must be used if the code or data protection is enabled.

Affected Silicon Revisions

A6	A8						
X							

8. Module: BOR

8.1 BOR Reset

This issue affects only the PIC12(L)F1822/ PIC16(L)F1823 devices. The device may undergo a BOR Reset when waking-up from Sleep and BOR is re-enabled. A BOR Reset may also occur the moment the software BOR is enabled.

Under certain voltage and temperature conditions and when either SBODEN or BOR_NSLEEP is selected, the devices may occasionally reset when waking-up from Sleep or BOR is enabled.

Work around

Method 1: In applications where BOR use is not critical, turn off the BOR in the Configuration Word.

Method 2: Set the FVREN bit of the FVRCON register. Maintain this bit on at all times.

Method 3: When BOR module is needed only during run-time, use the software-enabled BOR by setting the SBODEN option on the Configuration Word. BOR should be turned off by software before Sleep, then follow the below sequence for turning BOR on after Wake-up:

a. Wake-up event occurs;

b. Turn on FVR (FVREN bit of the FVRCON register);

c. Wait until FVRRDY bit is set;

d. Wait 15 µs after the FVR Ready bit is set;

e. Manually turn on the BOR.

Method 4: Use the software-enabled BOR as described in Method 3, but use the following sequence:

a. Switch to internal 32 kHz oscillator immediately before Sleep;

b. Upon wake-up, turn on FVR (FVREN bit of the FVRCON register);

c. Manually turn on the BOR;

d. Switch the clock back to the preferred clock source.

Note:	When using the software BOR follow the steps in Methods 3 or 4 above when enabling BOR for the first time during program execution.

Affected Silicon Revisions

A6	A8						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41413**B**):

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2010)

Initial release of this document.

Rev B Document (11/2010)

Updated errata to the new format; Added Silicon Revision A8; Added Module 5: Clock Switching.

Rev C Document (03/2011)

Added Modules 6, 7 and 8.

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