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Product Change Notification - SYST-22DREG067

Date:	22 May 2010
Product Category:	8-bit Microcontrollers
Device Family:	
Notification subject:	ERRATA - PIC16F631/677/685/687/689/690 Family Silicon Errata and Data Sheet Clarification
Notification text:	SYST-22DREG067 Microchip has released a new DeviceDoc for the PIC16F631/677/685/687/689/690 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC16F631/677/685/687/689/690 Family Silicon Errata and Data Sheet Clarification.
Attachment(s):	PIC16F631/677/685/687/689/690 Family Silicon Errata and Data Sheet Clarification

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Parts Affected

PIC16F677
PIC16F631
PIC16F685
PIC16F687
PIC16F689
PIC16F690

PIC16F631/677/685/687/689/690 Family Silicon Errata and Data Sheet Clarification

The PIC16F631/677/685/687/689/690 family devices that you have received conform functionally to the current Device Data Sheet (DS41262**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2 through Table 6.

The errata described in this document will be addressed in future revisions of the PIC16F631/677/685/687/689/690 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 through Table 6 apply to the current silicon revision.

Data Sheet clarifications and corrections start on page 12, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2, MPLAB ICD 3, PICkit™ 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger, PICkit™ 2 or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Programmer>Select Tool*).
4. Perform a "Connect" operation to the device (*Programmer>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device ID values for the various devices and silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)				
		A1	A3	A4	A5	A6
PIC16F631	142x	1				
PIC16F677	132x	1				
PIC16F685	04Ax		3	4	5	6
PIC16F687	132x		3	4	5	6
PIC16F689	134x		3	4	5	6
PIC16F690	134x		3	4	5	6

Note 1: The device and revision data is stored in the Device ID located at 2006h in program memory.

2: Refer to the *"PIC12F6XX/16F6XX Memory Programming Specification"* (DS41204) for detailed information.

TABLE 2: SILICON ISSUE SUMMARY (PIC16F631)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A1
Timer1	Ext. Crystal	5.1	Overflow may take additional count.	X
Timer1	Ext. Crystal	5.2	Oscillator may stop running at low temps.	X
Timer1	Ext. Crystal	5.3	Sleep in LP mode disables T1OSC.	X
WDT/Timer0	Prescaler	6.	Spurious Reset may occur.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 3: SILICON ISSUE SUMMARY (PIC16F677)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A1
SSP	Start Bit	2.1	Fail to recognize Start bit.	
SSP	SSPIF Flag	2.2	SSPIF flag set on first reception only.	X
ADC/INTOSC	Freq. Disturbance	4.	Oscillator may stop running at low temps.	X
Timer1	Ext. Crystal	5.1	Overflow may take additional count.	X
Timer1	Ext. Crystal	5.2	Oscillator may stop running at low temps.	X
Timer1	Ext. Crystal	5.3	Sleep in LP mode disables T1OSC.	X
WDT/Timer0	Prescaler	6.	Spurious Reset may occur.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 4: SILICON ISSUE SUMMARY (PIC16F685)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A3	A4	A5	A6
ECCP	Auto-Shutdown	3.	Overflow may take additional count.	X	X		
ADC/INTOSC	Freq. Disturbance	4.	Oscillator may stop running at low temps.	X	X	X	X
Timer1	Ext. Crystal	5.1	Overflow may take additional count.	X	X	X	X
Timer1	Ext. Crystal	5.2	Oscillator may stop running at low temps.	X	X	X	X
Timer1	Ext. Crystal	5.3	Sleep in LP mode disables T1OSC.	X	X	X	X
WDT/Timer0	Prescaler	6.	Spurious Reset may occur.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 5: SILICON ISSUE SUMMARY (PIC16F687/PIC16F689)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A3	A4	A5	A6
EUSART	Wake-up	1.1	WUE bit not clearing.	X	X		
EUSART	Auto-Baud	1.2	Incorrect baud rate after a break.	X	X		
EUSART	Auto-Baud	1.3	Baud rate value +2.	X	X		
EUSART	Auto-Baud	1.4	Delay after auto-baud before transmit.	X	X		
EUSART	Auto-Baud	1.5	R/W bit on $\overline{ACK}$.	X	X		
EUSART	Reset	1.6	Clock-stretching handling.	X	X		
EUSART	Extra Character	1.7	Multi-byte transmission.	X	X		
SSP	Start Bit	2.1	Fail to recognize Start bit.	X	X	X	
SSP	SSPIF Flag	2.2	SSPIF flag set on first reception only.	X	X	X	X
ADC/INTOSC	Freq. Disturbance	4.	Oscillator may stop running at low temps.	X	X	X	X
Timer1	Ext. Crystal	5.1	Overflow may take additional count.	X	X	X	X
Timer1	Ext. Crystal	5.2	Oscillator may stop running at low temps.	X	X	X	X
Timer1	Ext. Crystal	5.3	Sleep in LP mode disables T1OSC.	X	X	X	X
WDT/Timer0	Prescaler	6.	Spurious Reset may occur.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 6: SILICON ISSUE SUMMARY (PIC16F690)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A3	A4	A5	A6
EUSART	Wake-up	1.1	WUE bit not clearing.	X	X		
EUSART	Auto-Baud	1.2	Incorrect baud rate after a break.	X	X		
EUSART	Auto-Baud	1.3	Baud rate value +2.	X	X		
EUSART	Auto-Baud	1.4	Delay after auto-baud before transmit.	X	X		
EUSART	Auto-Baud	1.5	R/W bit on $\overline{ACK}$.	X	X		
EUSART	Reset	1.6	Clock-stretching handling.	X	X		
EUSART	Extra Character	1.7	Multi-byte transmission.	X	X		
SSP	Start Bit	2.1	Fail to recognize Start bit.	X	X	X	
SSP	SSPIF Flag	2.2	SSPIF flag set on first reception only.	X	X	X	X
ECCP	Auto-Shutdown	3.	Overflow may take additional count.	X	X	X	X
ADC/INTOSC	Freq. Disturbance	4.	Oscillator may stop running at low temps.	X	X	X	X
Timer1	Ext. Crystal	5.1	Overflow may take additional count.	X	X	X	X
Timer1	Ext. Crystal	5.2	Oscillator may stop running at low temps.	X	X	X	X
Timer1	Ext. Crystal	5.3	Sleep in LP mode disables T1OSC.	X	X	X	X
WDT/Timer0	Prescaler	6.	Spurious Reset may occur.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision.

1. Module: EUSART (PIC16F687/689/690 only)

1.1 WUE Bit is not clearing.

After a wake-up due to a Break character, the WUE bit is not automatically cleared.

Work around

Clear the WUE bit after waking up.

Fix

Rev. A5 Silicon and later revisions.

Affected Silicon Revisions

PIC16F687/PIC16F689/PIC16F690

A3	A4	A5	A6				
X	X						

1.2 Auto-baud captures the incorrect baud rate after a break.

The SPBRGH:SPBRG registers are not being initialized correctly. If WUE and ABDEN are set at the same time and a Break character followed by a Sync character are received, then the calculated baud rate will be random.

Work around

Set WUE and wait for the wake-up to occur.

Clear SPBRGH:SPBRG after waking up with the break.

Set ABDEN to begin the auto-baud process.

Fix

Rev. A5 Silicon and later revisions.

Affected Silicon Revisions

PIC16F687/PIC16F689/PIC16F690

A3	A4	A5	A6				
X	X						

1.3 Auto-baud calculates a baud rate value that is +2.

The SPBRGH:SPBRG are not initialized correctly when ABDEN is set. This causes the measured baud rate to be high by two counts.

Work around

Clearing the SPBRGH:SPBRG registers will correctly initialize the baud rate counter. After the auto-baud has been completed, the baud rate will now be +1. The firmware should now subtract 1 from the Baud Rate Generator to produce the correct baud rate.

Fix

Rev. A5 Silicon and later revisions.

Affected Silicon Revisions

PIC16F687/PIC16F689/PIC16F690

A3	A4	A5	A6				
X	X						

1.4. Delay after auto-baud before transmit is allowed.

After the auto-baud Sync character has been received and the RCIF flag is set, there is approximately 17 ms of delay before the transmitter is enabled.

Work around

After the RCIF flag is set indicating the baud rate has been measured, read the SPBRG register and write the value back to SPBRG. This will terminate the delay, and enable the transmitter module.

Fix

Rev. A5 Silicon and later revisions.

Affected Silicon Revisions

PIC16F687/PIC16F689/PIC16F690

A3	A4	A5	A6				
X	X						

1.5 Auto-baud sequence cannot be aborted in some cases.

If an auto-baud is started but no edges are received, there is no way to leave Auto-Baud mode.

Work around

Use the Watchdog Timer to reset the entire device.

Fix

Rev. A5 Silicon and later revisions.

Affected Silicon Revisions

PIC16F687/PIC16F689/PIC16F690

A3	A4	A5	A6				
X	X						

1.6 Clearing SPEN does not reset EUSART state machine correctly.

When SPEN is cleared, the entire EUSART is frozen. When SPEN is set, the EUSART resumes where it left off. This can cause some unexpected behavior.

Work around

To reset the EUSART, toggle TXEN and CREN after clearing SPEN. This will reset the transmit and receive state machines.

Fix

Rev. A5 Silicon and later revisions.

Affected Silicon Revisions

PIC16F687/PIC16F689/PIC16F690

A3	A4	A5	A6				
X	X						

1.7 Extra character transmitted after auto-baud.

If TXEN is high when ABDEN is set, it will be cleared as soon as the auto-baud process begins, and reset as soon as the auto-baud process completes. When TXEN is reset, the character in the transmit queue will be transmitted.

Work around

Before starting auto-baud, clear TXEN. This will reset the transmit state machine correctly. After the auto-baud is complete and the firmware has brought TXEN high, no character will be transmitted.

Fix

Rev. A5 Silicon and later revisions.

Affected Silicon Revisions

PIC16F687/PIC16F689/PIC16F690

A3	A4	A5	A6				
X	X						

2. Module: SSP (PIC16F687/689/690 only)

2.1 SSP module does not recognize first Start bit received.

In any of the I²C™ modes, the SSP module will fail to recognize the first Start bit received after a transition from module disable to module enable. Subsequent Stop bits and Start bits are detected properly.

Work around

Enable the SSP module in SSPMSK Access mode before changing the mode to the desired I²C operation.

EXAMPLE 1: CODE EXAMPLE

```
MOVLW  B'00111001'  ;Module enable, clock
MOVWF  SSPCON       ;enable, SSPMSK access.
                    ;Optionally load
                    ;address mask value
                    ;into SSPMSK register.
MOVLW  B'00110110'  ;Module enable, clock
MOVWF  SSPCON       ;enable, 7-bit address
                    ;I2C slave.
```

Fix

Rev. A6 Silicon and later revisions.

Affected Silicon Revisions

PIC16F677

A1							

PIC16F687/PIC16F689/PIC16F690

A3	A4	A5	A6				
X	X	X					

2.2 Under certain conditions, the SSPIF flag sets on reception of the first byte.

When all of the following conditions are met:

- The module is configured as a SPI slave
- CKP = 1
- CKE = 1
- Multiple bytes are sent with the $\overline{SS}$ line remaining low between bytes

The SSPIF flag will only be set on reception of the first byte and the following bytes will not be correctly received.

Work around

- Toggle the $\overline{SS}$ line between bytes

or

- On reception of the first byte modify the SSPM bits in the SSPCON register to configure the module as a SPI slave with $\overline{SS}$ pin disabled. Then restore the SSPM bits to the configuration for SPI slave with $\overline{SS}$ pin enabled. The module is then ready for reception of the following byte.

Fix

None.

Affected Silicon Revisions

PIC16F677

A1							
X							

PIC16F687/PIC16F689/PIC16F690

A3	A4	A5	A6				
X	X	X	X				

3. Module: ECCP with Auto-Shutdown (Silicon Rev. A4 and previous revisions) (PIC16F685 and PIC16F690 only)

The PIC16F631/677/685/687/689/690 Rev. A4 silicon for the ECCP auto-shutdown is connected to the C1IF and C2IF flags. See Figures 8-2 and 8-3 on the following page.

The auto-shutdown connection (Rev. A4 and previous) to C1IF and C2IF causes the auto-shutdown to incorrectly operate synchronously. Additionally, reads of CMxCON0 will incorrectly clear an auto-shutdown event.

Work around

Rev. A4 Silicon and previous revisions.

1) Poll the CxOUT bit until it is low.
2) Read CMxCON0 to precondition CxIF.
3) If CMxCON0 is read while CxOUT is changing, repeat steps 1 and 2.

Fix

Rev. A5 Silicon and later revisions.

The Silicon Rev. A5 (now shipping) and later revision devices have moved the auto-shutdown connection from CxIF to CxOUT. This will eliminate the synchronous shutdown and simplify the use of the comparator for a shutdown event. Figure 1 shows the function of auto-shutdown before and after the device revision.

Affected Silicon Revisions

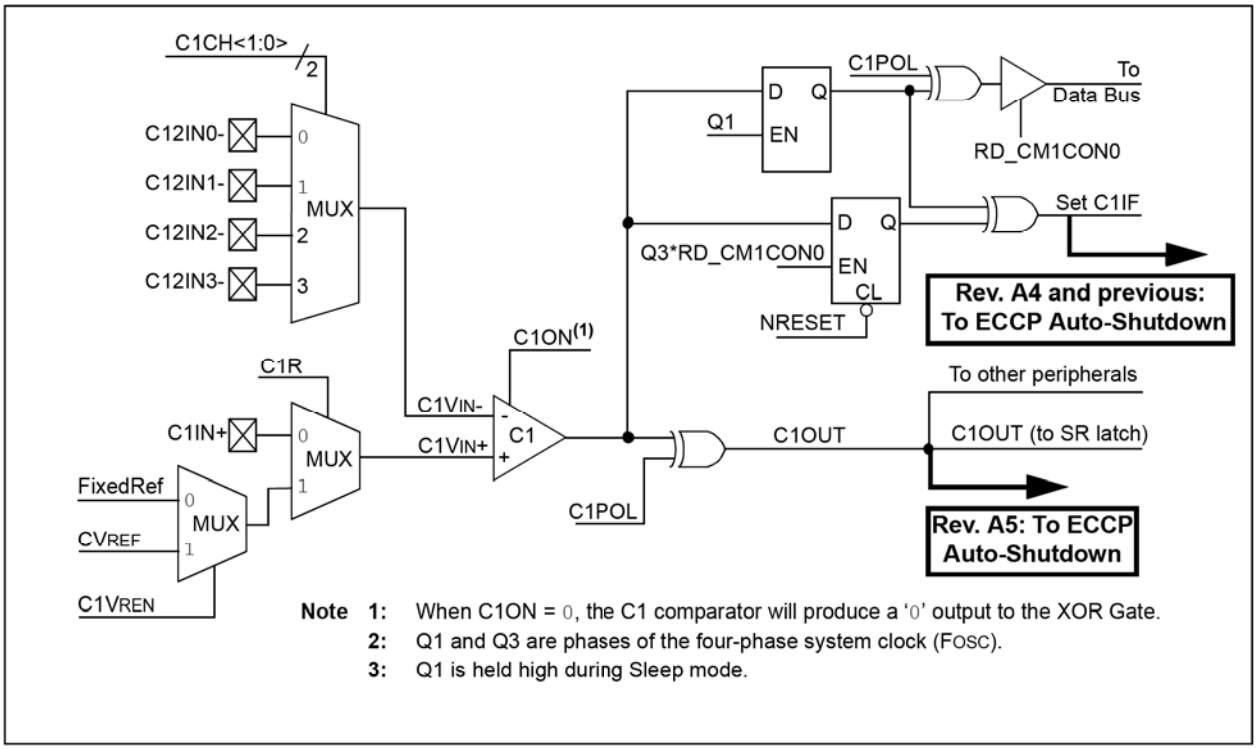
PIC16F685

A3	A4	A5	A6				
X	X						

PIC16F690

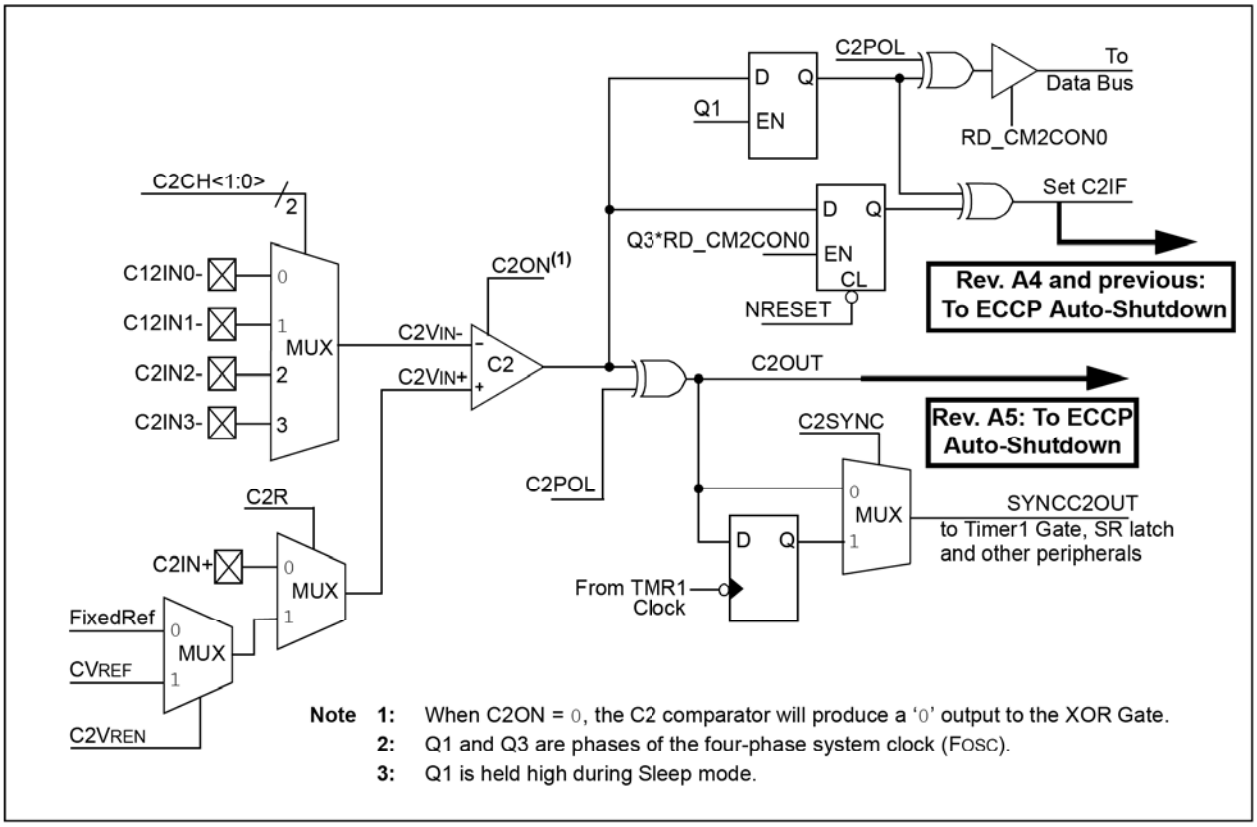
A3	A4	A5	A6				
X	X	X	X				

FIGURE 8-2: COMPARATOR C1 SIMPLIFIED BLOCK DIAGRAM



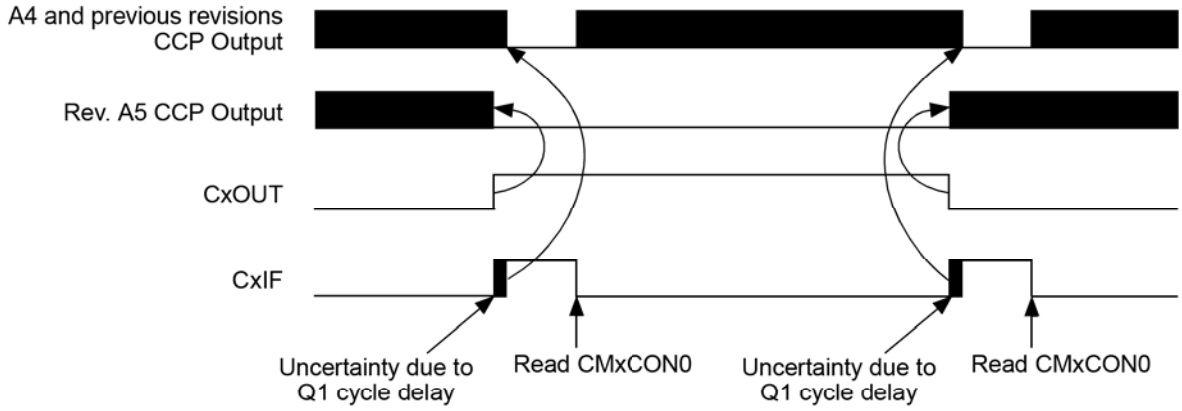
Note 1: When C1ON = 0, the C1 comparator will produce a '0' output to the XOR Gate.
2: Q1 and Q3 are phases of the four-phase system clock (FOSC).
3: Q1 is held high during Sleep mode.

FIGURE 8-3: COMPARATOR C2 SIMPLIFIED BLOCK DIAGRAM



Note 1: When C2ON = 0, the C2 comparator will produce a '0' output to the XOR Gate.
2: Q1 and Q3 are phases of the four-phase system clock (FOSC).
3: Q1 is held high during Sleep mode.

FIGURE 1: SILICON REVISION A4 AND PREVIOUS VS. REVISION A5



4. Module: Analog-To-Digital Converter (ADC) Module (PIC16F685/687/689/690 Only)

Selecting the VP6 reference as the analog input source (CHS<3:0> = 1101) for the ADC conversion after sampling another analog channel with input voltages approximately greater than 1.2V can temporarily disturb the HFINTOSC oscillator.

Note:	This only occurs when selecting the VP6 reference ADC channel using the CHS<3:0> bits in the ADCON0 register and NOT during the start of an actual ADC conversion using the GO/$\overline{\text{DONE}}$ bit in the ADCON0 register.

Work around

Select an ADC channel with input voltages lower than 1.2V prior to selecting the VP6 reference voltage input. Any analog channel can be used, even if that channel is configured as a digital I/O (configured as an output) that is driving the output pin low. An alternative is to configure the CVREF module to output a voltage less than 1.2V and then selecting that analog channel CHS<3:0> = 1100 as the analog input source.

EXAMPLE 2: AVOID DISTURBING THE HFINTOSC OSCILLATOR

```
BANKSEL    ADCON0         ;
MOVLW      B'XX110001'    ;Select ADC
MOVWF      ADCON0         ;Channel CVREF
MOVLW      B'XX110101'    ;Select ADC
MOVWF      ADCON0         ;Channel VP6
```

Silicon Fix

None.

Affected Silicon Revisions

PIC16F677

A1							
X							

PIC16F685/PIC16F687/PIC16F689/ PIC16F690

A3	A4	A5	A6				
X	X	X	X				

5. Module: Timer1

5.1 Asynchronous Timer1

This Errata supersedes Errata DS80233 and DS80329.

When TImer1 is started or updated, the timer needs to see a falling edge from the external clock source before a rising edge can increment the counter. If writes to TMR1H and TMR1L are not completed while the external clock pulse is still high, Timer1 will not count the first clock pulse after the update.

When using an external crystal, the pulse width from rising to falling edge is temperature dependent and may decrease with temperature. As a result, the timer may require an additional oscillation to overflow.

Work around

Switching to the HFINTOSC after reloading, the timer ensures the Timer1 will see a falling edge before switching back to the external clock source.

Due to the time from Timer1 overflow to the reload being application specific, wait for the timer to increment before beginning the reload sequence. This ensures the timer does not miss a rising edge during reload.

Affected Silicon Revisions

PIC16F631/PIC16F677

A1							
X							

PIC16F685/PIC16F687/PIC16F689/ PIC16F690

A3	A4	A5	A6				
X	X	X	X				

EXAMPLE 3:

```
    BTFSC   TMR1L,0
    GOTO    $-1
    BTFSS   TMR1L,0
    GOTO    $-1             ;Timer has just incremented, 31 µs before next rising edge to
                            ;complete reload

Update:

    BCF     T1CON,TMR1CS    ;Select HFINTOSC for Timer1
    BSF     TMR1H,7         ;Timer1 high byte 0x80
    BCF     T1CON,TMR1ON    ;Timer1 off
    BSF     T1CON,TMR1CS    ;Select external crystal
    BCF     T1CON,TMR1ON    ;Timer1 on


    Critical Timing of code sequence for instructions following last write to TMR1L or TMR1H.
```

5.2 LP/Timer1 Oscillator Operation Below 25°C

1-2% of devices experience reduced drive as temperatures approach -40°C. This will result in a loss of Timer1 counts or stopped Timer1 oscillation.

This can also prevent Timer1 oscillator start-up under cold conditions.

Work around

Use of low-power crystals properly matched to the device will reduce the likelihood of failure. A 1MΩ resistor between OSC2 and VDD will further improve the drive strength of the circuit.

Affected Silicon Revisions

PIC16F631/PIC16F677

A1							
X							

PIC16F685/PIC16F687/PIC16F689/ PIC16F690

A3	A4	A5	A6				
X	X	X	X				

5.3 LP/Timer1 Oscillator Shared Operation

When using LP oscillator as the system clock and enabling Timer1 external oscillator, the shared crystal will clock both the core and Timer1. On execution of the SLEEP instruction, the oscillator amplifier will be disabled and Timer1 will not be clocked while the device is in Sleep.

Work around

None.

Affected Silicon Revisions

PIC16F631/PIC16F677

A1							
X							

PIC16F685/PIC16F687/PIC16F689/ PIC16F690

A3	A4	A5	A6				
X	X	X	X				

6. Module: Timer0 and WDT Prescaler Assignment Spurious Reset

A spurious Reset may occur if the Timer0/Watchdog Timer (WDT) prescaler is assigned from the WDT to Timer0 and then back to the WDT.

Summary

The issue only arises when all of the below conditions are met:

- Timer0 external clock input (TOCKI) is enabled.
- The Prescaler is assigned to the WDT, then to the Timer0 and back to the WDT.
- During the assignments, the T0CKI pin is high when bit TOSE is set, or low when TOSE is clear.
- The 1:1 Prescaler option is chosen.

Description

On a POR, the Timer0/WDT prescaler is assigned to the WDT.

If the prescaler is reassigned to Timer0 and Timer0 external clock input (TOCKI) is enabled then the prescaler would be clocked by a transition on the TOCKI pin.

On power-up, the TOCKI pin is (by default) enabled for Timer0 in the OPTION register.

If the T0CKI pin is:

- High and Timer0 is configured to transition on a falling edge (TOSE set), or
- Low and Timer0 is configured to transition on a rising edge (TOSE clear)

Then, if the prescaler is reassigned to the WDT, a clock pulse to the prescaler will be generated on the reassignment.

If the prescaler is configured for the 1:1 option, the clock pulse will incorrectly cause a WDT Time-out Reset of the device.

Work around

1. Disable the Timer0 external clock input by clearing the TOCKI bit in the OPTION register.
2. Modify the TOSE bit in the OPTION register to the opposite configuration for the logic level on the T0CKI pin.
3. Select a prescaler rate other than 1:1 and issue a `CLRWDT` instruction before switching to the final prescaler rate.

Affected Silicon Revisions

PIC16F631/PIC16F677

A1							
X							

PIC16F685/PIC16F687/PIC16F689/ PIC16F690

A3	A4	A5	A6				
X	X	X	X				

Data Sheet Clarifications

The following typographical corrections and clarifications are to be noted for the latest version of the device data sheet (DS41262**E**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Peripheral Features

Corrections to Table 1: PIC16F631 Pin Summary.

TABLE 1: PIC16F631 PIN SUMMARY

I/O	Pin	Analog	Comparators	Timers	Interrupt	Pull-up	Basic
RA0	19	AN0/ULPWU	C1IN+	—	IOC	Y	ICSPDAT
RA1	18	—	C12IN0-	—	IOC	Y	ICSPCLK
RA2	17	—	C1OUT	T0CKI	IOC/INT	Y	—
RA3	4	—	—	—	IOC	Y(1)	$\overline{MCLR}$/VPP
RA4	3	—	—	$\overline{T1G}$	IOC	Y	OSC2/CLKOUT
RA5	2	—	—	T1CKI	IOC	Y	OSC1/CLKIN
RB4	13	—	—	—	IOC	Y	—
RB5	12	—	—	—	IOC	Y	—
RB6	11	—	—	—	IOC	Y	—
RB7	10	—	—	—	IOC	Y	—
RC0	16	—	C2IN+	—	—	—	—
RC1	15	—	C12IN1-	—	—	—	—
RC2	14	—	C12IN2-	—	—	—	—
RC3	7	—	C12IN3-	—	—	—	—
RC4	6	—	C2OUT	—	—	—	—
RC5	5	—	—	—	—	—	—
RC6	8	—	—	—	—	—	—
RC7	9	—	—	—	—	—	—
—	1	—	—	—	—	—	VDD
—	20	—	—	—	—	—	Vss

Note 1: Pull-up enabled only with external $\overline{MCLR}$ configuration.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (7/2005)
Original release of this document.
Clarifications/Corrections to the Data Sheet:
Added Modules 1 through 7:
Module 1: Device VDD Range
Module 2: 4x4 QFN Package Marking
Module 3: Table 1-1: Pinout Description – PIC16F685
Module 4: Register 10-5: EECON1
Module 5: Table11-2: Registers Associated with Capture, Compare and Timer1
Module 6: Section 12.0 EUSART
Module 7: Section 14.2.2 MCLR

Rev B Document (8/2005)
Silicon Section:
Added Module 1: EUSART (PIC16F687/689/690 only).

Clarifications/Corrections to the Data Sheet:
Added Modules 8 and 9:
Module 8: SSP Module Overview
Module 9: Electrical Specifications.

Rev C Document (11/2005)
Silicon Section:
Added Module 2: SSP (PIC16F687/689/690 only)

Rev D Document (01/2006)

Clarifications/Corrections to the Data Sheet:

Replaced the 20-Lead QFN package diagram in Module 2: 4x4 QFN Package Marking.

Rev E Document (7/2006)
Data Sheet Clarifications/Corrections Section: Removed Items 1 through 9, which have been incorporated into the data sheet. Added Item 1, 20-pin QFN Pin Diagram Title change.

Rev F Document (11/2006)
Data Sheet Clarifications/Corrections Section: Added Item 2, Product Identification System, Examples change.

Added Module 3: ECCP with Auto-Shutdown (Silicon Rev. B2). Updated Module1: EUSART (PIC16F687/689/690 only) and Module2: SSP (PIC16F687/689/690 only) with Fix information.

Rev G Document (01/2007)
Removed Rev. A6 reference from Module 2 (SSP).

Data Sheet Clarifications/Corrections Section: Added Module 3, Comparator and Voltage Reference Modules Associated Registers, removed REFCON register reference. Added Module 4: DC Characteristics, Table 17.3, revised Max values.

Rev H Document (07/2007)
Added Module 4: Analog-to-Digital Converter (ADC) Module. Module 2: Added Fix.

Rev J Document (09/2008)
Added Module 2.2: Under certain conditions, the SSPIF flag sets on reception of the first byte (under new 2. SSP (PIC16F687/689/690 only)), while changing Module 2. to 2.1. Revised Module 5: LP/Timer1 Oscillator Operations Below 25°C. Added Module 6: SSP.

Clarifications/Corrections to the Data Sheet:
Removed Modules 1 through 4, which have been included in the latest data sheet revision.

Rev K Document (04/2009)
Updated Errata to new format.

Deleted Module 6: SSP (PIC16F687/689/690).

Added Module 5: Timer1; Added Module 6: Timer0 and WDT Prescaler Assignment Spurious Reset.

Rev L Document (07/2009)

Data Sheet Clarifications: Added Module 1: Peripheral Features (Table 1: PIC16F631 Pin Summary).

Rev M Document (05/2010)

Added Module 5.3.

NOTES:

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