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Product Change Notification - CYER-19JIVU491

Date: 19 Apr 2010
Product Category: RF and Security; Analog (Linear & Mixed Signal) AND Interface; Touch Sensing Technologies; Analog (Thermal, Power Management & Safety); 8-bit Microcontrollers
Device Family:  
Notification subject: CCB 958: Qualification of the 14L & 16L SOIC (.150) at GTK (GRTK) assembly site.
Notification text:

PCN Status:
Initial notification

Microchip Part#s Affected:
See attachments of Affected Part Numbers Labeled as...
[PCN_CYER-19JIVU491_Affected_CPN.xls](#)
[PCN_CYER-19JIVU491_Affected_CPN.pdf](#)

Description of Change:
Qualification of the 14L & 16L SOIC (.150) at GTK (GRTK) assembly site.

Impacts to Data Sheet:
None

Reason for Change:
To improve on-time delivery performance

Change Implementation Status:
In Progress

Estimated First Ship Date:
July 30, 2010 (1031)

NOTE: Please be advised that during the transition period customers may receive pre and post change parts, due to existing inventory of the pre changed parts.

Markings to Distinguish Revised from Unrevised Devices: (e.g.: Date Code, Device Marking, Ship Container Marking)
Traceability code

Attachment(s): [PCN_CYER-19JIVU491_Affected_CPN.pdf](#)
[PCN_CYER-19JIVU491_Affected_CPN.xls](#)
[PCN_CYER-19JIVU491_Qual Plan.pdf](#)

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Parts Affected

HCS370
HCS515
MCP2022
MCP2030
MCP2036
MCP2120
MCP25020
MCP25025
MCP25050
MCP25055
MCP3004
MCP3008
MCP3204
MCP3208
MCP3302
MCP3304
MCP3424
MCP3428
MCP42010
MCP42050
MCP42100
MCP4231
MCP4241
MCP4251
MCP4261
MCP4922
MCP6004
MCP6024
MCP6034
MCP604
MCP6044
MCP6054
MCP6064
MCP6074
MCP609
MCP6144
MCP619
MCP6234
MCP6244
MCP6274
MCP6284
MCP6294
MCP6544
MCP6549

MCP6564
MCP6569
MCP6G04
MCP6L04
MCP6L4
MCP6L74
MCP6L94
MCP6S26
MCP6S28
MCP73861
MCP73862
MCP73863
MCP73864
PIC16C505
PIC16F505
PIC16F506
PIC16F526
PIC16F610
PIC16F616
PIC16F630
PIC16F636
PIC16F676
PIC16F684
PIC16F688
RE46C104
RE46C105
RE46C107
RE46C109
RE46C119
RE46C140
RE46C141
RE46C143
RE46C144
RE46C145
TC1027
TC9400



MICROCHIP

QUALIFICATION PLAN

PCN#: CYER-19JIVU491

**Date:
March 12, 2010**

**Qualification of 16L SOIC (.150) at GTK (GRTK)
assembly site and the 14L SOIC (.150) will qualify by
similarity.**

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Purpose: _____ Qualification of 16L SOIC (.150) at GTK (GRTK) assembly site. The 14L SOIC (.150) will qualify by similarity.

Mask: _____ VQAA27D7XA00

Part No.: _____ RE46C119

CCB#: _____ 958

Package:

Type _____ 16L SOIC .150"

Die thickness: _____ 15 mils

Die size: _____ 81.1 x 87.4 mils

Lead frame:

Paddle size: _____ 95x110 mils

Material _____ C194 /Fu Sheng (Taiwan)

Surface _____ Bare Cu

Process _____ Stamped

Lead Lock _____ No

Part Number _____ 11-0216N-004

Wire:

Material _____ Au / Sumitomo (Japan)

Die Attach Epoxy:

Part Number _____ CRM 1076DJ-G / Sumitomo (Japan)

Conductive _____ Yes

Mold Compound: _____ G600F / Sumitomo (Taiwan)

Package Reliability Tests

Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Quantity of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
Standard Pb-free Solderability	JESD22B-102E; Perform 8 hour steam aging for Matte tin finish and 1 hr steam aging for NiPdAu finish prior to testing.	22	5	1	27	> 95% lead coverage	5	
Backward Solderability	JESD22B-102E; Perform 8 hour steam aging for Matte tin finish and 1 hr steam aging for NiPdAu finish prior to testing. Backward: Matte tin/ NiPdAu finish, SnPb solder, wetting temp 215°C for SMD.	22	5	1	27	> 95% lead coverage	5	

Package Reliability Tests									
Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Quantity of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions	
Wire Bond Pull - WBP	Mil. Std. 883-2011	5	0	1	5	0 fails after TC	5	30 bonds from a min. 5 devices.	
Wire Bond Shear - WBS	CDF-AEC-Q100-001	5	0	1	5		5	30 bonds from a min. 5 devices.	
Bond Line Thickness (BLT) robustness assessment						>0.5 mils			
Wire Sweep								Required for any reduction in wire bond thickness.	
Physical Dimensions	Measure per JESD22 B100 and B108	10	0	3	30	0	5		
External Visual	Mil. Std. 883-2009/2010	ALL	0	3	ALL	0	5		

Package Reliability Tests

Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Quantity of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
HTSL (High Temp Storage Life)	+175°C for 504 hours or 150°C for 1008 hrs. Electrical test pre and post stress at +25C	45	5	3	150	0	10	
Preconditioning - * Required for surface mount devices	+150°C Bake for 24 hours, moisture loading requirements per MSL level + 3X reflow at peak reflow temperature per Jedec-STD-020C for package type; Electrical test pre and post stress at +25°C. Perform SAM analysis using the standard sample size. MSL1 @ 260°C	231	15	3	738	0	15	Spares should be properly identified. 77 parts from each lot to be used for HAST, Autoclave, Temp Cycle test.

Package Reliability Tests									
Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Quantity of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions	
HAST *	+130° C/85% RH for 96 hours. Electrical test pre and post stress at +25	77	5	3	246	0	10	Spares should be properly identified. Use the parts which have gone through Pre-conditioning.	
Autoclave *	+121° C/15 psig for 96 hours. Electrical test pre and post stress at +25° C	77	5	3	246	0	10	Spares should be properly identified. Use the parts which have gone through Pre-conditioning.	
Temp Cycle*	-65° C to +150° C for 500 cycles. Electrical test pre and post stress at hot temp; 3 gram force WBP, on 5 devices from 1 lot, test following Temp Cycle stress.	77	5	3	246	0	15	Spares should be properly identified. Use the parts which have gone through Pre-conditioning. For hot temp testing, pre/post test 1 lot at 85° C.	