HV20220

Low-Charge Injection 8-Channel High-Voltage Analog Switch

Features

- Very Low Quiescent Power Dissipation, typically 10 µA
- Output On-resistance, typically 22Ω
- Low Parasitic Capacitances
- DC to 50 MHz Small Signal Frequency Response
- –60 dB Typical Output Off Isolation at 5.0 MHz
- CMOS Logic Circuitry for Low Power
- Excellent Noise Immunity
- On-chip Shift Register, Latch and Clear Logic Circuitry
- Flexible High Voltage Supplies

Applications

- Medical Ultrasound Imaging
- Piezoelectric Transducer Drivers

General Description

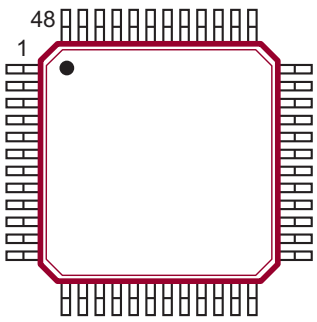
The HV20220 is a low-charge injection 8-channel high-voltage analog switch integrated circuit (IC) for applications requiring high-voltage switching controlled by low-voltage control signals, such as ultrasound imaging and printers.

Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. To reduce any possible clock feed-through noise, Latch Enable Bar ($\overline{LE}$) should be left high until all bits are clocked in. This switch combines high-voltage bilateral DMOS switches and low-power CMOS logic to provide efficient control of high-voltage analog signals.

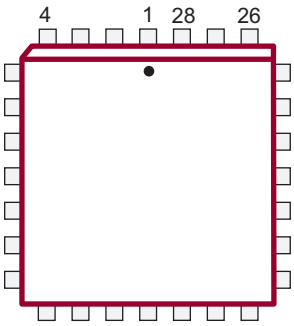
The IC is suitable for various combinations of high-voltage supplies, such as V_{PP}/V_{NN}: +50V/–150V or +100V/-100V.

Package Type

48-lead LQFP/TQFP

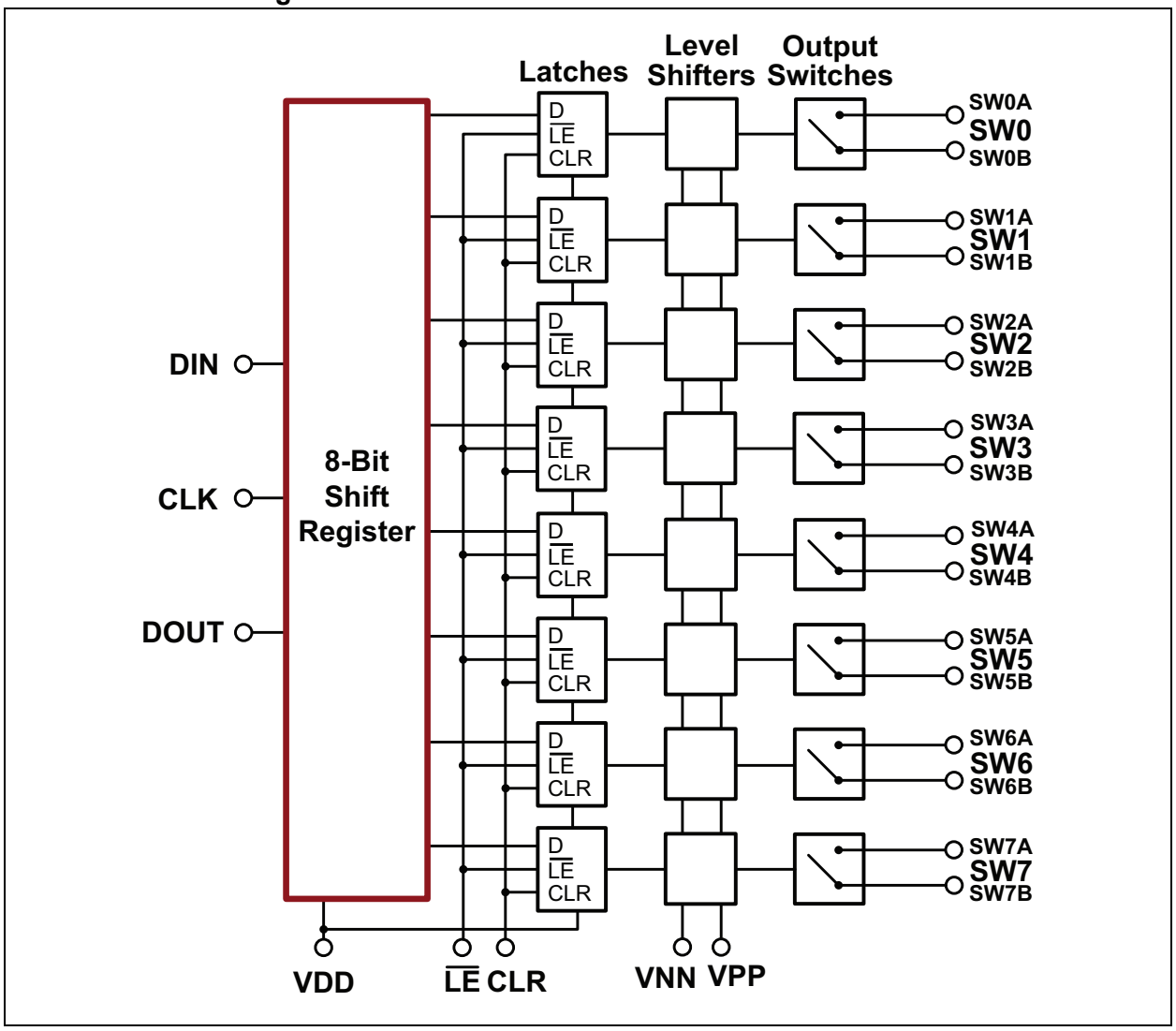


28-lead PLCC



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Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Logic Power Supply Voltage, V_{DD} ..... –0.5V to +15V
Differential Supply Voltage, V_{PP}–V_{NN} 220V
High-voltage Positive Supply, V_{PP} ..... –0.5V to V_{NN} +200V
High-voltage Negative Supply, V_{NN} ..... +0.5V to –200V
Logic Input Voltages ..... –0.5V to V_{DD} +0.3V
Analog Signal Range ..... V_{NN} to V_{PP}
Peak Analog Signal Current/Channel 3A
Storage Temperature ..... –65°C to 150°C
Power Dissipation
48-Lead LQFP 1W
48-Lead TQFP 1W
28-Lead PLCC 1.2W

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Logic Power Supply Voltage	V_{DD}	4.5	—	13.2	V	**Note 1**, **Note 3**
High-voltage Positive Supply	V_{PP}	40	—	V_{NN} +200	V	**Note 1**, **Note 3**
High-voltage Negative Supply	V_{NN}	–40	—	–160	V	**Note 1**, **Note 3**
High-level Input Voltage	V_{IH}	V_{DD} –1.5	—	V_{DD}	V	
Low-level Input Voltage	V_{IL}	0	—	1.5	V	
Analog Signal Voltage Peak-to-Peak	V_{SIG}	V_{NN} +10	—	V_{PP} -10	V	**Note 2**
Operating Ambient Temperature	T_A	0	—	70	°C	

Note 1: Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2: V_{SIG} must be $V_{NN} \le V_{SIG} \le {}_{VPP}$ or floating during power-up/down transition.
3: Rise and fall times of power supplies V_{DD}, V_{PP}, and V_{NN} should not be less than one millisecond.

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DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all values are over operating conditions.

Parameter	Sym.	0°C		+25°C			+70°C		Units	Conditions	
		Min.	Max	Min.	Typ.	Max	Min.	Max			
Small Signal Switch On-resistance	R_{ONS}	—	30	—	26	38	—	48	Ω	I_{SIG} = 5 mA	V_{PP} = +40V, V_{NN} = –160V
		—	25	—	22	27	—	32		I_{SIG} = 200 mA	
		—	25	—	22	27	—	30		I_{SIG} = 5 mA	V_{PP} = +100V, V_{NN} = –100V
		—	18	—	18	24	—	27		I_{SIG} = 200 mA	
		—	23	—	20	25	—	30		I_{SIG} = 5 mA	V_{PP} = +160V, V_{NN} = –40V
		—	22	—	16	25	—	27		I_{SIG} = 200 mA	
Small Signal Switch On-resistance Matching	ΔR_{ONS}	—	20	—	5	20	—	20	%	I_{SIG} = 5 mA, V_{PP} = +100V, V_{NN} = –100V	
Large Signal Switch On-resistance	R_{ONL}	—	—	—	15	—	—	—	Ω	V_{SIG} = V_{PP} – 10V, I_{SIG} = 1A	
Switch-Off Leakage per Switch	I_{SOL}	—	5	—	1	10	—	15	µA	V_{SIG} = V_{PP} – 10V, V_{NN}+10V	
DC Offset Switch-Off	V_{OS}	—	300	—	100	300	—	300	mV	R_L = 100 kΩ	
DC Offset Switch-On		—	500	—	100	500	—	500	mV	R_L = 100 kΩ	
V_{PP} Supply Quiescent Current	I_{PPQ}	—	—	—	10	50	—	—	µA	All switches off	
V_{NN} Supply Quiescent Current	I_{NNQ}	—	—	—	–10	–50	—	—	µA	All switches off	
V_{PP} Supply Quiescent Current	I_{PPQ}	—	—	—	10	50	—	—	µA	All switches on, I_{SW} = 5 mA	
V_{NN} Supply Quiescent Current	I_{NNQ}	—	—	—	–10	–50	—	—	µA	All switches on, I_{SW} = 5 mA	
Switch Output Peak Current	I_{SW}	—	3	—	3	2	—	2	A	V_{SIG} duty cycle < 0.1%	
Output Switching Frequency	f_{SW}	—	—	—	—	50	—	—	kHz	Duty cycle = 50%	
Average V_{PP} Supply Current	I_{PP}	—	6.5	—	—	7	—	8	mA	V_{PP} = +40V, V_{NN} = –160V	All output switches turn on and off at 50 kHz with no load.
		—	4	—	—	5	—	5.5		V_{PP} = +100V, V_{NN} = –100V	
		—	4	—	—	5	—	5.5		V_{PP} = +160V, V_{NN} = –40V	
Average V_{NN} Supply Current	I_{NN}	—	6.5	—	—	7	—	8	mA	V_{PP} = +40V, V_{NN} = –160V	All output switches turn on and off at 50 kHz with no load.
		—	4	—	—	5	—	5.5		V_{PP} = +100V, V_{NN} = –100V	
		—	4	—	—	5	—	5.5		V_{PP} = +160V, V_{NN} = –40V	
Logic Supply Average Current	I_{DD}	—	4	—	—	4	—	4	mA	f_{CLK} = 5 MHz, V_{DD} = 5V	
Logic Supply Quiescent Current	I_{DDQ}	—	10	—	—	10	—	10	µA		
Data Out Source Current	I_{SOR}	0.45	—	0.45	0.7	—	0.4	—	mA	V_{OUT} = V_{DD} – 0.7V	
Data Out Sink Current	I_{SINK}	0.45	—	0.45	0.7	—	0.4	—	mA	V_{OUT} = 0.7V	
Logic Input Capacitance	C_{IN}	—	10	—	—	10	—	10	pF		

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AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all values are over operating conditions.

Parameter	Sym.	0°C		+25°C			+70°C		Units	Conditions
		Min.	Max	Min.	Typ.	Max	Min.	Max		
Set-up Time before $\overline{LE}$ Rises	t_{SD}	150	—	150	—	—	150	—	ns	
Time width of $\overline{LE}$	t_{WLE}	150	—	150	—	—	150	—	ns	
Clock Delay Time to Data Out	t_{DO}	—	150	—	—	150	—	150	ns	
Time Width of CLR	t_{WCL}	150	—	150	—	—	150	—	ns	
Set-up Time Data to Clock	t_{SU}	15	—	15	8	—	20	—	ns	
Hold Time Data from Clock	t_H	35	—	35	—	—	35	—	ns	
Clock Frequency	f_{CLK}	—	5	—	—	5	—	5	MHz	50% duty cycle, $f_{DATA} = f_{CLK}/2$
Clock Rise and Fall Times	t_R, t_F	—	50	—	—	50	—	50	ns	
Turn-on Time	t_{ON}	—	5	—	—	5	—	5	µs	$V_{SIG} = V_{PP} – 10V$, $R_{LOAD} = 10 kΩ$
Turn-off Time	t_{OFF}	—	5	—	—	5	—	5	µs	$V_{SIG} = V_{PP} – 10V$, $R_{LOAD} = 10 kΩ$
Maximum V_{SIG} Slew Rate	dv/dt	—	20	—	—	20	—	20	V/ns	$V_{PP} = +160V$, $V_{NN} = –40V$
		—	20	—	—	20	—	20		$V_{PP} = +100V$, $V_{NN} = –100V$
		—	20	—	—	20	—	20		$V_{PP} = +40V$, $V_{NN} = –160V$
Off Isolation	K_O	–30	—	–30	–33	—	–30	—	dB	f = 5 MHz,1 kΩ/15 pF load
		–58	—	–58	—	—	–58	—		f = 5 MHz, 50Ω load
Switch Crosstalk	K_{CR}	–60	—	–60	–70	—	–60	—	dB	f = 5 MHz, 50Ω load
Output Switch Isolation Diode Current	I_{ID}	—	300	—	—	300	—	300	mA	300 ns pulse width, 2% duty cycle
Off Capacitance SW to GND	$C_{SG(OFF)}$	5	17	5	12	17	5	17	pF	0V, f = 1 MHz
On Capacitance SW to GND	$C_{SG(ON)}$	25	50	25	38	50	25	50	pF	0V, f = 1 MHz
Output Voltage Spike	$+V_{SPK}$	—	—	—	—	150	—	—	mV	$V_{PP} = +40V$, $V_{NN} = –160V$, $R_{LOAD} = 50Ω$
	$–V_{SPK}$	—	—	—	—	150	—	—		
	$+V_{SPK}$	—	—	—	—	150	—	—		$V_{PP} = +100V$, $V_{NN} = –100V$, $R_{LOAD} = 50Ω$
	$–V_{SPK}$	—	—	—	—	150	—	—		
	$+V_{SPK}$	—	—	—	—	150	—	—		$V_{PP} = +160V$, $V_{NN} = –40V$, $R_{LOAD} = 50Ω$
	$–V_{SPK}$	—	—	—	—	150	—	—		
Charge Injection	QC	—	—	—	820	—	—	—	pC	$V_{PP} = +40V$, $V_{NN} = –160V$, $V_{SIG} = 0V$
		—	—	—	600	—	—	—		$V_{PP} = +100V$, $V_{NN} = –100V$, $V_{SIG} = 0V$
		—	—	—	350	—	—	—		$V_{PP} = +160V$, $V_{NN} = –40V$, $V_{SIG} = 0V$

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TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Ambient Temperature	T_A	0	—	70	°C	
Storage Temperature	T_S	–65	—	+150	°C	
Package Thermal Resistances						
48-lead LQFP	θ_{JA}	—	52	—	°C/W	
48-lead TQFP	θ_{JA}	—	42	—	°C/W	
28-lead PLCC	θ_{JA}	—	48	—	°C/W	

TRUTH FUNCTION TABLE

D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CLR	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	**Hold Previous State**							
X	X	X	X	X	X	X	X	X	H	**All Switches Off**							

Note 1: The eight switches operate independently.

2: Serial data is clocked in on the L to H transition of the CLK.

3: The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift register data flow through the latch.

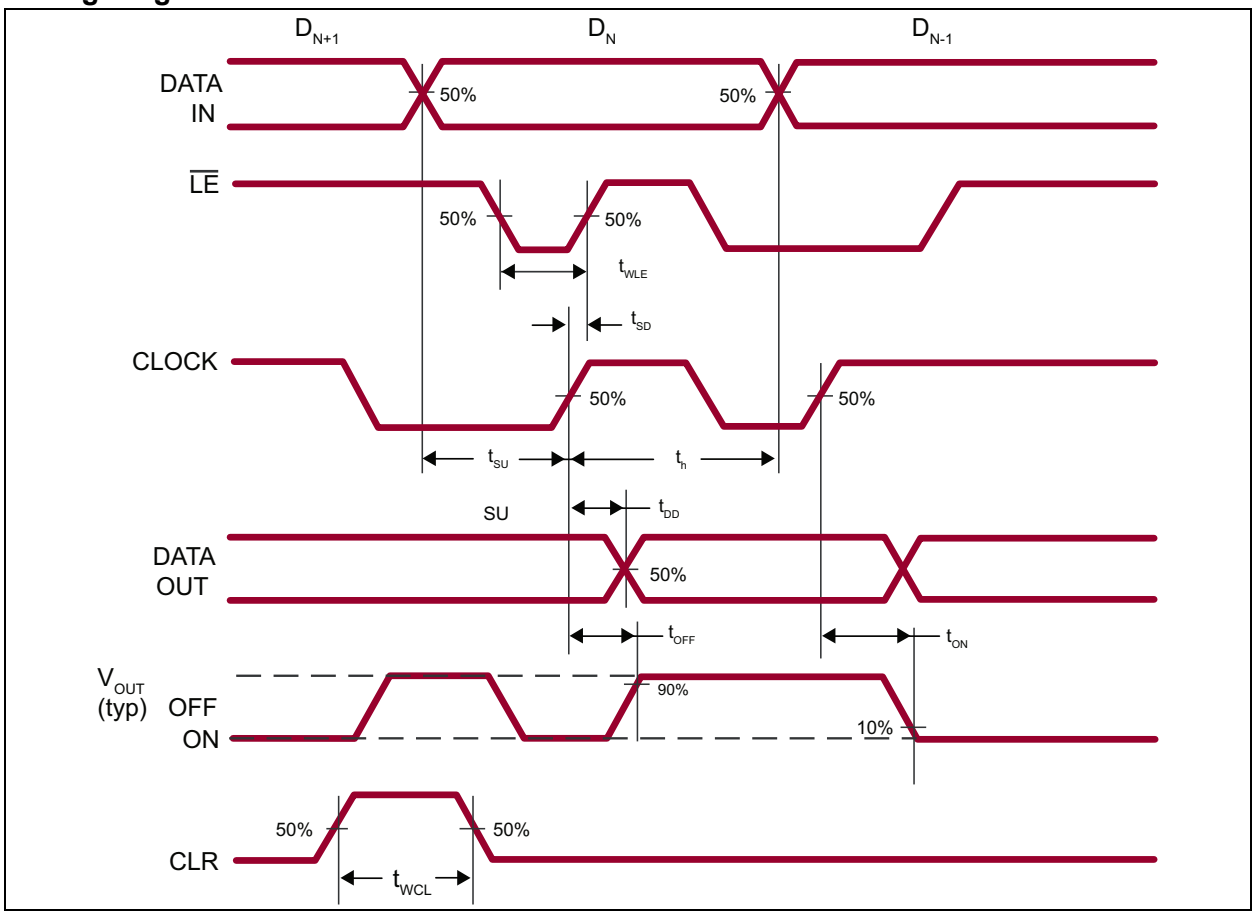
4: D_{OUT} is high when data in the Shift Register 7 is high.

5: Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.

6: The CLR clear input overrides all other inputs.

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Timing Diagram



2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

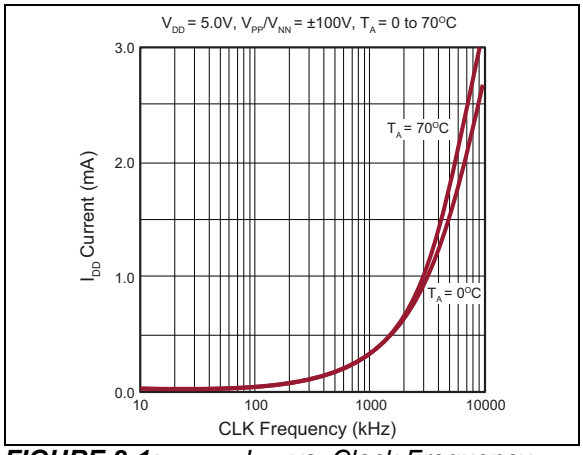


FIGURE 2-1: *I_{DD} vs. Clock Frequency.*

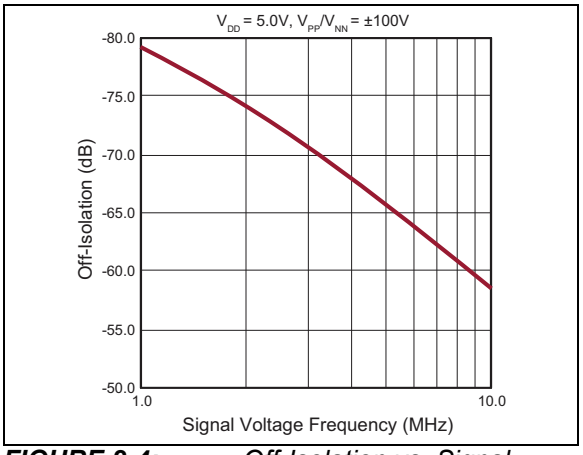


FIGURE 2-4: *Off-Isolation vs. Signal Voltage Frequency.*

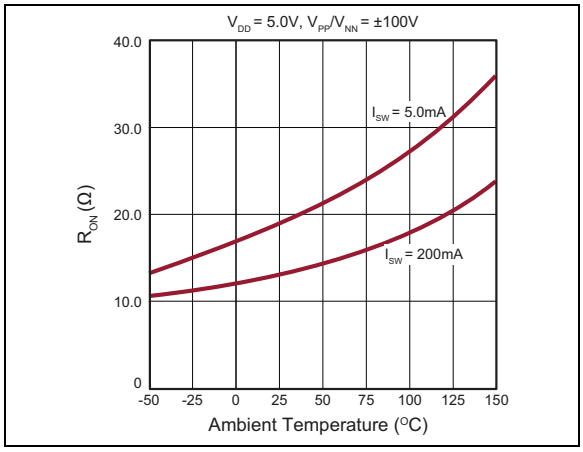


FIGURE 2-2: *R_{ON} vs. Ambient Temperature (T_A).*

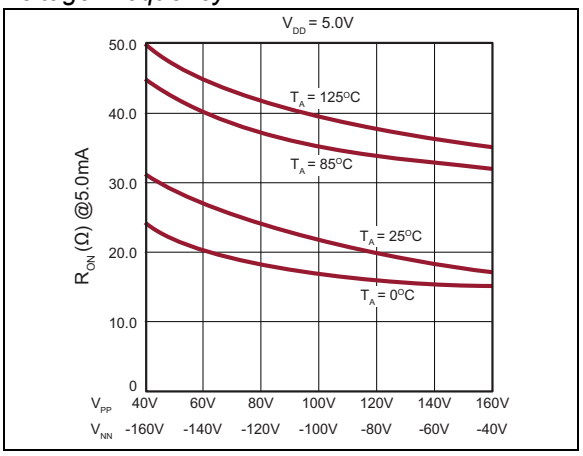


FIGURE 2-5: *R_{ON} vs. V_{PP}/V_{NN}.*

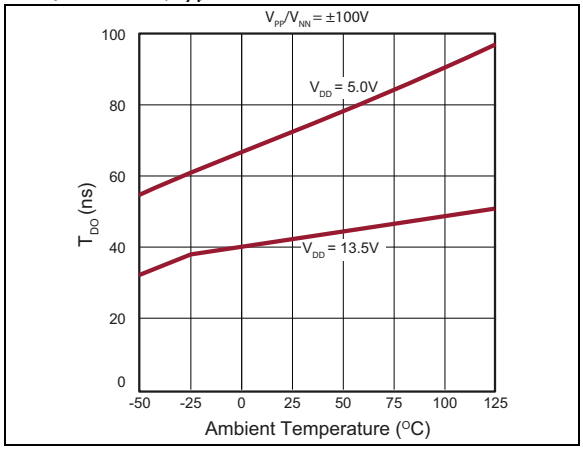


FIGURE 2-3: *T_{DO} vs. Ambient Temperature (T_A).*

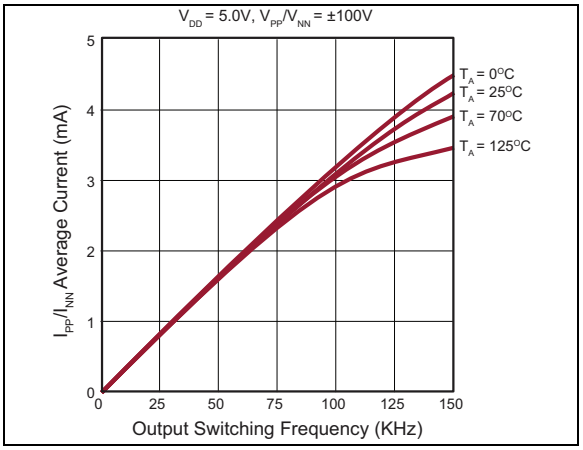


FIGURE 2-6: *I_{PP}/I_{NN} vs. Output Switching Frequency.*

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3.0 PIN DESCRIPTION

The HV20220 pins are listed in Table 3-1. Refer to **Package Type** for the location of pins.

TABLE 3-1: 48-LEAD LQFP/TQFP PIN TABLE

Pin Number	Pin Name	Description
1	SW5B	Terminal B of analog switch 5
2	NC	No connection
3	SW4A	Terminal A of analog switch 4
4	NC	No connection
5	SW4B	Terminal B of analog switch 4
6	NC	No connection
7	NC	No connection
8	SW3A	Terminal A analog switch 3
9	NC	No connection
10	SW3B	Terminal B of analog switch 3
11	NC	No connection
12	SW2A	Terminal A of analog switch 2
13	NC	No connection
14	SW2B	Terminal B of analog switch 2
15	NC	No connection
16	SW1A	Terminal A of analog switch 1
17	NC	No connection
18	SW1B	Terminal B of analog switch 1
19	NC	No connection
20	SW0A	Terminal A of analog switch 0
21	NC	No connection
22	SW0B	Terminal B of analog switch 0
23	NC	No connection
24	VPP	High-voltage positive supply
25	VNN	High-voltage negative supply
26	NC	No connection
27	NC	No connection
28	GND	Ground
29	VDD	Logic supply voltage
30	NC	No connection
31	NC	No connection
32	NC	No connection
33	DIN	Data in logic input
34	CLK	Clock logic input for shift registers
35	$\overline{LE}$	Latch enable logic input, low active
36	CLR	Latch clear logic input
37	DOUT	Data out logic output
38	NC	No connection
39	SW7A	Terminal A of analog switch 7
40	NC	No connection
41	SW7B	Terminal B of analog switch 7

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TABLE 3-1: 48-LEAD LQFP/TQFP PIN TABLE (CONTINUED)

Pin Number	Pin Name	Description
42	NC	No connection
43	SW6A	Terminal A of analog switch 6
44	NC	No connection
45	SW6B	Terminal B of analog switch 6
46	NC	No connection
47	SW5A	Terminal A of analog switch 5
48	NC	No connection

TABLE 3-2: 28-LEAD PLCC PIN TABLE

Pin Number	Pin Name	Description
1	SW3A	Terminal A of analog switch 3
2	SW3B	Terminal B of analog switch 3
3	SW2A	Terminal A of analog switch 2
4	SW2B	Terminal B of analog switch 2
5	SW1A	Terminal A of analog switch 1
6	SW1B	Terminal B of analog switch 1
7	SW0A	Terminal A of analog switch 0
8	SW0B	Terminal B of analog switch 0
9	VPP	High-voltage positive supply
10	VNN	High-voltage negative supply
11	NC	No connection
12	GND	Ground
13	VDD	Logic supply voltage
14	NC	No connection
15	NC	No connection
16	DIN	Data in logic input
17	CLK	Clock logic input for shift registers
18	$\overline{LE}$	Latch enable logic input, low active
19	CLR	Latch clear logic input
20	DOUT	Data out logic output
21	SW7A	Terminal A of analog switch 7
22	SW7B	Terminal B of analog switch 7
23	SW6A	Terminal A of analog switch 6
24	SW6B	Terminal B of analog switch 6
25	SW5A	Terminal A of analog switch 5
26	SW5B	Terminal B of analog switch 5
27	SW4A	Terminal A of analog switch 4
28	SW4B	Terminal B of analog switch 4

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4.0 FUNCTIONAL DESCRIPTION

Below are the test circuits for the HV20220.

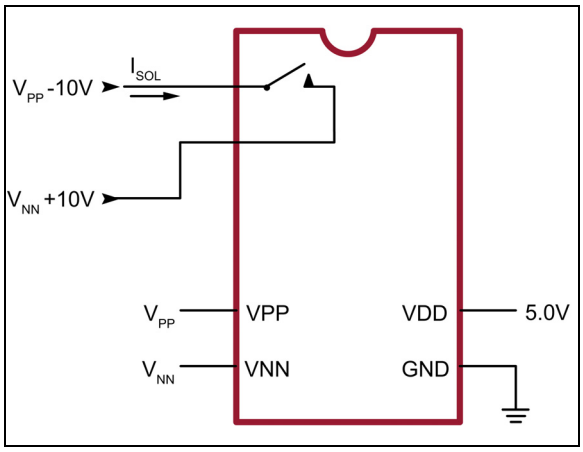


FIGURE 4-1: *Switch-off Leakage.*

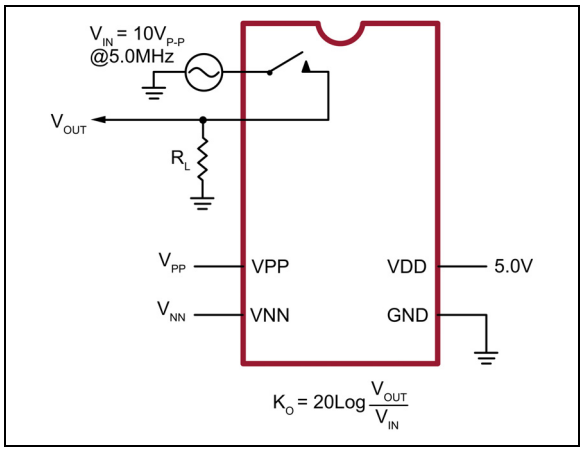


FIGURE 4-4: *OFF Isolation.*

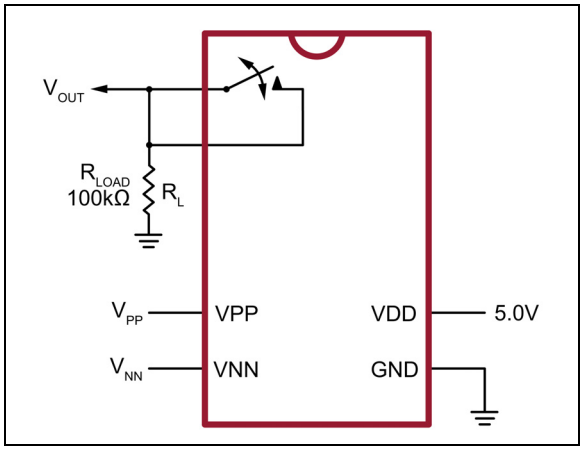


FIGURE 4-2: *DC Offset ON/OFF.*

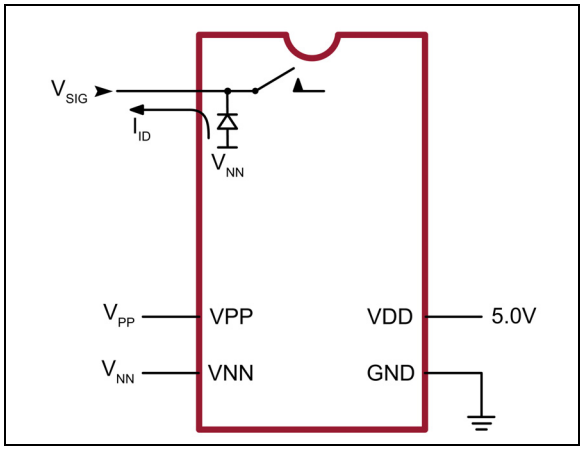


FIGURE 4-5: *Isolation Diode Current.*

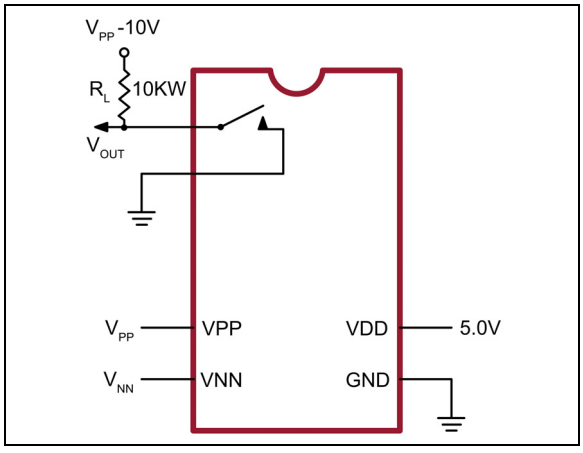


FIGURE 4-3: *T_{ON}/T_{OFF} Test Circuit.*

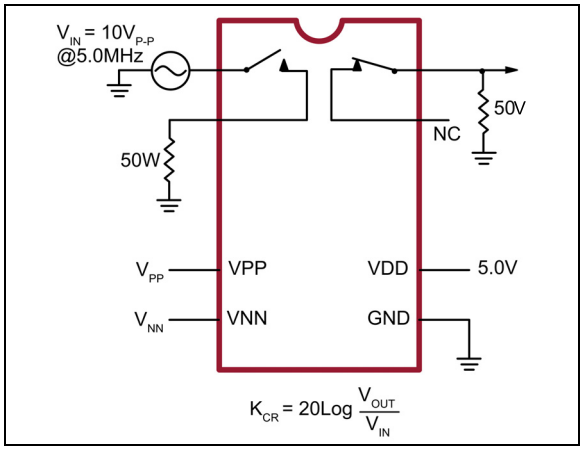


FIGURE 4-6: *Crosstalk.*

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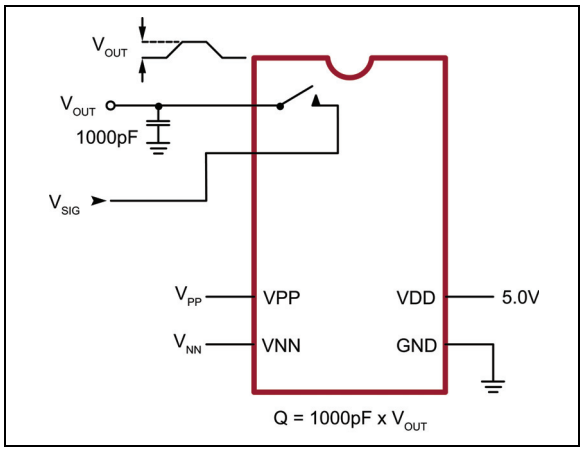


FIGURE 4-7: *Charge Injection.*

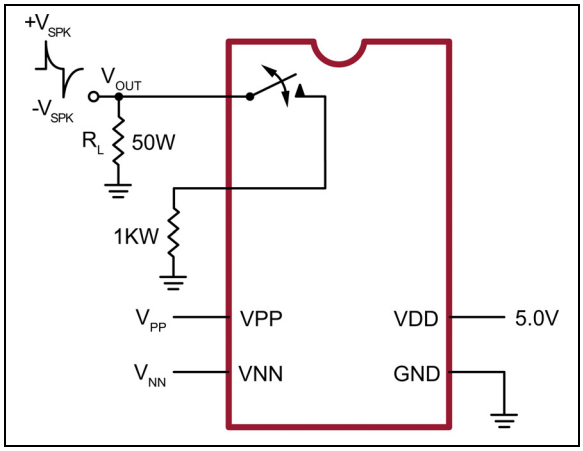


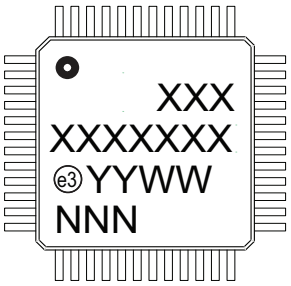
FIGURE 4-8: *Output Voltage Spike.*

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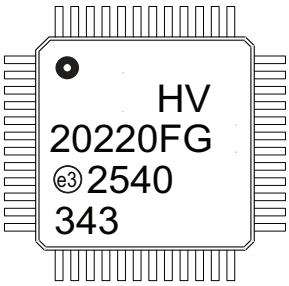
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

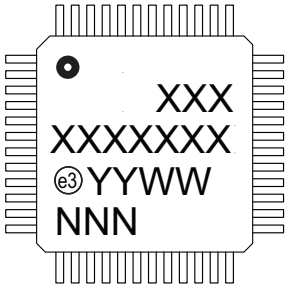
48-lead LQFP



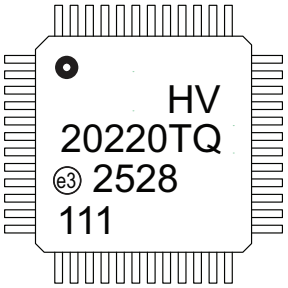
Example



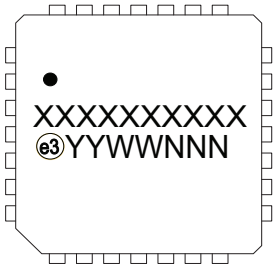
48-lead TQFP



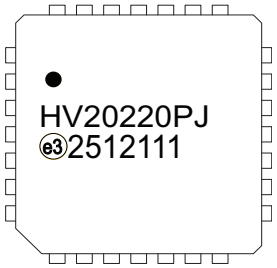
Example



28-lead PLCC (PJ)



Example



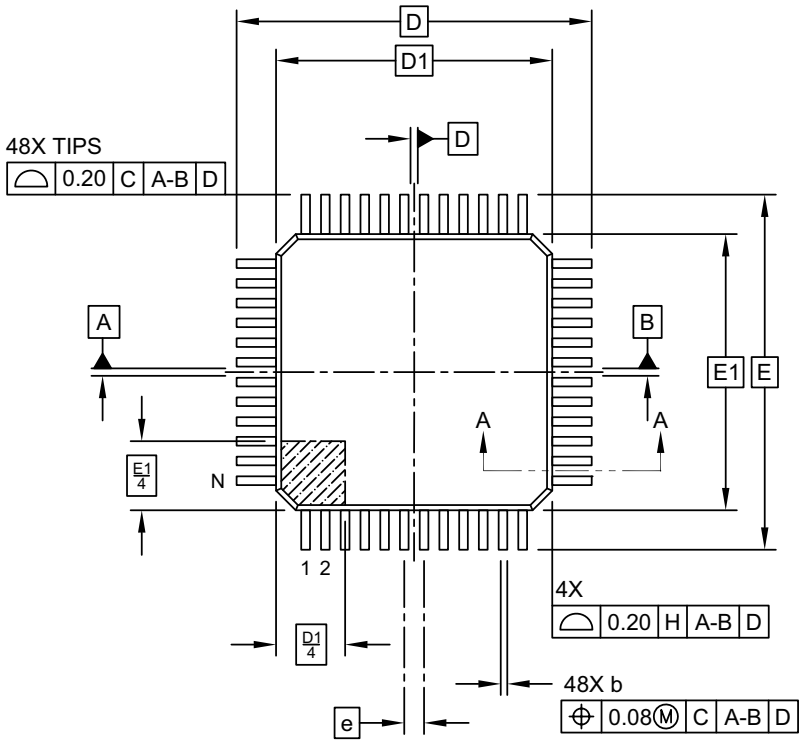
Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

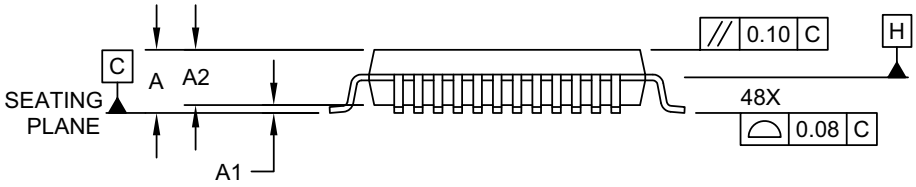
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48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP]
Supertex Legacy Package

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



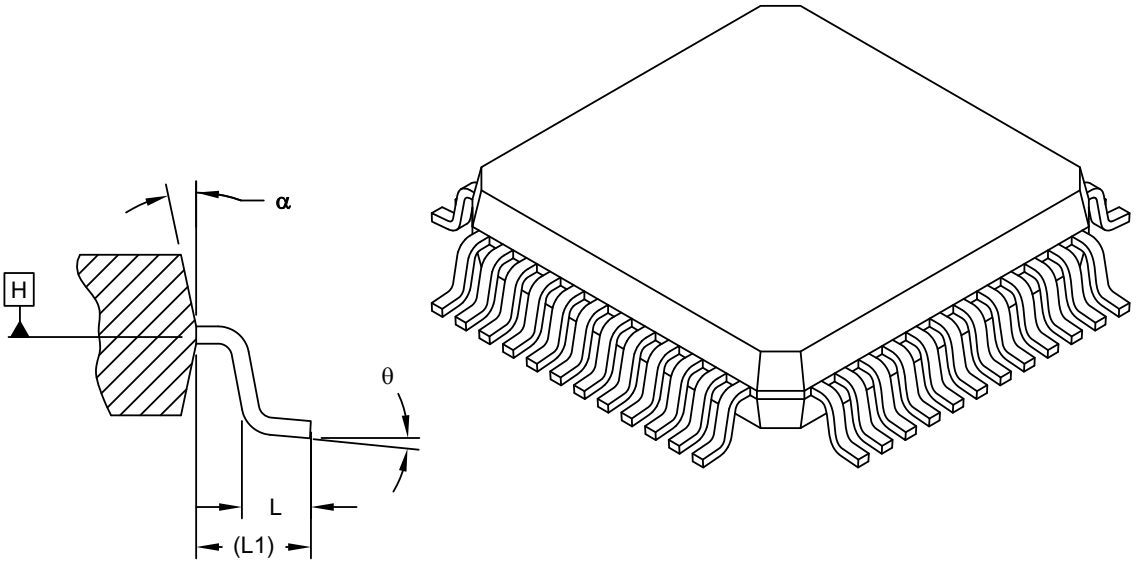
SIDE VIEW

Microchip Technology Drawing C04-278 Rev A Sheet 1 of 2

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48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		48	
Lead Pitch	e		0.50 BSC	
Overall Height	A	1.40	1.50	1.60
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	1.35	1.40	1.45
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	θ	0°	3.5°	7°
Overall Width	E		9.00 BSC	
Overall Length	D		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Molded Package Length	D1		7.00 BSC	
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

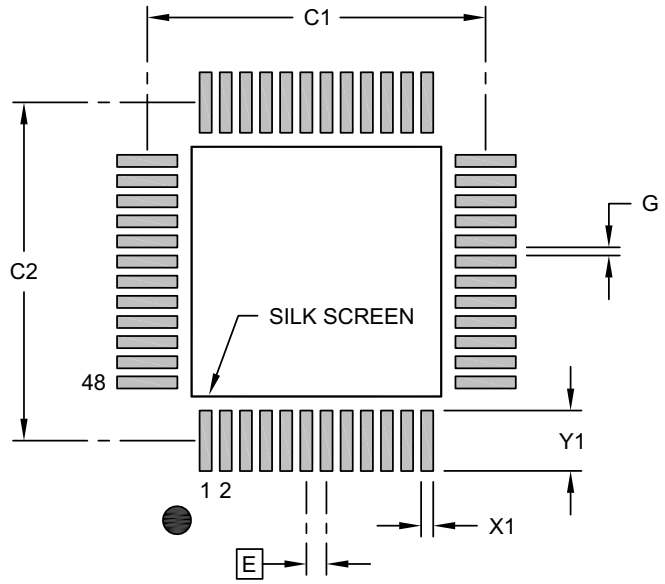
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-278 Rev A Sheet 2 of 2

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48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.50
Contact Pad to Contact Pad (X44)	G	0.20		

Notes:

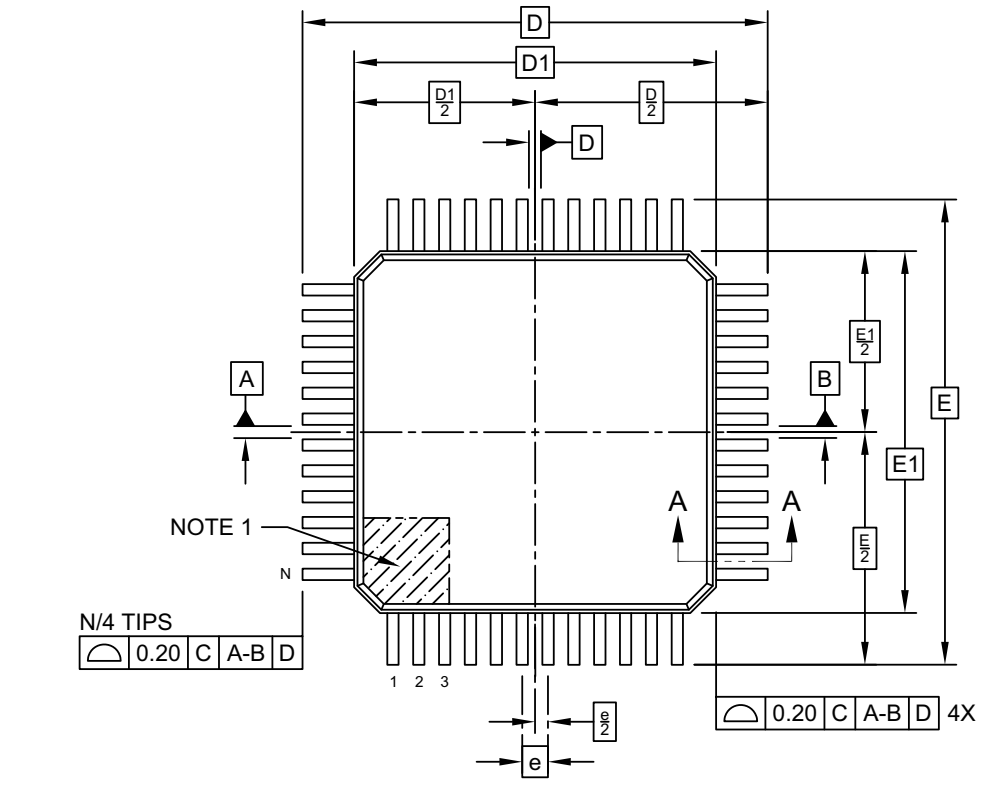
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2278 Rev A

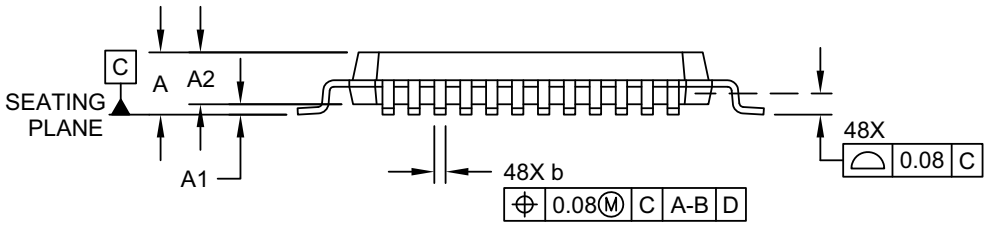
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48-Lead Plastic Thin Quad Flatpack (Y8X) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

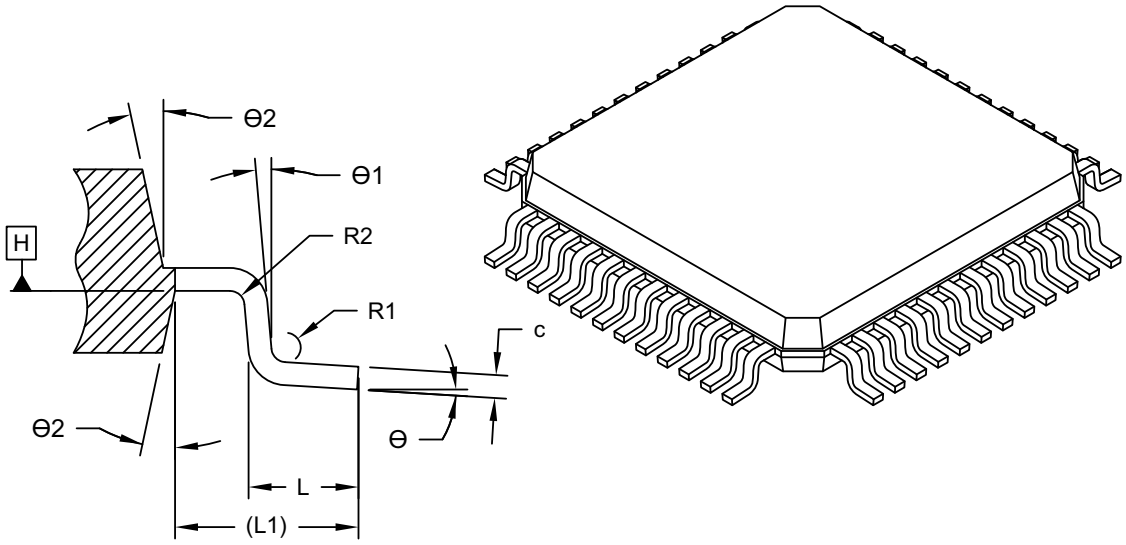


SIDE VIEW

Microchip Technology Drawing C04-300-Y8X Rev D Sheet 1 of 2

48-Lead Plastic Thin Quad Flatpack (Y8X) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D		9.00 BSC	
Molded Package Length	D1		7.00 BSC	
Overall Width	E		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Terminal Width	b	0.17	0.22	0.27
Terminal Thickness	c	0.09	-	0.16
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Bend Radius	R1	0.08	-	-
Lead Bend Radius	R2	0.08	-	0.20
Foot Angle	Θ	0°	3.5°	7°
Lead Angle	Θ1	0°	-	-
Mold Draft Angle	Θ2	11°	12°	13°

Notes:

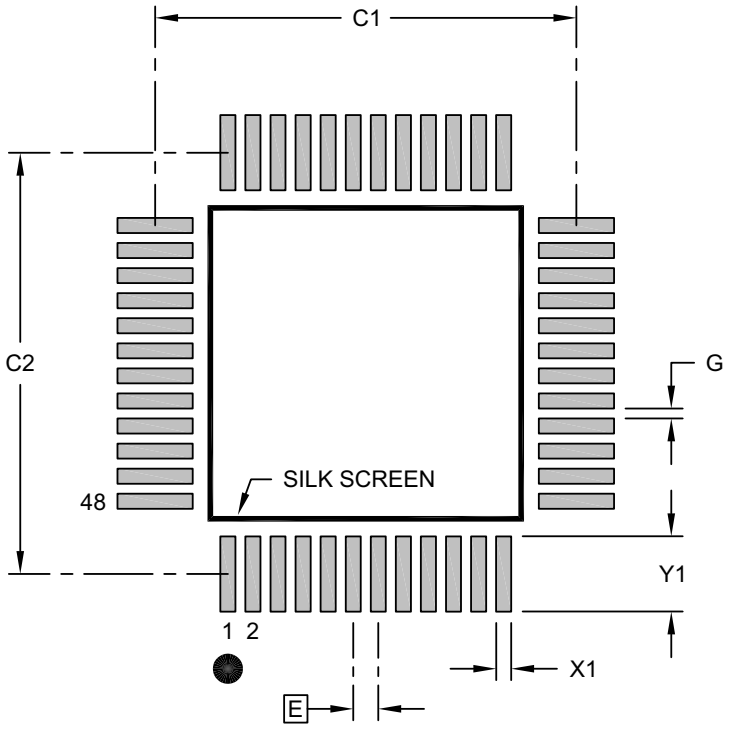
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-300-Y8X Rev D Sheet 2 of 2

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48-Lead Plastic Thin Quad Flatpack (Y8X) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

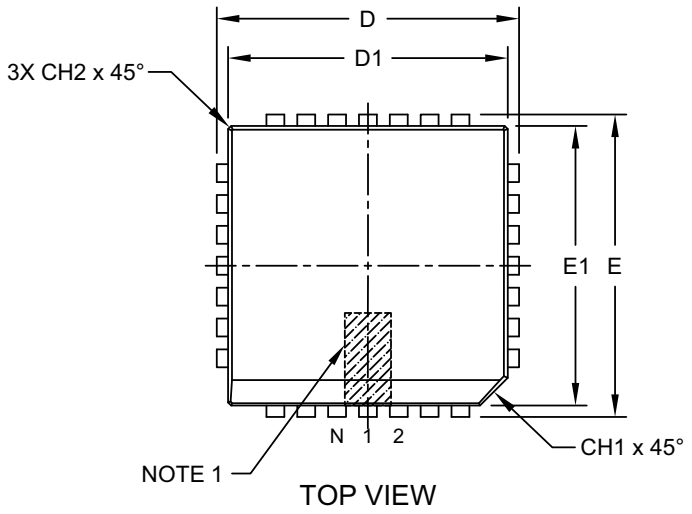
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2300-Y8X Rev D

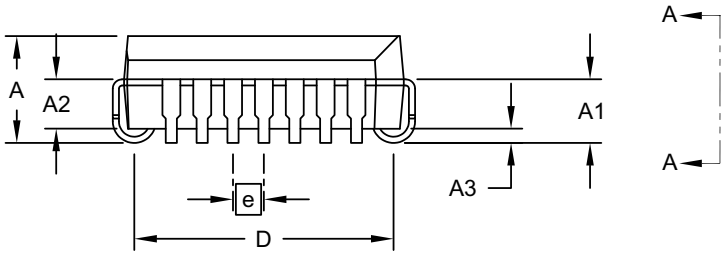
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28-Lead Plastic Leaded Chip Carrier (L4X) - Square [PLCC]

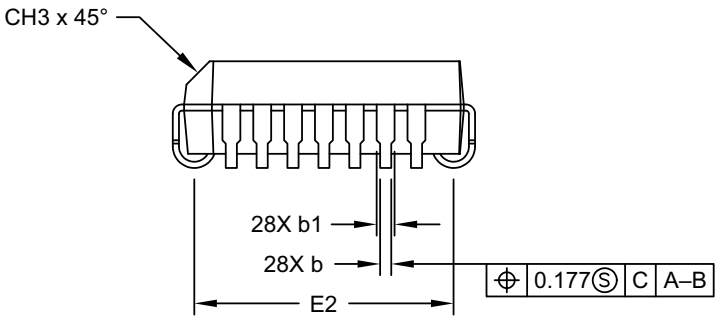
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



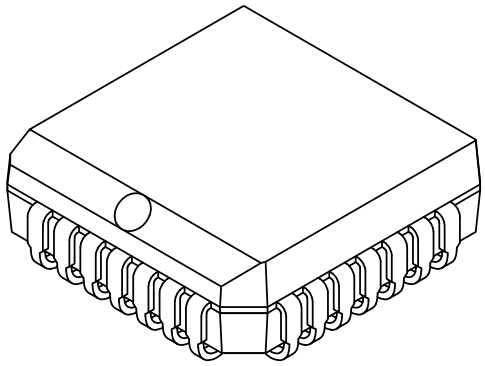
VIEW A-A

Microchip Technology Drawing C04-026-L4X Rev D Sheet 1 of 2

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28-Lead Plastic Leaded Chip Carrier (L4X) - Square [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	N		28			28	
Pitch	e		.050			1.27	
Overall Height	A	.165	.172	.180	4.19	4.37	4.57
Contact Height	A1	.090	.105	.120	2.29	2.67	3.05
Molded Package to Contact	A2	.062	-	.083	1.57	-	2.11
Standoff §	A3	.020	-	-	0.51	-	-
Corner Chamfer	CH1	.042	-	.048	1.07	-	1.22
Chamfers	CH2	-	-	.020	-	-	0.51
Side Chamfer	CH3	.042	-	.056	1.07	-	1.42
Overall Width	E	.485	.490	.495	12.32	12.45	12.57
Overall Length	D	.485	.490	.495	12.32	12.45	12.57
Molded Package Width	E1	.450	.453	.456	11.43	11.51	11.58
Molded Package Length	D1	.450	.453	.456	11.43	11.51	11.58
Footprint Width	E2	.382	.410	.438	9.70	10.41	11.13
Footprint Length	D2	.382	.410	.438	9.70	10.41	11.13
Lead Thickness	c	.0075	-	.0125	0.19	-	0.32
Upper Lead Width	b1	.025	-	.032	0.64	-	0.81
Lower Lead Width	b	.013	-	.021	0.33	-	0.53

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

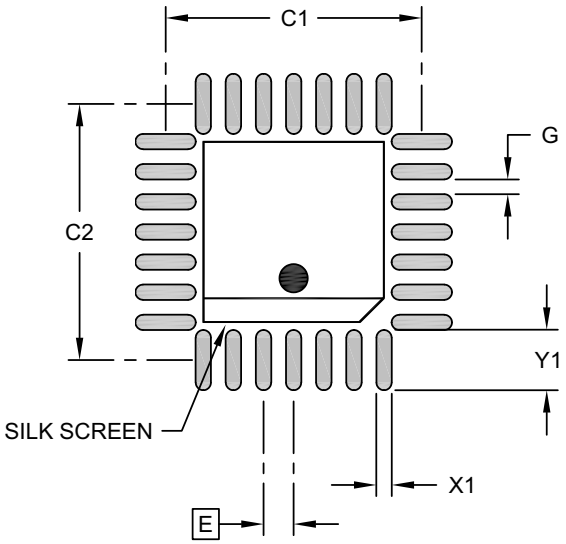
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-026-L4X Rev D Sheet 2 of 2

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28-Lead Plastic Leaded Chip Carrier (L4X) - Square [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		INCHES			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Contact Pitch	E	.050 BSC			1.27 BSC		
Contact Pad Spacing	C1		.425			10.80	
Contact Pad Spacing	C2		.425			10.80	
Contact Pad Width (X28)	X1			.026			0.66
Contact Pad Length (X28)	Y1			.100			2.54
Contact Pad to Center Pad (X24)	G	.008			0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2026-L4X Rev D

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NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (September 2025)

- Converted Supertex Doc #s DSFP-HV20220 to Microchip DS20005545A
- Changed the packaging quantity of the PJ M904 media type from 500/Reel to 750/Reel to align packaging specifications with the actual BQM
- Updated package outline drawings
- Made minor changes throughout the document

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV20220	=	Low-Charge Injection 8-Channel High-Voltage Analog Switch
Package:	FG	=	48-lead LQFP
	TQ	=	48-lead TQFP
	PJ	=	28-lead PLCC
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	250/Tray for an FG Package
	(blank)	=	250/Tray for a TQ Package
	(blank)	=	38/Tube for a PJ Package
	M931	=	1000/Reel for an FG package
	M931	=	1600/Reel for an TQ package
	M904	=	750/Reel for a PJ package

Example(s):

a)	HV20220FG-G:	Low-Charge Injection 8-Channel High-Voltage Analog Switch, 48-lead LQFP Package, 250/Tray
b)	HV20220FG-G-M931:	Low-Charge Injection 8-Channel High-Voltage Analog Switch, 48-lead LQFP Package,1000/Reel
c)	HV20220TQ-G:	Low-Charge Injection,8-Channel High-Voltage Analog Switch, 48-lead TQFP Package, 250/Tray
d)	HV20220TQ-G-M931:	Low-Charge Injection,8-Channel High-Voltage Analog Switch, 48-lead TQFP Package, 1600/Reel
e)	HV20220PJ-G:	Low-Charge Injection,8-Channel High-Voltage Analog Switch, 28-lead PLCC Package, 38/Tube
f)	HV20220PJ-G-M904:	Low-Charge Injection,8-Channel High-Voltage Analog Switch, 28-lead PLCC Package, 750/Reel

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