June 2012

## Features

- Frequency, Phase and Time Synchronization over IP, MPLS and Ethernet Packet Networks
  - Frequency accuracy performance for WCDMA-FDD, GSM, LTE-FDD and femtocell applications, with target performance less than ± 15 ppb.
  - Frequency performance for ITU-T G.823 and G.824 synchronization interface, as well as G.8261 PNT EEC, PNT PEC and CES interface specifications.
  - Phase Synchronization performance for WCDMA-TDD, Mobile WiMAX, TD-SCDMA and CDMA2000 applications with target performance less than ± 1 μs phase alignment.
  - Time Synchronization for UTC-traceability and GPS replacement.
- Meets the SONET/SDH jitter generation requirements up to OC-48/STM-16

**Ordering Information**

| | | |
|---|---|---|
| ZL30347GGG | 100 Pin CABGA | Trays |
| ZL30347GGG2 | 100 Pin CABGA* | Trays |

*Pb Free Tin/Silver/Copper

**-40°C to +85°C**

- Programmable output synthesizers (P0, P1) generate telecom clock frequencies from any multiple of 8 kHz up to 100 MHz
- Generates standard SONET/SDH clock rates (e.g., 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, 622.08 MHz) or Ethernet clock rates (e.g., 25 MHz, 50 MHz, 125 MHz, 156.25 MHz, 312.5 MHz) for synchronizing Gigabit Ethernet PHYs
- Client reference switching between multiple Servers
- Client holdover when Server packet connectivity is lost

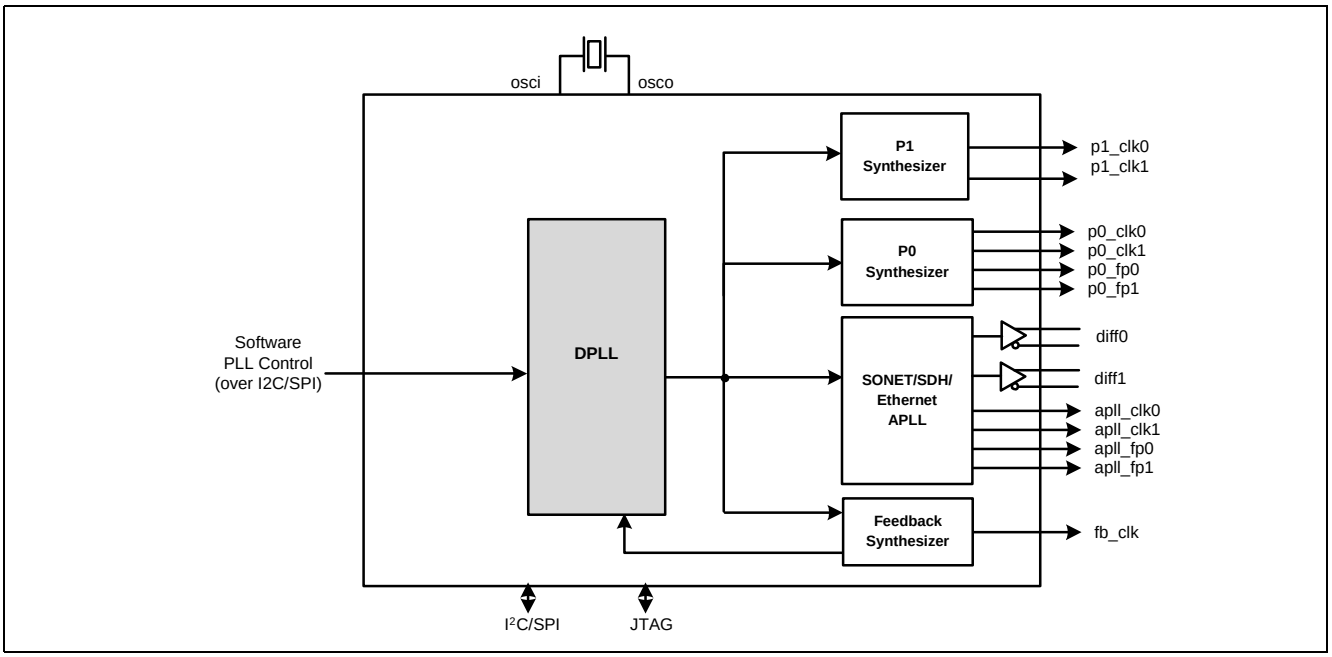



**Figure 1 - Functional Block Diagram**



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# 1.0 Features

## 1.1 Time Synchronization Algorithm

- External algorithm controls software digital PLL to adjust frequency & phase alignment
- Frequency, Phase and Time Synchronization over IP, MPLS and Ethernet Packet Networks
- Frequency accuracy performance for WCDMA-FDD, GSM, LTE-FDD and femtocell applications, with target performance less than ± 15 ppb.
- Frequency performance for ITU-T G.823 and G.824 synchronization interface, as well as G.8261 PNT EEC, PNT PEC and CES interface specifications.
- Phase Synchronization performance for WCDMA-TDD, Mobile WiMAX, TD-SCDMA and CDMA2000 applications with target performance less than ± 1 μs phase alignment.
- Time Synchronization for UTC-traceability and GPS replacement.
- Client reference switching between multiple Servers
- Client holdover when Server packet connectivity is lost

## 1.2 Electrical Clock Generation

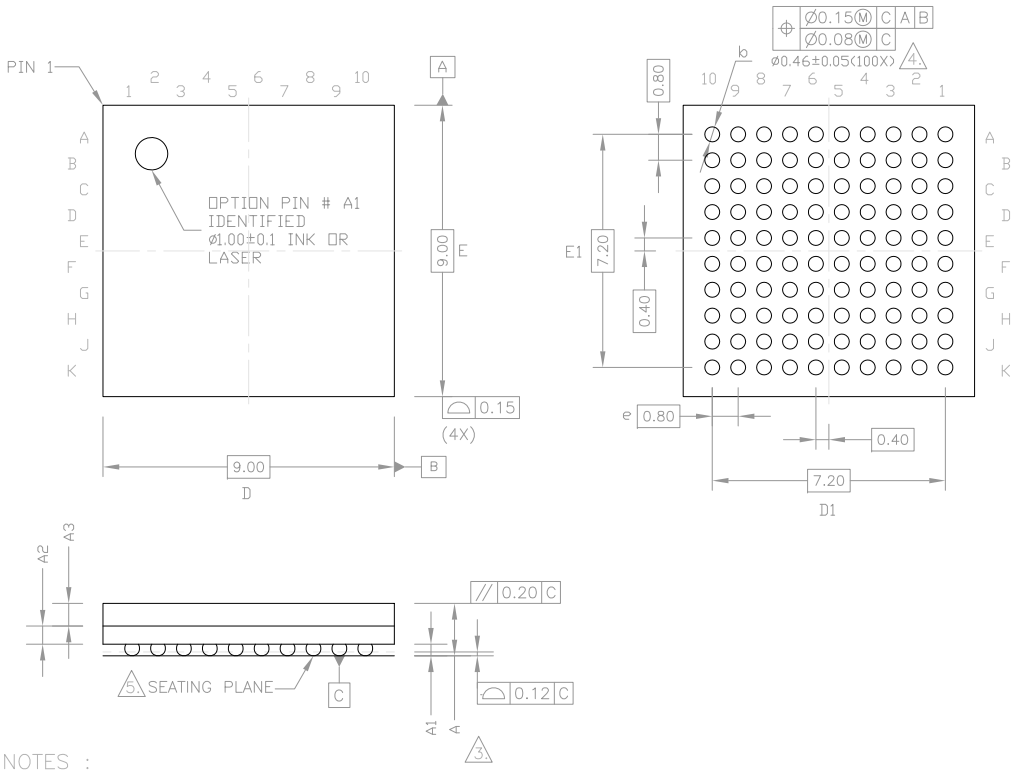
- Generates standard SONET/SDH clock rates (e.g., 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, 622.08 MHz) or Ethernet clock rates (e.g., 25 MHz, 50 MHz, 125 MHz, 156.25 MHz, 312.5 MHz) for synchronizing Gigabit Ethernet PHYs
- Programmable output synthesizers (P0, P1) generate telecom clock frequencies from any multiple of 8 kHz up to 100 MHz
- Generates several styles of telecom frame pulses with selectable pulse width, polarity and frequency
- Configurable input to output delay and output to output phase alignment

## 1.3 API Software

- Interfaces to 1588-capable PHY and switches with integrated timestamping
- Abstraction layer for independence from OS and CPU, from embedded SoC to home-grown
- Fits into centralized, highly integrated pizza box architectures as well as distributed architectures with multiple line cards and timing cards

# 2.0 Applications

- Integrated basestation reference clock for air interface for GSM, WCDMA, LTE and WiMAX macro, micro or femtocells
- Mobile Backhaul NID, edge router or access aggregation node
- EPON/GE-PON & GPON OLT
- EPON/GE-PON & GPON ONU/OLT
- DSLAM and RT-DSLAM




| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.52 | 1.62 | 1.72 | .059 | .064 | .069 |
| A1 | 0.31 | 0.36 | 0.41 | .012 | .014 | .016 |
| A2 | 0.51 | 0.56 | 0.61 | .020 | .022 | .024 |
| A3 | 0.65 | 0.70 | 0.75 | .026 | .028 | .029 |
| b | 0.41 | 0.46 | 0.51 | .016 | .018 | .020 |
| D | 8.90 | 9.00 | 9.10 | .350 | .354 | .358 |
| D1 | 7.20 BSC | | | .283 BSC | | |
| E | 8.90 | 9.00 | 9.10 | .350 | .354 | .358 |
| E1 | 7.20 BSC | | | .283 BSC | | |
| e | 0.8 BSC | | | .020 BSC | | |

NOTES :

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. SOLDER BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
3. THIS DIMENSION INCLUDES STAND–OFF HEIGHT, PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES, E.G., EXTERNAL HEATSINK OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AN ATTACHED FEATURE.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

| Microsemi CMPG | DWG. NO. | REV. |
|---|---|---|
| TITLE | CDCA# 22–0055 84–06–128–304 | 2 |
| 100L LFBGA PACKAGE OUTLINE BODY SIZE :9 X 9 X1.62MM MAX PITCH 1.0MM | SHEET | SIZE |
| | 1 OF 1 | A4 |



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Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.

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