March 2015

Features

- Synchronizes to any Telecom (N * 8 kHz) or any Synchronized Ethernet (SyncE) frequency.
- Generates any Telecom or SyncE frequency independent of the input frequency rate
- Uses proprietary DPLL technology to guarantee a stable synchronization path over any combination of input and output ratios and frequencies
- Provides input reference jitter filtering with programmable loop bandwidth in the range of 14 Hz to 896 Hz
- Supports two input references, each configurable as single ended LVCMOS (up to 177.5 MHz) or differential LVPECL (up to 750 MHz)
- Automatic hitless reference switching and stand-by mode on reference fail
- Digital PLL (DPLL) and high speed clock synthesis engine for generating high speed PHY clocks
- Provides four high performance differential LVPECL outputs with maximum speed up to 750 MHz with jitter below 0.7 psec RMS
- Provides 2 high performance single ended LVCMOS outputs with maximum speed of 177.5 MHz with jitter below 1.3 psec RMS

Ordering Information

ZL30158GGG2	64 Pin LBGA*	Trays

*Pb Free Tin/Silver/Copper
-40°C to +85°C

- Operates from a single crystal resonator or crystal oscillator
- Customer defined default device configuration, including input/output frequencies, is available via OTP(One Time Programmable) memory
- Dynamically configurable via SPI/I2C interface and volatile configuration registers

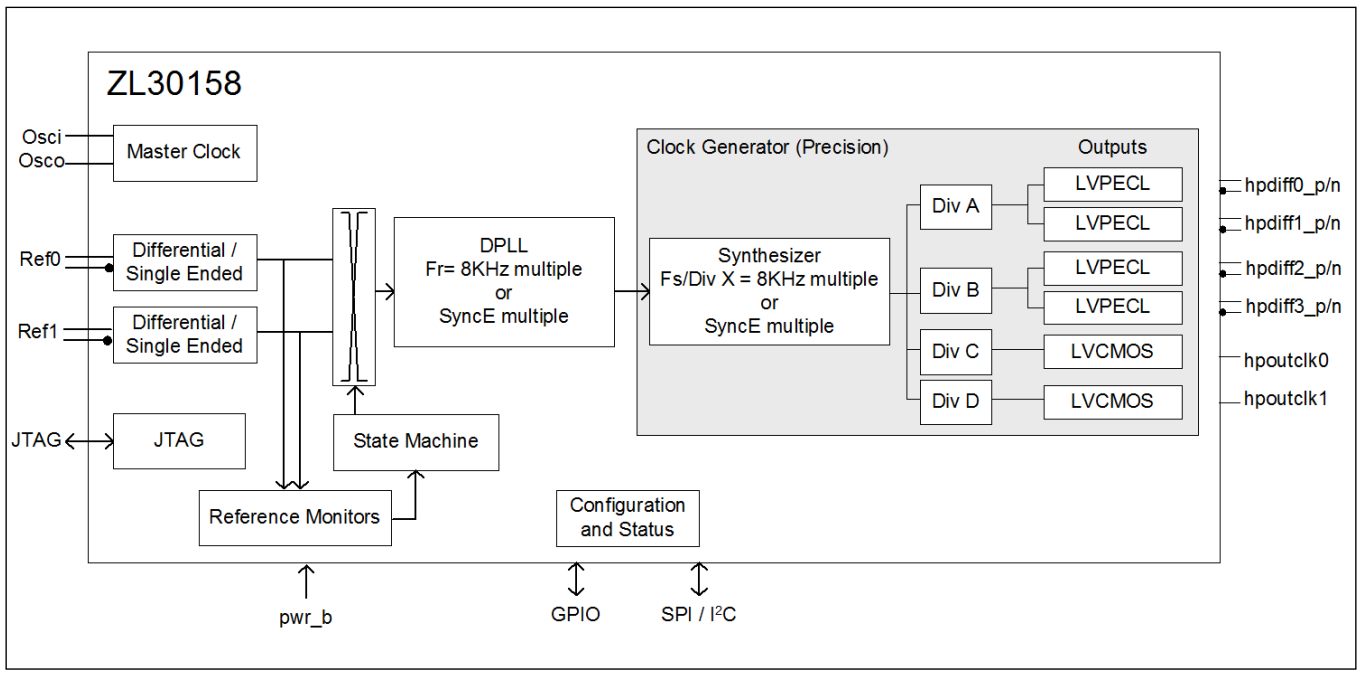


Figure 1 - Functional Block Diagram

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Applications

- Clock Generation for Physical Line Interface:
  - Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W
  - SONET/SDH, OC-192/OC-48
  - 100 BaseX, GE, Fibre channel
- Clock Generation and Distribution for back plane Interface:
  - TDM, Telecom Bus, Utopia, SBI
  - XAUI

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Change Summary

Below are the changes from the June 2012 issue to the March 2015 issue

Page	Item	Change
1	“Ordering Information“	Removed ZL30158GGG (leaded version) from the ordering information
1	Added Features bullet	Included availability of customer defined default configurations
16, 30, 30	Updated section 4.0, 5.0 and added 5.1	Updated to included the availability of Custom OTP configuration
101	13.0, “Package Markings“	Added section 13.0 for package markings

Below are the changes from the January 2012 issue to the June 2012 issue

Page	Item	Change
46 and 83	Register 0xC6 - Chip_Revision_2	Updated chip_revision_2 register 0xC6 = 0x03

Below are the changes from the December 2011 issue to the January 2012 issue

Page	Item	Change
41	Procedure to write registers	Added new procedure to update registers
42	Time between two write acesses to the same register	added register 0x0D to registers not requiring a wait time.;
42	Sticky Read Registers	Updated the StickyR procedure
46, 83	Register 0xC6 - Chip_revision_2	Added register 0xC6
47	Register 0x00 -id_reg	Updated Chip_revision bits[6:5]
52	Register 0x0D - Sticky_r_lock	Updated description of register 0x0D

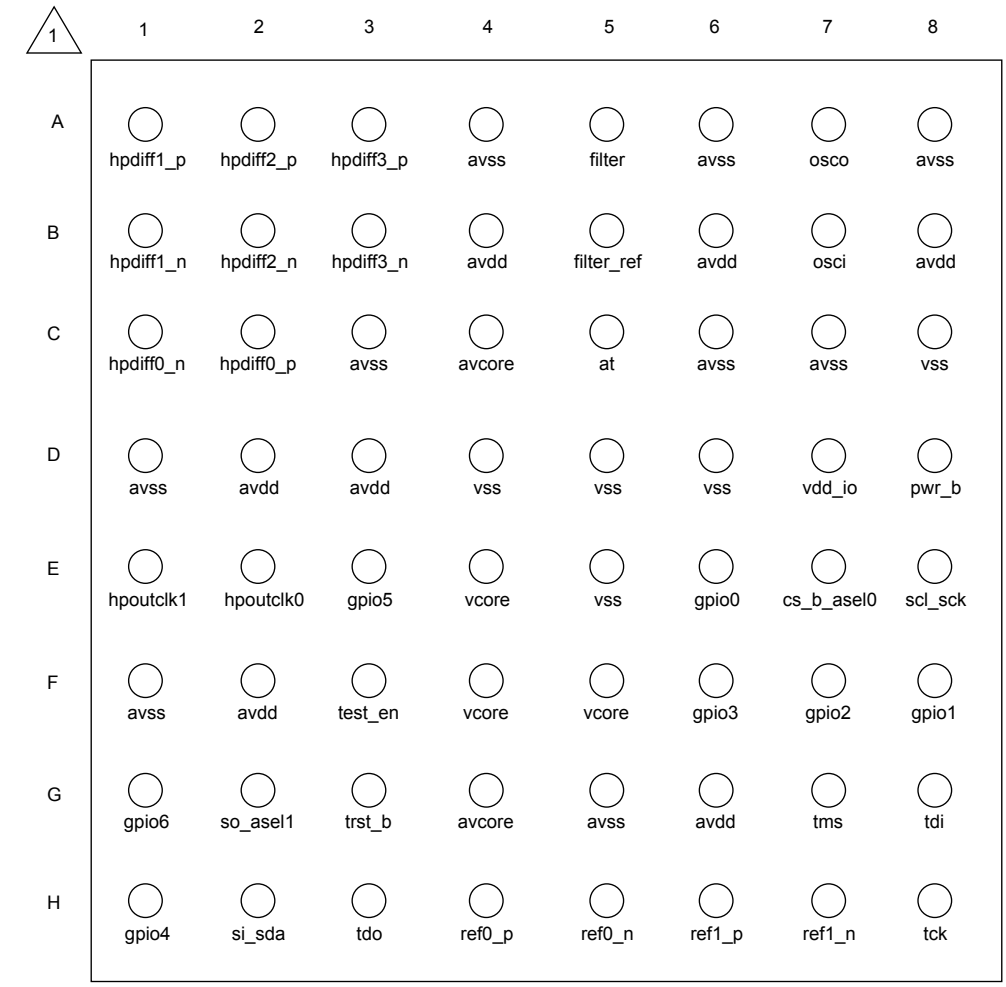
Below are the changes from the March 2011 issue to the December 2011 issue

Page	Item	Change
1	Features	• Maximum output frequency is changed from "720MHz" to "750MHz" • Maximum input frequency is changed from "720MHz" to "750MHz" • Corrected package description in ordering information to LBGA

Page	Item	Change
11	Pin description	• Maximum frequency limit on differential outputs is changed from " 720MHz" to "750MHz" • Maximum frequency limit on differential inputs is changed from " 720MHz" to "750MHz" • Pin B3 name is changed from "hpdifn_3" to "hpdiffn_3"
15	Application example	Maximum frequency is changed from " 720MHz" to "750MHz"
16	Input Sources	Maximum frequency limit on differential inputs is changed from " 720MHz" to "750MHz"
20	Divider and skew management	Maximum frequency limit on differential outputs is changed from " 720MHz" to "750MHz"
21	Output drivers	Maximum speed of differential outputs is changed from " 720MHz" to "750MHz"
24	Input Buffers	Input frequency range for differential inputs is changed fromfrom "8kHz to 720MHz" to "8kHz to 750MHz"
32	DPLL0 Lock Indication 2	"1us during 10s period" lock condition is changed to "10us during 1s period" .
35	Un-managed Mode	LOS detected a failure and RefSwMask<0> is at logic “1” changed to LOS detected a failure and HOMask<0> is at logic “1”
36	Managed mode	LOS detected a failure and RefSwMask<0> is at logic “1” changed to LOS detected a failure and HOMask<0> is at logic “1”
42	Time between two write accesses to the same register	Changed wait time from 5ms to 7ms
42	Reading from Sticky Read (StickyR) Registers	Updated StickyR procedure
43	Table 6	Heading of first column is changed from “Page_Addr” to “Reg_Addr”
47	Register 0x00	Updated ready_indication bit description
69	Detailed Register Map	"Page_Address" is changed to "Register_Address" for registers which addresses are from 0x80 to 0x85
57	Register 0x33	Added details to the description of bits[7:6]
62	Register 0x4C	000 = +/- 0.1% (in Ref0 frequency units) changed to 000 = +/- 0.1% (in Ref1 frequency units)
74	Register synth_post_div_C	Bit[15:0]: "note 3" added for odd post divider
77	Register synth_post_div_D	Bit[15:0]: "note 3" added for odd post divider
87	Register 0xF7	Updated description for spurs_suppression register

Page	Item	Change
89	DC Electrical Characteristics -Power Core	• "Power for Each Synthesis Engine” is changed to “Current for Each Synthesis Engine” • “P_{SYN}” is changed to “I_{SYN}”
92	AC Electrical Characteristics* - Inputs	Maximum frequency of differential inputs is changed from " 720MHz" to "750MHz"
94	AC Electrical Characteristics* - Outputs	Maximum frequency of differential outputs is changed from " 720MHz" to "750MHz"
98	Output Clocks Jitter Generation	Jitter measurement filter for 77.76MHz is changed from "12kHz-5MHz" to "12kHz-20MHz"
100	Section 12.0	Replaced drawing to reflect correct package description

1.0 Pin Diagram



1 - A1 corner is identified by metallized markings.

2.0 Pin Description

All device inputs and output are LVCMOS unless it was specifically stated to be differential.

Ball #	Name	I/O	Description
Input Reference			
H4 H5 H6 H7	ref0_p ref0_n ref1_p ref1_n	I	**Input Reference 0 and 1.** Input reference sources used for synchronization. The positive and negative pair of these inputs accepts a differential input signal. The refx_p input terminal accept a CMOS input reference. These inputs could be used as a device external feedback input. Maximum frequency limit on single ended inputs is 177.496 MHz, and 750 MHz on differential inputs.
Output Clocks			
E2 E1	hpoutclk0 hpoutclk1	O	**High Performance Output Clock 0 to 1.** This output can be configured to provide any one of the single ended high performance clock outputs. Maximum frequency limit on single ended LVCMOS outputs is 177.5 MHz
C2 C1 A1 B1 A2 B2 A3 B3	hpdiff0_p hpdiff0_n hpdiff1_p hpdiff1_n hpdiff2_p hpdiff2_n hpdiff3_p hpdiff3_n	O	**High Performance Differential Output Clock 0 to 3 (LVPECL).** This output can be configured to provide any one of the available high performance differential output clocks. Maximum frequency limit on differential outputs is 750 MHz
Control and Status			
D8	pwr_b	I	**Power-on Reset.** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. The pwr_b pin should be held low for at least 2 ms. This pin is internally pulled-up to V_{DD}. **User can access device registers either 50 ms after pwr_b goes high, or after bit 7 in register at address 0x00 goes high which can be determined by polling address 0x00.**

Table 1 - Pin Description

Ball #	Name	I/O	Description
E6 F8 F7 F6 H1 E3 G1	gpio0 gpio1 gpio2 gpio3 gpio4 gpio5 gpio6	I/O	**General Purpose Input and Output pins.** These are general purpose pins managed by the internal processor based on device configuration. Recommended usage of GPIO include: • DPLL lock indicators • DPLL holdover indicators • Reference fail indicators • Reference select control or monitor • Differential output clock enable (per output or as a bank of 2 or 4 outputs) • High performance LVCMOS output enable • Host Interrupt Output: flags changes of device status prompting the processor to read the enabled interrupt service registers (ISR). • Microport interface protocol I2C or SPI • Master Clock frequency rate Pins 5:0 are internally pulled down to GND and pin 6 is internally pulled up to V_{DD}. **After power on reset, device GPIO[0,1,3,4,5] configure some of device basic functions, GPIO[3] set I2C or SPI control mode, GPIO[1,0] set master clock rate selection. The GPIO[0,1,3] pins must be either pulled low or high with an external 1 KΩ resistor as needed for their assigned functions at reset; or they must be driven low or high for 50 ms after reset, and released and used for normal GPIO functions.** **The GPIO[4,5] pins must be either pulled low with external 1 KΩ resistors; or they must be driven low for 50 ms after reset, and then released and used for normal GPIO functions.**
Host Interface			
E8	scl_sck	I/O	**Clock for Serial Interface.** Provides clock for serial micro-port interface. This pin is also the serial clock line (SCL) when the host interface is configured for I2C mode. As an input this pin is internally pulled up to V_{DD}.
H2	si_sda	I/O	**Serial Interface Input.** Serial interface input stream. The serial data stream holds the access command, the address and the write data bits. This pin is also the serial data line (SDA) when host interface is configured for I2C mode. This pin is internally pulled up to V_{DD}.
G2	so_asel1	I/O	**Serial Interface Output.** Serial interface output stream. As an output the serial stream holds the read data bits. This pin is also the I2C address select when host interface is configured for I2C mode.
E7	cs_b_asel0	I	**Chip Select for Serial Interface.** Serial interface chip select, this is an active low signal. This pin is also the I2C address select when host interface is configured for I2C mode.This pin is internally pulled up to V_{DD}.
APLL Loop Filter			

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
A5	filter	A	**External Analog PLL Loop Filter terminal.**
B5	filter_ref	A	**Analog PLL External Loop Filter Reference.**
JTAG (IEEE 1149.1) and Test			
F3	test_en	I	**Test Mode Enable.** A logic high at this pin enables device test modes. This pin is internally pulled down to GND. Connect this pin to GND.
C5	at	A-I/O	**Analog PLL Test.** Test pin for analog PLL. Leave unconnected.
H3	tdo	O	**Test Serial Data Out.** JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
G8	tdi	I	**Test Serial Data In.** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
G3	trst_b	I	**Test Reset.** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to VDD. If this pin is not used then it should be connected to GND.
H8	tck	I	**Test Clock.** Provides the clock to the JTAG test logic. This pin is internally pulled up to V_{DD}. This pin is internally pulled up to VDD. If this pin is not used then it should be connected to GND.
G7	tms	I	**Test Mode Select.** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
Master Clock			
A7	osco	A-O	**Oscillator Master Clock.** For crystal operation, a crystal is connected from this pin to osci. Not suitable for driving other devices. For clock oscillator operation, this pin is left unconnected.
B7	osci	I	**Oscillator Master Clock.** For crystal operation, a crystal is connected from this pin to osco. For clock oscillator operation, this pin is connected to a clock source.
Power and Ground			
D7	V_{DD-IO}		**Positive Supply Voltage IO.** $3.3V_{DC}$ nominal.
E4 F4 F5	V_{CORE}		**Positive Supply Voltage.** $+1.8V_{DC}$ nominal.

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
B4 B6 B8 D2 D3 F2 G6	AV_{DD}		**Positive Analog Supply Voltage.** +3.3V_{DC} nominal.
C4 G4	AV_{CORE}		**Positive Analog Supply Voltage.** +1.8V_{DC} nominal.
C8 D4 D5 D6 E5	V_{SS}		**Ground.** 0 Volts.
A4 A6 A8 C3 C6 C7 D1 F1 G5	AV_{SS}		**Analog Ground.** 0 Volts.

Table 1 - Pin Description (continued)

3.0 Application Example

The device integrates a digital PLL and a high-speed low-jitter clock synthesizer. The digital PLL locks to reference frequencies as low as 8 kHz while maintaining loop stability and while maintaining the device's low-jitter generation. The digital PLL ensures reference switches occur in a hitless manner even with low frequency references, preventing bit errors on the transmission links. The digital PLL implements loop filters with settings as low as 14 Hz to clean noisy references; or as high as 896 Hz to closely track less noisy references. The high-speed low-jitter clock synthesizer generates clocks with frequencies as high as 750 MHz with typical jitter performance below 0.7 ps RMS. The digital PLL plus high-speed synthesizer architecture allows the device to easily convert between SONET/SDH and Ethernet frequencies.

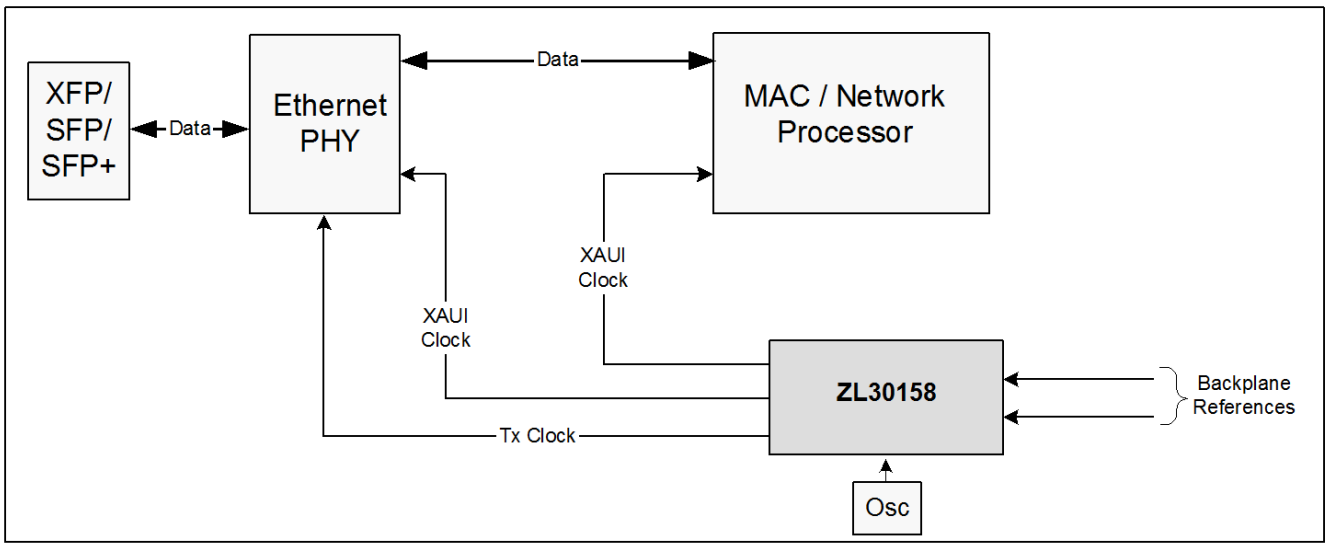


Figure 2 - Application Diagram

4.0 Functional Description

The functional block diagram of the device is shown in Figure 1. The ZL30158 is a SyncE and Telecom Rate Clock Translator that can be configured by any of the following methods; power-up with its default configuration; power-up with a custom OTP (One Time Programmable) configuration; after power-up it can be dynamically configured via the SPI/I2C port. Configurations set via the SPI/I2C are volatile and will need to be rewritten if the device is reset or powered-down. The SPI/I2C port is also used to access the status registers. The ZL30158's detailed operation is described in the following sections.

4.1 Input Sources

The device has 3 input sources: 2 input references (single ended or differential) and one oscillator clock source (oscillator or xtal).

The device master clock frequency is configured on reset via external voltage levels on GPIO[1:0] pins. The recommended frequency of the master clock is 24.576 MHz.

The device input reference frequency is programmed during initialization, change of input reference frequency can be supported if DPLL was forced in to Holdover mode before a frequency change. Automatic detection of input reference frequency is not supported.

The device accepts an input reference with maximum frequency of 177.5 MHz through single ended LVCMOS input (or 750 MHz frequency through differential inputs) and a minimum frequency of 8 kHz.

The device synchronizes (locks) to any Telecom or SyncE input reference.

4.1.1 SyncE References

The device can synchronize to any input frequency which is multiple of 25 kHz or multiple of 25 kHz * 66/64. Small subset of supported and commonly used SyncE frequencies is: 25 MHz, 125 MHz, 156.26 MHz, 161.1328125 MHz, 625 MHz.

4.1.2 Telecom References

The device can synchronize to any multiple of 8 kHz up to 524.28 MHz and to any multiple of 16 kHz for input frequencies between 524.28 MHz and 750 MHz. Small subset of supported and commonly used Telecom frequencies is: 8 kHz, 64 kHz, 1.544 MHz (DS1), 2.048 MHz (E1), 6.312 MHz (DS2), 8.448 MHz (E2), 34.368 MHz (E3), 44.736 (DS3), as well as SONET/SDH clock frequencies:19.44 MHz, 77.76 MHz, 155.52 MHz, 622.08 MHz.

4.2 Input Reference Monitoring

The input references are monitored by two reference monitor schemes, independent for each reference. They indicate abnormal behavior of the reference signal, for example; drift from its nominal frequency or excessive jitter.

- **Loss of Signal Monitor (LOS):** LOS is an external signal, fed to one of ZL30158 GPIO pins. LOS is typically generated by a PHY device whose recovered clock is fed to one of ZL30158 reference inputs. PHY device will generate LOS signal when it cannot reliably extract the clock from the line. User can set one of GPIO pins as LOS input by programming corresponding GPIO register.
- **Coarse Frequency Monitor (CFM)**: This circuit monitors the reference over a short time interval. It detects large frequency irregularities (larger than 0.1%).
- **Single Cycle Monitor (SCM)**: This detector checks the period of a single clock cycle to detect large phase hits or the complete loss of the clock.
- **Guard Soak Timer (GST):** Timer associated with the CFM and SCM modules to disqualify the reference input signal (see Table 2)

- The monitor failure indicators are flagged in the status registers and have associated mask bits, as follows:
- Reference Fail Mask: Ref0FailMask<3:0>, Ref1FailMask<3:0>: these mask bits masks the failure indicator on corresponding fail pins/bits.
- Reference Switching Mask for the current active (locked to) reference: RefSwMask<3:0> these mask bits masks the failure indicators that are used in the automatic reference switching state machine independently for each supported DPLL.
- Holdover Mask for the current active (locked to) reference: HOMask<3:0>, these mask bits masks the failure indicators that are used to go into auto-holdover independently for each supported DPLL.
- MSB bit for GST and LSB bit for LOS

The single cycle and coarse monitor failure flags feed a timer (Guard Soak Timer) that disqualifies the reference input signal when the failures are present for more than the period of time defined in Table 2.

Guard Soak Timer Control bits in control register	Time to disqualify a reference in Timing Card Application	Notes
00	minimum delay possible	
01	10 ms	
10	50 ms	default value
11	2.5 s	

Table 2 - Guard Soak Time To Disqualify A Reference

The Guard Soak Timer that is used for the CFM and SCM modules has a built-in decay time hysteresis according to Table 3 (Timer to Qualify a reference) to prevent flickering of status bits at the threshold boundaries.

The Timer to Qualify a reference is a multiple of the Guard Soak Timer. Table 3 shows the multiplication factor to multiply the Guard Soak Timer to calculate the time to qualify a reference.

Control bits to control the Timer to qualify a reference	Multiples of the Guard Soak Time to qualify a reference	Notes
00	2	
01	4	Default value
10	16	
11	32	

Table 3 - Guard Soak Time To Qualify A Reference

When a GPIO pin is used as a reference fail indicator, it indicates a valid reference if:

- The SCM does not detect phase hits, nor complete loss of clock or Ref<i>FailMask<1> is at logic “0”
- The CFM does not detect phase irregularity or Ref<i>FailMask<2> is at logic “0”
- The Guard Soak Time is triggered or Ref<i>FailMask<3> is at logic “0”

4.2.1 DPLL General Characteristics

Pull-in Hold-in range

The DPLL supports pull-in/hold-in of +/-52 ppm, +/-130 ppm, +/-400 ppm or +/-3900 ppm.

DPLL bandwidth (jitter/wander transfer)

The DPLL supports the following first order filtering cut-off frequencies (14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz and 896 Hz), DPLL bandwidth is determined during initialization.

The DPLL locks to an input reference and provides stable low jitter output clock if the selected loop bandwidth is less than 1/30th the input reference frequency. As an example, a 19.44 MHz reference could allow a bandwidth up to 896 Hz, and a 8 kHz reference would allow a maximum loop bandwidth of 56 Hz.

Jitter/Wander Generation

Jitter and wander generation performance (detailed in section 10.0, “Performance Characterization“).

Phase Transients

On reference switch with phase tracking active (i.e., TIE clear active or glitch-less reference switching), the DPLL transitions the phase of the output smoothly, limited by the selected loop bandwidth and by the selected phase slope limit.

The Microsemi device offers the following phase slope limiting options: 61 usec/sec, 7.5 usec/sec, 0.885 usec/sec or unlimited.

Holdover Stability

DPLL initial holdover accuracy is better than 50 ppb.

Input Tolerance Criteria

Input tolerance indicates that the device tolerates certain jitter, wander and phase transients at its input reference while maintaining outputs within an expected performance and without experiencing any alarms, reference switching or holdover conditions. Input tolerance is associated with input reference source characteristics and the standards associated with input reference type.

DPLL Monitoring

The DPLL provides lock and holdover indicators.

The lock time is dependent on employed loop bandwidth. The device has a lock time of less than 1 sec for all available DPLL loop bandwidth selections.

4.2.2 DPLL States

The device DPLL supports three states: Free-run, Normal (Locked) and Holdover. The Holdover and Free-run states are used to cope with reference impairments.

Each of these modes have a corresponding state in the internal State Machine described as follows:

Freerun State: the Freerun state is entered when synchronization to the reference is not required or is not possible. Typically this occurs immediately following system power-up. In the Freerun State, the device provides timing and synchronization signals which are based on the master clock frequency (supplied to osci pin) only, and are not synchronized to the reference input signals. The freerun accuracy of the output clock is equal to the accuracy of the master clock (osci). So if a ±20 ppm freerun output clock is required, the master clock must also be ±20 ppm.

Holdover State: the Holdover State is typically entered when input reference is temporarily disrupted. In the Holdover State, the device provides output clocks which are not locked to an external reference signal, but are based on storage techniques. The storage value is determined while the device is in Normal Mode and locked to an external reference signal. Initial holdover accuracy is a function of DPLL while holdover drift is reliant on the drift of the master clock (osci).

Normal State: the Normal State is entered when a valid reference clock is available for synchronization. In the Normal State the device provides output clocks which are synchronized to one of the available 2 input references. From a reset condition - if a valid input reference is available - the device takes less than a second (lock time) to output signals which are synchronized (phase and frequency locked) to the reference input.

4.2.3 DPLL Rate Conversion Function

The DPLL provides up scaling and down scaling functions

The DPLL supports rate conversion from Telecom to SyncE frequencies and vice versa.

The DPLL has the ability to switch from normal rate (before FEC is negotiated) to FEC rate and vice versa.

The following is just an example of the frequencies that can be supported (many more frequencies can be supported):

- **GbE:**
  - 25 MHz
  - 125 MHz
- **XAUI (chip to chip interface, which is a common chassis to chassis interface)**:
  - 156.25 MHz or x2 or x4 version
- **OC-192/STM-64:**
  - 155.52 MHz or x2 or x4 version
- **10 GbE:**
  - 156.25 MHz which is 125 MHz x 10/8 or x2 or x4 version
  - 156.25 MHz x 66/64 or x2 or x4 version
- Application Note ZLAN-267 explains how to generate the most common frequencies.

4.2.4 DPLL Input to Output And Output to Output Phase Alignment

Techniques offered for Phase Alignment

When the output clock is locked to a jitter free and wander free input clock, input to output latency is expected to have a typical error of 0 nsec.

The coarse and fine phase adjustments allow for input to output and output to output latency corrections to compensate for PCB load delay, as detailed in 4.6, “Output Drivers“.

4.3 Frequency Synthesis Engine

The device frequency synthesis engine is comprised of a hardware DCO and an analog jitter filtering APLL with built-in digital jitter attenuation scheme. The ultra low jitter frequency synthesis engine can generate output clocks which meet the jitter generation requirements detailed in section 10.0, “Performance Characterization“.

The frequency synthesis engine’s APLL requires an external RC loop filter as described in section 4.13

The frequency synthesis engines can generate any clock which is: M x 8 kHz, M x 25 kHz or M x 25 kHz x 66/64 where M is an integer.

When the DPLL is locked to an input reference, the DCO external control can be used. The DCO external control allows for the calibration of the DCO center frequency to adjust for external system oscillator center frequency.

4.4 Dividers and Skew Management

The device has 4 independent dividers associated with frequency synthesis engine.

The divider engines associated with the high performance differential outputs generate output clocks between 8 kHz and 750 MHz with 50% duty cycle. The other divider engines generate output clocks between 8 kHz and 177.5 MHz with 50% duty cycle.

The divider modules generating the single ended output clocks provides the ability to manage the phase skew of the output clock by a coarse step equal to the internal high speed clock period.

The single ended generated output clocks can be stopped either on rising or falling edge (programmed through serial interface or GPIO).

4.5 Output Multiplexer

Figure 3 shows the multiplexing configuration that is supported.

The muxing configuration allows for the oscillator input or the xtal buffered input (osc_clk) to be driven to one of the available programmable output drivers.

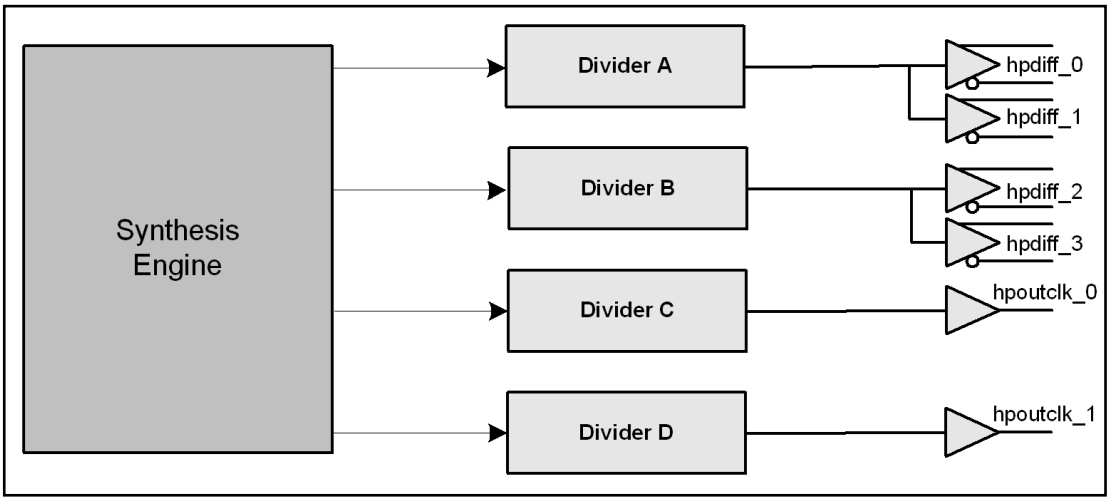


Figure 3 - Output Clocks Muxing Configuration

4.6 Output Drivers

The device has 4 high performance (HP) differential (LVPECL) outputs.

The device has 2 high performance (HP) single ended (LVCMOS) outputs.

High Performance (HP) single ended driver (LVCMOS) supports the jitter specification detailed in section 10.0, “Performance Characterization“ and a maximum speed of 177.5 MHz.

The high performance (HP) differential driver (LVPECL) supports the jitter specification detailed in section 10.0, “Performance Characterization“ and a maximum speed of 750 MHz.

HP differential LVPECL outputs should be terminated as shown in Figure 4. Terminating resistors provide 50 Ω equivalent Thevenin termination as well as biasing for the output LVPECL driver. Terminating resistors should be placed as close as possible to input pins of the LVPECL receiver. If the LVPECL receiver has internal biasing then AC coupling capacitors should be added.

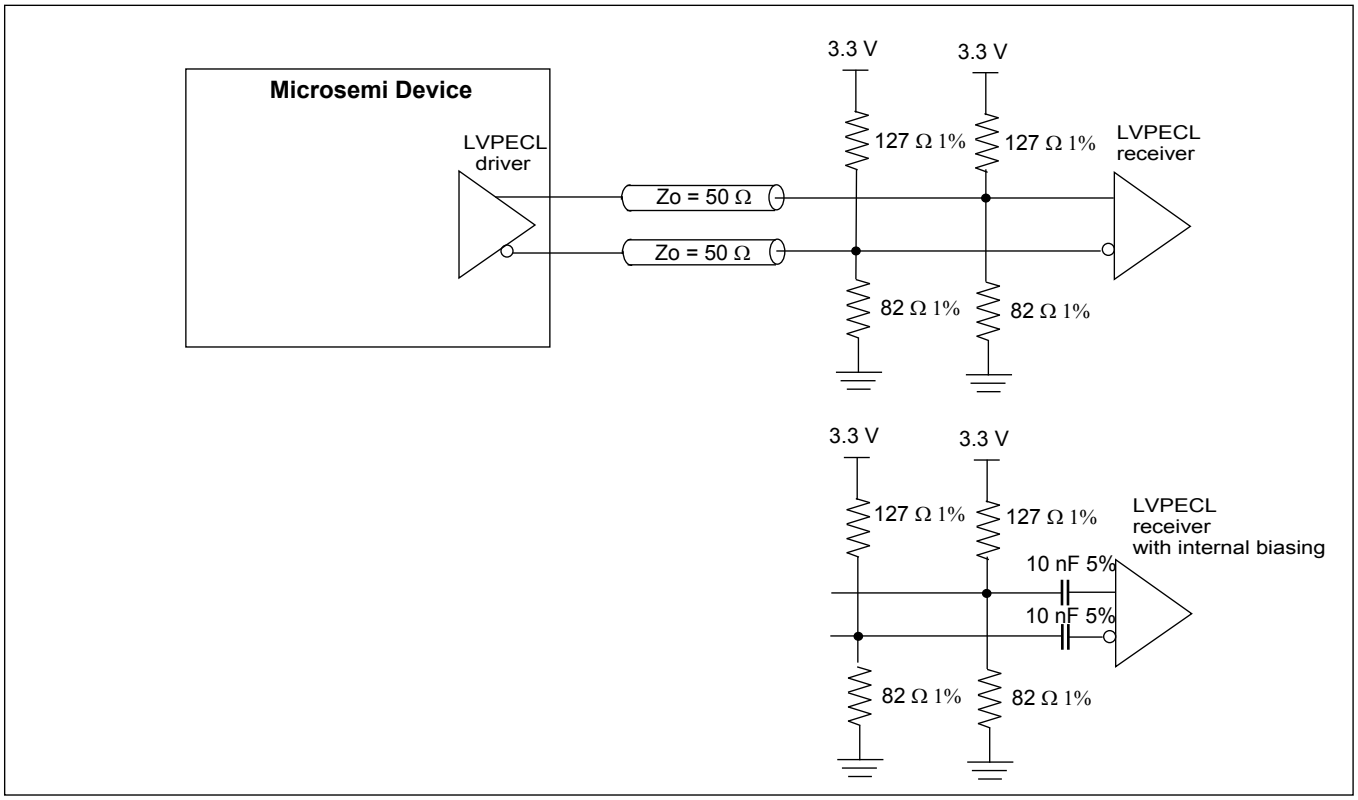


Figure 4 - Terminating HP LVPECL Outputs

If the transmission line is required to be AC coupled then the termination shown in Figure 5 should be implemented. 200 Ω resistors are used to provide DC biasing for LVPECL driver. Both AC coupling capacitor and biasing resistors should be placed as close as possible to output pins.

Thevenin termination (127 Ω and 82 Ω resistors) provide 50 Ω termination as well as biasing of the input LVPECL receiver. If the LVPECL receiver has internal DC biasing then the line should be terminated with 100 Ω termination resistor between positive and negative input. In both cases termination resistors should be places as close as possible to the LVPECL receiver pins. Some LVPECL receivers have internal biasing and termination. In this case no external termination should be present.

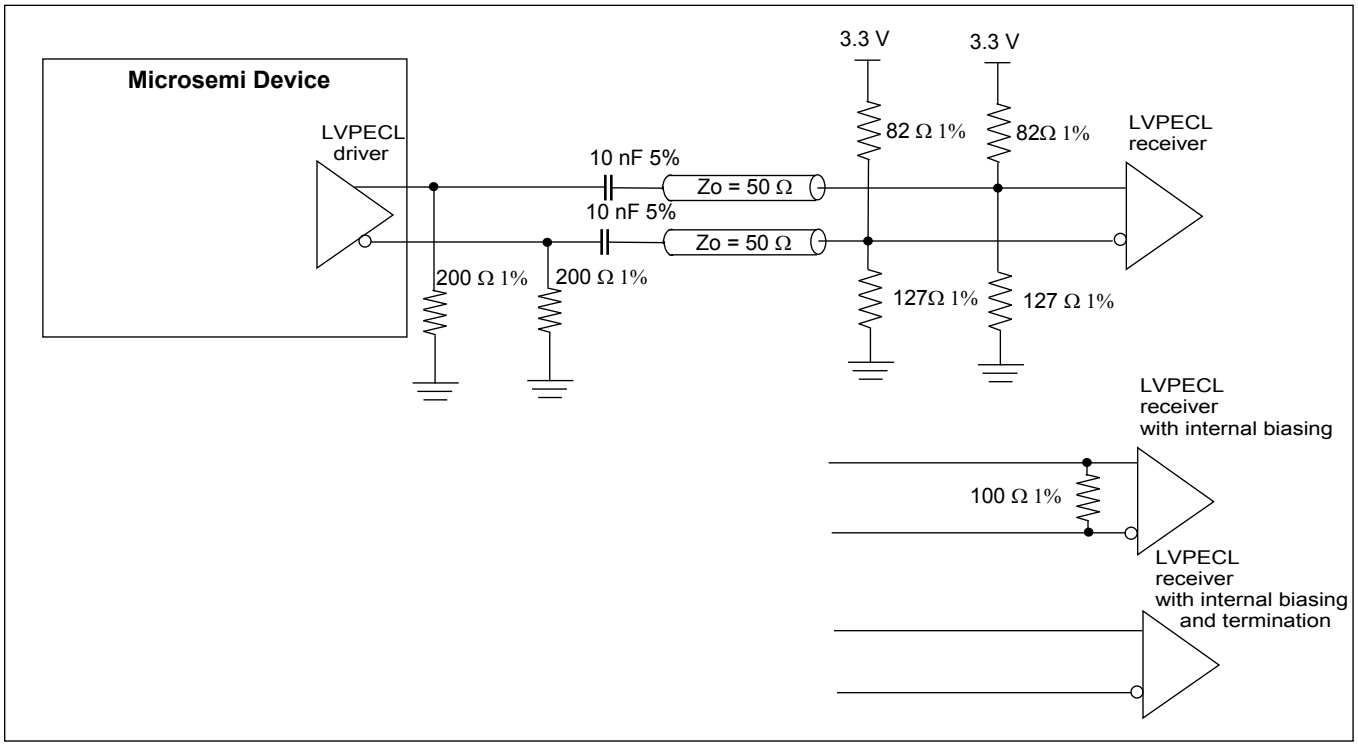


Figure 5 - Terminating AC coupled HP LVPECL Outputs

High performance LVCMOS outputs (hpoutclkx) should be terminated at the source with 22 Ω resistor as shown in Figure 6.

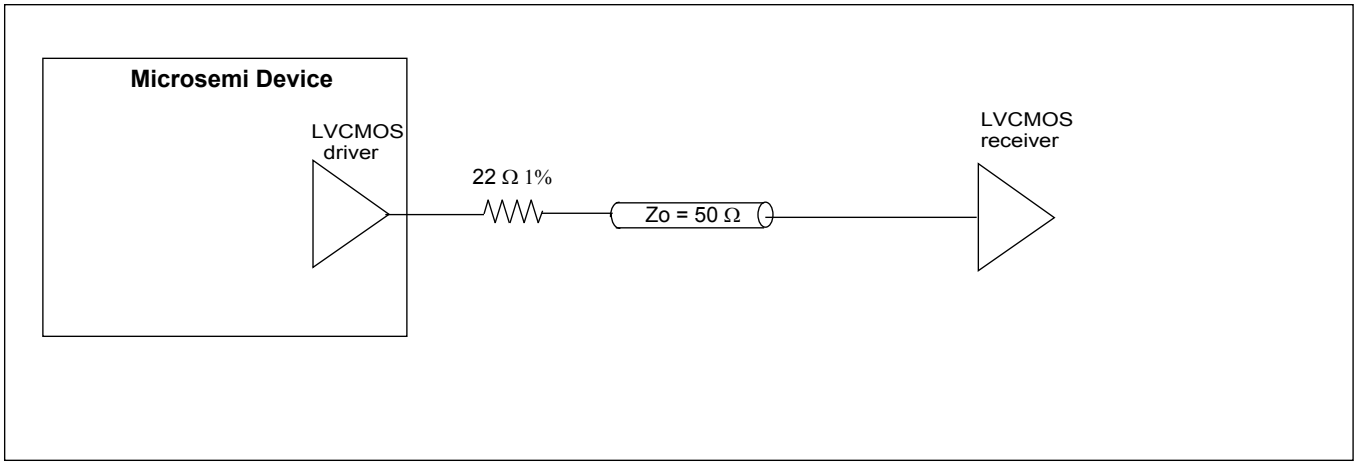


Figure 6 - Terminating HP LVCMOS Outputs

4.7 Input Buffers

ZL30158 has two reference inputs ref[1:0]_p/ref[1:0]_n that can work as either single ended or differential. By default ref0 is differential and ref1 is single ended. This can be changed by programming ref_config register at address 0x0A.

Input frequency range for differential inputs is: 8 kHz to 750 MHz; for single ended inputs is: 8 kHz to 177.5 MHz.

Differential reference inputs need to be properly terminated and biased as shown in Figure 7 and Figure 8 for LVPECL and Figure 9 and Figure 10 for LVDS drivers. When terminating LVPECL signal, it is necessary either to adjust termination resistors for DC coupling or to AC couple the LVPECL driver because ZL30158 differential inputs have different common mode (bias) voltage than LVPECL receivers. Thevenin termination (182 Ω and 68 Ω resistors) provide 50 ohm equivalent termination as well as biasing of the input buffer for DC coupled line. For AC coupled line, Thevenin termination with 127 Ω and 82 Ω resistors should be used as shown in Figure 8. The value of the AC coupling capacitors will depend on the minimum reference clock frequency. The value of 10 nF is good for input clock frequencies above 100 MHz. For lower clock frequencies capacitor values will have to be increased.

Terminations for DC and AC coupled LVDS line are shown in Figure 9 and Figure 10 respectively. Differential input biasing is provided by LVDS driver in case of DC coupling (Figure 9), whereas for AC coupling (Figure 10) biasing is generated by 12 KΩ and 8.2 KΩ resistors. In both cases, the line is terminated with 100 Ω.resistor.

For single ended CMOS inputs, refx_n input needs to be connected to the ground as shown in Figure 11. The value of series termination resistor will depend on CMOS output driver but the most common values are 33 Ω and 22 Ω.

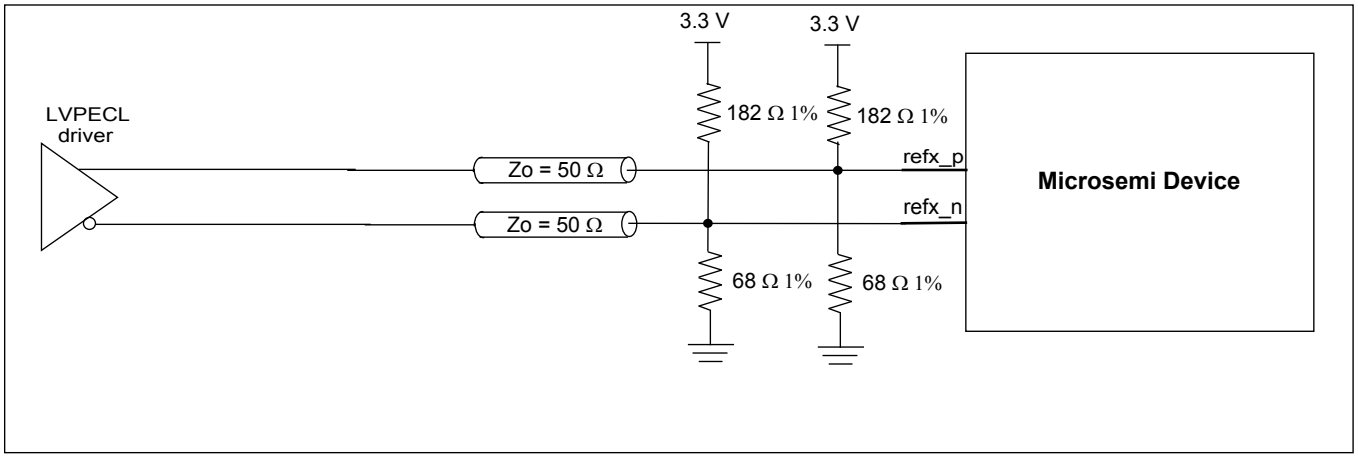


Figure 7 - Differential DC coupled LVPECL Termination

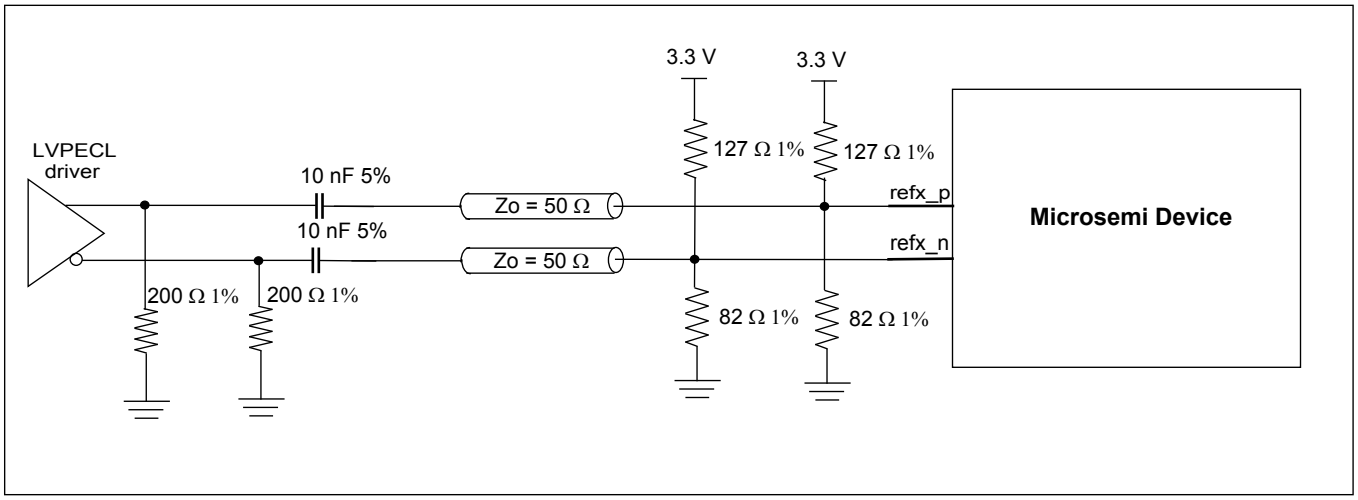


Figure 8 - Differential AC Coupled LVPECL Termination

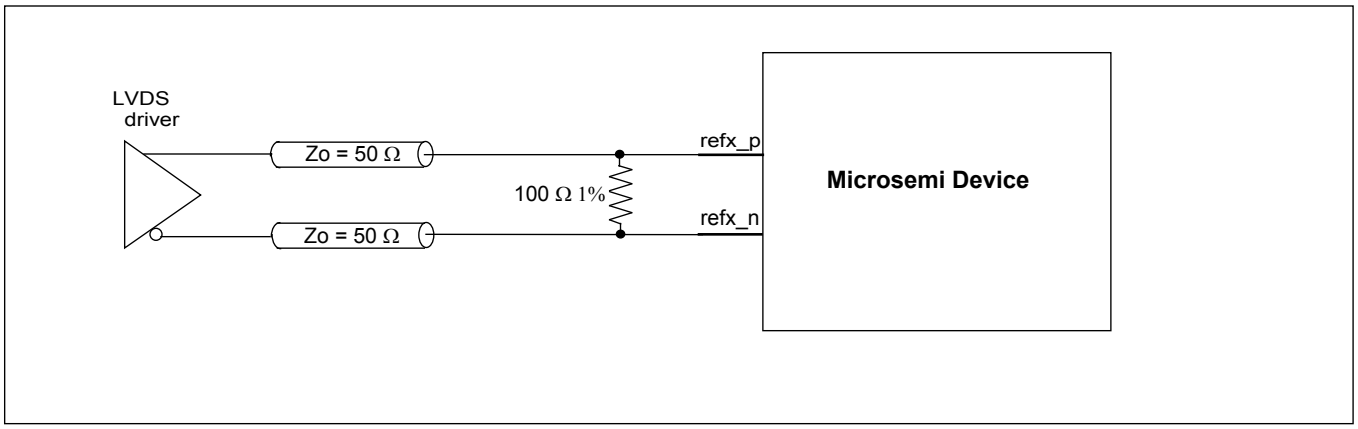


Figure 9 - Differential DC Coupled LVDS Termination

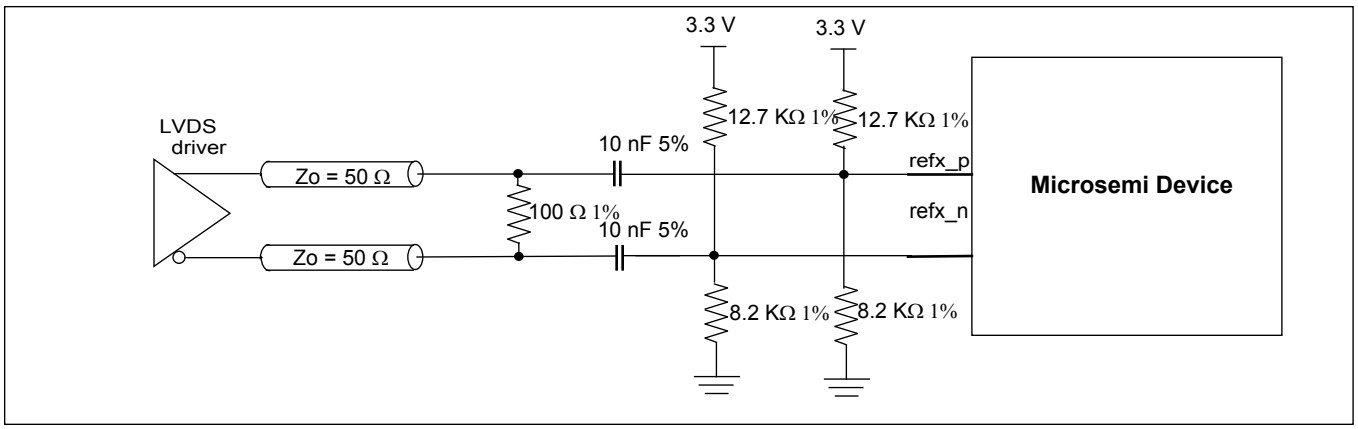


Figure 10 - Differential AC Coupled LVDS Termination

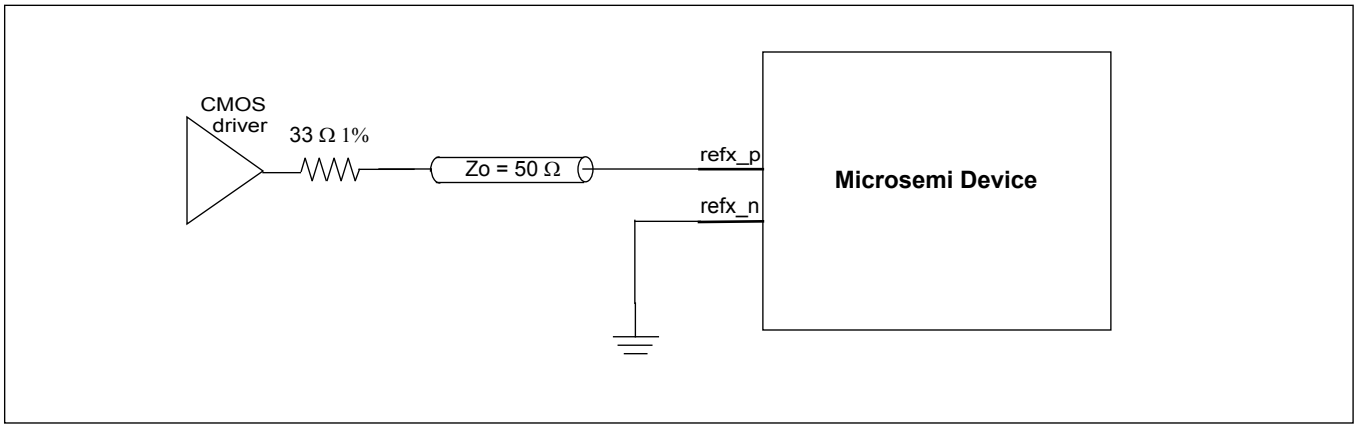


Figure 11 - Single ended CMOS Termination

4.8 Master Clock Interface

The master oscillator determines the DPLL's free-run frequency accuracy and holdover stability. The reference monitor circuitry also uses this frequency as its point of reference (0 ppm) when making frequency measurements. The master clock interface was designed to accept either a free-running clock oscillator (XO) or a crystal (XTAL). Refer to application note ZLAN-68 for a list of recommended clock oscillators.

4.9 Clock Oscillator

When using a clock oscillator as the master timing source, connect the oscillator's output clock to the **osci** pin as shown in Figure 12. The connection to osci should be direct and not AC coupled. The **osco** pin must be left unconnected.

When using crystal resonator as the master timing source, connect crystal between **osci** and **osco** pins as shown in Figure 12. Crystal should have bias resistor of 1 MΩ and load capacitances C1 and C2. Value of load capacitances is dependent on crystal and should be as per crystal datasheet. Crystal should be a fundamental mode type -- not an overtone. See ZLAN-68 for crystal recommendation.

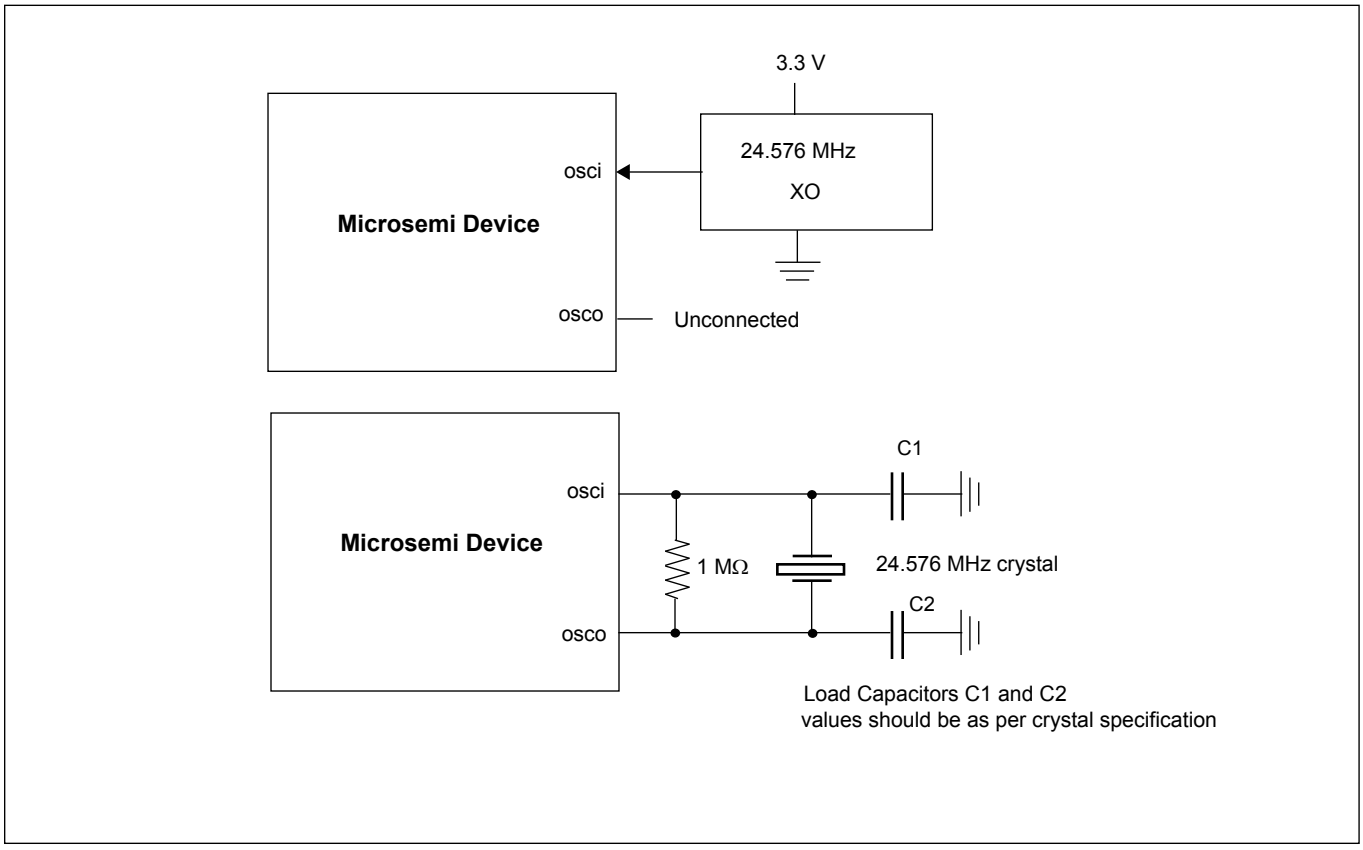


Figure 12 - Clock Oscillator Circuit

The device internal system clocks are generated off the device master clock input (Oscillator or a crystal employing an on-chip buffer/driver). The master clock selection is done at start-up using the available GPIO pins, right after pwr_b get de-asserted. GPIO[0,1] pins need to be held high for 50 ms after the de-assertion of pwr_b, after which time they can be released and used as any other GPIO. Alternatively, these pins can be pulled high with 1 KΩ resistors.

GPIO [1:0]	Master Clock Frequency
0	reserved
1	reserved
2	reserved
3	24.576 MHz

Table 4 - Master Clock Frequency Selection

4.10 Power Up/Down Sequence

The 3.3 V power rail should be powered before or simultaneously with the 1.8 V power rail to prevent the risk of latch-up (latch-up occur when the 1.8 V supply exceeds the 3.3 V rail by more than 1.8 V).

The power-down sequence is less critical, however it should be performed in the reverse order to reduce transient currents that consume power.

4.11 Power Supply Filtering

Jitter levels on the output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins. For recommended common layout practices, refer to Application Note ZLAN-230.

4.12 Reset and Configuration Circuit

To ensure proper operation, the device must be reset by holding the pwr_b pin low for at least 2 ms after power-up. Following reset, the device will operate under specified default settings.

The reset pin can be controlled with on-board system reset circuitry or by using a stand-alone power-up reset circuit as shown in Figure 13. This circuit provides approximately 2 ms of reset low time. The pwr_b input has Schmidt trigger properties to prevent level bouncing.

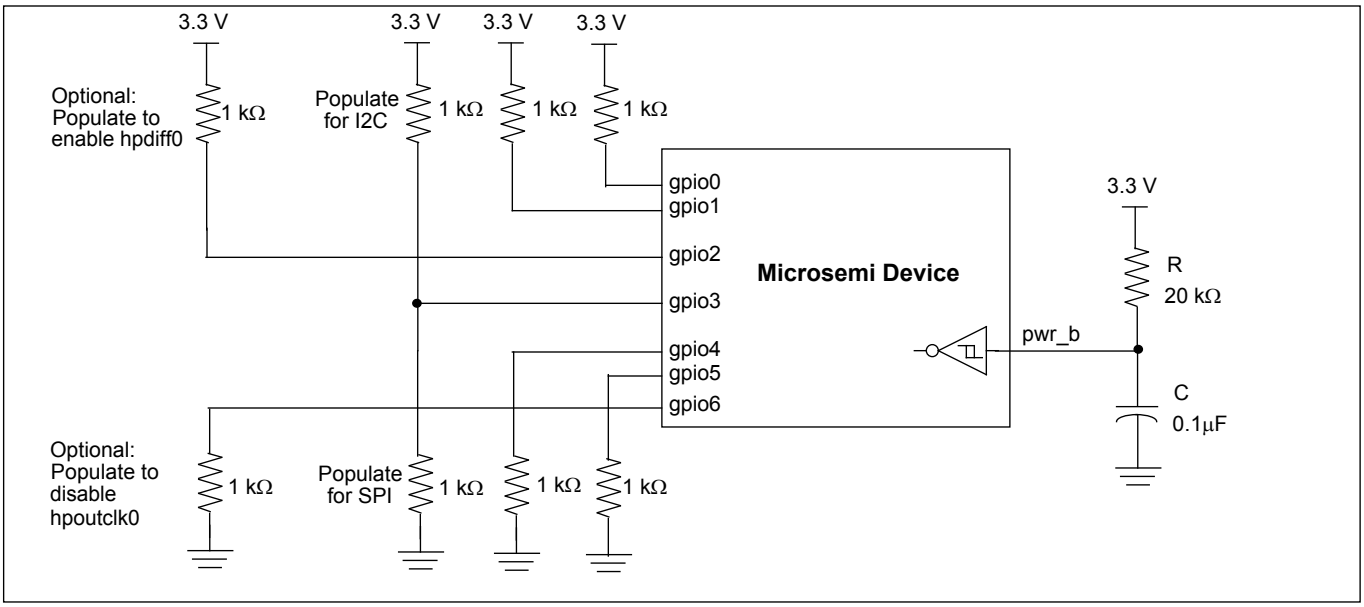


Figure 13 - Typical Power-Up Reset and Configuration Circuit

General purpose pins gpio[0,1,3,4,5] are used to configure device on the power up. They have to be pulled up/down with 1 KΩ resistors as shown in Figure 13 or they can be pulsed low/high during the pwr_b low pulse and kept at the same level for at least 50 ms after pwr_b goes high. After 50 ms they can be released and used as general purpose I/O.

By default all outputs are disabled (except hpoutclk0) to allow user first to program required frequencies for different outputs and then to enable corresponding outputs. If needed, hpoutclk0 can also be disabled on the power up by pulling down gpio6 pin. Hpoutclk0 is programmed by default to generate 125 MHz clock. Similarly, hpdiff0 generates 156.25 MHz clock by default and it can be enabled on the power up by pulling up gpio2 pin as shown in Figure 13. Hpdiff0 and hpdiff1 can be used during the prototype phase to verity if the device is working properly (generates 156.25 MHz and 125 MHz clocks) even before software driver is implemented. Alternatively, this feature can be used to drive an Ethernet Switch with embedded processor that needs 125 MHz or 156.25 MHz as a master clock.

4.13 Ultra Low Jitter Synthesizer Filter Components and Recommended Layout

The APLL for the ultra low jitter synthesizer in the Microsemi device uses external components to help optimize its loop bandwidth. For optimal jitter performance, the following component values are recommended:

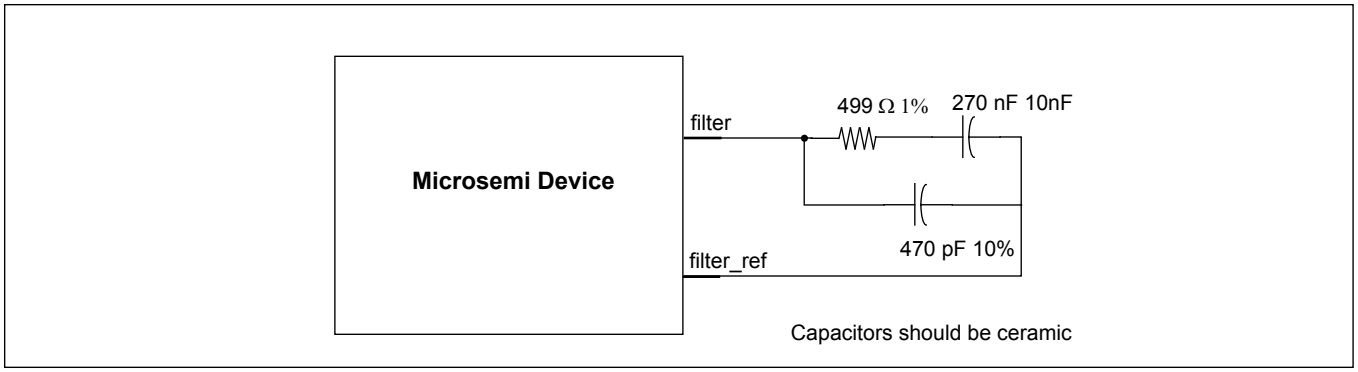


Figure 14 - APLL Filter Component Values

Recommended layout for loop filters is shown in Figure 15:

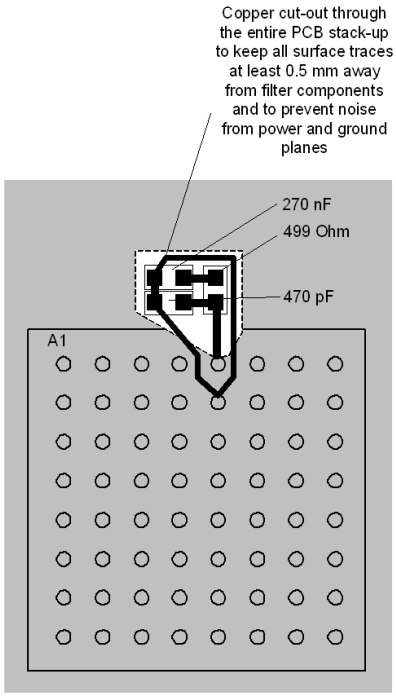


Figure 15 - Recommended layout for Loop Filters

5.0 Configuration and Control

The ZL30158 configuration is composed of 253 x 8 bits. The configuration registers are assigned their values by any of the following three methods:

1) Default configuration
2) Custom OTP (One Time Programmable) configuration
3) SPI/I2C configuration.

5.1 Custom OTP Configuration

At power-up the device sets its configuration registers to the user defined custom configuration values stored in it's OTP (One Time Programmable). Custom configurations can be generated using Microsemi's Clockcenter GUI software (ZLS30CLKCTR). For custom configured devices contact your local Microsemi Field Applications Engineer or Sales Manager.

5.2 GPIO Configuration and Programmability

The device GPIO is mapped by the SPI/I2C programmability. The following is an example of control and status signals that can be supported:

- DPLL lock indicators
- DPLL holdover indicators
- Reference 0 and 1 fail indicators
- Reference select control or monitor
- Differential output clock enable (per output or as a bank of 4 outputs)
- Host Interrupt Output: flags changes of device status prompting the processor to read the enabled interrupt service registers (ISR).
- Output clock stop/start

The following table defines the function of the GPIO pin when configured as a control pin. Configuring the value in bit 6:0 in GPIO configuration registers enables the stated function.

Value	Name	Description
Default		
0x00	default	GPIO pin defined as an input. No function assigned.
Input References		
0x10	Ref0 external LOS signal	Ref0 external Loss Of Signal (LOS) - indicator to DPLLs that Ref0 has failed. Internally in the DPLLs this signal is used for reference monitor indicator, reference switching or holdover entering and for ISR generation.
0x14	Ref1 external LOS signal	Same description as REF0 external LOS
DPLL		
0x20	DPLL Time Interval Error (TIE) clear enable	This signal is OR-ed with the 'DPLL TIE clear enable' bit of the 'DPLL control' register. Functionality of this signal is explained in the 'DPLL control' register.

Value	Name	Description
Synthesizer Post Divider		
0x44	Stop output clock from Synthesizer Post Divider C bit1	This signal is OR-ed with the 'Synthesizer Post Divider C stop clock' bit1 in the 'Synthesizer Post Divider stop clock' register. Functionality of this signal is explained in above mentioned register.
0x45	Stop output clock from Synthesizer Post Divider C bit0	Same description as Stop output clock Synthesizer Post Divider C bit1
0x46	Stop output clock from Synthesizer Post Divider D bit1	Same description as Stop output clock Synthesizer Post Divider C bit1
0x47	Stop output clock from Synthesizer Post Divider D bit0	Same description as Stop output clock Synthesizer Post Divider C bit1
High Performance Differential Outputs		
0x60	Enable Differential output HPDIFF0	This signal is OR-ed with the 'Enable HPDIFF0' bit in the 'High performance differential output enable' register. Functionality of this signal is explained in above mentioned register.
0x62	Enable Differential output HPDIFF1	Same description as Enable Differential output HPDIFF0
0x64	Enable Differential output HPDIFF2	Same description as Enable Differential output HPDIFF0
0x66	Enable Differential output HPDIFF3	Same description as Enable Differential output HPDIFF0
High Performance CMOS Outputs		
0x70	Enable HPOUTCLK0	This signal is OR-ed with the 'Enable HPOUTCLK0' bit in the 'High performance CMOS output enable' register. Functionality of this signal is explained in above mentioned register.
0x72	Enable HPOUTCLK1	Same description as Enable HPOUTCLK0

The following table defines the function of the GPIO pin when configured as a status pin. Configuring the value in bit 6:0 in GPIO configuration registers enables the stated function.

Value	Name	Description
Interrupt		
0x80	Interrupt output signal	This bit will be high if the interrupt has been asserted.
Input References		
0x88	Ref0 - Signal not present in last second	This bit will be high if Ref0 signal was not toggling in the last second.
0x89	Ref0 Single Cycle Measurement (SCM) failure	This bit will be set if Ref0 SCM indicator is active (see 'Ref0 SCM and CFM limits' register for SCM limits).
0x8A	Ref0 Coarse Frequency Measurement (CFM) failure	This bit will be set if Ref0 CFM indicator is active (see 'Ref0 SCM and CFM limits' register for CFM limits).
0x8B	Ref0 Guard Soak Timer (GST) indicator	Ref0 Guard Soak Timer (GST) indicator

Value	Name	Description
0x8C	Ref0 failure indicator	This bit will be set if either Ref0 external LOS signal is high, or Ref0 SCM, CFM or GST indicator is high, and appropriate mask bit in the 'Ref0 and Ref1 failure mask' register is set to 1 (not masked).
0x90	Ref1 - Signal not present in last second	Same description as for Ref0
0x91	Ref1 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0x92	Ref1 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0x93	Ref1 Guard Soak Timer (GST) indicator	Same description as for Ref0
0x94	Ref1 failure indicator	Same description as for Ref0
DPLL Filters		
0xA8	DPLL Normal mode indicator	This bit will be set when the DPLL is in normal locking mode (not holdover, not freerun)
0xA9	DPLL holdover mode indicator	This bit will be set when the DPLL is in holdover mode
0xAB	DPLL used reference	This bit represents the reference selected by the DPLL. 0 = Ref0 1 = Ref1
0xB0	DPLL Lock Indication 1	This bit will be set when DPLL phase error is less than 1 us during 1s period.
0xB1	DPLL Lock Indication 2	This bit will be set when DPLL phase error is less than 10 us during 1s period.
0xB2	DPLL Lock Indication 3	This bit will be set when DPLL phase error is less than 10 us during 10s period.

5.3 Configuration and Field Programmability Registers

This section refers to configuration registers (field programmable) that are set by the user to define device operation.

5.3.1 Input Reference Configuration and Programmability

The following is the set of parameters that are configurable:

- Input reference frequency as multiple of 8 kHz, 25 kHz and 66/64 * 25 kHz
- Default input reference selection
- Reference selection Priority
- Automatic or manual reference switching
- Glitch-less or hit-less reference switching
- Reference switch based on single cycle monitor or coarse frequency monitor or guard soak timer

5.3.2 DPLL Configuration and Programmability

The following is the set of parameters that are configurable:

- DPLL input reference
- DPLL loop bandwidth

5.3.3 Output Multiplexer Configuration and Programmability

The following is the set of parameters that are configurable:

- Output multiplexer configuration
- Start or Stop clock

5.3.4 Synthesis Macro Configuration and Programmability

The following is the set of parameters that are configurable:

- Synthesis Macro locked to DPLL freerun or disabled
- Synthesis Macro mode frequency as multiple of 8 kHz, 25 kHz and 66/64 * 25 kHz

5.3.5 Output Dividers and Skew Management Configuration and Programmability

The following is the set of parameters that are configurable:

- Post divider enable/disable
- Divider ratio
- Output delay value

5.3.6 Output Drivers configuration and Programmability

The following is the set of parameters that are configurable:

- Output driver Enable/Disable

5.4 State Control and Reference Switch Modes

The device has two main control modes of operation: un-managed mode and managed mode.

In un-managed mode of operation, the DPLL state (normal, freerun and holdover) and the selected reference is automatically set by the device internal state machine. It is based on availability of a valid reference and on the reference selection priority.

In managed mode of operation, the DPLL state (normal, freerun and holdover) and the selected reference is manually set by the user.

The device allows for smooth transition from in and out of the two modes of operation. Hence if the DPLL was in managed mode and locked to ref1 reference and it was switched to un-managed mode of operation, then the state machine continues managing the device starting from being locked to the ref1 reference and it will not force reference switching to any other reference unless a change in conditions required such transition.

To facilitate monitoring and managing the device during managed mode of operation, and to facilitate monitoring the device during the un-managed mode, some control and status bits can be muxed into the GPIO pins. The following is a list for such control and monitor bits:

- DPLL state (2 control bits), Normal, holdover and freerun
- DPLL reference selection (2 control and 2 status bits)
- DPLL reference switching mode (1 control bit) (tie_clr_b) hit-less and glitch-less
- Reference monitoring (3 status bits)
- DPLL holdover indication (1 status bit)
- DPLL lock indication (1 status bit)

5.4.1 Un-managed Mode

The un-managed mode combines the functionality of the normal state with automatic holdover and automatic reference switching. In this mode, transitioning from one mode to the other is controlled by the device internal state machine.

The on-chip state machine monitors the device status bits, and based on the status information the state machine makes a decision to force holdover or to perform reference switch.

In the un-managed mode of operation, the device internal state machine manages the device operating states. The reference switching state machine is based on the internal clock monitoring of each of the available input clock sources and the reference priority.

The state machine selects a reference source based on its priority value defined in a control register and the current availability of the reference. If all the references are available, the reference with the highest priority is selected; if this reference fails, the next highest priority reference is selected, and so on.

In un-managed mode, the state machine only reacts to failure indicators and performs reference switching if either one of the following conditions takes place and they are not masked with their corresponding mask bits as follows:

- LOS detected a failure and RefSwMask<0> is at logic “1”
- SCM detected a failure and RefSwMask<1> is at logic “1”
- CFM detected a failure and RefSwMask<2> is at logic “1”
- The Guard Soak Time is triggered and RefSwMask<3> is at logic “1”

The default conditions is RefSwMask<3:0> “1000”.

In un-managed mode of operation, the state machine only reacts to failure indicators and goes into auto-holdover under one of the following conditions if they are not masked with their corresponding mask bits:

- LOS detected a failure and HOMask<0> is at logic “1”
- SCM detected a failure and HOMask<1> is at logic “1”
- CFM detected a failure and HOMask<2> is at logic “1”
- The Guard Soak Time is triggered and HOMask<3> is at logic “1”
- Reference switch condition exist, and no reference is available

The default conditions is HOMask<3:0> is “0111”.

In un-managed mode of operation, the state machine automatically recovers from auto-holdover when the conditions to enter auto-holdover are not present.

In un-managed mode, the device automatically selects a valid reference input. If the current reference used for synchronization fails, the state machine switches to the other available reference. If all the available references fail, then the device enters the Holdover mode without switching to another reference. The selection is based on reference priority. Active reference is shown by reference selection status bits.

Reference Priority

Every reference has 3 bits in a control register associated with its priority value (0 to 3) to allow system designers to program the priority of the input references. The priorities are relative to each other, with lower value numbers being the higher priority. value “111" disables the ability to select the reference (i.e., mark reference: don’t use for synchronization). If two inputs are given the same priority number, the input is selected based on the reference naming convention (i.e., ref0 is higher priority than ref1). The default reference selection priority is based on reference number (i.e., ref0 is highest priority and ref1 is the lowest priority).

When two references have the same priority they will not revert to each other (as reference availability change) but they will revert to a reference with a higher priority when it is available.

5.4.2 Managed Mode

The managed mode combines the functionality of the Holdover, Freerun and Normal states with automatic Holdover, and manual reference switching through bits in the control registers. In this mode, transitioning from one state to the other is controlled by an external controller.

The external controller monitors the device status bits. Based on the status information, the external controller makes a decision to force holdover or to perform reference switch. In managed mode of reference selection, the active reference input is selected based on reference selection control bits. If the external controller sets the device to lock to a failed reference, the device stays in auto-holdover and only switches to that reference if it becomes valid.

The state machine only reacts to failure indicators and goes into auto-holdover under one of the following conditions if they are not masked with their corresponding mask bits:

- LOS detected a failure and HOMask<0> is at logic “1”
- SCM detected a failure and HOMask<1> is at logic “1”
- CFM detected a failure and HOMask<2> is at logic “1”
- The Guard Soak Time is triggered and HOMask<3> is at logic “1”

The default conditions HOMask<3:0> is “0111”.

The state machine automatically recovers from auto-holdover when the conditions to enter auto-holdover are not present.

Time critical state transitions for entry into auto-holdover and exit from auto-holdover are managed by the internal state machine. Such transition into and out of the auto-holdover state will not allow for change of reference, unless forced by reference selection control bits. A change on the reference select bits triggers an internal state transition into auto-holdover and then exit into Normal state and locking to the new reference.

6.0 Host Interface

A host processor controls and receives status from the Microsemi device using either a SPI or an I^2C interface. The type of interface is selected using the startup state of the GPIO pins.

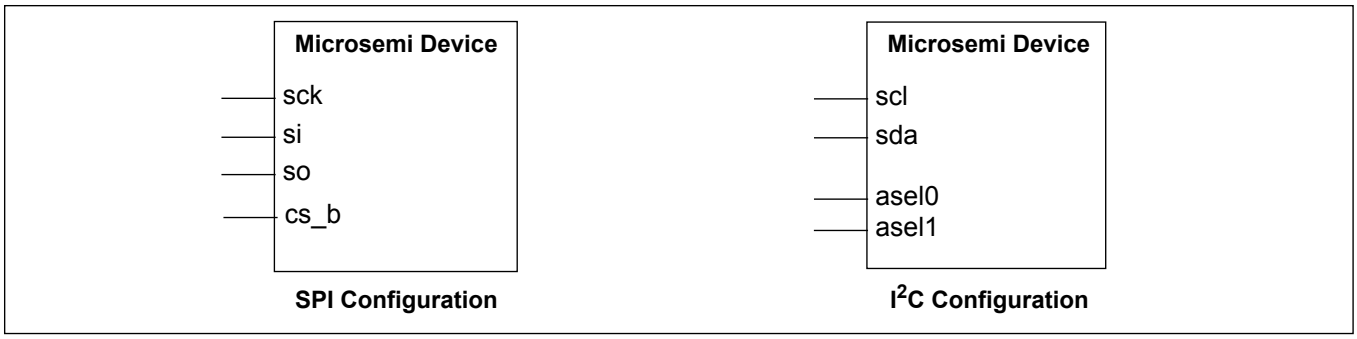


Figure 16 - Serial Interface Configuration

The selection between I2C and SPI interfaces is performed at start-up using GPIO[3] pin, right after pwr_b gets de-asserted. The GPIO pin need to be held at their appropriate value for 50 ms after the de-assertion of pwr_b, after which time they can be released and used as any other GPIO.

Both interfaces use seven bit address field and the device has eight bit address space. Hence, memory is divided in two pages. Page 0 with addresses 0x00 to 0x7E and Page 2 with addresses 0x80 to 0xFF. Writing 0x01 to Page Register at address 0x7F, toggles SPI/I2C accesses between Page 0 and Page 1.

GPIO[3]	Serial Interface
0	SPI
1	I2C

Table 5 - Serial Interface Selection

6.1 Serial Peripheral Interface

The serial peripheral interface (SPI) allows read/write access to the registers that are used to configure, read status, and allow manual control of the device.

This interface supports two modes of access: Most Significant Bit (MSB) first transmission or Least Significant Bit (LSB) first transmission. The mode is automatically selected based on the state of **sck**_scl pin when the **cs_b**_asel0 pin is active. If the **sck**_scl pin is low during **cs_b**_asel0 activation, then MSB first timing is selected. If the **sck**_scl pin is high during **cs_b**_asel0 activation, then LSB first timing is assumed.

The SPI port expects 7-bit addressing and 8-bit data transmission, and is reset when the chip select pin **cs_b**_asel0 is high. During SPI access, the **cs_b**_asel0 pin must be held low until the operation is complete. The first bit transmitted during the address phase of a transfer indicates whether a read (1) or a write (0) is being performed. Burst read/write mode is also supported by leaving the chip select signal **cs_b**_asel0 is low after a read or a write. The address will be automatically incremented after each data byte is read or written.

The serial peripheral interface supports half-duplex processor mode which means that during a write cycle to the device, output data from the **so**_asel1 pin must be ignored. Similarly, the input data on the **si**_sda pin is ignored by the device during a read cycle.

Functional waveforms for the LSB and MSB first mode, and burst mode are shown in Figure 17, Figure 18 and Figure 18. Timing characteristics are shown in Table 7, Figure 30 and Figure 31.

6.1.1 Least Significant Bit (LSB) First Transmission Mode

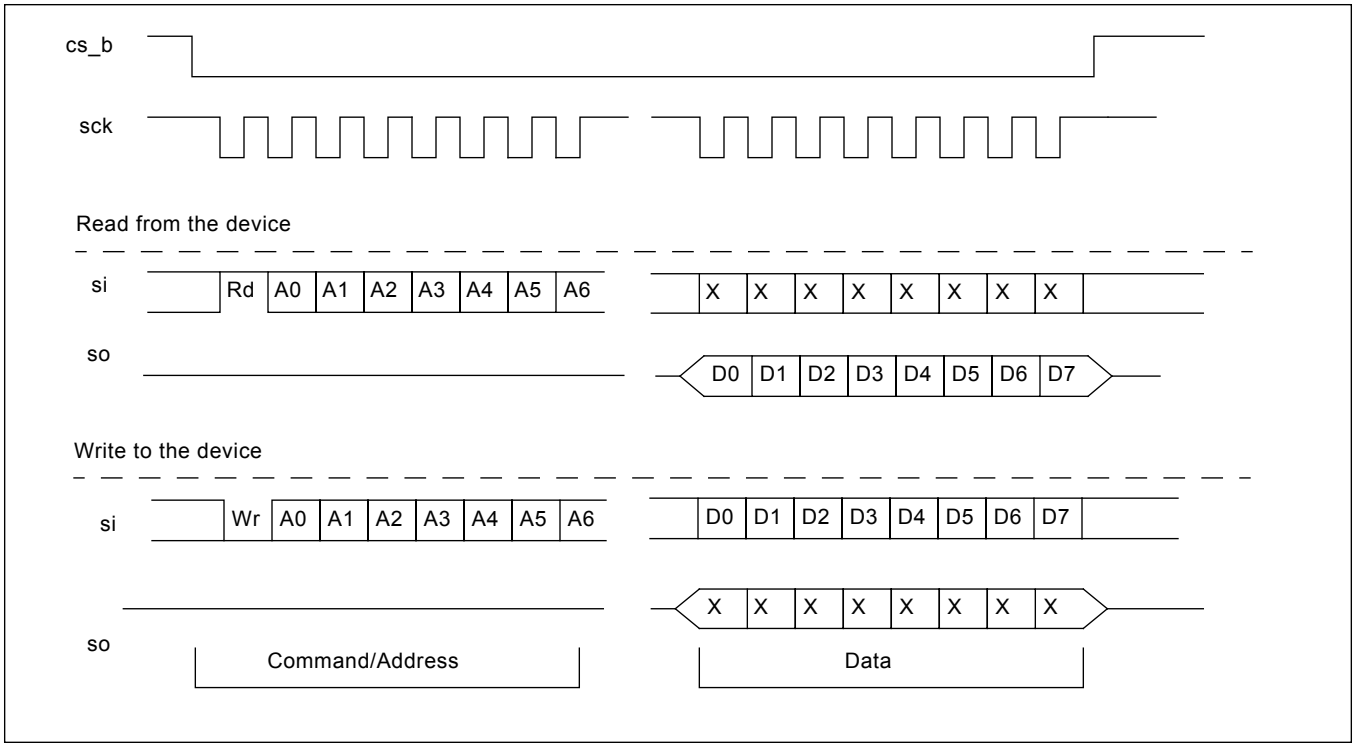


Figure 17 - Serial Peripheral Interface Functional Waveforms - LSB First Mode

6.1.2 Most Significant Bit (MSB) First Transmission Mode

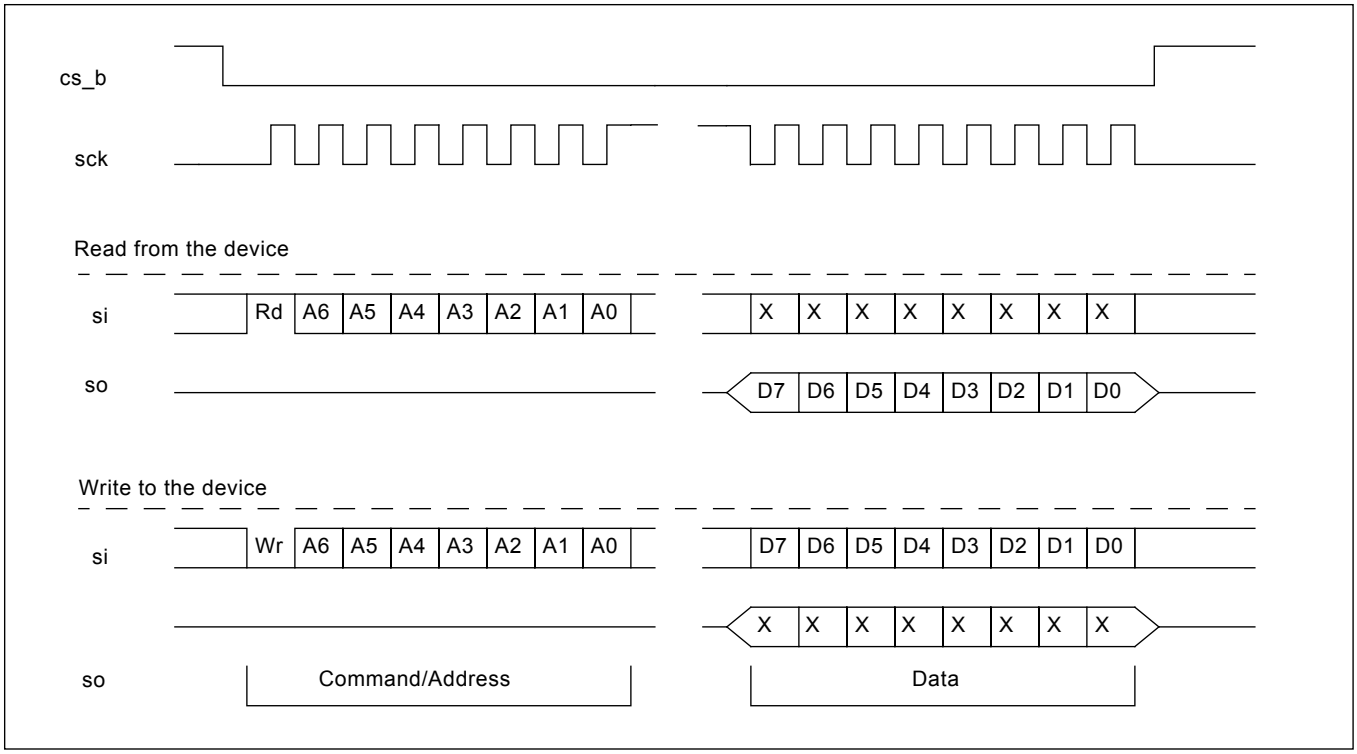


Figure 18 - Serial Peripheral Interface Functional Waveforms - MSB First Mode

6.1.3 SPI Burst Mode Operation

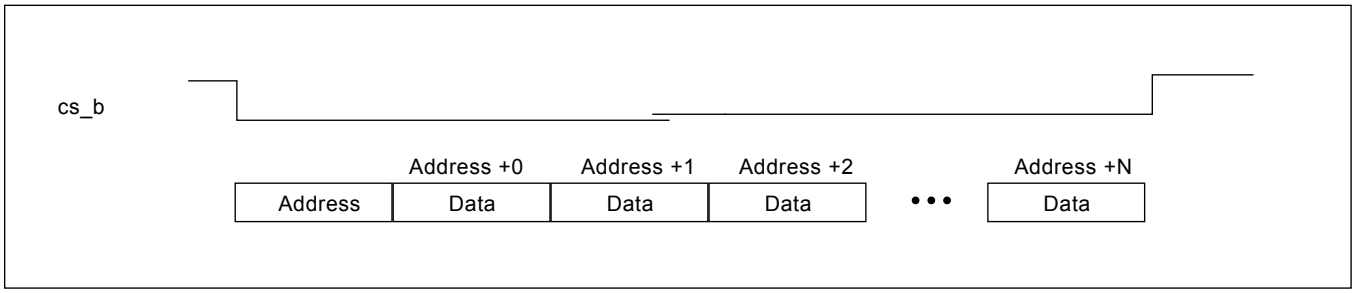


Figure 19 - Example of a Burst Mode Operation

6.1.4 I²C Interface

The I²C controller supports version 2.1 (January 2000) of the Philips I²C bus specification. The port operates in slave mode with 7-bit addressing, and can operate in Standard (100 kbits/s) and Fast (400 kbits/s) mode. Burst mode is supported in both standard and fast modes.

Data is transferred MSB first and occurs in 1 byte blocks. As shown in Figure 20, a **write** command consists of a 7-bit device (slave) address, a 7-bit register address (0x00 - 0x7F), and 8-bits of data.

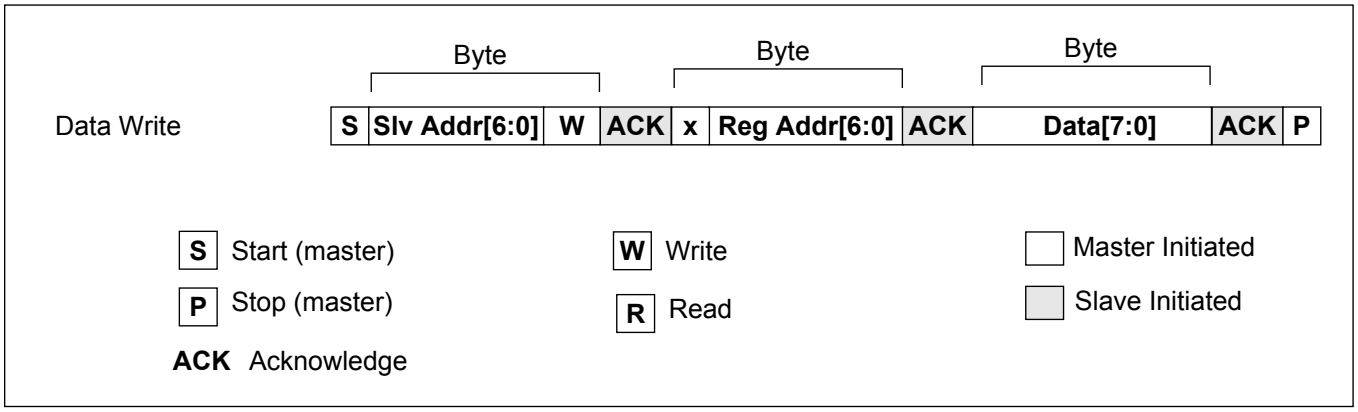


Figure 20 - I²C Data Write Protocol

A **read** is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. This is shown in Figure 21.

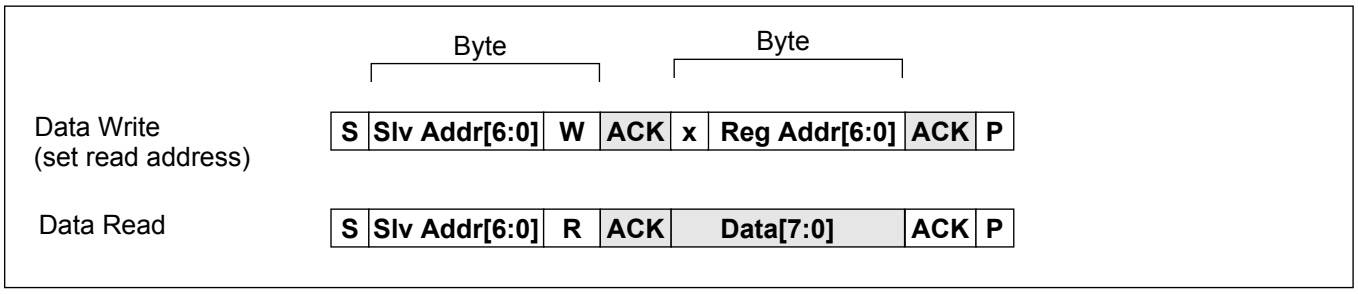


Figure 21 - I²C Data Read Protocol

The **7-bit device (slave) address** contains a 5-bit fixed address plus variable bits which are set with the **asel0,** and **asel1** pins. This allows multiple ZL30158s to share the same I²C bus. The address configuration is shown in Figure 22.

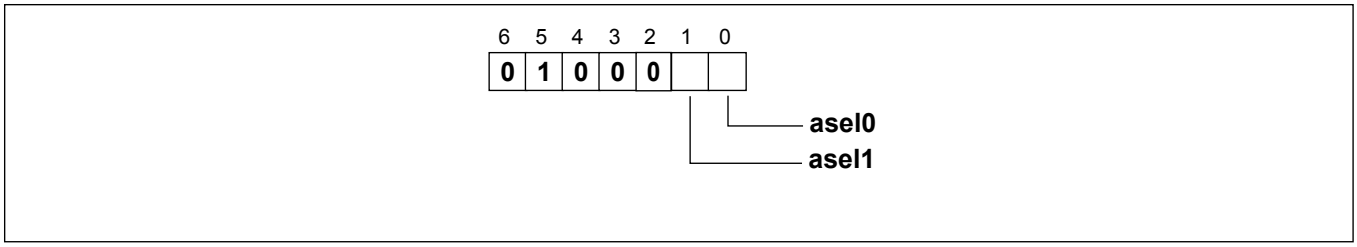


Figure 22 - I²C 7-bit Slave Address

The device also supports burst mode which allows multiple data write or read operations with a single specified address. This is shown in Figure 23 (write) and Figure 24 (read). The first data byte is written/read from the specified address, and subsequent data bytes are written/read using an automatically increment address. The maximum auto increment address of a burst operation is 0x7F. Any operations beyond this limit will be ignored. In other words, the auto increment address does not wrap around to 0x00 after reaching 0x7F.

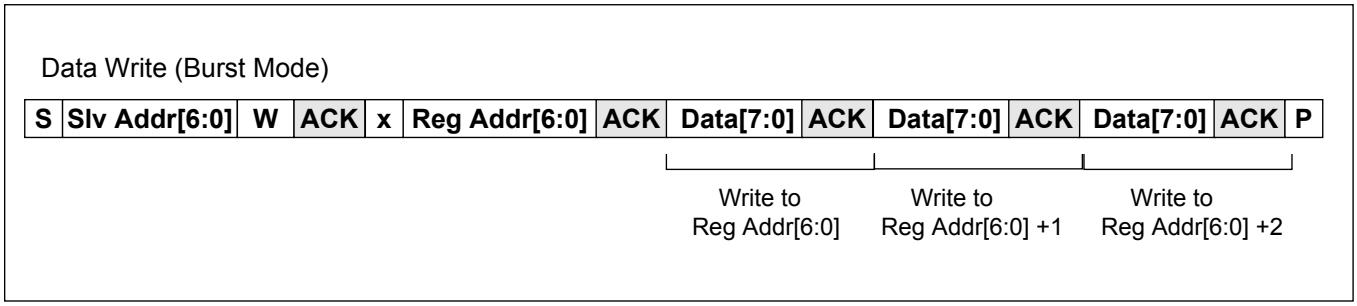


Figure 23 - I²C Data Write Burst Mode

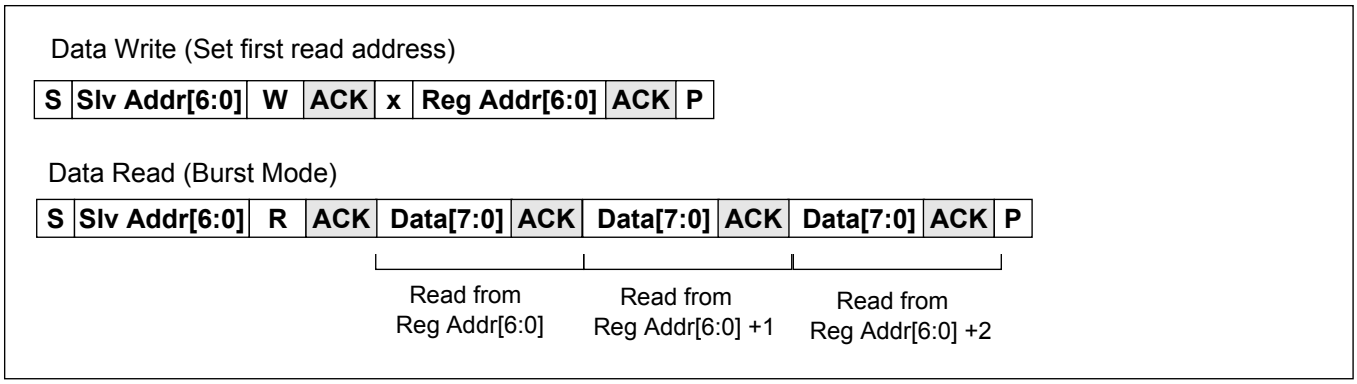


Figure 24 - I²C Data Read Burst Mode

7.0 Register Map

The device is mainly controlled by accessing software registers through the serial interface (SPI or I^2C). The device can be configured to operate in a highly automated manner which minimizes its interaction with the system's processor, or it can operate in a manual mode where the system processor controls most of the operation of the device.

The simplest way to generate appropriate configuration for the device is to use the evaluation board GUI which can operate standalone (without the board). With GUI user can quickly set all required parameters and save the configuration to a text file.

Multi-byte Register Values

The device register map is based on 8-bit register access, so register values that require more than 8 bits must be spread out over multiple registers and accessed in 8-bit segments. When accessing multi-byte register values, it is important that the registers are accessed in the proper order—they must follow big endian addressing scheme. The 8-bit register containing the most significant byte (MSB) must be accessed first, and the register containing the least significant byte (LSB) must be accessed last. An example of a multi-byte register is shown in Figure 25. When writing a multi-byte value, the value is latched when the LSB is written.

Example:
The programmable input reference M and N 16 bit values defining the M/N ratio is programmed using a 32-bit value which is spread over four 8-bit registers. The MSB is contained in address 0x14 and the LSB in 0x17. When reading or writing this multi-byte value, the MSB must be accessed first, followed by the middle bytes, and the LSB last.

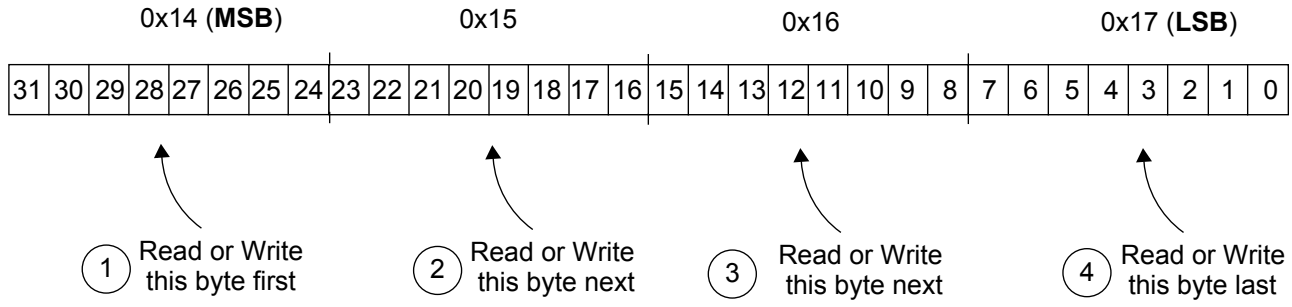


Figure 25 - Accessing Multi-byte Register Values

To assist in device setup, a configuration GUI is provided. The configuration GUI can directly configure the device evaluation board, but it also functions as a tool to provide details on how to configure different device registers.

Procedure for writing registers

The procedure for updating the control registers in the ZL30158 is as follows:

-write 0x01 to Sticky_R_Lock Register at address 0x0D

-write to one or more ZL30158 control register(s)

-write 0x00 to Sticky_R_Lock Register at address 0x0D

When changing the dpll_mode bits[1:0] in the dpll_mode_refsel registers (0x33) from ’11’ (automatic mode) to ’10’ (forced reference lock mode), the following procedure should be followed:

-write 0x01 to Sticky_R_Lock Register at address 0x0D

-write to one or more ZL30158 control register(s)*

-wait 7ms

-write 0x00 to Sticky_R_Lock Register at address 0x0D

* includes changing the dpll_mode bits[1:0] (from '11' to '10') in the DPLL_mode_refsel registers.

Time between two write accesses to the same register

User should wait at least 7 ms between two write accesses to the same register. For page register at address 0x7F, and Sticky_r_lock register at address 0x0D there is no wait time required between two write accesses.

Reading from Sticky Read (StickyR) Registers

Access to some status registers is defined as Sticky Read (StickyR). Procedure for accessing these registers is:

-write 0x01 to StickyR Lock Register at address 0x0D

-clear status register(s) by writing 0x00 to it

-write 0x00 to StickyR Lock Register at address 0x0D

-wait for 7 ms

-read the status register(s)

The following table provides a summary of the registers available for status updates and configuration of the device. Devices with a custom OTP configuration will power-up with the custom configuration values instead of the default values

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
Miscellaneous Registers				
0x00	id_reg	See Description	Chip ID and version identification. User should not write to this register. If this register is written to, the default value will be temporarily overwritten until the next reset. The temporary change of the default value will not affect the performance of the device.	R/W
Interrupts and Reference Monitor				
0x02	ref_fail_isr_status	0x00	Reference failure status register	StickyR
0x03	dpll_isr_status	0x00	DPLL status register for DPLL	StickyR
0x04	ref_fail_isr_mask	0x00	Reference failure interrupt service register mask	R/W
0x05	dpll_isr_mask	0x00	DPLL interrupt service register mask	R/W
0x07	ref_mon_fail_1_0	0x00	Ref1 and Ref0 failure indications	StickyR
0x09	ref_mon_fail_mask_1_0	0x66	Control register to mask each failure indicator for Ref1 and Ref0	R/W
0x0A	ref_config	0x10	Configures input references to be differential or single-ended	R/W
0x0B	gst_disqualif_time	0xAA	Control register for the guard soak timer disqualification time for the references	R/W
0x0C	gst_qualif_time	0x55	Control register for the guard soak timer qualification time for the references	R/W
0x0D	sticky_r_lock	0x00	Used to lock StickyR Status Registers from being updated by internal device logic	R/W
Input Frequency Configuration				
0x10:0x11	ref0_base_freq	0x61A8	Ref0 base frequency in Hz (16 bits, unsigned integer)	R/W
0x12: 0x13	ref0_freq_multiple	0x03E8	Ref0 frequency as a multiple of the base frequency (16 bits, unsigned integer)	R/W

Table 6 - Register Map

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x14:0x17	ref0_ratio_M_N	0x00010001	Ref0 Mr and Nr values, used for multiplication ratio Mr/Nr (2 x 16 bits unsigned integers)	R/W
0x18:0x19	ref1_base_freq	0x61A8	Ref1 base frequency in Hz (16 bits, unsigned integer)	R/W
0x1A: 0x1B	ref1_freq_multiple	0x1388	Ref1 frequency as a multiple of the base frequency (16 bits, unsigned integer)	R/W
0x1C:0x1F	ref1_ratio_M_N	0x00010001	Ref1 Mr and Nr values, used for multiplication ratio Mr/Nr (2 x 16 bits unsigned integers)	R/W
DPLL Configuration, State Machine Control and Monitor				
0x30	dpll_ctrl	0x0D	DPLL control register	R/W
0x32	dpll_ref_priority1_0	0x10	DPLL reference 1 and 0 selection priority	R/W
0x33	dpll_mode_refsel	0x03	DPLL reference selection control or reference selection status	R/W
0x34	dpll_ref_fail_mask	0x87	Control register to mask each failure indicator (SCM, CFM and GST) used for automatic reference switching and automatic holdover	R/W
0x44	dpll_hold_lock_fail	0x00	DPLL lock and holdover status	StickyR
0x45	ex_fb_ctrl	0x00	External feedback control	R/W
0x46	reduced_diff_out_pwr	0x00	Enables reduced power on high performance differential outputs	R/W
Input Reference Monitoring Registers				
0x47	phase_mem_limit_ref0	0x02	Reference 0 phase memory limit	R/W
0x48	phase_mem_limit_ref1	0x02	Reference 1 phase memory limit	R/W
0x4B	scm_cfm_limit_ref0	0x55	Reference 0 single cycle monitor (SCM) and coarse frequency monitor (CFM) limits	R/W
0x4C	scm_cfm_limit_ref1	0x55	Reference 1 single cycle monitor (SCM) and coarse frequency monitor (CFM) limits	R/W
0x4F	dpll_config	0x31	Enables DPLL	R/W
Output Synthesizer Configuration Registers				
0x50:0x51	synth_base_freq	0x61A8	Synthesizer base frequency	R/W

Table 6 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x52:0x53	synth_freq_multiple	0x0C35	Synthesizer base frequency multiplication number	R/W
0x54:0x57	synth_ratio_M_N	0x00010001	Specifies numerator Ms and denominator Ns for synthesizer multiplication ratio Ms/Ns	R/W
0x71	output_synthesizer_en	0x01	Output synthesizer enable	R/W
0x72	dpll_lock_selection	0xAA	DPLL lock selection	R/W
0x73:0x76	central_freq_offset	0x046AAAAB	Central frequency offset to compensate for oscillator inaccuracy	R/W
0x77	synth_filter_sel	0x00	Synthesizer selection between internal and external filter	R/W
0x78	synth_fine_phase_shift	0x00	Synthesizer fine phase shift	R/W
0x7F	page_register	0x00	Selects between pages 0 and 1	R/W
0x80:0x82	synth_post_div_A	0x000008	Synthesizer post divider A	R/W
0x83:0x85	synth_post_div_B	0x00000A	Synthesizer post divider B	R/W
0x86:0x88	synth_post_div_C	0x00000A	Synthesizer post divider C	R/W
0x89:0x8B	synth_post_div_D	0x000032	Synthesizer post divider D	R/W
Output Reference Selection and Output Driver Control				
0xB0	hp_diff_en	0x00	High Performance differential output enable	R/W
0xB1	hp_cmos_en	0x00	Enables High Performance CMOS outputs hpoutclk[1:0]	R/W
0xB8	synth_stop_clk	0x00	Stops output clocks at either high or low logical level	R/W
0xB9	syn_fail_flag_status	0x00	Indicates Synthesizers loss of lock	StickyR
0xBA	clear_sync_fail_flag	0x00	Clears Synthesizers fail flag in register 0xB9	R/W

Table 6 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0xBF:0xC0	phase_shift_s_postdiv_C	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer, Post Divider C.	R/W
0xC1:0xC2	phase_shift_s_postdiv_D	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer, Post Divider D.	R/W
0XC3	xo_or_crystal_sel	0x00	Disables OSCo driver.	R/W
0xC6	Chip_revision_2	0x03	Chip revision identification	R/W
0xE0	gpio_function_pin0	0x00	GPIO0 control or status select	R/W
0xE1	gpio_function_pin1	0x00	GPIO1 control or status select	R/W
0xE2	gpio_function_pin2	0x60	GPIO2 control or status select	R/W
0xE3	gpio_function_pin3	0x00	GPIO3control or status select	R/W
0xE4	gpio_function_pin4	0x00	GPIO4 control or status select	R/W
0xE5	gpio_function_pin5	0x00	GPIO5 control or status select	R/W
0xE6	gpio_function_pin6	0x70	GPIO6 control or status select	R/W
0xF7	spurs_suppression	0x00	Used for spurs suppression	R/W

Table 6 - Register Map (continued)

8.0 Detailed Register Map

Register_Address: **0x00**
Register Name: **id_reg**
Default Value: **See Description**
Type: **R/W**

Bit Field	Function Name	Description
4:0	chip_id	Chip Identification = 0b01000
6:5	chip_revision	Chip revision number = 0b00 (full chip revision = chip_revision_2 bits in register 0xC6 and chip_revision bits[6:5] in register 0x00)
7	ready_indication	After reset this bit goes high when device is ready. This signals that user can start to program/configure the device. It can take up to 50 ms for this bit to go high after the reset.This bit should not be polled until 40ms after reset

Register_Address: **0x02**
Register Name: **ref_fail_isr_status**
Default Value: **0x00**
Type: StickyR

Bit Field	Function Name	Description
0	ref0_fail	This bit is set to 1 when ref0 has a failure. The device will set this bit to high when ref0_fail_mask bit of the ref_fail_isr_mask register at address 0x04 is high and conditions for ref0 failure are satisfied. When this bit is set to high, it also sets IRQ line to high.
1	ref1_fail	Same description as for ref0
7:2	reserved	Leave as default

Register_Address: **0x03**
Register Name: **dpll_isr_status**
Default Value: **0x00**
Type: StickyR

Bit Field	Function Name	Description
0	dpll_holdover	The device will set this bit to high when dpll_holdover_mask bit of the dpll_interrupt_mask register at address 0x05 is high and DPLL went into holdover mode. When this bit is set to high, it also sets IRQ line to high.
1	dpll_loss_of_lock	The device will set this bit to high when 'dpll_loss_of_lock_mask bit of the dpll_interrupt_mask register at address 0x05 is high and DPLL has lost lock. When this bit is set to high, it also sets IRQ line to high.
7:2	reserved	Leave as default

Register_Address: **0x04**
Register Name: **ref_fail_isr_mask**
Default Value: **0x00**
Type: R/W

Bit Field	Function Name	Description
0	ref0_fail_isr_mask	Reference 0 failure interrupt generation mask. When set to zero disables interrupt generation and appearance in the Reference Status ISR register.
1	ref1_fail_isr_mask	Same description as above but for ref1.
7:2	reserved	Leave as default

Register_Address: **0x05**
Register Name: **dpll_isr_mask**
Default Value: **0x00**
Type: R/W

Bit Field	Function Name	Description
0	dpll_holdover_mask	DPLL holdover indication mask. When set to zero disables interrupt generation and appearance in the DPLL Status ISR register.

Register_Address: **0x05**
Register Name: **dpll_isr_mask**
Default Value: **0x00**
Type: R/W

Bit Field	Function Name	Description
1	dpll_loss_of_lock_mask	DPLL loss of lock indication mask. When set to zero disables interrupt generation and appearance in the DPLL Status ISR register.
7:2	reserved	Leave as default.

Register_Address: **0x07**
Register Name: **ref_mon_fail_1_0**
Default Value: **0x00**
Type: SticlyR

Bit Field	Function Name	Description
0	ref0_fail_los	Reference 0 Loss Of Signal (LOS) indicator. The device will set this bit to high when external Ref 0 LOS signal (typically from PHY device), applied to selected GPIO, goes high. The Ref0 LOS signal indicator can be associated with any of available GPIOs pins through the 'GPIO function' registers. **Note:** this bit is not maskable.
1	ref0_fail_scm	Reference 0 Single Cycle Monitor (SCM) indicator. This bit is set high whenever Single Cycle Failure on Reference 0 occurs. **Note:** this bit is not maskable.
2	ref0_fail_cfm	Reference 0 coarse frequency monitoring (SCM) indicator. This bit is set high whenever coarse frequency monitoring failure on Reference 0 occurs. **Note:** this bit is not maskable.
3	ref0_fail_gst	Guard Soak Timer (GST) failure indicator on Reference 0. This bit is set high whenever Reference 0 guard soak timer expires. **Note:** this bit is not maskable.
4	ref1_fail_los	Same description as above but for ref1.
5	ref1_fail_scm	Same description as above but for ref1.
6	ref1_fail_cfm	Same description as above but for ref1.
7	ref1_fail_gst	Same description as above but for ref1.

Register_Address: **0x09**
Register Name: **ref_mon_fail_mask_1_0**
Default Value: **0x66**
Type: R/W

Bit Field	Function Name	Description
3:0	ref0_fail_mask	Masks failure indicators (LOS,SCM, CFM, and GST) for reference 0. bit 0: LOS (Loss of Clock) bit 1: SMC (Single Cycle Monitor) bit 2: CFM (Coarse Frequency Monitor) bit 3: GST (Guard Soak Timer) 0: failure bit is masked (disabled) 1: failure bit is un-masked (enabled) Note: When set low these bits will mask corresponding Reference 0 failure indicators in Reference Failure Interrupt Status Register at address 0x02. They will not affect bits in Reference Monitoring Failure Mask Register at address 0x07 because bits in Reference Monitoring Failure Mask Register are not maskable.
7:4	ref1_fail_mask	Same description as above but for ref1.

Register_Address: **0x0A**
Register Name: **ref_config**
Default Value: **0x00**
Type: R/W

Bit Field	Function Name	Description
0	ref0_pre-divider_enable	When set high, the Reference 0 input clock will be divided by 2 prior to being fed to DPLL. All registers, which require frequency of the Reference 0 will have to be programmed with half of Reference 0 frequency. When set low, the Reference 0 is fed directly to DPLL.
1	ref1_pre-divider_enable	Same description as above but for ref1
3:2	reserved	Leave as default
4	ref0_diff_input_enable	When set high, the device expects differential clock at Ref 0 input pins (Ref0_P and Ref0_N). When set low, the device expects single-ended clock at Ref0_P input pin, and Ref0_N input should be connected to ground.

Register_Address: **0x0A**
Register Name: **ref_config**
Default Value: **0x00**
Type: R/W

Bit Field	Function Name	Description
5	ref1_diff_input_enable	Same description as above but for ref1
7:6	reserved	Leave as default

Register_Address: **0x0B**
Register Name: **gst_disqualif_time**
Default Value: **0xAA**
Type: R/W

Bit Field	Function Name	Description
1:0	ref0_gst_disqualif_timer	Selects time to disqualify input reference after detection of either the Ref 0 CFM or Ref 0 SCM indicators. 00: minimum delay 01: 10 ms 10: 50 ms (default) 11: 2.5 s
3:2	ref1_gst_disqualif_timer	Same description as above but for ref1
7:4	reserved	Leave as default

Register_Address: **0x0C**
Register Name: **gst_qualif_time**
Default Value: **0x55**
Type: R/W

Bit Field	Function Name	Description
1:0	ref0_gst_qualif_timer	Selects time to qualify input reference after deassertion of both the Ref 0 CFM and Ref 0 SCM indicators. 00: 2 x selected Ref0 GST disqualify time 01: 4 x selected Ref0 GST disqualify time (default) 10: 6 x selected Ref0 GST disqualify time 11: 8 x selected Ref0 GST disqualify time
3:2	ref1_gst_qualif_timer	Same description as above but for ref1

Register_Address: **0x0C**
Register Name: **gst_qualif_time**
Default Value: **0x55**
Type: R/W

Bit Field	Function Name	Description
7:4	reserved	Leave as default

Register_Address: **0x0D**
Register Name: **sticky_r_lock**
Default Value: **0x00**
Type: R/W

Bit Field	Function Name	Description
7:0	sticky_r_lock	This register is used when accessing StickyR status registers. Writing 0x01 to this register locks the status register from being updated by internal logic. Writing 0x00 to this register enables internal updates of StickyR status registers Please refer to **Reading from Sticky Read (StickyR) registers and Procedure for writing registers** procedure at the beginning of 7.0, “Register Map“ section.

Register_Address: **0x10:0x11**
Register Name: **ref0_base_freq**
Default Value: **0x61A8**
Type: R/W

Bit Field	Function Name	Description
15:0	ref0_base_freq	Unsigned binary value of these bits represents Ref0 base frequency Br in Hz. The Br has to be set to one of the following three values (otherwise 0x1F40 will be used instead): 0x1F40 for 8 kHz, 0x3E80 for 16 kHz, 0x61A8 for 25 kHz **Note:** in order to write 16 bit value to this register (and any other register that is bigger than 8 bits), the most significant byte has to be written to the lower address and least significant byte has to be written to the higher address. Hence, memory mapping follows big endian.

Register_Address: **0x12:0x13**
Register Name: **ref0_freq_multiple**
Default Value: **0x03E8**
Type: R/W

Bit Field	Function Name	Description
15:0	ref0_freq_multiple	Unsigned binary value of these bits represents Ref0 base frequency multiplication number. 'Base frequency' number Br multiplied by the 'Base frequency multiple' number Kr has to equal the reference frequency in Hz. Examples of some references frequencies and appropriate values that can be programmed for Br and Kr to match that reference frequency: Reference frequency — Base frequency Br — Base frequency multiple Kr 2.048 MHz — 8 kHz (0x1F40) — 256 (0x0100) 1.544 MHz — 8 kHz (0x1F40) — 193 (0x00C1) 19.44 MHz — 8 kHz (0x1F40) — 2430 (0x097E) 622.08 MHz — 16 kHz (0x3E80) — 38880 (0x97E0) 156.25 MHz — 25 kHz (0x61A8) — 6250 (0x186A) 25 MHz — 25 HHz (0x61A8) — 1000 (0x03E8)

Register_Address: **0x14:0x17**
Register Name: **ref0_ratio_M_N**
Default Value: **0x00010001**
Type: R/W

Bit Field	Function Name	Description
15:0	ref0_FEC_denom_Nr	Unsigned binary value of Mr bits, in combination with unsigned binary value of Nr bits represents Ref0 FEC multiplication ratio. For FEC reference frequencies, the 'Base frequency' number Br multiplied by the 'Base frequency multiple' number Kr, multiplied by Mr and divided by Nr has to equal the reference frequency in Hz; Ref_freq [Hz] = Br x Kr x Mr / Nr Mr and Nr are limited to: 1) Mr = 66 and Nr = 64. These values for Mr and Nr are allowed only when Br and Kr are programmed to Br = 25000 and Kr = 6250. 2) Mr = 1 and Nr = 1 for all other cases (default values)
31:16	ref0_FEC_numer_Mr	

Register_Address: **0x18:0x19**
Register Name: **ref1_base_freq**
Default Value: **0x61A8**
Type: R/W

Bit Field	Function Name	Description
15:0	ref1_base_freq	Unsigned binary value of these bits represents Ref1 base frequency Br in Hz. The Br has to be set to one of the following three values (otherwise 0x1F40 will be used instead): 0x1F40 for 8 kHz, 0x3E80 for 16 kHz, 0x61A8 for 25 kHz **Note:** in order to write 16 bit value to this register (and any other register that is bigger than 8 bits), the most significant byte has to be written to the lower address and least significant byte has to be written to the higher address. Hence, memory mapping follows big endian.

Register_Address: **0x1A:0x1B**
Register Name: **ref1_freq_multiple**
Default Value: **0x13E8**
Type: R/W

Bit Field	Function Name	Description
15:0	ref1_freq_multiple	Unsigned binary value of these bits represents Ref1 base frequency multiplication number. 'Base frequency' number Br multiplied by the 'Base frequency multiple' number Kr has to equal the reference frequency in Hz. Examples of some references frequencies and appropriate values that can be programmed for Br and Kr to match that reference frequency: Reference frequency — Base frequency Br — Base frequency multiple Kr 2.048 MHz — 8 kHz (0x1F40) — 256 (0x0100) 1.544 MHz — 8 kHz (0x1F40) — 193 (0x00C1) 19.44 MHz — 8 kHz (0x1F40) — 2430 (0x097E) 622.08 MHz — 16 kHz (0x3E80) — 38880 (0x97E0) 156.25 MHz — 25 kHz (0x61A8) — 6250 (0x186A) 25 MHz — 25 HHz (0x61A8) — 1000 (0x03E8)

Register_Address: **0x1C:0x1F**
Register Name: **ref1_ratio_M_N**
Default Value: **0x00010001**
Type: R/W

Bit Field	Function Name	Description
15:0	ref1_FEC_denom_Nr	Unsigned binary value of Mr bits, in combination with unsigned binary value of Nr bits represents Ref0 FEC multiplication ratio. For FEC reference frequencies, the 'Base frequency' number Br multiplied by the 'Base frequency multiple' number Kr, multiplied by Mr and divided by Nr has to equal the reference frequency in Hz; Ref_freq [Hz] = Br x Kr x Mr / Nr Mr and Nr are limited to: 1) Mr = 66 and Nr = 64. These values for Mr and Nr are allowed only when Br and Kr are programmed to Br = 25000 and Kr = 6250. 2) Mr = 1 and Nr = 1 for all other cases (default values)
31:16	ref1_FEC_numer_Mr	

Register_Address: **0x30**
Register Name: **dpll_ctrl**
Default Value: **0x0D**
Type: R/W

Bit Field	Function Name	Description
1:0	dpll_pull_in_hold_in	Selects pull-in and hold-in range for DPLL. 00: +/- 52 ppm 01: +/- 130 ppm 10: +/- 400 ppm 11: +/- 3900 ppm
3:2	dpll_phase_slope_limit	Selects phase slope limit for DPLL 00: 61 usec/sec 01: 7.5 usec/sec 10: 0.885 usec/sec 11: Unlimited
4	dpll_tie_clear_enable	Set high to align phase of the DPLL output clock with the phase of input reference. This bit should be held low if hitless reference switching is required.

Register_Address: **0x30**
Register Name: **dpll_ctrl**
Default Value: **0x0D**
Type: R/W

Bit Field	Function Name	Description
7:5	dpll_loop_bandwidth	Selects loop bandwidth of DPLL: 000: 14 Hz 001: 28 Hz 010: 56 Hz 011: 112 Hz 100: 224 Hz 101: 448 Hz 110: 896 Hz 111: reserved

Register_Address: **0x32**
Register Name: **dpll_ref_priority1_0**
Default Value: **0x10**
Type: R/W

Bit Field	Function Name	Description
2:0	dpll_ref0_priority	Selects Ref0 priority when DPLL operates in automatic reference switching mode: 000: ref0 has highest priority 001: ref0 has 2nd highest priority 010: ref0 has 3rd highest priority 011: ref0 has 4th highest priority 100: ref0 has 5th highest priority 101: ref0 has 6th highest priority 110: ref0 has 7th highest priority 111: ref0 is disabled **Note:** When references are programmed to have different priority number, DPLL will perform 'REVERTIVE' switching between them. This means that the DPLL will always switch to the highest priority reference (reference with lowest priority number) whenever that reference becomes available (doesn't fail). When references are programmed to have the same priority number, DPLL will perform 'NON-REVERTIVE' switching between them. This means that the DPLL will not perform switch to another reference with the same priority when that reference becomes available. Combinations of same and different priority numbers can be used, such that DPLL performs revertive switching between different priority references, but non-revertive switching among references with the same priority.

Register_Address: **0x32**
Register Name: **dpll_ref_priority1_0**
Default Value: **0x10**
Type: R/W

Bit Field	Function Name	Description
3	reserved	Leave as default
6:4	dpll_ref1_priority	Description same as above but for dpll_ref1_priority
7	reserved	Leave as default

Register_Address: **0x33**
Register Name: **dpll_mode_refsel**
Default Value: **0x03**
Type: R/W

Bit Field	Function Name	Description
1:0	dpll_mode	Selects DPLL mode of operation. 00: freerun mode 01: forced holdover mode 10: forced reference lock mode 11: automatic mode In 'automatic mode', reference selection is based on reference availability and reference priority selection. In this mode, DPLL will go to holdover only if none of 2 references is available. In 'forced reference lock mode', the DPLL has to lock to programmed reference (selected by the 'Reference selection or selected reference status' bits of this register. If the selected reference is not available, the DPLL will go to holdover mode and will not switch to another reference, regardless if some other references might be available. When the 'forced holdover mode' is programmed, all references are ignored and DPLL has to go to holdover (based on last selected reference). When the 'freerun mode' is selected, the DPLL has to generate all its output clocks based only on the oscillator OSCI input.
4:2	reserved	Leave as default
5	dpll_ext_fb_enable	When this bit is set to 1, DPLL will use the external feedback phase to compensate for the delay on all related output clocks (all output clocks coming from all synthesizers that are associated with the DPLL). When this bit is 0, DPLL will ignore external feedback. **Note:** There is only one external feedback available, so the external feedback phase will be used if this bit is set, regardless whether DPLL is used to create the external feedback phase or one of other DPLLs.

Register_Address: **0x33**
Register Name: **dpll_mode_refsel**
Default Value: **0x03**
Type: R/W

Bit Field	Function Name	Description
7:6	dpll_refsel_refstatus	When the 'DPLL mode' bits of this register are set to 11 (automatic mode), these bits are status bits and they represent selected reference status, i.e. 00 = Ref0 is selected as reference for DPLL and so on. When the 'DPLL mode' bits of this register are set to 10 (forced reference mode), these bits are control bits and they select which reference is DPLL forced to select as follows: 00: ref0 01: ref1 10: ref2 11: ref3 When forced reference fails, the DPLL will go to holdover mode. When the 'DPLL mode' bits of this register are set to 00 or 01 (freerun or holdover mode), these bits are ignored.

Register_Address: **0x34**
Register Name: **dpll_ref_fail_mask**
Default Value: **0x87**
Type: R/W

Bit Field	Function Name	Description
3:0	dpll_holdover_mask	When set low these bits prevent DPLL from going to holdover mode when corresponding reference failure mechanism occur. xxx0: mask holdover on LOS xx0x: mask holdover on SCM x0xx: mask holdover on CFM 0xxx: mask holdover on GST **Note:** GST bit should never be programmed to 1 if neither CFM nor SCM bits are programmed to 1 (e.g. bits 3:1 should never be programmed to '100').
7:4	dpll_refswitch_fail_mask	When set low these bits prevent reference switching to be performed when corresponding reference failure occurs. xxx0: mask reference switch on LOS xx0x: mask reference switch on SCM x0xx: mask reference switch on CFM 0xxx: mask reference switch on GST

Register_Address: **0x44**
Register Name: **dpll_hold_lock_fail**
Default Value: **0x00**
Type: R

Bit Field	Function Name	Description
0	dpll_holdover_status	The device will set this bit high when DPLL is in holdover mode. **Note:** This bit is not maskable.
1	dpll_lock_status	The device will set this bit high when DPLL is locked to an input reference. **Note:** This bit is not maskable.
7:2	reserved	Leave as default

Register_Address: **0x45**
Register Name: **ext_fb_ctrl**
Default Value: **0x00**
Type: R/W

Bit Field	Function Name	Description
1:0	reserved	Leave as default
2	ext_fb_ref_select	0: ref0 is selected as external feedback source 1: ref1 is selected as external feedback source
6:3	reserved	Leave as default
7	ext_fb_enable	When set high, this bit enables external feedback **Note:** In order to have proper behaviour with external feedback, it is required that main reference and the external feedback source are frequency locked (they do not have to have the same frequency).

Register_Address: **0x46**
Register Name: **reduced_diff_out_pw**
Default Value: **0x00**
Type: R/W

Bit Field	Function Name	Description
0	hpout0_reduced_pwr	When this bit is set to high, it will enable reduced power mode for HPDIFF0_P and HPDIFF0_N outputs. When low, the outputs are in full power mode.
1	hpout1_reduced_pwr	Same description as above but for HPDIFF1 output.
2	hpout2_reduced_pwr	Same description as above but for HPDIFF2 output.
3	hpout3_reduced_pwr	Same description as above but for HPDIFF3 output.
7:4	reserved	Leave as default.

Register_Address: **0x47**
Register Name: **phasememlimit_ref0**
Default Value: **0x02**
Type: R/W

Bit Field	Function Name	Description
7:0	ref0_phasemem_limit	Unsigned binary value of these bits represents Ref0 phase memory limit expressed in 10 us units. This register should be programmed to have value that is at least one reference period.

Register_Address: **0x48**
Register Name: **phasememlimit_ref1**
Default Value: **0x02**
Type: R/W

Bit Field	Function Name	Description
7:0	ref1_phasemem_limit	Unsigned binary value of these bits represents Ref1 phase memory limit expressed in 10 us units. This register should be programmed to have value that is at least one reference period.

Register_Address: **0x4B**
Register Name: **scm_cfm_limit_ref0**
Default Value: **0x55**
Type: R/W

Bit Field	Function Name	Description
2:0	ref0_cfm_limit	These bits represent Ref0 Coarse Frequency Monitor (CFM) limit selection. When Ref0 fails criteria specified by these bits, the CFM failure indicator will go high (can be read in the 'Ref0 and Ref1 failure indicators' register). Selection: 000 = +/- 0.1% (in Ref0 frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50%
3	reserved	Leave as default.
6:4	ref0_scm_limit	These bits represent Ref0 Single Cycle Monitor (SCM) limit selection. When Ref0 fails criteria specified by these bits, the SCM failure indicator will go high. Selection: 000 = +/- 0.1% (in Ref0 frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50% Note that Ref0 clock is sampled by 800 MHz clock, so the measurement granularity is 1.25 ns. This imposes limitation to SCM limits that can be programmed depending on Ref0 clock frequencies: +/- 0.1% can be programmed for frequencies below 800 kHz +/- 0.5% : below 4 MHz +/- 1% : below 8 MHz +/- 2% : below 16 MHz +/- 5% : below 40 MHz +/- 10% : below 80 MHz +/- 20% : below 160 MHz +/- 50% : below 400 MHz **Note:** SCM indicator should not be used (should be masked) for input references frequencies above 400 MHz.

Register_Address: **0x4B**
Register Name: **scm_cfm_limit_ref0**
Default Value: **0x55**
Type: R/W

Bit Field	Function Name	Description
7	reserved	Leave as default.

Register_Address: **0x4C**
Register Name: **scm_cfm_limit_ref1**
Default Value: **0x55**
Type: R/W

Bit Field	Function Name	Description
2:0	ref1_cfm_limit	These bits represent Ref1 Coarse Frequency Monitor (CFM) limit selection. When Ref1 fails criteria specified by these bits, the CFM failure indicator will go high. Selection: 000 = +/- 0.1% (in Ref1 frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50%
3	reserved	Leave as default

Register_Address: **0x4C**
Register Name: **scm_cfm_limit_ref1**
Default Value: **0x55**
Type: R/W

Bit Field	Function Name	Description
6:4	ref1_scm_limit	These bits represent Ref1 Single Cycle Monitor (SCM) limit selection. When Ref1 fails criteria specified by these bits, the SCM failure indicator will go high. Selection: 000 = +/- 0.1% (in Ref1 frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50% Note that Ref1 clock is sampled by 800 MHz clock, so the measurement granularity is 1.25 ns. This imposes limitation to SCM limits that can be programmed depending on Ref1 clock frequencies: +/- 0.1% can be programmed for frequencies below 800 kHz +/- 0.5% : below 4 MHz +/- 1% : below 8 MHz +/- 2% : below 16 MHz +/- 5% : below 40 MHz +/- 10% : below 80 MHz +/- 20% : below 160 MHz +/- 50% : below 400 MHz **Note:** SCM indicator should not be used (should be masked) for input references frequencies above 400 MHz.
7	default	Leave as default.

Register_Address: **0x4F**
Register Name: **dpll_config**
Default Value: **0x31**
Type:**R/W**

Bit Field	Function Name	Description
0	dpll_config	Enables DPLL 0: DPLL disabled 1: DPLL enabled
3:1	reserved	Leave as default.
5:4	phase_acquisiton_enable	When set high enables corresponding phase acquisition module. When set low powers down corresponding module. x1: enables phase acquisition module 0 1x: enables phase acquisition module 1
7:5	reserved	Leave as default

Register_Address: **0x50:0x51**
Register Name: **synth_base_freq**
Default Value: **0x61A8**
Type:**R/W**

Bit Field	Function Name	Description
15:0	synth_base_freq_Bs	Unsigned binary value of these bits represents Synthesizer base frequency Bs in Hz. Examples of values fro Bs that can be programmed: 0x1F40 for 8 kHz, 0x61A8 for 25 kHz, 0x9C40 for 40 kHz. **Note 1**: Bs has to be directly divisible from 1600000000, i.e. mod (1600000000, Bs) has to be 0 **Note 2:** Bs has to be chosen such that programmed output frequency is either 8 k or 25 k multiple (except for allowed case of Ms/Ns = 66/64 when Br = 25000 and Kr = 3125). So, either 8000 or 25000 has to be directly divisible from Bs x Ks / P, i.e. mod (Bs x Ks / P, 8000) or mod (Bs x Ks / P, 25000) has to be 0, where P is chosen postdivider ratio.

Register_Address: **0x52:0x53**
Register Name: **synth_freq_multiple**
Default Value: **0x0C35**
Type:**R/W**

Bit Field	Function Name	Description
15:0	synth_base_freq_mult_Ks	Unsigned binary value of these bits represents Synthesizer base frequency multiplication number. The 'Base frequency' number Bs multiplied by the 'Base frequency multiple' number Ks, and multiplied by 16 equals the synthesizer frequency in Hz. Synthesizer frequency multiple Ks / Base frequency Bs / Base frequency 1.048576 GHz / 8 kHz (0x1F40) / 8192 (0x2000) 1.25 GHz / 25 kHz (0x61A8) / 3125 (0x0C35) **Note:** Ks has to be chosen such that programmed output frequency is either 8 k or 25 k multiple (except for allowed case of Ms/Ns = 66/64 when Br = 25000 and Kr = 3125). So, either 8000 or 25000 has to be directly divisible from Bs x Ks / P, i.e. mod (Bs x Ks / P, 8000) or mod (Bs x Ks / P, 25000) has to be 0, where P is chosen postdivider ratio.

Register_Address: **0x54:0x57**
Register Name: **synth_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
15:0	synth_ratio_denom_Ns	Unsigned binary value of Ms bits, in combination with unsigned binary value of Ns bits represents Synthesizer FEC multiplication ratio. Synthesizer FEC frequencies are calculated using the following formula: Synth_freq [Hz] = Bs x Ks x 16 x Ms / Ns
31:16	synth_ratio_numer_Ms	Ms and Ns are limited to: 1) Ms = 66 and Ns = 64. These values for Ms and Ns are allowed only when Bs and Ks are programmed to Br = 25000 and Kr = 3125. 2) Ms = 1 and Ns = 1 for all other cases (default values)

Register_Address: **0x71**
Register Name: **output_synth_en**
Default Value: **0x01**
Type:**R/W**

Bit Field	Function Name	Description
0	synth_en	Enables output Synthesizer 0: disables synth output 1: enables synth output
7:1	reserved	Leave as default

Register_Address: **0x72**
Register Name: **dpll_lock_selection**
Default Value: **0xAA**
Type:**R/W**

Bit Field	Function Name	Description
1:0	dpll_lock_selection	Selects DPLL lock indicator status condition (appearing in the 'DPLL lock fail' register). 00: reserved 01: phase error is smaller than 1 us during 1 s 10: phase error is smaller than 10 us during 1 s 11: phase error is smaller than 10 us during 10 s
7:2	reserved	Leave as default

Register_Address: **0x73:0x76**
Register Name: **central_freq_offset**
Default Value: **0x046AAAAB**
Type:**R/W**

Bit Field	Function Name	Description
31:0	central_freq_offset	2's complement binary value of these bits represent central frequency offset for the device. This value should be used to compensate for oscillator inaccuracy, or make the device look like Numerically Controlled Oscillator (NCO). This register controls central frequency of all 4 Synthesizers. Expressed in steps of +/- 2^-32 of nominal setting. When oscillator inaccuracy is known: inacc_osc = (f_osc - f_nom)/f_nom (usually specified in ppm), value to be programmed in this register is calculated as per the following formula: X = (1/(1 + inacc_osc) - 1)*2^32, when f_osc < f_nom X = (1/(1 + inacc_osc))*2^32, when f_osc > f_nom, where inacc_osc - represents oscillator frequency inaccuracy, f_osc - represents oscillator frequency, and f_nom - represents oscillator nominal frequency (i.e., 25 MHz, 20 MHz) Generally, when the oscillator frequency is lower than the nominal, frequency offset has to be programmed to compensate it in opposite direction, i.e. frequency offset has to be positive, and vice versa. Example 1): if oscillator inaccuracy is -2% (f_osc = 24.5 MHz; inacc_osc = (f_osc - 25 MHz)/25MHz = -0.02), X= (1/(1+(-0.02)) - 1)*2^32 = (1/0.98 - 1)*2^32 = 87652394 = 0x0539782A Example 2): if oscillator inaccuracy is +2% (f_osc = 25.5 MHz; inacc_osc = (f_osc - 25 MHz)/25MHz = 0.02), X= (1/(1+ 0.02))*2^32 = (1/1.02)*2^32 = 4210752251 = 0xFAFAFAFB When NCO behaviour is desired, the output frequency should be calculated as per formula: fout = (1 + X/2^32)*finit where X -represent 2's complement number specified in this register finit - initial frequency set by Bs, Ks, Ms, Ns and postdivider number for particular VCO fout - output frequency **Note 1:** Nominal frequency for central frequency offset calculation is 25 MHz although master clock frequency is required to be 24.576 MHz. Because of this default value in this register is 0x046AAAAB. **Note 2:** Central Frequency Offset should not exceed +/-5% off nominal.

Register_Address: **0x77**
Register Name: **synth_filter_sel**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
0	synth_filter_select	Selects filter used by Synthesizer 0: external filter 1: internal filter
7:1	reserved	reserved

Register_Address: **0x78**
Register Name: **synth_fine_phase_shift**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	syn_fine_phase_shift	Unsigned binary value of these bits represent Synth fine phase shift (advancement) in steps of Synth_period / 256. **Note 1:** This register controls fine phase shift for all clocks coming out of the Synthesizer (including all four postdividers).

Register_Address: **0x7F**
Register Name: **page_register**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
0	page_select	This register is used to toggle memory access between page 0 (addresses 0x00 to 0x7E) and page 1 (addresses 0x80 to 0xFF). This is required because SPI and I2C ports have only seven address bits and the device memory space is eight bit wide. 0: selects addresses 0x00 to 0x7E 1: selects addresses 0x80 to 0xFB
7:1	reserved	reserved

Register_Address: **0x80:0x82**
Register Name: **synth_post_div_A**
Default Value: **0x000008**
Type:**R/W**

Bit Field	Function Name	Description
15:0	frm_pulse_period_or_div	When bits 23:20 of this register are programmed to '1111', binary value of these bits represent number of periods of the selected related clock in between two frame pulses When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock (Synthesizer Post Divider value PA). The Synthesizer VCO frequency is divided by the PA value to get desired output clock frequency on selected output pins. **Note 1:** Values 0x000000 and 0x000001 are not allowed. They cause output pin to not to have any clock. **Note 2:** PA has to be chosen such that programmed output frequency is either 8 k or 25 k multiple (except for allowed case of Ms/Ns = 66/64 when Br = 25000 and Kr = 3125). So, either 8000 or 25000 has to be directly divisible from Bs x Ks / PA, i.e. mod (Bs x Ks / PA, 8000) or mod (Bs x Ks / PA, 25000) has to be 0, where PA is chosen postdivider ratio. Otherwise, the PA is internally forced to 0x000001.

Register_Address: **0x80:0x82**
Register Name: **synth_post_div_A**
Default Value: **0x000008**
Type:**R/W**

Bit Field	Function Name	Description
17:16	frm_pulse_clk_sel_or_div	When bits 23:20 of this register are programmed to '1111', these bits select related clock (postdivider) within the synthesizer (frame pulse width is equal to the related clock period): 00: reserved 01: hpdiff2,3 (Synth postdivider B) 10: hpoutclk0 (Synth postdivider C) 11: hpoutclk1(Synth postdivider D) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock. **Note:** It is forbidden for frame pulse to select 'itself' as its related clock.
18	frm_pulse_polar_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse polarity: 0: regular (non-inverse) polarity 1: inverse polarity When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock.
19	frm_pulse_type_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse type: 0: ST-BUS type frame pulse (frame boundary straddles in the middle of the frame pulse) 1: GCI Bus type frame pulse (frame boundary defined by the edge of the frame pulse) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock.

Register_Address: **0x80:0x82**
Register Name: **synth_post_div_A**
Default Value: **0x000008**
Type:**R/W**

Bit Field	Function Name	Description
23:20	frm_pulse_or_div	When these bits are programmed to '1111', the appropriate output clock is selected to have a 'frame pulse' shape. Details about the frame pulse type, polarity and frequency are specified in bits 19:0 of this register. When these bits are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with bits 19:0 of this register creates postdivider ratio for the output clock (i.e. division ratio between appropriate VCO frequency and the desired output clock frequency). Note: Maximum division ratio for 'normal' clock is 0xEFFFFF = 15728639.

Register_Address: **0x83:0x85**
Register Name: **synth_post_div_B**
Default Value: **0x00000A**
Type:**R/W**

Bit Field	Function Name	Description
15:0	frm_pulse_period_or_div	When bits 23:20 of this register are programmed to '1111', binary value of these bits represent number of periods of the selected related clock in between two frame pulses When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock (Synthesizer Post Divider value PB). The Synthesizer VCO frequency is divided by the PB value to get desired output clock frequency on selected output pins. **Note 1:** Values 0x000000 and 0x000001 are not allowed. They cause output pin to not to have any clock. **Note 2:** PB has to be chosen such that programmed output frequency is either 8 k or 25 k multiple (except for allowed case of Ms/Ns = 66/64 when Br = 25000 and Kr = 3125). So, either 8000 or 25000 has to be directly divisible from Bs x Ks / PB, i.e. mod (Bs x Ks / PB, 8000) or mod (Bs x Ks / PB, 25000) has to be 0, where PB is chosen postdivider ratio. Otherwise, the PB is internally forced to 0x000001.

Register_Address: **0x83:0x85**
Register Name: **synth_post_div_B**
Default Value: **0x00000A**
Type:**R/W**

Bit Field	Function Name	Description
17:16	frm_pulse_clk_sel_or_div	When bits 23:20 of this register are programmed to '1111', these bits select related clock (postdivider) within the synthesizer (frame pulse width is equal to the related clock period): 00: hpdiff0,1 (Synth postdivider A) 01: reserved 10: hpoutclk0 (Synth postdivider C) 11: hpoutclk1(Synth postdivider D) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock. **Note:** It is forbidden for frame pulse to select 'itself' as its related clock.
18	frm_pulse_polar_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse polarity: 0: regular (non-inverse) polarity 1: inverse polarity When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock.
19	frm_pulse_type_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse type: 0: ST-BUS type frame pulse (frame boundary straddles in the middle of the frame pulse) 1: GCI Bus type frame pulse (frame boundary defined by the edge of the frame pulse) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock.

Register_Address: **0x83:0x85**
Register Name: **synth_post_div_B**
Default Value: **0x00000A**
Type:**R/W**

Bit Field	Function Name	Description
23:20	frm_pulse_or_div	When these bits are programmed to '1111', the appropriate output clock is selected to have a 'frame pulse' shape. Details about the frame pulse type, polarity and frequency are specified in bits 19:0 of this register. When these bits are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with bits 19:0 of this register creates postdivider ratio for the output clock (i.e. division ratio between appropriate VCO frequency and the desired output clock frequency). Note: Maximum division ratio for 'normal' clock is 0xEFFFFF = 15728639.

Register_Address: **0x86:0x88**
Register Name: **synth_post_div_C**
Default Value: **0x00000A**
Type:**R/W**

Bit Field	Function Name	Description
15:0	frm_pulse_period_or_div	When bits 23:20 of this register are programmed to '1111', binary value of these bits represent number of periods of the selected related clock in between two frame pulses. When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock (Synthesizer Post Divider value PC). The Synthesizer VCO frequency is divided by the PC value to get desired output clock frequency on selected output pins. **Note 1:** Values 0x000000 and 0x000001 are not allowed. They cause output pin to not to have any clock. **Note 2:** PC has to be chosen such that programmed output frequency is either 8 k or 25 k multiple (except for allowed case of Ms/Ns = 66/64 when Br = 25000 and Kr = 3125). So, either 8000 or 25000 has to be directly divisible from Bs x Ks / PC, i.e. mod (Bs x Ks / PC, 8000) or mod (Bs x Ks / PC, 25000) has to be 0, where PC is chosen postdivider ratio. Otherwise, the PC is internally forced to 0x000001. **Note 3:** The output clock duty-cycle may not be within specified 45% to 55% when post divider value PC is an odd number and where frequency of the output clock is close to the maximum output frequency supported by hpoutclk. The worst case duty-cycle is 30% is when synthesizer frequency is set to 1 GHz and the PC is set to 7. If duty-cycle of 45% to 55% is required, user can set synthesizer to run at 1GHz * 8/7 and PC to 8 which will still generate the same frequency but within 45% to 55% duty-cycle. For odd PC values greater than or equal to 41 (43, 45 ...) the duty-cycle will be within 45% to 55%. For even PC values duty-cycle is always within 45% to 55%.

Register_Address: **0x86:0x88**
Register Name: **synth_post_div_C**
Default Value: **0x00000A**
Type:**R/W**

Bit Field	Function Name	Description
17:16	frm_pulse_clk_sel_or_div	When bits 23:20 of this register are programmed to '1111', these bits select related clock (postdivider) within the synthesizer (frame pulse width is equal to the related clock period): 00: hpdiff0,1 (Synth postdivider A) 01: hpdiff2,3 (Synth postdivider B) 10: reserved 11: hpoutclk1(Synth postdivider D) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock. **Note:** It is forbidden for frame pulse to select 'itself' as its related clock.
18	frm_pulse_polar_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse polarity: 0: regular (non-inverse) polarity 1: inverse polarity When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock.
19	frm_pulse_type_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse type: 0: ST-BUS type frame pulse (frame boundary straddles in the middle of the frame pulse) 1: GCI Bus type frame pulse (frame boundary defined by the edge of the frame pulse) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock.

Register_Address: **0x86:0x88**
Register Name: **synth_post_div_C**
Default Value: **0x00000A**
Type:**R/W**

Bit Field	Function Name	Description
23:20	frm_pulse_or_div	When these bits are programmed to '1111', the appropriate output clock is selected to have a 'frame pulse' shape. Details about the frame pulse type, polarity and frequency are specified in bits 19:0 of this register. When these bits are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with bits 19:0 of this register creates postdivider ratio for the output clock (i.e. division ratio between appropriate VCO frequency and the desired output clock frequency). Note: Maximum division ratio for 'normal' clock is 0xEFFFFF = 15728639.

Register_Address: **0x89:0x8B**
Register Name: **synth_post_div_D**
Default Value: **0x000032**
Type:**R/W**

Bit Field	Function Name	Description
15:0	frm_pulse_period_or_div	When bits 23:20 of this register are programmed to '1111', binary value of these bits represent number of periods of the selected related clock in between two frame pulses When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock (Synthesizer Post Divider value PD). The Synthesizer VCO frequency is divided by the PD value to get desired output clock frequency on selected output pins. **Note 1:** Values 0x000000 and 0x000001 are not allowed. They cause output pin to not to have any clock. **Note 2:** PD has to be chosen such that programmed output frequency is either 8 k or 25 k multiple (except for allowed case of Ms/Ns = 66/64 when Br = 25000 and Kr = 3125). So, either 8000 or 25000 has to be directly divisible from Bs x Ks / PD, i.e. mod (Bs x Ks / PD, 8000) or mod (Bs x Ks / PD, 25000) has to be 0, where PC is chosen postdivider ratio. Otherwise, the PD is internally forced to 0x000001. **Note 3:** The output clock duty-cycle may not be within specified 45% to 55% when post divider value PD is an odd number and where frequency of the output clock is close to the maximum output frequency supported by hpoutclk. The worst case duty-cycle is 30% is when synthesizer frequency is set to 1 GHz and the PD is set to 7. If duty-cycle of 45% to 55% is required, user can set synthesizer to run at 1GHz * 8/7 and PD to 8 which will still generate the same frequency but within 45% to 55% duty-cycle. For odd PD values greater than or equal to 41 (43, 45 ...) the duty-cycle will be within 45% to 55%. For even PD values duty-cycle is always within 45% to 55%.

Register_Address: **0x89:0x8B**
Register Name: **synth_post_div_D**
Default Value: **0x000032**
Type:**R/W**

Bit Field	Function Name	Description
17:16	frm_pulse_clk_sel_or_div	When bits 23:20 of this register are programmed to '1111', these bits select related clock (postdivider) within the synthesizer (frame pulse width is equal to the related clock period): 00: hpdiff0,1 (Synth postdivider A) 01: hpdiff2,3 (Synth postdivider B) 10: hpoutclk0(Synth postdivider C) 11: reserved When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock. **Note:** It is forbidden for frame pulse to select 'itself' as its related clock.
18	frm_pulse_polar_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse polarity: 0: regular (non-inverse) polarity 1: inverse polarity When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock.
19	frm_pulse_type_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse type: 0: ST-BUS type frame pulse (frame boundary straddles in the middle of the frame pulse) 1: GCI Bus type frame pulse (frame boundary defined by the edge of the frame pulse) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock.

Register_Address: **0x89:0x8B**
Register Name: **synth_post_div_D**
Default Value: **0x000032**
Type:**R/W**

Bit Field	Function Name	Description
23:20	frm_pulse_or_div	When these bits are programmed to '1111', the appropriate output clock is selected to have a 'frame pulse' shape. Details about the frame pulse type, polarity and frequency are specified in bits 19:0 of this register. When these bits are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with bits 19:0 of this register creates postdivider ratio for the output clock (i.e. division ratio between appropriate VCO frequency and the desired output clock frequency). Note: Maximum division ratio for 'normal' clock is 0xEFFFFF = 15728639.

Register_Address: **0xB0**
Register Name: **hp_diff_en**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
3:0	hp_diff_en	Set high to enable corresponding high performance differential output. Set low to tristate the corresponding output. xxx1: enables hpdiff0_p/n xx1x: enables hpdiff1_p/n x1xx: enables hpdiff2_p/n 1xxx: enables hpdiff3_p/n
7:4	reserved	Leave as default

Register_Address: **0xB1**
Register Name: **hp_cmos_en**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
1:0	hp_cmos_en	Set high to enable corresponding high performance output. Set low to tristate the corresponding output. x1: enables hpout0 1x: enables hpout1
7:2	reserved	Leave as default.

Register_Address: **0xB8**
Register Name: **synth_stop_clock**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
1:0	synth_post_div_C_stop	Appropriate setting of these bits will cause Synthesizer Post Divider C to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop hpoutclk0 at falling edge (output stays low) 11: stop hpoutclk0 at rising edge (output stays high) **Note:** Polarity will be reversed is this clock is selected by register 0xB5 to appear on configurable outputs.
3:2	synth_post_div_D_stop	Appropriate setting of these bits will cause Synthesizer Post Divider D to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop hpoutclk1 at falling edge (output stays low) 11: stop hpoutclk1 at rising edge (output stays high) **Note:** Polarity will be reversed is this clock is selected by register 0xB5 to appear on configurable outputs.
7:4	reserved	Leave as default

Register_Address: **0xB9**
Register Name:**sync_fail_flag_status**
Default Value: **0x00**
Type:**StickyR**

Bit Field	Function Name	Description
0	Synth_syncFail_flag	When high, this bit indicates that Synthesizer has lost lock. If this status bit appears set after clearing Synth_ClearSyncFail_flag (register at address 0xBA), it is indication that Synthesizer has lost lock, therefore generating wrong output frequency. **Note:** This bit will be set upon power up or device reset.
7:1	reserved	Leave as default.

Register_Address: **0xBA**
Register Name:**clear_sync_fail_flag**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
0	Synth_clearSyncFail_flag	When high, this bit clears sticky Synth_syncFail_flag. **Note:** after clearing Synth_syncFail_flag, this bit must be set low for normal device operation.
7:1	reserved	Leave as default.

Register_Address: **0xBF:0xC0**
Register Name:**phase_shift_s0_postdiv_c**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	phase_shift_s0_postdiv_c	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer frequency for all clocks coming from Synthesizer Post Divider C (0:no shift, -1: delay output clock for 1 period, 1: advance output clock for 1 period, and so on).

Register_Address: **0xBF:0xC0**
Register Name:**phase_shift_s0_postdiv_c**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	quad_shift_s0_postdiv_c	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer Post Divider C. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xC1:0xC2**
Register Name:**phase_shift_s0_postdiv_d**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	phase_shift_s0_postdiv_d	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer frequency for all clocks coming from Synthesizer Post Divider D (0: no shift, -1: delay output clock for 1 period, 1: advance output clock for 1 period, and so on).
15:13	quad_shift_s0_postdiv_d	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer Post Divider D. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xC3**
Register Name:**xo_or_crystal_sel**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
0	xo_or_crystal_sel	0: enables OSCo driver 1: disables OSCo driver Set to 1 when xo is used as master clock. Set to 0 when crystal is used as master clock.
7:1	Reserved	Leave as default

Register_Address: **0xC6**
Register Name:**Chip_revision_2**
Default Value: **0x03**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Chip_revision_2	Chip_revision_2 = 0b00000011 (full chip revision = chip_revision_2 bits in register 0xC6 and chip_revision bits[6:5] in register 0x00)

Register_Address: **0xE0**
Register Name:**gpio_function_pin0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin0_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO0 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO pin unused.
7	gpio_pin0_con_or_stat_sel	Selects whether GPIO0 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE1**
Register Name:**gpio_function_pin1**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin1_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO1 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO pin unused.
7	gpio_pin1_con_or_stat_sel	Selects whether GPIO1 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE2**
Register Name:**gpio_function_pin2**
Default Value: **0x60**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin2_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO2 control or status select' bit. The control and status table consist of 128 bits each. Default: hpdiff0 enable.
7	gpio_pin2_con_or_stat_sel	Selects whether GPIO2 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE3**
Register Name:**gpio_function_pin3**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin3_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO3 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO pin unused.
7	gpio_pin3_con_or_stat_sel	Selects whether GPIO3 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE4**
Register Name:**gpio_function_pin4**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin4_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO4 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO pin unused.
7	gpio_pin4_con_or_stat_sel	Selects whether GPIO4 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE5**
Register Name:**gpio_function_pin5**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin5_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO5 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO pin unused.

Register_Address: **0xE5**
Register Name:**gpio_function_pin5**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	gpio_pin5_con_or_stat_sel	Selects whether GPIO5 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE6**
Register Name:**gpio_function_pin6**
Default Value: **0x70**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin6_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO6 control or status select' bit. The control and status table consist of 128 bits each. Default:hpoutclk0 enable.
7	gpio_pin6_con_or_stat_sel	Selects whether GPIO6 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xF7**
Register Name:**spurs_suppression**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	spurs_suppression	This register is used for spurs suppression. Depending on the synthesizer configuration GUI will generate recommended value. Please refer to GUI for recommended value that should be written to this register. When the spurs_supression register is changed, the ZL30158 requires 200msec to reconfigure itself, no reads or writes to the device are permitted during this reconfiguration period. The spurs_suppression register should only be written with values recommended by the GUI and it should only be written if a 24.576MHz master clock oscillator or crystal resonator is being used

9.0 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage	V_{DD_R}	-0.5	4.6	V
2	Core supply voltage	V_{CORE_R}	-0.5	2.5	V
3	Voltage on any digital pin	V_{PIN}	-0.5	6	V
4	Voltage on osci and osco pin	V_{OSC}	-0.3	V_{DD} + 0.3	V
5	Storage temperature	T_{ST}	-55	125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated

Recommended Operating Conditions*

	Characteristics	Sym	Min.	Typ.	Max.	Units
1	Supply voltage	V_{DD-IO} AV_{DD}	3.135	3.30	3.465	V
2	Core supply voltage	V_{CORE} AV_{CORE}	1.71	1.80	1.89	V
3	Operating temperature	T_A	-40	25	85	°C
4	Input voltage	V_{DD-IO}	3.135	3.30	3.465	V

* Voltages are with respect to ground (GND) unless otherwise stated

DC Electrical Characteristics - Power - Core

	Characteristics	Sym	Typ.	Max.	Units	Notes
1	Core supply current (Vcore)	I_{CORE} (Vdd 3.3V)	46	48	mA	
		I_{CORE} (Vdd 1.8V)	102	109	mA	
2	Current for HP Synthesis Engine	I_{SYN} (Vdd 3.3V)	57	73	mA	
		I_{SYN}(Vdd 1.8V)	0.2	1	mA	

DC Electrical Characteristics - Power - High Performance Outputs

	Characteristics	Sym.	Typ.	Max.	Units	Notes
1	Power for each hpdiff clock driver	P_{hpdiff}(Vdd 3.3V)	85	91	mW	Including power to biasing and load resistors R_L = 50Ω
2	Power for each hpdiff clock driver minus power dissipated in the biasing and load resistors.	P_{hpdiff}(Vdd 3.3V)	36	42	mW	Without power to biasing and load resistors R_L = 50Ω
3	Power for each hpdiff clock driver (reduced power mode)	$P_{hpdifflp}$(Vdd 3.3V)	80	86	mW	Including power to biasing and load resistors R_L = 50Ω
4	Power for each hpdiff clock driver minus power dissipated in the load resistor. (reduced power mode)	$P_{hpdifflp}$(Vdd 3.3V)	31	37	mW	Without power to biasing and load resistors R_L = 50Ω
5	Power for each output divider of high performance synthesizers (enabled if one of two differential outputs assigned to it is enabled).	P_{div}(Vdd 3.3V)	17	40	mW	
6	Power for each hpoutclk clock driver	P_{hpout}(Vdd 3.3V)	17+ 7	40+36	mW	155.52 MHz output 10 pF load fixed power (due to output divider) + variable power (proportional to frequency and load)

DC Electrical Characteristics - Inputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage	V_{CIH}	$0.7 \cdot V_{DD-IO}$			V	
2	CMOS low-level input voltage	V_{CIL}			$0.3 \cdot V_{DD-IO}$	V	
3	CMOS Input leakage current	I_{IL}	-10		10	µA	$V_I = V_{DD}$ or 0 V
4	Differential input common mode voltage	V_{CM}	1.1		2.0	V	
5	Differential input voltage difference	V_{ID}	0.25		1.0	V	

AC/DC Electrical Characteristics - OSCi Input

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage	V_{CIH}	2.0			V	
2	CMOS low-level input voltage	V_{CIL}			0.8	V	
3	Input leakage current	I_{IL}	-10		10	µA	$V_I = V_{DD}$ or 0 V
4	Duty Cycle		40		60	%	

DC Electrical Characteristics - High Performance Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	HPCMOS High-level output voltage	V_{OH}	$0.8 \cdot AV_{DD}$			V	I_{OH} = 2mA C_L = 5pF
2	HPCMOS Low-level output voltage	V_{OH}			$0.2 \cdot AV_{DD}$	V	I_{OL} = 2mA C_L = 5pF
3	LVPECL: High-level output voltage	V_{OH_LVPECL}	AV_{DD} - 1.12	AV_{DD} - 1.00	AV_{DD} - 0.88	V	R_L = 50Ω to AV_{DD} - 2V, C_L = 1pF
4	LVPECL: Low-level output voltage	V_{OL_LVPECL}	AV_{DD} - 1.81	AV_{DD} - 1.71	AV_{DD} - 1.55	V	R_L = 50Ω to AV_{DD} - 2V, C_L = 1pF
5	LVPECL: Differential output voltage *	V_{OD_LVPECL}	0.53	0.67	0.80	V	R_L = 50Ω to AV_{DD} - 2V, C_L = 1pF

* Output swing is guaranteed for frequency up to 720MHz, it may decrease by 50mv if the frequency is greater than 720 MHz

AC Electrical Characteristics* - Output Timing Parameters Measurement Voltage Levels (see Figure 26)

	Characteristics	Sym.	CMOS	LVPECL	Units
1	Threshold Voltage	$V_{T\text{-}CMOS}$ $V_{T\text{-}LVPECL}$	$0.5V_{DD}$	V_{DD}-1.35	V
2	Rise and Fall Threshold Voltage High	V_{HM}	$0.8V_{DD}$	$0.8V_{OD_LVPECL}$	V
3	Rise and Fall Threshold Voltage Low	V_{LM}	$0.2V_{DD}$	$0.2V_{OD_LVPECL}$	V

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated

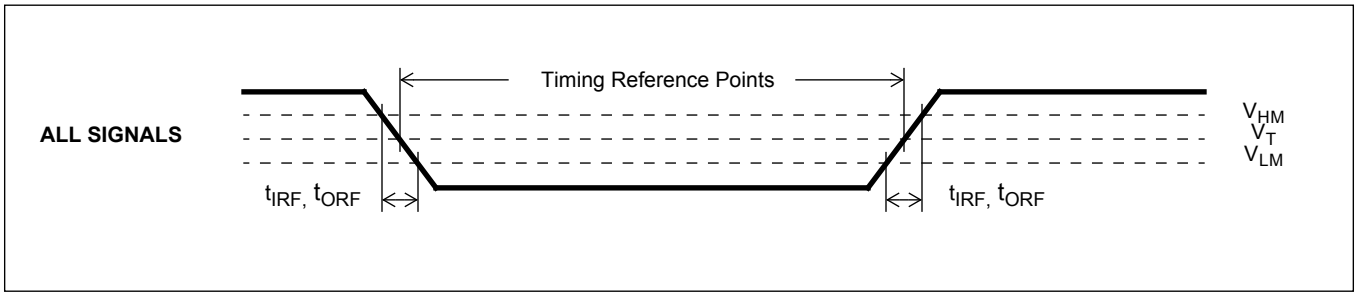


Figure 26 - Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics* - Inputs (see Figure 27).

	Characteristics	Symbol	Min.	Typ.	Max.	Units
1	Input reference Frequency (CMOS Inputs)	$1/t_{REFP}$			177.5	MHz
2	Input reference Frequency (LVPECL Inputs)	$1/t_{REFP}$			750	MHz
3	Input reference pulse width high or low	t_{REFW}	0.55			ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions

AC Electrical Characteristics* - Input To Output Timing (see Figure 27)

	Characteristics	Symbol	Min.	Typ.	Max.	Units
1	Input reference to hpoutclk0 output clock (with same frequency) delay	t_{HP_REFD}		0		ns
2	Input reference to outclk0 (with same frequency) delay	t_{REFD}		0		ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

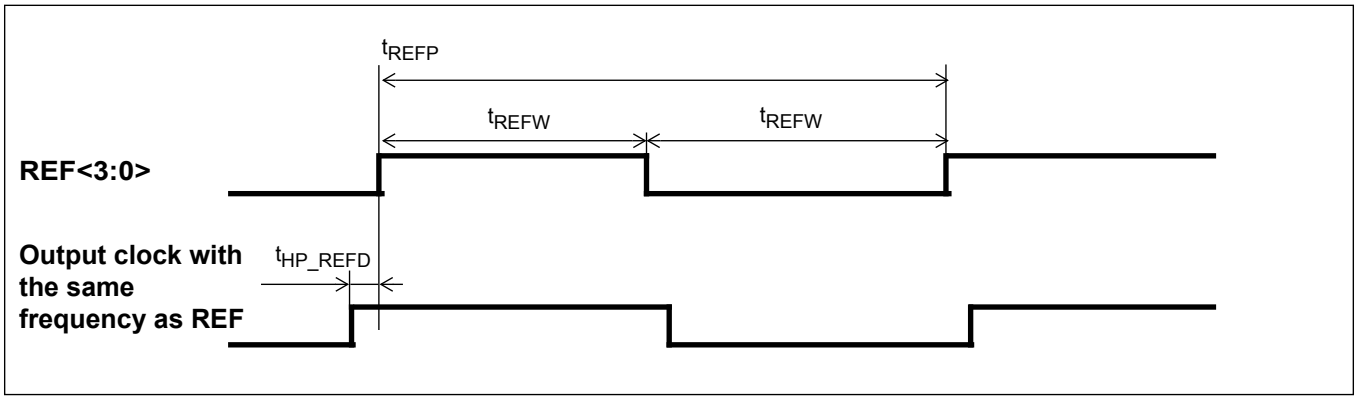


Figure 27 - Input To Output Timing for hpoutclk0

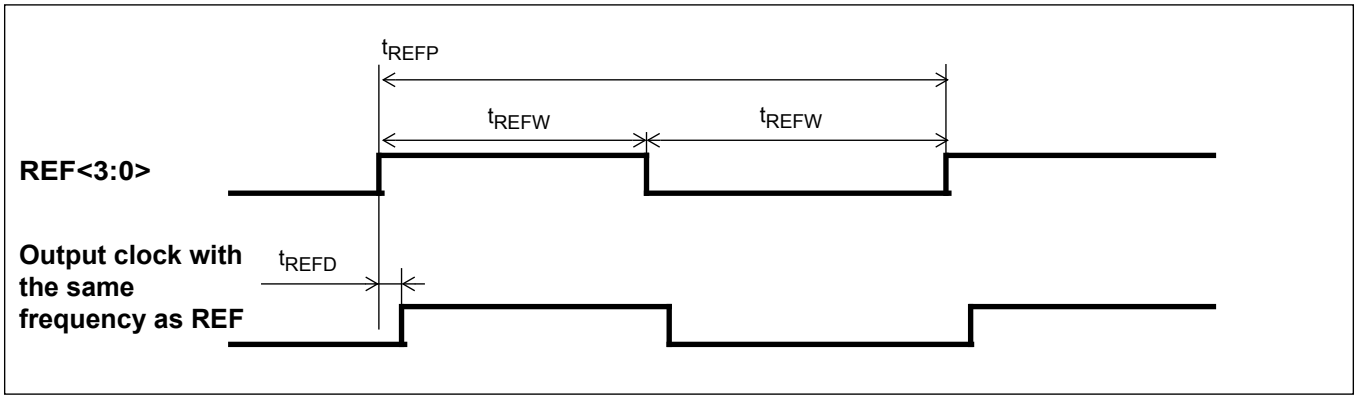


Figure 28 - Input To Output Timing To outclk0

AC Electrical Characteristics* - Outputs (see Figure 29).

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Clock skew between outputs	$t_{OUT2OUTD}$		0		ns	
2	Output clock Duty Cycle	t_{PWH}, t_{PWL}	45%	50%	55%	Duty Cycle	
3	LVPECL Output clock rise or fall time	t_r / t_f	265	370	515	ps	
4	LVCMOS output clock rise and fall time	t_r / t_f	620	950	1490	ps	10pF load
5	Output Clock Frequency (hpdiff)	F_{hpdiff}			750	MHz	
6	Output Clock Frequency (hpoutclk)	F_{hpout}			177.5	MHz	

* Supply voltage and operating temperature are as per Recommended Operating Conditions

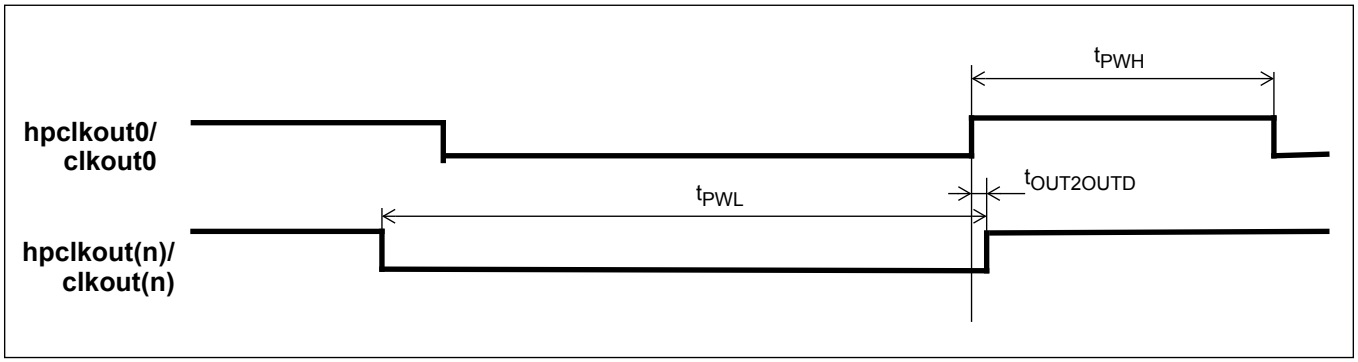


Figure 29 - Output Timing Referenced To hpclkout0/clkout0

Functional waveforms and timing characteristics for the LSB first mode are shown in Figure 30, and Figure 31 describe the MSB first mode. Table 7 shows the timing specifications.

Specification	Name	Min.	Max.	Units
sck period	tcyc	124		ns
sck pulse width low	tclkl	62		ns
sck pulse width high	tclkh	62		ns
si setup (write) from sck rising	trxs	10		ns
si hold (write) from sck rising	trxh	10		ns
so delay (read) from sck falling	txd		25	ns
cs_b setup from sck falling (LSB first)	tcssi	20		ns
cs_b setup from sck rising (MSB first)	tcssm	20		ns
cs_b hold from sck falling (MSB first)	tcshm	10		ns
cs_b hold from sck rising (LSB first)	tcshi	10		ns
cs_b to output high impedance	tohz		60	ns

Table 7 - Serial Peripheral Interface Timing

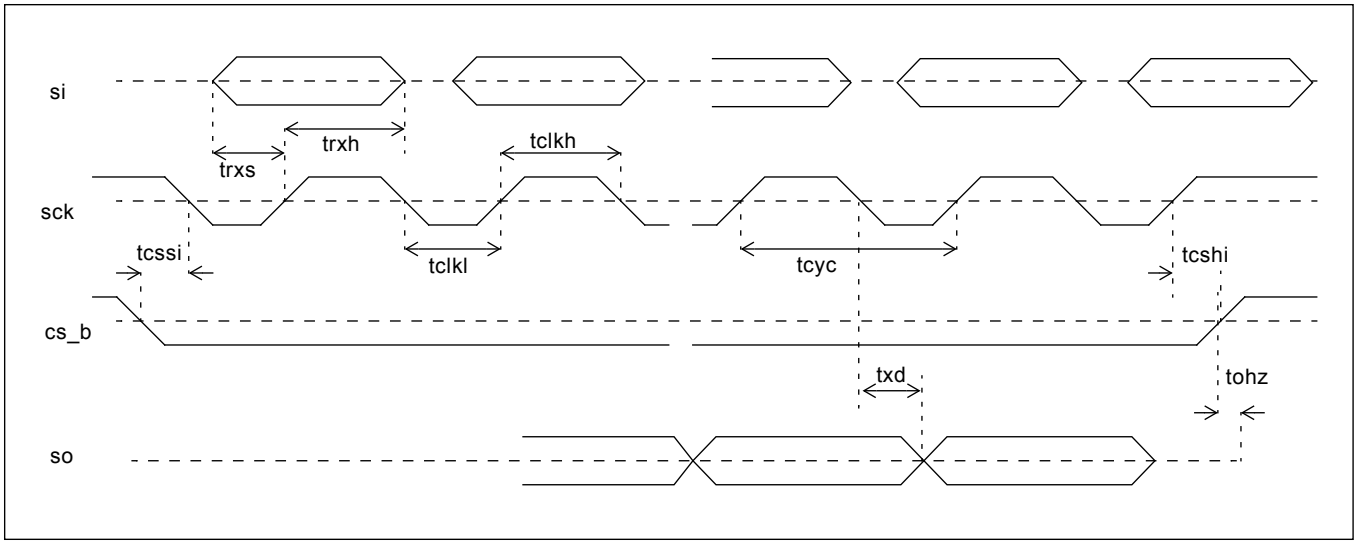


Figure 30 - Serial Peripheral Interface Timing - LSB First Mode

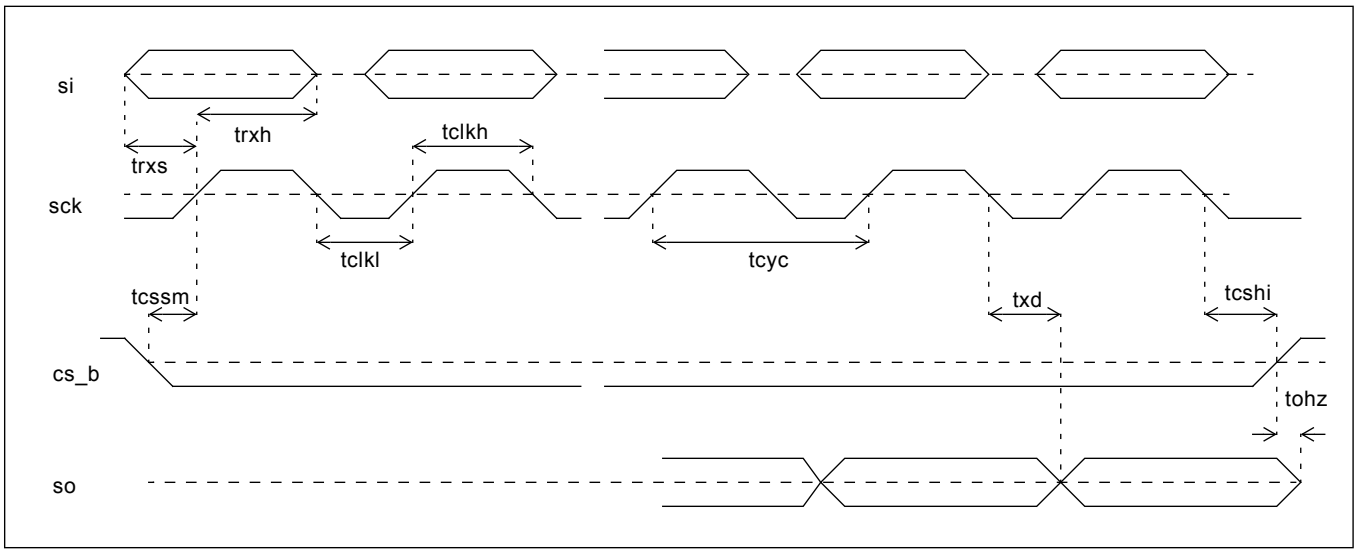


Figure 31 - Serial Peripheral Interface Timing - MSB First Mode

The timing specification for the I^2C interface is shown in Figure 32 and Table 8.

Specification	Name	Min.	Typ.	Max.	Units	Note
SCL clock frequency	f_{SCL}	0		400	kHz	
Hold time START condition	$t_{HD:STA}$	0.6			us	
Low period SCL	t_{LOW}	1.3			us	
Hi period SCL	t_{HIGH}	0.6			us	
Setup time START condition	$t_{SU:STA}$	0.6			us	
Data hold time	$t_{HD:DAT}$	0		0.9	us	
Data setup time	$t_{SU:DAT}$	100			ns	
Rise time	t_r				ns	Determined by choice of pull-up resistor
Fall time	t_f	20 + $0.1C_b$		250	ns	
Setup time STOP condition	$t_{SU:STO}$	0.6			us	
Bus free time between STOP/START	t_{BUF}	1.3			us	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0		50	ns	
Max capacitance for each I/O pin				10	pF	

Table 8 - I^2C Serial Microport Timing

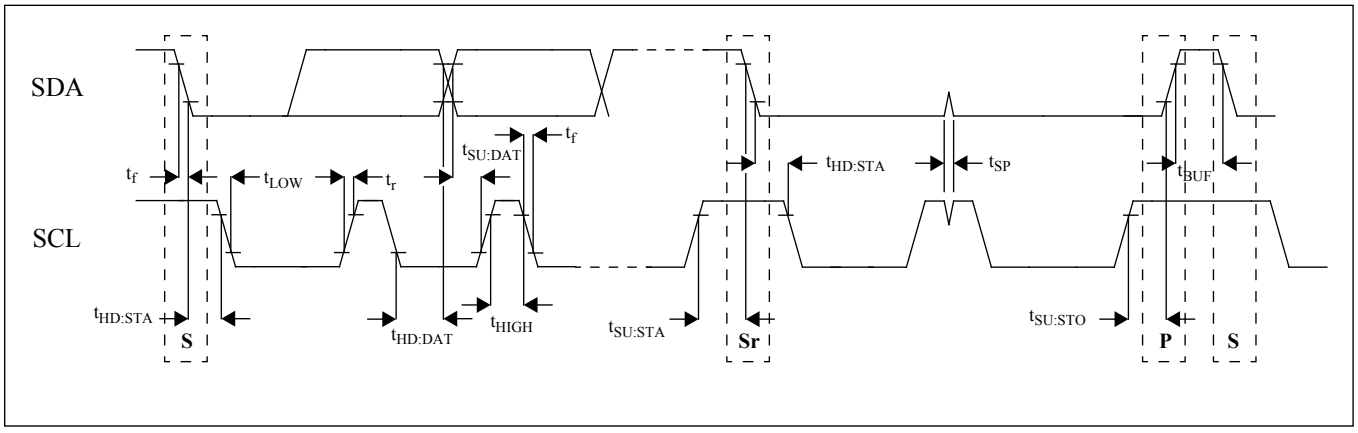


Figure 32 - I^2C Serial Microport Timing

10.0 Performance Characterization

10.1 Output Clocks Jitter Generation

Output Frequency	Jitter Measurement Filter	Max.	Units	Notes
622.08 MHz	50 kHz - 80 MHz	0.65	ps_{rms}	
	12 kHz - 20 MHz	0.77	ps_{rms}	

Table 9 - Jitter Generation Specifications - HPDIFF Outputs

Output Frequency	Jitter Measurement Filter	Max.	Units	Notes
25 MHz	12 kHz - 5 MHz	0.99	ps_{rms}	
77.76 MHz	12 kHz - 20 MHz	1.16	ps_{rms}	
125 MHz	12 kHz - 20 MHz	0.96	ps_{rms}	
156.25 MHz	12 kHz - 20 MHz	1.00	ps_{rms}	

Table 10 - Jitter Generation Specifications - HPOUT Outputs

10.2 DPLL Performance Characteristics

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Pull-in/Hold-in Range	+/-52		+/-3900	ppm	user selectable
2	Lock Time *			1	sec	
3	Reference Switching MTIE			5	nsec	
4	Entry into Holdover MTIE			5	nsec	
5	Exit from Holdover MTIE			5	nsec	
6	Holdover Accuracy			50	ppb	
7	Phase gain in the passband			0.1	dB	

* Lock time of 1 sec is achieved when pulling a 9.2ppm reference for any selected bandwidth and when phase slope limit is larger than 7.5 usec.

Table 11 - DPLL Characteristics

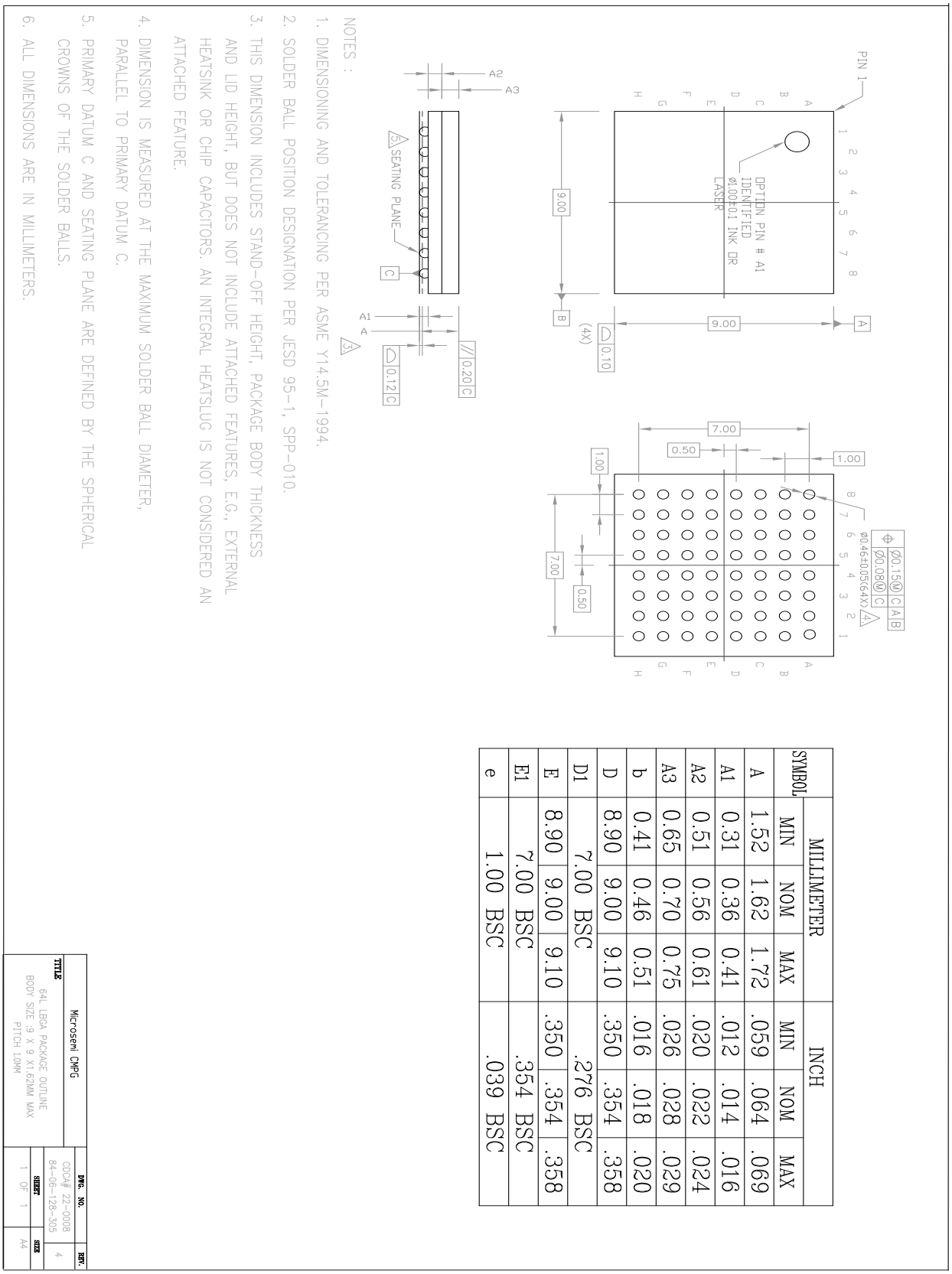
11.0 Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Junction to Ambient Thermal Resistance	θ_{ja}	Still Air 1 m/s 2 m/s	35.5 31.9 30.6	^{o}C/W
Junction to Case Thermal Resistance	θ_{jc}		8.3	^{o}C/W
Maximum Junction Temperature*	T_{jmax}		125	^{o}C
Maximum Ambient Temperature	T_A		85	^{o}C

* Proper thermal management must be practiced to ensure that T_{jmax} is not exceeded.

Table 12 - Thermal Data

12.0 Mechanical Drawing



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.52	1.62	1.72	.059	.064	.069
A1	0.31	0.36	0.41	.012	.014	.016
A2	0.51	0.56	0.61	.020	.022	.024
A3	0.65	0.70	0.75	.026	.028	.029
b	0.41	0.46	0.51	.016	.018	.020
D	8.90	9.00	9.10	.350	.354	.358
D1	7.00 BSC			.276 BSC		
E	8.90	9.00	9.10	.350	.354	.358
E1	7.00 BSC			.354 BSC		
e	1.00 BSC			.039 BSC		

NOTES :

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. SOLDER BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
3. THIS DIMENSION INCLUDES STAND-OFF HEIGHT, PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES, E.G., EXTERNAL HEATSINK OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AN ATTACHED FEATURE.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

Microsemi CMPG		DWG. NO.	REV.
TITLE: 64L LBGA PACKAGE OUTLINE BODY SIZE :9 X 9 X1.62MM MAX PITCH 1.0MM		CDCA# 22-0008 84-06-128-305	4
		SHEET 1 OF 1	SIZE A4

13.0 Package Markings

13.1 64-pin BGA. Package Top Mark Format

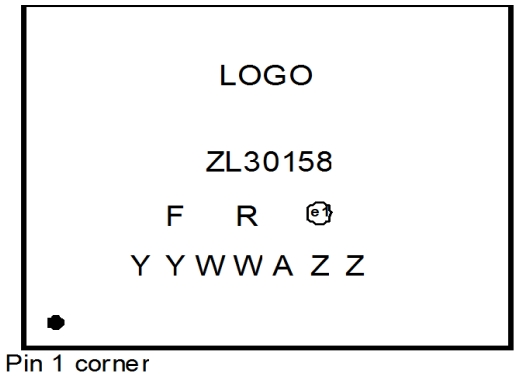


Figure 33 - Non-customized Device Top Mark

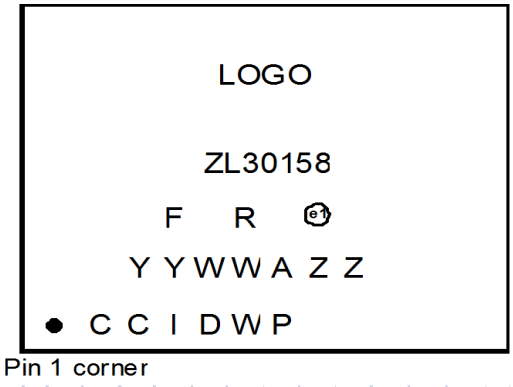


Figure 34 - Custom Factory Programmed Device Top Mark

Line	Characters	Description
1	ZL30158	Part Number
2	F	Fab Code
2	R	Product Revision Code
2	e1	Denotes Pb-Free Package
3	YY	Last Two Digits of the Year of Encapsulation
3	WW	Work Week of Assembly
3	A	Assembly Location Code
3	ZZ	Assembly Lot Sequence
4	CCID	Custom Programming Identification Code
4	WP	Work Week of Programming

Table 13 - Package Marking Legend



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