## Features

May 2009

- Synchronizes to 8 kHz, 2.048 MHz, 8.192 MHz or 16.384 MHz
- Provides a range of output clocks:
  - 65.536 MHz TDM clock locked to the input reference
  - General purpose 25 MHz fan-out to 6 outputs locked to the external crystal or oscillator
  - General purpose 125 MHz and 66 MHz or 100 MHz locked to the external crystal or oscillator
- Provides DPLL lock and reference fail indication
- Automatic free run mode on reference fail
- DPLL bandwidth of 922 Hz for all rates of input reference and 58 Hz for an 8 kHz input reference
- Less than 5 $psec_{rms}$ on 25 MHz outputs, and less than 0.6 $ns_{pp}$ intrinsic jitter on the all other outputs
- Minimal input to output and output to output skew
- 25 MHz external master clock source: clock oscillator or crystal
- Simple hardware control interface

**Ordering Information**

| | | |
|---|---|---|
| ZL30110LDE | 32 Pin QFN | Tubes, Bake & Dry Pack |
| ZL30110LDG1 | 32 Pin QFN* | Trays, Bake & Dry Pack |
| ZL30110LDF1 | 32 Pin QFN* | Tape & Reel |

*Pb Free Matte Tin

**-40°C to +85°C**

## Applications

- Clock rate conversion PLL for Telecommunication Equipment
- Small/Medium Enterprise Router / Gateway
- Broadband access (xPON/xDSL) CPE gateway

## Description

The ZL30110 clock rate conversion digital phase-locked loop (DPLL) provides accurate and reliable frequency conversion.

The ZL30110 generates a range of clocks that are either locked to the input reference or locked to the external crystal or oscillator.

In the locked mode, the reference input is continuously monitored for a failure condition. In the event of a failure, the DPLL continues to provide a stable free running clock ensuring system reliability.

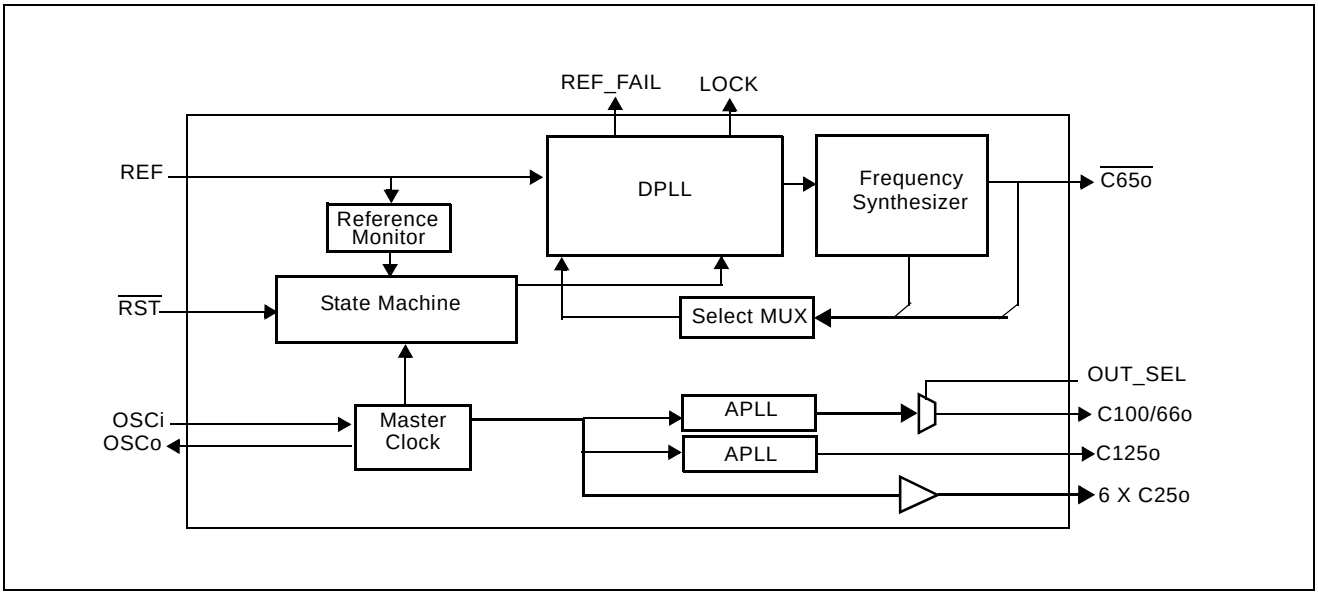



**Figure 1 - Functional Block Diagram**



Zarlink Semiconductor Inc.
Zarlink, ZL and the Zarlink Semiconductor logo are trademarks of Zarlink Semiconductor Inc.
Copyright 2006-2009, Zarlink Semiconductor Inc. All Rights Reserved.

## 1.0 Change Summary

The following table captures the changes from the April 2008 issue.

| Page | Item | Change |
|---|---|---|
| 1 | Ordering Information | Updates to Packaging Information. Added new packaging variants. Added Section 8.0. |

The following table captures the changes from the November 2006 issue.

| Page | Item | Change |
|---|---|---|
| 19 | “Performance Characteristics* - Unfiltered Jitter Generation - Pk-Pk“ | Made an addition to the table. |

## 2.0 Physical Description

### 2.1 Pin Connections

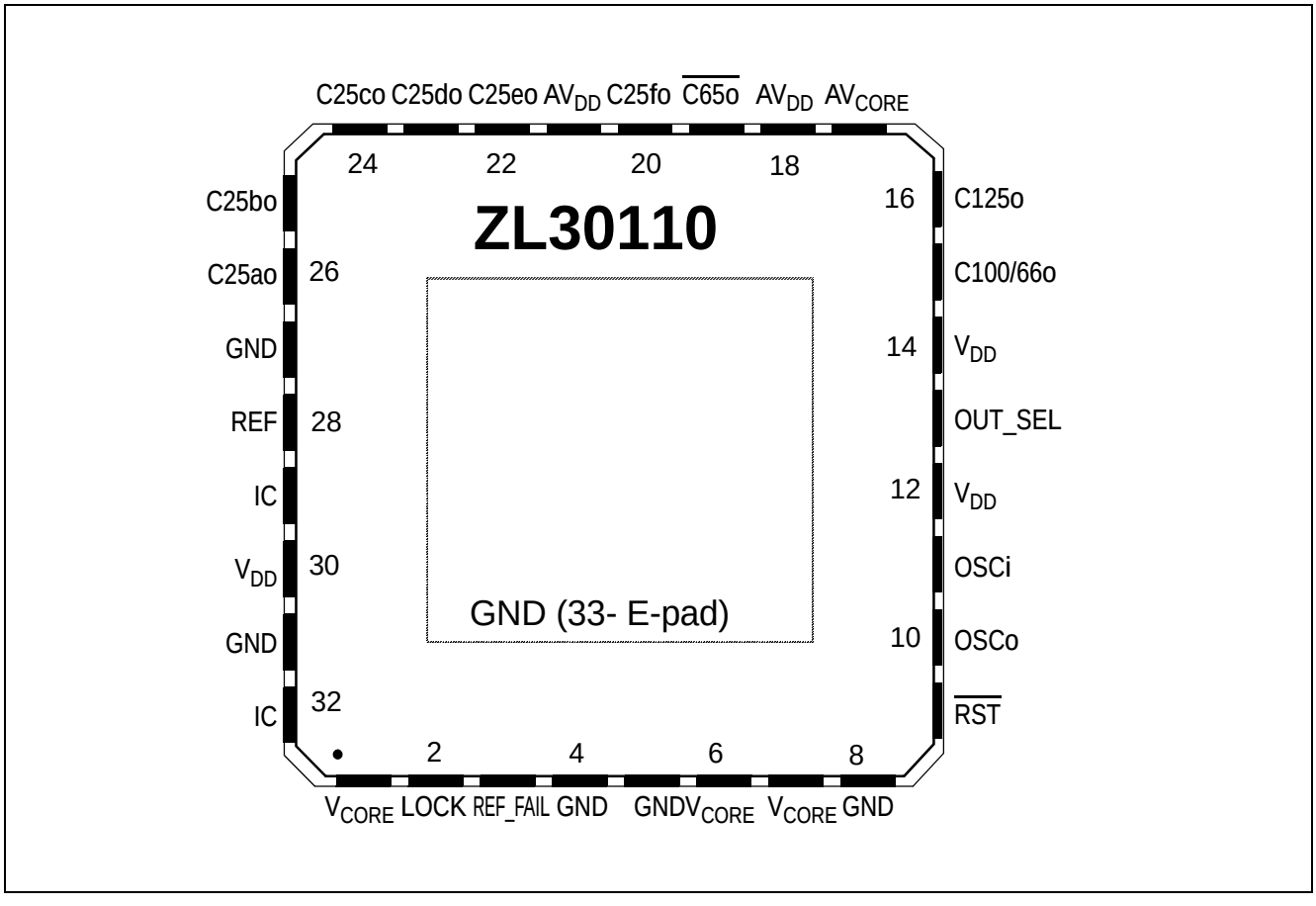



**Figure 2 - Pin Connections (32 pin 5 mm X 5 mm QFN with E-pad)**

# Table of Contents

**1.0 Change Summary . . . . . 2**
**2.0 Physical Description . . . . . 2**
2.1 Pin Connections . . . . . 2
2.2 Pin Description . . . . . 6
**3.0 Functional Description . . . . . 8**
3.1 Reference Monitor . . . . . 8
3.2 Digital Phase Lock Loop (DPLL) . . . . . 9
3.3 Frequency Synthesizers . . . . . 9
3.4 State Machine . . . . . 9
3.5 APLL . . . . . 9
3.6 Master Clock . . . . . 9
**4.0 DPLL Modes of Operation . . . . . 10**
4.1 Freerun Mode . . . . . 10
4.2 Normal Mode . . . . . 10
**5.0 Measures of Performance . . . . . 11**
5.1 Jitter . . . . . 11
5.2 Jitter Generation (Intrinsic Jitter) . . . . . 11
5.3 Jitter Transfer . . . . . 11
5.4 Lock Time . . . . . 11
**6.0 Applications . . . . . 12**
6.1 Power Supply Decoupling . . . . . 12
6.2 Master Clock . . . . . 12
6.2.1 Clock Oscillator . . . . . 12
6.2.2 Crystal Oscillator . . . . . 13
6.3 Power Up Sequence . . . . . 14
6.4 Reset Circuit . . . . . 14
**7.0 Characteristics . . . . . 15**
7.1 AC and DC Electrical Characteristics . . . . . 15
7.2 Performance Characteristics . . . . . 18
**8.0 Packaging Information . . . . . 19**

# List of Figures

Figure 1 - Functional Block Diagram . . . . . 1
Figure 2 - Pin Connections (32 pin 5 mm X 5 mm QFN with E-pad) . . . . . 2
Figure 3 - Reference Monitor Circuit . . . . . 8
Figure 4 - DPLL Mode Switching . . . . . 10
Figure 5 - Clock Oscillator Circuit. . . . . 12
Figure 6 - Power-Up Reset Circuit . . . . . 14
Figure 7 - Timing Parameter Measurement Voltage Levels . . . . . 16
Figure 8 - Input to Output Timing for Synchronous Clock . . . . . 17
Figure 9 - Asynchronous Clocks Input to Output Timing . . . . . 18

# List of Tables

Table 1 - Clock Oscillator Specification . . . . . 12
Table 2 - Crystal Oscillator Specification . . . . . 13

## 2.2 Pin Description

| Pin # | Name | I/O Type | Description |
|---|---|---|---|
| **Input Reference** | | | |
| 28 | REF | I | **Reference (LVCMOS, Schmitt Trigger).** This is the input reference source used for synchronization. One of four possible frequencies may be used: 8 kHz, 2.048 MHz, 8.192 MHz or 16.384 MHz. This pin is internally pulled down to GND. |
| **Master Clock** | | | |
| 11 | OSCi | I | **Oscillator Master Clock (Input).** For crystal operation, a 25 MHz crystal is connected from this pin to OSCo. For clock oscillator operation, this pin must be connected to a clock source. |
| 10 | OSCo | O | **Oscillator Master Clock (LVCMOS).** For crystal operation, a 25 MHz crystal is connected from this pin to OSCi. This output is not suitable for driving other devices (see C25o output pin for support of such function). For clock oscillator operation, this pin must be left unconnected. |
| **Control and Status** | | | |
| 9 | $\overline{\text{RST}}$ | I | **Reset (LVCMOS, Schmitt Trigger).** A logic low at this input resets the device. On power up, the $\overline{\text{RST}}$ pin must be held low for a minimum of 300 ns after the power supply pins have reached the minimum supply voltage. When the $\overline{\text{RST}}$ pin goes high, the device will transition into a Reset state for 3 ms. In the Reset state all outputs will be forced into high impedance. |
| 13 | OUT_SEL | I | **Output Select (LVCMOS, Schmitt Trigger).** This input pin selects the output clock frequency of the C100/66o, a logic low selects the 100 MHz output, while logic high selects the 66 MHz output clock. |
| 3 | REF_FAIL | O | **Reference Failure Indicator (LVCMOS).** A logic high at this pin indicates that the REF reference frequency is exhibiting abrupt phase or frequency change. |
| 2 | LOCK | O | **Lock Indicator (LVCMOS).** This output goes to a logic high when the PLL is frequency locked to a valid input reference. |
| **Output Clocks** | | | |
| 19 | $\overline{\text{C65o}}$ | O | **Clock 65.536 MHz (LVCMOS).** This output is used in general TDM applications. The falling edge of this clock is aligned with rising edge of the input reference (REF). |
| 26 | C25ao | O | **Clock 25 MHz (LVCMOS).** This is a buffered external oscillator clock, the phase and frequency accuracy of this output tracks that of the external crystal or oscillator. |
| 25 | C25bo | O | **Clock 25 MHz (LVCMOS).** This is a buffered external oscillator clock, the phase and frequency accuracy of this output tracks that of the external crystal or oscillator. |
| 24 | C25co | O | **Clock 25 MHz (LVCMOS).** This is a buffered external oscillator clock, the phase and frequency accuracy of this output tracks that of the external crystal or oscillator. |
| 23 | C25do | O | **Clock 25 MHz (LVCMOS).** This is a buffered external oscillator clock, the phase and frequency accuracy of this output tracks that of the external crystal or oscillator. |

| Pin # | Name | I/O Type | Description |
|---|---|---|---|
| 22 | C25eo | O | **Clock 25 MHz (LVCMOS).** This is a buffered external oscillator clock, the phase and frequency accuracy of this output tracks that of the external crystal or oscillator. |
| 20 | C25fo | O | **Clock 25 MHz (LVCMOS).** This is a buffered external oscillator clock, the phase and frequency accuracy of this output tracks that of the external crystal or oscillator. |
| 15 | C100/66o | O | **Clock 100 MHz or 66 MHz (LVCMOS).** This is 100 MHz or 66 MHz rate converted clocks off the 25 MHz fixed frequency external oscillator, the phase and frequency accuracy of this output tracks that of the external crystal or oscillator device. |
| 16 | C125o | O | **Clock 125 MHz (LVCMOS).** This is 125 MHz rate converted clock off the 25 MHz fixed frequency external oscillator, the phase and frequency accuracy of this output tracks that of the external crystal or oscillator device. |
| **Miscellaneous** | | | |
| 29 | IC | | **Internal Connection.** Connect to VDD. |
| 32 | IC | | **Internal Connection.** Connect to VDD. |
| **Power and Ground** | | | |
| 12 | $V_{DD}$ | | **Positive Supply Voltage.** +3.3 $V_{DC}$ nominal. |
| 14 | $V_{DD}$ | | **Positive Supply Voltage.** +3.3 $V_{DC}$ nominal. |
| 30 | $V_{DD}$ | | **Positive Supply Voltage.** +3.3 $V_{DC}$ nominal. |
| 1 | $V_{CORE}$ | | **Positive Supply Voltage.** +1.8 $V_{DC}$ nominal. |
| 6 | $V_{CORE}$ | | **Positive Supply Voltage.** +1.8 $V_{DC}$ nominal. |
| 7 | $V_{CORE}$ | | **Positive Supply Voltage.** +1.8 $V_{DC}$ nominal. |
| 17 | $AV_{CORE}$ | | **Positive Analog Supply Voltage.** +1.8 $V_{DC}$ nominal. |
| 18 | $AV_{DD}$ | | **Positive Analog Supply Voltage.** +3.3 $V_{DC}$ nominal. |
| 21 | $AV_{DD}$ | | **Positive Analog Supply Voltage.** +3.3 $V_{DC}$ nominal. |
| 4 | GND | | **Ground.** 0 V. |
| 5 | GND | | **Ground.** 0 V. |
| 8 | GND | | **Ground.** 0 V. |
| 27 | GND | | **Ground.** 0 V. |
| 31 | GND | | **Ground.** 0 V. |
| 33 E-pad | GND | | **Internal Connection.** Package E-pad, this pin is internally connected to device GND, it should be connected to GND. |

# 3.0 Functional Description

## 3.1 Reference Monitor

The input reference is monitored by two reference monitor blocks. The block diagram of reference monitoring is shown in Figure 3. The reference frequency is detected and the clock is continuously monitored for two independent criteria that indicate abnormal behavior of the reference signal, for example; loss of clock or excessive level of frequency error. To ensure proper operation of the reference monitor circuit, the minimum input pulse width restriction of 15 nsec must be observed.

- **Reference Frequency Detector (RFD)**: This detector determines whether the frequency of the reference clock is 8 kHz, 2.048 MHz, 8.192 MHz or 16.384 MHz and provides this information to the various monitor circuits and the phase detector circuit of the DPLL.
- **Coarse Frequency Monitor (CFM)**: This circuit monitors the reference frequency over intervals of approximately 30 μs to quickly detect large frequency changes.
- **Single Cycle Monitor (SCM)**: This detector checks the period of a single clock cycle to detect large phase hits or the complete loss of the clock.

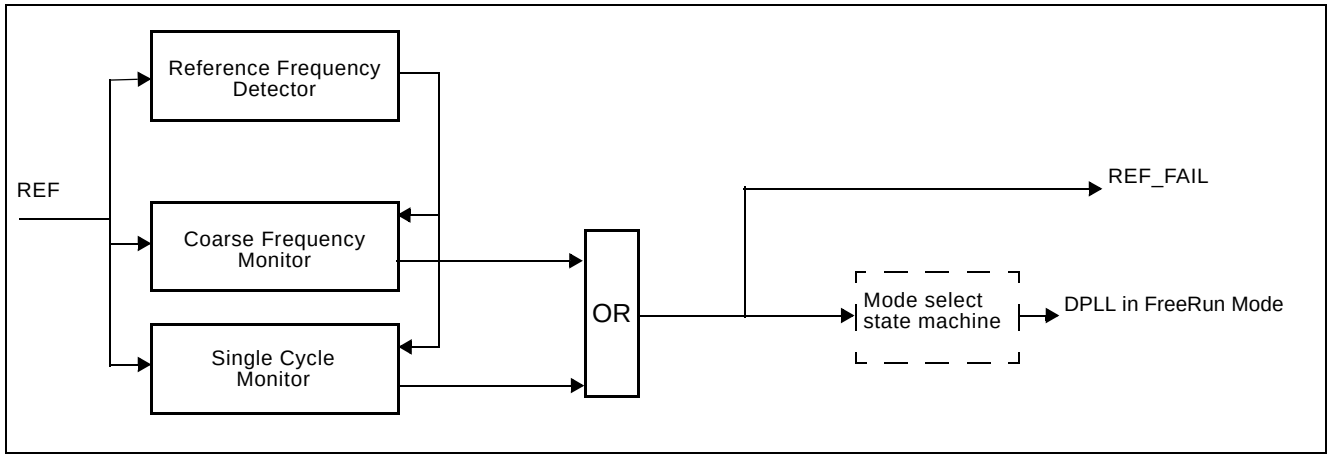



**Figure 3 - Reference Monitor Circuit**

Exceeding the thresholds of any of the monitors forces the corresponding REF_FAIL pin to go high. The single cycle and coarse frequency failure flags force the DPLL into FreeRun mode.

## 3.2 Digital Phase Lock Loop (DPLL)

The DPLL of the ZL30110 consists of a phase detector, a loop filter and a digitally controlled oscillator.

**Phase Detector** - the phase detector compares the input reference signal to the feedback signal and provides an error signal corresponding to the phase difference between the two.

**Loop Filter** - the loop filter is similar to a first order low pass filter with a bandwidth of 922 Hz. For stability reasons, the loop filter bandwidth for an 8 kHz reference is limited to a maximum of 58 Hz.

**Digitally Controlled Oscillator (DCO)** - the DCO receives the filtered signal from the Loop Filter, and based on its value, generates a corresponding digital output signal. The synchronization method of the DCO is dependent on the state of the ZL30110.

In Normal Mode, the DCO provides an output signal which is frequency and phase locked to the selected input reference signal.

In Freerun Mode, the DCO is free running with an accuracy equal to the accuracy of the OSCi 25 MHz source.

**Lock Indicator** - the lock detector monitors if the output value of the phase detector is within the phase-lock-window for a certain time. The selected phase-lock-window guarantees the stable operation of the LOCK pin with maximum network jitter and wander on the reference input. If the DPLL goes into FreeRun mode, the LOCK pin will initially stay high for 0.1 s. If at that point the DPLL is still in FreeRun mode, the LOCK pin will go low. In Freerun mode the LOCK pin will go low immediately.

## 3.3 Frequency Synthesizers

The output of the DCO is used by the frequency synthesizer to generate the output clock which is synchronized to the inputs (REF). The frequency synthesizer uses digital techniques to generate output clock and advanced noise shaping techniques to minimize the output jitter. The clock and frame pulse outputs have limited driving capability and should be buffered when driving high capacitance loads.

## 3.4 State Machine

As shown in Figure 1, the state machine controls the DPLL.

## 3.5 APLL

The ZL30110 employ two Analog PLLs as a clock multiplying and rate conversion engine. One APLL is used to multiply the master clock (OSCi) to 125 MHz, a second APLL is used to convert the master clock (OSCi) to 100 MHz or 66 MHz clock.

## 3.6 Master Clock

The ZL30110 can use either a clock or crystal as the master timing source. For recommended master timing circuits, see the Applications - Master Clock section.

## 4.0 DPLL Modes of Operation

The ZL30110 has two possible modes of operation; Normal, and Freerun. The ZL30110 starts up in Freerun mode, it automatically transitions to Normal mode if a valid reference is available and transitions to Freerun mode if the reference fails.

### 4.1 Freerun Mode

Freerun mode is typically used when an independent clock source is required or immediately following system power-up before synchronization is achieved.

In Freerun mode, the ZL30110 provides timing and synchronization signals which are based on the master clock frequency (supplied to OSCi pin) only and are not synchronized to the reference input signals.

The accuracy of the output clock is equal to the accuracy of the master clock (OSCi). So if a ±32 ppm output clock is required, the master clock must also be ±32 ppm. See Applications - Section 6.2, “Master Clock“.

Freerun Mode is also used for short durations while system synchronization is temporarily disrupted. The accuracy of the output clock during these input reference disruptions is better than the accuracy of the master clock (OSCi), but it is off compared to the reference before disruptions.

### 4.2 Normal Mode

Normal mode is typically used when a system clock source, synchronized to the network is required. In Normal mode, the ZL30110 provides timing synchronization signals, which are synchronized to the input (REF). The input reference signal may have a nominal frequency of 8 kHz, 2.048 MHz, 8.192 MHz or 16.384 MHz. The frequency of the reference inputs are automatically detected by the reference monitors.

When the ZL30110 comes out of RESET it will initially go into Freerun mode and generate a clock with the accuracy of its freerunning local oscillator (see Figure 4). If the ZL30110 determines that its selected reference is disrupted (see Figure 3), it will remain in Freerun until the selected reference is no longer disrupted. If the ZL30110 determines that the reference is not disrupted (see Figure 3) then the state machine will cause the DPLL to recover from Freerun and transition to Normal mode.

When the ZL30110 is operating in Normal mode, if it determines that the input reference is disrupted (Figure 3) then its state machine will cause it to automatically go to Freerun mode. When the ZL30110 determines that its selected reference is not disrupted then the state machine will cause the DPLL to recover from Freerun and transition to Normal mode.

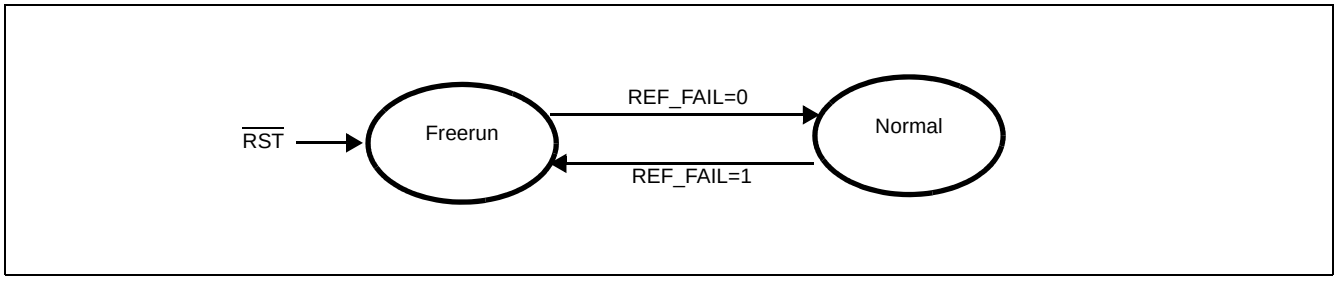



**Figure 4 - DPLL Mode Switching**

# 5.0 Measures of Performance

The following are some PLL performance indicators and their corresponding definitions.

## 5.1 Jitter

Timing jitter is defined as the high frequency variation of the clock edges from their ideal positions in time. Wander is defined as the low-frequency variation of the clock edges from their ideal positions in time. High and low frequency variation imply phase oscillation frequencies relative to some demarcation frequency. (Often 10 Hz or 20 Hz for DS1 or E1, higher for SONET/SDH clocks.) Jitter parameters given in this data sheet are total timing jitter numbers, not cycle-to-cycle jitter.

## 5.2 Jitter Generation (Intrinsic Jitter)

Jitter generation is the measure of the jitter produced by the PLL and is measured at its output. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Jitter is usually measured with various band limiting filters depending on the applicable standards.

## 5.3 Jitter Transfer

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

## 5.4 Lock Time

This is the time it takes the PLL to frequency lock to the input signal. Phase lock occurs when the input signal and output signal are aligned in phase with respect to each other within a certain phase distance (not including jitter). Lock time is affected by many factors which include:

- initial input to output phase difference
- initial input to output frequency difference
- PLL loop filter bandwidth

The presence of input jitter makes it difficult to define when the PLL is locked as it may not be able to align its output to the input within the required phase distance, dependent on the PLL bandwidth and the input jitter amplitude and frequency.

## 6.0 Applications

This section contains ZL30110 application specific details for power supply decoupling, reset operation, clock and crystal operation.

### 6.1 Power Supply Decoupling

Jitter levels on the ZL30110 output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the ZL30110 device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins. For recommended common layout practices, refer to Zarlink Application Note ZLAN-178.

### 6.2 Master Clock

The ZL30110 can use either a clock or crystal as the master timing source.

#### 6.2.1 Clock Oscillator

When selecting a clock oscillator, numerous parameters must be considered. This includes absolute frequency, frequency change over temperature, output rise and fall times, output levels, duty cycle and phase noise.

The output clock should be connected directly (not AC coupled) to the OSCi input of the ZL30110, and the OSCo output should be left open as shown in Figure 5.

| | | |
|---|---|---|
| 1 | Frequency | 25 MHz |
| 2 | Tolerance | as required (better than +/-50ppm) |
| 3 | Rise & fall time | < 8 ns |
| 4 | Duty cycle | 40% to 60% |

**Table 1 - Clock Oscillator Specification**

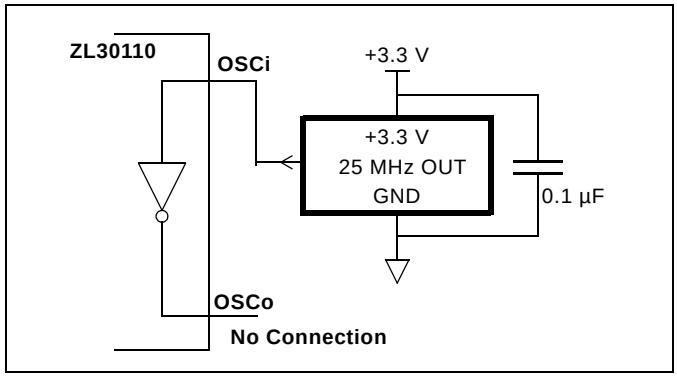



**Figure 5 - Clock Oscillator Circuit**

### 6.2.2 Crystal Oscillator

Alternatively, a Crystal Oscillator may be used. The accuracy of a crystal oscillator depends on the crystal tolerance as well as the load capacitance tolerance. Typically, for a 25 MHz crystal specified with a 32 pF load capacitance, each 1 pF change in load capacitance contributes approximately 9 ppm to the frequency deviation. Consequently, capacitor tolerances and stray capacitances have a major effect on the accuracy of the oscillator frequency.

The crystal should be a fundamental mode type - not an overtone. The fundamental mode crystal permits a simpler oscillator circuit with no additional filter components and is less likely to generate spurious responses. A typical crystal oscillator specification is shown in Table 2.

| | | |
|---|---|---|
| 1 | Frequency | 25 MHz |
| 2 | Tolerance | as required (better than +/-50ppm) |
| 3 | Oscillation mode | fundamental |
| 4 | Resonance mode | parallel |
| 5 | Load capacitance | as required |
| 6 | Maximum series resistance | 50 Ω |

**Table 2 - Crystal Oscillator Specification**

## 6.3 Power Up Sequence

The ZL30110 requires that the 3.3 V supply is not powered up after the 1.8 V supply. This is to prevent the risk of latch-up due to the presence of protection diodes in the IO pads.

Two options are given:

1. Power-up the 3.3 V supply fully first, then power up the 1.8 V supply

2. Power up the 3.3 V supply and the 1.8 V supply simultaneously, ensuring that the 3.3 V supply is never lower than a few hundred millivolts below the 1.8 V supply (e.g., by using a schottky diode or controlled slew rate)

## 6.4 Reset Circuit

A simple power up reset circuit with about a 60 μs reset low time is shown in Figure 6. Resistor $R_P$ is for protection only and limits current into the $\overline{RST}$ pin during power down conditions. The reset low time is not critical but should be greater than 300 ns.

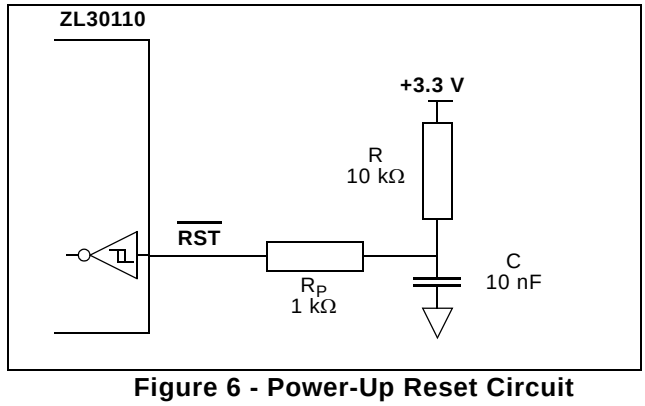



**Figure 6 - Power-Up Reset Circuit**

# 7.0 Characteristics

## 7.1 AC and DC Electrical Characteristics

**Absolute Maximum Ratings***

| | Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|---|
| 1 | Supply voltage | $V_{DD_R}$ | -0.5 | 4.6 | V |
| 2 | Core supply voltage | $V_{CORE_R}$ | -0.5 | 2.5 | V |
| 3 | Voltage on any digital pin | $V_{PIN}$ | -0.5 | 6 | V |
| 4 | Voltage on OSCi and OSCo pin | $V_{OSC}$ | -0.3 | $V_{DD}$ + 0.3 | V |
| 5 | Current on any pin | $I_{PIN}$ | | 30 | mA |
| 6 | Storage temperature | $T_{ST}$ | -55 | 125 | °C |
| 7 | ESD rating | $V_{ESD}$ | | 2k | V |

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated.

**Recommended Operating Conditions***

| | Characteristics | Sym. | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| 1 | Supply voltage | $V_{DD}$ | 3.1 | 3.3 | 3.5 | V |
| 2 | Core supply voltage | $V_{CORE}$ | 1.7 | 1.8 | 1.9 | V |
| 3 | Operating temperature | $T_A$ | -40 | 25 | 85 | °C |
| 4 | Input Voltage | $V_I$ | 0 | 3.3 | 3.5 | V |

* Voltages are with respect to ground (GND) unless otherwise stated.

**DC Electrical Characteristics***

| | Characteristics | Sym. | Min. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 1 | Supply current | $I_{DD}$ | | 115 | mA | All Outputs loaded with 30 pf |
| 2 | Core supply current | $I_{CORE}$ | | 20 | mA | All Outputs loaded with 30 pf |
| 3 | Schmitt trigger Low to High threshold point | $V_{CIH}$ | 1.43 | 1.85 | V | |
| 4 | Schmitt trigger High to Low threshold point | $V_{CIL}$ | 0.8 | 1.1 | V | |
| 5 | Input leakage current | $I_{IL}$ | -105 | 105 | µA | $V_I$=$V_{DD}$ or 0 V |

**DC Electrical Characteristics***

| | Characteristics | Sym. | Min. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 6 | High-level output voltage | $V_{OH}$ | 2.4 | | V | $I_{OH}$ = 8 mA for clock outputs, 4 mA for status outputs |
| 7 | Low-level output voltage | $V_{OL}$ | | 0.4 | V | $I_{OL}$ = 8 mA for clock outputs, 4 mA for status outputs |

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated.

**AC Electrical Characteristics* - Timing Parameter Measurement Voltage Levels (see Figure 7).**

| | Characteristics | Sym. | CMOS | Units |
|---|---|---|---|---|
| 1 | Threshold Voltage | $V_T$ | $0.5xV_{DD}$ | V |
| 2 | Rise and Fall Threshold Voltage High | $V_{HM}$ | $0.7xV_{DD}$ | V |
| 3 | Rise and Fall Threshold Voltage Low | $V_{LM}$ | $0.3xV_{DD}$ | V |

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated.

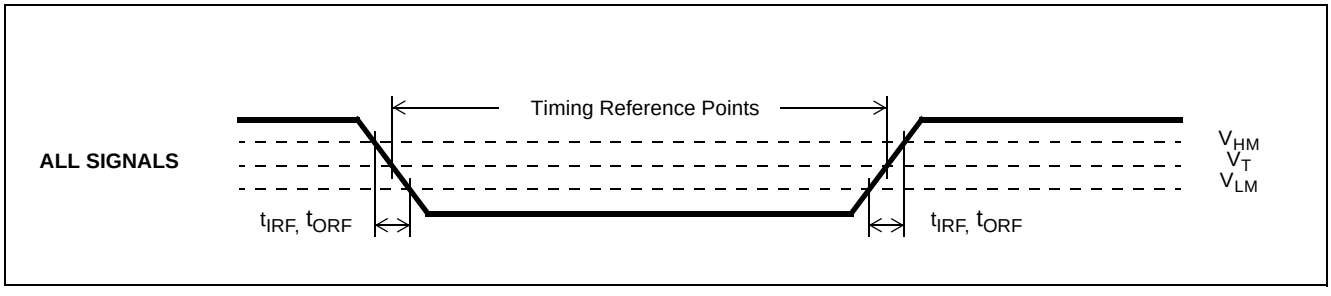



**Figure 7 - Timing Parameter Measurement Voltage Levels**

**AC Electrical Characteristics* - Timing for input reference (see Figure 8).**

| | Characteristics | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| 1 | 8 kHz reference period | $t_{REF8kP}$ | 120 | 125 | 128 | µs |
| 2 | 2.048 MHz reference period | $t_{REF2P}$ | 263 | 488 | 712 | ns |
| 3 | 8.192 MHz reference period | $t_{REF8P}$ | 63 | 122 | 175 | ns |
| 4 | 16.384 MHz reference period | $t_{REF16P}$ | 38 | 61 | 75 | ns |
| 5 | reference pulse width high or low | $t_{REFW}$ | 15 | | | ns |

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Period Min/Max values are the limits to avoid a single-cycle fault detection. Short-term and long-term average periods must be within +/-130 ppm limit.

**AC Electrical Characteristics* - Input to output timing for synchronous clock (see Figure 8).**

| | Characteristics | Symbol | Min. | Max. | Units |
|---|---|---|---|---|---|
| 1 | 8 kHz reference input to $\overline{C65o}$ delay | $t_{REF8_C65D}$ | -0.7 | 6.7 | ns |
| 2 | 2.048 MHz reference input to $\overline{C65o}$ delay | $t_{REF2_C65D}$ | 1.5 | 9.6 | ns |
| 3 | 8.192 MHz reference input to $\overline{C65o}$ delay | $t_{REF8_C65D}$ | 2.1 | 9.2 | ns |
| 4 | 16.384 MHz reference input to $\overline{C65o}$ delay | $t_{REF16_C65D}$ | 2.1 | 9.6 | ns |
| 5 | $\overline{C65o}$ pulse width low | $t_{C65L}$ | 7.0 | 8.6 | ns |
| 6 | Output clock rise or fall time | $t_{ORF}$ | 1.1 | 2.3 | ns |

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
Outputs loaded with 30 pF.

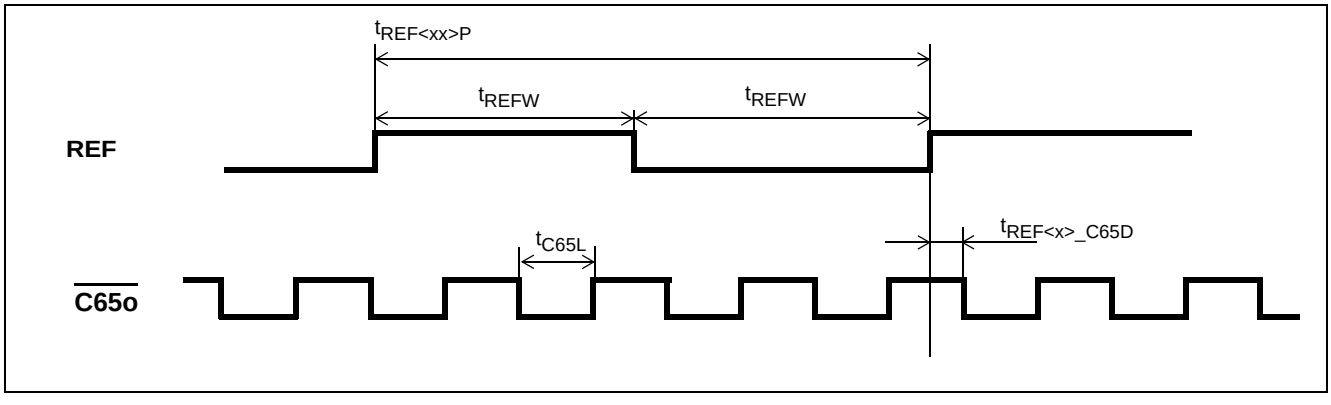



**Figure 8 - Input to Output Timing for Synchronous Clock**

**AC Electrical Characteristics* - Input to output timing for Asynchronous clocks (see Figure 9).**

| | Characteristics | Symbol | Min. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 1 | 25 MHz master clock input to C25a/b/c/d/e/fo delay | $t_{M_C25D}$ | 3 | 14 | ns | |

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

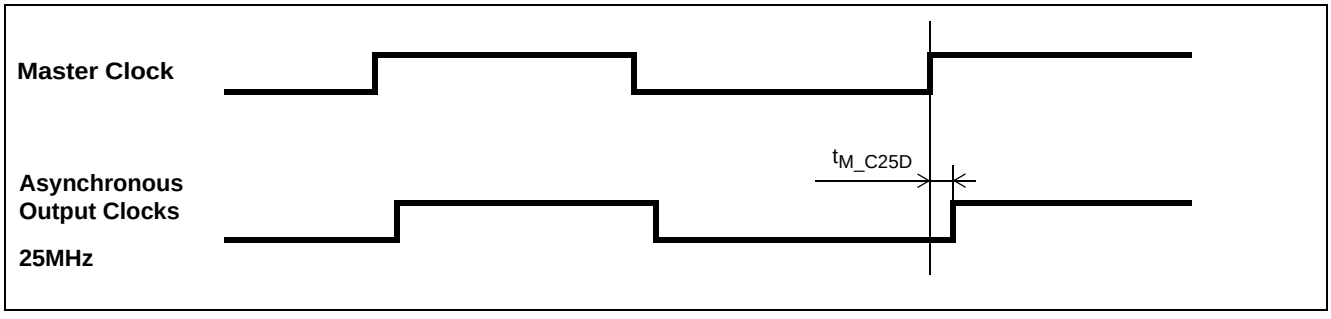



**Figure 9 - Asynchronous Clocks Input to Output Timing**

**AC Electrical Characteristics* - Output timing for Asynchronous clocks (see Figure 9).**

| | Characteristics | Symbol | Min. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 1 | C25a/b/c/d/e/fo pulse width low** | $t_{C25L}$ | 18 | 22 | ns | 30 pF output load |
| 2 | C125o pulse width low | $t_{C125L}$ | 3.2 | 4.6 | ns | 25 pF output load |
| 3 | C100o pulse width low | $t_{C100L}$ | 4.1 | 5.6 | ns | 30 pF output load |
| 4 | C66o pulse width low | $t_{C66L}$ | 6.8 | 8.0 | ns | 30 pF output load |

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
** Buffered OSCi clock input, characterization data did not account for input clock duty cycle nor rise/fall time degradation.

## 7.2 Performance Characteristics

**Performance Characteristics* - Functional**

| | Characteristics | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 1 | DPLL capture range | -130 | | +130 | ppm | The 25 MHz Master Clock oscillator set at 0.ppm |
| **Lock Time** | | | | | | |
| 2 | DPLL 58 Hz Filter | | | 1 | s | input reference = 8 kHz, ±100 ppm frequency offset |
| 3 | DPLL 922 Hz Filter | | | 1 | s | input reference ≠ 8 kHz, ±100 ppm frequency offset |
| 4 | APLL 450 kHz Filter | | | 150 | µs | |

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

**Performance Characteristics* - Unfiltered Jitter Generation - Pk-Pk**

| | Characteristics | Max. [$ns_{pp}$] | Notes |
|---|---|---|---|
| 1 | $\overline{C65o}$ (65.536 MHz) | 0.60 | |
| 2 | $\overline{C65o}$ (65.536 MHz) | 0.30 | cycle-to-cycle |
| 3 | C25a/b/c/d/e/fo (25 MHz) | 0.20 | |
| 4 | C125o (125 MHz) | 0.54 | |
| 5 | C100o (100 MHz) | 0.60 | |
| 6 | C66o (66 MHz) | 0.60 | |

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

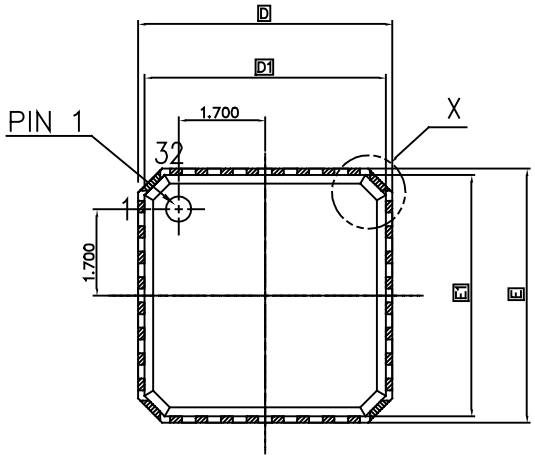
**Performance Characteristics* - Filtered Jitter Generation - RMS**

| | Characteristics | Max. [$ps_{rms}$] | Notes |
|---|---|---|---|
| 1 | C25a/b/c/d/e/fo (25 MHz) - (625 kHz - Nyquist) | 4 | |
| 2 | C125o (125 MHz) (625 kHz - Nyquist) | 20 | |

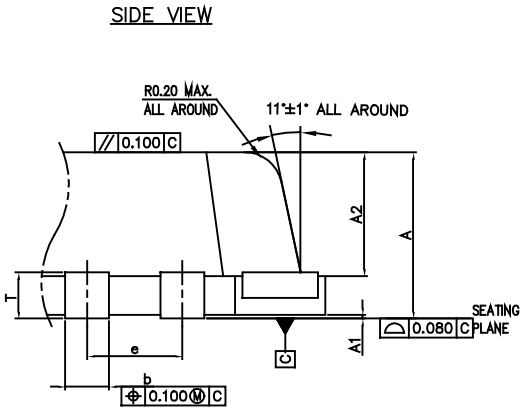
* Supply voltage and operating temperature are as per Recommended Operating Conditions.

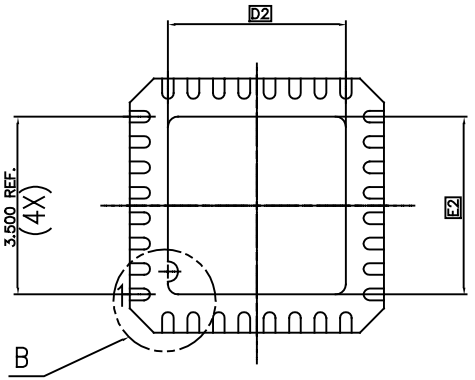
## 8.0 Packaging Information

| Part Number | Package Drawing Number |
|---|---|
| ZL30110LDE | 103364 |
| ZL30110LDG1<br>ZL30110LDF1 | 22-0005 |




TOP VIEW

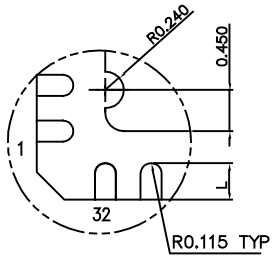


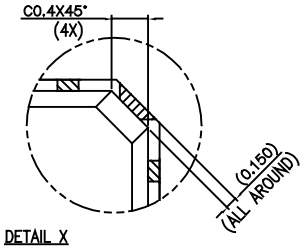

BOTTOM VIEW

| S/N | SYM | DIMENSIONS | REMARKS |
|---|---|---|---|
| 1 | A | 0.850±0.050 | OVERALL HEIGHT |
| 2 | A1 | 0.025±0.020 | STANDOFF |
| 3 | A2 | 0.650±0.050 | CAVITY THICKNESS |
| 4 | D | 5.000±0.100 | PKG. LENGTH |
| 5 | D1 | 4.750±0.100 | CAVITY LENGTH |
| 6 | D2 | 3.500±0.050 | EXPOSED PAD LENGTH |
| 7 | E | 5.000±0.100 | PKG. WIDTH |
| 8 | E1 | 4.750±0.100 | CAVITY WIDTH |
| 9 | E2 | 3.500±0.050 | EXPOSED PAD WIDTH |
| 10 | L | 0.400±0.100 | FOOT LENGTH |
| 11 | T | 0.190~0.245 | FRAME THICKNESS |
| 12 | b | 0.230 $^{+0.070}_{-0.050}$ | LEAD WIDTH |
| 13 | e | 0.500 BASE | LEAD PITCH |

COMPLIANT TO JEDEC STANDARD: MO-220




DETAIL B




DETAIL X

## NOTES:

1. DIMENSIONS & TOLERANCES CONFORM TO ASME Y14.5M, – 1994
2. PIN 1 IDENTIFIER MUST BE ON THE TOP SURFACE OF THE PACKAGE USING AN INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. PACKAGE WARPAGE MAX 0.08 mm.
5. NOT TO SCALE.
6. DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION

© Zarlink Semiconductor 2003 All rights reserved.

| ISSUE | 1 | 2 | 3 | |
|---|---|---|---|---|
| ACN | CDCA | CDCA | CDCA | |
| DATE | 30-01-2004 | 15-08-2005 | 22-08-2005 | |
| APPRD. | | | | |

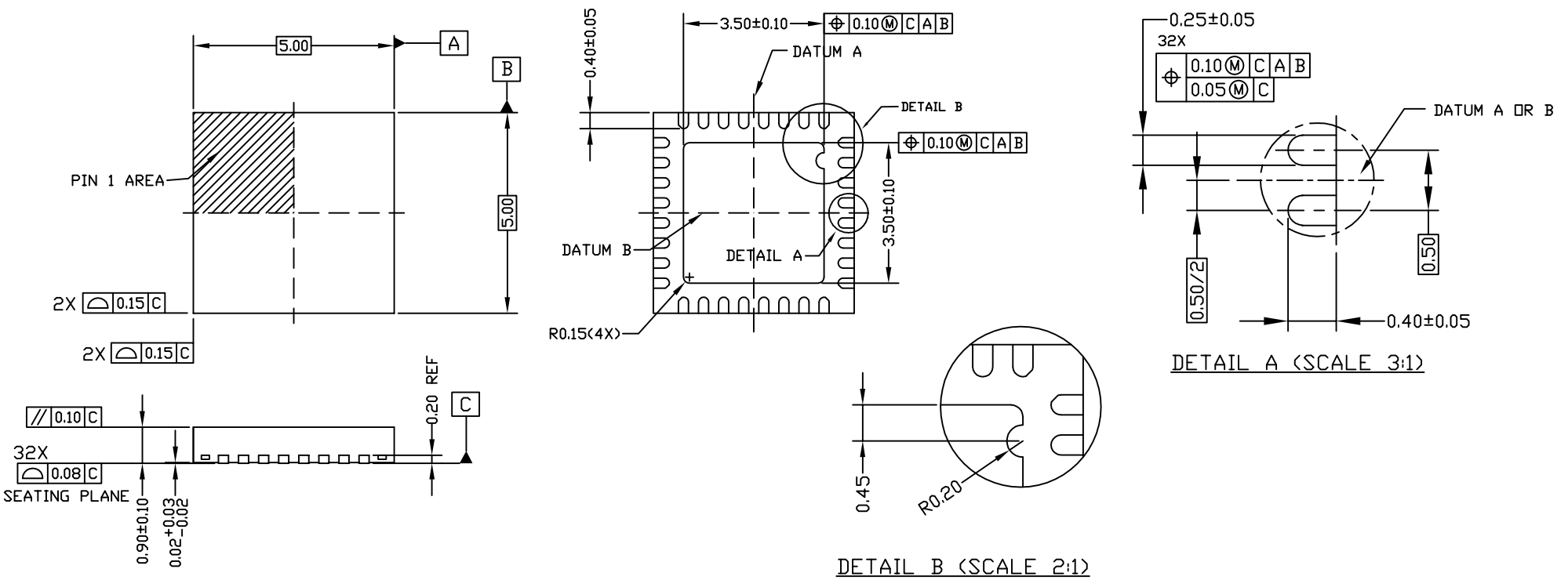
ZARLINK SEMICONDUCTOR

Previous package codes

Package Code LD

Package Outline for Stamped 32 lead QFN (5 x 5mm), 3.7mm DAP (Die Attach Pad)

103364




DETAIL B (SCALE 2:1)

DETAIL A (SCALE 3:1)

NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5–1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

| Zarlink Semiconductor | | | | DWG. NO. | REV. |
|---|---|---|---|---|---|
| TITLE 32 QFN PACKAGE OUTLINE<br>BODY SIZE : 5X5X0.90 mm<br>PITCH : 0.50mm | | | | CDCA 22–0005<br>ASE84–06–137–167 | 1 |
| | | | | SHEET: 1 OF 1 | SIZE: A0 |
| BY | DRAWN | CHECKED | APPROVED | ACAD FILE | REF JEDEC NO |
| | ASE | J Kelly | J Kelly | D6137167 | MO–220 |

**For more information about all Zarlink products visit our Web Site at**

**www.zarlink.com**

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I2C components conveys a licence under the Philips I2C Patent rights to use these components in and I2C System, provided that the system conforms to the I2C Standard Specification as defined by Philips.

Zarlink, ZL, the Zarlink Semiconductor logo and the Legerity logo and combinations thereof, VoiceEdge, VoicePort, SLAC, ISLIC, ISLAC and VoicePath are trademarks of Zarlink Semiconductor Inc.

TECHNICAL DOCUMENTATION - NOT FOR RESALE