ZL40226
Precision 2:8 LVDS Fanout Buffer with Simple Input Reference Switching
Data Sheet

April 2014

Features

Inputs/Outputs

- Accepts two differential or single-ended inputs
  - LVPECL, LVDS, CML, HCSL, LVCMOS
- Eight precision LVDS outputs
- Operating frequency up to 750 MHz

Power

- Option for 2.5 V or 3.3 V power supply
- Current consumption of 113 mA
- On-chip Low Drop Out (LDO) Regulator for superior power supply rejection

Performance

- Ultra low additive jitter of 104 fs RMS

Ordering Information

ZL40226LDG1	32 Pin QFN	Trays
ZL40226LDF1	32 Pin QFN	Tape and Reel

Matte Tin

Package size: 5 x 5 mm

-40°C to +85°C

Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Redundant clock distribution
- Wired communications: OTN, SONET/SDH, GE, 10 GE, FC and 10G FC
- PCI Express generation 1/2/3 clock distribution
- Wireless communications
- High performance microprocessor clock distribution

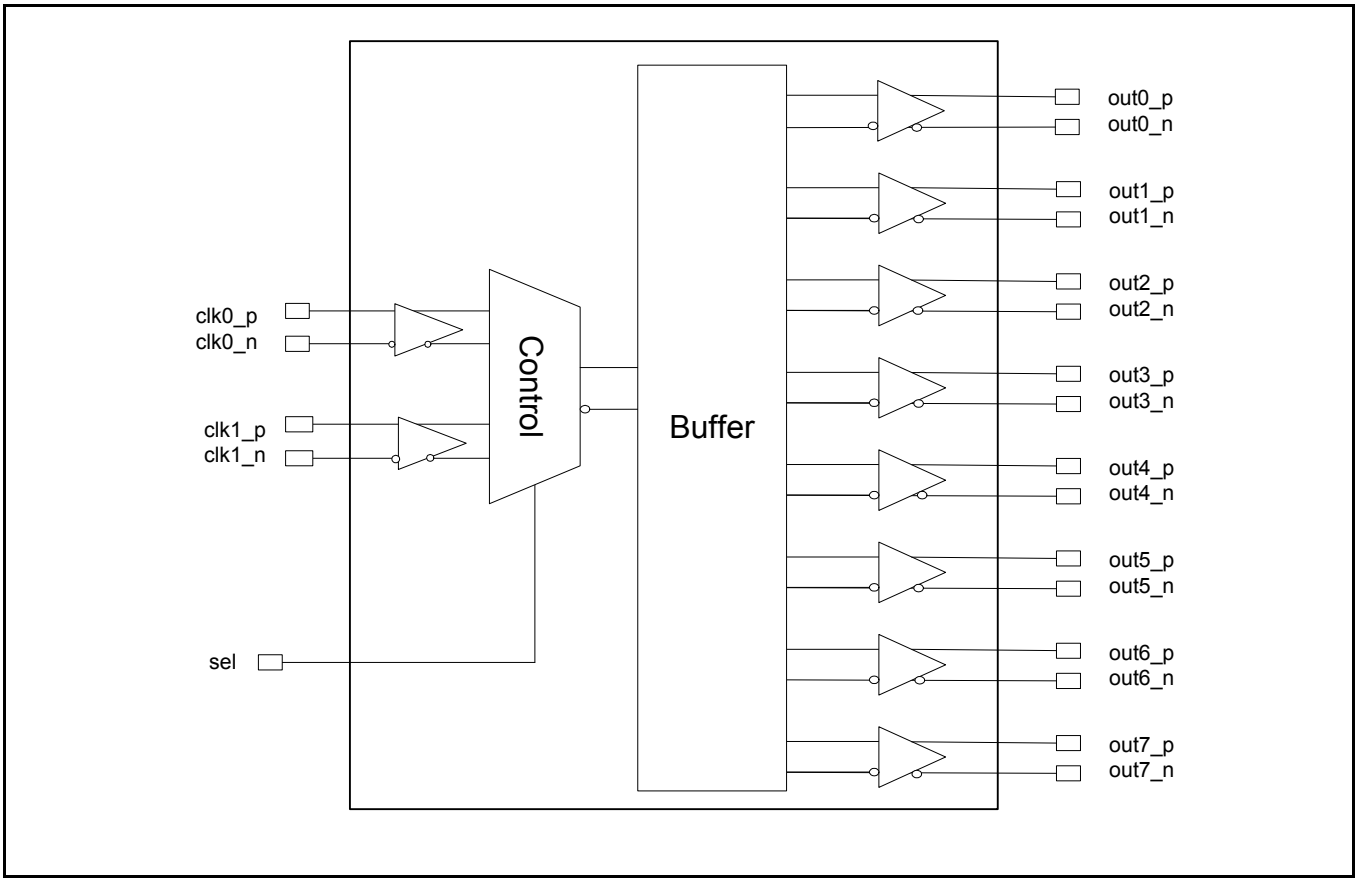


Figure 1 - Functional Block Diagram

Microsemi Corporation
Copyright 2014, Microsemi Corporation, All Rights Reserved.

Table of Contents

Features **1**
Inputs/Outputs 1
Power 1
Performance 1
Applications **1**
Change Summary **4**
1.0 Package Description **5**
2.0 Pin Description **6**
3.0 Functional Description **7**
3.1 Clock Input Selection 7
3.2 Clock Input Termination 7
3.3 Clock Outputs 12
3.4 Device Additive Jitter 15
3.5 Power Supply 16
3.5.1 Sensitivity to power supply noise 16
3.5.2 Power supply filtering 16
3.5.3 PCB layout considerations 16
4.0 AC and DC Electrical Characteristics **17**
5.0 Performance Characterization **19**
6.0 Typical Behavior **20**
7.0 Package Characteristics **21**
8.0 Mechanical Drawing **22**

List of Figures

Figure 1 - Functional Block Diagram . . . 1
Figure 2 - Pin Connections . . . 5
Figure 3 - LVPECL Input DC Coupled Thevenin Equivalent . . . 7
Figure 4 - LVPECL Input DC Coupled Parallel Termination . . . 8
Figure 5 - LVPECL Input AC Coupled Termination . . . 8
Figure 6 - LVDS Input DC Coupled . . . 9
Figure 7 - LVDS Input AC Coupled . . . 9
Figure 8 - CML Input AC Coupled . . . 10
Figure 9 - HCSL Input AC Coupled . . . 10
Figure 10 - CMOS Input DC Coupled Referenced to VDD/2 . . . 11
Figure 11 - CMOS Input DC Coupled Referenced to Ground . . . 11
Figure 12 - Simplified LVDS Output Driver . . . 12
Figure 13 - LVDS DC Coupled Termination (Internal Receiver Termination) . . . 12
Figure 14 - LVDS DC Coupled Termination (External Receiver Termination) . . . 13
Figure 15 - LVDS AC Coupled Termination . . . 13
Figure 16 - LVDS AC Output Termination for CML Inputs . . . 14
Figure 17 - Additive Jitter . . . 15
Figure 18 - Decoupling Connections for Power Pins . . . 16
Figure 19 - Differential Voltage Parameter . . . 18
Figure 20 - Input To Output Timing . . . 18

Change Summary

Below are the changes from the February 2013 issue to the April 2014 issue:

Page	Item	Change
1	Applications	Added PCI Express clock distribution.
6	Pin Description	Added exposed pad to Pin Description.
7, 8	Figure 3 and Figure 4	Removed 22 ohm series resistors from Figure 3 and 4. These resistors are not required; however there is no impact to performance if the resistors are included.
18	Figure 19	Clarification of V_{ID} and V_{OD}.

Below are the changes from the November 2012 issue to the February 2013 issue:

Page	Item	Change
8	Figure 4	Changed text to indicate the circuit is not recommended for VDD_driver=2.5V.
8	Figure 5	Changed pull-up and pull-down resistors from 2kOhm to 100 Ohm.
12	Figure 12	Changed gate values to +/+ on the left and -/- on the right.

1.0 Package Description

The device is packaged in a 32 pin QFN

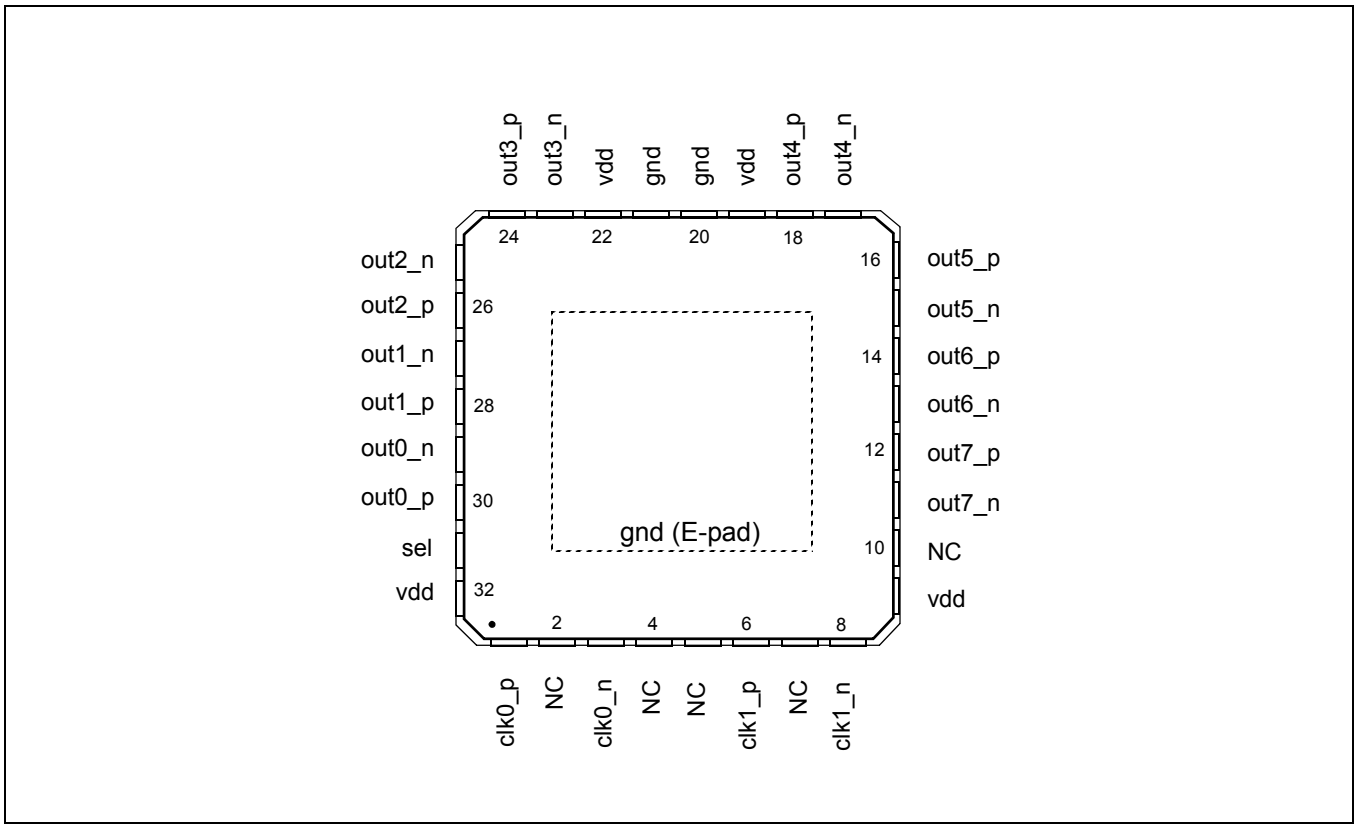


Figure 2 - Pin Connections

2.0 Pin Description

Pin #	Name	Description
1,3, 6, 8	clk0_p, clk0_n, clk1_p, clk1_n	**Differential Input (Analog Input).** Differential (or singled ended) input signals. For all input signal configuration see Section 3.2, “Clock Input Termination“.
30, 29, 28, 27, 26, 25, 24, 23, 18, 17, 16, 15, 14, 13, 12, 11	out0_p, out0_n out1_p, out1_n out2_p, out2_n out3_p, out3_n out4_p, out4_n out5_p, out5_n out6_p, out6_n out7_p, out7_n	**Differential Output (Analog Output).** Differential outputs.
9, 19, 22, 32	vdd	**Positive Supply Voltage.** 2.5V_{DC} or 3.3 V_{DC} nominal.
20, 21	gnd	**Ground.** 0 V.
31	sel	**Input Select (Input).** Selects the reference input that is buffered; 0: clk0 1: clk1 This pin is internally pulled down to GND.
2, 4, 5, 7, 10	NC	**No Connection.** Leave unconnected.
Exposed Pad		**Device GND**.

3.0 Functional Description

The ZL40226 is an LVDS clock fanout buffer with eight identical output clock drivers capable of operating at frequencies up to 750MHz.

The two Inputs to the ZL40226 are externally terminated to allow use of precision termination components and to allow full flexibility of input termination. The ZL40226 can accept DC coupled LVPECL or LVDS and AC coupled LVPECL, LVDS, CML or HCSL input signals; single ended input signals can also be accepted. A pin compatible device with internal termination is also available.

The ZL40226 is designed to fan out low-jitter reference clocks for wired or optical communications applications while adding minimal jitter to the clock signal. An internal linear power supply regulator and bulk capacitors minimize additive jitter due to power supply noise. The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

The device block diagram is shown in Figure 1; its operation is described in the following sections.

3.1 Clock Input Selection

The select line chooses which input clock is routed to the outputs.

Sel	Active Input
0	clk0
1	clk1

Table 1 - Input Selection

3.2 Clock Input Termination

The ZL40212 is adaptable to support different types of differential and single-ended input signals depending on the passive components used in the input termination. The application diagrams in the following figures allow the ZL40212 to accept LVPECL, LVDS, CML, HCSL and single-ended inputs.

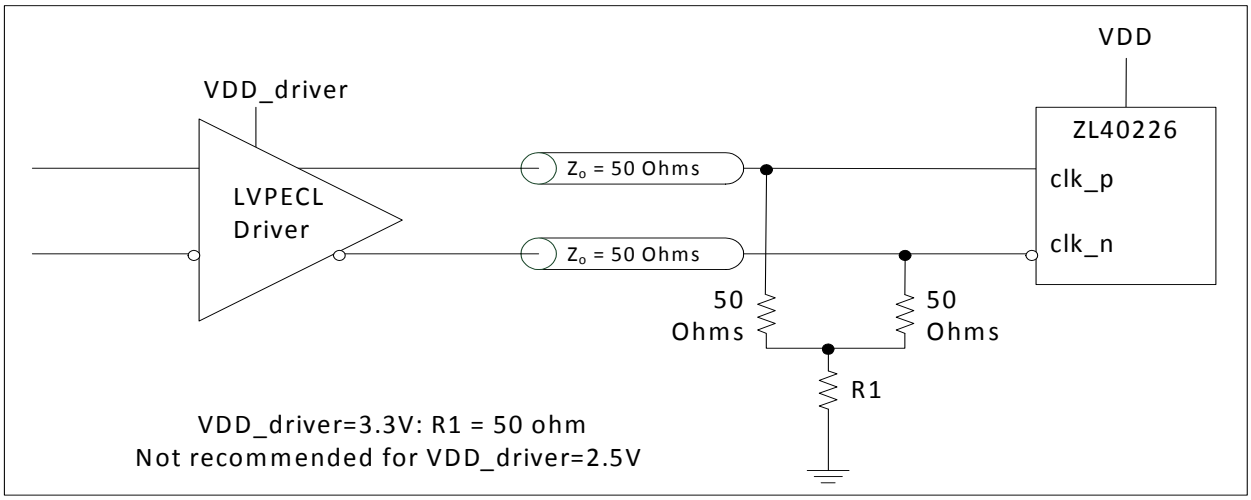


Figure 3 - LVPECL Input DC Coupled Thevenin Equivalent

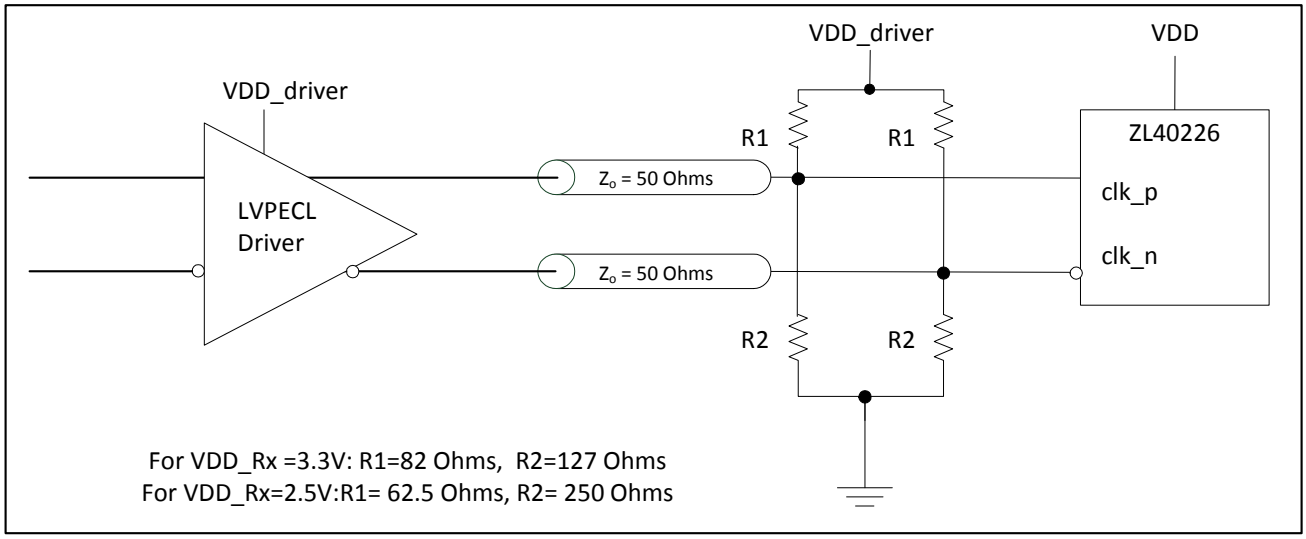


Figure 4 - LVPECL Input DC Coupled Parallel Termination

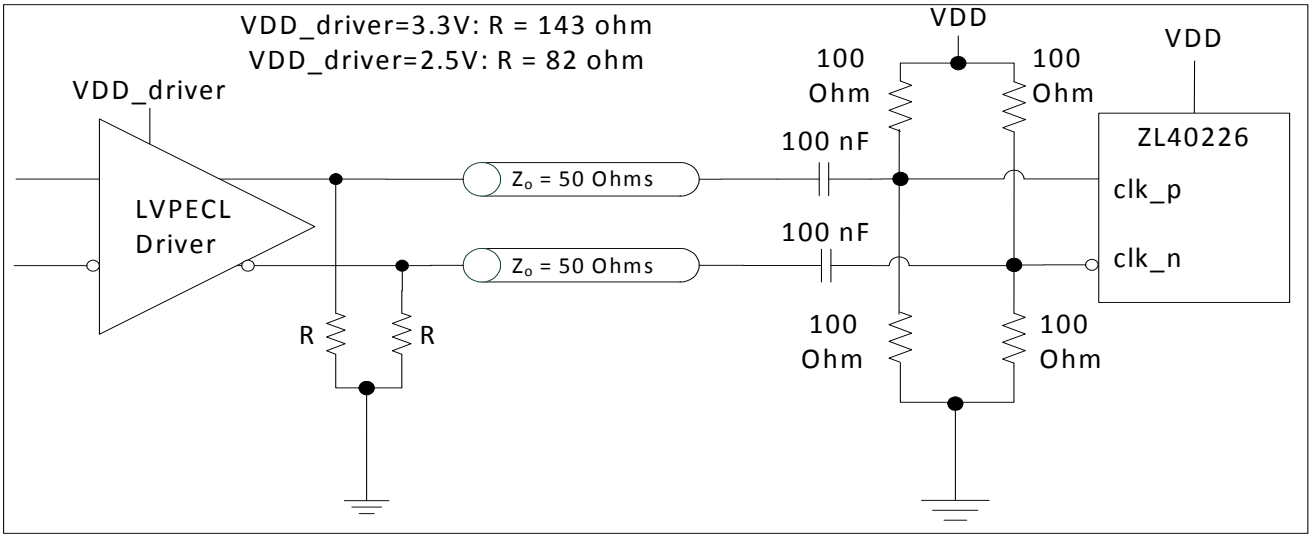


Figure 5 - LVPECL Input AC Coupled Termination

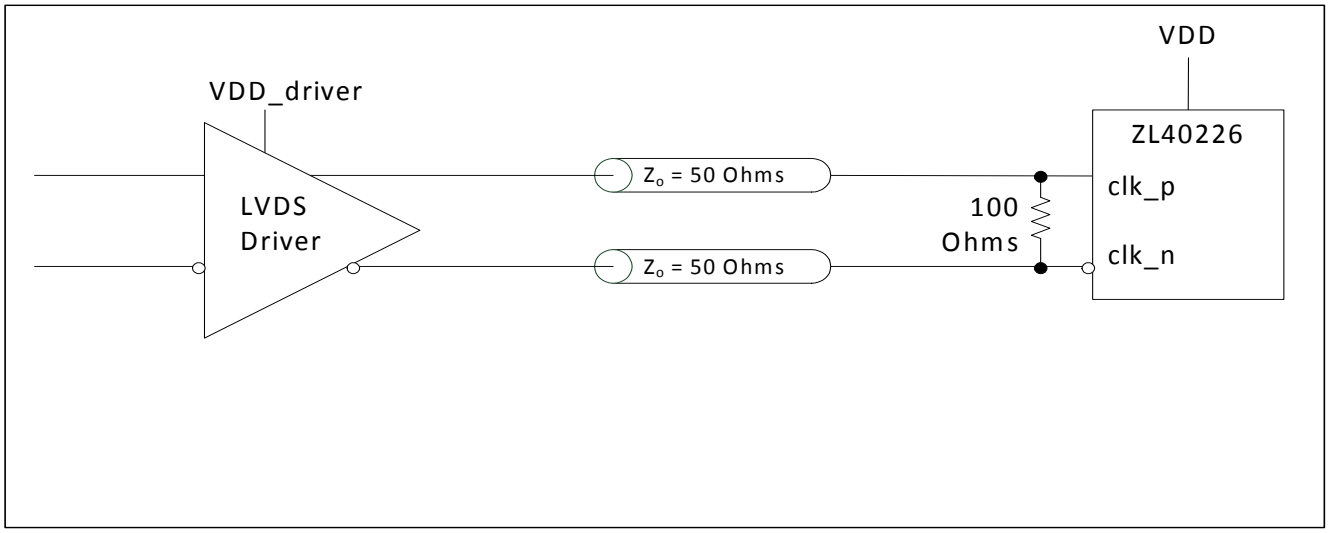


Figure 6 - LVDS Input DC Coupled

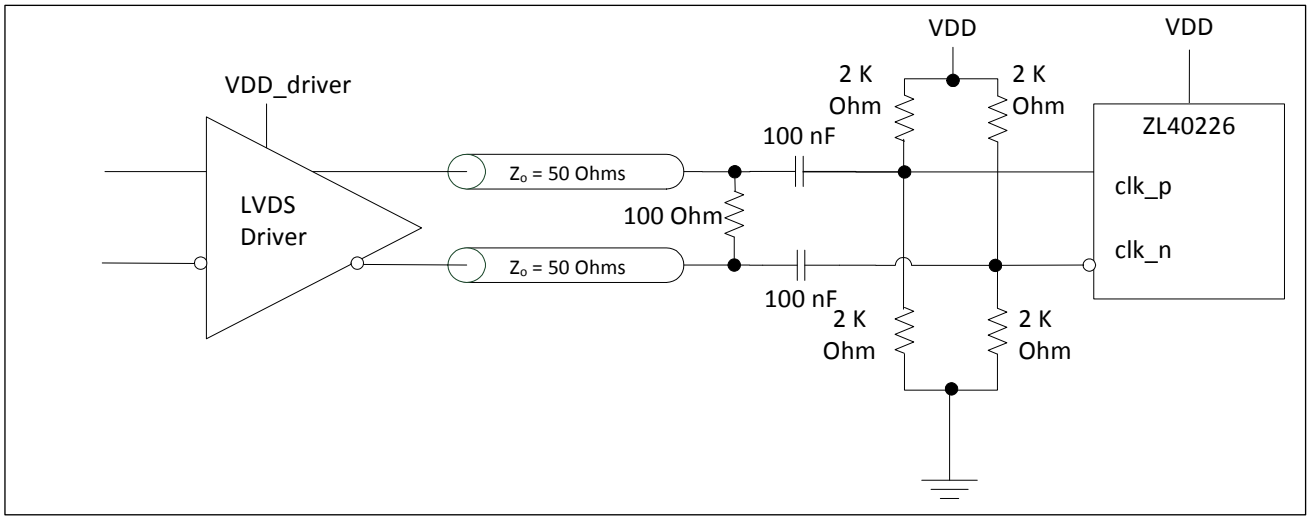


Figure 7 - LVDS Input AC Coupled

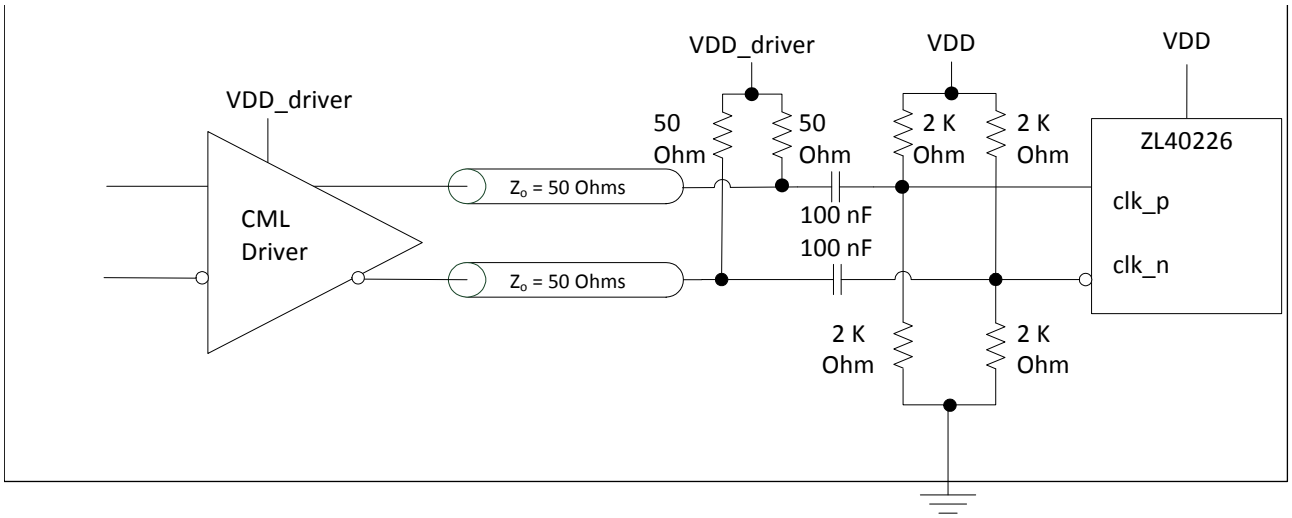


Figure 8 - CML Input AC Coupled

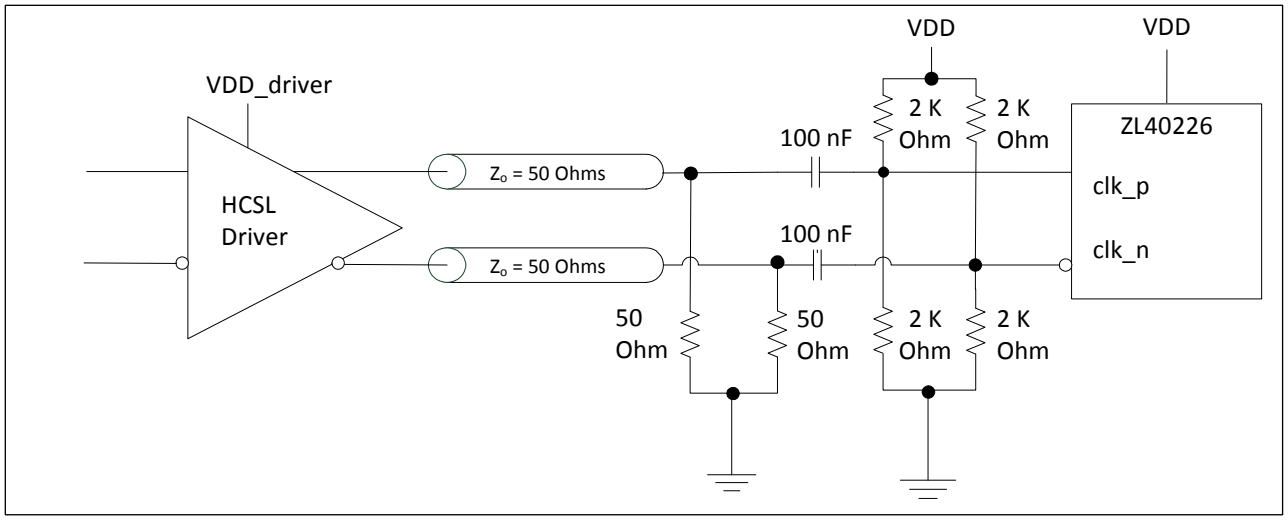


Figure 9 - HCSL Input AC Coupled

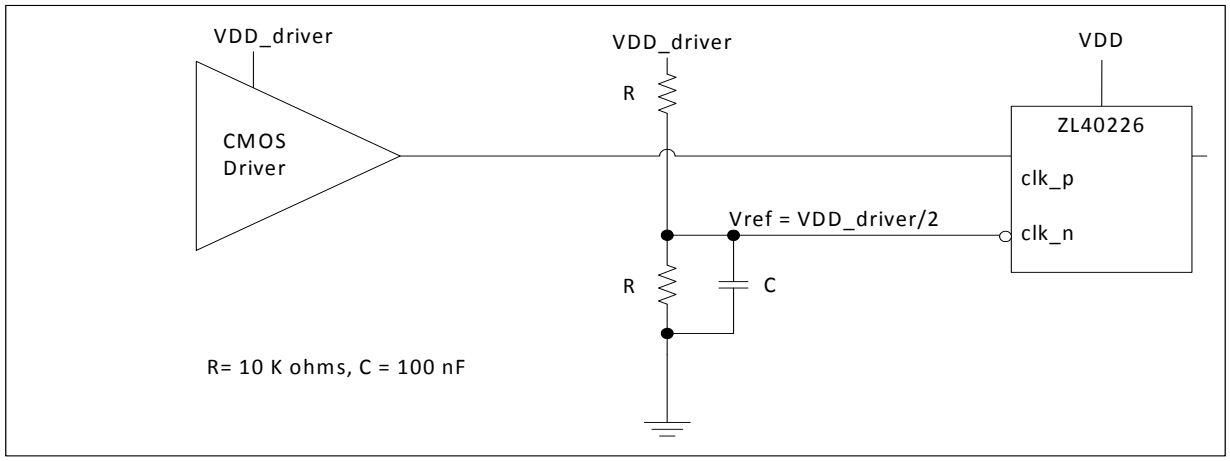


Figure 10 - CMOS Input DC Coupled Referenced to VDD/2

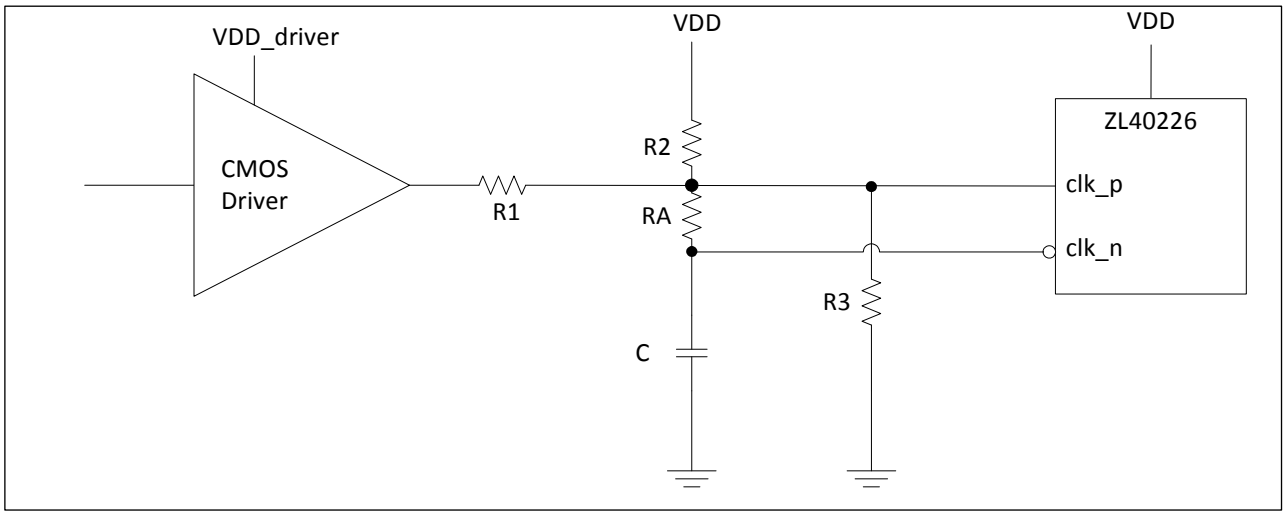


Figure 11 - CMOS Input DC Coupled Referenced to Ground

VDD_driver	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	RA (kΩ)	C (pF)
1.5	1.25	3.075	open	10	10
1.8	1	3.8	open	10	10
2.5	0.33	4.2	open	10	10
3.3	0.75	open	4.2	10	10

Table 2 - Component Values for Single Ended Input Reference to Ground

* For frequencies below 100 MHz, increase C to avoid signal integrity issues.

3.3 Clock Outputs

LVDS has lower signal swing than LVPECL which results in a low power consumption. A simplified diagram for the LVDS output stage is shown in Figure 12.

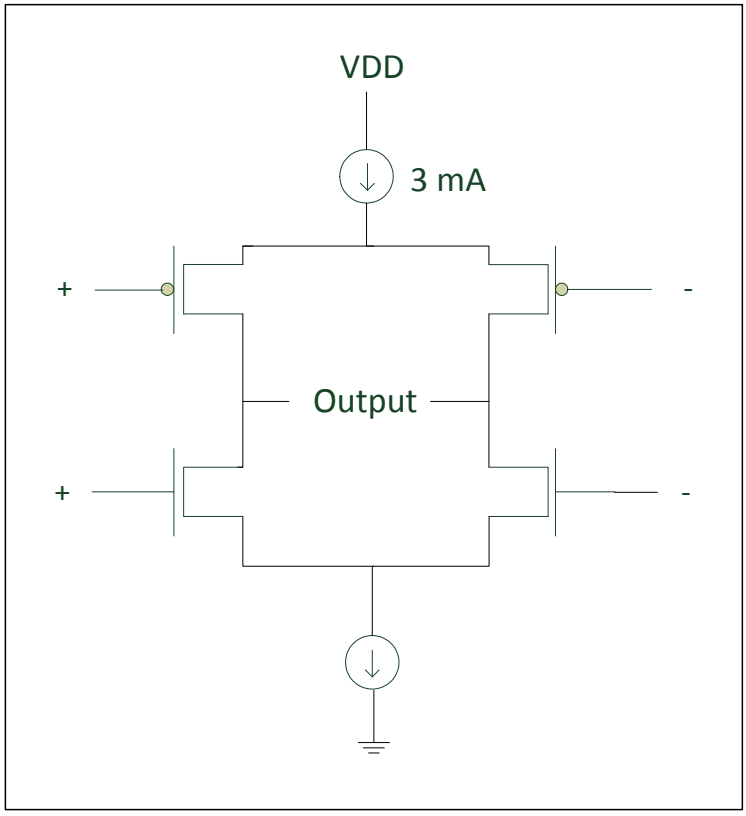


Figure 12 - Simplified LVDS Output Driver

The methods to terminate the ZL40226 drivers are shown in the following figures.

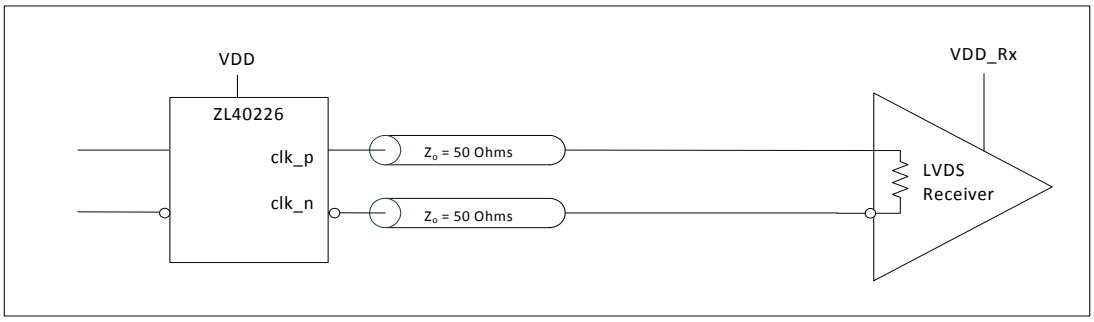


Figure 13 - LVDS DC Coupled Termination (Internal Receiver Termination)

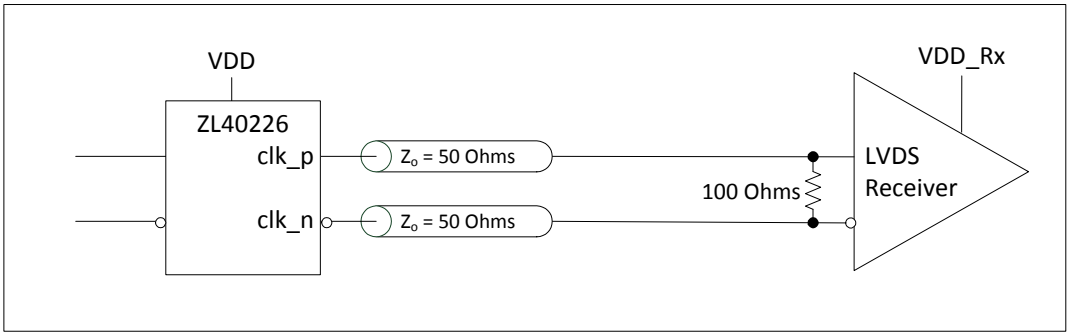


Figure 14 - LVDS DC Coupled Termination (External Receiver Termination)

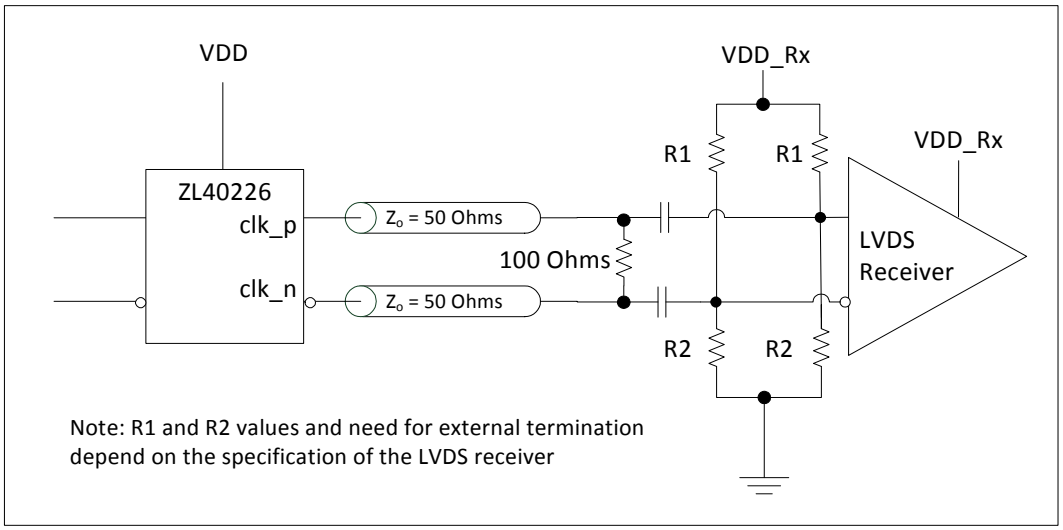


Figure 15 - LVDS AC Coupled Termination

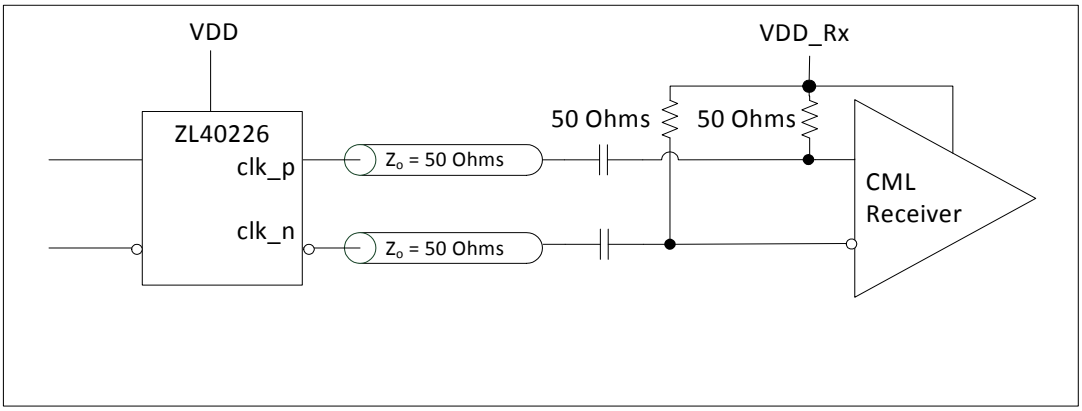


Figure 16 - LVDS AC Output Termination for CML Inputs

3.4 Device Additive Jitter

The ZL40226 clock fanout buffer is not intended to filter clock jitter. The jitter performance of this type of device is characterized by its additive jitter. Additive jitter is the jitter the device would add to a hypothetical jitter-free clock as it passes through the device. The additive jitter of the ZL40226 is random and as such it is not correlated to the jitter of the input clock signal.

The square of the resultant random RMS jitter at the output of the ZL40226 is equal to the sum of the squares of the various random RMS jitter sources including: input clock jitter; additive jitter of the buffer; and additive jitter due to power supply noise. There may be additional deterministic jitter sources, but they are not shown in Figure 17.

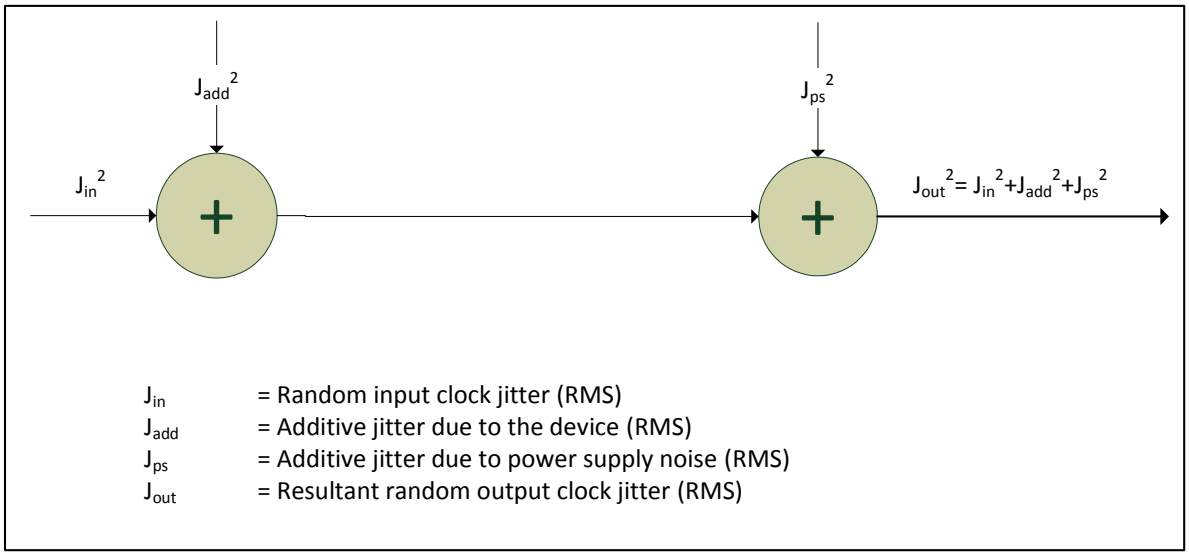


Figure 17 - Additive Jitter

3.5 Power Supply

This device operates with either a 2.5V supply or 3.3V supply.

3.5.1 Sensitivity to power supply noise

Power supply noise from sources such as switching power supplies and high-power digital components such as FPGAs can induce additive jitter on clock buffer outputs. The ZL40226 is equipped with a low drop out (LDO) linear power regulator and on-chip bulk capacitors to minimize additive jitter due to power supply noise. The on-chip regulation, recommended power supply filtering, and good PCB layout all work together to minimize the additive jitter from power supply noise.

3.5.2 Power supply filtering

For optimal jitter performance, the ZL40226 should be isolated from the power planes connected to its power supply pins as shown in Figure 18.

- 10 µF capacitors should be size 0603 or size 0805 X5R or X7R ceramic, 6.3 V minimum rating
- 0.1 µF capacitors should be size 0402 X5R ceramic, 6.3 V minimum rating
- Capacitors should be placed next to the connected device power pins

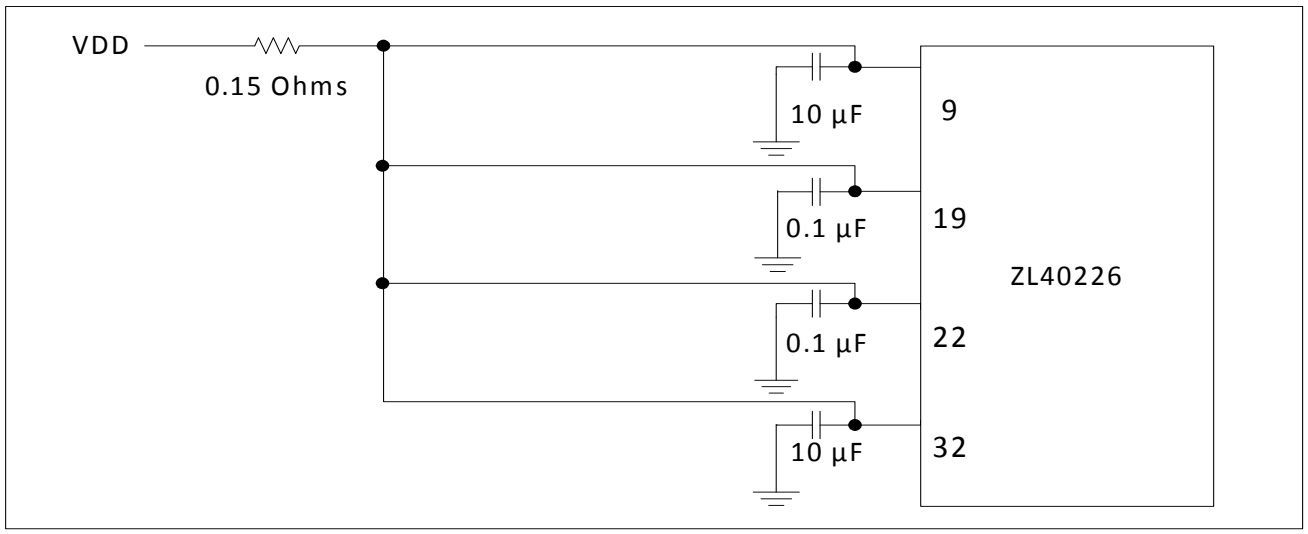


Figure 18 - Decoupling Connections for Power Pins

3.5.3 PCB layout considerations

The power supply filtering shown in Figure 18 can be implemented either as a plane island, or as a routed power topology with the same performance.

4.0 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Sym.	Min.	Max.	Units
1	Supply voltage	V_{DD_R}	-0.5	4.6	V
2	Voltage on any digital pin	V_{PIN}	-0.5	V_{DD}	V
3	Soldering temperature	T		260	°C
4	Storage temperature	T_{ST}	-55	125	°C
5	Junction temperature	T_j		125	°C
6	Voltage on input pin	V_{input}		V_{DD}	V
7	Input capacitance each pin	C_p		500	fF

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated

Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Supply voltage 2.5 V mode	V_{DD25}	2.375	2.5	2.625	V
2	Supply voltage 3.3 V mode	V_{DD33}	3.135	3.3	3.465	V
3	Operating temperature	T_A	-40	25	85	°C

* Voltages are with respect to ground (GND) unless otherwise stated

DC Electrical Characteristics - Current Consumption

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply current LVDS drivers - loaded (all outputs are active)	I_{dd_load}		113		mA	

DC Electrical Characteristics - Inputs and Outputs - for 2.5/3.3 V Supply

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS control logic high-level input	V_{CIH}	$0.7*V_{DD}$			V	
2	CMOS control logic low-level input	V_{CIL}			$0.3*V_{DD}$	V	
3	CMOS control logic Input leakage current	I_{IL}		1		µA	$V_I = V_{DD}$ or 0 V
4	Differential input voltage difference	V_{ID}	0.25		1	V	
5	Differential input common mode voltage	V_{CM}	1.1		1.6	V	for 2.5 V
6	Differential input common mode voltage	V_{CM}	1.1		2.0	V	for 3.3 V
7	LVDS output differential voltage*	V_{OD}	0.25	0.30	0.40	V	
8	LVDS output common mode	V_{CM}	1.1	1.25	1.375	V	

* The VOD parameter was measured from 125 MHz to 750 MHz.

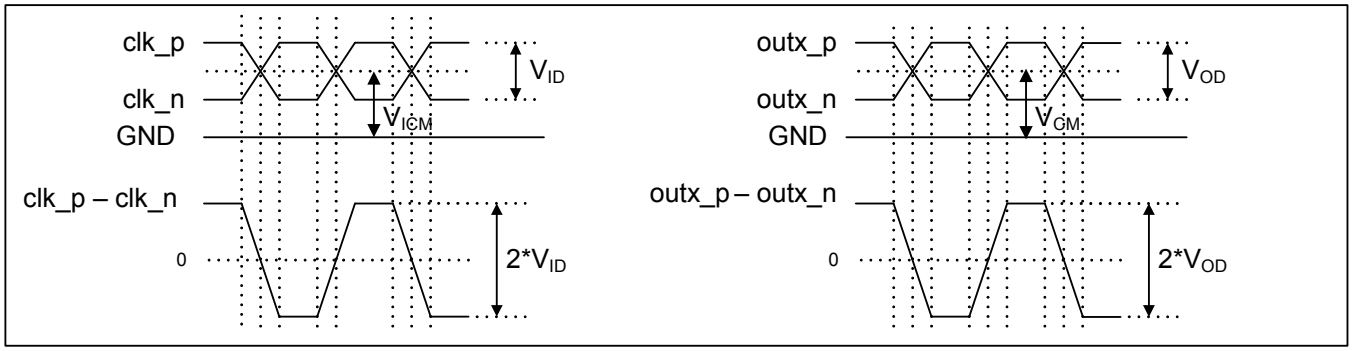


Figure 19 - Differential Voltage Parameter

AC Electrical Characteristics* - Inputs and Outputs (see Figure 20) - for 2.5/3.3 V supply.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Maximum Operating Frequency	$1/t_p$			750	MHz	
2	Input to output clock propagation delay	t_{pd}	0	1	2	ns	
3	Output to output skew	$t_{out2out}$		80	150	ps	
4	Part to part output skew	$t_{part2part}$		120	300	ps	
5	Output clock Duty Cycle degradation	t_{PWH}/ t_{PWL}	-5	0	5	Percent	
6	LVDS Output slew rate	r_{sl}	0.55			V/ns	
7	Reference transition time	t_{switch}		0.5	1	us	

* Supply voltage and operating temperature are as per Recommended Operating Conditions

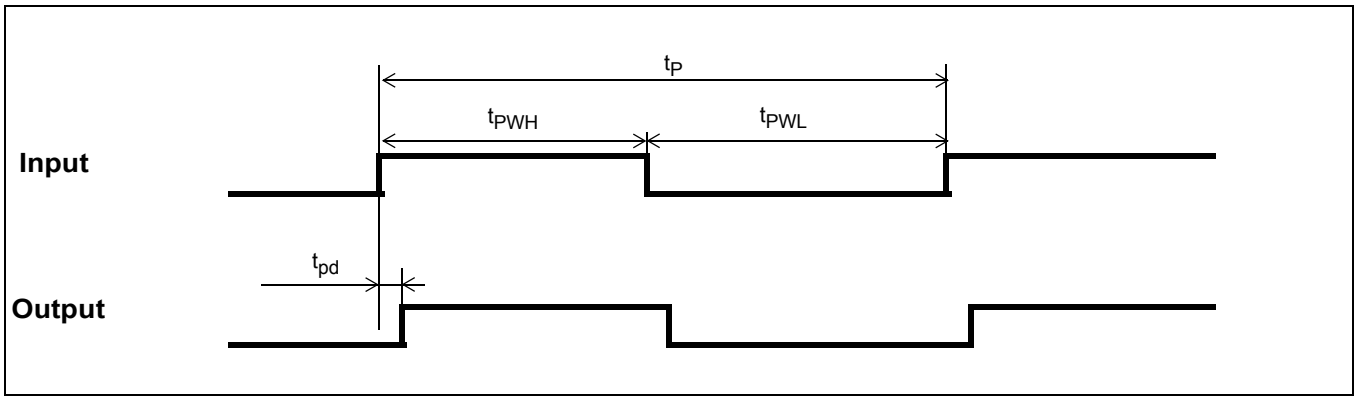


Figure 20 - Input To Output Timing

5.0 Performance Characterization

Additive Jitter at 2.5 V*

	Output Frequency (MHz)	Jitter Measurement Filter	Typical RMS (fs)	Notes
1	125	12 kHz - 20 MHz	148	
2	212.5	12 kHz - 20 MHz	138	
3	311.04	12 kHz - 20 MHz	121	
4	425	12 kHz - 20 MHz	115	
5	500	12 kHz - 20 MHz	107	
6	622.08	12 kHz - 20 MHz	107	
7	750	12 kHz - 20 MHz	105	

*The values in this table were taken with an approximate slew rate of 0.8 V/ns.

Additive Jitter at 3.3 V*

	Output Frequency (MHz)	Jitter Measurement Filter	Typical RMS (fs)	Notes
1	125	12 kHz - 20 MHz	150	
2	212.5	12 kHz - 20 MHz	138	
3	311.04	12 kHz - 20 MHz	120	
4	425	12 kHz - 20 MHz	115	
5	500	12 kHz - 20 MHz	107	
6	622.08	12 kHz - 20 MHz	106	
7	750	12 kHz - 20 MHz	104	

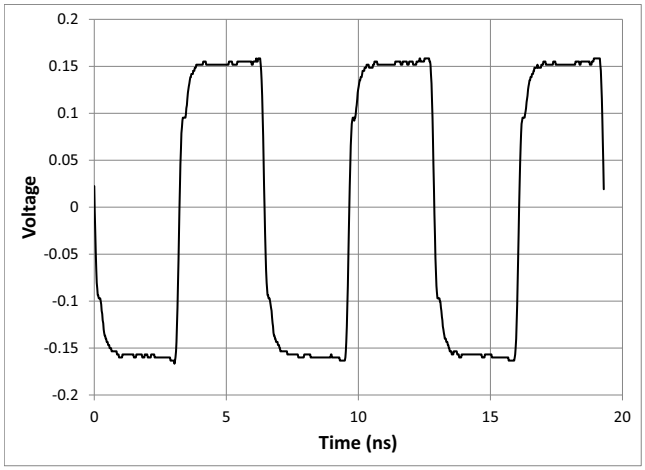
*The values in this table were taken with an approximate slew rate of 0.8 V/ns.

Additive Jitter from a Power Supply Tone*

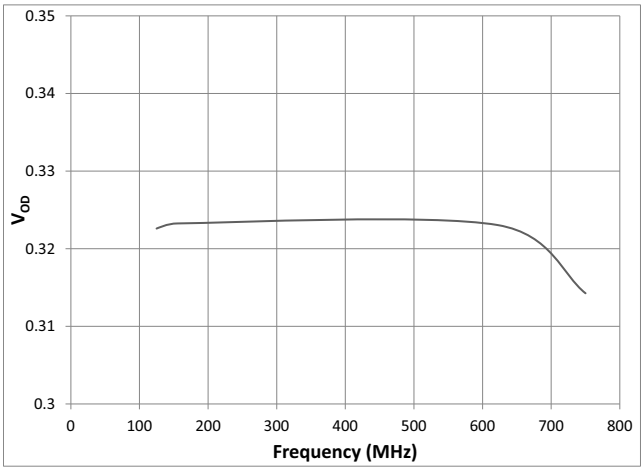
Carrier frequency	Parameter	Typical	Units	Notes
125MHz	25 mV at 100 kHz	24	fs RMS	
750MHz	25 mV at 100 kHz	23	fs RMS	

* The values in this table are the additive periodic jitter caused by an interfering tone typically caused by a switching power supply. For this test, measurements were taken over the full temperature and voltage range for V_{DD} = 3.3 V. The magnitude of the interfering tone is measured at the DUT.

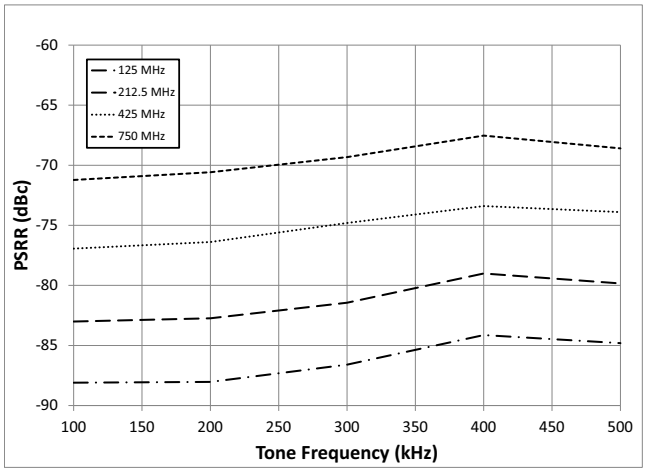
6.0 Typical Behavior



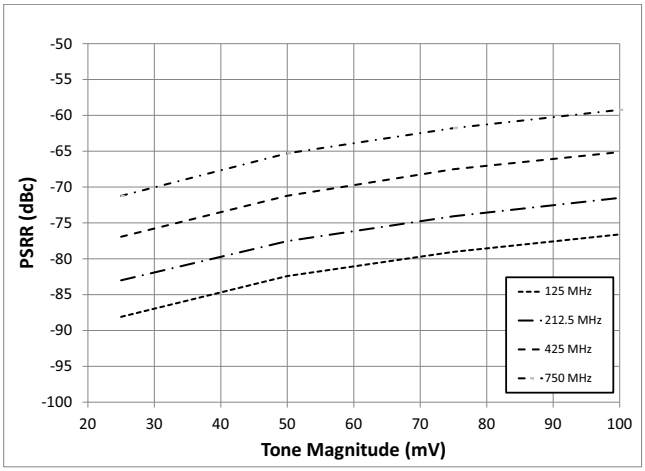
Typical Waveform at 155.52 MHz



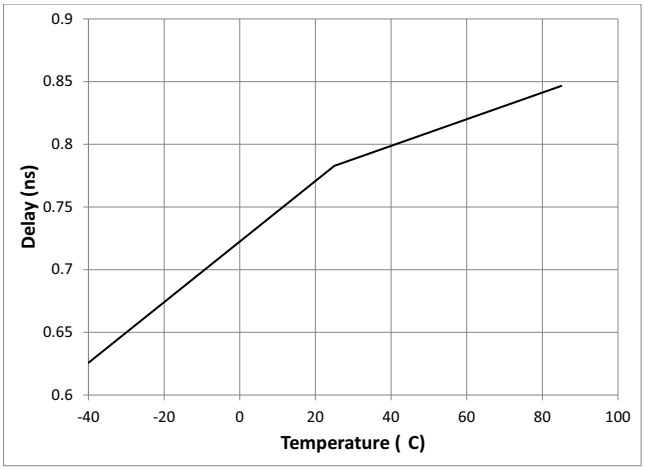
V_{OD} vs Frequency



Power Supply Tone Frequency versus PSRR



Power Supply Tone Magnitude versus PSRR



Propagation Delay versus Temperature

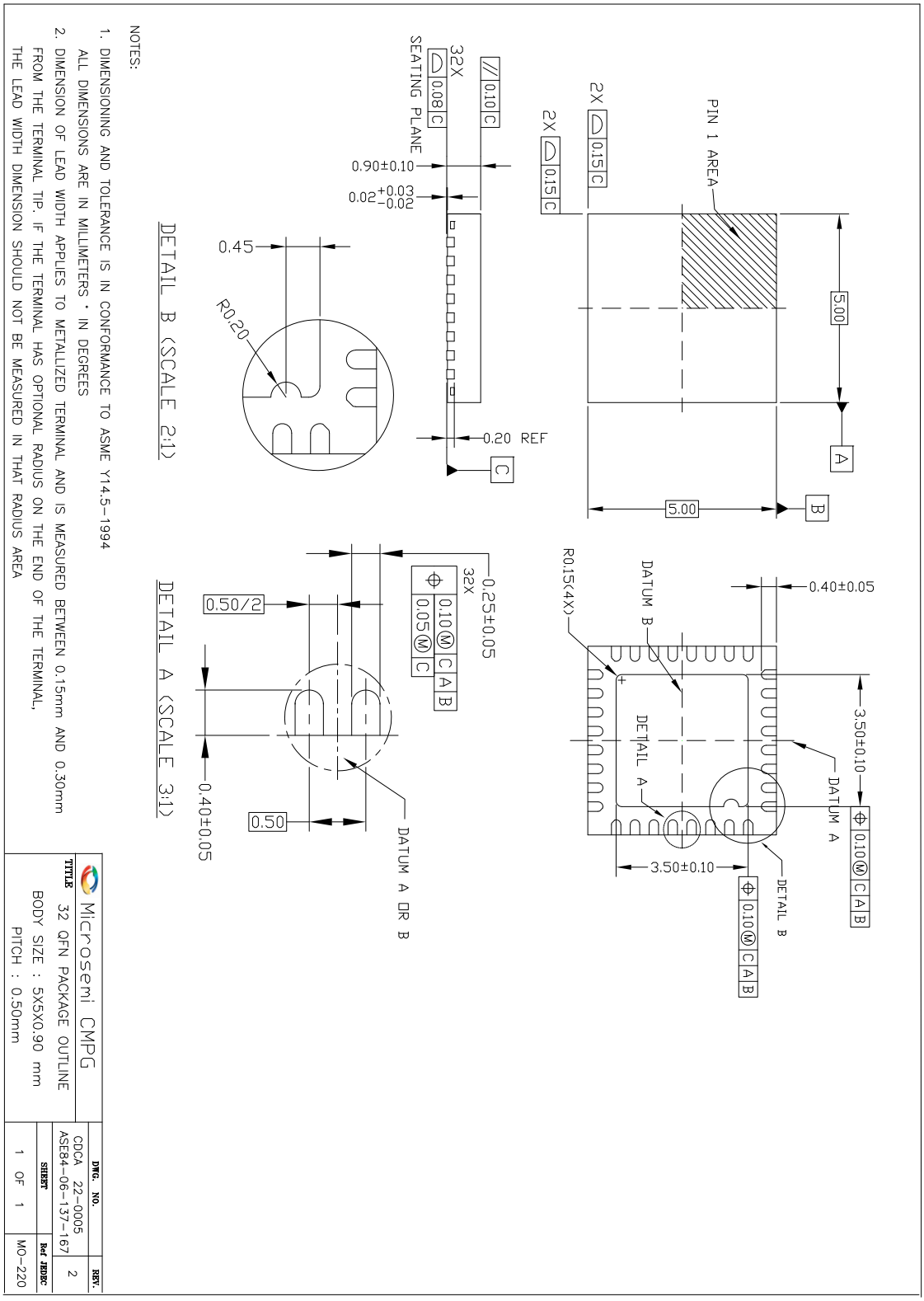
Note: This is for a single device. For more details, see the characterization section.

7.0 Package Characteristics

Thermal Data

Parameter	Symbol	Test Condition	Value	Unit
Junction to Ambient Thermal Resistance	Θ_{JA}	Still Air 1 m/s 2 m/s	37.4 33.1 31.5	^{o}C/W
Junction to Case Thermal Resistance	Θ_{JC}		24.4	^{o}C/W
Junction to Board Thermal Resistance	Θ_{JB}		19.5	^{o}C/W
Maximum Junction Temperature*	T_{jmax}		125	^{o}C
Maximum Ambient Temperature	T_{A}		85	^{o}C

8.0 Mechanical Drawing



NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994
   ALL DIMENSIONS ARE IN MILLIMETERS ' IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Microsemi CMPG	DWG. NO.	REV.
TITLE: 32 QFN PACKAGE OUTLINE BODY SIZE : 5X5X0.90 mm PITCH : 0.50mm	CDCA 22-0005 ASE84-06-137-167	2
	SHEET	Ref JEDEC
	1 OF 1	MO-220

Information relating to products and services furnished herein by Microsemi Corporation or its subsidiaries (collectively “Microsemi”) is believed to be reliable. However, Microsemi assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Microsemi or licensed from third parties by Microsemi, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Microsemi, or non-Microsemi furnished goods or services may infringe patents or other intellectual property rights owned by Microsemi.

This publication is issued to provide information only and (unless agreed by Microsemi in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Microsemi without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user’s responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical and other products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Microsemi’s conditions of sale which are available on request.

For more information about all Microsemi products
visit our website at
www.microsemi.com

TECHNICAL DOCUMENTATION – NOT FOR RESALE



Microsemi Corporate Headquarters One
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense and security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world’s standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 3,400 employees globally. Learn more at www.microsemi.com.

© 2014 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.