ZL40201

Precision 1:2 LVPECL Fanout Buffer with On-Chip Input Termination

Data Sheet

April 2014

Features

Inputs/Outputs

- Accepts differential or single-ended input
  - LVPECL, LVDS, CML, HCSL, LVCMOS
- On-chip input termination resistors and biasing for AC coupled inputs
- Two precision LVPECL outputs
- Operating frequency up to 750 MHz

Power

- Option for 2.5 V or 3.3 V power supply
- Core current consumption of 49 mA
- On-chip Low Drop Out (LDO) Regulator for superior power supply rejection

Performance

- Ultra low additive jitter of 40 fs

Ordering Information

ZL40201LDG1	16 Pin QFN	Trays
ZL40201LDF1	16 Pin QFN	Tape and Reel

Matte Tin

Package size: 3 x 3 mm

-40°C to +85°C

Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Wired communications: OTN, SONET/SDH, GE, 10 GE, FC and 10G FC
- PCI Express generation 1/2/3 clock distribution
- Wireless communications
- High performance microprocessor clock distribution

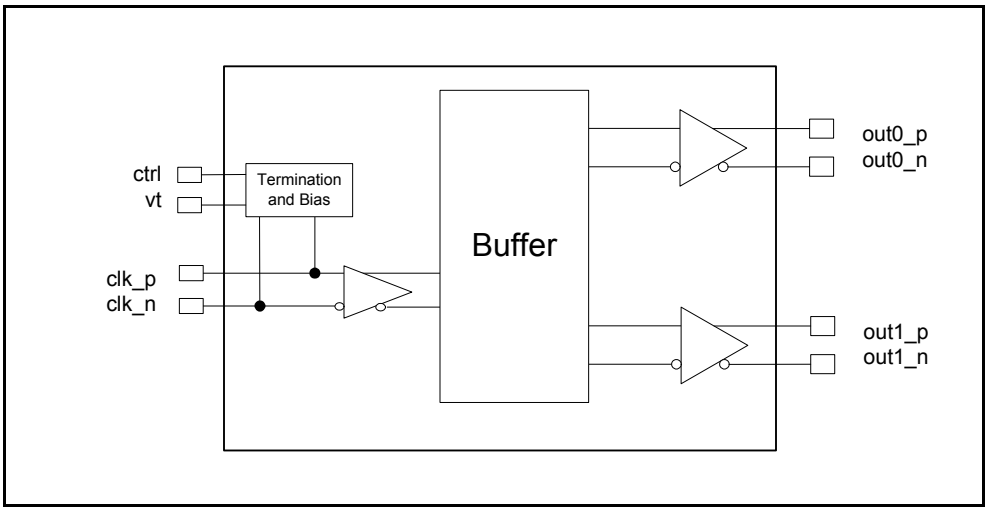


Figure 1 - Functional Block Diagram

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Change Summary

Below

Page	Item	Change
1	Applications	Added PCI Express clock distribution.
5	Pin Description	Added exposed pad to Pin Description.
7	Figure 4 and Figure 5	Removed 22 Ohm series resistors from Figure 4 and 5. These resistors are not required; however, there is no impact to performance if the resistors are included.
17	Figure 20	Clarification of V_{ID} and V_{OD}.

Below are the changes from the November 2012 issue to the February 2013 issue:

Page	Item	Change
7	Figure 4	Changed text to indicate the circuit is not recommended for VDD_driver=2.5V.

1.0 Package Description

The device is packaged in a 16 pin QFN

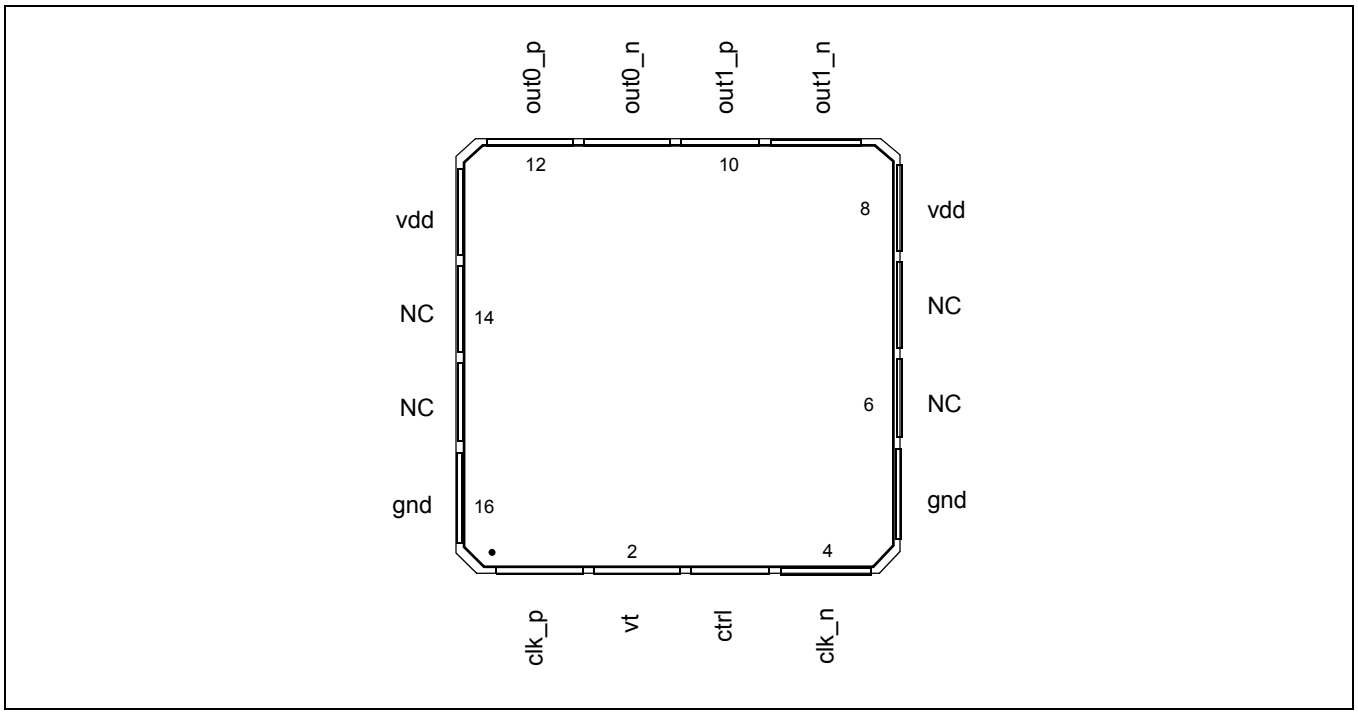


Figure 2 - Pin Connections

2.0 Pin Description

Pin #	Name	Description
1, 4	clk_p, clk_n,	**Differential Input (Analog Input).** Differential (or singled ended) input signals. For all input signal configuration see“Clock Inputs” on page 6
12, 11, 10, 9	out0_p, out0_n out1_p, out1_n	**Differential Output (Analog Output).** Differential outputs.
8, 13	vdd	**Positive Supply Voltage.** 2.5 V_{DC} or 3.3 V_{DC} nominal.
5, 16	gnd	**Ground.** 0 V.
2	vt	**On-Chip Input Termination Node (Analog).** Center tap between internal 50 Ohm termination resistors. See “Clock Inputs” on page 6 for more information.
3	ctrl	**Digital Control for On-Chip Input Termination (Input).** Selects differential input mode; 0: DC coupled modes 1: AC coupled differential modes These pins are internally pulled down to GND. See “Clock Inputs” on page 6 for more information.
6, 7, 14, 15	NC	**No Connection.** Leave unconnected.
Exposed Pad		**Device GND**.

3.0 Functional Description

The ZL40201 is an LVPECL clock fan out buffer with two identical output clock drivers capable of operating at frequencies up to 750MHz.

The ZL40201 provides an internal input termination network for DC and AC coupled inputs; optional input biasing for AC coupled inputs is also provided. The ZL40201 can accept DC or AC coupled LVPECL and LVDS input signals, AC coupled CML or HCSL input signals, and single ended signals. A pin compatible device with external termination is also available.

The ZL40201 is designed to fan out low-jitter reference clocks for wired or optical communications applications while adding minimal jitter to the clock signal. An internal linear power supply regulator and bulk capacitors minimize additive jitter due to power supply noise. The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

The device block diagram is shown in Figure 1; its operation is described in the following sections.

3.1 Clock Inputs

The device has a differential input equipped with two on-chip 50 Ohm termination resistors arranged in series with a center tap. The input can accept many differential and single-ended signals with AC or DC coupling as appropriate. A control pin is available to enable internal biasing for AC coupled inputs. A block diagram of the input stage is in Figure 3.

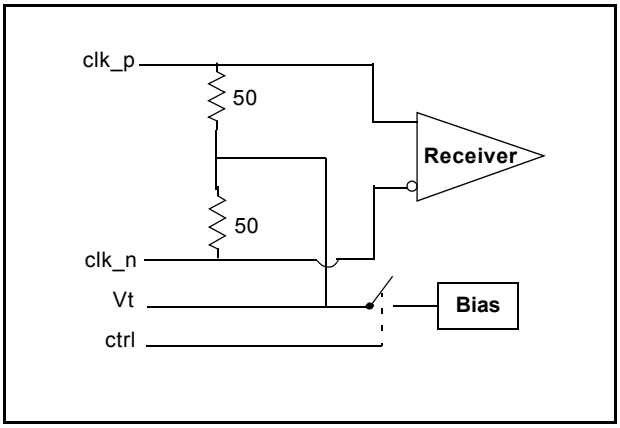


Figure 3 - Simplified Diagram of Input Stage

This following figures give the components values and configuration for the various circuits compatible with the input stage and the use of the *Vt* and *ctrl* pins in each case.

In the following diagrams where the *ctrl* pin is "1" and the *Vt* pin is not connected, the *Vt* pin can be instead connected to V_{DD} with a capacitor.The same capacitor can also help in Figure 4 between *Vt* and V_{DD}. This capacitor will minimize the noise at the point between the two internal termination resistors and improve the overall performance of the device.

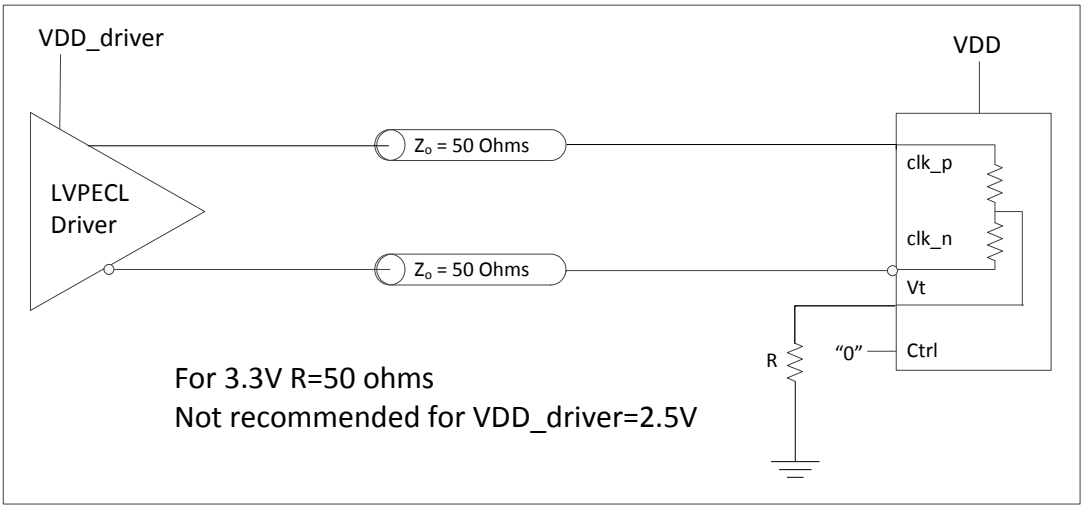


Figure 4 - Clock Input - LVPECL - DC Coupled

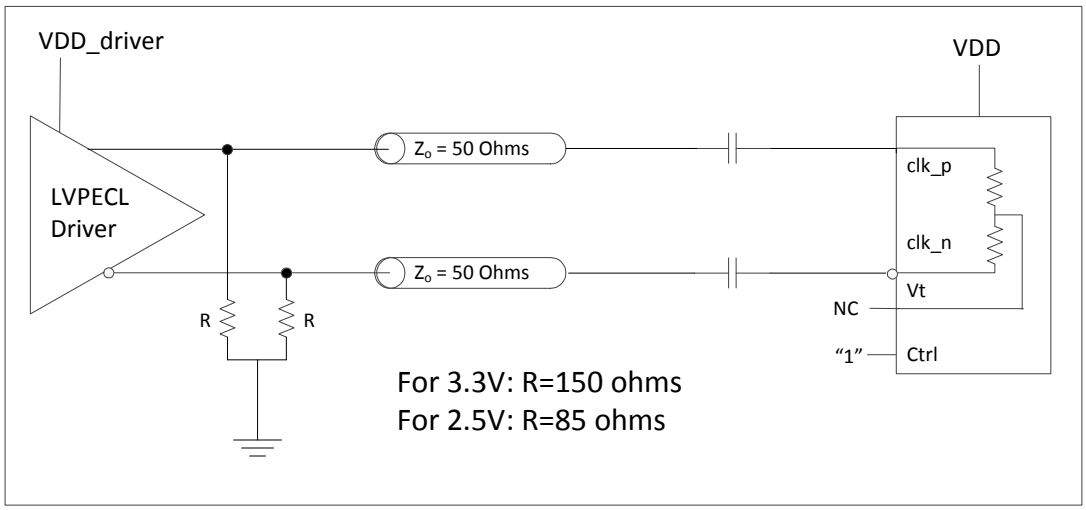


Figure 5 - Clock Input - LVPECL - AC Coupled

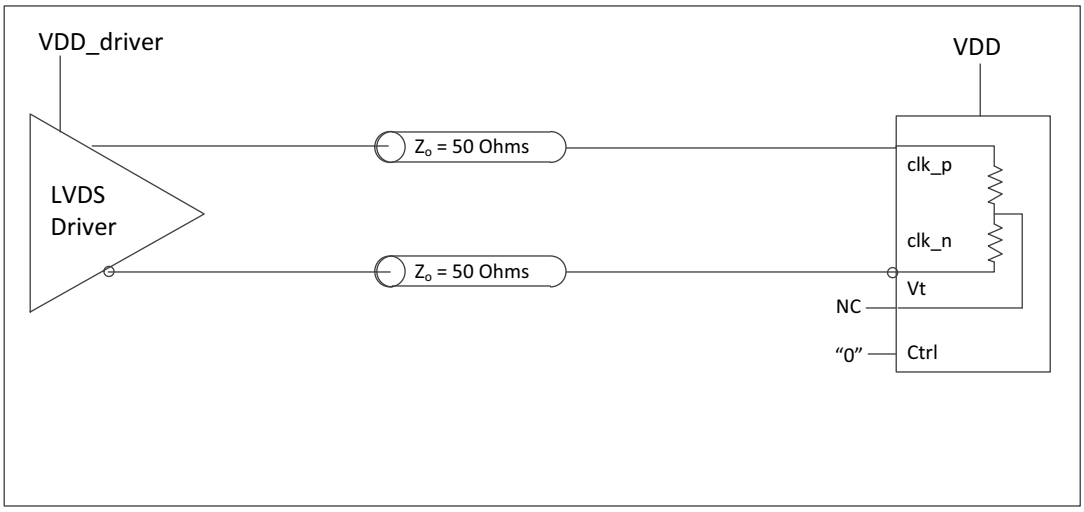


Figure 6 - Clock Input - LVDS - DC Coupled

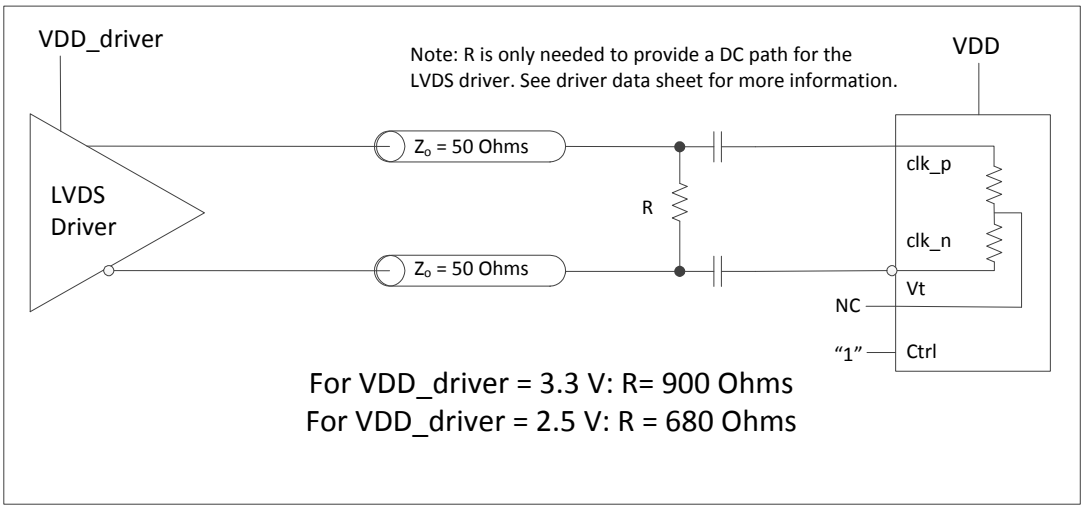


Figure 7 - Clock Input - LVDS - AC Coupled

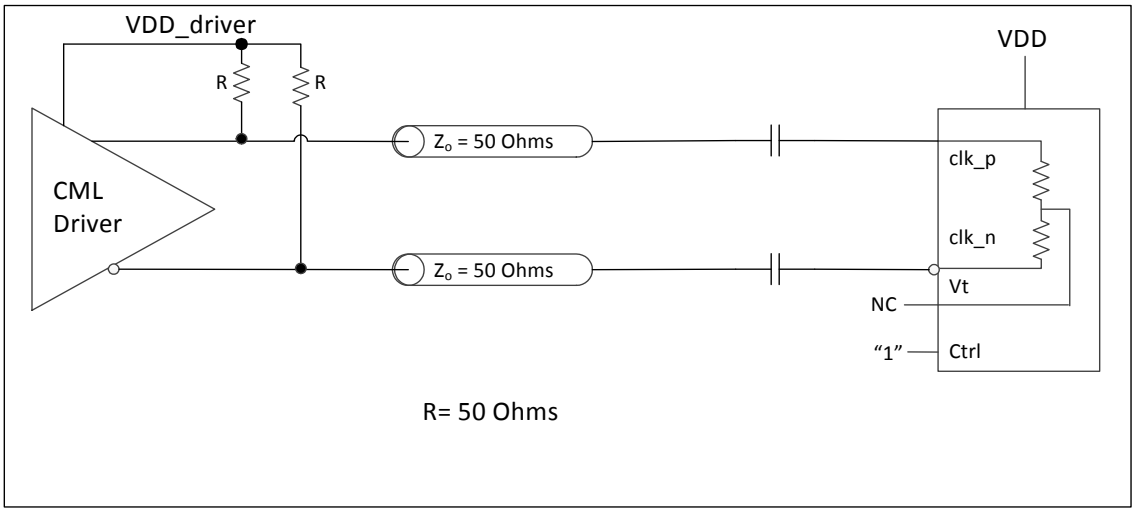


Figure 8 - Clock Input - CML- AC Coupled

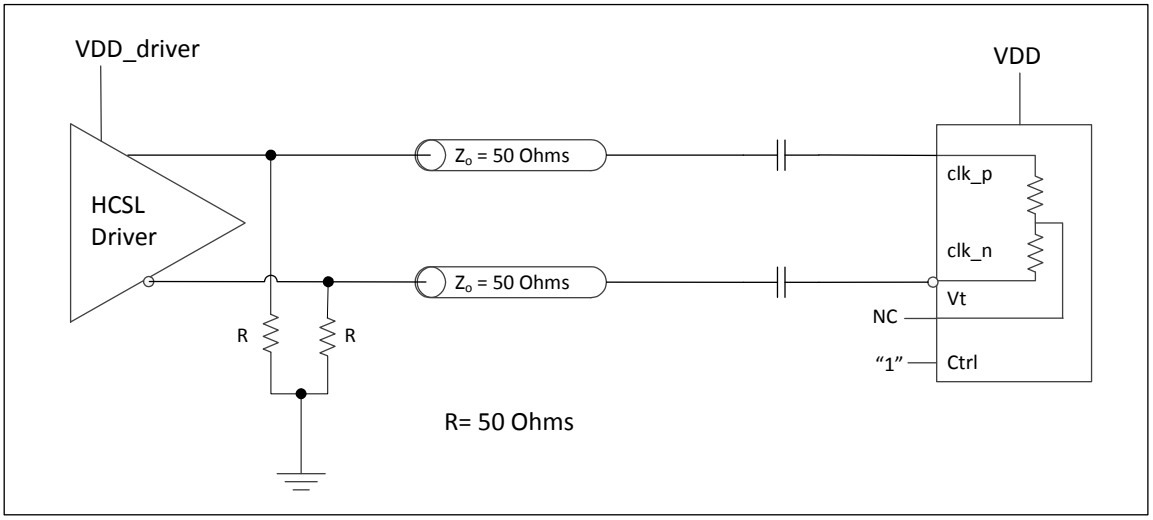


Figure 9 - Clock Input - HCSL- AC Coupled

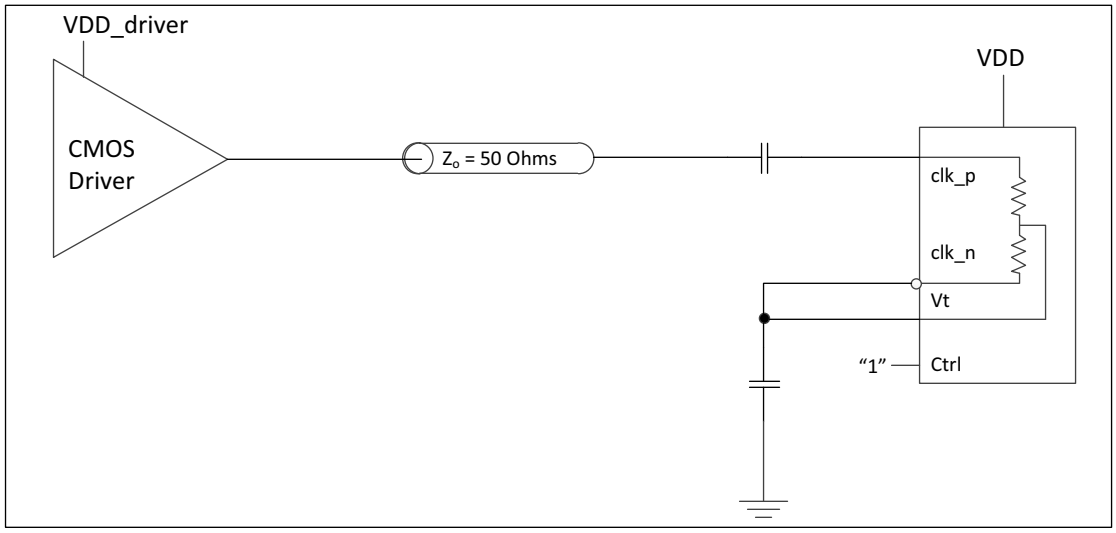


Figure 10 - Clock Input - AC-coupled Single-Ended

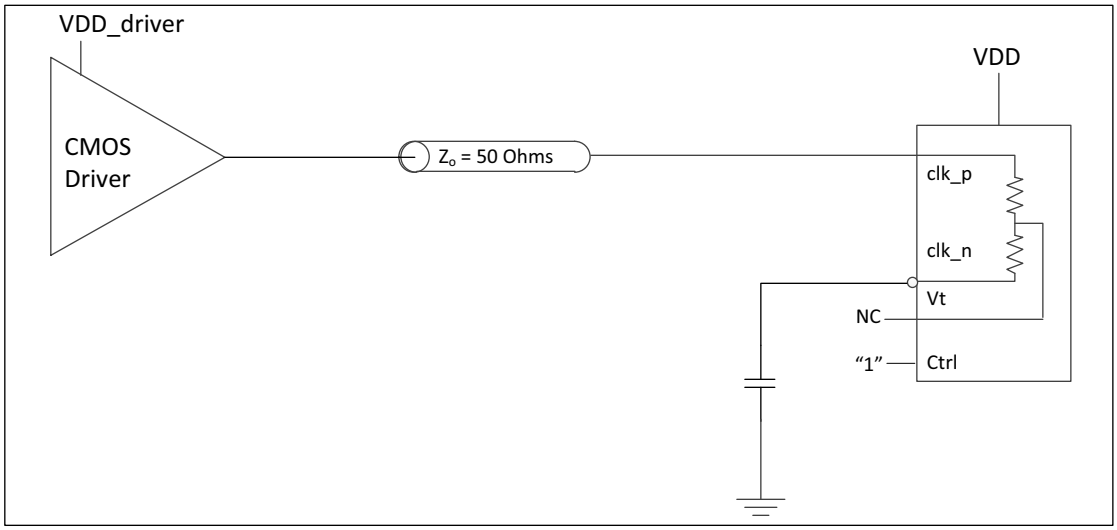


Figure 11 - Clock Input - DC-coupled 3.3V CMOS

3.2 Clock Outputs

LVPECL has a very low output impedance and a differential signal swing between 1V and 1.6 V. A simplified diagram for the output stage is shown in Figure 12.The LVPECL to LVDS output termination is not shown since there is a different device with the same inputs and LVDS outputs.

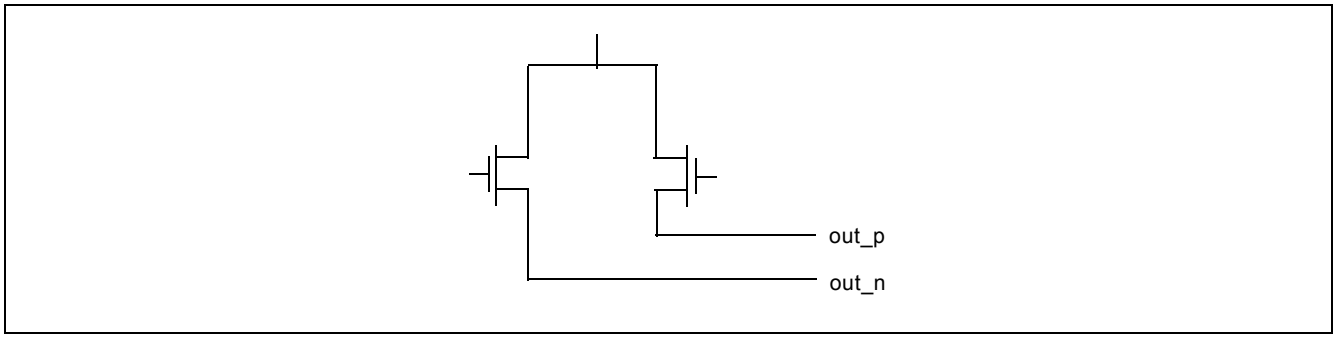


Figure 12 - Simplified Output Driver

The methods to terminate the ZL40201 LVPECL drivers are shown in the following figures.

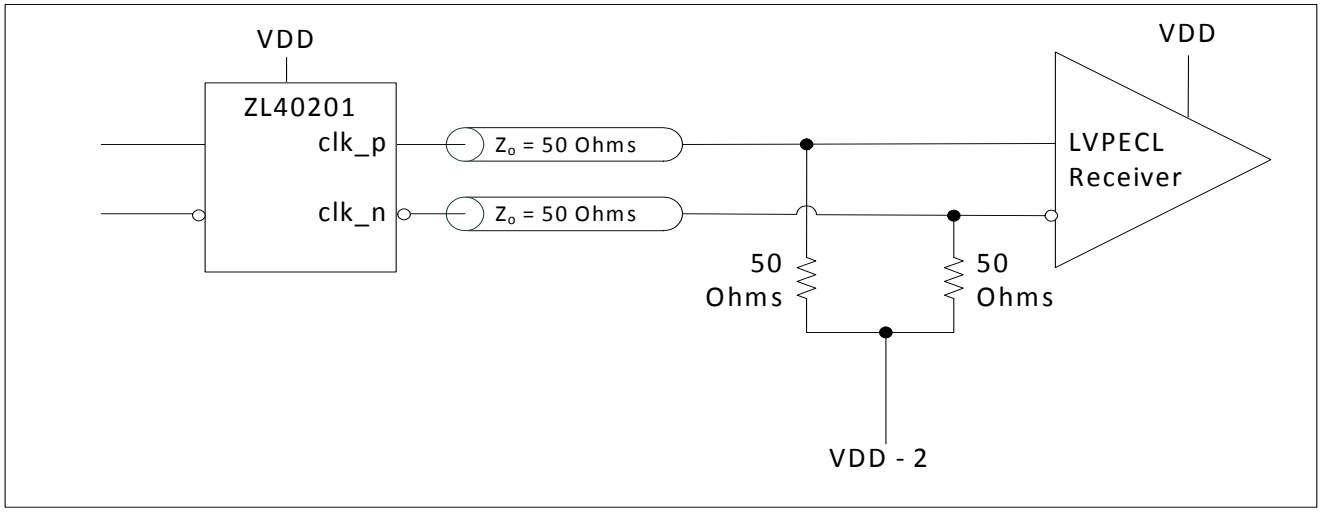


Figure 13 - LVPECL Basic Output Termination

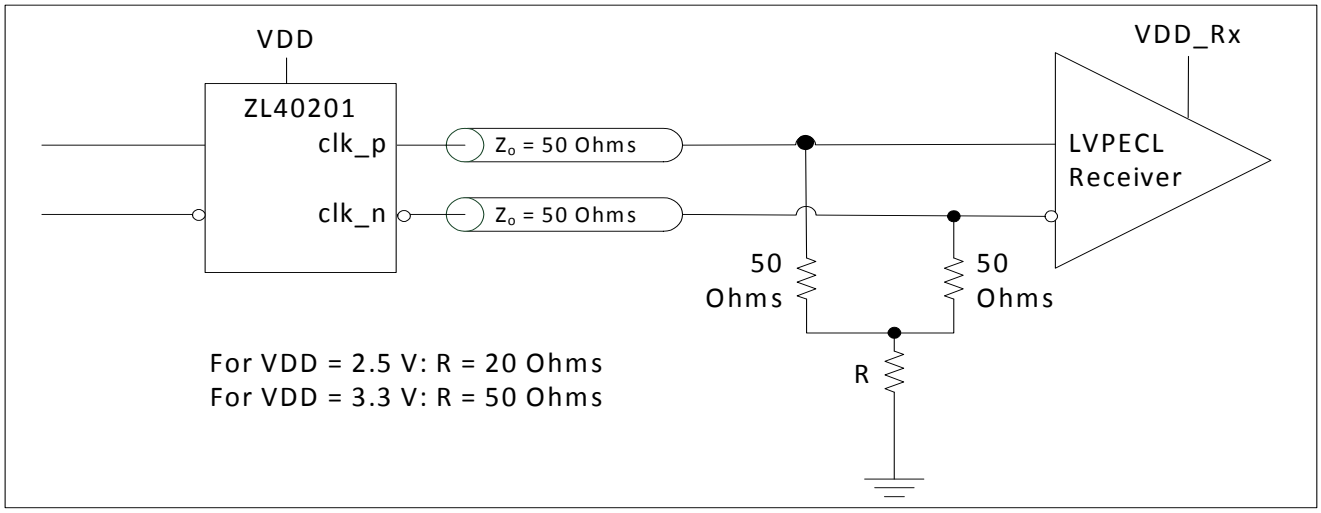


Figure 14 - LVPECL Parallel Output Termination

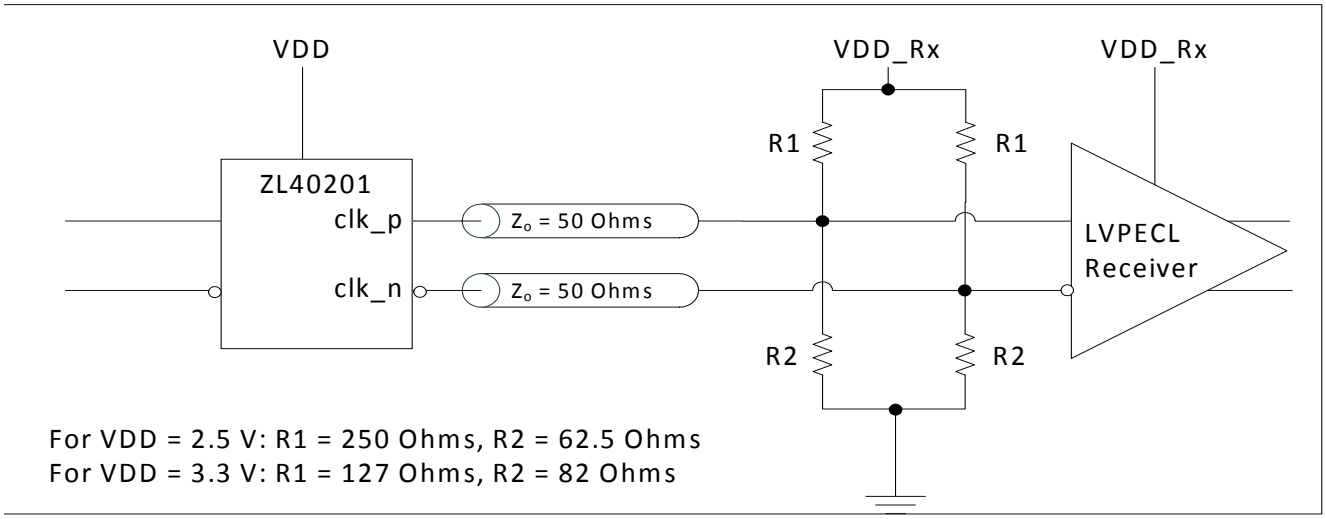


Figure 15 - LVPECL Parallel Thevenin-Equivalent Output Termination

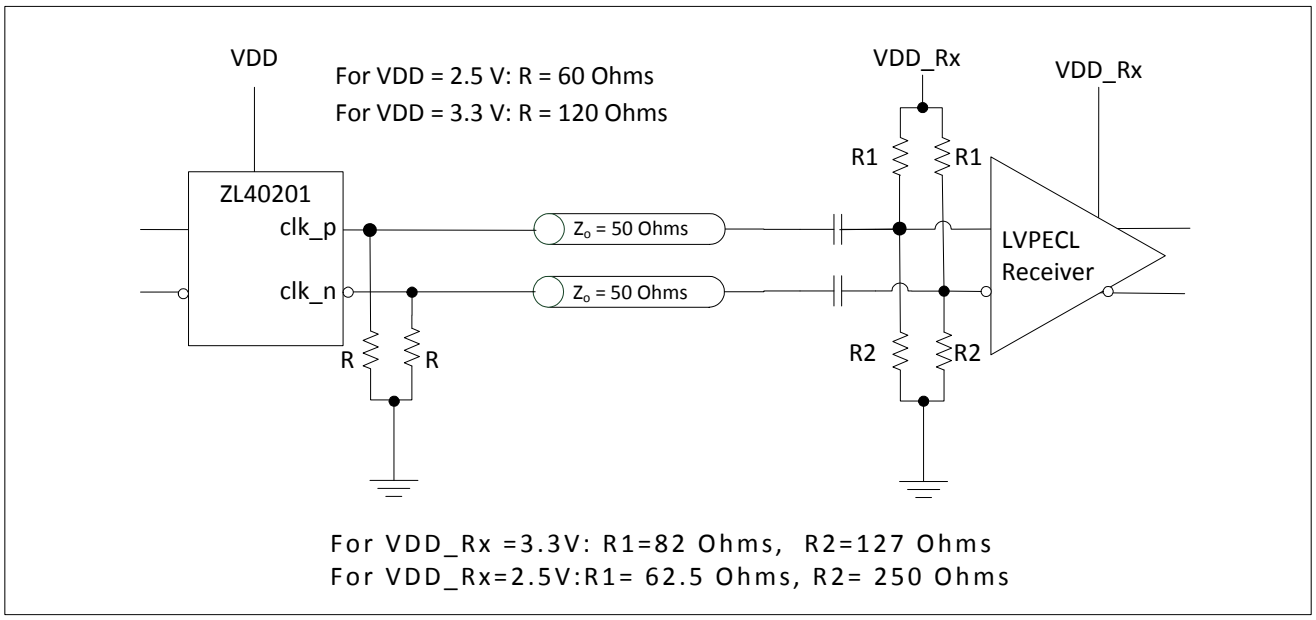


Figure 16 - LVPECL AC Output Termination

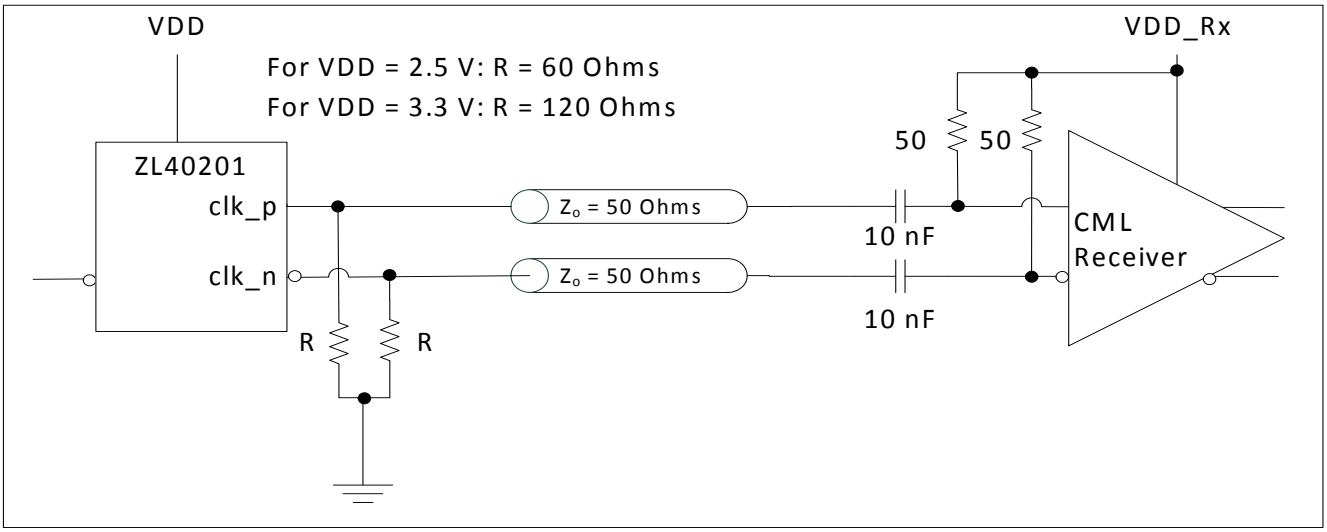


Figure 17 - LVPECL AC Output Termination for CML Inputs

3.3 Device Additive Jitter

The ZL40201 clock fanout buffer is not intended to filter clock jitter. The jitter performance of this type of device is characterized by its additive jitter. Additive jitter is the jitter the device would add to a hypothetical jitter-free clock as it passes through the device. The additive jitter of the ZL40201 is random and as such it is not correlated to the jitter of the input clock signal.

The square of the resultant random RMS jitter at the output of the ZL40201 is equal to the sum of the squares of the various random RMS jitter sources including: input clock jitter; additive jitter of the buffer; and additive random jitter due to power supply noise. There may be additional deterministic jitter sources, but they are not shown in Figure 18.

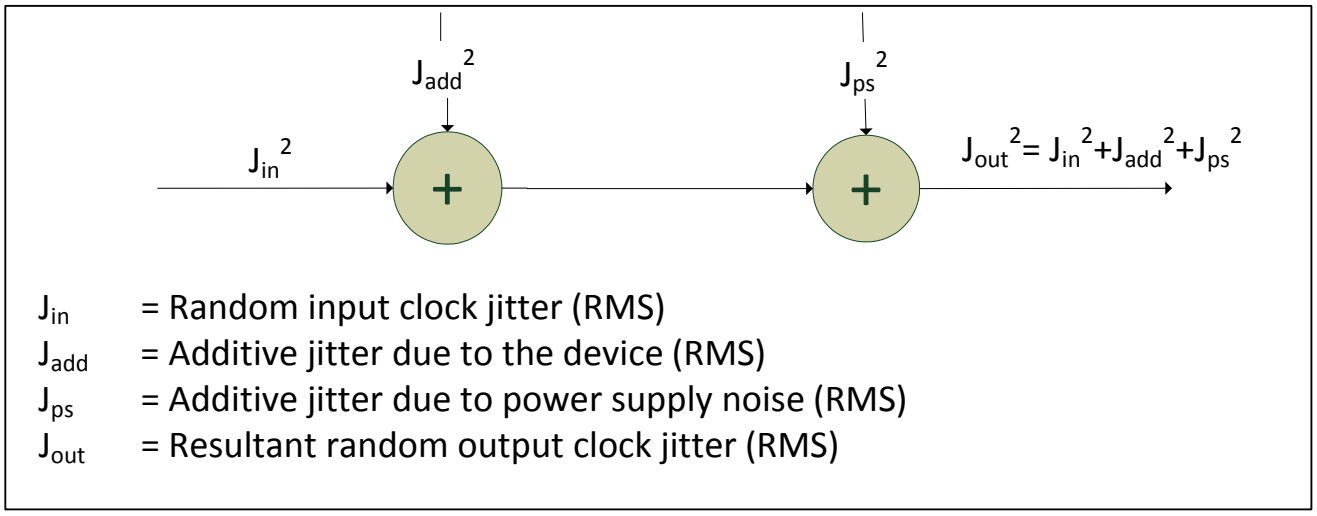


Figure 18 - Additive Jitter

3.4 Power Supply

This device operates with either a 2.5V supply or 3.3V supply.

3.4.1 Sensitivity to power supply noise

Power supply noise from sources such as switching power supplies and high-power digital components such as FPGAs can induce additive jitter on clock buffer outputs. The ZL40201 is equipped with a low drop out (LDO) power regulator and on-chip bulk capacitors to minimize additive jitter due to power supply noise. The LDO regulator on the ZL40201 allows this device to have superior performance even in the presence of external noise sources. TThe on-chip regulation, recommended power supply filtering, and good PCB layout all work together to minimize the additive jitter from power supply noise.

The performance of these clock buffers in the presence of power supply noise is detailed in ZLAN-403, “Power Supply Rejection in Clock Buffers” which is available from Applications Engineering.

3.4.2 Power supply filtering

For optimal jitter performance, the device should be isolated from the power planes connected to its power supply pins as shown in Figure 19.

- 10 µF capacitors should be size 0603 or size 0805 X5R or X7R ceramic, 6.3 V minimum rating
- 0.1 µF capacitors should be size 0402 X5R ceramic, 6.3 V minimum rating
- Capacitors should be placed next to the connected device power pins
- a 0.3 ohm resistor is recommended for the filter shown in Figure 19

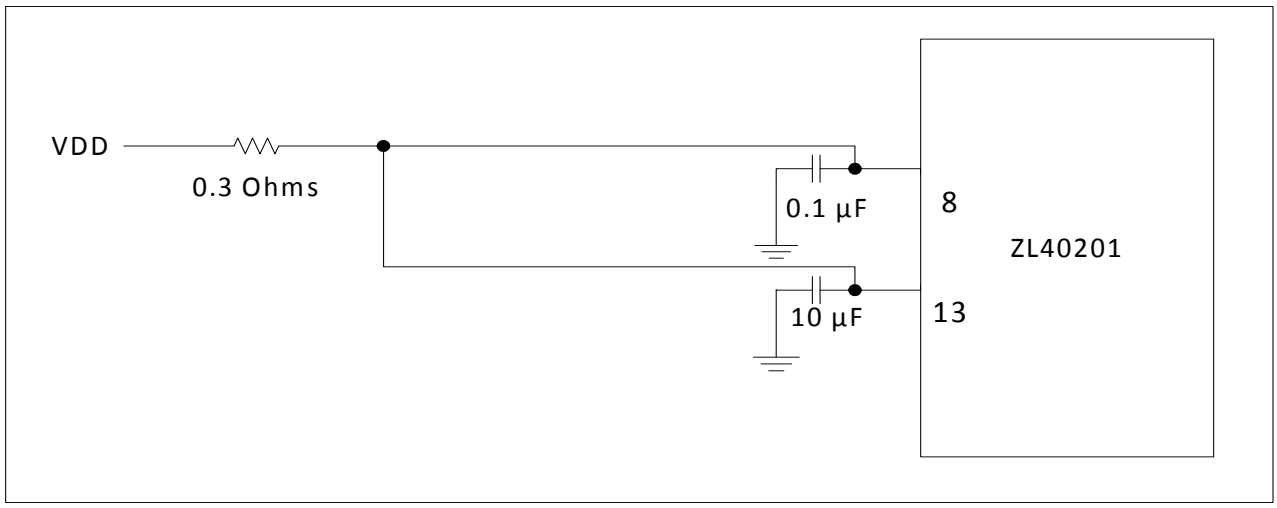


Figure 19 - Decoupling Connections for Power Pins

3.4.3 PCB layout considerations

The power nets in Figure 19 can be implemented either as a plane island or routed power topology without changing the overall jitter performance of the device.

4.0 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Sym.	Min.	Max.	Units
1	Supply voltage	V_{DD_R}	-0.5	4.6	V
2	Voltage on any digital pin	V_{PIN}	-0.5	V_{DD}	V
3	LVPECL output current	I_{out}		30	mA
4	Soldering temperature	T		260	°C
5	Storage temperature	T_{ST}	-55	125	°C
6	Junction temperature	T_j		125	°C
7	Voltage on input pin	V_{input}		V_{DD}	V
8	Input capacitance each pin	C_p		500	fF

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated

Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Supply voltage 2.5 V mode	V_{DD25}	2.375	2.5	2.625	V
2	Supply voltage 3.3 V mode	V_{DD33}	3.135	3.3	3.465	V
3	Operating temperature	T_A	-40	25	85	°C

* Voltages are with respect to ground (GND) unless otherwise stated

DC Electrical Characteristics - Current Consumption

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply current LVPECL drivers - unloaded	I_{dd_unload}		49		mA	Unloaded
2	Supply current LVPECL drivers - loaded (all outputs are active)	I_{dd_load}		88		mA	Including power to $R_L = 50\Omega$

DC Electrical Characteristics - Inputs and Outputs - for 3.3 V Supply

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS control logic high-level input voltage	V_{CIH}	$0.7*V_{DD}$			V	
2	CMOS control logic low-level input voltage	V_{CIL}			$0.3*V_{DD}$	V	
3	CMOS control logic Input leakage current	I_{IL}		1		µA	$V_I = V_{DD}$ or 0 V
4	Differential input common mode voltage	V_{CM}	1.1		2.0	V	
5	Differential input voltage difference	V_{ID}	0.25		1	V	

DC Electrical Characteristics - Inputs and Outputs - for 3.3 V Supply

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
6	Differential input resistance	V_{IR}	80	100	120	ohm	
7	LVPECL output high voltage	V_{OH}	V_{DD}-1.40			V	
8	LVPECL output low voltage	V_{OL}			V_{DD}-1.62	V	
9	LVPECL output differential voltage*	V_{OD}	0.5		0.9	V	

* Parameter measured from 125 to 750 MHz

DC Electrical Characteristics - Inputs and Outputs - for 2.5 V Supply

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS control logic high-level input voltage	V_{CIH}	0.7*V_{DD}			V	
2	CMOS control logic low-level input voltage	V_{CIL}			0.3*V_{DD}	V	
3	CMOS control logic Input leakage current	I_{IL}		1		µA	V_I = V_{DD} or 0 V
4	Differential input common mode voltage	V_{CM}	1.1		1.6	V	
5	Differential input voltage difference	V_{ID}	0.25		1	V	
6	Differential input resistance	V_{IR}	80	100	120	ohm	
7	LVPECL output high voltage	V_{OH}	V_{DD}-1.40			V	
8	LVPECL output low voltage	V_{OL}			V_{DD}-1.62	V	
9	LVPECL output voltage differentia*I	V_{OD}	0.4		0.9	V	

* Parameter measured from 125 to 750 MHz

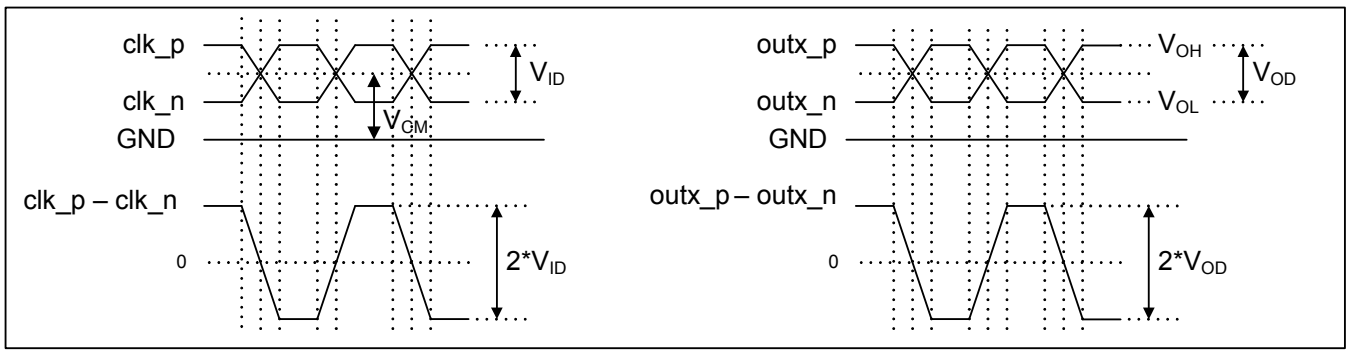


Figure 20 - Differential Voltage Definition

AC Electrical Characteristics* - Inputs and Outputs (see Figure 21) - for 3.3 V supply.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Maximum Operating Frequency	$1/t_p$			750	MHz	
2	input to output clock propagation delay	t_{pd}	0	1	2	ns	
3	output to output skew	$t_{out2out}$		50	100	ps	
4	part to part output skew	$t_{part2part}$		80	300	ps	
5	Output clock Duty Cycle degradation	t_{PWH}/ t_{PWL}	-2	0	2	Percent	
6	LVPECL Output Slew Rate	r_{sl}	0.75	1.2		V/ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions

AC Electrical Characteristics* - Inputs and Outputs (see Figure 21) - for 2.5 V supply.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Maximum Operating Frequency	$1/t_p$			750	MHz	
2	input to output clock propagation delay	t_{pd}	0	1	2	ns	
3	output to output skew	$t_{out2out}$		50	100	ps	
4	part to part output skew	$t_{part2part}$		80	300	ps	
5	Output clock Duty Cycle degradation	t_{PWH}/ t_{PWL}	-2	0	2	Percent	
6	LVPECL Output Slew Rate	r_{sl}	0.75	1.2		V/ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions

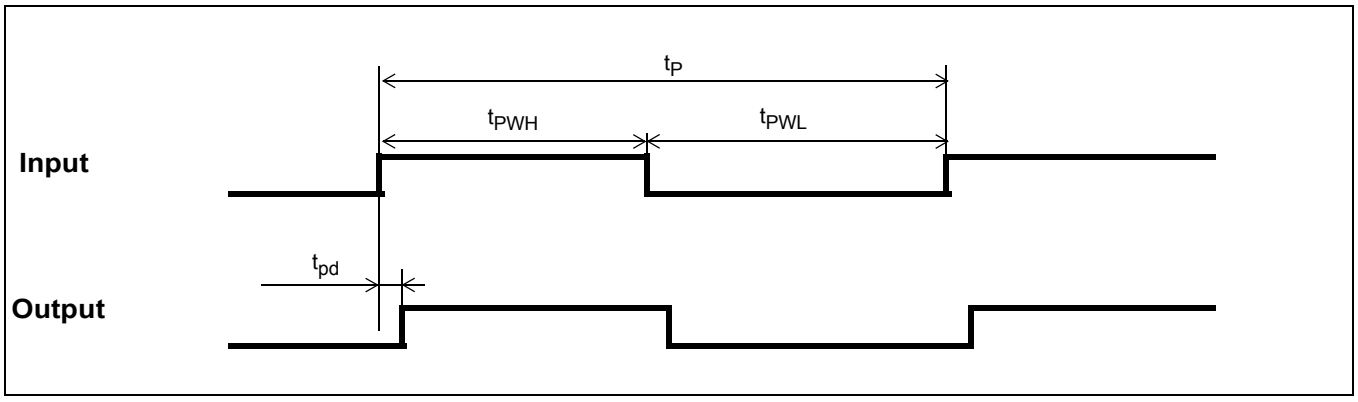


Figure 21 - Input To Output Timing

5.0 Performance Characterization

Additive Jitter at 2.5 V*

	Output Frequency (MHz)	Jitter Measurement Filter	Typical (fs)	Notes
1	125	12 kHz - 20 MHz	105	
2	212.5	12 kHz - 20 MHz	108	
3	311.04	12 kHz - 20 MHz	96	
4	425	12 kHz - 20 MHz	79	
5	500	12 kHz - 20 MHz	69	
6	622.08	12 kHz - 20 MHz	56	
7	750	12 kHz - 20 MHz	41	

*The values in this table were taken with an aproximate slew rate of 0.8 V/ns.

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Additive Jitter at 3.3*V

	Output Frequency (MHz)	Jitter Measurement Filter	Typical (fs)	Notes
1	125	12 kHz - 20 MHz	108	
2	212.5	12 kHz - 20 MHz	108	
3	311.04	12 kHz - 20 MHz	97	
4	425	12 kHz - 20 MHz	79	
5	500	12 kHz - 20 MHz	69	
6	622.08	12 kHz - 20 MHz	56	
7	750	12 kHz - 20 MHz	40	

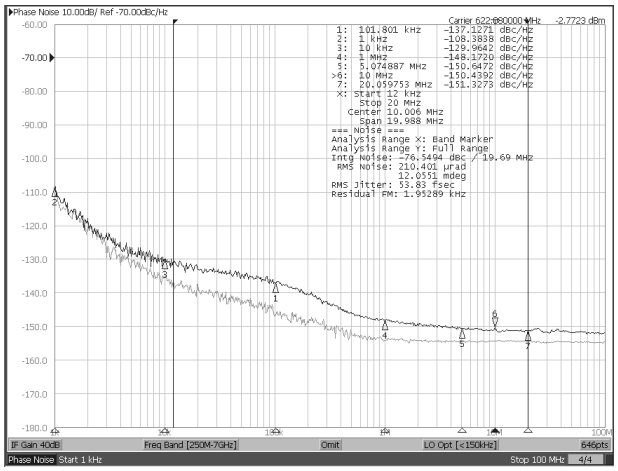
*The values in this table were taken with an aproximate slew rate of 0.8 V/ns.

Additive Jitter from a Power Supply Tone*

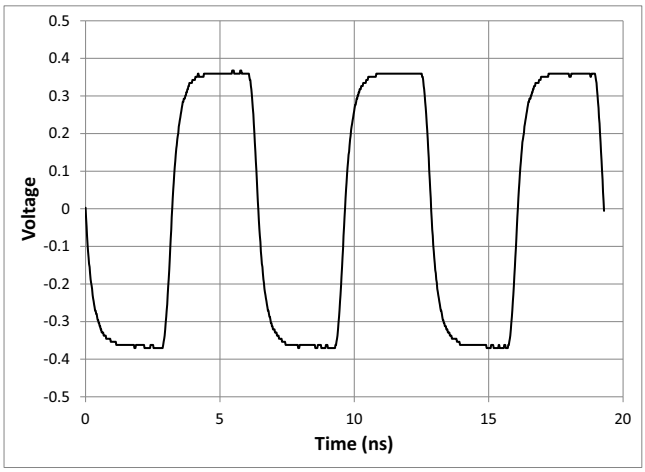
Carrier frequency	Parameter	Typical	Units	Notes
125MHz	25 mV at 100 kHz	132	fs RMS	
750MHz	25 mV at 100 kHz	82	fs RMS	

* The values in this table are the additive periodic jitter caused by an interfering tone typically caused by a switching power supply. For this test, measurements were taken over the full temperature and voltage range for V_{DD} = 3.3 V. The magnitude of the interfering tone is measured at the DUT.

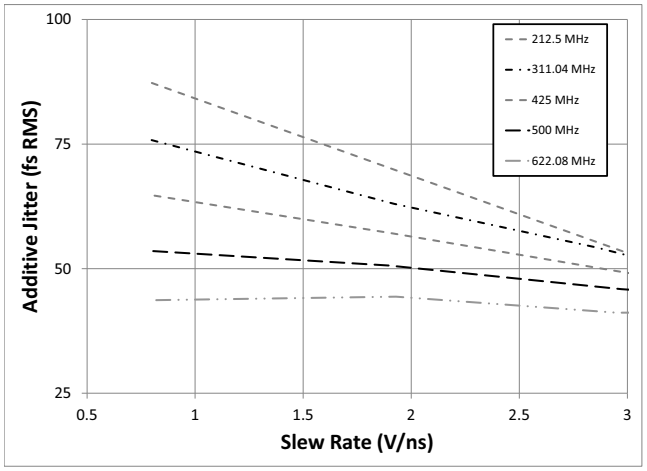
6.0 Typical Behavior



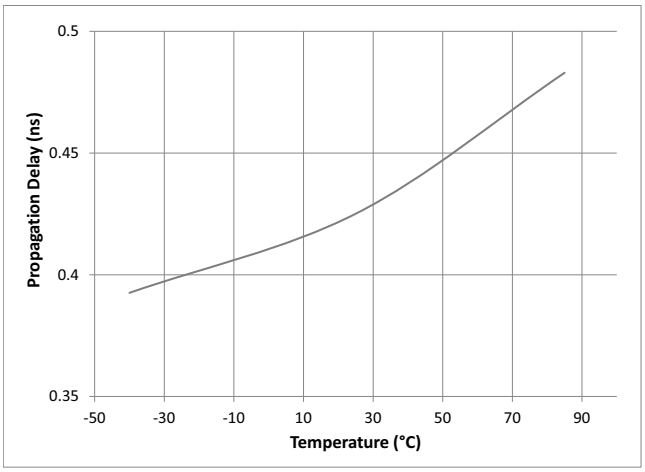
Typical Phase Noise at 622.08 MHz



Typical Waveform at 155.52 MHz

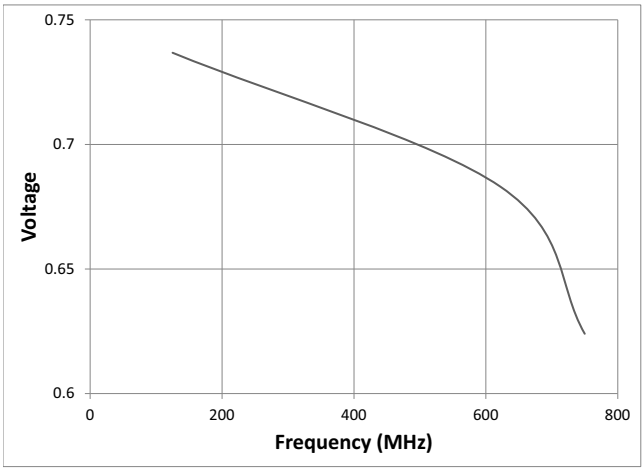


Input Slew Rate versus Additive Jitter

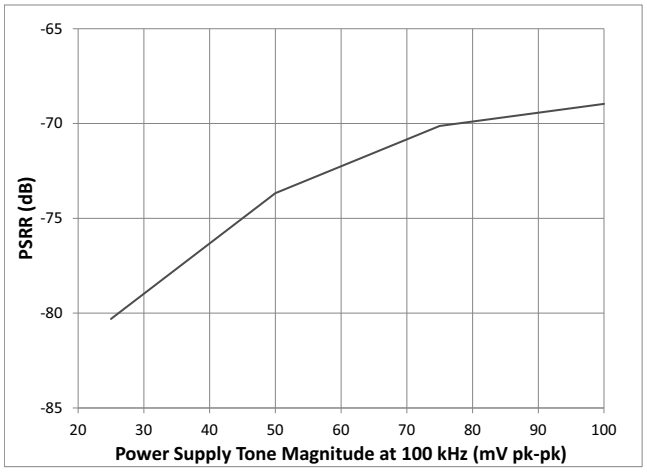


Propagation Delay versus Temperature

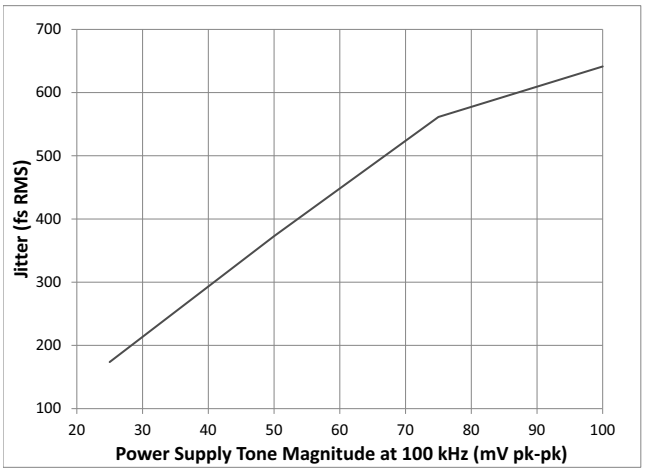
Note: This is for a single device. For more details see the characterization section.



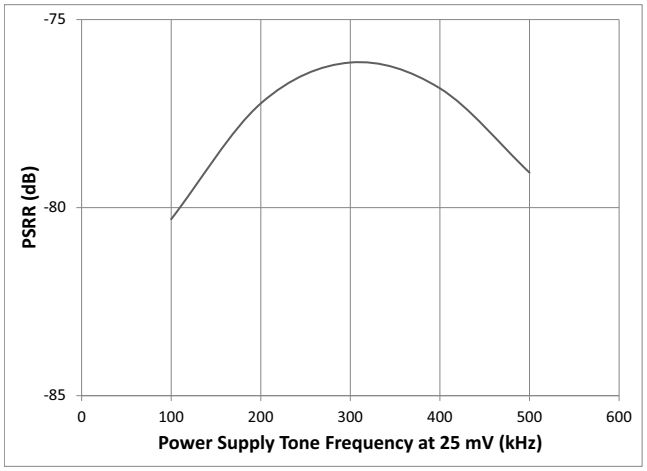
V_{OD} versus Frequency



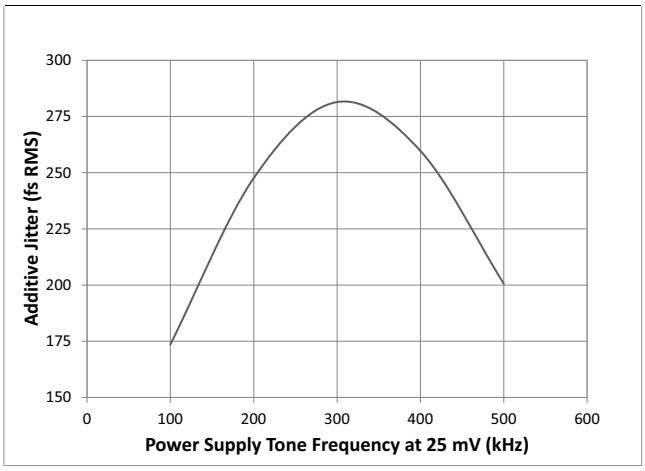
Power Supply Tone Magnitude versus PSRR (at 100 kHz) at 125 MHz



Power Supply Tone Magnitude versus Additive Jitter (at 100 kHz) at 125 MHz



Power Supply Tone Frequency (at 25 mV) versus PSRR at 125 MHz



Power Supply Tone Frequency (at 25 mV) versus Additive Jitter at 125 MHz

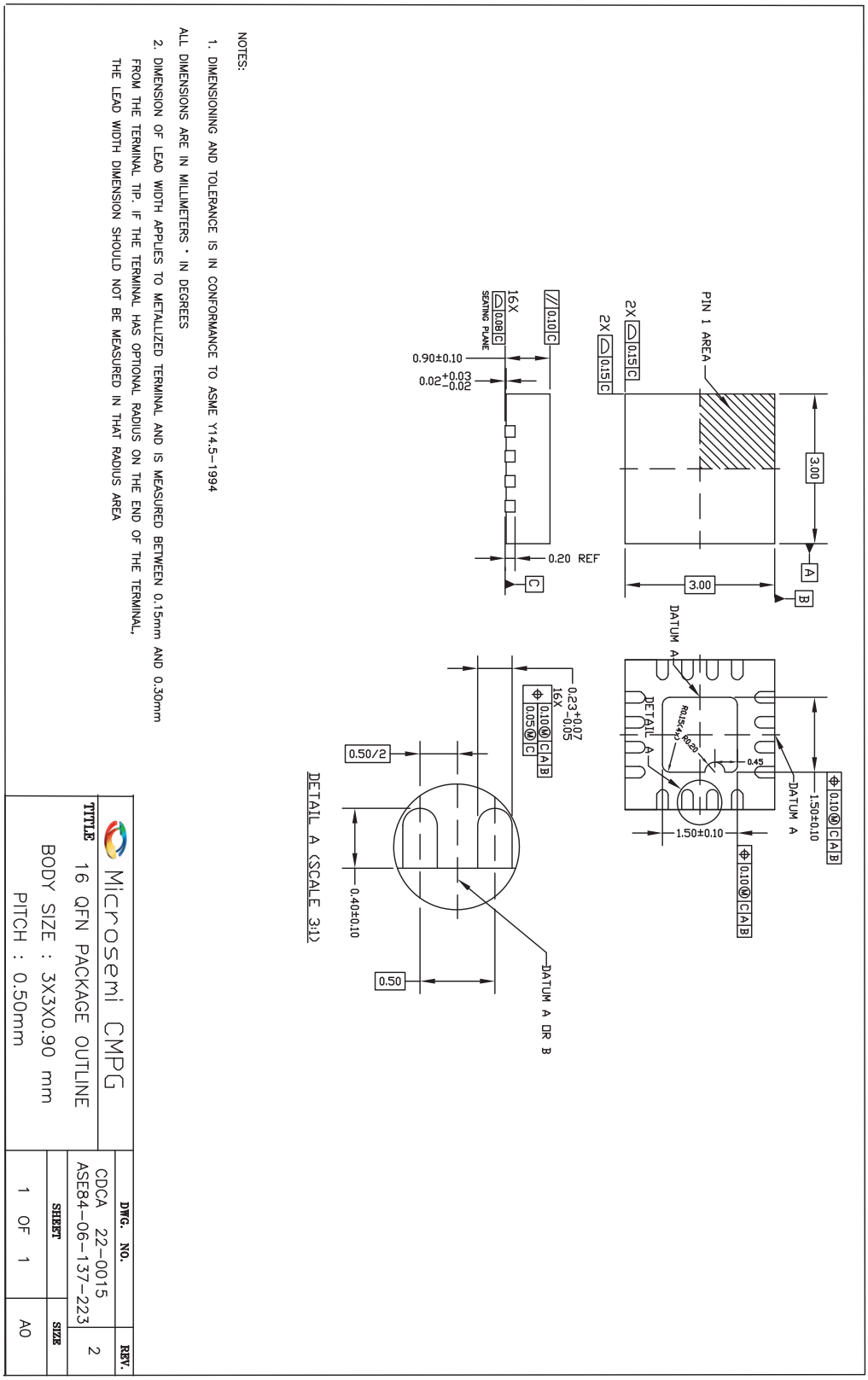
7.0 Package Thermal Characteristics

Thermal Data

Parameter	Symbol	Test Condition	Value	Unit
Junction to Ambient Thermal Resistance	Θ_{JA}	Still Air 1 m/s 2 m/s	67.9 61.6 58.1	^{o}C/W
Junction to Case Thermal Resistance	Θ_{JC}	Still Air	44.1	^{o}C/W
Junction to Board Thermal Resistance	Θ_{JB}	Still Air	23.2	^{o}C/W
Maximum Junction Temperature*	T_{jmax}		125	^{o}C
Maximum Ambient Temperature	T_A		85	^{o}C

* Proper thermal management must be practiced to ensure that T_{jmax} is not exceeded.

8.0 Mechanical Drawing



NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994

ALL DIMENSIONS ARE IN MILLIMETERS ' IN DEGREES

2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Microsemi CMPG

TITLE: 16 QFN PACKAGE OUTLINE
BODY SIZE : 3X3X0.90 mm
PITCH : 0.50mm

DWG. NO.	REV.
CDCA 22-0015 ASE84-06-137-223	2

SIZE	SHEET
A0	1 OF 1

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