High Input Voltage, Adjustable 3-Terminal Linear Regulator

Features

- 13.2 to 100V input voltage range
- Stable with 100nF output capacitor
- Adjustable 1.20 to 88V output regulation
- 5% reference voltage tolerance
- Output current limiting, 50mA min.
- 10µA typical ADJ current
- Over temperature protection
- Available in 3 different packages

Applications

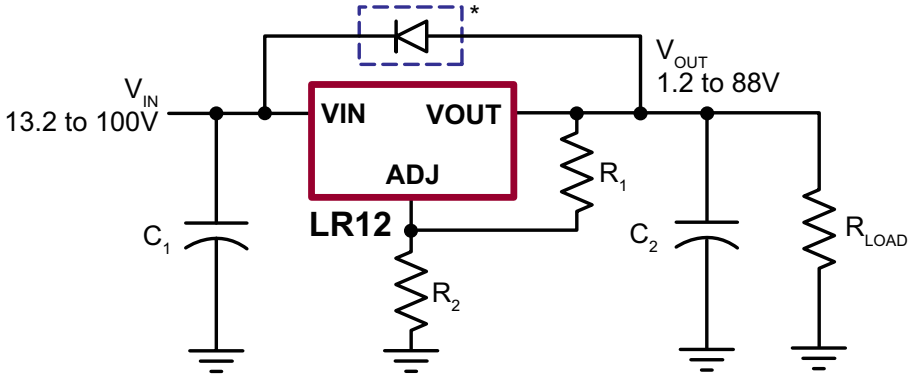
- DC/DC SMPS startup circuits
- Adjustable high voltage constant current sources
- Industrial controls
- Motor controls
- Battery powered systems
- Power supplies
- Telecom applications
- LED drivers
- Automotive applications

General Description

The Supertex LR12 is a high voltage, low output current, adjustable linear regulator. It has a wide operating input voltage range of 13.2 - 100V. The output voltage can be adjusted from 1.20 - 88V, provided that the input voltage is at least 12V greater than the output voltage. The output voltage can be adjusted by means of two external resistors R_1 and R_2 as shown in the typical application circuits. The LR12 regulates the voltage difference between VOUT and ADJ pins to a nominal value of 1.20V. The 1.20V is amplified by the external resistor ratio R_1 and R_2. An internal constant bias current of typically 10µA is connected to the ADJ pin. This increases V_{OUT} by a constant voltage of 10µA times R_2.

The LR12 has current limiting and temperature limiting. The output current limit is 100mA maximum and the minimum temperature limit is 125°C. An output short circuit current will therefore be limited to 100mA maximum. When the junction temperature reaches its temperature limit, the output current and/or output voltage will decrease to keep the junction temperature from exceeding its temperature limit. For SMPS start-up circuit applications, the LR12 turns off when an external voltage greater than the output voltage of the LR12 is applied to VOUT of the LR12. To maintain stability, a bypass capacitor of 100nF or larger and a minimum DC output current of 500µA are required.

LR12 Typical Application



* *Required for conditions where V_{IN} is less than V_{OUT}.*

Ordering Information

Part Number	Package Options	Packing
LR12K4-G	TO-252 (D-PAK)	2000/Reel
LR12LG-G	8-Lead SOIC	2500/Reel
LR12N3-G	TO-92	1000/Bag
LR12N3-G P002	TO-92	2000/Reel
LR12N3-G P003	TO-92	2000/Reel
LR12N3-G P005	TO-92	2000/Reel
LR12N3-G P013	TO-92	2000/Reel
LR12N3-G P014	TO-92	2000/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

Parameter	Value
V_{IN-ADJ}	-0.5V to +120V
$V_{OUT-ADJ}$	-10V to +10V
V_{IN} - V_{OUT}	-0.5V to +120V
Operating ambient temperature	-40°C to +85°C
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C
Power Dissipation @ T_A = 25°C TO-252 (D-PAK) 8-Lead SOIC TO-92	 2.0W 1.8W 0.6W

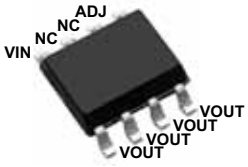
Typical Thermal Resistance

Package	θ_{ja} (°C/W)
TO-252	81°C/W
8-Lead SOIC	101°C/W
TO-92	132°C/W

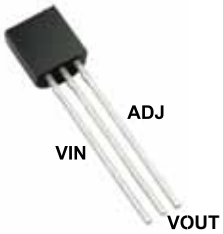
Pin Configuration



TO-252 (D-PAK)



8-Lead SOIC



TO-92

Product Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____= "Green" Packaging

Package may or may not include the following marks: Si or

TO-252 (D-PAK)



YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC



Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92

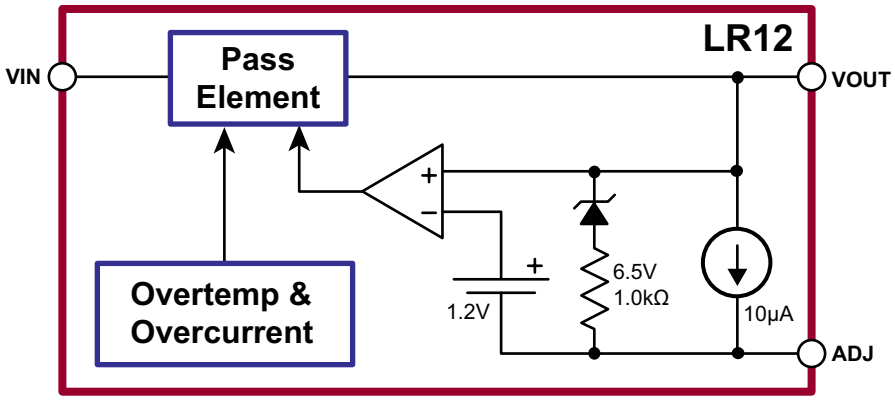
Electrical Characteristics *(Test conditions unless otherwise specified: -40°C < T_A < +85°C)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{IN} - V_{OUT}	Input to output voltage difference	12	-	98.8	V	---
V_{OUT}	Overall output voltage regulation	1.14	1.20	1.26	V	13.2V < V_{IN} <100V, R_1 = 2.4KΩ, R_2 = 0
ΔV_{OUT}	Line regulation	-	0.003	0.03	%/V	15V < V_{IN} <100V, V_{OUT} = 5.0V, I_{OUT} = 0.5A
	Load regulation	-	1.4	3.0	%	V_{IN} = 15V, V_{OUT} = 5.0V, 0.5mA< I_{OUT}<50mA
	Temperature regulation	-1.0	-	+1.0	%	V_{IN} = 15V, V_{OUT} = 5.0V, I_{OUT} = 10mA, -40°C < T_A < 85°C

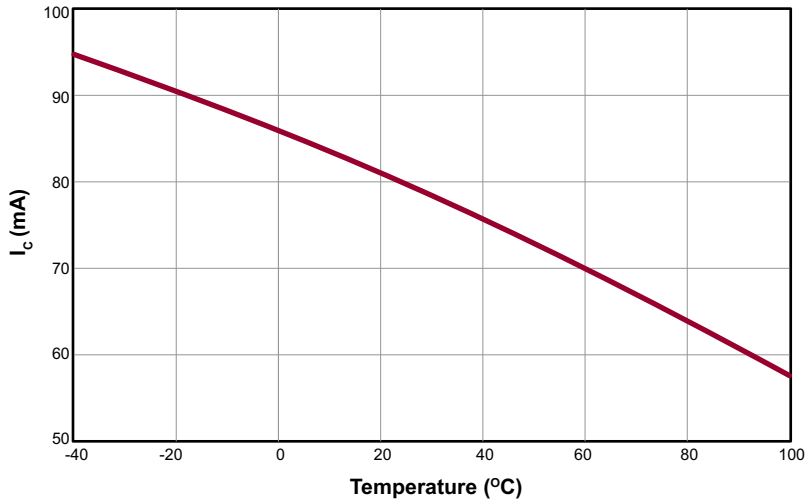
Electrical Characteristics *(cont.)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output current limit	50	-	100	ma	$T_J < 85^oC$, $V_{IN} - V_{OUT} < 12V$
		-	-	-0.5		$T_J < 125^oC$, $V_{IN} - V_{OUT} < 100V$
	Minimum output current	0.5	-	-	mA	Includes R_1 and load current
I_{ADJ}	Adjust output current	5.0	10	15	µA	---
C2	Minimum output load capacitance	100	-	-	nF	---
DV_{OUT}/D_{VIN}	Ripple rejection ratio	50	60	-	dB	120Hz, V_{OUT} = 5.0V
T_{LIMIT}	Junction temperature limit	125	-	-	^oC	---

Functional Block Diagram



Current Limit



Typical Application Circuits

Figure 1: High Input Voltage, 5.0V Output Linear Regulator

* *Required for conditions where V_{IN} is less than V_{OUT}*

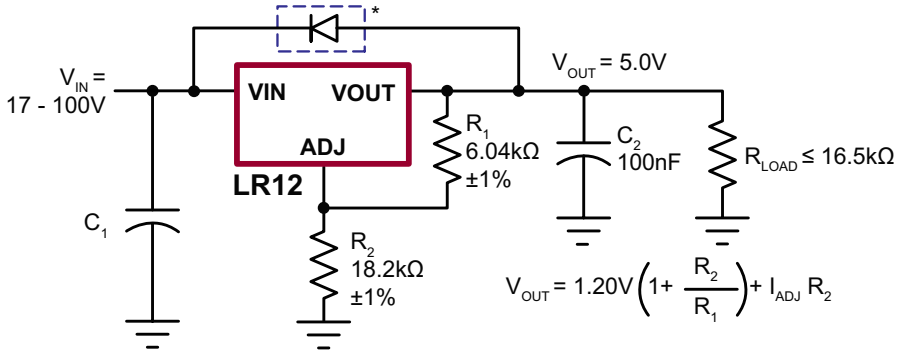


Figure 2: SMPS Start-Up Circuit

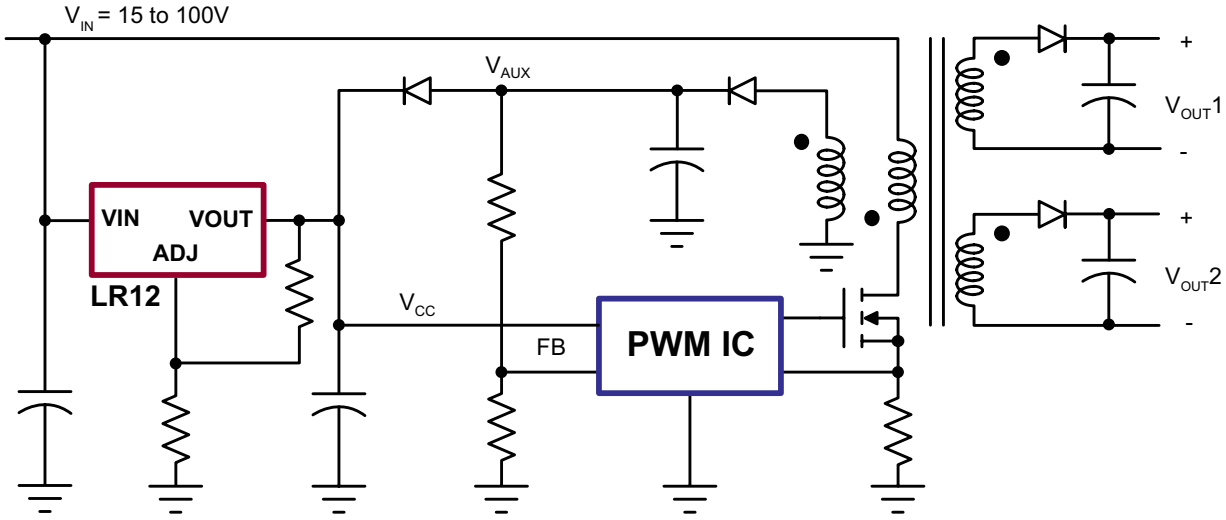
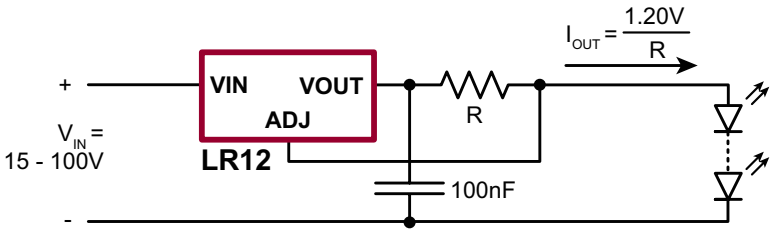
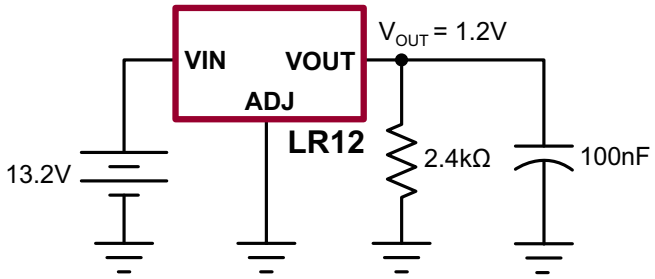
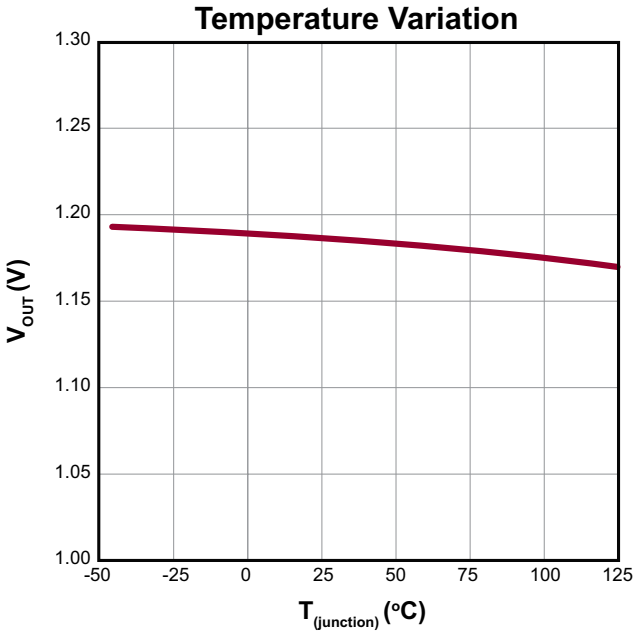


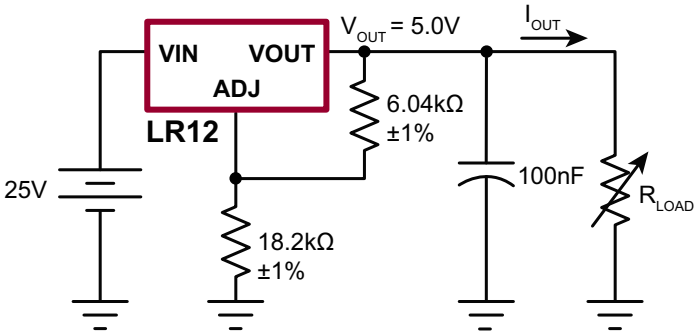
Figure 3: High Voltage Adjustable Constant Current Source

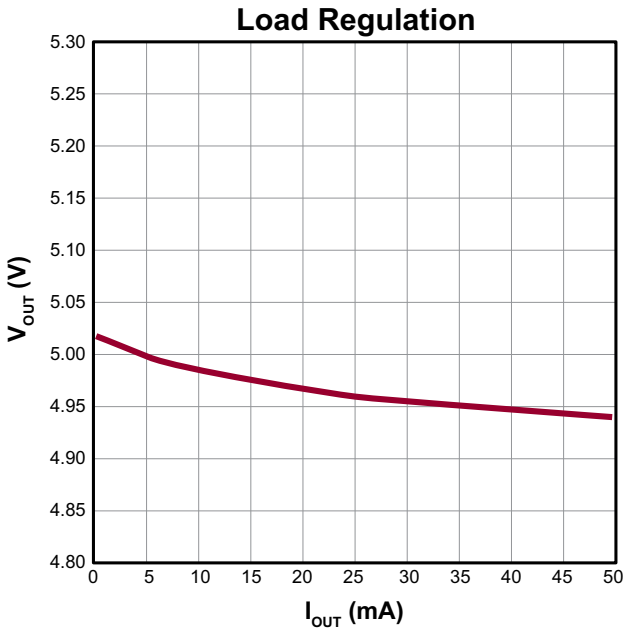


Typical Performance Curves

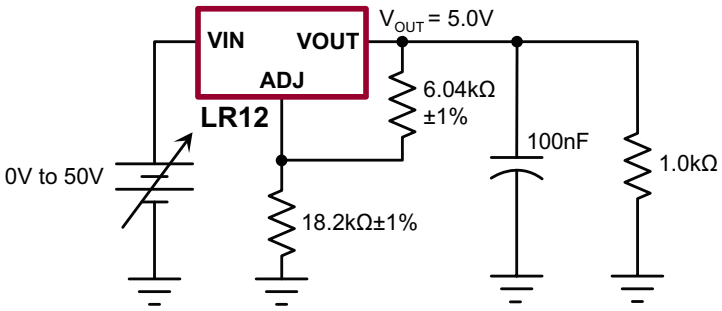


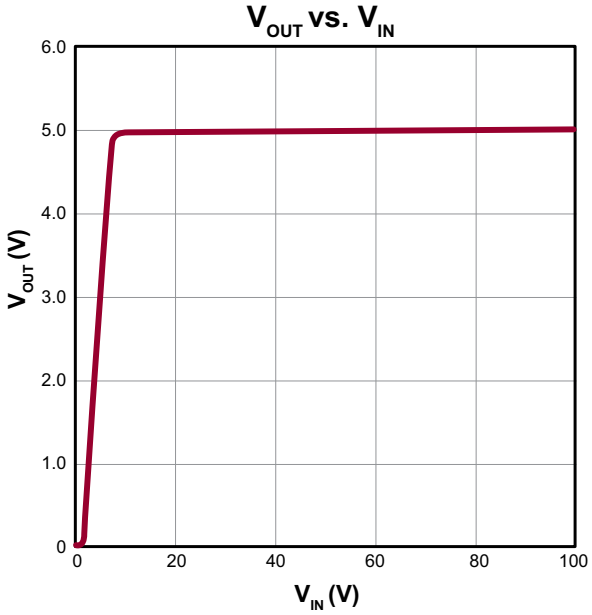


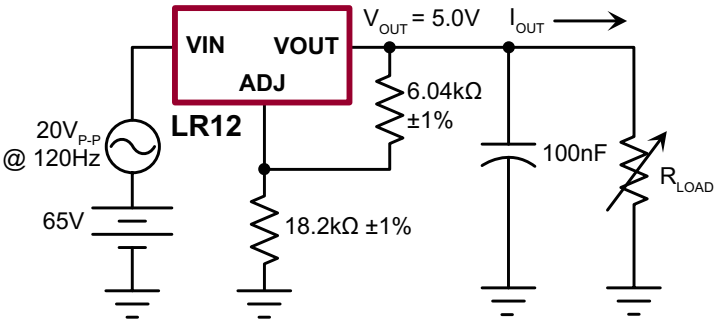


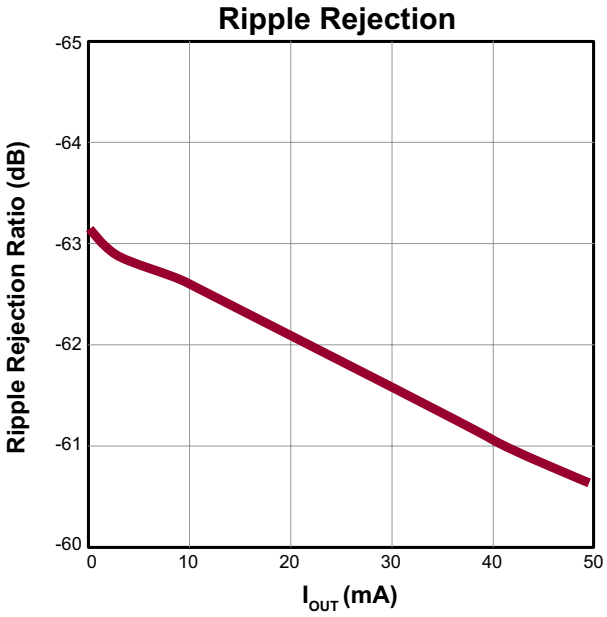


Typical Performance Curves *(cont.)*



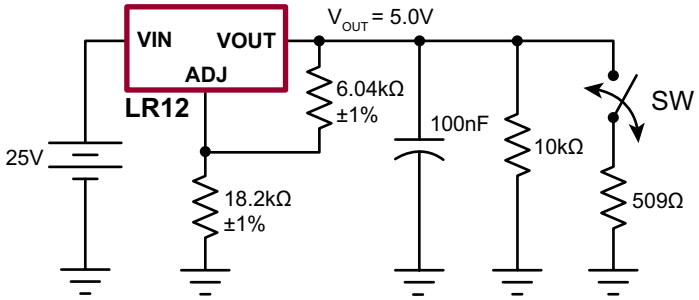




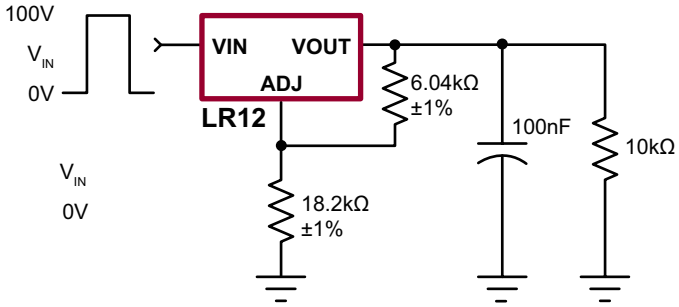


Typical Performance Curves *(cont)*

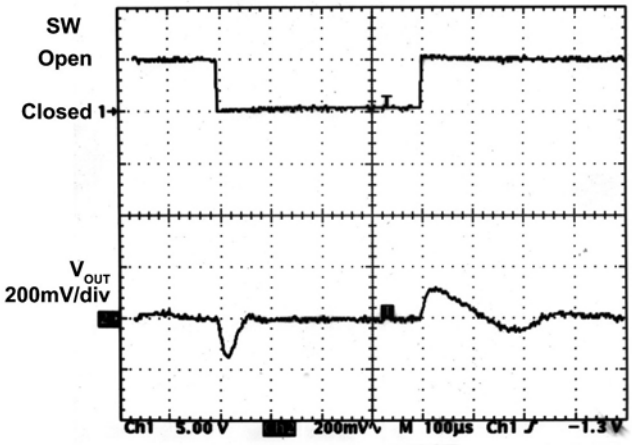
Load Transient Response



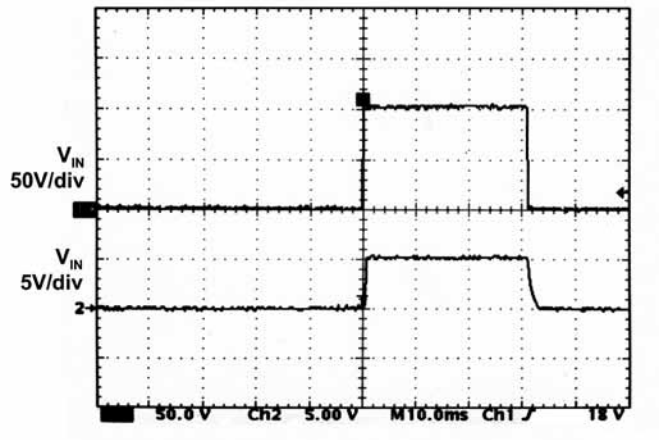
Line Transient Response



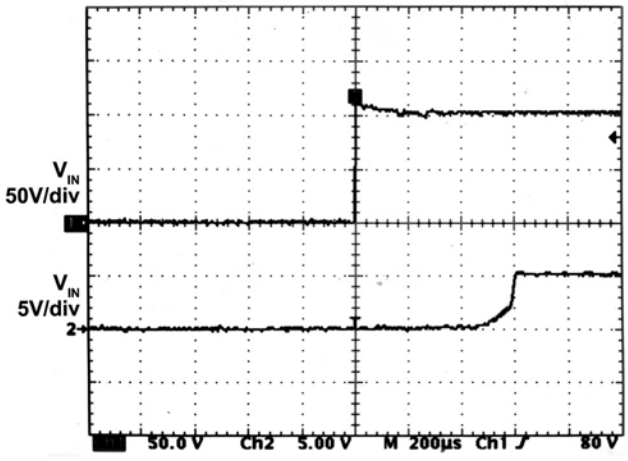
Load Transient Response, Load = 509Ω



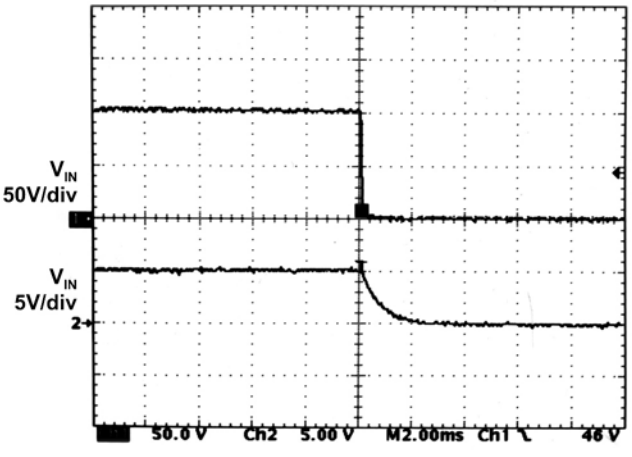
Line Turn On/Off Response



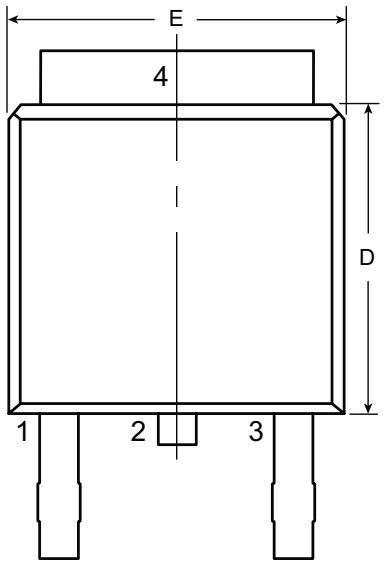
Line Power Up Transient



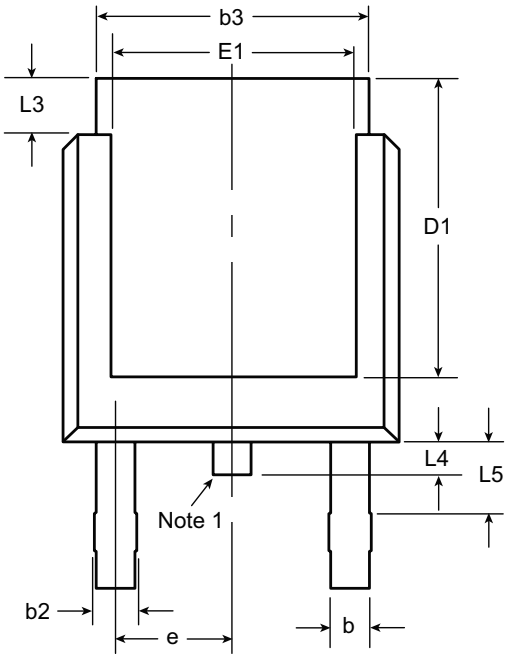
Line Power Down Transient



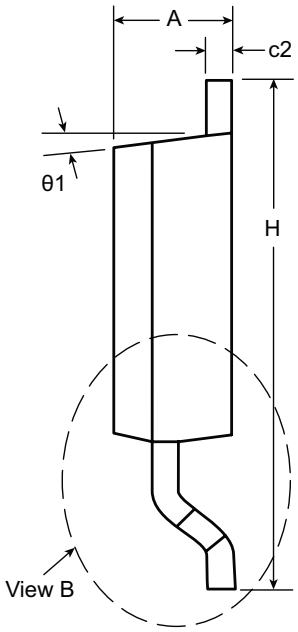
3-Lead TO-252 (D-PAK) Package Outline (K4)



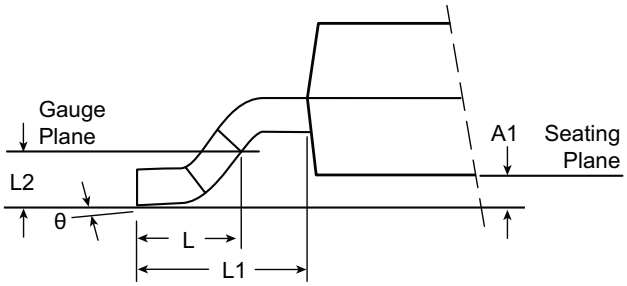
Front View



Rear View



Side View



View B

Note:

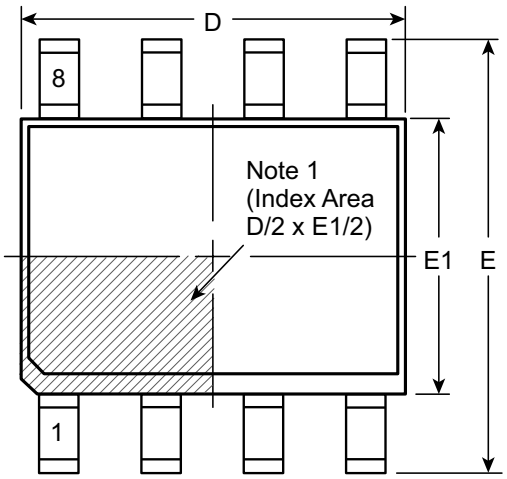
1. *Although 4 terminal locations are shown, only 3 are functional. Lead number 2 was removed.*

Symbol		A	A1	b	b2	b3	c2	D	D1	E	E1	e	H	L	L1	L2	L3	L4	L5	θ	θ1
Dimen-sion (inches)	MIN	.086	.000*	.025	.030	.195	.018	.235	.205	.250	.170	.090 BSC	.370	.055	.108 REF	.020 BSC	.035	.025*	.045	0^0	0^0
	NOM	-	-	-	-	-	-	.240	-	-	-		-	.060			-	-	-	-	-
	MAX	.094	.005	.035	.045	.215	.035	.245	.217*	.265	.182*		.410	.070			.050	.040	.060	10^0	15^0

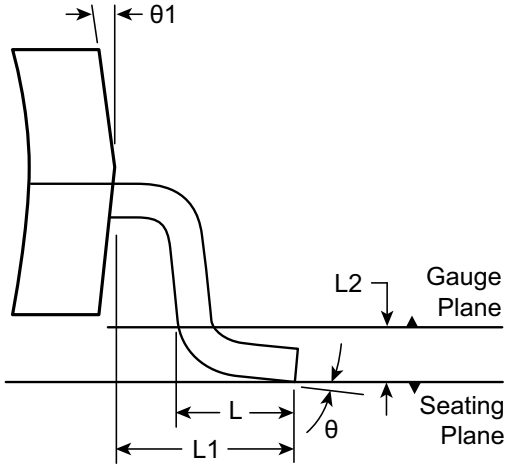
JEDEC Registration TO-252, Variation AA, Issue E, June 2004.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.
Supertex Doc. #: *DSPD-3TO252K4, Version E091009.*

8-Lead SOIC (Narrow Body) Package Outline (LG)

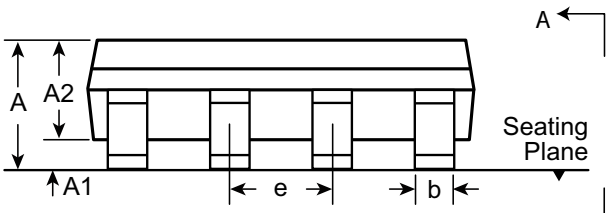
4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



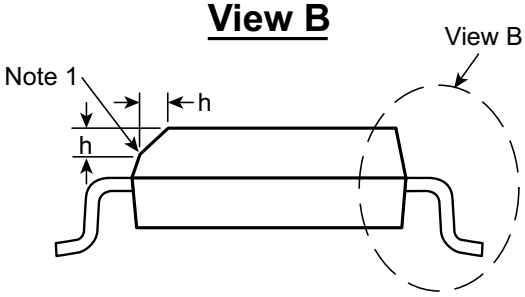
Top View



View B



Side View



View A-A

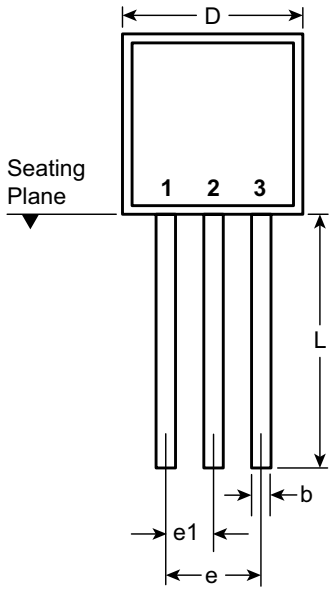
Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

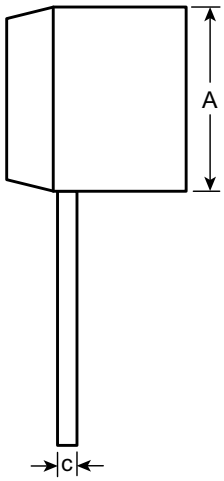
Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-8SOLGTG, Version I041309.*

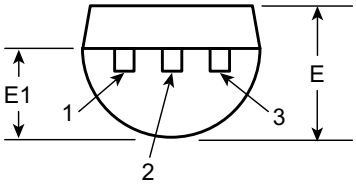
3-Lead TO-92 Package Outline (N3)



Front View



Side View



Bottom View

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
***Supertex Doc.#:** DSPD-3TO92N3, Version E041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc. does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." **Supertex inc.** does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the **Supertex inc.** (website: http//www.supertex.com)

©2013 **Supertex inc.** All rights reserved. Unauthorized use or reproduction is prohibited.

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
www.supertex.com