# IGLOO® PLUS Low Power Flash FPGAs with Flash*Freeze Technology

## INTRODUCTION

The IGLOO® PLUS family of flash FPGAs, based on a 130 nm flash process, offers the lowest power FPGA, a single-chip solution, small-footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOO PLUS devices enables entering and exiting an ultra-low power mode that consumes as little as 5 µW while retaining the design information, SRAM content, registers, and I/O states. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low power consumption while the IGLOO PLUS device is completely functional in the system. This allows the IGLOO PLUS device to control system power management based on external inputs (for example, scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOO PLUS devices the advantage of being a secure, low power, single-chip solution that is Instant On. IGLOO PLUS is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO PLUS devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). IGLOO PLUS devices have up to 125 k system gates, supported with up to 36 kbits of true dual-port SRAM and up to 212 user I/Os. The AGLP030 devices have no PLL or RAM support.

### Features and Benefits

#### LOW POWER

- 1.2V to 1.5V Core Voltage Support for Low Power
- Supports Single-Voltage System Operation
- 5 µW Power Consumption in Flash*Freeze Mode
- Low Power Active FPGA Operation
- Flash*Freeze Technology Enables Ultra-Low Power Consumption while Maintaining FPGA Content
- Configurable Hold Previous State, Tristate, HIGH, or LOW State per I/O in Flash*Freeze Mode
- Easy Entry To/Exit From Ultra-Low Power Flash*Freeze Mode

#### FEATURE RICH

- 30k to 125k System Gates
- Up to 36 kbits of True Dual-Port SRAM
- Up to 212 User I/Os

#### REPROGRAMMABLE FLASH TECHNOLOGY

- 130 nm, 7-Layer Metal, Flash-Based CMOS Process
- Instant On Level 0 Support
- Single-Chip Solution
- Retains Programmed Design When Powered Off
- 250 MHz (1.5V systems) and 160 MHz (1.2V systems) System Performance

#### IN-SYSTEM PROGRAMMING (ISP) AND SECURITY

- ISP Using On-Chip 128-bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE® 1532–compliant)†
- FlashLock® Designed to Secure FPGA Contents

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## HIGH-PERFORMANCE ROUTING HIERARCHY

- Segmented, Hierarchical Routing and Clock Structure

## ADVANCED I/O

- 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—4 Banks per Chip on All IGLOO PLUS Devices
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3V/2.5V/1.8V/1.5V/1.2V
- Selectable Schmitt Trigger Inputs
- Wide Range Power Supply Voltage Support per JESD8-B, Allowing I/Os to Operate from 2.7V to 3.6V
- Wide Range Power Supply Voltage Support per JESD8-12, Allowing I/Os to Operate from 1.14V to 1.575V
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold-Sparing I/Os
- Programmable Output Slew Rate and Drive Strength
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Small-Footprint Packages across the IGLOO PLUS Family

## CLOCK CONDITIONING CIRCUIT (CCC) AND PLL†

- Six CCC Blocks, One with an Integrated PLL
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range (1.5 MHz up to 250 MHz)

## EMBEDDED MEMORY

- 1 kbit of FlashROM User Nonvolatile Memory
- SRAMs and FIFOs with Variable-Aspect-Ratio 4,608-bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations)†
- True Dual-Port SRAM (except ×18)†

**TABLE 1: IGLOO® PLUS PRODUCT FAMILY**

| IGLOO PLUS Devices | AGLP030 | AGLP060 | AGLP125 |
|---|---|---|---|
| System Gates | 30,000 | 60,000 | 125,000 |
| Typical Equivalent Macrocells | 256 | 512 | 1,024 |
| VersaTiles (D-flip-flops) | 792 | 1,584 | 3,120 |
| Flash*Freeze Mode (typical, µW) | 5 | 10 | 16 |
| RAM Kbits (1,024 bits) | — | 18 | 36 |
| 4,608-bit Blocks | — | 4 | 8 |
| Secure (AES) ISP | — | Yes | Yes |
| FlashROM Kbits | 1 | 1 | 1 |
| Integrated PLL in CCCs [1] | — | 1 | 1 |
| VersaNet Globals [2] | 6 | 18 | 18 |
| I/O Banks | 4 | 4 | 4 |
| Maximum User I/Os | 120 | 157 | 212 |
| Package Pins<br>CS<br>VQ | CS201[3], CS289[3]<br>VQ128 | CS201[3], CS289[3]<br>VQ176[3] | CS281[3], CS289[3] |

**Note 1:** AGLP060 in CS201 does not support the PLL.

**2:** Six chip (main) and twelve quadrant global networks are available for AGLP060 and AGLP125.

**3:** The package is discontinued.

*†. The AGLP030 device does not support this feature.*


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## I/Os Per Package

**TABLE 2: I/OS PER PACKAGE**

| IGLOO® PLUS Devices | AGLP030 | AGLP060 | AGLP125 |
|---|---|---|---|
| Package | Single-Ended I/Os | | |
| CS201 | 120[1] | 157[1] | — |
| CS281 | — | — | 212[1] |
| CS289 | 120[1] | 157[1] | 212[1] |
| VQ128 | 101 | — | — |
| VQ176 | — | 137[1] | — |

**Note 1:** The package is discontinued.

**2:** When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.

**TABLE 3: IGLOO® PLUS FPGAS PACKAGE SIZE DIMENSIONS**

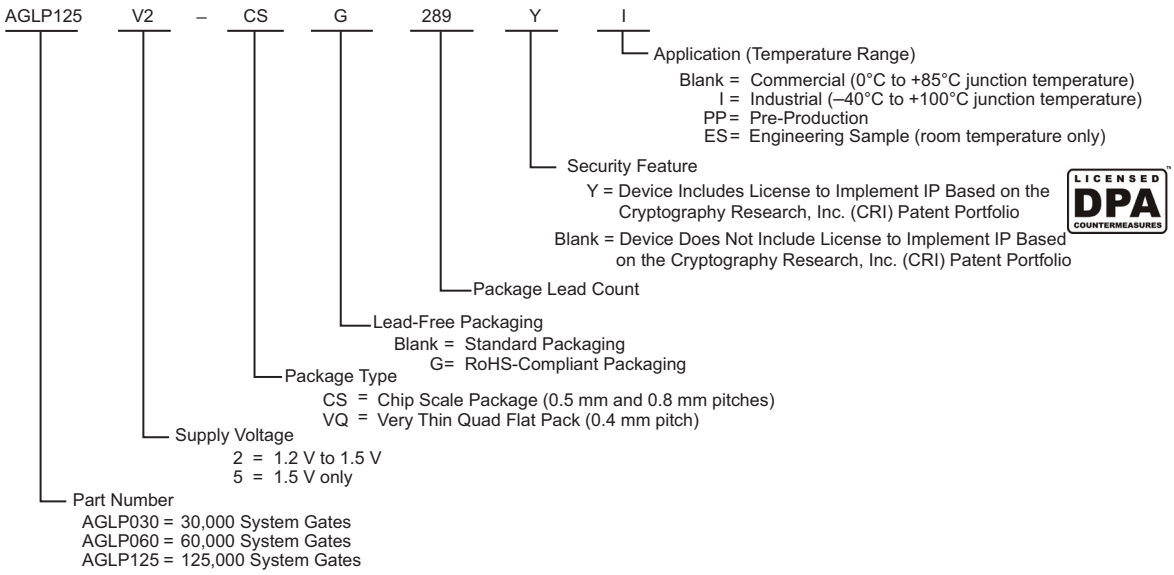
| Package | CS201 | CS281 | CS289 | VQ128 | VQ176 |
|---|---|---|---|---|---|
| Length × Width (mm/mm) | 8 × 8 | 10 × 10 | 14 × 14 | 14 × 14 | 20 × 20 |
| Nominal Area (mm2) | 64 | 100 | 196 | 196 | 400 |
| Pitch (mm) | 0.5 | 0.5 | 0.8 | 0.4 | 0.4 |
| Height (mm) | 0.89 | 1.05 | 1.20 | 1.0 | 1.0 |

## IGLOO PLUS Device Status

**TABLE 4: IGLOO® PLUS DEVICE STATUS**

| IGLOO PLUS Device | Status |
|---|---|
| AGLP030 | Production |
| AGLP060 | Discontinued |
| AGLP125 | Discontinued |

## IGLOO PLUS Ordering Information




**Note 1:** Marking information: IGLOO PLUS V2 devices do not have a V2 marking, but IGLOO PLUS V5 devices are marked accordingly.

**2:** "G" indicates RoHS-compliant packages.

## Temperature Grade Offerings

**TABLE 5: TEMPERATURE GRADE OFFERINGS**

| Package | AGLP030 | AGLP060 | AGLP125 |
|---|---|---|---|
| CS201 | C[3], I[3] | C[3], I[3] | – |
| CS281 | — | — | C[3], I[3] |
| CS289 | C[3], I[3] | C[3], I[3] | C[3], I[3] |
| VQ128 | C, I | – | — |
| VQ176 | — | C[3], I[3] | — |

**Note 1:** C = Commercial temperature range: 0 °C to 85 °C junction temperature.

**2:** I = Industrial temperature range: –40 °C to 100 °C junction temperature.

**3:** The package is discontinued.


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# 1.0 IGLOO PLUS DEVICE FAMILY OVERVIEW

## 1.1 Flash*Freeze Technology

The IGLOO PLUS device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low power Flash*Freeze mode. IGLOO PLUS devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, registers, and I/O states. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOO PLUS V2 devices to support a wide range of core and I/O voltages (1.2V to 1.5V) allows further reduction in power consumption, thus achieving the lowest total system power.

During Flash*Freeze mode, each I/O can be set to the following configurations: hold previous state, tristate, or set as HIGH or LOW.

The availability of low power modes, combined with reprogrammability, a single-chip and single-voltage solution, and availability of small-footprint, high-pin-count packages, make IGLOO PLUS devices the best fit for portable electronics.

## 1.2 Flash Advantages

### 1.2.1 LOW POWER

IGLOO PLUS devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO PLUS devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO PLUS devices also have low dynamic power consumption to further maximize power savings; power is even further reduced by the use of a 1.2V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOO PLUS device the lowest total system power offered by any FPGA.

### 1.2.2 SECURITY

Nonvolatile, flash-based IGLOO PLUS devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO PLUS devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO PLUS devices (except AGLP030) utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of security in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOO PLUS devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO PLUS devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO PLUS devices with AES-based security provide a high level of protection for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of the IGLOO PLUS family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The IGLOO PLUS family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An IGLOO PLUS device provides the best available security for programmable logic designs.

### 1.2.3 SINGLE CHIP

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO PLUS FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

The IGLOO PLUS devices can be operated with a 1.2V or 1.5V single-voltage supply for core and I/Os, eliminating the need for additional supplies while minimizing total power consumption.

### 1.2.4 INSTANT ON

Flash-based IGLOO PLUS devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based IGLOO PLUS devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO PLUS device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO PLUS devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO PLUS flash FPGAs allow the user to quickly enter and exit Flash*Freeze mode. This is done almost instantly (within 1 µs), and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs, the device does not need to reload configuration and design state from external memory components; instead, it retains all necessary information to resume operation immediately.

### 1.2.5 REDUCED COST OF OWNERSHIP

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based IGLOO PLUS devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm.

The IGLOO PLUS family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOO PLUS family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

### 1.2.6 FIRM-ERROR IMMUNITY

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO PLUS flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO PLUS FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

## 1.3 Advanced Flash Technology

The IGLOO PLUS family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130 nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO PLUS family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

## 1.4 Advanced Architecture

The proprietary IGLOO PLUS architecture provides granularity comparable to standard-cell ASICs. The IGLOO PLUS device consists of five distinct and programmable architectural features (see the following figure):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory†
- Extensive CCCs and PLLs†

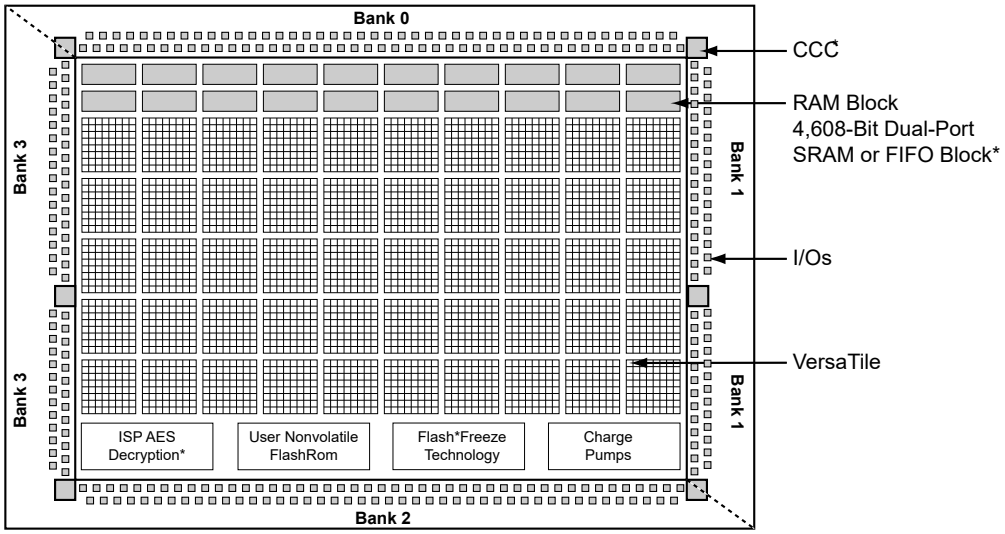
*†. The AGLP030 device does not support PLL or SRAM.*


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- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO PLUS core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC® family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

**FIGURE 1-1: IGLOO® PLUS DEVICE ARCHITECTURE OVERVIEW WITH FOUR I/O BANKS (AGLP030, AGLP060, AND AGLP125)**




**Note:** *Not supported by AGLP030 devices

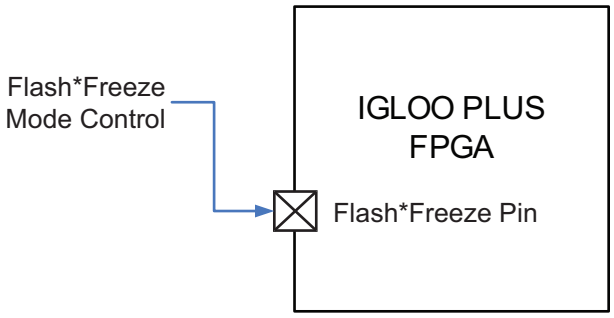
### 1.4.1 FLASH*FREEZE TECHNOLOGY

The IGLOO PLUS device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or be tristated during Flash*Freeze mode. Alternatively, they can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 5 µW in this mode.

Flash*Freeze technology allows the user to switch to Active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. See the following figure for an illustration of entering/exiting Flash*Freeze mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned.

**FIGURE 1-2: IGLOO® PLUS FLASH*FREEZE MODE**



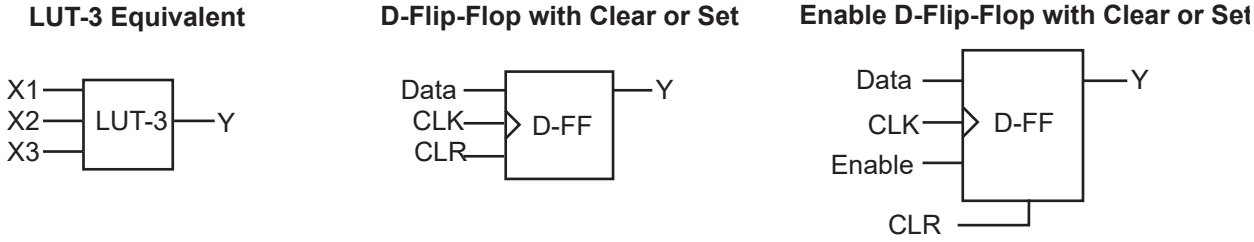

### 1.4.2 VERSATILES

The IGLOO PLUS core consists of VersaTiles, which have been enhanced beyond the ProASIC[PLUS®] core tiles. The IGLOO PLUS VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

See the following figure for the VersaTile configurations.

**FIGURE 1-3: VERSATILE CONFIGURATIONS**




### 1.4.3 USER NONVOLATILE FLASHROM

IGLOO PLUS devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOO PLUS IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in AGLP030 devices), as in security keys stored in the FlashROM for a user design.


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The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The IGLOO PLUS development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

### 1.4.4 SRAM AND FIFO

IGLOO PLUS devices (except AGLP030 devices) have embedded SRAM blocks along their north side. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in AGLP030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

### 1.4.5 PLL AND CCC

IGLOO PLUS devices provide designers with very flexible clock conditioning circuit (CCC) capabilities. Each member of the IGLOO PLUS family contains six CCCs. One CCC (center west side) has a PLL. The AGLP030 device does not have a PLL or CCCs; it contains only inputs to six globals.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

The four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range ($f_{IN_CCC}$) = 1.5 MHz up to 250 MHz
- Output frequency range ($f_{OUT_CCC}$) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 µs (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases (for PLL only) is 40 ps × 250 MHz / $f_{OUT_CCC}$

### 1.4.6 GLOBAL CLOCKING

IGLOO PLUS devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

### 1.4.7 I/OS WITH ADVANCED I/O STANDARDS

The IGLOO PLUS family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2V, 1.5V, 1.8V, 2.5V, 3.0V wide range, and 3.3V). IGLOO PLUS FPGAs support many different I/O standards.

The I/Os are organized into four banks. All devices in IGLOO PLUS have four banks. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and output enable registers.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

## 1.5 Wide Range I/O Support

IGLOO PLUS devices support JEDEC-defined wide range I/O operation. IGLOO PLUS devices support both the JESD8-B specification, covering 3V and 3.3V supplies, for an effective operating range of 2.7V to 3.6V, and JESD8-12 with its 1.2V nominal, supporting an effective operating range of 1.14V to 1.575V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

## 1.6 Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

**Note:** PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify.
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

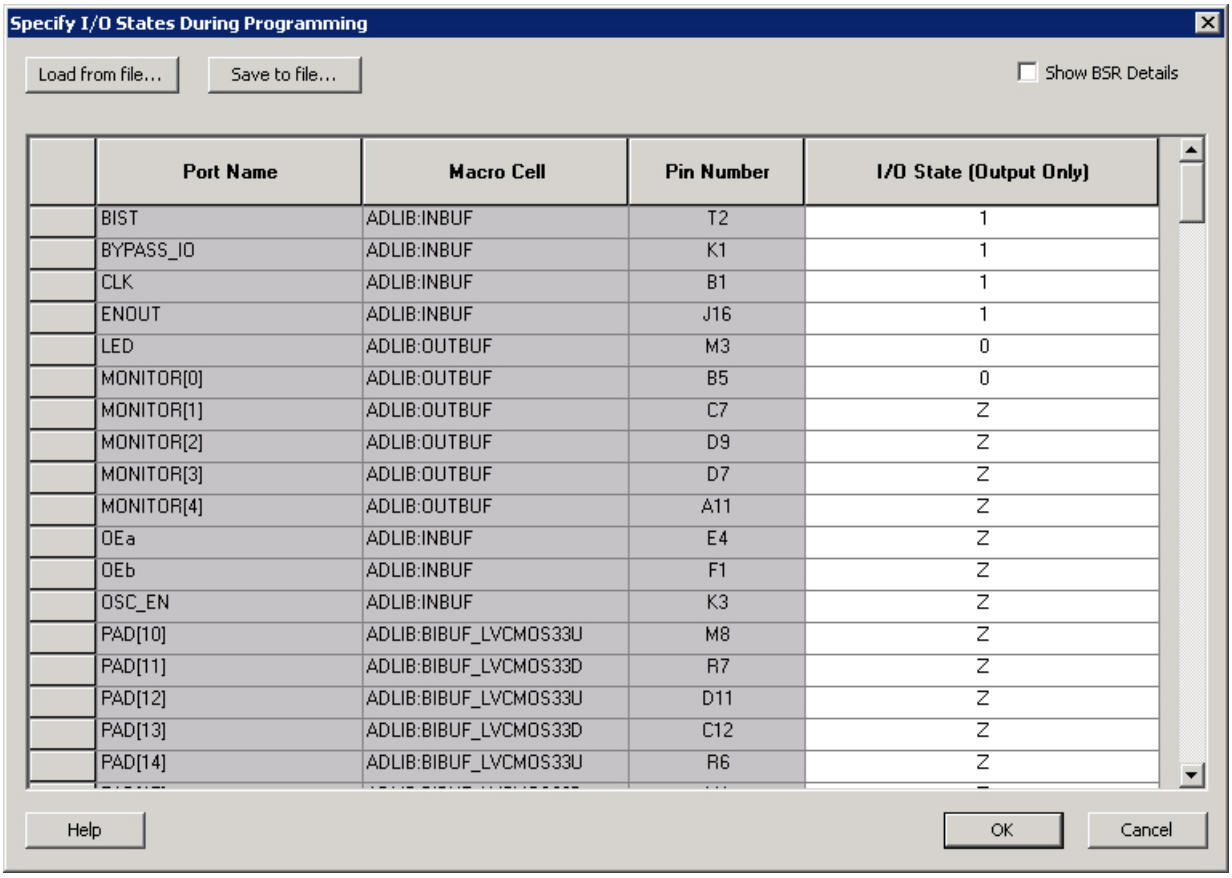
   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming Z -Tri-State: I/O is tristated


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**FIGURE 1-4: I/O STATES DURING PROGRAMMING WINDOW**




6. Click OK to return to the FlashPoint – Programming File Generator window.

**Note:** I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

# 2.0 IGLOO PLUS DC AND SWITCHING CHARACTERISTICS

## 2.1 Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 is not implied.

**TABLE 2-1: ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| VCC | DC core supply voltage | –0.3 to 1.65 | V |
| VJTAG | JTAG DC voltage | –0.3 to 3.75 | V |
| VPUMP | Programming voltage | –0.3 to 3.75 | V |
| VCCPLL | Analog power supply (PLL) | –0.3 to 1.65 | V |
| VCCI | DC I/O buffer supply voltage | –0.3 to 3.75 | V |
| $V_I$[1] | I/O input voltage | –0.3 V to 3.6 V | V |
| $T_{STG}$[2] | Storage temperature | –65 to +150 | °C |
| $T_J$[2] | Junction temperature | +125 | °C |

**Note 1:** The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4.

**2:** For flash programming and retention maximum limits, refer to Table 2-3, and for recommended operating limits, refer to Table 2-2.

**TABLE 2-2: RECOMMENDED OPERATING CONDITIONS[1,2]**

| Symbol | Parameter | | Commercial | Industrial | Units |
|---|---|---|---|---|---|
| $T_J$ | Junction temperature[2] | | 0 to + 85 | –40 to +100 | °C |
| VCC[3] | 1.5V DC core supply voltage[4] | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | 1.2V–1.5V wide range core voltage[5,6] | | 1.14 to 1.575 | 1.14 to 1.575 | V |
| VJTAG | JTAG DC voltage | | 1.4 to 3.6 | 1.4 to 3.6 | V |
| VPUMP[7] | Programming voltage | Programming mode | 3.15 to 3.45 | 3.15 to 3.45 | V |
| | | Operation | 0 to 3.6 | 0 to 3.6 | V |
| VCCPLL[8] | Analog power supply (PLL) | 1.5V DC core supply voltage[4] | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | | 1.2V–1.5V wide range core voltage[5] | 1.14 to 1.575 | 1.14 to 1.575 | V |
| VCCI | 1.2V DC supply voltage[5] | | 1.14 to 1.26 | 1.14 to 1.26 | V |
| | 1.2V DC wide range supply voltage[5] | | 1.14 to 1.575 | 1.14 to 1.575 | V |
| | 1.5V DC supply voltage | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | 1.8V DC supply voltage | | 1.7 to 1.9 | 1.7 to 1.9 | V |
| | 2.5V DC supply voltage | | 2.3 to 2.7 | 2.3 to 2.7 | V |
| | 3.3V wide range DC supply voltage[9] | | 2.7 to 3.6 | 2.7 to 3.6 | V |
| | 3.3V DC supply voltage | | 3.0 to 3.6 | 3.0 to 3.6 | V |


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**TABLE 2-2: RECOMMENDED OPERATING CONDITIONS[1,2]**

| Symbol | Parameter | Commercial | Industrial | Units |
|---|---|---|---|---|

**Note 1:** All parameters representing voltages are measured with respect to GND unless otherwise specified.

**2:** To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microchip recommends that the user follow best design practices using Microchip's timing and power simulation tools.

**3:** The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-21. VCCI should be at the same voltage within a given I/O bank.

**4:** For IGLOO PLUS V5 devices

**5:** For IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.

**6:** All IGLOO PLUS devices (V5 and V2) must be programmed with the VCC core voltage at 1.5 V. Applications using V2 devices powered by a 1.2 V supply must switch the core supply to 1.5 V for in-system programming.

**7:** VPUMP can be left floating during operation (not programming mode).

**8:** VCCPLL pins should be tied to VCC pins. See the Pin Descriptions chapter of the *IGLOO PLUS FPGA Fabric User's Guide* for further information.

**9:** 3.3 V wide range is compliant to the JDEC8b specification and supports 3.0V VCCI operation.

**10:** VMV pins must be connected to the corresponding VCCI pins. See the "Pin Descriptions" chapter of the *IGLOO FPGA Fabric User's Guide* for further information.

**11:** Software Default Junction Temperature Range in the Libero SoC software is set to 0 °C to +70 °C for commercial, and -40 °C to +85 °C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microchip recommends using custom settings for temperature range before running timing and power analysis tools. For more information, refer to https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/core-docs/Libero/libero_g3g4_ccf.zip.

**TABLE 2-3: FLASH PROGRAMMING LIMITS – RETENTION, STORAGE, AND OPERATING TEMPERATURE [1]**

| Product Grade | Programming Cycles | Program Retention (biased/unbiased) | Maximum Storage Temperature $T_{STG}$ (°C) [2] | Maximum Operating Junction Temperature $T_J$ (°C) [2] |
|---|---|---|---|---|
| Commercial | 500 | 20 years | 110 | 100 |
| Industrial | 500 | 20 years | 110 | 100 |

**Note 1:** This is a stress rating only; functional operation at any condition other than those indicated is not implied.

**2:** These limits apply for program/data retention only. Refer to Table 2-1 and Table 2-2 for device operating conditions and absolute limits.

**TABLE 2-4: OVERSHOOT AND UNDERSHOOT LIMITS [1]**

| VCCI | Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2] | Maximum Overshoot/ Undershoot[2] |
|---|---|---|
| 2.7 V or less | 10% | 1.4V |
| | 5% | 1.49V |
| 3 V | 10% | 1.1V |
| | 5% | 1.19V |
| 3.3V | 10% | 0.79V |
| | 5% | 0.88V |
| 3.6 V | 10% | 0.45V |
| | 5% | 0.54V |

**TABLE 2-4: OVERSHOOT AND UNDERSHOOT LIMITS [1]**

| VCCI | Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2] | Maximum Overshoot/ Undershoot[2] |
|---|---|---|

**Note 1:** Based on reliability requirements at 85 °C.

**2:** The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15V.

## 2.2 I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOO PLUS device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1.

There are five regions to consider during power-up.

IGLOO PLUS I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 and Figure 2-2).
2. VCCI > VCC – 0.75V (typical)
3. Chip is in the operating mode.

**VCCI Trip Point**:

- Ramping up (V5 devices): 0.6V < trip_point_up < 1.2V
- Ramping down (V5 devices): 0.5V < trip_point_down < 1.1V
- Ramping up (V2 devices): 0.75V < trip_point_up < 1.05V
- Ramping down (V2 devices): 0.65V < trip_point_down < 0.95V

**VCCI Trip Point**:

- Ramping up (V5 devices): 0.6V < trip_point_up < 1.1V
- Ramping down (V5 devices): 0.5V < trip_point_down < 1.0V
- Ramping up (V2 devices): 0.65V < trip_point_up < 1.05V
- Ramping down (V2 devices): 0.55V < trip_point_down < 0.95V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

### 2.2.1 PLL BEHAVIOR AT BROWNOUT CONDITION

Microchip recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1 and Figure 2-2 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V for V5 devices, and 0.75 V ± 0.2 V for V2 devices), the PLL output lock signal goes Low and/or the output clock is lost. Refer to the "Brownout Voltage" section in the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *IGLOO PLUS Device Family User's Guide* for information on clock and lock recovery.

### 2.2.2 INTERNAL POWER-UP ACTIVATION SEQUENCE

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.


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**FIGURE 2-1: V5 DEVICES – I/O STATE AS A FUNCTION OF VCCI AND VCC VOLTAGE LEVELS**

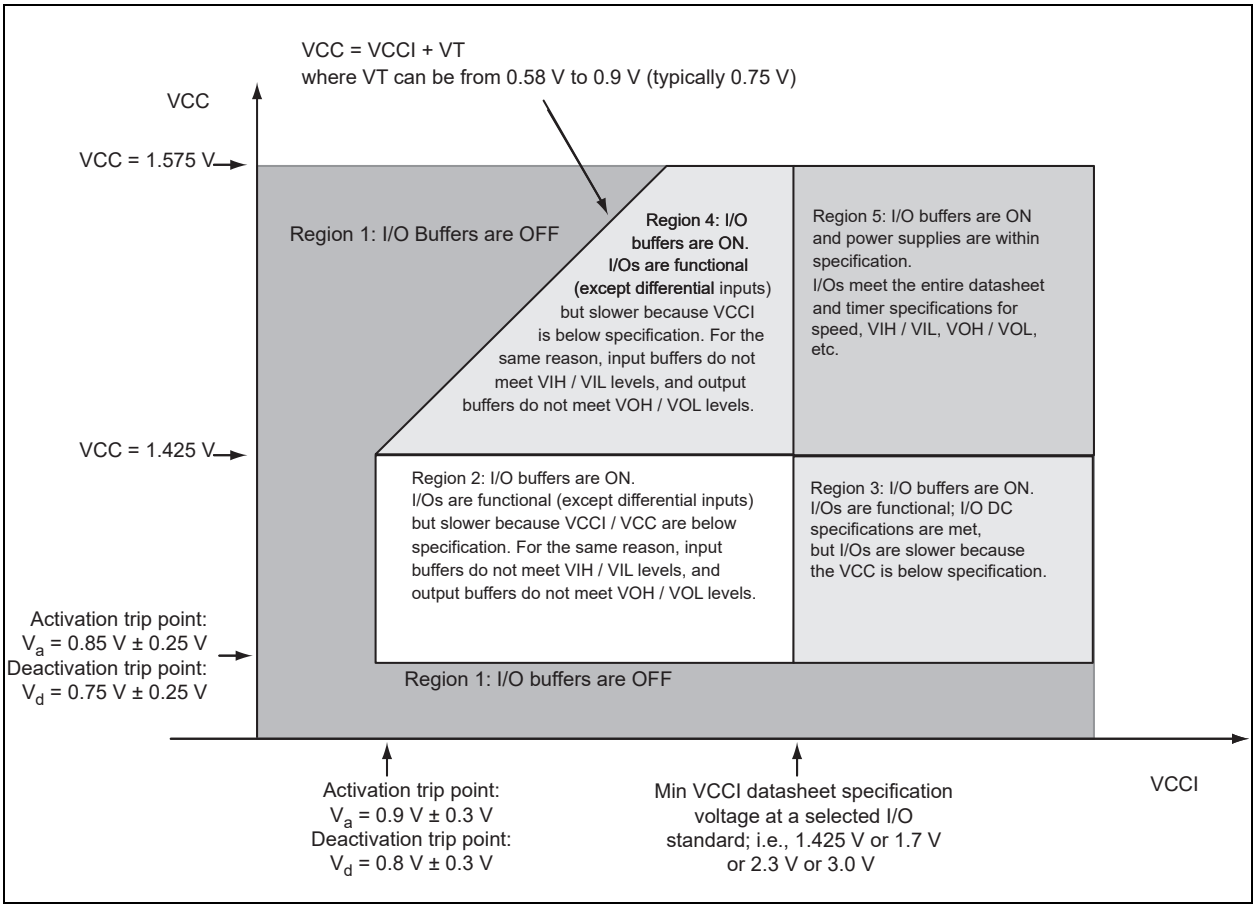
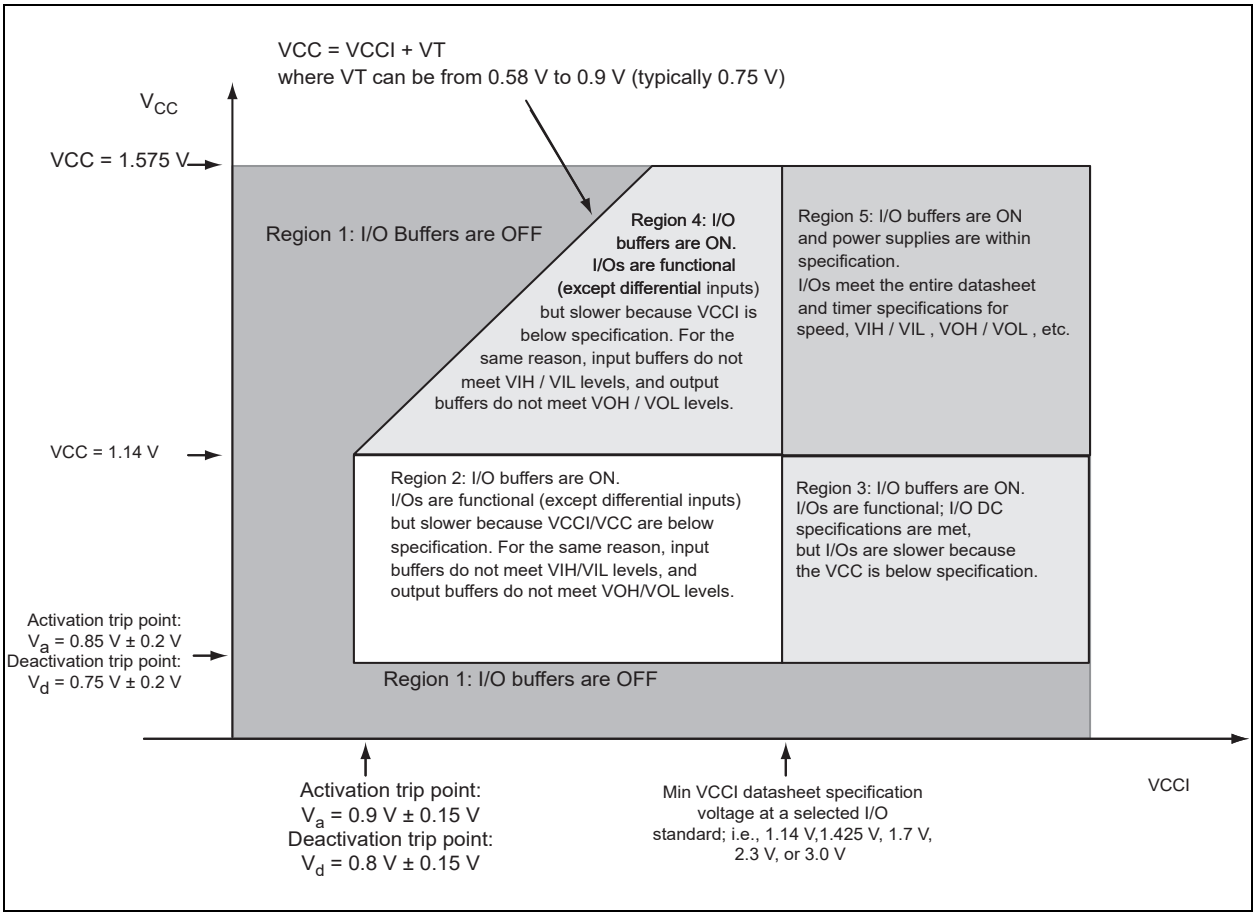


**FIGURE 2-2: V2 DEVICES – I/O STATE AS A FUNCTION OF VCCI AND VCC VOLTAGE LEVELS**




## 2.3 Thermal Characteristics

### 2.3.1 INTRODUCTION

The temperature variable in the Microchip Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature.

The following equation can be used to calculate junction temperature.

**Equation 1**

$T_J$ = Junction Temperature = $\Delta T + T_A$

where:

$T_A$ = Ambient temperature

$\Delta T$ = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

$\theta_{ja}$ = Junction-to-ambient of the package. $\theta_{ja}$ numbers are located in Figure 2-5.

P = Power dissipation


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### 2.3.2 PACKAGE THERMAL CHARACTERISTICS

The device junction-to-case thermal resistivity is $\theta_{jc}$ and the junction-to-ambient air thermal resistivity is $\theta_{ja}$. The thermal characteristics for $\theta_{ja}$ are shown for two air flow rates. The maximum operating junction temperature is 100 °C. The following equation shows a sample calculation of the maximum operating power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

**Equation 2**:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{100\text{°C} - 70\text{°C}}{20.5\text{°C/W}} = 1.46\ \text{W}$$

**TABLE 2-5: PACKAGE THERMAL RESISTIVITIES**

| Package Type | Device | Pin Count | $\theta_{jc}$ | $\theta_{jb}$ | $\theta_{ja}$ | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Still Air | 1 m/s | 2.5 m/s | |
| Chip Scale Package (CSP) | AGLP030 | CS201 | - | - | 46.3 | - | - | C/W |
| | AGLP060 | CS201 | 7.1 | 19.7 | 40.5 | 35.1 | 32.9 | C/W |
| | AGLP060 | CS289 | 13.9 | 34.1 | 48.7 | 43.5 | 41.9 | C/W |
| | AGLP125 | CS289 | 10.8 | 27.9 | 42.2 | 37.1 | 35.5 | C/W |
| | AGLP125 | CS281 | 11.3 | 17.6 | - | - | - | C/W |
| Thin Quad Flat Package (VQ) | AGLP030 | VQ128 | 18.0 | 50.0 | 56.0 | 49.0 | 47.0 | C/W |
| | AGLP060 | VQ176 | 21.0 | 55.0 | 58.0 | 52.0 | 50.0 | C/W |

### 2.3.3 TEMPERATURE AND VOLTAGE DERATING FACTORS

**TABLE 2-6: TEMPERATURE AND VOLTAGE DERATING FACTORS FOR TIMING DELAYS (NORMALIZED TO $T_J$ = 70 °C, VCC = 1.425V)—FOR IGLOO® PLUS V2 OR V5 DEVICES, 1.5V DC CORE SUPPLY VOLTAGE**

| Array Voltage VCC (V) | Junction Temperature (°C) | | | | | |
|---|---|---|---|---|---|---|
| | –40 °C | 0 °C | 25 °C | 70 °C | 85 °C | 100 °C |
| 1.425 | 0.934 | 0.953 | 0.971 | 1.000 | 1.007 | 1.013 |
| 1.5 | 0.855 | 0.874 | 0.891 | 0.917 | 0.924 | 0.929 |
| 1.575 | 0.799 | 0.816 | 0.832 | 0.857 | 0.864 | 0.868 |

**TABLE 2-7: TEMPERATURE AND VOLTAGE DERATING FACTORS FOR TIMING DELAYS (NORMALIZED TO $T_J$ = 70 °C, VCC = 1.14V)—FOR IGLOO® PLUS V2, 1.2V DC CORE SUPPLY VOLTAGE**

| Array Voltage VCC (V) | Junction Temperature (°C) | | | | | |
|---|---|---|---|---|---|---|
| | –40 °C | 0 °C | 25 °C | 70 °C | 85 °C | 100 °C |
| 1.14 | 0.963 | 0.975 | 0.989 | 1.000 | 1.007 | 1.011 |
| 1.2 | 0.853 | 0.865 | .0877 | 0.893 | 0.893 | 0.897 |
| 1.26 | 0.781 | 0.792 | 0.803 | 0.813 | 0.819 | 0.822 |

## 2.4 Calculating Power Dissipation

### 2.4.1 QUIESCENT SUPPLY CURRENT

Quiescent supply current ($I_{DD}$) calculation depends on multiple factors, including operating voltages (VCC, VCCI, and VJTAG), operating temperature, system clock frequency, and power mode usage. Microchip recommends using the Power Calculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

**TABLE 2-8: POWER SUPPLY STATE PER MODE**

| Modes/Power Supplies | Power Supply Configurations | | | | |
|---|---|---|---|---|---|
| | VCC | VCCPLL | VCCI | VJTAG | VPUMP |
| Flash*Freeze | On | On | On | On | On/off/floating |
| Sleep | Off | Off | On | Off | Off |
| Shutdown | Off | Off | Off | Off | Off |
| No Flash*Freeze | On | On | On | On | On/off/floating |

**Note:** Off: Power Supply level = 0 V

**TABLE 2-9: QUIESCENT SUPPLY CURRENT (IDD) CHARACTERISTICS, IGLOO® PLUS FLASH*FREEZE MODE***

| | Core Voltage | AGLP030 | AGLP060 | AGLP125 | Units |
|---|---|---|---|---|---|
| Typical (25 °C) | 1.2V | 4 | 8 | 13 | µA |
| | 1.5V | 6 | 10 | 18 | µA |

**Note:** *IDD includes VCC, VPUMP, VCCI, VJTAG, and VCCPLL currents.

**TABLE 2-10: QUIESCENT SUPPLY CURRENT (IDD) CHARACTERISTICS, IGLOO® PLUS SLEEP MODE***

| ICCI Current | Core Voltage | AGLP030 | AGLP060 | AGLP125 | Units |
|---|---|---|---|---|---|
| VCCI = 1.2V (per bank) Typical (25 °C) | 1.2V | 1.7 | 1.7 | 1.7 | µA |
| VCCI = 1.5V (per bank) Typical (25 °C) | 1.2V / 1.5V | 1.8 | 1.8 | 1.8 | µA |
| VCCI = 1.8V, (per bank) Typical (25 °C) | 1.2V / 1.5V | 1.9 | 1.9 | 1.9 | µA |
| VCCI = 2.5V (per bank) Typical (25 °C) | 1.2V / 1.5V | 2.2 | 2.2 | 2.2 | µA |
| VCCI = 3.3V (per bank) Typical (25 °C) | 1.2V / 1.5V | 2.5 | 2.5 | 2.5 | µA |

**Note:** *IDD = $N_{BANKS}$ * ICCI

**TABLE 2-11: QUIESCENT SUPPLY CURRENT (IDD) CHARACTERISTICS, IGLOO® PLUS SHUTDOWN MODE**

| | Core Voltage | AGLP030 | AGLP060 | AGLP125 | Units |
|---|---|---|---|---|---|
| Typical (25 °C) | 1.2V / 1.5V | 0 | 0 | 0 | µA |

**TABLE 2-12: QUIESCENT SUPPLY CURRENT (IDD), NO IGLOO® PLUS FLASH*FREEZE MODE [1]**

| | Core Voltage | AGLP030 | AGLP060 | AGLP125 | Units |
|---|---|---|---|---|---|
| **ICCA Current [2]** | | | | | |
| Typical (25 °C) | 1.2V | 6 | 10 | 13 | µA |
| | 1.5V | 16 | 20 | 28 | µA |
| **ICCI or IJTAG Current** | | | | | |
| VCCI / VJTAG = 1.2V (per bank) Typical (25 °C) | 1.2V | 1.7 | 1.7 | 1.7 | µA |


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**TABLE 2-12: QUIESCENT SUPPLY CURRENT (IDD), NO IGLOO® PLUS FLASH*FREEZE MODE [1]**

| | Core Voltage | AGLP030 | AGLP060 | AGLP125 | Units |
|---|---|---|---|---|---|
| VCCI / VJTAG = 1.5V (per bank)<br>Typical (25 °C) | 1.2V/1.5V | 1.8 | 1.8 | 1.8 | µA |
| VCCI / VJTAG = 1.8V, (per bank)<br>Typical (25 °C) | 1.2V/1.5V | 1.9 | 1.9 | 1.9 | µA |
| VCCI / VJTAG = 2.5V (per bank)<br>Typical (25 °C) | 1.2V/1.5V | 2.2 | 2.2 | 2.2 | µA |
| VCCI / VJTAG = 3.3V (per bank)<br>Typical (25 °C) | 1.2V/1.5V | 2.5 | 2.5 | 2.5 | µA |

**Note 1:** IDD = $N_{BANKS}$ * ICCI + ICCA. JTAG counts as one bank when powered.

**2:** Includes VCC, VCCPLL, and VPUMP currents.

### 2.4.2 POWER PER I/O PIN

**TABLE 2-13: SUMMARY OF I/O INPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS**

| | VCCI (V) | Dynamic Power PAC9 (µW/MHz) [1] |
|---|---|---|
| **Single-Ended** | | |
| 3.3V LVTTL / 3.3V LVCMOS | 3.3 | 16.26 |
| 3.3V LVTTL / 3.3V LVCMOS – Schmitt Trigger | 3.3 | 18.95 |
| 3.3 V LVCMOS Wide Range[2] | 3.3 | 16.26 |
| 3.3 V LVCMOS Wide Range[2] – Schmitt Trigger | 3.3 | 18.95 |
| 2.5V LVCMOS | 2.5 | 4.59 |
| 2.5V LVCMOS – Schmitt Trigger | 2.5 | 6.01 |
| 1.8V, LVCMOS | 1.8 | 1.61 |
| 1.8V, LVCMOS – Schmitt Trigger | 1.8 | 1.70 |
| 1.5V LVCMOS (JESD8-11) | 1.5 | 0.96 |
| 1.5V LVCMOS (JESD8-11) – Schmitt Trigger | 1.5 | 0.90 |
| 1.2V LVCMOS[3] | 1.2 | 0.55 |
| 1.2V LVCMOS[3] – Schmitt Trigger | 1.2 | 0.47 |
| 1.2 V LVCMOS Wide Range[3] | 1.2 | 0.55 |
| 1.2 V LVCMOS Wide Range[3] – Schmitt Trigger | 1.2 | 0.47 |

**Note 1:** PAC9 is the total dynamic power measured on VCCI.

**2:** All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

**3:** Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.

**TABLE 2-14: SUMMARY OF I/O OUTPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS[1]**

| | $C_{LOAD}$ (pF) | VCCI (V) | Dynamic Power PAC10 (µW/MHz)[2] |
|---|---|---|---|
| **Single-Ended** | | | |
| 3.3V LVTTL / 3.3V LVCMOS | 5 | 3.3 | 127.11 |
| 3.3 V LVCMOS Wide Range[3] | 5 | 3.3 | 127.11 |
| 2.5V LVCMOS | 5 | 2.5 | 70.71 |
| 1.8V, LVCMOS | 5 | 1.8 | 35.57 |
| 1.5V LVCMOS (JESD8-11) | 5 | 1.5 | 24.30 |
| 1.2V LVCMOS[4] | 5 | 1.2 | 15.22 |
| 1.2 V LVCMOS Wide Range[4] | 5 | 1.2 | 15.22 |

**Note 1:** Dynamic power consumption is given for standard load and software default drive strength and output slew.

**2:** PAC10 is the total dynamic power measured on VCCI.

**3:** All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

**4:** Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.


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## 2.5 Power Consumption of Various Internal Resources

**TABLE 2-15: DIFFERENT COMPONENTS CONTRIBUTING TO DYNAMIC POWER CONSUMPTION IN IGLOO® PLUS DEVICES—FOR IGLOO PLUS V2 OR V5 DEVICES, 1.5V CORE SUPPLY VOLTAGE**

| Parameter | Definition | Device Specific Dynamic Power (µW/MHz) | | |
|---|---|---|---|---|
| | | AGLP125 | AGLP060 | AGLP030 |
| PAC1 | Clock contribution of a Global Rib | 4.489 | 2.696 | 0.000[1] |
| PAC2 | Clock contribution of a Global Spine | 1.991 | 1.962 | 3.499 |
| PAC3 | Clock contribution of a VersaTile row | 1.510 | 1.523 | 1.537 |
| PAC4 | Clock contribution of a VersaTile used as a sequential module | 0.153 | 0.151 | 0.151 |
| PAC5 | First contribution of a VersaTile used as a sequential module | 0.029 | 0.029 | 0.029 |
| PAC6 | Second contribution of a VersaTile used as a sequential module | 0.323 | 0.323 | 0.323 |
| PAC7 | Contribution of a VersaTile used as a combinatorial module | 0.280 | 0.300 | 0.278 |
| PAC8 | Average contribution of a routing net | 1.097 | 1.081 | 1.130 |
| PAC9 | Contribution of an I/O input pin (standard-dependent) | See Table 2-13. | | |
| PAC10 | Contribution of an I/O output pin (standard-dependent) | See Table 2-14. | | |
| PAC11 | Average contribution of a RAM block during a read operation | 25.00 | | |
| PAC12 | Average contribution of a RAM block during a write operation | 30.00 | | |
| PAC13 | Dynamic contribution for PLL | 2.70 | | |

**Note:** 1. There is no Center Global Rib present in AGLP030, and thus it starts directly at the spine resulting in 0µW/MHz.

**TABLE 2-16: DIFFERENT COMPONENTS CONTRIBUTING TO THE STATIC POWER CONSUMPTION IN IGLOO® PLUS DEVICES—FOR IGLOO PLUS V2 OR V5 DEVICES, 1.5V CORE SUPPLY VOLTAGE**

| Parameter | Definition | Device-Specific Static Power (mW) | | |
|---|---|---|---|---|
| | | AGLP125 | AGLP060 | AGLP030 |
| PDC1 | Array static power in Active mode | See Table 2-12 | | |
| PDC2 | Array static power in Static (Idle) mode | See Table 2-11 | | |
| PDC3 | Array static power in Flash*Freeze mode | See Table 2-9 | | |
| PDC4 | Static PLL contribution | 1.84[1] | | |
| PDC5 | Bank quiescent power (VCCI-dependent) | See Table 2-12 | | |

**Note 1:** This is the minimum contribution of the PLL when operating at lowest frequency.

**2:** For a different output load, drive strength, or slew rate, Microchip recommends using the Microchip power spreadsheet calculator or the SmartPower tool in Libero SoC software.

**TABLE 2-17: DIFFERENT COMPONENTS CONTRIBUTING TO DYNAMIC POWER CONSUMPTION IN IGLOO® PLUS DEVICES—FOR IGLOO PLUS V2 DEVICES, 1.2V CORE SUPPLY VOLTAGE**

| Parameter | Definition | Device-Specific Dynamic Power (µW/MHz) | | |
|---|---|---|---|---|
| | | AGLP125 | AGLP060 | AGLP030 |
| PAC1 | Clock contribution of a Global Rib | 2.874 | 1.727 | 0.000[1] |
| PAC2 | Clock contribution of a Global Spine | 1.264 | 1.244 | 2.241 |

**TABLE 2-17: DIFFERENT COMPONENTS CONTRIBUTING TO DYNAMIC POWER CONSUMPTION IN IGLOO® PLUS DEVICES—FOR IGLOO PLUS V2 DEVICES, 1.2V CORE SUPPLY VOLTAGE**

| Parameter | Definition | Device-Specific Dynamic Power (µW/MHz) | | |
|---|---|---|---|---|
| | | AGLP125 | AGLP060 | AGLP030 |
| PAC3 | Clock contribution of a VersaTile row | 0.963 | 0.975 | 0.981 |
| PAC4 | Clock contribution of a VersaTile used as a sequential module | 0.098 | 0.096 | 0.096 |
| PAC5 | First contribution of a VersaTile used as a sequential module | 0.018 | 0.018 | 0.018 |
| PAC6 | Second contribution of a VersaTile used as a sequential module | 0.203 | 0.203 | 0.203 |
| PAC7 | Contribution of a VersaTile used as a combinatorial module | 0.160 | 0.170 | 0.158 |
| PAC8 | Average contribution of a routing net | 0.679 | 0.686 | 0.748 |
| PAC9 | Contribution of an I/O input pin (standard-dependent) | See Table 2-13 | | |
| PAC10 | Contribution of an I/O output pin (standard-dependent) | See Table 2-14 | | |
| PAC11 | Average contribution of a RAM block during a read operation | 25.00 | | |
| PAC12 | Average contribution of a RAM block during a write operation | 30.00 | | |
| PAC13 | Dynamic contribution for PLL | 2.10 | | |

**Note:** 1. There is no Center Global Rib present in AGLP030, and thus it starts directly at the spine resulting in 0µW/MHz.

**TABLE 2-18: DIFFERENT COMPONENTS CONTRIBUTING TO THE STATIC POWER CONSUMPTION IN IGLOO® PLUS DEVICES—FOR IGLOO PLUS V2 DEVICES, 1.2V CORE SUPPLY VOLTAGE**

| Parameter | Definition | Device-Specific Static Power (mW) | | |
|---|---|---|---|---|
| | | AGLP125 | AGLP060 | AGLP030 |
| PDC1 | Array static power in Active mode | See Table 2-12 | | |
| PDC2 | Array static power in Static (Idle) mode | See Table 2-11 | | |
| PDC3 | Array static power in Flash*Freeze mode | See Table 2-9 | | |
| PDC4 | Static PLL contribution | 0.90[1] | | |
| PDC5 | Bank quiescent power (VCCI-dependent) | See Table 2-12 | | |

**Note 1:** This is the minimum contribution of the PLL when operating at lowest frequency.

**2:** For a different output load, drive strength, or slew rate, Microchip recommends using the Microchip power spreadsheet calculator or the SmartPower tool in Libero SoC software.


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## 2.6 Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-19.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-20.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-20. The calculation should be repeated for each clock domain defined in the design.

### 2.6.1 METHODOLOGY

#### 2.6.1.1 Total Power Consumption—$P_{TOTAL}$

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

$P_{STAT}$ is the total static power consumption.

$P_{DYN}$ is the total dynamic power consumption.

#### 2.6.1.2 Total Static Power Consumption—$P_{STAT}$

$$P_{STAT} = (PDC1 \text{ or } PDC2 \text{ or } PDC3) + N_{BANKS} * PDC5$$

$N_{BANKS}$ is the number of I/O banks powered in the design.

#### 2.6.1.3 Total Dynamic Power Consumption—$P_{DYN}$

$$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

#### 2.6.1.4 Global Clock Contribution—$P_{CLOCK}$

$$P_{CLOCK} = (PAC1 + N_{SPINE}*PAC2 + N_{ROW}*PAC3 + N_{S\text{-}CELL}* PAC4) * F_{CLK}$$

$N_{SPINE}$ is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *IGLOO PLUS FPGA Fabric User's Guide*.

$N_{ROW}$ is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *IGLOO PLUS FPGA Fabric User's Guide*.

$F_{CLK}$ is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

#### 2.6.1.5 Sequential Cells Contribution—$P_{S\text{-}CELL}$

$$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19.

$F_{CLK}$ is the global clock signal frequency.

#### 2.6.1.6 Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$$P_{C\text{-}CELL} = N_{C\text{-}CELL}* \alpha_1 / 2 * PAC7 * F_{CLK}$$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19.

$F_{CLK}$ is the global clock signal frequency.

#### 2.6.1.7 Routing Net Contribution—$P_{NET}$

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19.

$F_{CLK}$ is the global clock signal frequency.

#### 2.6.1.8 I/O Input Buffer Contribution—$P_{INPUTS}$

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$\alpha_2$ is the I/O buffer toggle rate—guidelines are provided in Table 2-19.

$F_{CLK}$ is the global clock signal frequency.

#### 2.6.1.9 I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

$\alpha_2$ is the I/O buffer toggle rate—guidelines are provided in Table 2-19.

$\beta_1$ is the I/O buffer enable rate—guidelines are provided in Table 2-20.

$F_{CLK}$ is the global clock signal frequency.

#### 2.6.1.10 RAM Contribution—$P_{MEMORY}$

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

$N_{BLOCKS}$ is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

$\beta_2$ is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

$\beta_3$ is the RAM enable rate for write operations—guidelines are provided in Table 2-20.

#### 2.6.1.11 PLL Contribution—$P_{PLL}$

$P_{PLL} = PDC4 + PAC1_3 * F_{CLKOUT}$

$F_{CLKOUT}$ is the output clock frequency.[1]

### 2.6.2 GUIDELINES

#### 2.6.2.1 Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
- Bit 0 (LSB) = 100%
- Bit 1 = 50%
- Bit 2 = 25%
- …
- Bit 7 (MSB) = 0.78125%
- Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

1. *If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.*


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#### 2.6.2.2 Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

**TABLE 2-19: TOGGLE RATE GUIDELINES RECOMMENDED FOR POWER CALCULATION**

| Component | Definition | Guideline |
|---|---|---|
| $\alpha_1$ | Toggle rate of VersaTile outputs | 10% |
| $\alpha_2$ | I/O buffer toggle rate | 10% |

**TABLE 2-20: ENABLE RATE GUIDELINES RECOMMENDED FOR POWER CALCULATION**

| Component | Definition | Guideline |
|---|---|---|
| $\beta_1$ | I/O output buffer enable rate | 100% |
| $\beta_2$ | RAM enable rate for read operations | 12.5% |
| $\beta_3$ | RAM enable rate for write operations | 12.5% |

## 2.7 User I/O Characteristics

### 2.7.1 TIMING MODEL

**FIGURE 2-3: TIMING MODEL— PERATING CONDITIONS: STD SPEED, COMMERCIAL TEMPERATURE RANGE ($T_J$ = 70 °C), WORST-CASE VCC = 1.425V, FOR DC 1.5V CORE VOLTAGE, APPLICABLE TO V2 AND V5 DEVICES**

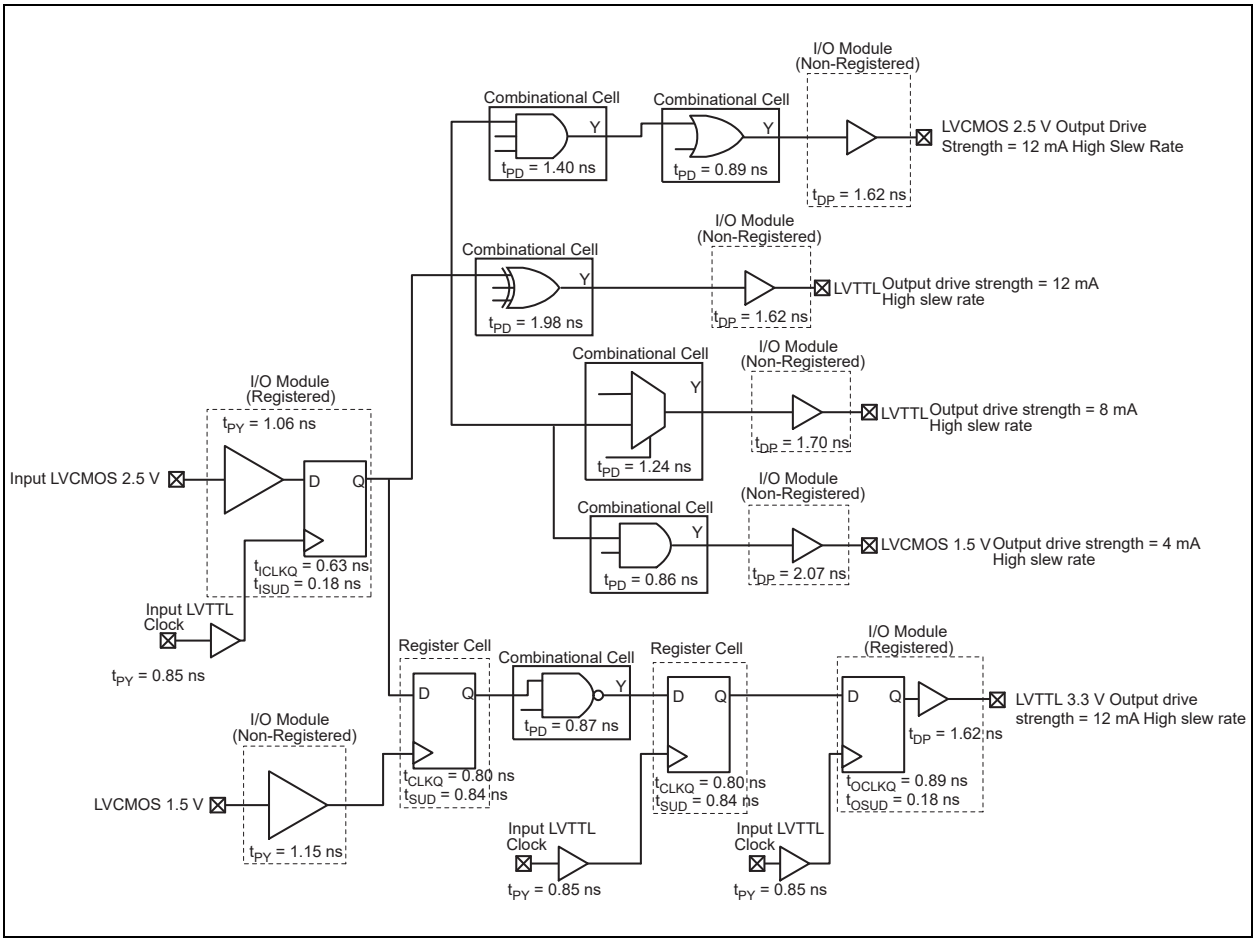
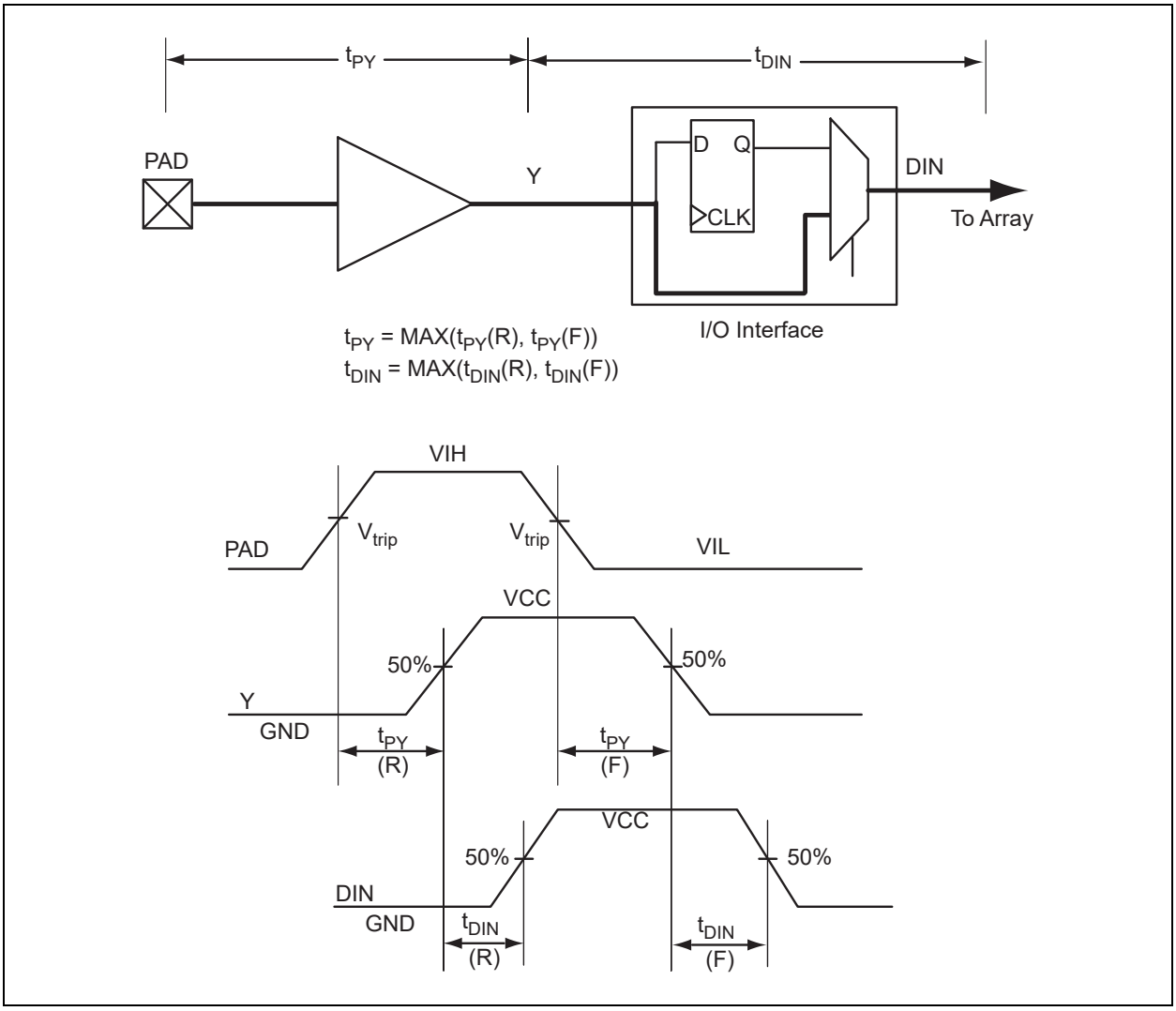


**FIGURE 2-4: INPUT BUFFER TIMING MODEL AND DELAYS (EXAMPLE)**





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**FIGURE 2-5: OUTPUT BUFFER MODEL AND DELAYS (EXAMPLE)**

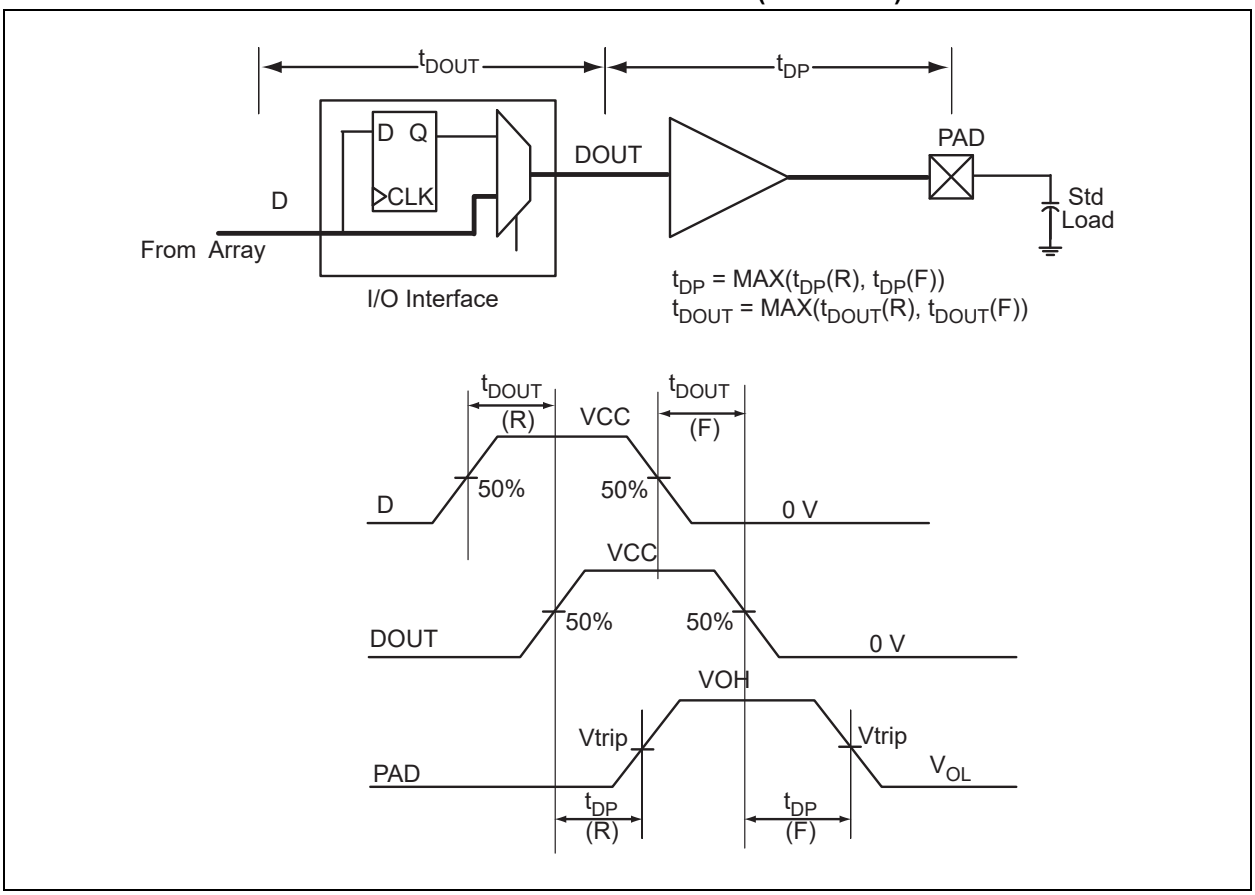
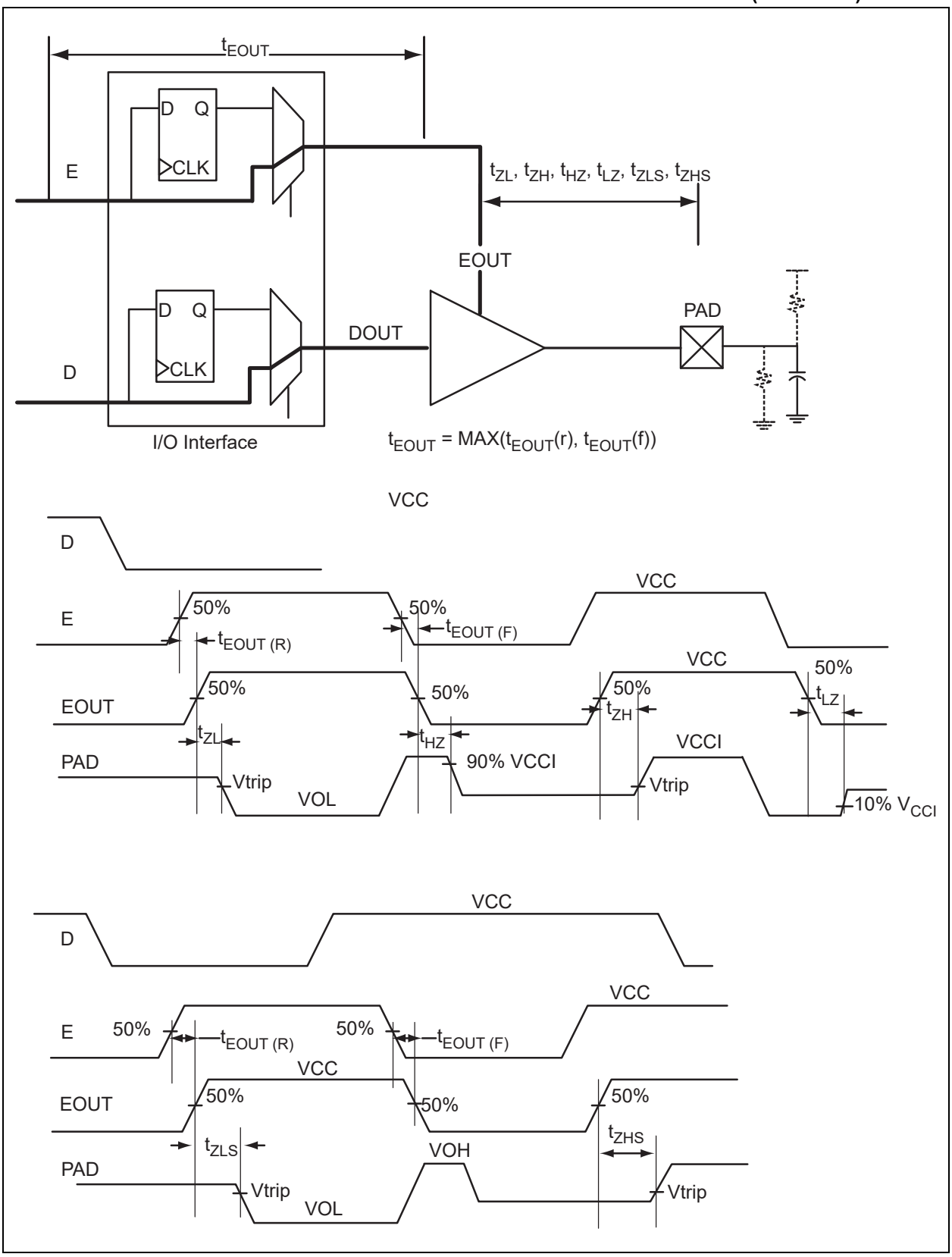


**FIGURE 2-6: TRISTATE OUTPUT BUFFER TIMING MODEL AND DELAYS (EXAMPLE)**





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### 2.7.2 OVERVIEW OF I/O PERFORMANCE

#### 2.7.2.1 Summary of I/O DC Input and Output Levels – Default I/O Software Settings

**TABLE 2-21: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS—SOFTWARE DEFAULT SETTINGS**

| I/O Standard | Drive Strength | Equiv. Software Default Drive Strength Option[2] | Slew Rate | VIL | | VIH | | VOL | VOH | IOL[1] | IOH[1] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA |
| 3.3V LVTTL / 3.3V LVCMOS | 12 mA | 12 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 |
| 3.3V LVCMOS Wide Range[3] | 100 µA | 12 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD 3 0.2 | 0.1 | 0.1 |
| 2.5V LVCMOS | 12 mA | 12 mA | High | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 |
| 1.8V, LVCMOS | 8 mA | 8 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 8 | 8 |
| 1.5V LVCMOS | 4 mA | 4 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 4 | 4 |
| 1.2 V LVCMOS[4] | 2 mA | 2 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 |
| 1.2 V LVCMOS Wide Range[4,5] | 100 µA | 2 mA | High | –0.3 | 0.3 * VCCI | 0.7 * VCCI | 3.6 | 0.1 | VCCI – 0.1 | 0.1 | 0.1 |

**Note 1:** Currents are measured at 85 °C junction temperature.

**2:** Note that 1.2V LVCMOS and 3.3V LVCMOS wide range are applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.

**3:** All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

**4:** Applicable to IGLOO PLUS V2 devices operating at $VCC_I \geq VCC$.

**5:** All LVCMOS 1.2V software macros support LVCMOS 1.2V wide range as specified in the JESD8-12 specification.

**TABLE 2-22: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT LEVELS—APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS**

| DC I/O Standards | Commercial[1] | | Industrial[2] | |
|---|---|---|---|---|
| | IIL[3] | IIH[4] | IIL[3] | IIH[4] |
| | µA | µA | µA | µA |
| 3.3V LVTTL / 3.3V LVCMOS | 10 | 10 | 15 | 15 |
| 3.3 V LVCMOS Wide Range | 10 | 10 | 15 | 15 |
| 2.5V LVCMOS | 10 | 10 | 15 | 15 |
| 1.8V, LVCMOS | 10 | 10 | 15 | 15 |
| 1.5V LVCMOS | 10 | 10 | 15 | 15 |
| 1.2V LVCMOS[5] | 10 | 10 | 15 | 15 |
| 1.2 V LVCMOS Wide Range[5] | 10 | 10 | 15 | 15 |

**Note 1:** Commercial range (0 °C < $T_A$ < 70 °C)

**2:** Industrial range (–40 °C < $T_A$ < 85 °C)

**3:** IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

**4:** IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

**5:** Applicable to IGLOO PLUS V2 devices operating at VCCI ³ VCC.

### 2.7.2.2 Summary of I/O Timing Characteristics – Default I/O Software Settings

**TABLE 2-23: SUMMARY OF AC MEASURING POINTS**

| Standard | Measuring Trip Point (Vtrip) |
|---|---|
| 3.3V LVTTL / 3.3V LVCMOS | 1.4V |
| 3.3 V LVCMOS Wide Range | 1.4 V |
| 2.5V LVCMOS | 1.2V |
| 1.8V, LVCMOS | 0.90 V |
| 1.5V LVCMOS | 0.75 V |
| 1.2V LVCMOS | 0.60 V |
| 1.2V LVCMOS Wide Range | 0.60 V |

**TABLE 2-24: I/O AC PARAMETER DEFINITIONS**

| Parameter | Parameter Definition |
|---|---|
| $t_{DP}$ | Data to Pad delay through the Output Buffer |
| $t_{PY}$ | Pad to Data delay through the Input Buffer |
| $t_{DOUT}$ | Data to Output Buffer delay through the I/O interface |
| $t_{EOUT}$ | Enable to Output Buffer Tristate Control delay through the I/O interface |
| $t_{DIN}$ | Input Buffer to Data delay through the I/O interface |
| $t_{HZ}$ | Enable to Pad delay through the Output Buffer—High to Z |
| $t_{ZH}$ | Enable to Pad delay through the Output Buffer—Z to High |
| $t_{LZ}$ | Enable to Pad delay through the Output Buffer—Low to Z |
| $t_{ZL}$ | Enable to Pad delay through the Output Buffer—Z to Low |
| $t_{ZHS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to High |
| $t_{ZLS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to Low |


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**TABLE 2-25: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS, STD SPEED GRADE, COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 3.0 V**

| I/O Standard | Drive Strength | Equivalent Software Default Drive Strength Option[1] | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3V LVTTL / 3.3V LVCMOS | 12 mA | 12 mA | High | 5 pF | – | 0.97 | 1.76 | 0.18 | 0.85 | 1.15 | 0.66 | 1.80 | 1.39 | 2.20 | 2.64 | ns |
| 3.3 V LVCMOS Wide Range[2] | 100 µA | 12 mA | High | 5 pF | – | 0.97 | 2.47 | 0.18 | 1.18 | 1.64 | 0.66 | 2.48 | 1.91 | 3.16 | 3.76 | ns |
| 2.5V LVCMOS | 12 mA | 12 mA | High | 5 pF | – | 0.97 | 1.77 | 0.18 | 1.06 | 1.22 | 0.66 | 1.81 | 1.51 | 2.22 | 2.56 | ns |
| 1.8V, LVCMOS | 8 mA | 8 mA | High | 5 pF | – | 0.97 | 2.00 | 0.18 | 1.00 | 1.43 | 0.66 | 2.04 | 1.76 | 2.29 | 2.55 | ns |
| 1.5V LVCMOS | 4 mA | 4 mA | High | 5 pF | – | 0.97 | 2.29 | 0.18 | 1.16 | 1.62 | 0.66 | 2.33 | 2.00 | 2.37 | 2.57 | ns |

**Note 1:** Note that 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.

**2:** All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.

**3:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**TABLE 2-26: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS, STD SPEED GRADE COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 3.0 V**

| I/O Standard | Drive Strength | Equivalent Software Default Drive Strength Option[1] | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY})$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3V LVTTL / 3.3V LVCMOS | 12 mA | 12 mA | High | 5 pF | – | 0.98 | 2.31 | 0.19 | 0.99 | 1.37 | 0.67 | 2.34 | 1.86 | 2.65 | 3.38 | ns |
| 3.3 V LVCMOS Wide Range[2] | 100 µA | 12 mA | High | 5 pF | – | 0.98 | 3.21 | 0.19 | 1.32 | 1.92 | 0.67 | 3.21 | 2.52 | 3.73 | 4.73 | ns |
| 2.5V LVCMOS | 12 mA | 12 mA | High | 5 pF | – | 0.98 | 2.29 | 0.19 | 1.19 | 1.40 | 0.67 | 2.32 | 1.94 | 2.65 | 3.27 | ns |

**TABLE 2-26: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS, STD SPEED GRADE COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 3.0 V**

| I/O Standard | Drive Strength | Equivalent Software Default Drive Strength Option[1] | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$) | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1.8V, LVCMOS | 8 mA | 8 mA | High | 5 pF | – | 0.98 | 2.45 | 0.19 | 1.12 | 1.61 | 0.67 | 2.48 | 2.16 | 2.71 | 3.16 | ns |
| 1.5V LVCMOS | 4 mA | 4 mA | High | 5 pF | – | 0.98 | 2.71 | 0.19 | 1.26 | 1.80 | 0.67 | 2.75 | 2.39 | 2.78 | 3.15 | ns |
| 1.2 V LVCMOS | 2 mA | 2 mA | High | 5 pF | – | 0.98 | 3.38 | 0.19 | 1.57 | 2.34 | 0.67 | 3.26 | 2.78 | 2.99 | 3.24 | ns |
| 1.2 V LVCMOS Wide Range[3] | 100 µA | 2 mA | High | 5 pF | – | 0.98 | 3.38 | 0.19 | 1.57 | 2.34 | 0.67 | 3.26 | 2.78 | 2.99 | 3.24 | ns |

**Note 1:** The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

**2:** All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

**3:** All LVCMOS 1.2V software macros support LVCMOS 1.2V wide range as specified in the JESD8-12 specification.

**4:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

### 2.7.3 DETAILED I/O DC CHARACTERISTICS

**TABLE 2-27: INPUT CAPACITANCE**

| Symbol | Definition | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | VIN = 0, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on the clock pin | VIN = 0, f = 1.0 MHz | | 8 | pF |

**TABLE 2-28: I/O OUTPUT BUFFER MAXIMUM RESISTANCES [1]**

| Standard | Drive Strength | $R_{PULL\text{-}DOWN}$ (Ω) [2] | $R_{PULL\text{-}UP}$ (Ω) [3] |
|---|---|---|---|
| 3.3V LVTTL / 3.3V LVCMOS | 2 mA | 100 | 300 |
| | 4 mA | 100 | 300 |
| | 6 mA | 50 | 150 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 25 | 75 |
| 3.3V LVCMOS Wide Range | 100 µA | Same as equivalent software default drive | |


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**TABLE 2-28: I/O OUTPUT BUFFER MAXIMUM RESISTANCES [1]**

| | | | |
|---|---|---|---|
| 2.5V LVCMOS | 2 mA | 100 | 200 |
| | 4 mA | 100 | 200 |
| | 6 mA | 50 | 100 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| 1.8V, LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| 1.5V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| 1.2V LVCMOS | 2 mA | 157.5 | 163.8 |
| 1.2V LVCMOS Wide Range[4] | 100 µA | 157.5 | 163.8 |

**Note 1:** These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on $VCC_I$, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS model on the Microchip website at https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-fpgas#IGLOOPlusibis.

**2:** $R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec

**3:** $R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / IOHspec

**4:** Applicable to IGLOO PLUS V2 devices operating at VCCI ≥ VCC.

**TABLE 2-29: I/O WEAK PULL-UP/PULL-DOWN RESISTANCES—MINIMUM AND MAXIMUM WEAK PULL-UP/PULL-DOWN RESISTANCE VALUES**

| VCCI | $R_{(WEAK\ PULL\text{-}UP)}$ [1] (Ω) | | $R_{(WEAK\ PULL\text{-}DOWN)}$ [2] (Ω) | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| 3.3V | 10 K | 45 K | 10 K | 45 K |
| 3.3 V (wide range I/Os) | 10 K | 45 K | 10 K | 45 K |
| 2.5V | 11 K | 55 K | 12 K | 74 K |
| 1.8V, | 18 K | 70 K | 17 K | 110 K |
| 1.5V | 19 K | 90 K | 19 K | 140 K |
| 1.2V | 25 K | 110 K | 25 K | 150 K |
| 1.2V (wide range I/Os) | 19 K | 110 K | 19 K | 150 K |

**Note 1:** $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / $I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$

**2:** $R_{(WEAK\ PULLDOWN\text{-}MAX)}$ = (VOLspec) / $I_{(WEAK\ PULLDOWN\text{-}MIN)}$

**TABLE 2-30: I/O SHORT CURRENTS IOSH/IOSL**

| | Drive Strength | IOSL (mA)* | IOSH (mA)* |
|---|---|---|---|
| 3.3V LVTTL/3.3V LVCMOS | 2 mA | 27 | 25 |
| | 4 mA | 27 | 25 |
| | 6 mA | 54 | 51 |
| | 8 mA | 54 | 51 |
| | 12 mA | 109 | 103 |
| | 16 mA | 109 | 103 |

**Note:** *$T_J$ = 100 °C

**TABLE 2-30: I/O SHORT CURRENTS IOSH/IOSL**

| | Drive Strength | IOSL (mA)* | IOSH (mA)* |
|---|---|---|---|
| 3.3V LVCMOS Wide Range | 100 µA | Same as equivalent software default drive | |
| 2.5V LVCMOS | 2 mA | 18 | 16 |
| | 4 mA | 18 | 16 |
| | 6 mA | 37 | 32 |
| | 8 mA | 37 | 32 |
| | 12 mA | 74 | 65 |
| 1.8V, LVCMOS | 2 mA | 11 | 9 |
| | 4 mA | 22 | 17 |
| | 6 mA | 44 | 35 |
| | 8 mA | 44 | 35 |
| 1.5V LVCMOS | 2 mA | 16 | 13 |
| | 4 mA | 33 | 25 |
| 1.2V LVCMOS | 2 mA | 26 | 20 |
| 1.2V LVCMOS Wide Range | 100 µA | 26 | 20 |

**Note:** *$T_J$ = 100 °C

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100 °C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

**TABLE 2-31: DURATION OF SHORT CIRCUIT EVENT BEFORE FAILURE**

| Temperature | Time before Failure |
|---|---|
| –40 °C | > 20 years |
| 0 °C | > 20 years |
| 25 °C | > 20 years |
| 70 °C | 5 years |
| 85 °C | 2 years |
| 100 °C | 6 months |

**TABLE 2-32: SCHMITT TRIGGER INPUT HYSTERESIS**

**Hysteresis Voltage Value (Typ.) for Schmitt Mode Input Buffers**

| Input Buffer Configuration | Hysteresis Value (typ.) |
|---|---|
| 3.3V LVTTL/LVCMOS (Schmitt trigger mode) | 240 mV |
| 2.5V LVCMOS (Schmitt trigger mode) | 140 mV |
| 1.8V, LVCMOS (Schmitt trigger mode) | 80 mV |
| 1.5V LVCMOS (Schmitt trigger mode) | 60 mV |
| 1.2V LVCMOS (Schmitt trigger mode) | 40 mV |

**TABLE 2-33: I/O INPUT RISE TIME, FALL TIME, AND RELATED I/O RELIABILITY[1]**

| Input Buffer | Input Rise/Fall Time (min.) | Input Rise/Fall Time (max.) | Reliability |
|---|---|---|---|
| LVTTL/LVCMOS (Schmitt trigger disabled) | No requirement | 10 ns [2] | 20 years (100 °C) |


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**TABLE 2-33: I/O INPUT RISE TIME, FALL TIME, AND RELATED I/O RELIABILITY[1]**

| Input Buffer | Input Rise/Fall Time (min.) | Input Rise/Fall Time (max.) | Reliability |
|---|---|---|---|
| LVTTL/LVCMOS (Schmitt trigger enabled) | No requirement | No requirement, but input noise voltage cannot exceed Schmitt hysteresis. | 20 years (100 °C) |

**Note 1:** For clock signals and similar edge-generating signals, please, refer to SSO application note.

**2:** The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microchip recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

## 2.7.4 SINGLE-ENDED I/O CHARACTERISTICS

### 2.7.4.1 3.3V LVTTL/3.3V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3V applications. It uses an LVTTL input buffer and push-pull output buffer.

**TABLE 2-34: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS**

| 3.3V LVTTL / 3.3V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 2 | 2 | 25 | 27 | 10 | 10 |
| 4 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 25 | 27 | 10 | 10 |
| 6 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 6 | 6 | 51 | 54 | 10 | 10 |
| 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 51 | 54 | 10 | 10 |
| 12 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 | 103 | 109 | 10 | 10 |
| 16 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 16 | 16 | 103 | 109 | 10 | 10 |

**Note 1:** IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

**2:** IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

**3:** Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.

**4:** Currents are measured at 85 °C junction temperature.

**5:** Software default selection highlighted in gray.

**FIGURE 2-7: AC LOADING**

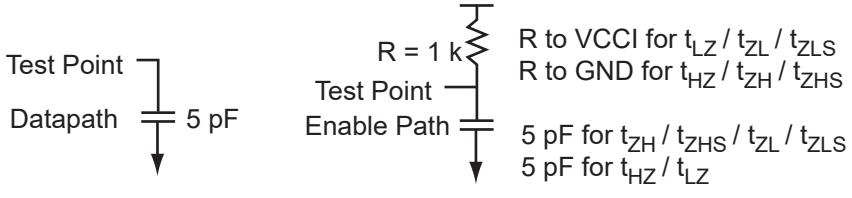


**TABLE 2-35: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS**

| Input Low (V) | Input High (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 3.3 | 1.4 | 5 |

**Note:** *Measuring point = Vtrip. See Table 2-23 for a complete table of trip points.

*2.7.4.1.1 Timing Characteristics*

**Applies to 1.5V DC Core Voltage**

**TABLE 2-36: 3.3V LVTTL / 3.3V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 3.0V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 3.94 | 0.18 | 0.85 | 1.15 | 0.66 | 4.02 | 3.46 | 1.82 | 1.87 | ns |
| 4 mA | STD | 0.97 | 3.94 | 0.18 | 0.85 | 1.15 | 0.66 | 4.02 | 3.46 | 1.82 | 1.87 | ns |
| 6 mA | STD | 0.97 | 3.20 | 0.18 | 0.85 | 1.15 | 0.66 | 3.27 | 2.94 | 2.04 | 2.27 | ns |
| 8 mA | STD | 0.97 | 3.20 | 0.18 | 0.85 | 1.15 | 0.66 | 3.27 | 2.94 | 2.04 | 2.27 | ns |
| 12 mA | STD | 0.97 | 2.72 | 0.18 | 0.85 | 1.15 | 0.66 | 2.78 | 2.57 | 2.20 | 2.53 | ns |
| 16 mA | STD | 0.97 | 2.72 | 0.18 | 0.85 | 1.15 | 0.66 | 2.78 | 2.57 | 2.20 | 2.53 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**TABLE 2-37: 3.3V LVTTL / 3.3V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 3.0V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 2.36 | 0.18 | 0.85 | 1.15 | 0.66 | 2.41 | 1.90 | 1.82 | 1.98 | ns |
| 4 mA | STD | 0.97 | 2.36 | 0.18 | 0.85 | 1.15 | 0.66 | 2.41 | 1.90 | 1.82 | 1.98 | ns |
| 6 mA | STD | 0.97 | 1.96 | 0.18 | 0.85 | 1.15 | 0.66 | 2.01 | 1.56 | 2.04 | 2.38 | ns |
| 8 mA | STD | 0.97 | 1.96 | 0.18 | 0.85 | 1.15 | 0.66 | 2.01 | 1.56 | 2.04 | 2.38 | ns |
| 12 mA | STD | 0.97 | 1.76 | 0.18 | 0.85 | 1.15 | 0.66 | 1.80 | 1.39 | 2.20 | 2.64 | ns |
| 16 mA | STD | 0.97 | 1.76 | 0.18 | 0.85 | 1.15 | 0.66 | 1.80 | 1.39 | 2.20 | 2.64 | ns |

**Note 1:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**2:** Software default selection highlighted in gray.

**Applies to 1.2V DC Core Voltage**

**TABLE 2-38: 3.3V LVTTL / 3.3V LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 3.0V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.98 | 4.56 | 0.19 | 0.99 | 1.37 | 0.67 | 4.63 | 3.98 | 2.26 | 2.57 | ns |
| 4 mA | STD | 0.98 | 4.56 | 0.19 | 0.99 | 1.37 | 0.67 | 4.63 | 3.98 | 2.26 | 2.57 | ns |
| 6 mA | STD | 0.98 | 3.80 | 0.19 | 0.99 | 1.37 | 0.67 | 3.96 | 3.45 | 2.49 | 2.98 | ns |
| 8 mA | STD | 0.98 | 3.80 | 0.19 | 0.99 | 137 | 0.67 | 3.86 | 3.45 | 2.49 | 2.98 | ns |
| 12 mA | STD | 0.98 | 3.31 | 0.19 | 0.99 | 1.37 | 0.67 | 3.36 | 3.07 | 2.65 | 3.25 | ns |
| 16 mA | STD | 0.98 | 3.31 | 0.19 | 0.99 | 1.37 | 0.67 | 3.36 | 3.07 | 2.65 | 3.25 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.


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**TABLE 2-39: 3.3V LVTTL / 3.3V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 3.0V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.98 | 2.92 | 0.19 | 0.99 | 1.37 | 0.67 | 2.97 | 2.38 | 2.25 | 2.70 | ns |
| 4 mA | STD | 0.98 | 2.92 | 0.19 | 0.99 | 1.37 | 0.67 | 2.97 | 2.38 | 2.25 | 2.70 | ns |
| 6 mA | STD | 0.98 | 2.52 | 0.19 | 0.99 | 1.37 | 0.67 | 2.56 | 2.03 | 2.49 | 3.11 | ns |
| 8 mA | STD | 0.98 | 2.52 | 0.19 | 0.99 | 1.37 | 0.67 | 2.56 | 2.03 | 2.49 | 3.11 | ns |
| 12 mA | STD | 0.98 | 2.31 | 0.19 | 0.99 | 1.37 | 0.67 | 2.34 | 1.86 | 2.65 | 3.38 | ns |
| 16 mA | STD | 0.98 | 2.31 | 0.19 | 0.99 | 1.37 | 0.67 | 2.34 | 1.86 | 2.65 | 3.38 | ns |

**Note 1:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.
**2:** Software default selection highlighted in gray

### 2.7.4.2 3.3V LVCMOS Wide Range

**TABLE 2-40: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS**

| 3.3V LVCMOS Wide Range | Equivalent Software Default Drive Strength Option[1] | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[2] | IIH[3] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | µA | µA | Max. µA[4] | Max. µA[4] | µA[5] | µA[5] |
| 100 µA | 2 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 µA | 4 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | VDD – 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 µA | 6 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | VDD – 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 µA | 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | VDD – 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 µA | 12 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | VDD – 0.2 | 100 | 100 | 103 | 109 | 10 | 10 |
| 100 µA | 16 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | VDD – 0.2 | 100 | 100 | 103 | 109 | 10 | 10 |

**Note 1:** The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
**2:** IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.
**3:** IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < V CCI. Input current is larger when operating outside recommended ranges.
**4:** Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
**5:** Currents are measured at 85 °C junction temperature.
**6:** Software default selection highlighted in gray.

**TABLE 2-41: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS**

| Input Low (V) | Input High (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 3.3 | 1.4 | 5 |

**Note:** *Measuring point = Vtrip. See Table 2-23 for a complete table of trip points.

*2.7.4.2.1 Timing Characteristics*

**Applies to 1.5V DC Core Voltage**

**TABLE 2-42: 3.3V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 2.7V**

| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 4 mA | STD | 0.97 | 5.85 | 0.18 | 1.18 | 1.64 | 0.66 | 5.86 | 5.05 | 2.57 | 2.57 | ns |
| 100 µA | 6 mA | STD | 0.97 | 4.70 | 0.18 | 1.18 | 1.64 | 0.66 | 4.72 | 4.27 | 2.92 | 3.19 | ns |
| 100 µA | 8 mA | STD | 0.97 | 4.70 | 0.18 | 1.18 | 1.64 | 0.66 | 4.72 | 4.27 | 2.92 | 3.19 | ns |
| 100 µA | 12 mA | STD | 0.97 | 3.96 | 0.18 | 1.18 | 1.64 | 0.66 | 3.98 | 3.70 | 3.16 | 3.59 | ns |
| 100 µA | 16 mA | STD | 0.97 | 3.96 | 0.18 | 1.18 | 1.64 | 0.66 | 3.98 | 3.70 | 3.16 | 3.59 | ns |

**Note 1:** The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

**2:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**TABLE 2-43: 3.3V LVCMOS WIDE RANGE HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 2.7V**

| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 4 mA | STD | 0.97 | 3.39 | 0.18 | 1.18 | 1.64 | 0.66 | 3.41 | 2.69 | 2.57 | 2.73 | ns |
| 100 µA | 6 mA | STD | 0.97 | 2.79 | 0.18 | 1.18 | 1.64 | 0.66 | 2.80 | 2.17 | 2.92 | 3.36 | ns |
| 100 µA | 8 mA | STD | 0.97 | 2.79 | 0.18 | 1.18 | 1.64 | 0.66 | 2.80 | 2.17 | 2.92 | 3.36 | ns |
| 100 µA | 12 mA | STD | 0.97 | 2.47 | 0.18 | 1.18 | 1.64 | 0.66 | 2.48 | 1.91 | 3.16 | 3.76 | ns |
| 100 µA | 16 mA | STD | 0.97 | 2.47 | 0.18 | 1.18 | 1.64 | 0.66 | 2.48 | 1.91 | 3.16 | 3.76 | ns |

**Note 1:** The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

**2:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**3:** Software default selection highlighted in gray.


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**Applies to 1.2V DC Core Voltage**

**TABLE 2-44: 3.3V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 2.7V**

| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 4 mA | STD | 0.98 | 6.68 | 0.19 | 1.32 | 1.92 | 0.67 | 6.68 | 5.74 | 3.13 | 3.47 | ns |
| 100 µA | 6 mA | STD | 0.98 | 5.51 | 0.19 | 1.32 | 1.92 | 0.67 | 5.51 | 4.94 | 3.48 | 4.11 | ns |
| 100 µA | 8 mA | STD | 0.98 | 5.51 | 0.19 | 1.32 | 1.92 | 0.67 | 5.51 | 4.94 | 3.48 | 4.11 | ns |
| 100 µA | 12 mA | STD | 0.98 | 4.75 | 0.19 | 1.32 | 1.92 | 0.67 | 4.75 | 4.36 | 3.73 | 4.52 | ns |
| 100 µA | 16 mA | STD | 0.98 | 4.75 | 0.19 | 1.32 | 1.92 | 0.67 | 4.75 | 4.36 | 3.73 | 4.52 | ns |

**Note 1:** The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

**2:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**TABLE 2-45: 3.3V LVCMOS WIDE RANGE HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 2.7V**

| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 4 mA | STD | 0.98 | 4.16 | 0.19 | 1.32 | 1.92 | 0.67 | 4.16 | 3.32 | 3.12 | 3.66 | ns |
| 100 µA | 6 mA | STD | 0.98 | 3.54 | 0.19 | 1.32 | 1.92 | 0.67 | 3.54 | 2.79 | 3.48 | 4.31 | ns |
| 100 µA | 8 mA | STD | 0.98 | 3.54 | 0.19 | 1.32 | 1.92 | 0.67 | 3.54 | 2.79 | 3.48 | 4.31 | ns |
| 100 µA | 12 mA | STD | 0.98 | 3.21 | 0.19 | 1.32 | 1.92 | 0.67 | 3.21 | 2.52 | 3.73 | 4.73 | ns |
| 100 µA | 16 mA | STD | 0.98 | 3.21 | 0.19 | 1.32 | 1.92 | 0.67 | 3.21 | 2.52 | 3.73 | 4.73 | ns |

**Note 1:** The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

**2:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**3:** Software default selection highlighted in gray.

### 2.7.4.3 2.5V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

**TABLE 2-46: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS**

| 2.5V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 2 | 2 | 16 | 18 | 10 | 10 |
| 4 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 4 | 4 | 16 | 18 | 10 | 10 |
| 6 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 6 | 6 | 32 | 37 | 10 | 10 |
| 8 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 | 32 | 37 | 10 | 10 |
| 12 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 | 65 | 74 | 10 | 10 |

**Note 1:** IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

**2:** IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

**3:** Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.

**4:** Currents are measured at 85 °C junction temperature.

**5:** Software default selection highlighted in gray.

**FIGURE 2-8: AC LOADING**

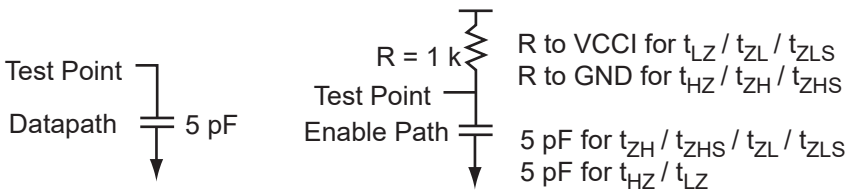



**TABLE 2-47: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS**

| Input Low (V) | Input High (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 2.5 | 1.2 | 5 |

**Note:** *Measuring point = Vtrip. See Table 2-23 for a complete table of trip points.

*2.7.4.3.1 Timing Characteristics*

**Applies to 1.5V DC Core Voltage**

**TABLE 2-48: 2.5V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 2.3V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | STD | 0.97 | 4.44 | 0.18 | 1.06 | 1.22 | 0.66 | 4.53 | 4.15 | 1.80 | 1.70 | ns |
| 6 mA | STD | 0.97 | 3.61 | 0.18 | 1.06 | 1.22 | 0.66 | 3.69 | 3.50 | 2.05 | 2.18 | ns |
| 8 mA | STD | 0.97 | 3.61 | 0.18 | 1.06 | 1.22 | 0.66 | 3.69 | 3.50 | 2.05 | 2.18 | ns |
| 12 mA | STD | 0.97 | 3.07 | 0.18 | 1.06 | 1.22 | 0.66 | 3.14 | 3.03 | 2.22 | 2.48 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.


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**TABLE 2-49: 2.5V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 2.3V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | STD | 0.97 | 2.41 | 0.18 | 1.06 | 1.22 | 0.66 | 2.47 | 2.22 | 1.79 | 1.77 | ns |
| 6 mA | STD | 0.97 | 1.99 | 0.18 | 1.06 | 1.22 | 0.66 | 2.04 | 1.75 | 2.04 | 2.25 | ns |
| 8 mA | STD | 0.97 | 1.99 | 0.18 | 1.06 | 1.22 | 0.66 | 2.04 | 1.75 | 2.04 | 2.25 | ns |
| 12 mA | STD | 0.97 | 1.77 | 0.18 | 1.06 | 1.22 | 0.66 | 1.81 | 1.51 | 2.22 | 2.56 | ns |

**Note 1:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.
**2:** Software default selection highlighted in gray.

**Applies to 1.2V DC Core Voltage**

**TABLE 2-50: 2.5 LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE $VCC_I$ = 2.3V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | STD | 0.98 | 5.04 | 0.19 | 1.19 | 1.40 | 0.67 | 5.12 | 4.65 | 2.22 | 2.36 | ns |
| 6 mA | STD | 0.98 | 4.19 | 0.19 | 1.19 | 1.40 | 0.67 | 4.25 | 3.98 | 2.48 | 2.85 | ns |
| 8 mA | STD | 0.98 | 4.19 | 0.19 | 1.19 | 1.40 | 0.67 | 4.25 | 3.98 | 2.48 | 2.85 | ns |
| 12 mA | STD | 0.98 | 3.63 | 0.19 | 1.19 | 1.40 | 0.67 | 3.69 | 3.50 | 2.66 | 3.16 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**TABLE 2-51: 2.5V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 2.3V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | STD | 0.98 | 2.96 | 0.19 | 1.19 | 1.40 | 0.67 | 3.00 | 2.67 | 2.22 | 2.46 | ns |
| 6 mA | STD | 0.98 | 2.52 | 0.19 | 1.19 | 1.40 | 0.67 | 2.56 | 2.18 | 2.47 | 2.95 | ns |
| 8 mA | STD | 0.98 | 2.52 | 0.19 | 1.19 | 1.40 | 0.67 | 2.56 | 2.18 | 2.47 | 2.95 | ns |
| 12 mA | STD | 0.98 | 2.29 | 0.19 | 1.19 | 1.40 | 0.67 | 2.32 | 1.94 | 2.65 | 3.27 | ns |

**Note 1:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.
**2:** Software default selection highlighted in gray.

### 2.7.4.4 1.8V, LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

**TABLE 2-52: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS**

| 1.8V, LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min., V | Max., V | Min., V | Max., V | Max., V | Min., V | mA | mA | Max., mA[3] | Max., mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 2 | 2 | 9 | 11 | 10 | 10 |

**TABLE 2-52: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS**

| 1.8V, LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min., V | Max., V | Min., V | Max., V | Max., V | Min., V | mA | mA | Max., mA[3] | Max., mA[3] | µA[4] | µA[4] |
| 4 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 4 | 4 | 17 | 22 | 10 | 10 |
| 6 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 6 | 6 | 35 | 44 | 10 | 10 |
| 8 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 8 | 8 | 35 | 44 | 10 | 10 |

**Note 1:** IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

**2:** IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

**3:** Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.

**4:** Currents are measured at 85 °C junction temperature.

**5:** Software default selection highlighted in gray.

**FIGURE 2-9: AC LOADING**

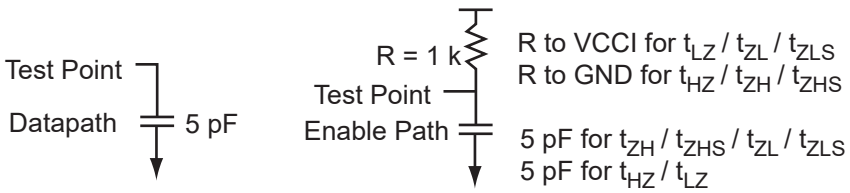



**TABLE 2-53: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS**

| Input Low (V) | Input High (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 1.8 | 0.9 | 5 |

**Note:** *Measuring point = Vtrip. See Table 2-23 for a complete table of trip points.

*2.7.4.4.1 Timing Characteristics*

**Applies to 1.5V DC Core Voltage**

**TABLE 2-54: 1.8V, LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE —COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 1.7V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 5.89 | 0.18 | 1.00 | 1.43 | 0.66 | 6.01 | 5.43 | 1.78 | 1.30 | ns |
| 4 mA | STD | 0.97 | 4.82 | 0.18 | 1.00 | 1.43 | 0.66 | 4.92 | 4.56 | 2.08 | 2.08 | ns |
| 6 mA | STD | 0.97 | 4.13 | 0.18 | 1.00 | 1.43 | 0.66 | 4.21 | 3.96 | 2.30 | 2.46 | ns |
| 8 mA | STD | 0.97 | 4.13 | 0.18 | 1.00 | 1.43 | 0.66 | 4.21 | 3.96 | 2.30 | 2.46 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.


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**TABLE 2-55: 1.8V, LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE— COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 1.7V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 2.82 | 0.18 | 1.00 | 1.43 | 0.66 | 2.88 | 2.78 | 1.78 | 1.35 | ns |
| 4 mA | STD | 0.97 | 2.30 | 0.18 | 1.00 | 1.43 | 0.66 | 2.35 | 2.11 | 2.08 | 2.15 | ns |
| 6 mA | STD | 0.97 | 2.00 | 0.18 | 1.00 | 1.43 | 0.66 | 2.04 | 1.76 | 2.29 | 2.55 | ns |
| 8 mA | STD | 0.97 | 2.00 | 0.18 | 1.00 | 1.43 | 0.66 | 2.04 | 1.76 | 2.29 | 2.55 | ns |

**Note 1:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.
**2:** Software default selection highlighted in gray.

**Applies to 1.2V DC Core Voltage**

**TABLE 2-56: 1.8V, LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE— COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 1.7V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.98 | 6.43 | 0.19 | 1.12 | 1.61 | 0.67 | 6.54 | 5.93 | 2.19 | 1.88 | ns |
| 4 mA | STD | 0.98 | 5.33 | 0.19 | 1.12 | 1.61 | 0.67 | 5.41 | 5.03 | 2.50 | 2.68 | ns |
| 6 mA | STD | 0.98 | 4.61 | 0.19 | 1.12 | 1.61 | 0.67 | 4.69 | 4.41 | 2.72 | 3.07 | ns |
| 8 mA | STD | 0.98 | 4.61 | 0.19 | 1.12 | 1.61 | 0.67 | 4.69 | 4.41 | 2.72 | 3.07 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**TABLE 2-57: 1.8V, LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE— COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 1.7V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.98 | 3.30 | 0.19 | 1.12 | 1.61 | 0.67 | 3.34 | 3.21 | 2.19 | 1.93 | ns |
| 4 mA | STD | 0.98 | 2.76 | 0.19 | 1.12 | 1.61 | 0.67 | 2.79 | 2.51 | 2.50 | 2.76 | ns |
| 6 mA | STD | 0.98 | 2.45 | 0.19 | 1.12 | 1.61 | 0.67 | 2.48 | 2.16 | 2.71 | 3.16 | ns |
| 8 mA | STD | 0.98 | 2.45 | 0.19 | 1.12 | 1.61 | 0.67 | 2.48 | 2.16 | 2.71 | 3.16 | ns |

**Note 1:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.
**2:** Software default selection highlighted in gray.

### 2.7.4.5 1.5V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

**TABLE 2-58: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS**

| 1.5V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL [1] | IIH [2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA [3] | Max. mA [3] | µA [4] | µA [4] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.7 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 13 | 16 | 10 | 10 |
| 4 mA | –0.3 | 0.35 * VCCI | 0.7 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 4 | 4 | 25 | 33 | 10 | 10 |

**TABLE 2-58: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS**

| 1.5V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL [1] | IIH [2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA [3] | Max. mA [3] | µA [4] | µA [4] |

**Note 1:** IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

**2:** IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

**3:** Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.

**4:** Currents are measured at 85 °C junction temperature.

**5:** Software default selection highlighted in gray.

**FIGURE 2-10: AC LOADING**

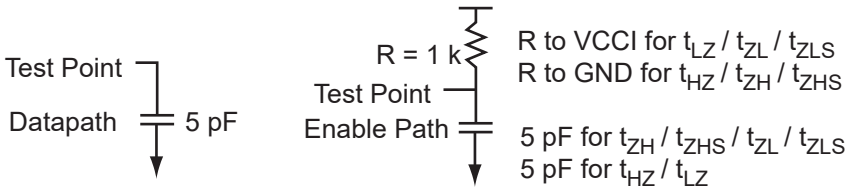



**TABLE 2-59: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS**

| Input Low (V) | Input High (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 1.5 | 0.75 | 5 |

**Note:** *Measuring point = Vtrip. See Table 2-23 for a complete table of trip points.

*2.7.4.5.1 Timing Characteristics*

**Applies to 1.5V DC Core Voltage**

**TABLE 2-60: 1.5V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 1.4V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 6.07 | 0.18 | 1.16 | 1.62 | 0.66 | 6.19 | 5.53 | 2.13 | 2.02 | ns |
| 4 mA | STD | 0.97 | 5.24 | 0.18 | 1.16 | 1.62 | 0.66 | 5.34 | 4.81 | 2.37 | 2.47 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**TABLE 2-61: 1.5V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 1.4V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 2.65 | 0.18 | 1.16 | 1.62 | 0.66 | 2.71 | 2.43 | 2.13 | 2.11 | ns |
| 4 mA | STD | 0.97 | 2.29 | 0.18 | 1.16 | 1.62 | 0.66 | 2.33 | 2.00 | 2.37 | 2.57 | ns |

**Note 1:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**2:** Software default selection highlighted in gray.


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**Applies to 1.2V DC Core Voltage**

**TABLE 2-62: 1.5V LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 1.4V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.98 | 6.57 | 0.19 | 1.26 | 1.80 | 0.67 | 6.68 | 6.01 | 2.54 | 2.59 | ns |
| 4 mA | STD | 0.98 | 5.72 | 0.19 | 1.26 | 1.80 | 0.67 | 5.81 | 5.27 | 2.79 | 3.05 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**TABLE 2-63: 1.5V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 1.4V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.98 | 3.08 | 0.19 | 1.26 | 1.80 | 0.67 | 3.13 | 2.82 | 2.53 | 2.68 | ns |
| 4 mA | STD | 0.98 | 2.71 | 0.19 | 1.26 | 1.80 | 0.67 | 2.75 | 2.39 | 2.78 | 3.15 | ns |

**Note 1:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.
**2:** Software default selection highlighted in gray.

### 2.7.4.6 1.2V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2V complies with the LVCMOS standard JESD8-12A for general purpose 1.2V applications. It uses a 1.2V input buffer and a push-pull output buffer.

**TABLE 2-64: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS**

| 1.2V LVCMOS [1] | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL [2] | IIH [3] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA [4] | Max. mA [4] | µA [5] | µA [5] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 20 | 26 | 10 | 10 |

**Note 1:** Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.
**2:** IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.
**3:** IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.
**4:** Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
**5:** Currents are measured at 85 °C junction temperature.
**6:** Software default selection highlighted in gray.

**FIGURE 2-11: AC LOADING**

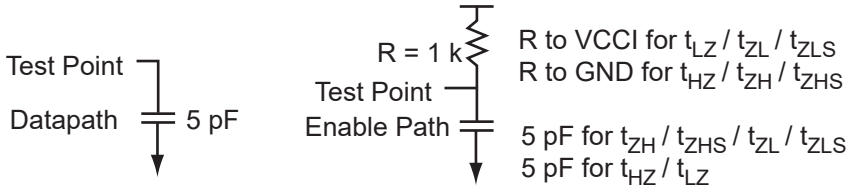


**TABLE 2-65: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS**

| Input Low (V) | Input High (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 1.2 | 0.6 | 5 |

**Note:** *Measuring point = Vtrip. See Table 2-23 for a complete table of trip points.

*2.7.4.6.1 Timing Characteristics*

**Applies to 1.2V DC Core Voltage**

**TABLE 2-66: 1.2V LVCMOS LOW SLEW**

**Commercial-Case Conditions: $T_J$ = 70 °C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.14V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.98 | 8.27 | 0.19 | 1.57 | 2.34 | 0.67 | 7.94 | 6.77 | 3.00 | 3.11 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**TABLE 2-67: 1.2V LVCMOS HIGH SLEW—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 1.14V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.98 | 3.38 | 0.19 | 1.57 | 2.34 | 0.67 | 3.26 | 2.78 | 2.99 | 3.24 | ns |

**Note 1:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**2:** Software default selection highlighted in gray.


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2.7.4.7 1.2V LVCMOS Wide Range

**TABLE 2-68: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS**

| 1.2V LVCMOS Wide Range[1] | | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[3] | IIH[4] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Equivalent Software Default Drive Strength Option[2] | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[5] | Max mA[5] | µA[6] | µA[6] |
| 100 µA | 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 20 | 26 | 10 | 10 |

**Note 1:** Applicable to V2 devices only.

**2:** The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

**3:** IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

**4:** IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

**5:** Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.

**6:** Currents are measured at 85 °C junction temperature.

**7:** Software default selection highlighted in gray.

**TABLE 2-69: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS**

| Input Low (V) | Input High (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 1.2 | 0.6 | 5 |

**Note:** *Measuring point = Vtrip. See Table 2-23 for a complete table of trip points.

*2.7.4.7.1 Timing Characteristics*

Applies to 1.2V DC Core Voltage

**TABLE 2-70: 1.2V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 1.14V**

| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 2 mA | STD | 0.98 | 8.27 | 0.19 | 1.57 | 2.34 | 0.67 | 7.94 | 6.77 | 3.00 | 3.11 | ns |

**Note 1:** The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

**2:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**TABLE 2-71: 1.2V LVCMOS WIDE RANGE HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 1.14V**

| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 2 mA | STD | 0.98 | 3.38 | 0.19 | 1.57 | 2.34 | 0.67 | 3.26 | 2.78 | 2.99 | 3.24 | ns |

**Note 1:** The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

**2:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**3:** Software default selection highlighted in gray.


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## 2.7.5 I/O REGISTER SPECIFICATIONS

### 2.7.5.1 Fully Registered I/O Buffers with Asynchronous Preset

**FIGURE 2-12: TIMING MODEL OF REGISTERED I/O BUFFERS WITH ASYNCHRONOUS PRESET**

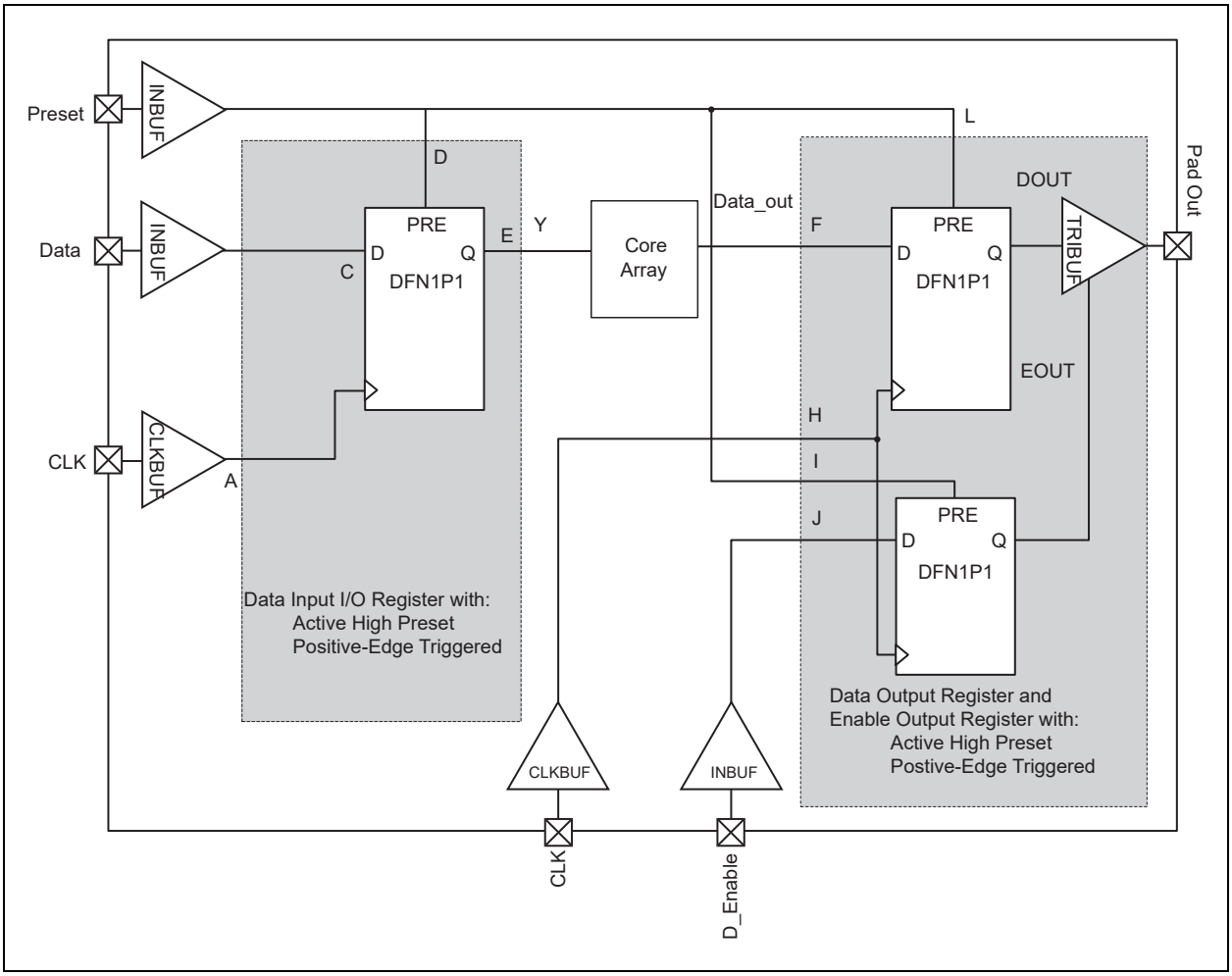



**TABLE 2-72: PARAMETER DEFINITION AND MEASURING NODES**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | H, DOUT |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | F, H |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | F, H |
| $t_{OPRE2Q}$ | Asynchronous Preset-to-Q of the Output Data Register | L, DOUT |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | L, H |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | L, H |
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | H, EOUT |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | J, H |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | J, H |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | I, EOUT |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | I, H |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | I, H |

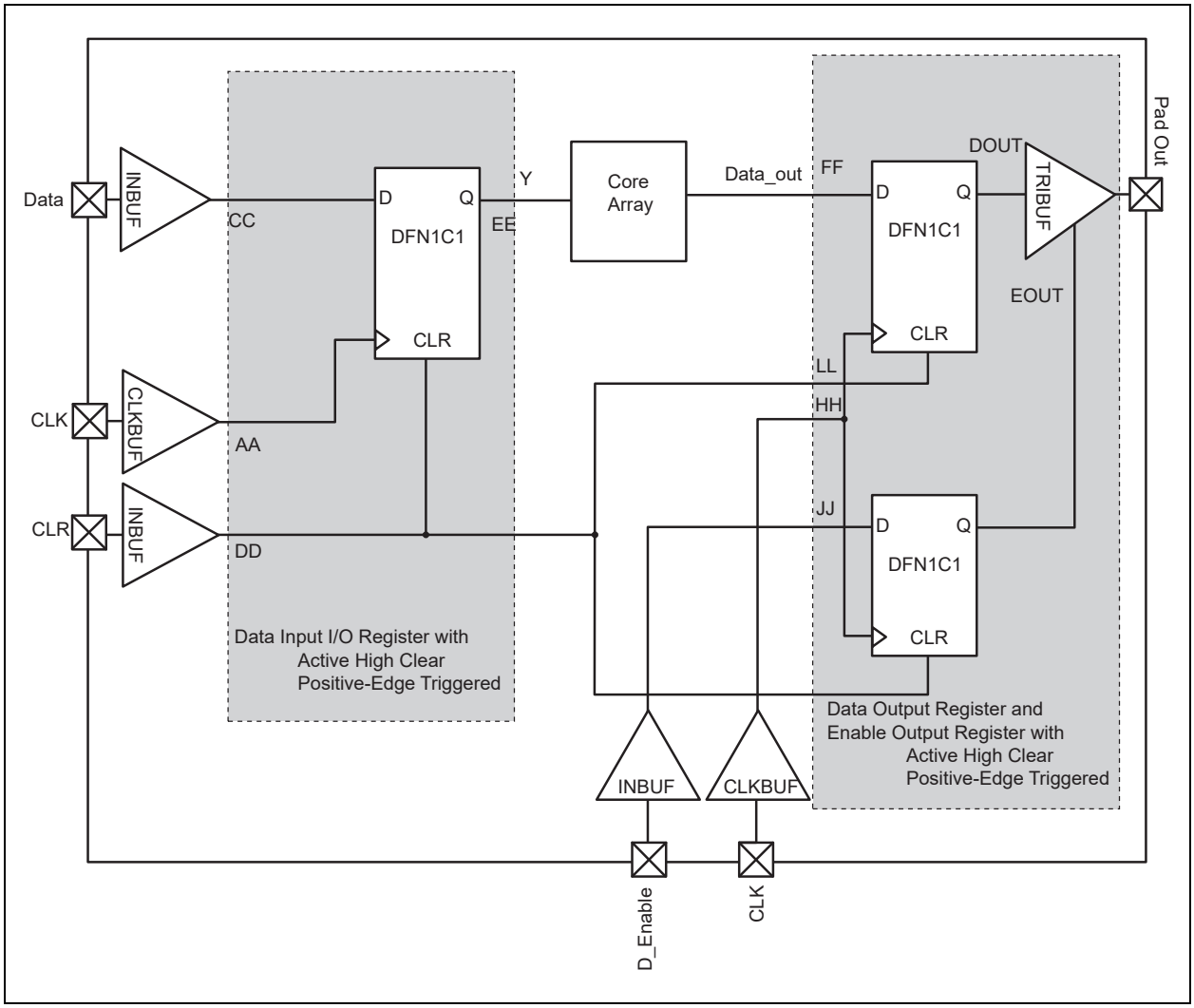
**TABLE 2-72: PARAMETER DEFINITION AND MEASURING NODES**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|---|---|---|
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | A, E |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | C, A |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | C, A |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | D, E |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | D, A |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | D, A |

**Note:** *See Figure 2-12 for more information.

2.7.5.2 Fully Registered I/O Buffers with Asynchronous Clear

**FIGURE 2-13: TIMING MODEL OF THE REGISTERED I/O BUFFERS WITH ASYNCHRONOUS CLEAR**





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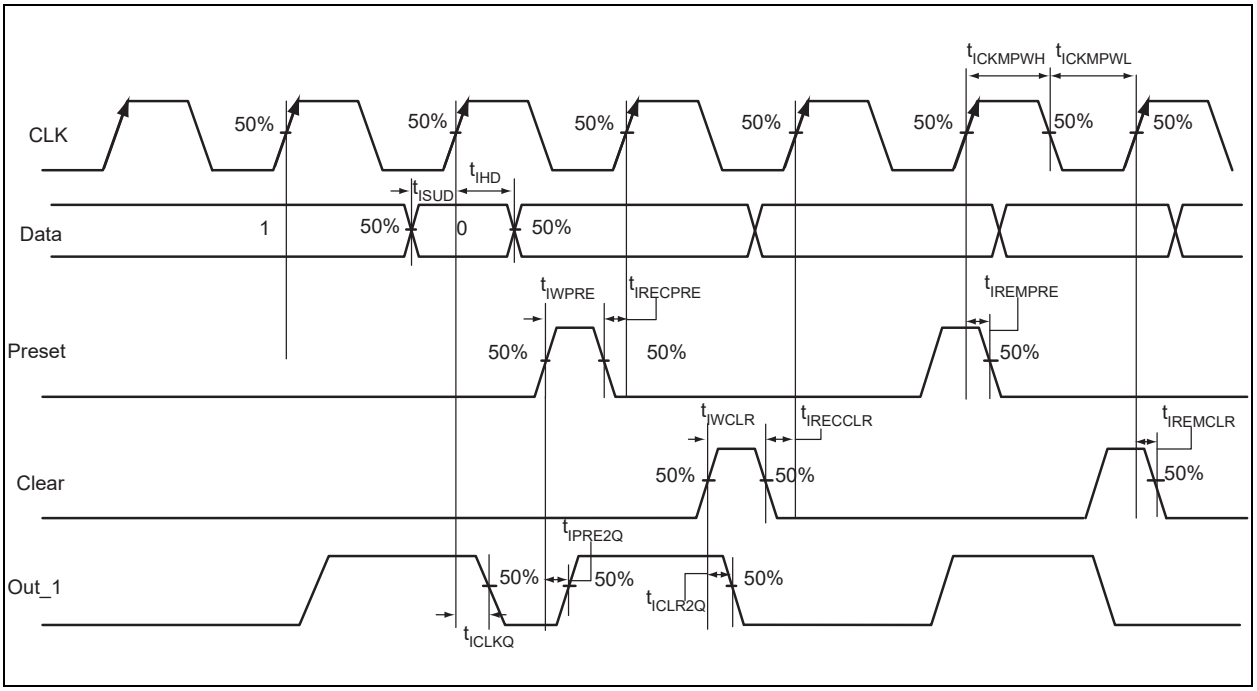
**TABLE 2-73: PARAMETER DEFINITION AND MEASURING NODES**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | HH, DOUT |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | FF, HH |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | FF, HH |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | LL, DOUT |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | LL, HH |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | LL, HH |
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | HH, EOUT |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | JJ, HH |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | JJ, HH |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | II, EOUT |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | II, HH |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | II, HH |
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | AA, EE |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | CC, AA |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | CC, AA |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | DD, EE |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | DD, AA |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | DD, AA |

**Note:** *See Figure 2-13 on page 2-52 for more information.

2.7.5.3 Input Register

**FIGURE 2-14: INPUT REGISTER TIMING DIAGRAM**




*2.7.5.3.1 Timing Characteristics*

### 1.5V DC Core Voltage

**TABLE 2-74: INPUT DATA REGISTER PROPAGATION DELAYS—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | 0.41 | ns |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | 0.32 | ns |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | 0.00 | ns |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | 0.57 | ns |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | 0.57 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{IWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width High for the Input Data Register | 0.31 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width Low for the Input Data Register | 0.28 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

### 1.2V DC Core Voltage

**TABLE 2-75: INPUT DATA REGISTER PROPAGATION DELAYS—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V**

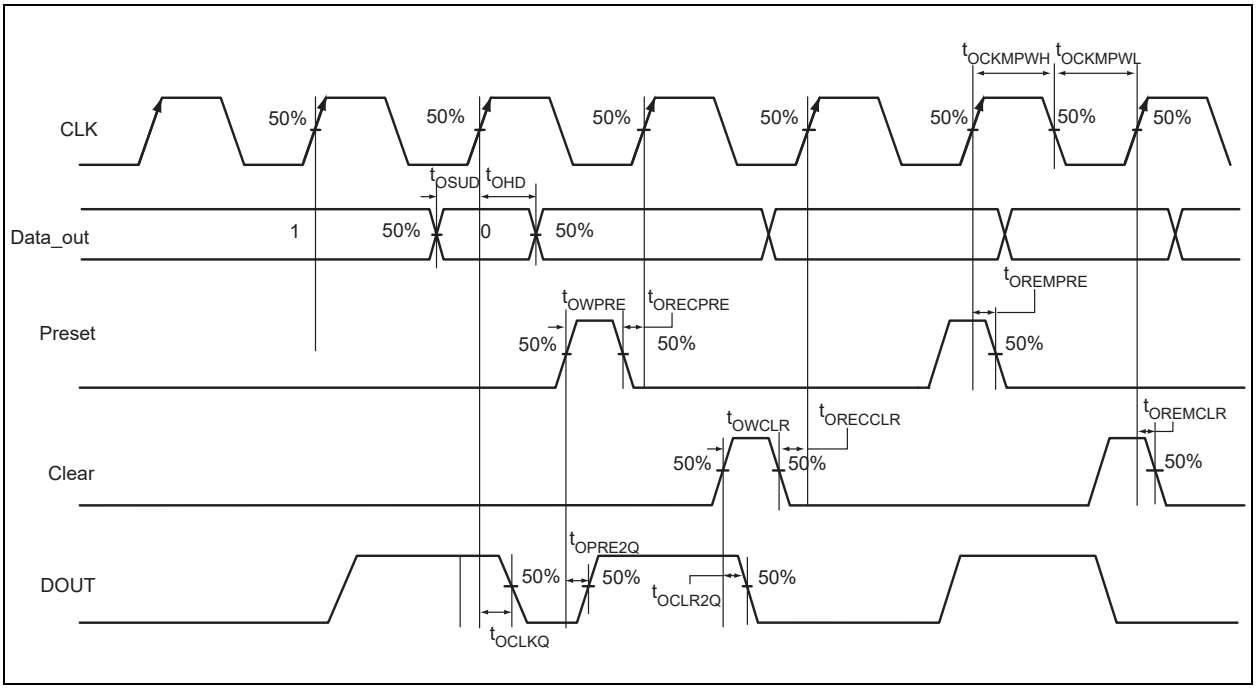
| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | 0.66 | ns |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | 0.43 | ns |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | 0.00 | ns |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | 0.86 | ns |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | 0.86 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{IWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width High for the Input Data Register | 0.31 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width Low for the Input Data Register | 0.28 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.


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### 2.7.5.4 Output Register

**FIGURE 2-15: OUTPUT REGISTER TIMING DIAGRAM**




*2.7.5.4.1 Timing Characteristics*

**1.5V DC Core Voltage**

**TABLE 2-76: OUTPUT DATA REGISTER PROPAGATION DELAYS—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | 0.66 | ns |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | 0.33 | ns |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | 0.00 | ns |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | 0.82 | ns |
| $t_{OPRE2Q}$ | Asynchronous Preset-to-Q of the Output Data Register | 0.88 | ns |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | 0.24 | ns |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | 0.24 | ns |
| $t_{OWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| $t_{OWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| $t_{OCKMPWH}$ | Clock Minimum Pulse Width High for the Output Data Register | 0.31 | ns |
| $t_{OCKMPWL}$ | Clock Minimum Pulse Width Low for the Output Data Register | 0.28 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**1.2V DC Core Voltage**

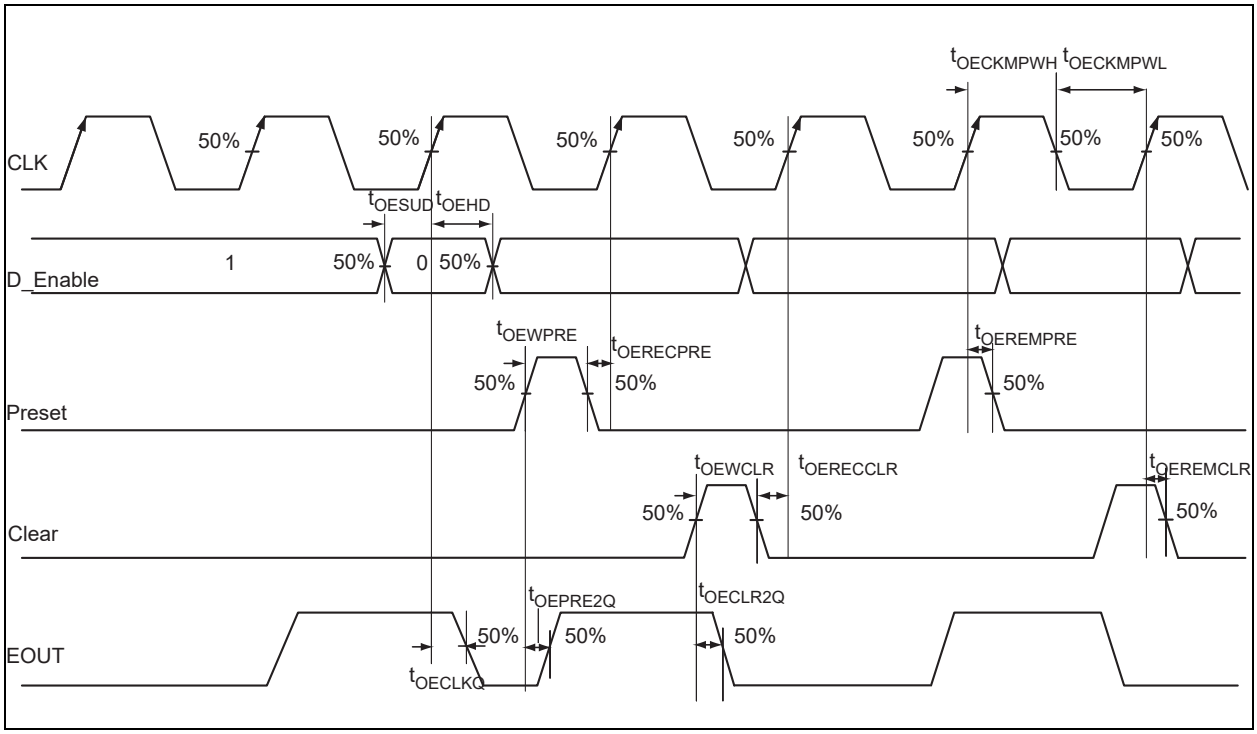
**TABLE 2-77: OUTPUT DATA REGISTER PROPAGATION DELAYS—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | 1.03 | ns |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | 0.52 | ns |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | 0.00 | ns |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | 1.22 | ns |
| $t_{OPRE2Q}$ | Asynchronous Preset-to-Q of the Output Data Register | 1.31 | ns |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | 0.24 | ns |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | 0.24 | ns |
| $t_{OWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| $t_{OWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| $t_{OCKMPWH}$ | Clock Minimum Pulse Width High for the Output Data Register | 0.31 | ns |
| $t_{OCKMPWL}$ | Clock Minimum Pulse Width Low for the Output Data Register | 0.28 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

### 2.7.5.5 Output Enable Register

**FIGURE 2-16: OUTPUT ENABLE REGISTER TIMING DIAGRAM**





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*2.7.5.5.1 Timing Characteristics*

**1.5V DC Core Voltage**

**TABLE 2-78: OUTPUT ENABLE REGISTER PROPAGATION DELAYS—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | 0.68 | ns |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | 0.33 | ns |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 0.84 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 0.91 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OEWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width High for the Output Enable Register | 0.31 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width Low for the Output Enable Register | 0.28 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**1.2V DC Core Voltage**

**TABLE 2-79: OUTPUT ENABLE REGISTER PROPAGATION DELAYS—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | 1.06 | ns |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | 0.52 | ns |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 1.25 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 1.36 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OEWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width High for the Output Enable Register | 0.31 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width Low for the Output Enable Register | 0.28 | ns |

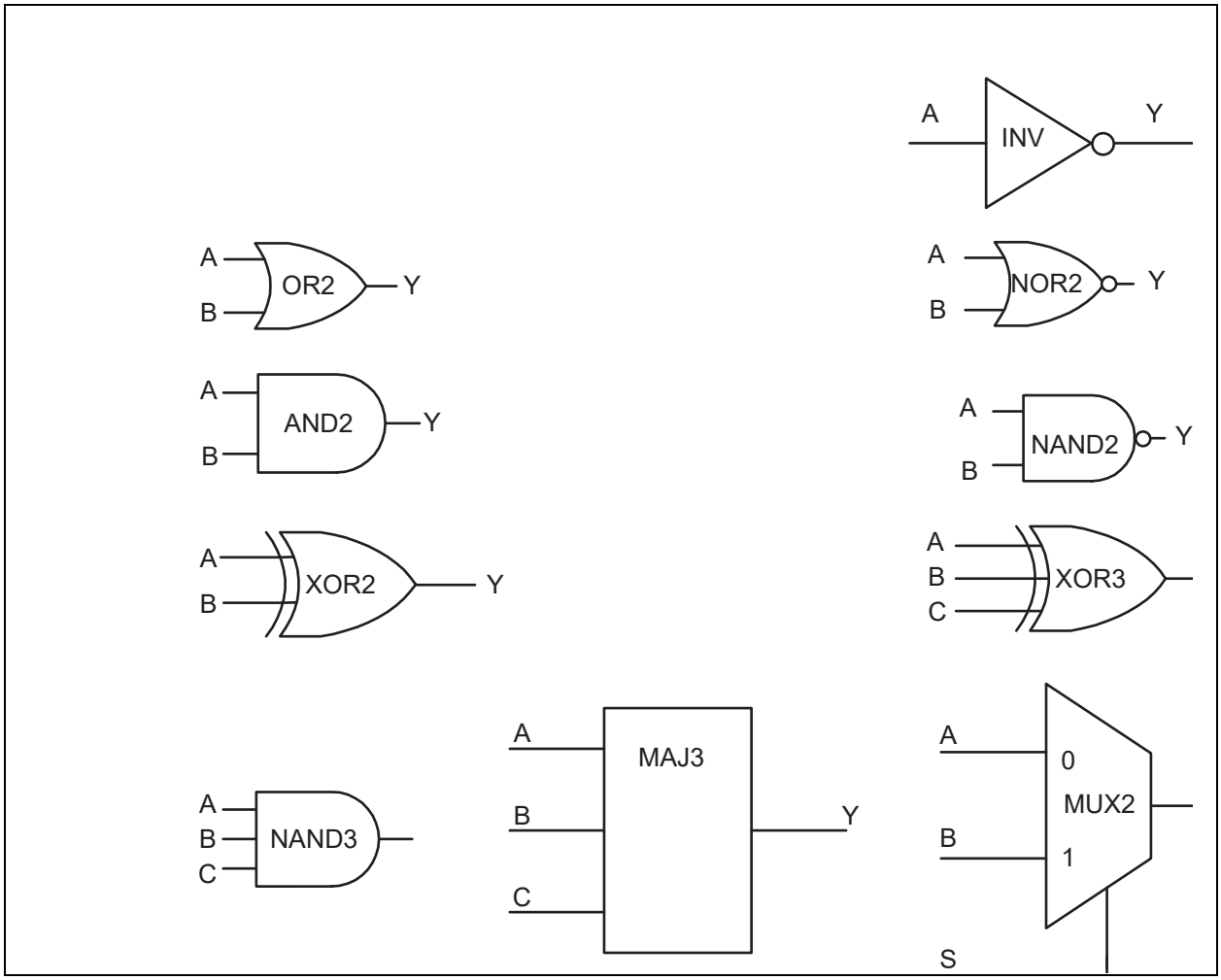
**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

## 2.8 VersaTile Characteristics

### 2.8.1 VERSATILE SPECIFICATIONS AS A COMBINATORIAL MODULE

The IGLOO PLUS library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/ E Macro Library Guide*.

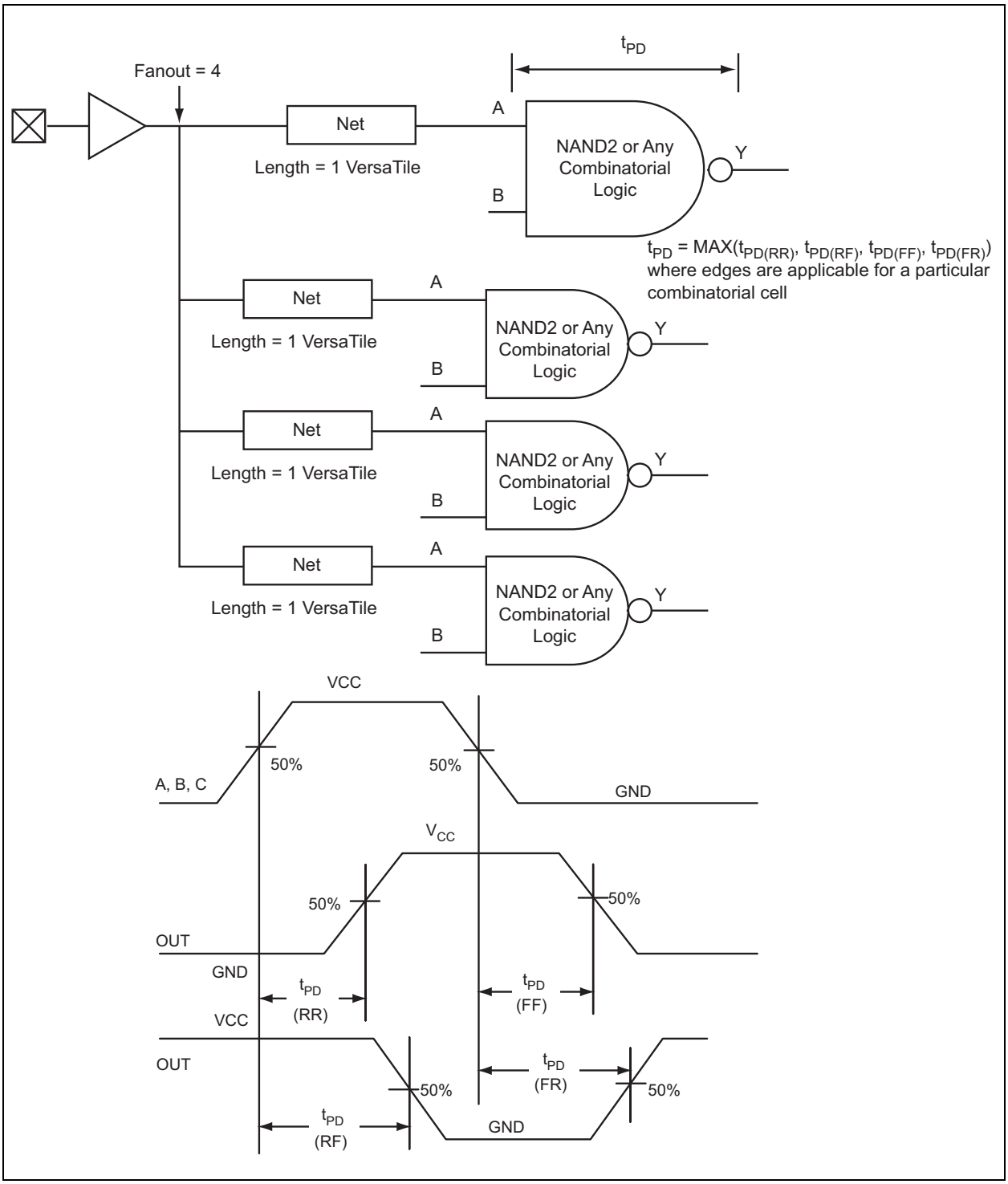
**FIGURE 2-17: SAMPLE OF COMBINATORIAL CELLS**





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**FIGURE 2-18: TIMING MODEL AND WAVEFORMS**



### 2.8.1.1 Timing Characteristics

#### *2.8.1.1.1 1.5V DC Core Voltage*

**TABLE 2-80: COMBINATORIAL CELL PROPAGATION DELAYS—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V**

| Combinatorial Cell | Equation | Parameter | Std. | Units |
|---|---|---|---|---|
| INV | Y = !A | $t_{PD}$ | 0.72 | ns |
| AND2 | Y = A · B | $t_{PD}$ | 0.86 | ns |
| NAND2 | Y = !(A · B) | $t_{PD}$ | 1.00 | ns |
| OR2 | Y = A + B | $t_{PD}$ | 1.26 | ns |
| NOR2 | Y = !(A + B) | $t_{PD}$ | 1.16 | ns |
| XOR2 | Y = A ⊕ B | $t_{PD}$ | 1.46 | ns |
| MAJ3 | Y = MAJ(A, B, C) | $t_{PD}$ | 1.47 | ns |
| XOR3 | Y = A ⊕ B ⊕ C | $t_{PD}$ | 2.12 | ns |
| MUX2 | Y = A !S + B S | $t_{PD}$ | 1.24 | ns |
| AND3 | Y = A · B · C | $t_{PD}$ | 1.40 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

#### *2.8.1.1.2 1.2V DC Core Voltage*

**TABLE 2-81: COMBINATORIAL CELL PROPAGATION DELAYS—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V**

| Combinatorial Cell | Equation | Parameter | Std. | Units |
|---|---|---|---|---|
| INV | Y = !A | $t_{PD}$ | 1.26 | ns |
| AND2 | Y = A · B | $t_{PD}$ | 1.46 | ns |
| NAND2 | Y = !(A · B) | $t_{PD}$ | 1.78 | ns |
| OR2 | Y = A + B | $t_{PD}$ | 2.47 | ns |
| NOR2 | Y = !(A + B) | $t_{PD}$ | 2.17 | ns |
| XOR2 | Y = A ⊕ B | $t_{PD}$ | 2.62 | ns |
| MAJ3 | Y = MAJ(A, B, C) | $t_{PD}$ | 2.66 | ns |
| XOR3 | Y = A ⊕ B ⊕ C | $t_{PD}$ | 3.77 | ns |
| MUX2 | Y = A !S + B S | $t_{PD}$ | 2.20 | ns |
| AND3 | Y = A · B · C | $t_{PD}$ | 2.49 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

### 2.8.2 VERSATILE SPECIFICATIONS AS A SEQUENTIAL MODULE

The IGLOO PLUS library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.


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**FIGURE 2-19: SAMPLE OF SEQUENTIAL CELLS**

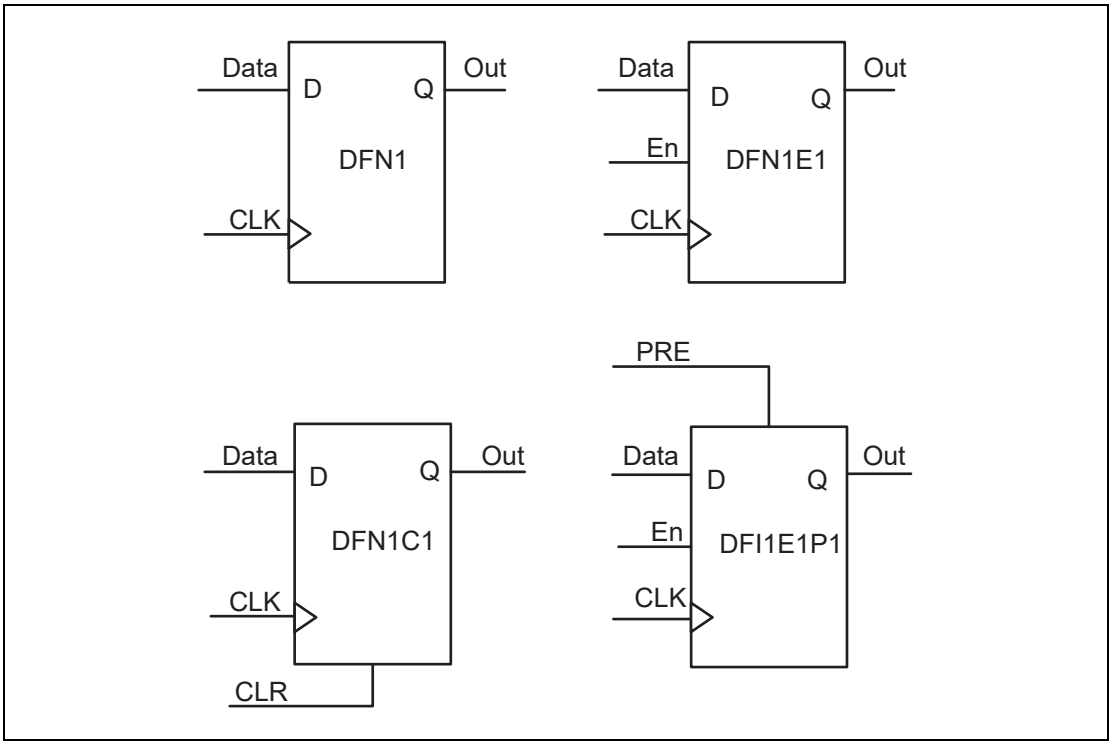
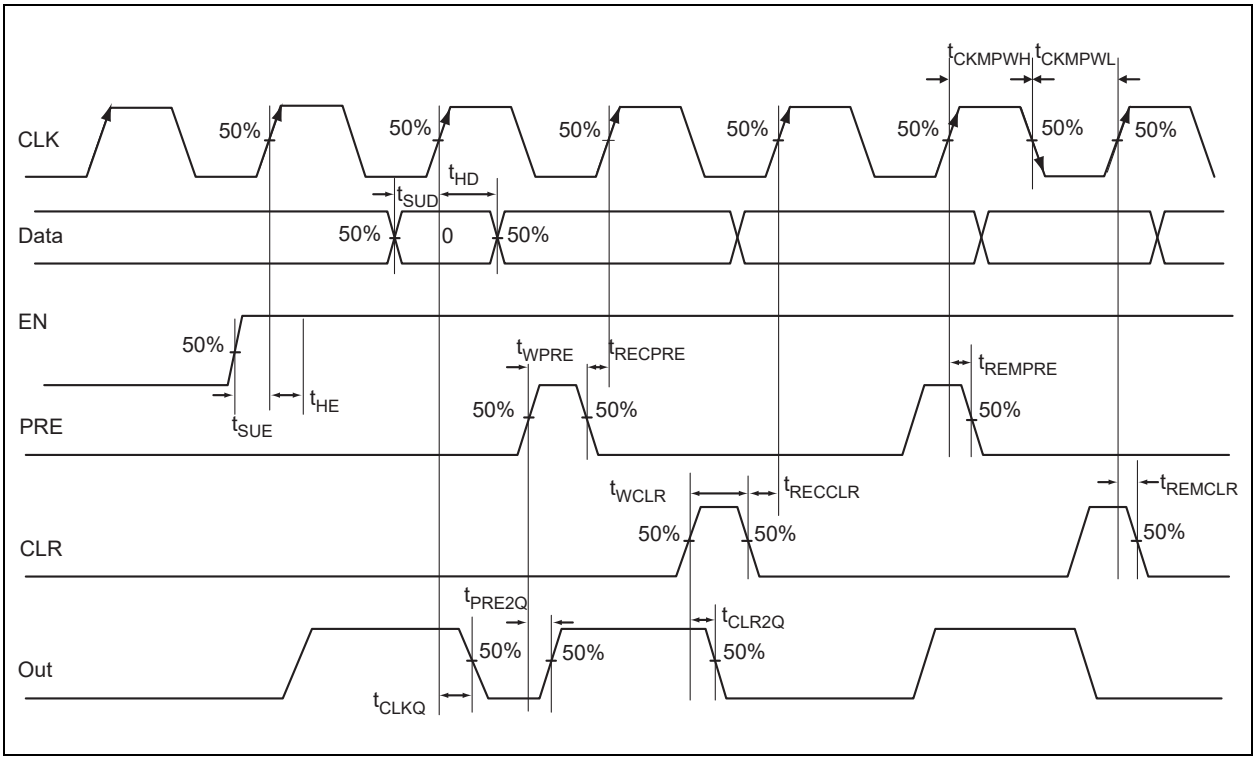



**FIGURE 2-20: TIMING MODEL AND WAVEFORMS**



### 2.8.2.1 Timing Characteristics

#### *2.8.2.1.1 1.5V DC Core Voltage*

**TABLE 2-82: REGISTER DELAYS—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{CLKQ}$ | Clock-to-Q of the Core Register | 0.89 | ns |
| $t_{SUD}$ | Data Setup Time for the Core Register | 0.81 | ns |
| $t_{HD}$ | Data Hold Time for the Core Register | 0.00 | ns |
| $t_{SUE}$ | Enable Setup Time for the Core Register | 0.73 | ns |
| $t_{HE}$ | Enable Hold Time for the Core Register | 0.00 | ns |
| $t_{CLR2Q}$ | Asynchronous Clear-to-Q of the Core Register | 0.60 | ns |
| $t_{PRE2Q}$ | Asynchronous Preset-to-Q of the Core Register | 0.62 | ns |
| $t_{REMCLR}$ | Asynchronous Clear Removal Time for the Core Register | 0.00 | ns |
| $t_{RECCLR}$ | Asynchronous Clear Recovery Time for the Core Register | 0.24 | ns |
| $t_{REMPRE}$ | Asynchronous Preset Removal Time for the Core Register | 0.00 | ns |
| $t_{RECPRE}$ | Asynchronous Preset Recovery Time for the Core Register | 0.23 | ns |
| $t_{WCLR}$ | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.30 | ns |
| $t_{WPRE}$ | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.30 | ns |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width High for the Core Register | 0.56 | ns |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width Low for the Core Register | 0.56 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

#### *2.8.2.1.2 1.2V DC Core Voltage*

**TABLE 2-83: REGISTER DELAYS—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{CLKQ}$ | Clock-to-Q of the Core Register | 1.61 | ns |
| $t_{SUD}$ | Data Setup Time for the Core Register | 1.17 | ns |
| $t_{HD}$ | Data Hold Time for the Core Register | 0.00 | ns |
| $t_{SUE}$ | Enable Setup Time for the Core Register | 1.29 | ns |
| $t_{HE}$ | Enable Hold Time for the Core Register | 0.00 | ns |
| $t_{CLR2Q}$ | Asynchronous Clear-to-Q of the Core Register | 0.87 | ns |
| $t_{PRE2Q}$ | Asynchronous Preset-to-Q of the Core Register | 0.89 | ns |
| $t_{REMCLR}$ | Asynchronous Clear Removal Time for the Core Register | 0.00 | ns |
| $t_{RECCLR}$ | Asynchronous Clear Recovery Time for the Core Register | 0.24 | ns |
| $t_{REMPRE}$ | Asynchronous Preset Removal Time for the Core Register | 0.00 | ns |
| $t_{RECPRE}$ | Asynchronous Preset Recovery Time for the Core Register | 0.24 | ns |
| $t_{WCLR}$ | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.46 | ns |
| $t_{WPRE}$ | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.46 | ns |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width High for the Core Register | 0.95 | ns |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width Low for the Core Register | 0.95 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

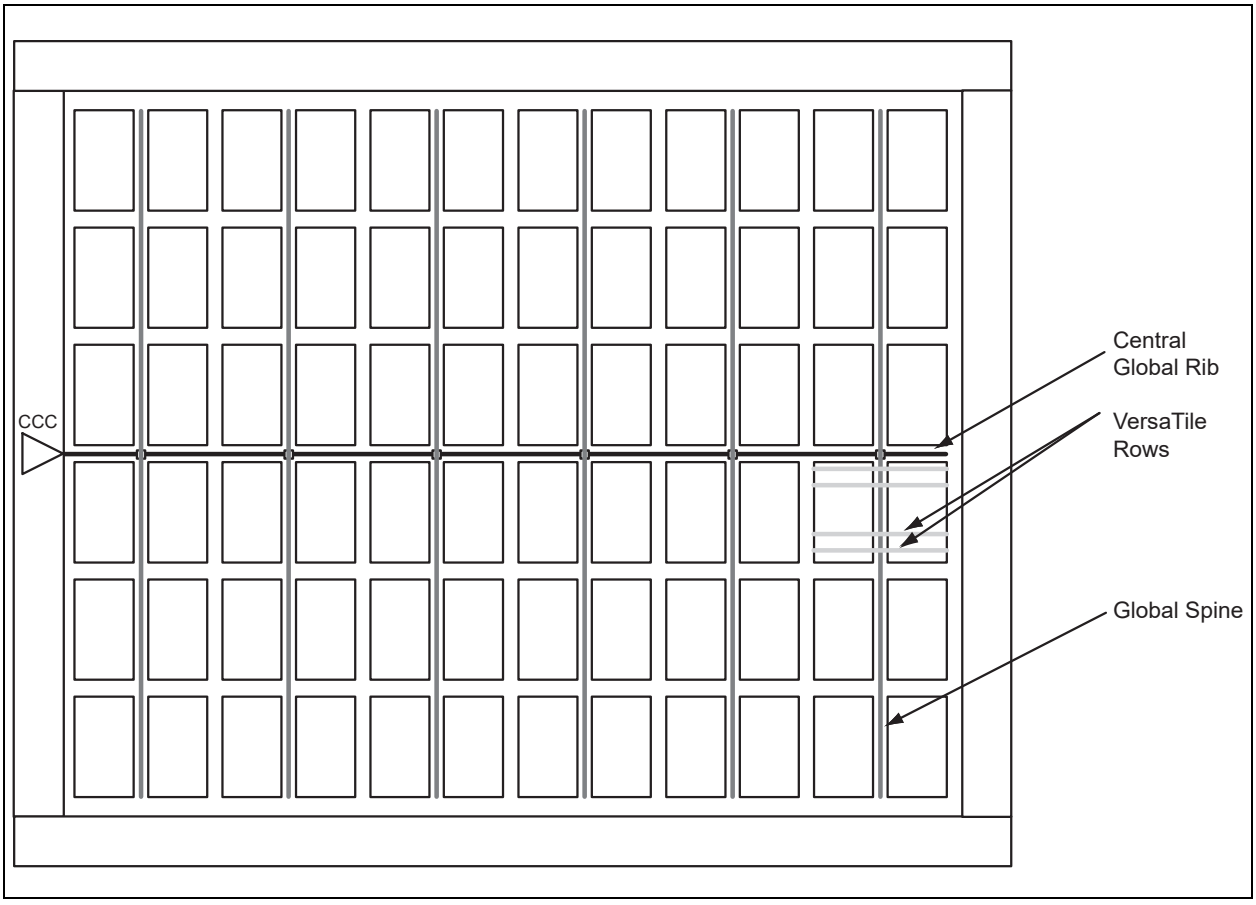

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## 2.9 Global Resource Characteristics

### 2.9.1 AGLP125 CLOCK TREE TOPOLOGY

Clock delays are device-specific. Figure 2-21 is an example of a global tree used for clock routing. The global tree presented in Figure 2-21 is driven by a CCC located on the west side of the AGLP125 device. It is used to drive all D-flip-flops in the device.

**FIGURE 2-21: EXAMPLE OF GLOBAL TREE USE IN AN AGLP125 DEVICE FOR CLOCK ROUTING**




### 2.9.2 GLOBAL TREE TIMING CHARACTERISTICS

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the Section 2.10, Clock Conditioning Circuits. Table 2-84 to Table 2-89 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

#### 2.9.2.1 Timing Characteristics

##### *2.9.2.1.1 1.5V DC Core Voltage*

**TABLE 2-84: AGLP030 GLOBAL RESOURCE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, VCC = 1.425V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.21 | 1.42 | ns |

**TABLE 2-84: AGLP030 GLOBAL RESOURCE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, VCC = 1.425V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.23 | 1.49 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.18 | — | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.15 | — | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | — | 0.27 | ns |

**Note 1:** Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

**2:** Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

**3:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**TABLE 2-85: AGLP060 GLOBAL RESOURCE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, VCC = 1.425V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.32 | 1.62 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.34 | 1.72 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.18 | — | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.15 | — | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | — | 0.38 | ns |

**Note 1:** Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

**2:** Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

**3:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**TABLE 2-86: AGLP125 GLOBAL RESOURCE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, VCC = 1.425V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.36 | 1.71 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.39 | 1.82 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.18 | — | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.15 | — | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | — | 0.43 | ns |

**Note 1:** Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

**2:** Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

**3:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.


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*2.9.2.1.2 1.2V DC Core Voltage*

**TABLE 2-87: AGLP030 GLOBAL RESOURCE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, VCC = 1.14V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.80 | 2.09 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.88 | 2.27 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.40 | — | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.65 | — | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | — | 0.39 | ns |

**Note 1:** Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

**2:** Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

**3:** For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

**TABLE 2-88: AGLP060 GLOBAL RESOURCE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, VCC = 1.14V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 2.02 | 2.43 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 2.09 | 2.65 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.40 | — | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.65 | — | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | — | 0.56 | ns |

**Note 1:** Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

**2:** Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

**3:** For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

**TABLE 2-89: AGLP125 GLOBAL RESOURCE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, VCC = 1.14V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 2.08 | 2.54 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 2.15 | 2.77 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.40 | — | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.65 | — | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | — | 0.62 | ns |

**TABLE 2-89: AGLP125 GLOBAL RESOURCE—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, VCC = 1.14V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |

**Note 1:** Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

**2:** Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

**3:** For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

## 2.10 Clock Conditioning Circuits

### 2.10.1 CCC ELECTRICAL SPECIFICATIONS

#### 2.10.1.1 Timing Characteristics

**TABLE 2-90: IGLOO® PLUS CCC/PLL SPECIFICATION—FOR IGLOO PLUS V2 OR V5 DEVICES, 1.5V DC CORE SUPPLY VOLTAGE**

| Parameter | — | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Clock Conditioning Circuitry Input Frequency $f_{IN_CCC}$ | | 1.5 | — | 250 | MHz |
| Clock Conditioning Circuitry Output Frequency $f_{OUT_CCC}$ | | 0.75 | — | 250 | MHz |
| Delay Increments in Programmable Delay Blocks [1, 2] | | — | 360[3] | — | ps |
| Number of Programmable Values in Each Programmable Delay Block | | — | — | 32 | |
| Serial Clock (SCLK) for Dynamic PLL[4,5] | — | — | — | 100 | MHz |
| Input Cycle-to-Cycle Jitter (peak magnitude) | — | — | — | 1 | ns |
| Acquisition Time | — | — | — | — | — |
| | LockControl = 0 | — | — | 300 | µs |
| | LockControl = 1 | — | — | 6.0 | ms |
| Tracking Jitter[6] | — | — | — | — | — |
| | LockControl = 0 | — | — | 2.5 | ns |
| | LockControl = 1 | — | — | 1.5 | ns |
| Output Duty Cycle | — | 48.5 | — | 51.5 | % |
| Delay Range in Block: Programmable Delay 1 [1, 2] | — | 1.25 | — | 15.65 | ns |
| Delay Range in Block: Programmable Delay 2 [1, 2] | — | 0.469 | — | 15.65 | ns |
| Delay Range in Block: Fixed Delay [1, 2] | — | — | 3.5 | — | ns |
| VCO Output Peak-to-Peak Period Jitter $F_{CCC_OUT}$[7] | — | Maximum Peak-to-Peak Period Jitter[7,8,9] | | | |
| | — | SSO ≤ 2 | SSO ≤ 4 | SSO ≤ 8 | SSO ≤ 16 |
| 0.75 MHz to 50 MHz | — | 0.50% | 0.60% | 0.80% | 1.20% |
| 50 MHz to 250 MHz | — | 2.50% | 4.00% | 6.00% | 12.00% |


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**TABLE 2-90: IGLOO® PLUS CCC/PLL SPECIFICATION—FOR IGLOO PLUS V2 OR V5 DEVICES, 1.5V DC CORE SUPPLY VOLTAGE**

| Parameter | — | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|

**Note 1:** This delay is a function of voltage and temperature. See Table 2-6 and Table 2-7 for deratings.

**2:** $T_J$ = 25 °C, VCC = 1.5V

**3:** When the CCC/PLL core is generated by Microchip core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.

**4:** Maximum value obtained for a STD speed grade device in Worst Case Commercial Conditions. For specific junction temperature and voltage supply, refer to Table 2-6 and Table 2-7 for derating values.

**5:** The AGLP030 device does not support a PLL.

**6:** Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.

**7:** VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the per cent jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.

**8:** Measurements done with LVTTL 3.3 V 8 mA I/O drive strength and high slew rate, VCC/VCCPLL = 1.425 V, VCCI = 3.3 V, VQ/PQ/TQ type of packages, 20 pF load.

**9:** SSO are outputs that are synchronous to a single clock domain and have clock-to-out times that are within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the *IGLOO PLUS FPGA Fabric User's Guide*.

**TABLE 2-91: IGLOO® PLUS CCC/PLL SPECIFICATION—FOR IGLOO PLUS V2 DEVICES, 1.2V DC CORE SUPPLY VOLTAGE**

| Parameter | — | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Clock Conditioning Circuitry Input Frequency $f_{IN_CCC}$ | | 1.5 | — | 160 | MHz |
| Clock Conditioning Circuitry Output Frequency $f_{OUT_CCC}$ | | 0.75 | — | 160 | MHz |
| Delay Increments in Programmable Delay Blocks [1, 2] | | — | 580[3] | — | ps |
| Number of Programmable Values in Each Programmable Delay Block | | — | — | 32 | — |
| Serial Clock (SCLK) for Dynamic PLL[4,5] | — | — | — | 60 | MHz |
| Input Cycle-to-Cycle Jitter (peak magnitude) | — | — | — | .25 | ns |
| Acquisition Time | — | — | — | — | — |
| | LockControl = 0 | — | — | 300 | µs |
| | LockControl = 1 | — | — | 6.0 | ms |
| Tracking Jitter[6] | — | — | — | — | — |
| | LockControl = 0 | — | — | 4 | ns |
| | LockControl = 1 | — | — | 3 | ns |
| Output Duty Cycle | — | 48.5 | — | 51.5 | % |
| Delay Range in Block: Programmable Delay 1 [1, 2] | — | 2.3 | — | 20.86 | ns |
| Delay Range in Block: Programmable Delay 2 [1, 2] | — | 0.863 | — | 20.86 | ns |
| Delay Range in Block: Fixed Delay [1, 2] | — | — | 5.7 | — | ns |
| VCO Output Peak-to-Peak Period Jitter $F_{CCC_OUT}$[7] | | Maximum Peak-to-Peak Period Jitter[7,8,9] | | | |
| | — | SSO ≤ 2 | SSO ≤ 4 | SSO ≤ 8 | SSO ≤ 16 |
| 0.75 MHz to 50 MHz | — | 0.50% | 1.20% | 2.00% | 3.00% |
| 50 MHz to 160 MHz | — | 2.50% | 5.00% | 7.00% | 15.00% |

**TABLE 2-91: IGLOO® PLUS CCC/PLL SPECIFICATION—FOR IGLOO PLUS V2 DEVICES, 1.2V DC CORE SUPPLY VOLTAGE**

| Parameter | — | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|

**Note 1:** This delay is a function of voltage and temperature. See Table 2-6 and Table 2-7 for deratings.

**2:** $T_J$ = 25 °C, VCC = 1.2V

**3:** When the CCC/PLL core is generated by Microchip core generator software, not all delay values of the specified delay increments are available. Refer to the online help associated with the core for more information.

**4:** Maximum value obtained for a STD speed grade device in Worst Case Commercial Conditions.For specific junction temperature and voltage supply levels, refer to Table 2-6 and Table 2-7 for derating values.

**5:** The AGLP030 device does not support PLL.

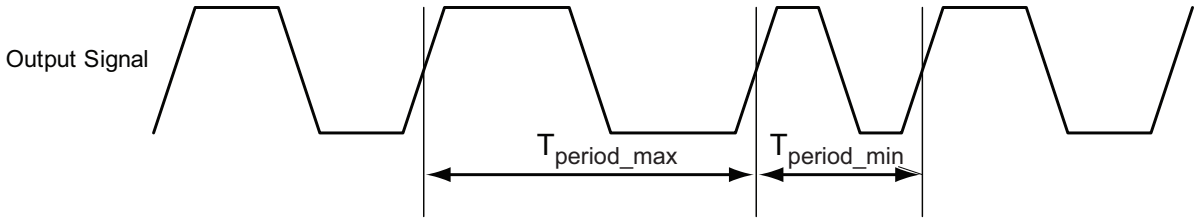
**6:** Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.

**7:** VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the per cent jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.

**8:** Measurements are done with LVTTL 3.3V, 8 mA, I/O drive strength and high slew rate. VCC/VCCPLL = 1.14V, VCCI = 3.3V, VQ/PQ/TQ type of packages, 20 pF load.

**9:** SSO are outputs that are synchronous to a single clock domain, and have their clock-to-out times within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the *IGLOO PLUS FPGA Fabric User's Guide*.

**FIGURE 2-22: PEAK-TO-PEAK JITTER DEFINITION**



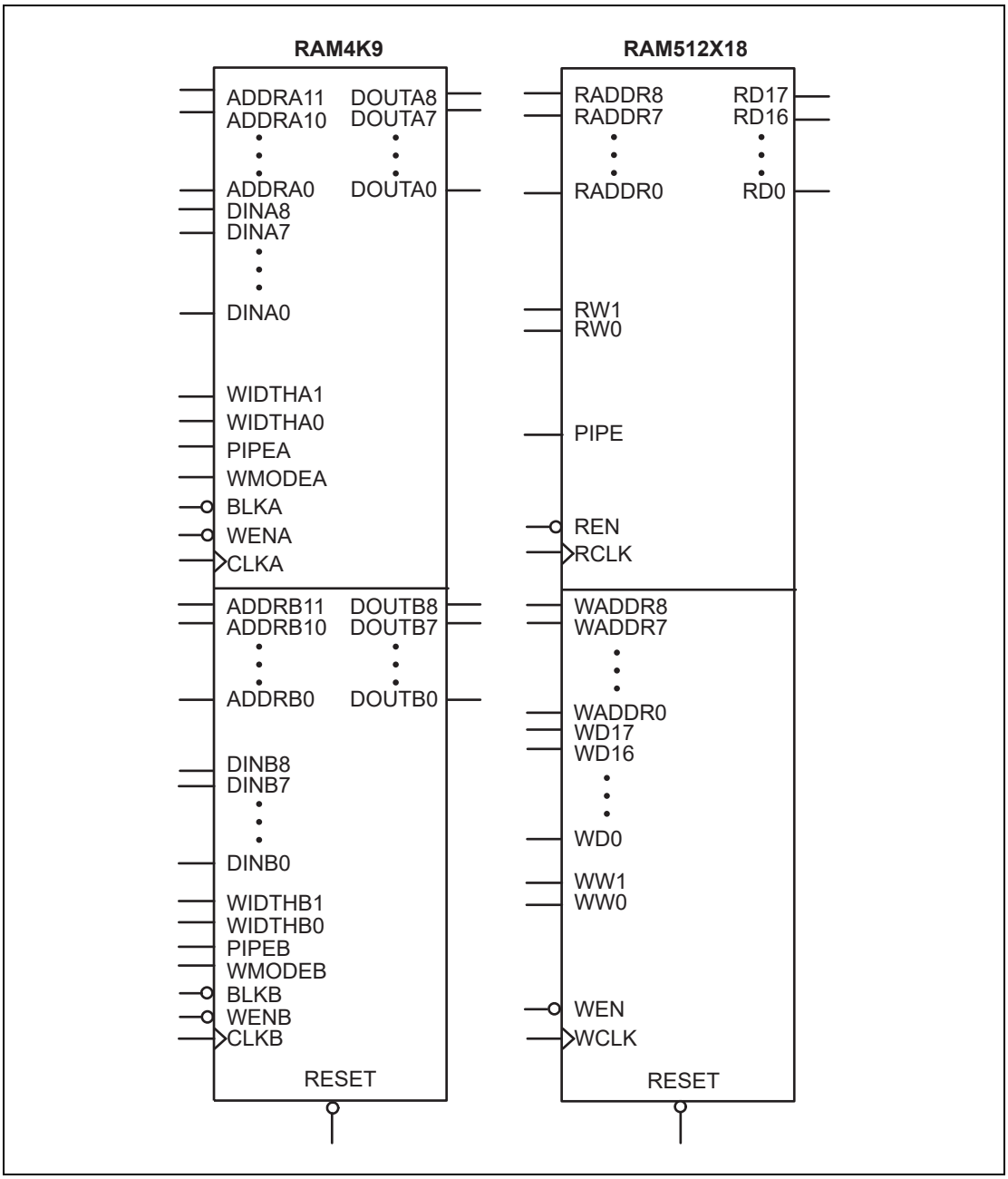

**Note:** Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period_max} - T_{period_min}$.


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## 2.11 Embedded SRAM and FIFO Characteristics

### 2.11.1 SRAM

**FIGURE 2-23: RAM MODELS**



2.11.1.1 Timing Waveforms

**FIGURE 2-24: RAM READ FOR PASS-THROUGH OUTPUT. APPLICABLE TO BOTH RAM4K9 AND RAM512X18.**

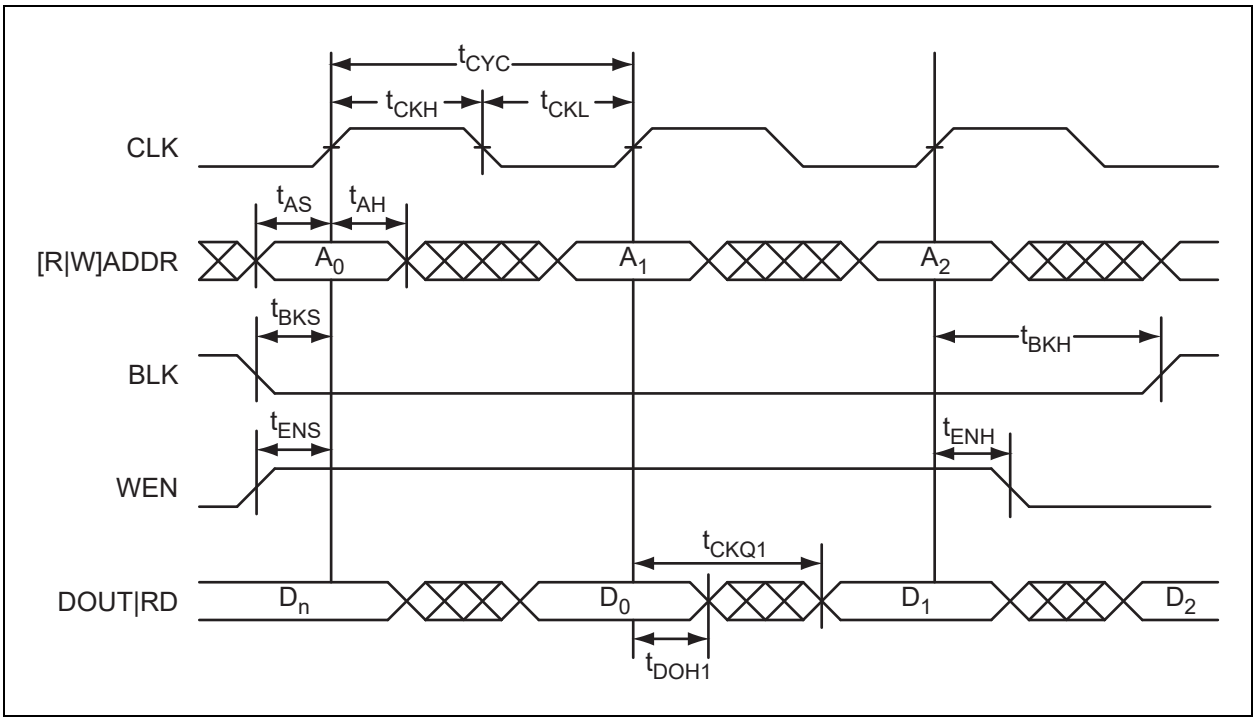
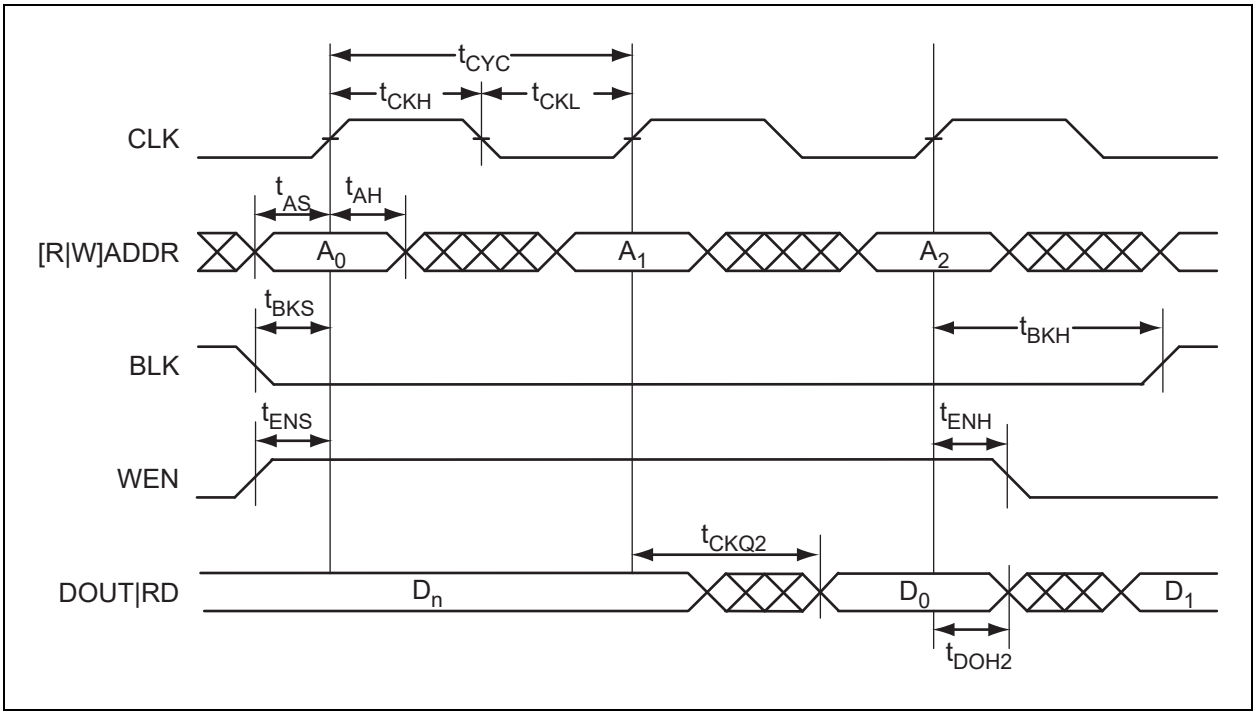



**FIGURE 2-25: RAM READ FOR PIPELINED OUTPUT. APPLICABLE TO BOTH RAM4K9 AND RAM512X18.**





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**FIGURE 2-26: RAM WRITE, OUTPUT RETAINED. APPLICABLE TO BOTH RAM4K9 AND RAM512X18.**

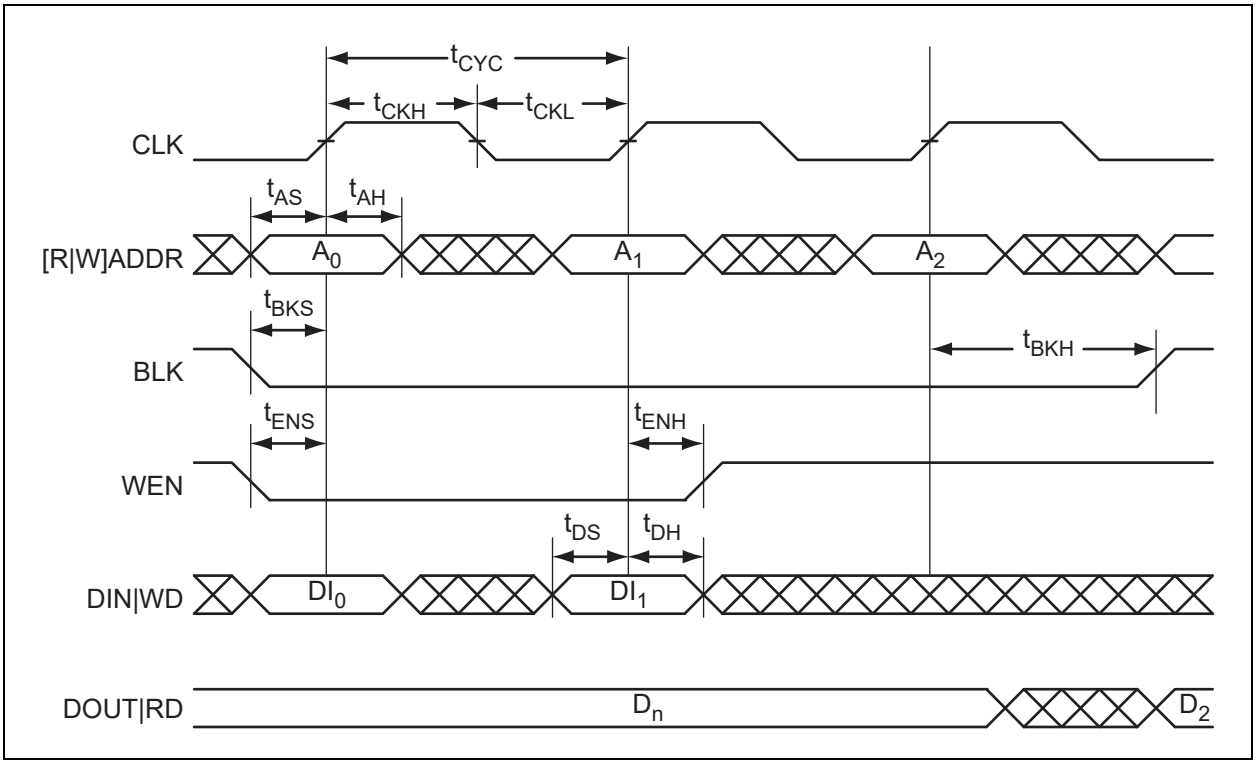


**FIGURE 2-27: RAM WRITE, OUTPUT AS WRITE DATA (WMODE = 1). APPLICABLE TO RAM4K9 ONLY.**

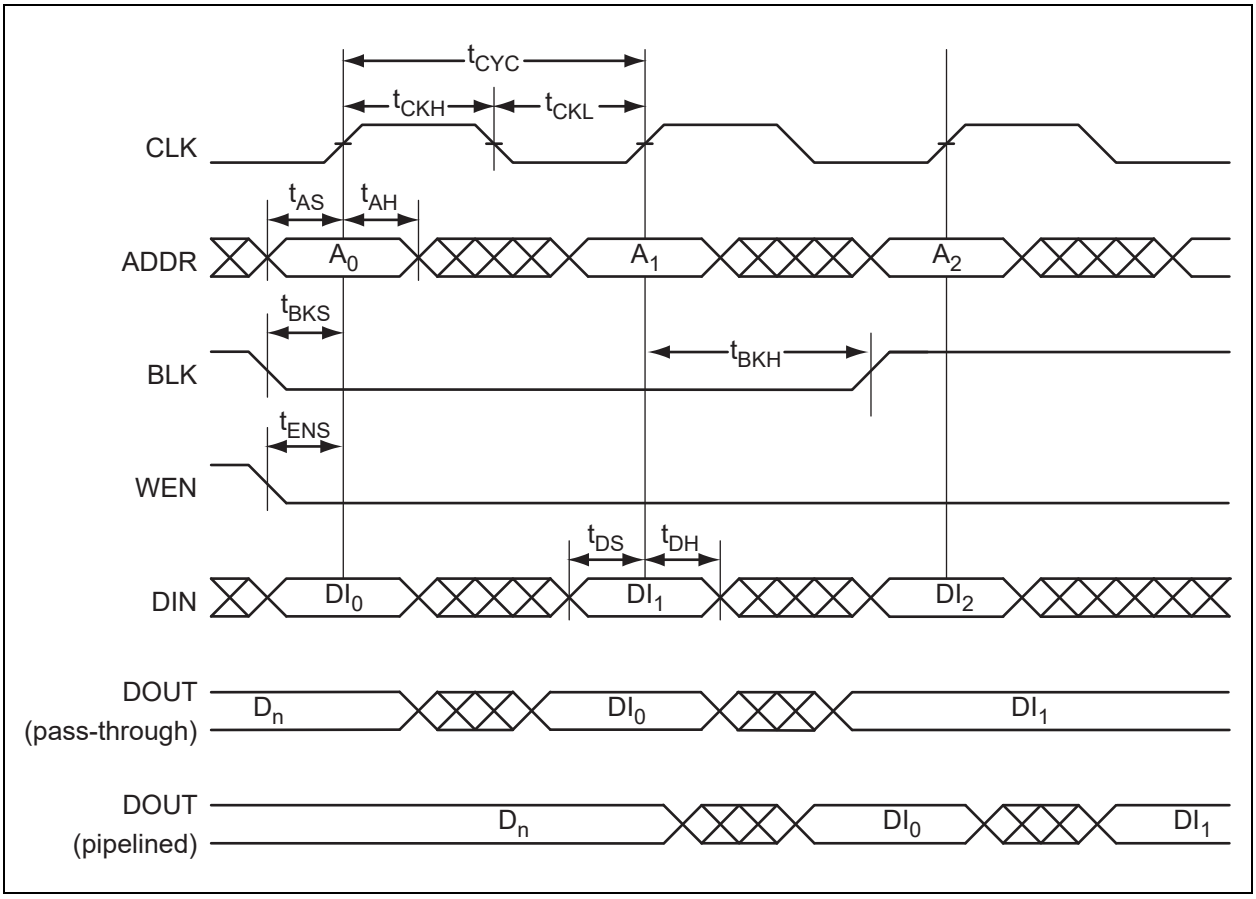
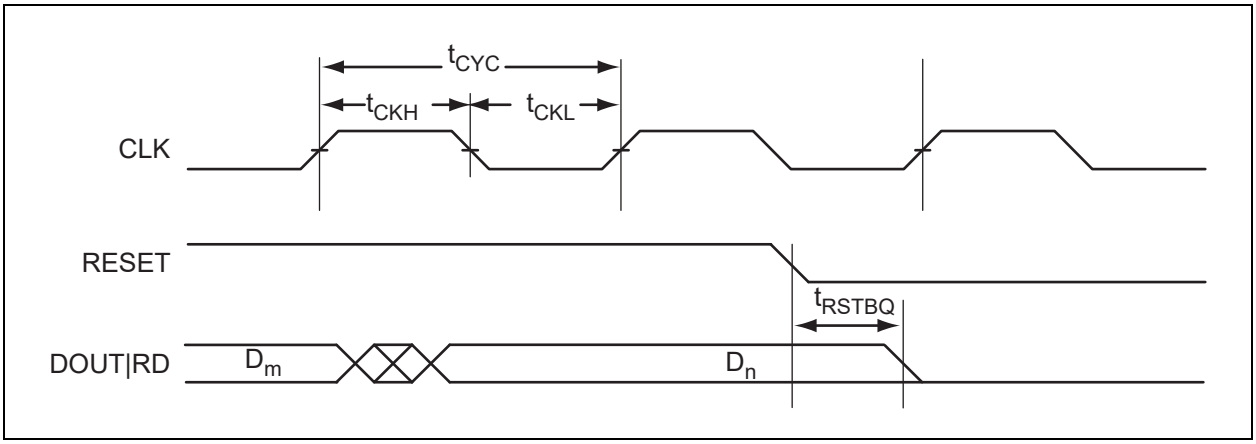



**FIGURE 2-28: RAM RESET**





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### 2.11.1.2 Timing Characteristics

#### *2.11.1.2.1 1.5V DC Core Voltage*

**TABLE 2-92: RAM4K9—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.69 | ns |
| $t_{AH}$ | Address hold time | 0.13 | ns |
| $t_{ENS}$ | REN, WEN setup time | 0.68 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.13 | ns |
| $t_{BKS}$ | BLK setup time | 1.37 | ns |
| $t_{BKH}$ | BLK hold time | 0.13 | ns |
| $t_{DS}$ | Input data (DIN) setup time | 0.59 | ns |
| $t_{DH}$ | Input data (DIN) hold time | 0.30 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on DOUT (output retained, WMODE = 0) | 2.94 | ns |
| | Clock High to new data valid on DOUT (flow-through, WMODE = 1) | 2.55 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on DOUT (pipelined) | 1.51 | ns |
| $t_{C2CWWL}$ [1] | Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge | 0.29 | ns |
| $t_{C2CRWH}$ [1] | Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge | 0.24 | ns |
| $t_{C2CWRH}$ [1] | Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge | 0.40 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on DOUT (flow-through) | 1.72 | ns |
| | RESET Low to data out Low on DOUT (pipelined) | 1.72 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.51 | ns |
| $t_{RECRSTB}$ | RESET recovery | 2.68 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.68 | ns |
| $t_{CYC}$ | Clock cycle time | 6.24 | ns |
| $F_{MAX}$ | Maximum frequency | 160 | MHz |

**Note 1:** For more information, refer to the application note *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.

**2:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**TABLE 2-93: RAM512X18—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.69 | ns |
| $t_{AH}$ | Address hold time | 0.13 | ns |
| $t_{ENS}$ | REN, WEN setup time | 0.61 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.07 | ns |
| $t_{DS}$ | Input data (WD) setup time | 0.59 | ns |
| $t_{DH}$ | Input data (WD) hold time | 0.30 | ns |

**Note 1:** For more information, refer to the application note *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.

**2:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**TABLE 2-93: RAM512X18—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{CKQ1}$ | Clock High to new data valid on RD (output retained) | 3.51 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on RD (pipelined) | 1.43 | ns |
| $t_{C2CRWH}$[1] | Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge | 0.21 | ns |
| $t_{C2CWRH}$[1] | Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge | 0.25 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on RD (flow-through) | 1.72 | ns |
| | RESET Low to data out Low on RD (pipelined) | 1.72 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.51 | ns |
| $t_{RECRSTB}$ | RESET recovery | 2.68 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.68 | ns |
| $t_{CYC}$ | Clock cycle time | 6.24 | ns |
| $F_{MAX}$ | Maximum frequency | 160 | MHz |

**Note 1:** For more information, refer to the application note *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.

**2:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

*2.11.1.2.2 1.2V DC Core Voltage*

**TABLE 2-94: RAM4K9—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{AS}$ | Address setup time | 1.28 | ns |
| $t_{AH}$ | Address hold time | 0.25 | ns |
| $t_{ENS}$ | REN, WEN setup time | 1.25 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.25 | ns |
| $t_{BKS}$ | BLK setup time | 2.54 | ns |
| $t_{BKH}$ | BLK hold time | 0.25 | ns |
| $t_{DS}$ | Input data (DIN) setup time | 1.10 | ns |
| $t_{DH}$ | Input data (DIN) hold time | 0.55 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on DOUT (output retained, WMODE = 0) | 5.51 | ns |
| | Clock High to new data valid on DOUT (flow-through, WMODE = 1) | 4.77 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on DOUT (pipelined) | 2.82 | ns |
| $t_{C2CWWL}$[1] | Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge | 0.30 | ns |
| $t_{C2CRWH}$[1] | Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge | 0.32 | ns |
| $t_{C2CWRH}$[1] | Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge | 0.44 | ns |

**Note 1:** For more information, refer to the application note *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.

**2:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.


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**TABLE 2-94: RAM4K9—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{RSTBQ}$ | RESET Low to data out Low on DOUT (flow-through) | 3.21 | ns |
| | RESET Low to data out Low on DOUT (pipelined) | 3.21 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.93 | ns |
| $t_{RECRSTB}$ | RESET recovery | 4.94 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 1.18 | ns |
| $t_{CYC}$ | Clock cycle time | 10.90 | ns |
| $F_{MAX}$ | Maximum frequency | 92 | MHz |

**Note 1:** For more information, refer to the application note *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.

**2:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

**TABLE 2-95: RAM512X18—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V**

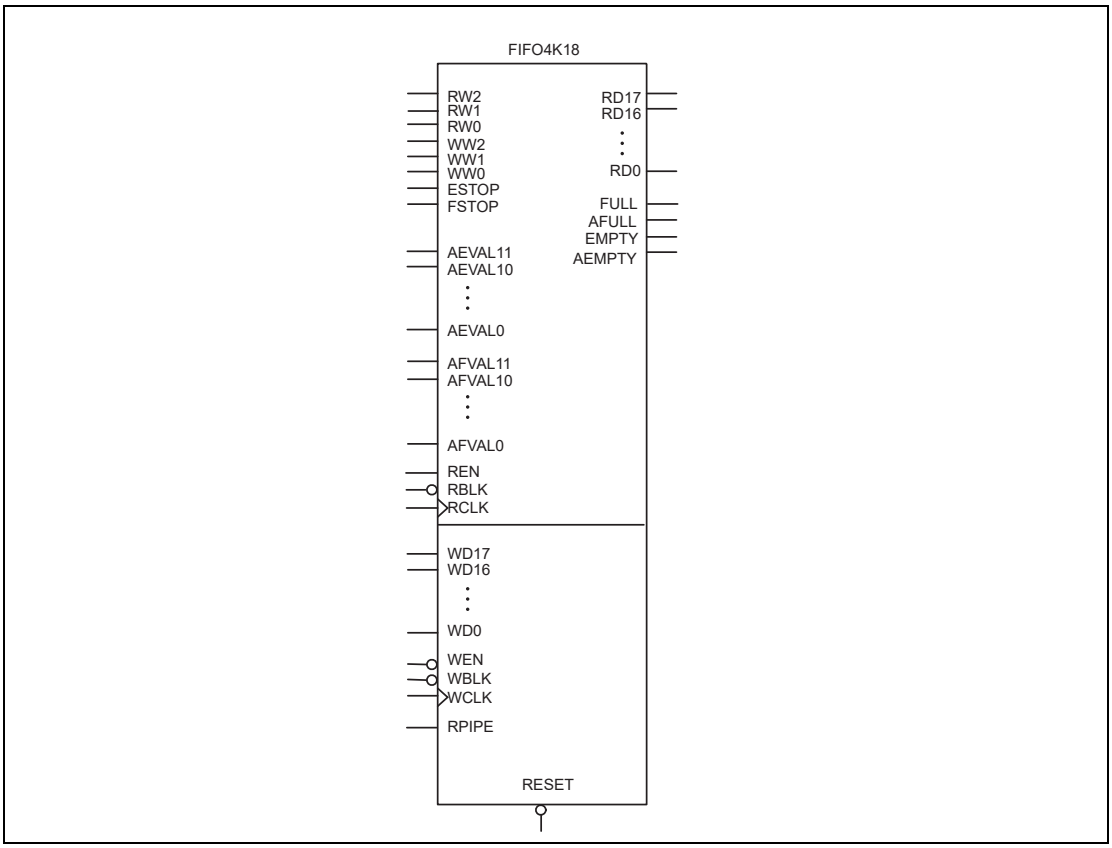
| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{AS}$ | Address setup time | 1.28 | ns |
| $t_{AH}$ | Address hold time | 0.25 | ns |
| $t_{ENS}$ | REN, WEN setup time | 1.13 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.13 | ns |
| $t_{DS}$ | Input data (WD) setup time | 1.10 | ns |
| $t_{DH}$ | Input data (WD) hold time | 0.55 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on RD (output retained) | 6.56 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on RD (pipelined) | 2.67 | ns |
| $t_{C2CRWH}$[1] | Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge | 0.29 | ns |
| $t_{C2CWRH}$[1] | Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge | 0.36 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on RD (flow through) | 3.21 | ns |
| | RESET Low to data out Low on RD (pipelined) | 3.21 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.93 | ns |
| $t_{RECRSTB}$ | RESET recovery | 4.94 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 1.18 | ns |
| $t_{CYC}$ | Clock cycle time | 10.90 | ns |
| $F_{MAX}$ | Maximum frequency | 92 | MHz |

**Note 1:** For more information, refer to the application note *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.

**2:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

### 2.11.2 FIFO

**FIGURE 2-29: FIFO MODEL**





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2.11.2.1 Timing Waveforms

**FIGURE 2-30: FIFO READ**

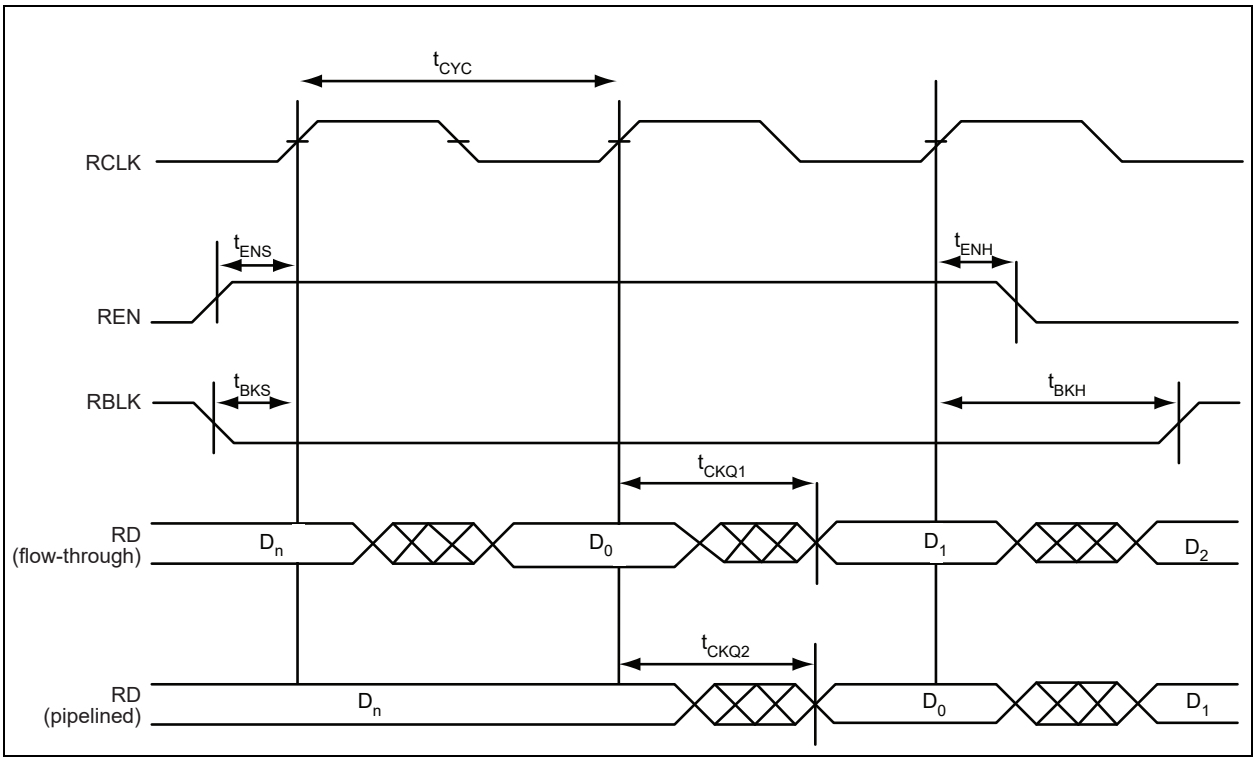



**FIGURE 2-31: FIFO WRITE**

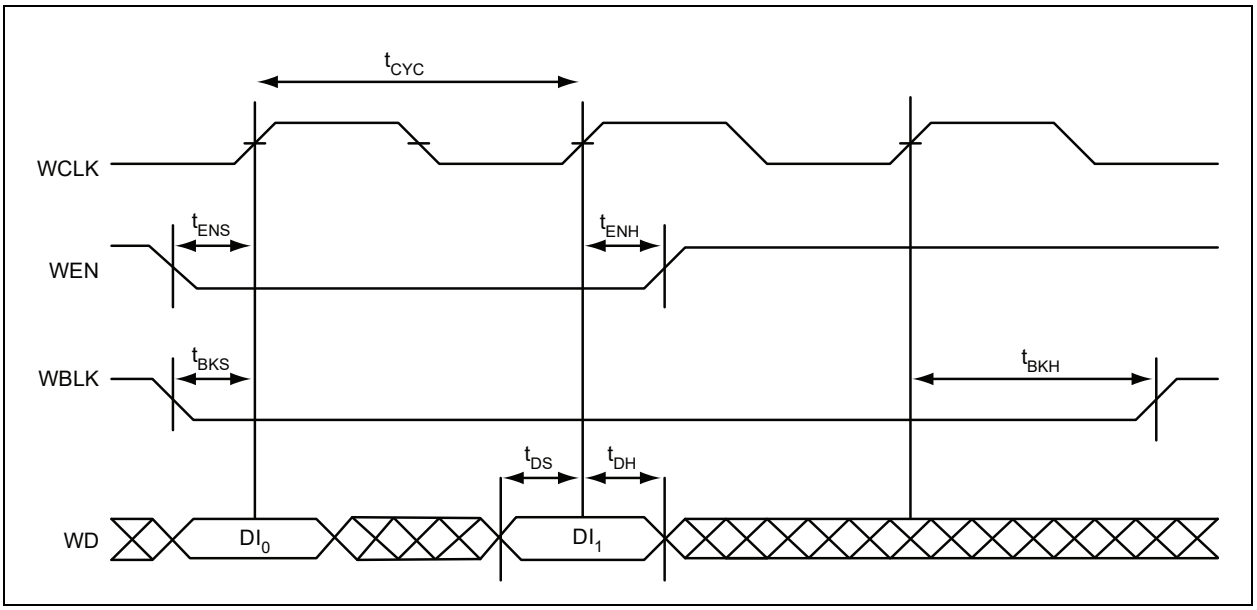


**FIGURE 2-32: FIFO RESET**

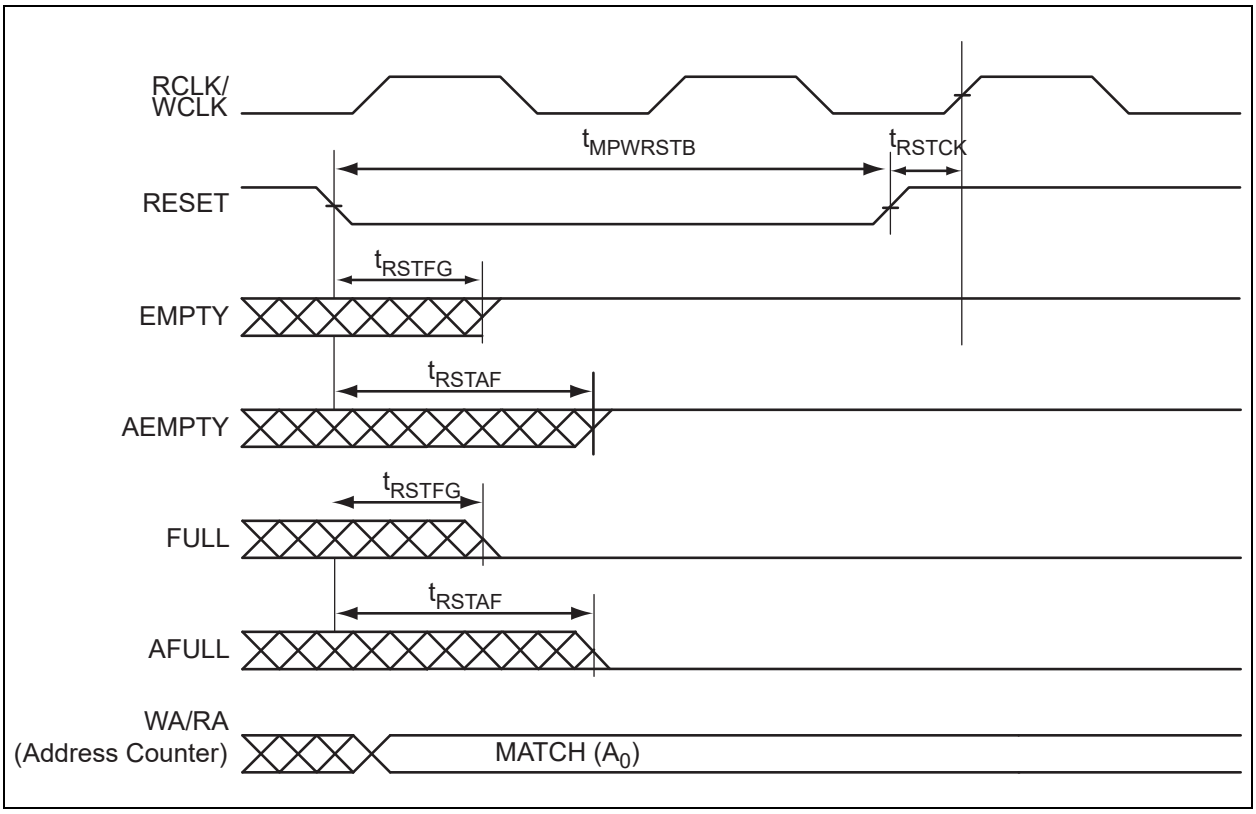
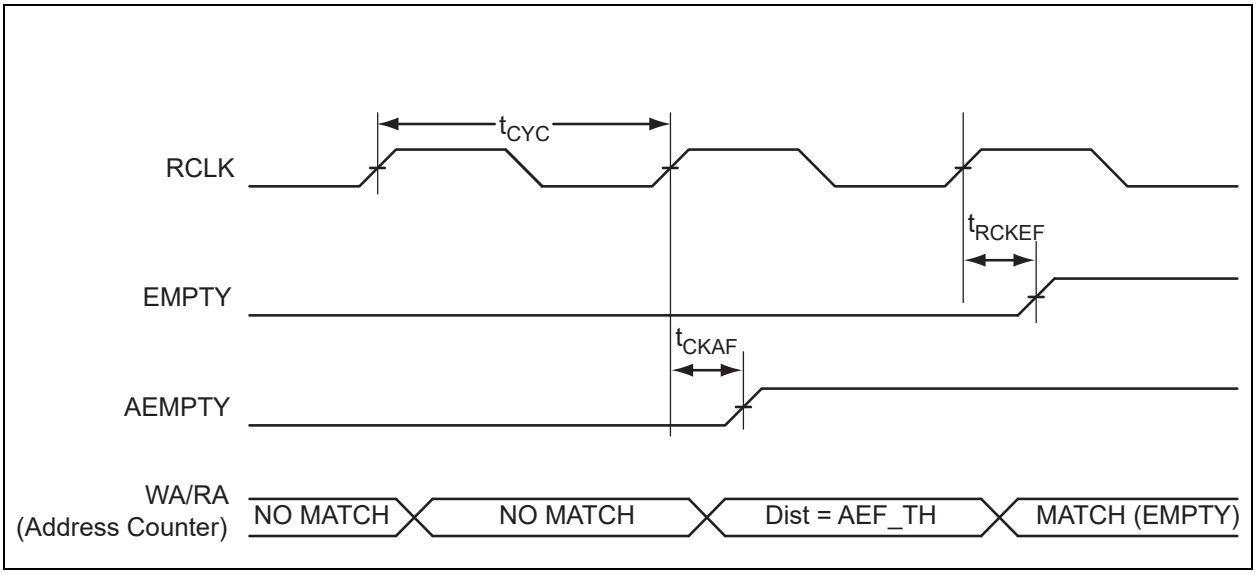



**FIGURE 2-33: FIFO EMPTY FLAG AND AEMPTY FLAG ASSERTION**





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**FIGURE 2-34: FIFO FULL FLAG AND AFULL FLAG ASSERTION**

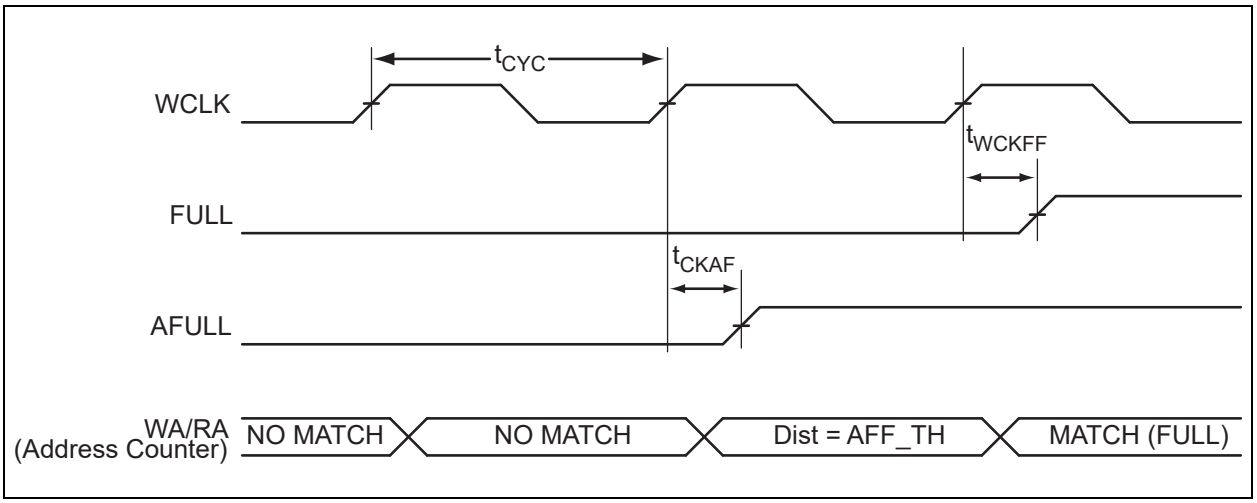



**FIGURE 2-35: FIFO EMPTY FLAG AND AEMPTY FLAG DEASSERTION**

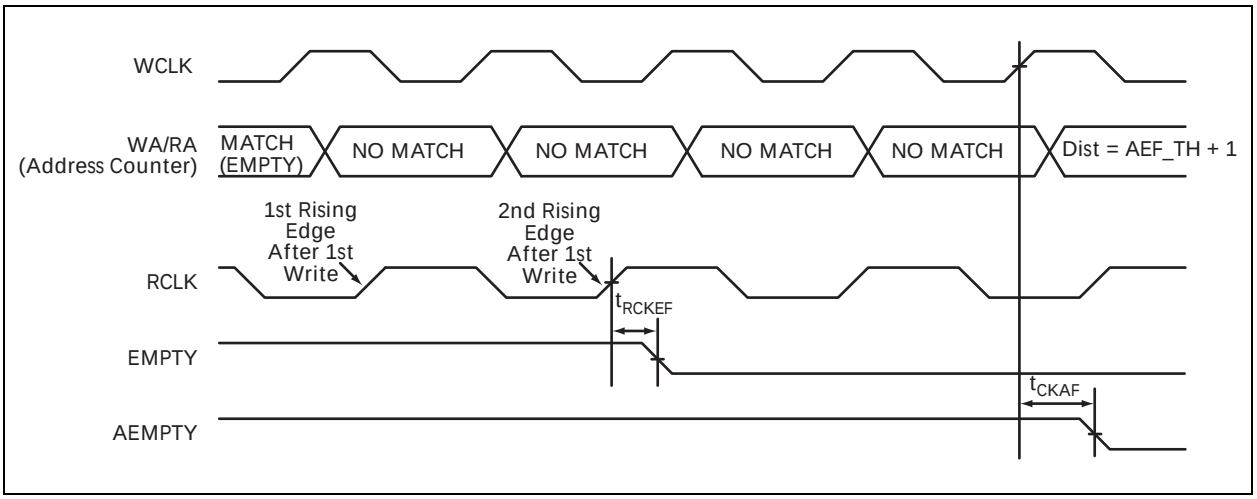
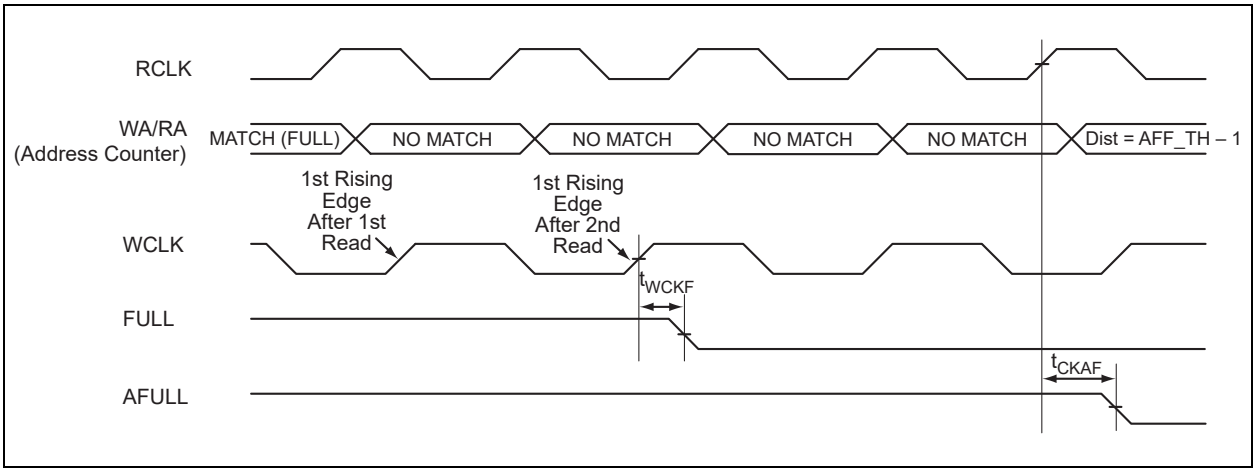



**FIGURE 2-36: FIFO FULL FLAG AND AFULL FLAG DEASSERTION**



### 2.11.2.2 Timing Characteristics

#### *2.11.2.2.1 1.5V DC Core Voltage*

**TABLE 2-96: FIFO—WORST COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, VCC = 1.425V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ENS}$ | REN, WEN Setup Time | 1.66 | ns |
| $t_{ENH}$ | REN, WEN Hold Time | 0.13 | ns |
| $t_{BKS}$ | BLK Setup Time | 0.30 | ns |
| $t_{BKH}$ | BLK Hold Time | 0.00 | ns |
| $t_{DS}$ | Input Data (WD) Setup Time | 0.63 | ns |
| $t_{DH}$ | Input Data (WD) Hold Time | 0.20 | ns |
| $t_{CKQ1}$ | Clock High to New Data Valid on RD (flow-through) | 2.77 | ns |
| $t_{CKQ2}$ | Clock High to New Data Valid on RD (pipelined) | 1.50 | ns |
| $t_{RCKEF}$ | RCLK High to Empty Flag Valid | 2.94 | ns |
| $t_{WCKFF}$ | WCLK High to Full Flag Valid | 2.79 | ns |
| $t_{CKAF}$ | Clock High to Almost Empty/Full Flag Valid | 10.71 | ns |
| $t_{RSTFG}$ | RESET Low to Empty/Full Flag Valid | 2.90 | ns |
| $t_{RSTAF}$ | RESET Low to Almost Empty/Full Flag Valid | 10.60 | ns |
| $t_{RSTBQ}$ | RESET Low to Data Out Low on RD (flow-through) | 1.68 | ns |
| | RESET Low to Data Out Low on RD (pipelined) | 1.68 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.51 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 2.68 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.68 | ns |
| $t_{CYC}$ | Clock Cycle Time | 6.24 | ns |
| $F_{MAX}$ | Maximum Frequency for FIFO | 160 | MHz |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

#### *2.11.2.2.2 1.2V DC Core Voltage*

**TABLE 2-97: FIFO—WORST COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, VCC = 1.14V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ENS}$ | REN, WEN Setup Time | 3.44 | ns |
| $t_{ENH}$ | REN, WEN Hold Time | 0.26 | ns |
| $t_{BKS}$ | BLK Setup Time | 0.30 | ns |
| $t_{BKH}$ | BLK Hold Time | 0.00 | ns |
| $t_{DS}$ | Input Data (WD) Setup Time | 1.30 | ns |
| $t_{DH}$ | Input Data (WD) Hold Time | 0.41 | ns |
| $t_{CKQ1}$ | Clock High to New Data Valid on RD (flow-through) | 5.67 | ns |
| $t_{CKQ2}$ | Clock High to New Data Valid on RD (pipelined) | 3.02 | ns |
| $t_{RCKEF}$ | RCLK High to Empty Flag Valid | 6.02 | ns |
| $t_{WCKFF}$ | WCLK High to Full Flag Valid | 5.71 | ns |
| $t_{CKAF}$ | Clock High to Almost Empty/Full Flag Valid | 22.17 | ns |
| $t_{RSTFG}$ | RESET Low to Empty/Full Flag Valid | 5.93 | ns |
| $t_{RSTAF}$ | RESET Low to Almost Empty/Full Flag Valid | 21.94 | ns |
| $t_{RSTBQ}$ | RESET Low to Data Out Low on RD (flow-through) | 3.41 | ns |
| | RESET Low to Data Out Low on RD (pipelined) | 3.41 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.


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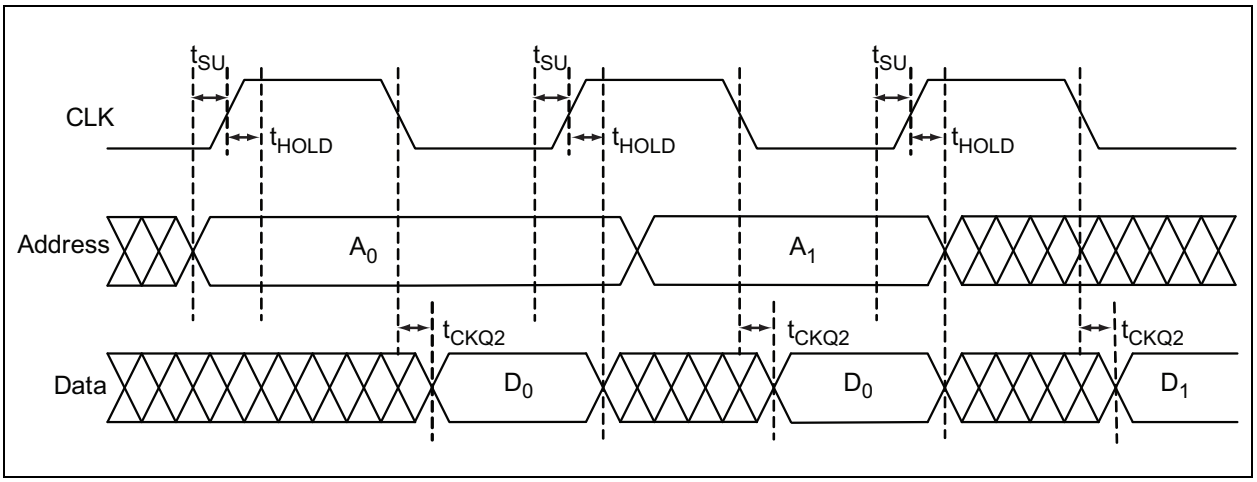
**TABLE 2-97: FIFO—WORST COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, VCC = 1.14V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{REMRSTB}$ | RESET Removal | 1.02 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 5.48 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 1.18 | ns |
| $t_{CYC}$ | Clock Cycle Time | 10.90 | ns |
| $F_{MAX}$ | Maximum Frequency for FIFO | 92 | MHz |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

## 2.11.3 EMBEDDED FLASHROM CHARACTERISTICS

**FIGURE 2-37: TIMING DIAGRAM**




### 2.11.3.1 Timing Characteristics

#### *2.11.3.1.1 1.5V DC Core Voltage*

**TABLE 2-98: EMBEDDED FLASHROM ACCESS TIME—WORST COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, VCC = 1.425V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{SU}$ | Address Setup Time | 0.57 | ns |
| $t_{HOLD}$ | Address Hold Time | 0.00 | ns |
| $t_{CK2Q}$ | Clock to Out | 17.58 | ns |
| $F_{MAX}$ | Maximum Clock Frequency | 15 | MHz |

#### *2.11.3.1.2 1.2V DC Core Voltage*

**TABLE 2-99: EMBEDDED FLASHROM ACCESS TIME—WORST COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, VCC = 1.14V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{SU}$ | Address Setup Time | 0.59 | ns |
| $t_{HOLD}$ | Address Hold Time | 0.00 | ns |
| $t_{CK2Q}$ | Clock to Out | 30.94 | ns |
| $F_{MAX}$ | Maximum Clock Frequency | 10 | MHz |

## 2.12 JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the Section 2.7, User I/O Characteristics for more details.

### 2.12.1 TIMING CHARACTERISTICS

#### 2.12.1.1 1.5V DC Core Voltage

**TABLE 2-100: JTAG 1532—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.425V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DISU}$ | Test Data Input Setup Time | 1.00 | ns |
| $t_{DIHD}$ | Test Data Input Hold Time | 2.00 | ns |
| $t_{TMSSU}$ | Test Mode Select Setup Time | 1.00 | ns |
| $t_{TMDHD}$ | Test Mode Select Hold Time | 2.00 | ns |
| $t_{TCK2Q}$ | Clock to Q (data out) | 8.00 | ns |
| $t_{RSTB2Q}$ | Reset to Q (data out) | 25.00 | ns |
| $F_{TCKMAX}$ | TCK Maximum Frequency | 15 | MHz |
| $t_{TRSTREM}$ | ResetB Removal Time | 0.58 | ns |
| $t_{TRSTREC}$ | ResetB Recovery Time | 0.00 | ns |
| $t_{TRSTMPW}$ | ResetB Minimum Pulse | TBD | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

#### 2.12.1.2 1.2V DC Core Voltage

**TABLE 2-101: JTAG 1532—COMMERCIAL-CASE CONDITIONS: $T_J$ = 70 °C, WORST-CASE VCC = 1.14V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DISU}$ | Test Data Input Setup Time | 1.50 | ns |
| $t_{DIHD}$ | Test Data Input Hold Time | 3.00 | ns |
| $t_{TMSSU}$ | Test Mode Select Setup Time | 1.50 | ns |
| $t_{TMDHD}$ | Test Mode Select Hold Time | 3.00 | ns |
| $t_{TCK2Q}$ | Clock to Q (data out) | 11.00 | ns |
| $t_{RSTB2Q}$ | Reset to Q (data out) | 30.00 | ns |
| $F_{TCKMAX}$ | TCK Maximum Frequency | 9.00 | MHz |
| $t_{TRSTREM}$ | ResetB Removal Time | 1.18 | ns |
| $t_{TRSTREC}$ | ResetB Recovery Time | 0.00 | ns |
| $t_{TRSTMPW}$ | ResetB Minimum Pulse | TBD | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.


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# 3.0 PIN DESCRIPTIONS AND PACKAGING

## 3.1 Supply Pins

### 3.1.1 GND - GROUND

Ground supply voltage to the core, I/O outputs, and I/O logic.

### 3.1.2 GNDQ - GROUND (QUIET)

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

### 3.1.3 VCC - CORE SUPPLY VOLTAGE

Supply voltage to the FPGA core, nominally 1.5V for IGLOO PLUS V5 devices, and 1.2V or 1.5V for IGLOO PLUS V2 devices. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

For IGLOO PLUS V2 devices, VCC can be switched dynamically from 1.2V to 1.5V or vice versa. This allows in-system programming (ISP) when VCC is at 1.5V and the benefit of low power operation when VCC is at 1.2V.

### 3.1.4 VCCIBX - I/O SUPPLY VOLTAGE

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are four I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

### 3.1.5 VMVX - I/O SUPPLY VOLTAGE (QUIET)

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (that is, VMV0 to VCCIB0, VMV1 to VCCIB1, and so on).

### 3.1.6 VCCPLA/B/C/D/E/F - PLL SUPPLY VOLTAGE

Supply voltage to analog PLL, nominally 1.5V or 1.2V, depending on the device.

- 1.5 V for IGLOO PLUS V5 devices
- 1.2 V or 1.5 V for IGLOO PLUS V2 devices

When the PLLs are not used, the Microchip Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microchip recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed signal FPGAs " chapter of the *IGLOO PLUS FPGA Fabric User's Guide* for a complete board solution for the PLL analog power supply and ground.

There is one VCCPLF pin on IGLOO PLUS devices.

### 3.1.7 VCOMPLA/B/C/D/E/F - PLL GROUND

Ground to analog PLL power supplies. When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on IGLOO PLUS devices.

### 3.1.8 VJTAG - JTAG SUPPLY VOLTAGE

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microchip recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

### 3.1.9 VPUMPP - ROGRAMMING SUPPLY VOLTAGE

IGLOO PLUS devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microchip recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

## 3.2 User Pins

### 3.2.1 I/O - USER INPUT/OUTPUT

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

### 3.2.2 GL - GLOBALS

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOO PLUS FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the I/O Structure chapter of the *IGLOO PLUS FPGA Fabric User's Guide* for an explanation of the naming of global pins.

### 3.2.3 FF - FLASH*FREEZE MODE ACTIVATION PIN

The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O.


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When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

The following table shows the Flash*Freeze pin location on the available packages for IGLOO and ProASIC3L devices. The Flash*Freeze pin location is independent of device (except for a PQ208 package), allowing migration to larger or smaller IGLOO devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOO PLUS Device Family User's Guide* for more information on I/O states during Flash*Freeze mode.

**TABLE 3-1: FLASH*FREEZE PIN LOCATION IN IGLOO® PLUS DEVICES**

| Package | Flash*Freeze Pin |
|---|---|
| CS281 | W2 |
| CS201 | R4 |
| CS289 | U1 |
| VQ128 | 34 |
| VQ176 | 47 |

## 3.3 JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

### 3.3.1 TCK - TEST CLOCK

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microchip recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

**Note:** To operate at all VJTAG voltages, 500Ω to 1 kΩ will satisfy the requirements. Refer to the following table for more information.

**TABLE 3-2: RECOMMENDED TIE-OFF VALUES FOR THE TCK AND TRST PINS**

| VJTAG | Tie-Off Resistance |
|---|---|
| VJTAG at 3.3V | 200Ω to 1 kΩ |
| VJTAG at 2.5V | 200Ω to 1 kΩ |
| VJTAG at 1.8V | 500Ω to 1 kΩ |
| VJTAG at 1.5V | 500Ω to 1 kΩ |

**Note 1:** Equivalent parallel resistance if more than one device is on the JTAG chain

**2:** The TCK pin can be pulled up/down.

**3:** The TRST pin is pulled down.

### 3.3.2 TDI - TEST DATA INPUT

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

### 3.3.3 TDO - TEST DATA OUTPUT

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

### 3.3.4 TMS - TEST MODE SELECT

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

### 3.3.5 TRST - BOUNDARY SCAN RESET PIN

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-2 and must satisfy the parallel resistance value requirement. The values in Table 3-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microchip recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500Ω to 1 kΩ will satisfy the requirements.

## 3.4 Special Function Pins

### 3.4.1 NC - NO CONNECT

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

### 3.4.2 DC - DO NOT CONNECT

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

## 3.5 Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microchip consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microchip IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Microchip offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

## 3.6 Related Documents

*IGLOO PLUS Device Family User's Guide*

http://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/ProductDocuments/UserGuides/iglooplus_ug.pdf

The following documents provide packaging information and device selection for low power flash devices.

## 3.7 Product Catalog

https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/ProductDocuments/Brochures/igloo_low-power_flash_fpgas_brochure.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

## 3.8 Package Mechanical Drawings

https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/ProductDocuments/PackagingSpecifications/PD3068-Package_Mechanical_Drawings_Datasheet_V62.pdf

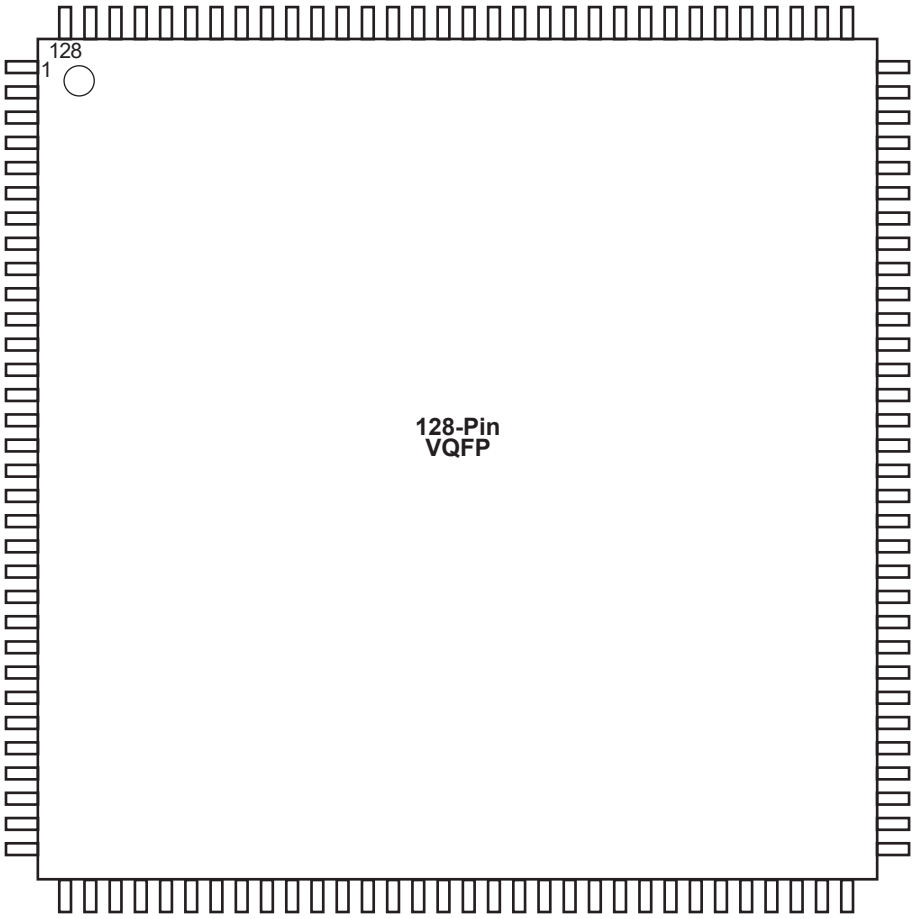

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This document contains the package mechanical drawings for all packages currently or previously supplied by Microchip. Use the bookmarks to navigate to the package mechanical drawings.

# 4.0 PACKAGE PIN ASSIGNMENTS

## 4.1 VQ128

**FIGURE 4-1:**




**Note:** This is the top view of the package.

**Note:** For Package Manufacturing and Environmental information, visit the Resource Center at https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/fpga/libero-software-later-versions. Pin information is in the "Pin Descriptions" chapter of the *IGLOO PLUS FPGA Fabric User's Guide*.


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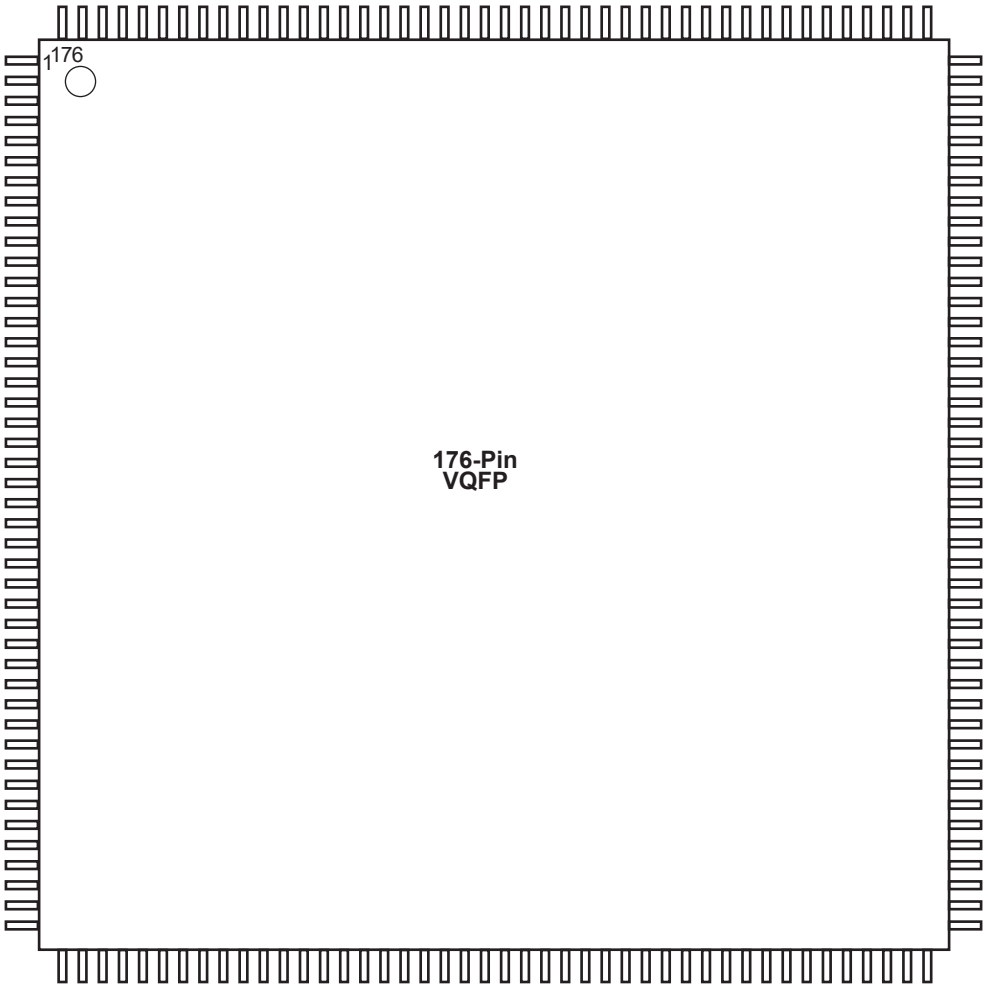
| TABLE 4-1: VQ128 | |
|---|---|
| Pin Number | AGLP030 Function |
| 1 | IO119RSB3 |
| 2 | IO118RSB3 |
| 3 | IO117RSB3 |
| 4 | IO115RSB3 |
| 5 | IO116RSB3 |
| 6 | IO113RSB3 |
| 7 | IO114RSB3 |
| 8 | GND |
| 9 | VCCIB3 |
| 10 | IO112RSB3 |
| 11 | IO111RSB3 |
| 12 | IO110RSB3 |
| 13 | IO109RSB3 |
| 14 | GEC0/IO108RSB3 |
| 15 | GEA0/IO107RSB3 |
| 16 | GEB0/IO106RSB3 |
| 17 | VCC |
| 18 | IO104RSB3 |
| 19 | IO103RSB3 |
| 20 | IO102RSB3 |
| 21 | IO101RSB3 |
| 22 | IO100RSB3 |
| 23 | IO99RSB3 |
| 24 | GND |
| 25 | VCCIB3 |
| 26 | IO97RSB3 |
| 27 | IO98RSB3 |
| 28 | IO95RSB3 |
| 29 | IO96RSB3 |
| 30 | IO94RSB3 |
| 31 | IO93RSB3 |
| 32 | IO92RSB3 |
| 33 | IO91RSB2 |
| 34 | FF/IO90RSB2 |
| 35 | IO89RSB2 |
| 36 | IO88RSB2 |
| 37 | IO86RSB2 |
| 38 | IO84RSB2 |
| 39 | IO83RSB2 |
| 40 | GND |
| 41 | VCCIB2 |
| 42 | IO82RSB2 |
| 43 | IO81RSB2 |

| TABLE 4-1: VQ128 | |
|---|---|
| Pin Number | AGLP030 Function |
| 44 | IO79RSB2 |
| 45 | IO78RSB2 |
| 46 | IO77RSB2 |
| 47 | IO75RSB2 |
| 48 | IO74RSB2 |
| 49 | VCC |
| 50 | IO73RSB2 |
| 51 | IO72RSB2 |
| 52 | IO70RSB2 |
| 53 | IO69RSB2 |
| 54 | IO68RSB2 |
| 55 | IO66RSB2 |
| 56 | IO65RSB2 |
| 57 | GND |
| 58 | VCCIB2 |
| 59 | IO63RSB2 |
| 60 | IO61RSB2 |
| 61 | IO59RSB2 |
| 62 | TCK |
| 63 | TDI |
| 64 | TMS |
| 65 | VPUMP |
| 66 | TDO |
| 67 | TRST |
| 68 | IO58RSB1 |
| 69 | VJTAG |
| 70 | IO56RSB1 |
| 71 | IO57RSB1 |
| 72 | VCCIB1 |
| 73 | GND |
| 74 | IO55RSB1 |
| 75 | IO54RSB1 |
| 76 | IO53RSB1 |
| 77 | IO52RSB1 |
| 78 | IO51RSB1 |
| 79 | IO50RSB1 |
| 80 | IO49RSB1 |
| 81 | VCC |
| 82 | GDB0/IO48RSB1 |
| 83 | GDA0/IO47RSB1 |
| 84 | GDC0/IO46RSB1 |
| 85 | IO45RSB1 |
| 86 | IO44RSB1 |

| TABLE 4-1: VQ128 | |
|---|---|
| Pin Number | AGLP030 Function |
| 87 | IO43RSB1 |
| 88 | IO42RSB1 |
| 89 | VCCIB1 |
| 90 | GND |
| 91 | IO40RSB1 |
| 92 | IO41RSB1 |
| 93 | IO39RSB1 |
| 94 | IO38RSB1 |
| 95 | IO37RSB1 |
| 96 | IO36RSB1 |
| 97 | IO35RSB0 |
| 98 | IO34RSB0 |
| 99 | IO33RSB0 |
| 100 | IO32RSB0 |
| 101 | IO30RSB0 |
| 102 | IO28RSB0 |
| 103 | IO27RSB0 |
| 104 | VCCIB0 |
| 105 | GND |
| 106 | IO26RSB0 |
| 107 | IO25RSB0 |
| 108 | IO23RSB0 |
| 109 | IO22RSB0 |
| 110 | IO21RSB0 |
| 111 | IO19RSB0 |
| 112 | IO18RSB0 |
| 113 | VCC |
| 114 | IO17RSB0 |
| 115 | IO16RSB0 |
| 116 | IO14RSB0 |
| 117 | IO13RSB0 |
| 118 | IO12RSB0 |
| 119 | IO10RSB0 |
| 120 | IO09RSB0 |
| 121 | VCCIB0 |
| 122 | GND |
| 123 | IO07RSB0 |
| 124 | IO05RSB0 |
| 125 | IO03RSB0 |
| 126 | IO02RSB0 |
| 127 | IO01RSB0 |
| 128 | IO00RSB0 |

## 4.2 VQ176

**FIGURE 4-2:**




**Note:** This is the bottom view of the package.

**Note:** For Package Manufacturing and Environmental information, visit the Resource Center at https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/fpga/libero-software-later-versions.


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| TABLE 4-2: VQ176 | |
|---|---|
| Pin Number | AGLP060 Function |
| 1 | GAA2/IO156RSB3 |
| 2 | IO155RSB3 |
| 3 | GAB2/IO154RSB3 |
| 4 | IO153RSB3 |
| 5 | GAC2/IO152RSB3 |
| 6 | GND |
| 7 | VCCIB3 |
| 8 | IO149RSB3 |
| 9 | IO147RSB3 |
| 10 | IO145RSB3 |
| 11 | IO144RSB3 |
| 12 | IO143RSB3 |
| 13 | VCC |
| 14 | IO141RSB3 |
| 15 | GFC1/IO140RSB3 |
| 16 | GFB1/IO138RSB3 |
| 17 | GFB0/IO137RSB3 |
| 18 | VCOMPLF |
| 19 | GFA1/IO136RSB3 |
| 20 | VCCPLF |
| 21 | GFA0/IO135RSB3 |
| 22 | GND |
| 23 | VCCIB3 |
| 24 | GFA2/IO134RSB3 |
| 25 | GFB2/IO133RSB3 |
| 26 | GFC2/IO132RSB3 |
| 27 | IO131RSB3 |
| 28 | IO130RSB3 |
| 29 | IO129RSB3 |
| 30 | IO127RSB3 |
| 31 | IO126RSB3 |
| 32 | IO125RSB3 |
| 33 | IO123RSB3 |
| 34 | IO122RSB3 |
| 35 | IO121RSB3 |
| 36 | IO119RSB3 |
| 37 | GND |
| 38 | VCCIB3 |
| 39 | GEC1/IO116RSB3 |
| 40 | GEB1/IO114RSB3 |
| 41 | GEC0/IO115RSB3 |
| 42 | GEB0/IO113RSB3 |
| 43 | GEA1/IO112RSB3 |

| TABLE 4-2: VQ176 | |
|---|---|
| Pin Number | AGLP060 Function |
| 44 | GEA0/IO111RSB3 |
| 45 | GEA2/IO110RSB2 |
| 46 | NC |
| 47 | FF/GEB2/ IO109RSB2 |
| 48 | GEC2/IO108RSB2 |
| 49 | IO106RSB2 |
| 50 | IO107RSB2 |
| 51 | IO104RSB2 |
| 52 | IO105RSB2 |
| 53 | IO102RSB2 |
| 54 | IO103RSB2 |
| 55 | GND |
| 56 | VCCIB2 |
| 57 | IO101RSB2 |
| 58 | IO100RSB2 |
| 59 | IO99RSB2 |
| 60 | IO98RSB2 |
| 61 | IO97RSB2 |
| 62 | IO96RSB2 |
| 63 | IO95RSB2 |
| 64 | IO94RSB2 |
| 65 | IO93RSB2 |
| 66 | VCC |
| 67 | IO92RSB2 |
| 68 | IO91RSB2 |
| 69 | IO90RSB2 |
| 70 | IO89RSB2 |
| 71 | IO88RSB2 |
| 72 | IO87RSB2 |
| 73 | IO86RSB2 |
| 74 | IO85RSB2 |
| 75 | IO84RSB2 |
| 76 | GND |
| 77 | VCCIB2 |
| 78 | IO83RSB2 |
| 79 | IO82RSB2 |
| 80 | GDC2/IO80RSB2 |
| 81 | IO81RSB2 |
| 82 | GDA2/IO78RSB2 |
| 83 | GDB2/IO79RSB2 |
| 84 | NC |
| 85 | NC |
| 86 | TCK |

| TABLE 4-2: VQ176 | |
|---|---|
| Pin Number | AGLP060 Function |
| 87 | TDI |
| 88 | TMS |
| 89 | VPUMP |
| 90 | TDO |
| 91 | TRST |
| 92 | VJTAG |
| 93 | GDA1/IO76RSB1 |
| 94 | GDC0/IO73RSB1 |
| 95 | GDB1/IO74RSB1 |
| 96 | GDC1/IO72RSB1 |
| 97 | VCCIB1 |
| 98 | GND |
| 99 | IO70RSB1 |
| 100 | IO69RSB1 |
| 101 | IO67RSB1 |
| 102 | IO66RSB1 |
| 103 | IO65RSB1 |
| 104 | IO63RSB1 |
| 105 | IO62RSB1 |
| 106 | IO61RSB1 |
| 107 | GCC2/IO60RSB1 |
| 108 | GCB2/IO59RSB1 |
| 109 | GCA2/IO58RSB1 |
| 110 | GCA0/IO57RSB1 |
| 111 | GCA1/IO56RSB1 |
| 112 | VCCIB1 |
| 113 | GND |
| 114 | GCB0/IO55RSB1 |
| 115 | GCB1/IO54RSB1 |
| 116 | GCC0/IO53RSB1 |
| 117 | GCC1/IO52RSB1 |
| 118 | IO51RSB1 |
| 119 | IO50RSB1 |
| 120 | VCC |
| 121 | IO48RSB1 |
| 122 | IO47RSB1 |
| 123 | IO45RSB1 |
| 124 | IO44RSB1 |
| 125 | IO43RSB1 |
| 126 | VCCIB1 |
| 127 | GND |
| 128 | GBC2/IO40RSB1 |
| 129 | IO39RSB1 |

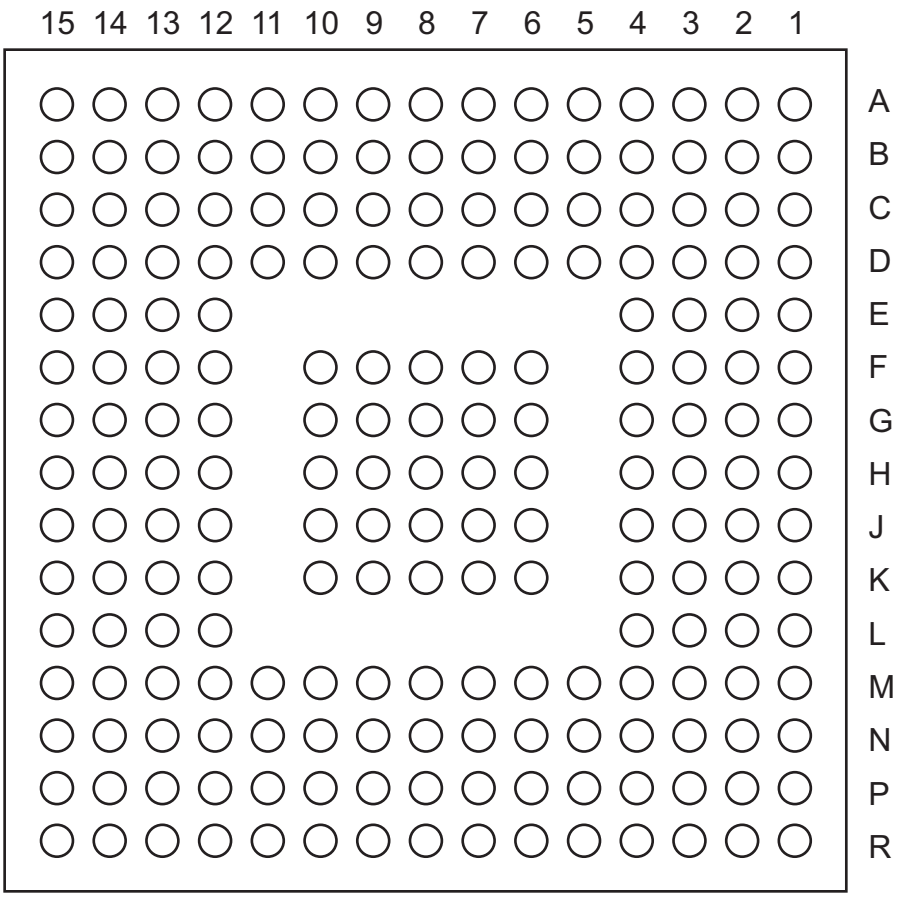
| TABLE 4-2: VQ176 | |
|---|---|
| Pin Number | AGLP060 Function |
| 130 | GBB2/IO38RSB1 |
| 131 | IO37RSB1 |
| 132 | GBA2/IO36RSB1 |
| 133 | GBA1/IO35RSB0 |
| 134 | NC |
| 135 | GBA0/IO34RSB0 |
| 136 | NC |
| 137 | GBB1/IO33RSB0 |
| 138 | NC |
| 139 | GBC1/IO31RSB0 |
| 140 | GBB0/IO32RSB0 |
| 141 | GBC0/IO30RSB0 |
| 142 | IO29RSB0 |
| 143 | IO28RSB0 |
| 144 | IO27RSB0 |
| 145 | VCCIB0 |
| 146 | GND |
| 147 | IO26RSB0 |
| 148 | IO25RSB0 |
| 149 | IO24RSB0 |
| 150 | IO23RSB0 |
| 151 | IO22RSB0 |
| 152 | IO21RSB0 |
| 153 | IO20RSB0 |
| 154 | IO19RSB0 |
| 155 | IO18RSB0 |
| 156 | VCC |
| 157 | IO17RSB0 |
| 158 | IO16RSB0 |
| 159 | IO15RSB0 |
| 160 | IO14RSB0 |
| 161 | IO13RSB0 |
| 162 | IO12RSB0 |
| 163 | IO11RSB0 |
| 164 | IO10RSB0 |
| 165 | IO09RSB0 |
| 166 | VCCIB0 |
| 167 | GND |
| 168 | IO07RSB0 |
| 169 | IO08RSB0 |
| 170 | GAC1/IO05RSB0 |
| 171 | IO06RSB0 |
| 172 | GAB1/IO03RSB0 |

| TABLE 4-2: VQ176 | |
|---|---|
| Pin Number | AGLP060 Function |
| 173 | GAC0/IO04RSB0 |
| 174 | GAB0/IO02RSB0 |
| 175 | GAA1/IO01RSB0 |
| 176 | GAA0/IO00RSB0 |


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## 4.3 CS201

**FIGURE 4-3:**




**Note:** This is the bottom view of the package.

**Note:** For Package Manufacturing and Environmental information, visit the Resource Center at https://www.microchip.com/en-us/products/fpgas-and-plds/packaging.

| TABLE 4-3: CS201 | |
|---|---|
| Pin Number | AGLP030 Function |
| A1 | NC |
| A2 | IO04RSB0 |
| A3 | IO06RSB0 |
| A4 | IO09RSB0 |
| A5 | IO11RSB0 |
| A6 | IO13RSB0 |
| A7 | IO17RSB0 |
| A8 | IO18RSB0 |
| A9 | IO24RSB0 |
| A10 | IO26RSB0 |
| A11 | IO27RSB0 |
| A12 | IO31RSB0 |
| A13 | NC |
| A14 | NC |
| A15 | NC |
| B1 | NC |
| B2 | NC |
| B3 | IO08RSB0 |
| B4 | IO05RSB0 |
| B5 | IO07RSB0 |
| B6 | IO15RSB0 |
| B7 | IO14RSB0 |
| B8 | IO16RSB0 |
| B9 | IO20RSB0 |
| B10 | IO22RSB0 |
| B11 | IO34RSB0 |
| B12 | IO29RSB0 |
| B13 | NC |
| B14 | NC |
| B15 | NC |
| C1 | NC |
| C2 | NC |
| C3 | GND |
| C4 | IO00RSB0 |
| C5 | IO02RSB0 |
| C6 | IO12RSB0 |
| C7 | IO23RSB0 |
| C8 | IO19RSB0 |
| C9 | IO28RSB0 |
| C10 | IO32RSB0 |
| C11 | IO35RSB0 |
| C12 | NC |
| C13 | GND |

| TABLE 4-3: CS201 | |
|---|---|
| Pin Number | AGLP030 Function |
| C14 | IO41RSB1 |
| C15 | IO37RSB1 |
| D1 | IO117RSB3 |
| D2 | IO118RSB3 |
| D3 | NC |
| D4 | GND |
| D5 | IO01RSB0 |
| D6 | IO03RSB0 |
| D7 | IO10RSB0 |
| D8 | IO21RSB0 |
| D9 | IO25RSB0 |
| D10 | IO30RSB0 |
| D11 | IO33RSB0 |
| D12 | GND |
| D13 | NC |
| D14 | IO36RSB1 |
| D15 | IO39RSB1 |
| E1 | IO115RSB3 |
| E2 | IO114RSB3 |
| E3 | NC |
| E4 | NC |
| E12 | NC |
| E13 | NC |
| E14 | GDC0/IO46RSB1 |
| E15 | GDB0/IO48RSB1 |
| F1 | IO113RSB3 |
| F2 | IO116RSB3 |
| F3 | IO119RSB3 |
| F4 | IO111RSB3 |
| F6 | GND |
| F7 | VCC |
| F8 | VCCIB0 |
| F9 | VCCIB0 |
| F10 | VCCIB0 |
| F12 | NC |
| F13 | NC |
| F14 | IO40RSB1 |
| F15 | IO38RSB1 |
| G1 | NC |
| G2 | IO112RSB3 |
| G3 | IO110RSB3 |
| G4 | IO109RSB3 |
| G6 | VCCIB3 |

| TABLE 4-3: CS201 | |
|---|---|
| Pin Number | AGLP030 Function |
| G7 | GND |
| G8 | VCC |
| G9 | GND |
| G10 | GND |
| G12 | NC |
| G13 | NC |
| G14 | IO42RSB1 |
| G15 | IO44RSB1 |
| H1 | NC |
| H2 | GEB0/IO106RSB3 |
| H3 | GEC0/IO108RSB3 |
| H4 | NC |
| H6 | VCCIB3 |
| H7 | GND |
| H8 | VCC |
| H9 | GND |
| H10 | VCCIB1 |
| H12 | IO54RSB1 |
| H13 | GDA0/IO47RSB1 |
| H14 | IO45RSB1 |
| H15 | IO43RSB1 |
| J1 | GEA0/IO107RSB3 |
| J2 | IO105RSB3 |
| J3 | IO104RSB3 |
| J4 | IO102RSB3 |
| J6 | VCCIB3 |
| J7 | GND |
| J8 | VCC |
| J9 | GND |
| J10 | VCCIB1 |
| J12 | NC |
| J13 | NC |
| J14 | IO52RSB1 |
| J15 | IO50RSB1 |
| K1 | IO103RSB3 |
| K2 | IO101RSB3 |
| K3 | IO99RSB3 |
| K4 | IO100RSB3 |
| K6 | GND |
| K7 | VCCIB2 |
| K8 | VCCIB2 |
| K9 | VCCIB2 |
| K10 | VCCIB1 |


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| TABLE 4-3: CS201 | |
|---|---|
| Pin Number | AGLP030 Function |
| K12 | NC |
| K13 | IO57RSB1 |
| K14 | IO49RSB1 |
| K15 | IO53RSB1 |
| L1 | IO96RSB3 |
| L2 | IO98RSB3 |
| L3 | IO95RSB3 |
| L4 | IO94RSB3 |
| L12 | NC |
| L13 | NC |
| L14 | IO51RSB1 |
| L15 | IO58RSB1 |
| M1 | IO93RSB3 |
| M2 | IO92RSB3 |
| M3 | IO97RSB3 |
| M4 | GND |
| M5 | NC |
| M6 | IO79RSB2 |
| M7 | IO77RSB2 |
| M8 | IO72RSB2 |
| M9 | IO70RSB2 |
| M10 | IO61RSB2 |
| M11 | IO59RSB2 |
| M12 | GND |
| M13 | NC |
| M14 | IO55RSB1 |
| M15 | IO56RSB1 |
| N1 | NC |
| N2 | NC |
| N3 | GND |
| N4 | NC |
| N5 | IO88RSB2 |
| N6 | IO81RSB2 |
| N7 | IO75RSB2 |
| N8 | IO68RSB2 |
| N9 | IO66RSB2 |
| N10 | IO65RSB2 |
| N11 | IO71RSB2 |
| N12 | IO63RSB2 |
| N13 | GND |
| N14 | TDO |
| N15 | VJTAG |
| P1 | NC |

| TABLE 4-3: CS201 | |
|---|---|
| Pin Number | AGLP030 Function |
| P2 | NC |
| P3 | NC |
| P4 | NC |
| P5 | IO87RSB2 |
| P6 | IO86RSB2 |
| P7 | IO84RSB2 |
| P8 | IO80RSB2 |
| P9 | IO74RSB2 |
| P10 | IO73RSB2 |
| P11 | IO76RSB2 |
| P12 | IO67RSB2 |
| P13 | IO64RSB2 |
| P14 | VPUMP |
| P15 | TRST |
| R1 | NC |
| R2 | NC |
| R3 | IO91RSB2 |
| R4 | FF/IO90RSB2 |
| R5 | IO89RSB2 |
| R6 | IO83RSB2 |
| R7 | IO82RSB2 |
| R8 | IO85RSB2 |
| R9 | IO78RSB2 |
| R10 | IO69RSB2 |
| R11 | IO62RSB2 |
| R12 | IO60RSB2 |
| R13 | TMS |
| R14 | TDI |
| R15 | TCK |

| TABLE 4-4: CS201 | |
|---|---|
| Pin Number | AGLP060 Function |
| A1 | IO150RSB3 |
| A2 | GAA0/IO00RSB0 |
| A3 | GAC0/IO04RSB0 |
| A4 | IO08RSB0 |
| A5 | IO11RSB0 |
| A6 | IO15RSB0 |
| A7 | IO17RSB0 |
| A8 | IO18RSB0 |
| A9 | IO22RSB0 |
| A10 | IO26RSB0 |
| A11 | IO29RSB0 |
| A12 | GBC1/IO31RSB0 |
| A13 | GBA2/IO36RSB1 |
| A14 | IO41RSB1 |
| A15 | NC |
| B1 | IO151RSB3 |
| B2 | GAB2/IO154RSB3 |
| B3 | IO06RSB0 |
| B4 | IO09RSB0 |
| B5 | IO13RSB0 |
| B6 | IO10RSB0 |
| B7 | IO12RSB0 |
| B8 | IO20RSB0 |
| B9 | IO23RSB0 |
| B10 | IO25RSB0 |
| B11 | IO24RSB0 |
| B12 | IO27RSB0 |
| B13 | IO37RSB1 |
| B14 | IO46RSB1 |
| B15 | IO42RSB1 |
| C1 | IO155RSB3 |
| C2 | GAA2/IO156RSB3 |
| C3 | GND |
| C4 | GAA1/IO01RSB0 |
| C5 | GAB1/IO03RSB0 |
| C6 | IO07RSB0 |
| C7 | IO16RSB0 |
| C8 | IO21RSB0 |
| C9 | IO28RSB0 |
| C10 | GBB1/IO33RSB0 |
| C11 | GBA1/IO35RSB0 |
| C12 | GBB2/IO38RSB1 |
| C13 | GND |

| TABLE 4-4: CS201 | |
|---|---|
| Pin Number | AGLP060 Function |
| C14 | IO48RSB1 |
| C15 | IO39RSB1 |
| D1 | IO146RSB3 |
| D2 | IO144RSB3 |
| D3 | IO148RSB3 |
| D4 | GND |
| D5 | GAB0/IO02RSB0 |
| D6 | GAC1/IO05RSB0 |
| D7 | IO14RSB0 |
| D8 | IO19RSB0 |
| D9 | GBC0/IO30RSB0 |
| D10 | GBB0/IO32RSB0 |
| D11 | GBA0/IO34RSB0 |
| D12 | GND |
| D13 | GBC2/IO40RSB1 |
| D14 | IO51RSB1 |
| D15 | IO44RSB1 |
| E1 | IO142RSB3 |
| E2 | IO149RSB3 |
| E3 | IO153RSB3 |
| E4 | GAC2/IO152RSB3 |
| E12 | IO43RSB1 |
| E13 | IO49RSB1 |
| E14 | GCC0/IO53RSB1 |
| E15 | GCB0/IO55RSB1 |
| F1 | IO141RSB3 |
| F2 | GFC1/IO140RSB3 |
| F3 | IO145RSB3 |
| F4 | IO147RSB3 |
| F6 | GND |
| F7 | VCC |
| F8 | VCCIB0 |
| F9 | VCCIB0 |
| F10 | VCCIB0 |
| F12 | IO47RSB1 |
| F13 | IO45RSB1 |
| F14 | GCC1/IO52RSB1 |
| F15 | GCA1/IO56RSB1 |
| G1* | VCOMPLF |
| G2 | GFB0/IO137RSB3 |
| G3 | GFC0/IO139RSB3 |
| G4 | IO143RSB3 |
| G6 | VCCIB3 |

| TABLE 4-4: CS201 | |
|---|---|
| Pin Number | AGLP060 Function |
| G7 | GND |
| G8 | VCC |
| G9 | GND |
| G10 | GND |
| G12 | IO50RSB1 |
| G13 | GCB1/IO54RSB1 |
| G14 | GCC2/IO60RSB1 |
| G15 | GCA2/IO58RSB1 |
| H1* | VCCPLF |
| H2 | GFA1/IO136RSB3 |
| H3 | GFB1/IO138RSB3 |
| H4 | NC |
| H6 | VCCIB3 |
| H7 | GND |
| H8 | VCC |
| H9 | GND |
| H10 | VCCIB1 |
| H12 | GCB2/IO59RSB1 |
| H13 | GCA0/IO57RSB1 |
| H14 | IO64RSB1 |
| H15 | IO62RSB1 |
| J1 | GFA2/IO134RSB3 |
| J2 | GFA0/IO135RSB3 |
| J3 | GFB2/IO133RSB3 |
| J4 | IO131RSB3 |
| J6 | VCCIB3 |
| J7 | GND |
| J8 | VCC |
| J9 | GND |
| J10 | VCCIB1 |
| J12 | IO61RSB1 |
| J13 | IO63RSB1 |
| J14 | IO68RSB1 |
| J15 | IO66RSB1 |
| K1 | IO130RSB3 |
| K2 | GFC2/IO132RSB3 |
| K3 | IO127RSB3 |
| K4 | IO129RSB3 |
| K6 | GND |
| K7 | VCCIB2 |
| K8 | VCCIB2 |
| K9 | VCCIB2 |
| K10 | VCCIB1 |


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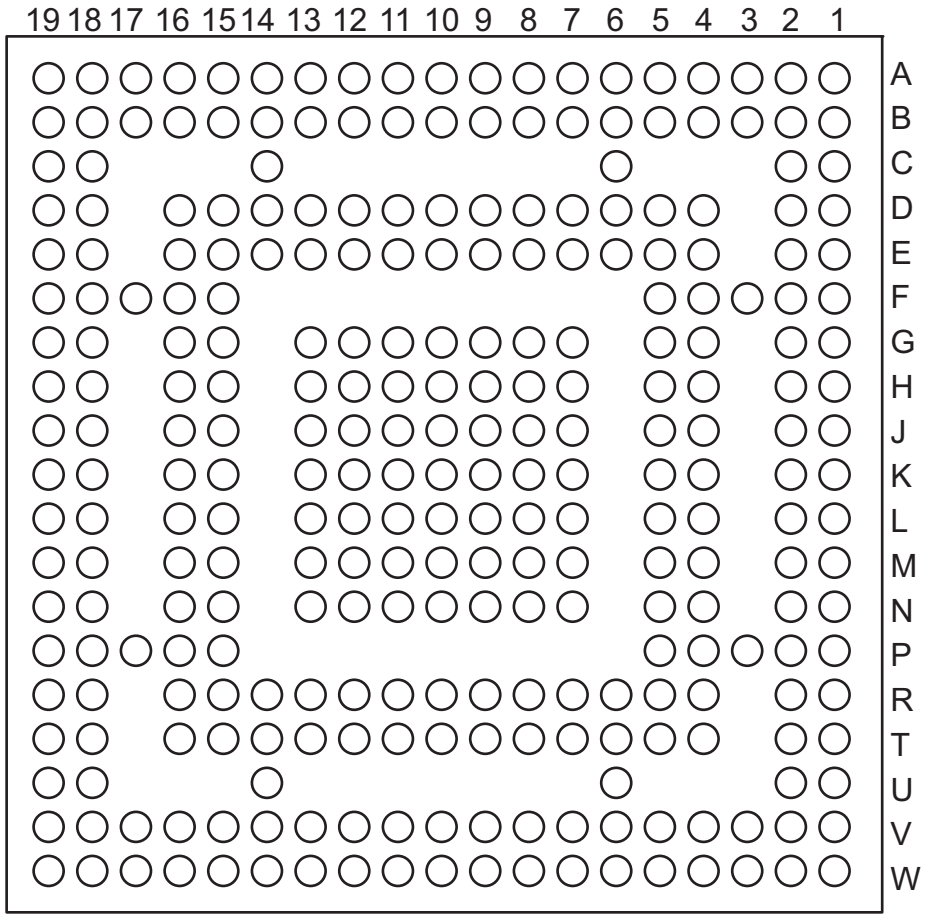
| TABLE 4-4: CS201 | |
|---|---|
| Pin Number | AGLP060 Function |
| K12 | IO65RSB1 |
| K13 | IO67RSB1 |
| K14 | IO69RSB1 |
| K15 | IO70RSB1 |
| L1 | IO126RSB3 |
| L2 | IO128RSB3 |
| L3 | IO121RSB3 |
| L4 | IO123RSB3 |
| L12 | GDB1/IO74RSB1 |
| L13 | GDC1/IO72RSB1 |
| L14 | IO71RSB1 |
| L15 | GDC0/IO73RSB1 |
| M1 | IO122RSB3 |
| M2 | IO124RSB3 |
| M3 | IO119RSB3 |
| M4 | GND |
| M5 | IO125RSB3 |
| M6 | IO98RSB2 |
| M7 | IO96RSB2 |
| M8 | IO91RSB2 |
| M9 | IO89RSB2 |
| M10 | IO82RSB2 |
| M11 | GDA2/IO78RSB2 |
| M12 | GND |
| M13 | GDA1/IO76RSB1 |
| M14 | GDA0/IO77RSB1 |
| M15 | GDB0/IO75RSB1 |
| N1 | IO117RSB3 |
| N2 | IO120RSB3 |
| N3 | GND |
| N4 | GEB1/IO114RSB3 |
| N5 | IO107RSB2 |
| N6 | IO100RSB2 |
| N7 | IO94RSB2 |
| N8 | IO87RSB2 |
| N9 | IO85RSB2 |
| N10 | GDC2/IO80RSB2 |
| N11 | IO90RSB2 |
| N12 | IO84RSB2 |
| N13 | GND |
| N14 | TDO |
| N15 | VJTAG |
| P1 | GEC0/IO115RSB3 |

| TABLE 4-4: CS201 | |
|---|---|
| Pin Number | AGLP060 Function |
| P2 | GEC1/IO116RSB3 |
| P3 | GEA0/IO111RSB3 |
| P4 | GEA1/IO112RSB3 |
| P5 | IO106RSB2 |
| P6 | IO105RSB2 |
| P7 | IO103RSB2 |
| P8 | IO99RSB2 |
| P9 | IO93RSB2 |
| P10 | IO92RSB2 |
| P11 | IO95RSB2 |
| P12 | IO86RSB2 |
| P13 | IO83RSB2 |
| P14 | VPUMP |
| P15 | TRST |
| R1 | IO118RSB3 |
| R2 | GEB0/IO113RSB3 |
| R3 | GEA2/IO110RSB2 |
| R4 | FF/GEB2/ IO109RSB2 |
| R5 | GEC2/IO108RSB2 |
| R6 | IO102RSB2 |
| R7 | IO101RSB2 |
| R8 | IO104RSB2 |
| R9 | IO97RSB2 |
| R10 | IO88RSB2 |
| R11 | IO81RSB2 |
| R12 | GDB2/IO79RSB2 |
| R13 | TMS |
| R14 | TDI |
| R15 | TCK |

**Note:** Pin numbers G1 and H1 must be connected to ground because a PLL is not supported for AGLP060-CS/G201.

## 4.4 CS281

**FIGURE 4-4:**




**Note:** This is the bottom view of the package.

**Note:** For Package Manufacturing and Environmental information, visit the Resource Center at https://www.microchip.com/en-us/products/fpgas-and-plds/packaging.


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| TABLE 4-5: CS281 | |
|---|---|
| **Pin Number** | **AGLP125 Function** |
| A1 | GND |
| A2 | GAB0/IO02RSB0 |
| A3 | GAC1/IO05RSB0 |
| A4 | IO09RSB0 |
| A5 | IO13RSB0 |
| A6 | IO15RSB0 |
| A7 | IO18RSB0 |
| A8 | IO23RSB0 |
| A9 | IO25RSB0 |
| A10 | VCCIB0 |
| A11 | IO33RSB0 |
| A12 | IO41RSB0 |
| A13 | IO43RSB0 |
| A14 | IO46RSB0 |
| A15 | IO55RSB0 |
| A16 | IO56RSB0 |
| A17 | GBC1/IO58RSB0 |
| A18 | GBA0/IO61RSB0 |
| A19 | GND |
| B1 | GAA2/IO211RSB3 |
| B2 | VCCIB0 |
| B3 | GAB1/IO03RSB0 |
| B4 | GAC0/IO04RSB0 |
| B5 | IO11RSB0 |
| B6 | GND |
| B7 | IO21RSB0 |
| B8 | IO22RSB0 |
| B9 | IO28RSB0 |
| B10 | IO32RSB0 |
| B11 | IO36RSB0 |
| B12 | IO39RSB0 |
| B13 | IO42RSB0 |
| B14 | GND |
| B15 | IO52RSB0 |
| B16 | GBC0/IO57RSB0 |
| B17 | GBA1/IO62RSB0 |
| B18 | VCCIB1 |
| B19 | IO64RSB1 |
| C1 | GAB2/IO209RSB3 |
| C2 | IO210RSB3 |
| C6 | IO12RSB0 |
| C14 | IO47RSB0 |
| C18 | IO54RSB0 |
| C19 | GBB2/IO65RSB1 |

| TABLE 4-5: CS281 | |
|---|---|
| **Pin Number** | **AGLP125 Function** |
| D1 | IO206RSB3 |
| D2 | IO208RSB3 |
| D4 | GAA0/IO00RSB0 |
| D5 | GAA1/IO01RSB0 |
| D6 | IO10RSB0 |
| D7 | IO17RSB0 |
| D8 | IO24RSB0 |
| D9 | IO27RSB0 |
| D10 | GND |
| D11 | IO31RSB0 |
| D12 | IO40RSB0 |
| D13 | IO49RSB0 |
| D14 | IO45RSB0 |
| D15 | GBB0/IO59RSB0 |
| D16 | GBA2/IO63RSB1 |
| D18 | GBC2/IO67RSB1 |
| D19 | IO66RSB1 |
| E1 | IO203RSB3 |
| E2 | IO205RSB3 |
| E4 | IO07RSB0 |
| E5 | IO06RSB0 |
| E6 | IO14RSB0 |
| E7 | IO20RSB0 |
| E8 | IO29RSB0 |
| E9 | IO34RSB0 |
| E10 | IO30RSB0 |
| E11 | IO37RSB0 |
| E12 | IO38RSB0 |
| E13 | IO48RSB0 |
| E14 | GBB1/IO60RSB0 |
| E15 | IO53RSB0 |
| E16 | IO69RSB1 |
| E18 | IO68RSB1 |
| E19 | IO71RSB1 |
| F1 | IO198RSB3 |
| F2 | GND |
| F3 | IO201RSB3 |
| F4 | IO204RSB3 |
| F5 | IO16RSB0 |
| F15 | IO50RSB0 |
| F16 | IO74RSB1 |
| F17 | IO72RSB1 |
| F18 | GND |
| F19 | IO73RSB1 |

| TABLE 4-5: CS281 | |
|---|---|
| **Pin Number** | **AGLP125 Function** |
| G1 | IO195RSB3 |
| G2 | IO200RSB3 |
| G4 | IO202RSB3 |
| G5 | IO08RSB0 |
| G7 | GAC2/IO207RSB3 |
| G8 | VCCIB0 |
| G9 | IO26RSB0 |
| G10 | IO35RSB0 |
| G11 | IO44RSB0 |
| G12 | VCCIB0 |
| G13 | IO51RSB0 |
| G15 | IO70RSB1 |
| G16 | IO75RSB1 |
| G18 | GCC0/IO80RSB1 |
| G19 | GCB1/IO81RSB1 |
| H1 | GFB0/IO191RSB3 |
| H2 | IO196RSB3 |
| H4 | GFC1/IO194RSB3 |
| H5 | GFB1/IO192RSB3 |
| H7 | VCCIB3 |
| H8 | VCC |
| H9 | VCCIB0 |
| H10 | VCC |
| H11 | VCCIB0 |
| H12 | VCC |
| H13 | VCCIB1 |
| H15 | IO77RSB1 |
| H16 | GCB0/IO82RSB1 |
| H18 | GCA1/IO83RSB1 |
| H19 | GCA2/IO85RSB1 |
| J1 | VCOMPLF |
| J2 | GFA0/IO189RSB3 |
| J4 | VCCPLF |
| J5 | GFC0/IO193RSB3 |
| J7 | GFA2/IO188RSB3 |
| J8 | VCCIB3 |
| J9 | GND |
| J10 | GND |
| J11 | GND |
| J12 | VCCIB1 |
| J13 | GCC1/IO79RSB1 |
| J15 | GCA0/IO84RSB1 |
| J16 | GCB2/IO86RSB1 |
| J18 | IO76RSB1 |

| TABLE 4-5: CS281 | |
|---|---|
| **Pin Number** | **AGLP125 Function** |
| J19 | IO78RSB1 |
| K1 | VCCIB3 |
| K2 | GFA1/IO190RSB3 |
| K4 | GND |
| K5 | IO19RSB0 |
| K7 | IO197RSB3 |
| K8 | VCC |
| K9 | GND |
| K10 | GND |
| K11 | GND |
| K12 | VCC |
| K13 | GCC2/IO87RSB1 |
| K15 | IO89RSB1 |
| K16 | GND |
| K18 | IO88RSB1 |
| K19 | VCCIB1 |
| L1 | GFB2/IO187RSB3 |
| L2 | IO185RSB3 |
| L4 | GFC2/IO186RSB3 |
| L5 | IO184RSB3 |
| L7 | IO199RSB3 |
| L8 | VCCIB3 |
| L9 | GND |
| L10 | GND |
| L11 | GND |
| L12 | VCCIB1 |
| L13 | IO95RSB1 |
| L15 | IO91RSB1 |
| L16 | NC |
| L18 | IO90RSB1 |
| L19 | NC |
| M1 | IO180RSB3 |
| M2 | IO179RSB3 |
| M4 | IO181RSB3 |
| M5 | IO183RSB3 |
| M7 | VCCIB3 |
| M8 | VCC |
| M9 | VCCIB2 |
| M10 | VCC |
| M11 | VCCIB2 |
| M12 | VCC |
| M13 | VCCIB1 |
| M15 | IO122RSB2 |
| M16 | IO93RSB1 |

| TABLE 4-5: CS281 | |
|---|---|
| **Pin Number** | **AGLP125 Function** |
| M18 | IO92RSB1 |
| M19 | NC |
| N1 | IO178RSB3 |
| N2 | IO175RSB3 |
| N4 | IO182RSB3 |
| N5 | IO161RSB2 |
| N7 | GEA2/IO164RSB2 |
| N8 | VCCIB2 |
| N9 | IO137RSB2 |
| N10 | IO135RSB2 |
| N11 | IO131RSB2 |
| N12 | VCCIB2 |
| N13 | VPUMP |
| N15 | IO117RSB2 |
| N16 | IO96RSB1 |
| N18 | IO98RSB1 |
| N19 | IO94RSB1 |
| P1 | IO174RSB3 |
| P2 | GND |
| P3 | IO176RSB3 |
| P4 | IO177RSB3 |
| P5 | GEA0/IO165RSB3 |
| P15 | IO111RSB2 |
| P16 | IO108RSB2 |
| P17 | GDC1/IO99RSB1 |
| P18 | GND |
| P19 | IO97RSB1 |
| R1 | IO173RSB3 |
| R2 | IO172RSB3 |
| R4 | GEC1/IO170RSB3 |
| R5 | GEB1/IO168RSB3 |
| R6 | IO154RSB2 |
| R7 | IO149RSB2 |
| R8 | IO146RSB2 |
| R9 | IO138RSB2 |
| R10 | IO134RSB2 |
| R11 | IO132RSB2 |
| R12 | IO130RSB2 |
| R13 | IO118RSB2 |
| R14 | IO112RSB2 |
| R15 | IO109RSB2 |
| R16 | GDA1/IO103RSB1 |
| R18 | GDB0/IO102RSB1 |
| R19 | GDC0/IO100RSB1 |

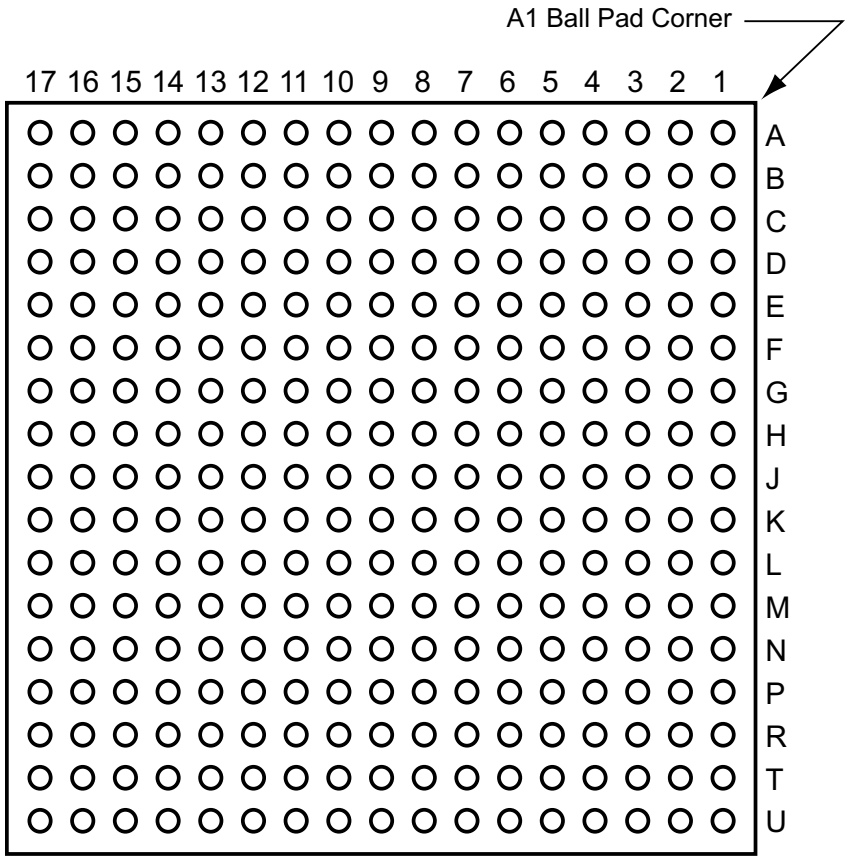
| TABLE 4-5: CS281 | |
|---|---|
| **Pin Number** | **AGLP125 Function** |
| T1 | IO171RSB3 |
| T2 | GEC0/IO169RSB3 |
| T4 | GEB0/IO167RSB3 |
| T5 | IO157RSB2 |
| T6 | IO158RSB2 |
| T7 | IO148RSB2 |
| T8 | IO145RSB2 |
| T9 | IO143RSB2 |
| T10 | GND |
| T11 | IO129RSB2 |
| T12 | IO126RSB2 |
| T13 | IO125RSB2 |
| T14 | IO116RSB2 |
| T15 | GDC2/IO107RSB2 |
| T16 | TMS |
| T18 | VJTAG |
| T19 | GDB1/IO101RSB1 |
| U1 | IO160RSB2 |
| U2 | GEA1/IO166RSB3 |
| U6 | IO151RSB2 |
| U14 | IO121RSB2 |
| U18 | TRST |
| U19 | GDA0/IO104RSB1 |
| V1 | IO159RSB2 |
| V2 | VCCIB3 |
| V3 | GEC2/IO162RSB2 |
| V4 | IO156RSB2 |
| V5 | IO153RSB2 |
| V6 | GND |
| V7 | IO144RSB2 |
| V8 | IO141RSB2 |
| V9 | IO140RSB2 |
| V10 | IO133RSB2 |
| V11 | IO127RSB2 |
| V12 | IO123RSB2 |
| V13 | IO120RSB2 |
| V14 | GND |
| V15 | IO113RSB2 |
| V16 | GDA2/IO105RSB2 |
| V17 | TDI |
| V18 | VCCIB2 |
| V19 | TDO |
| W1 | GND |


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| TABLE 4-5: CS281 | |
|---|---|
| **Pin Number** | **AGLP125 Function** |
| W2 | FF/GEB2/<br>IO163RSB2 |
| W3 | IO155RSB2 |
| W4 | IO152RSB2 |
| W5 | IO150RSB2 |
| W6 | IO147RSB2 |
| W7 | IO142RSB2 |
| W8 | IO139RSB2 |
| W9 | IO136RSB2 |
| W10 | VCCIB2 |
| W11 | IO128RSB2 |
| W12 | IO124RSB2 |
| W13 | IO119RSB2 |
| W14 | IO115RSB2 |
| W15 | IO114RSB2 |
| W16 | IO110RSB2 |
| W17 | GDB2/IO106RSB2 |
| W18 | TCK |
| W19 | GND |

## 4.5 CS289

**FIGURE 4-5:**




**Note:** This is the bottom view of the package.

**Note:** For Package Manufacturing and Environmental information, visit the Resource Center at https://www.microchip.com/en-us/products/fpgas-and-plds/packaging.


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| TABLE 4-6: CS289 | |
|---|---|
| Pin Number | AGLP030 Function |
| A1 | IO03RSB0 |
| A2 | NC |
| A3 | NC |
| A4 | GND |
| A5 | IO10RSB0 |
| A6 | IO14RSB0 |
| A7 | IO16RSB0 |
| A8 | IO18RSB0 |
| A9 | GND |
| A10 | IO23RSB0 |
| A11 | IO27RSB0 |
| A12 | NC |
| A13 | NC |
| A14 | GND |
| A15 | NC |
| A16 | NC |
| A17 | IO30RSB0 |
| B1 | IO01RSB0 |
| B2 | GND |
| B3 | NC |
| B4 | NC |
| B5 | IO07RSB0 |
| B6 | NC |
| B7 | VCCIB0 |
| B8 | IO17RSB0 |
| B9 | IO19RSB0 |
| B10 | IO24RSB0 |
| B11 | IO28RSB0 |
| B12 | VCCIB0 |
| B13 | NC |
| B14 | NC |
| B15 | NC |
| B16 | IO31RSB0 |
| B17 | GND |
| C1 | NC |
| C2 | IO00RSB0 |
| C3 | IO04RSB0 |
| C4 | NC |
| C5 | VCCIB0 |
| C6 | IO09RSB0 |
| C7 | IO13RSB0 |
| C8 | IO15RSB0 |
| C9 | IO21RSB0 |
| C10 | GND |
| C11 | IO29RSB0 |
| C12 | NC |
| C13 | NC |

| TABLE 4-6: CS289 | |
|---|---|
| Pin Number | AGLP030 Function |
| C14 | NC |
| C15 | GND |
| C16 | IO34RSB0 |
| C17 | NC |
| D1 | NC |
| D2 | IO119RSB3 |
| D3 | GND |
| D4 | IO02RSB0 |
| D5 | NC |
| D6 | NC |
| D7 | NC |
| D8 | GND |
| D9 | IO20RSB0 |
| D10 | IO25RSB0 |
| D11 | NC |
| D12 | NC |
| D13 | GND |
| D14 | IO32RSB0 |
| D15 | IO35RSB0 |
| D16 | NC |
| D17 | NC |
| E1 | VCCIB3 |
| E2 | IO114RSB3 |
| E3 | IO115RSB3 |
| E4 | IO118RSB3 |
| E5 | IO05RSB0 |
| E6 | NC |
| E7 | IO06RSB0 |
| E8 | IO11RSB0 |
| E9 | IO22RSB0 |
| E10 | IO26RSB0 |
| E11 | VCCIB0 |
| E12 | NC |
| E13 | IO33RSB0 |
| E14 | IO36RSB1 |
| E15 | IO38RSB1 |
| E16 | VCCIB1 |
| E17 | NC |
| F1 | IO111RSB3 |
| F2 | NC |
| F3 | IO116RSB3 |
| F4 | VCCIB3 |
| F5 | IO117RSB3 |
| F6 | NC |
| F7 | NC |
| F8 | IO08RSB0 |
| F9 | IO12RSB0 |

| TABLE 4-6: CS289 | |
|---|---|
| Pin Number | AGLP030 Function |
| F10 | NC |
| F11 | NC |
| F12 | NC |
| F13 | NC |
| F14 | GND |
| F15 | NC |
| F16 | IO37RSB1 |
| F17 | IO41RSB1 |
| G1 | IO110RSB3 |
| G2 | GND |
| G3 | IO113RSB3 |
| G4 | NC |
| G5 | NC |
| G6 | NC |
| G7 | GND |
| G8 | GND |
| G9 | VCC |
| G10 | GND |
| G11 | GND |
| G12 | IO40RSB1 |
| G13 | NC |
| G14 | IO39RSB1 |
| G15 | IO44RSB1 |
| G16 | NC |
| G17 | GND |
| H1 | NC |
| H2 | GEC0/IO108RSB3 |
| H3 | NC |
| H4 | IO112RSB3 |
| H5 | NC |
| H6 | IO109RSB3 |
| H7 | GND |
| H8 | GND |
| H9 | GND |
| H10 | GND |
| H11 | GND |
| H12 | NC |
| H13 | NC |
| H14 | IO45RSB1 |
| H15 | VCCIB1 |
| H16 | GDB0/IO48RSB1 |
| H17 | IO42RSB1 |
| J1 | NC |
| J2 | GEA0/IO107RSB3 |
| J3 | VCCIB3 |
| J4 | IO105RSB3 |
| J5 | NC |

| TABLE 4-6: CS289 | |
|---|---|
| Pin Number | AGLP030 Function |
| J6 | NC |
| J7 | VCC |
| J8 | GND |
| J9 | GND |
| J10 | GND |
| J11 | VCC |
| J12 | IO50RSB1 |
| J13 | IO43RSB1 |
| J14 | IO51RSB1 |
| J15 | IO52RSB1 |
| J16 | GDC0/IO46RSB1 |
| J17 | GDA0/IO47RSB1 |
| K1 | GND |
| K2 | GEB0/IO106RSB3 |
| K3 | IO102RSB3 |
| K4 | IO104RSB3 |
| K5 | IO99RSB3 |
| K6 | NC |
| K7 | GND |
| K8 | GND |
| K9 | GND |
| K10 | GND |
| K11 | GND |
| K12 | NC |
| K13 | NC |
| K14 | NC |
| K15 | IO53RSB1 |
| K16 | GND |
| K17 | IO49RSB1 |
| L1 | IO103RSB3 |
| L2 | IO101RSB3 |
| L3 | NC |
| L4 | GND |
| L5 | NC |
| L6 | NC |
| L7 | GND |
| L8 | GND |
| L9 | VCC |
| L10 | GND |
| L11 | GND |
| L12 | IO58RSB1 |
| L13 | IO54RSB1 |
| L14 | VCCIB1 |
| L15 | NC |
| L16 | NC |
| L17 | NC |
| M1 | NC |

| TABLE 4-6: CS289 | |
|---|---|
| Pin Number | AGLP030 Function |
| M2 | VCCIB3 |
| M3 | IO100RSB3 |
| M4 | IO98RSB3 |
| M5 | IO93RSB3 |
| M6 | IO97RSB3 |
| M7 | NC |
| M8 | NC |
| M9 | IO71RSB2 |
| M10 | NC |
| M11 | IO63RSB2 |
| M12 | NC |
| M13 | IO57RSB1 |
| M14 | NC |
| M15 | NC |
| M16 | NC |
| M17 | VCCIB1 |
| N1 | NC |
| N2 | NC |
| N3 | IO95RSB3 |
| N4 | IO96RSB3 |
| N5 | GND |
| N6 | NC |
| N7 | IO85RSB2 |
| N8 | IO79RSB2 |
| N9 | IO77RSB2 |
| N10 | VCCIB2 |
| N11 | NC |
| N12 | NC |
| N13 | IO59RSB2 |
| N14 | NC |
| N15 | GND |
| N16 | IO56RSB1 |
| N17 | IO55RSB1 |
| P1 | IO94RSB3 |
| P2 | NC |
| P3 | GND |
| P4 | NC |
| P5 | NC |
| P6 | IO87RSB2 |
| P7 | IO80RSB2 |
| P8 | GND |
| P9 | IO72RSB2 |
| P10 | IO67RSB2 |
| P11 | IO61RSB2 |
| P12 | NC |
| P13 | VCCIB2 |
| P14 | NC |

| TABLE 4-6: CS289 | |
|---|---|
| Pin Number | AGLP030 Function |
| P15 | IO60RSB2 |
| P16 | IO62RSB2 |
| P17 | VJTAG |
| R1 | GND |
| R2 | IO91RSB2 |
| R3 | NC |
| R4 | NC |
| R5 | NC |
| R6 | VCCIB2 |
| R7 | IO83RSB2 |
| R8 | IO78RSB2 |
| R9 | IO74RSB2 |
| R10 | IO70RSB2 |
| R11 | GND |
| R12 | NC |
| R13 | NC |
| R14 | NC |
| R15 | NC |
| R16 | TMS |
| R17 | TRST |
| T1 | IO92RSB3 |
| T2 | IO89RSB2 |
| T3 | NC |
| T4 | GND |
| T5 | NC |
| T6 | IO84RSB2 |
| T7 | IO81RSB2 |
| T8 | IO76RSB2 |
| T9 | VCCIB2 |
| T10 | IO69RSB2 |
| T11 | IO65RSB2 |
| T12 | IO64RSB2 |
| T13 | NC |
| T14 | GND |
| T15 | NC |
| T16 | TDI |
| T17 | TDO |
| U1 | FF/IO90RSB2 |
| U2 | GND |
| U3 | NC |
| U4 | IO88RSB2 |
| U5 | IO86RSB2 |
| U6 | IO82RSB2 |
| U7 | GND |
| U8 | IO75RSB2 |
| U9 | IO73RSB2 |
| U10 | IO68RSB2 |


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| TABLE 4-6: CS289 | |
|---|---|
| **Pin Number** | **AGLP030 Function** |
| U11 | IO66RSB2 |
| U12 | GND |
| U13 | NC |
| U14 | NC |
| U15 | NC |
| U16 | TCK |
| U17 | VPUMP |

| TABLE 4-7: CS289 | |
|---|---|
| **Pin Number** | **AGLP060 Function** |
| A1 | GAB1/IO03RSB0 |
| A2 | NC |
| A3 | NC |
| A4 | GND |
| A5 | IO10RSB0 |
| A6 | IO14RSB0 |
| A7 | IO16RSB0 |
| A8 | IO18RSB0 |
| A9 | GND |
| A10 | IO23RSB0 |
| A11 | IO27RSB0 |
| A12 | NC |
| A13 | NC |
| A14 | GND |
| A15 | NC |
| A16 | NC |
| A17 | GBC0/IO30RSB0 |
| B1 | GAA1/IO01RSB0 |
| B2 | GND |
| B3 | NC |
| B4 | NC |
| B5 | IO07RSB0 |
| B6 | NC |
| B7 | VCCIB0 |
| B8 | IO17RSB0 |
| B9 | IO19RSB0 |
| B10 | IO24RSB0 |
| B11 | IO28RSB0 |
| B12 | VCCIB0 |
| B13 | NC |
| B14 | NC |
| B15 | NC |
| B16 | GBC1/IO31RSB0 |
| B17 | GND |
| C1 | IO155RSB3 |
| C2 | GAA0/IO00RSB0 |
| C3 | GAC0/IO04RSB0 |
| C4 | NC |
| C5 | VCCIB0 |
| C6 | IO09RSB0 |
| C7 | IO13RSB0 |
| C8 | IO15RSB0 |
| C9 | IO21RSB0 |
| C10 | GND |
| C11 | IO29RSB0 |
| C12 | NC |
| C13 | NC |
| C14 | NC |

| TABLE 4-7: CS289 | |
|---|---|
| **Pin Number** | **AGLP060 Function** |
| C15 | GND |
| C16 | GBA0/IO34RSB0 |
| C17 | IO39RSB1 |
| D1 | IO150RSB3 |
| D2 | IO151RSB3 |
| D3 | GND |
| D4 | GAB0/IO02RSB0 |
| D5 | NC |
| D6 | NC |
| D7 | NC |
| D8 | GND |
| D9 | IO20RSB0 |
| D10 | IO25RSB0 |
| D11 | NC |
| D12 | NC |
| D13 | GND |
| D14 | GBB0/IO32RSB0 |
| D15 | GBA1/IO35RSB0 |
| D16 | IO37RSB1 |
| D17 | IO42RSB1 |
| E1 | VCCIB3 |
| E2 | IO147RSB3 |
| E3 | GAC2/IO152RSB3 |
| E4 | GAA2/IO156RSB3 |
| E5 | GAC1/IO05RSB0 |
| E6 | NC |
| E7 | IO06RSB0 |
| E8 | IO11RSB0 |
| E9 | IO22RSB0 |
| E10 | IO26RSB0 |
| E11 | VCCIB0 |
| E12 | NC |
| E13 | GBB1/IO33RSB0 |
| E14 | GBA2/IO36RSB1 |
| E15 | GBB2/IO38RSB1 |
| E16 | VCCIB1 |
| E17 | IO44RSB1 |
| F1 | GFC1/IO140RSB3 |
| F2 | IO142RSB3 |
| F3 | IO149RSB3 |
| F4 | VCCIB3 |
| F5 | GAB2/IO154RSB3 |
| F6 | IO153RSB3 |
| F7 | NC |
| F8 | IO08RSB0 |
| F9 | IO12RSB0 |
| F10 | NC |
| F11 | NC |

| TABLE 4-7: CS289 | |
|---|---|
| **Pin Number** | **AGLP060 Function** |
| F12 | NC |
| F13 | GBC2/IO40RSB1 |
| F14 | GND |
| F15 | IO43RSB1 |
| F16 | IO46RSB1 |
| F17 | IO45RSB1 |
| G1 | GFC0/IO139RSB3 |
| G2 | GND |
| G3 | IO144RSB3 |
| G4 | IO145RSB3 |
| G5 | IO146RSB3 |
| G6 | IO148RSB3 |
| G7 | GND |
| G8 | GND |
| G9 | VCC |
| G10 | GND |
| G11 | GND |
| G12 | IO48RSB1 |
| G13 | IO41RSB1 |
| G14 | IO47RSB1 |
| G15 | IO49RSB1 |
| G16 | IO50RSB1 |
| G17 | GND |
| H1 | VCOMPLF |
| H2 | GFB0/IO137RSB3 |
| H3 | NC |
| H4 | IO141RSB3 |
| H5 | IO143RSB3 |
| H6 | GFB1/IO138RSB3 |
| H7 | GND |
| H8 | GND |
| H9 | GND |
| H10 | GND |
| H11 | GND |
| H12 | GCC1/IO52RSB1 |
| H13 | IO51RSB1 |
| H14 | GCA0/IO57RSB1 |
| H15 | VCCIB1 |
| H16 | GCA2/IO58RSB1 |
| H17 | GCC0/IO53RSB1 |
| J1 | VCCPLF |
| J2 | GFA1/IO136RSB3 |
| J3 | VCCIB3 |
| J4 | IO131RSB3 |
| J5 | IO130RSB3 |
| J6 | IO129RSB3 |
| J7 | VCC |
| J8 | GND |


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| TABLE 4-7: CS289 | |
|---|---|
| **Pin Number** | **AGLP060 Function** |
| J9 | GND |
| J10 | GND |
| J11 | VCC |
| J12 | GCB2/IO59RSB1 |
| J13 | GCB1/IO54RSB1 |
| J14 | IO62RSB1 |
| J15 | IO63RSB1 |
| J16 | GCB0/IO55RSB1 |
| J17 | GCA1/IO56RSB1 |
| K1 | GND |
| K2 | GFA0/IO135RSB3 |
| K3 | GFB2/IO133RSB3 |
| K4 | IO128RSB3 |
| K5 | IO123RSB3 |
| K6 | IO125RSB3 |
| K7 | GND |
| K8 | GND |
| K9 | GND |
| K10 | GND |
| K11 | GND |
| K12 | IO64RSB1 |
| K13 | IO61RSB1 |
| K14 | IO66RSB1 |
| K15 | IO65RSB1 |
| K16 | GND |
| K17 | GCC2/IO60RSB1 |
| L1 | GFA2/IO134RSB3 |
| L2 | GFC2/IO132RSB3 |
| L3 | IO127RSB3 |
| L4 | GND |
| L5 | IO121RSB3 |
| L6 | GEC1/IO116RSB3 |
| L7 | GND |
| L8 | GND |
| L9 | VCC |
| L10 | GND |
| L11 | GND |
| L12 | GDC1/IO72RSB1 |
| L13 | GDB1/IO74RSB1 |
| L14 | VCCIB1 |
| L15 | IO70RSB1 |
| L16 | IO68RSB1 |
| L17 | IO67RSB1 |
| M1 | IO126RSB3 |
| M2 | VCCIB3 |
| M3 | IO124RSB3 |
| M4 | IO122RSB3 |
| M5 | GEB0/IO113RSB3 |

| TABLE 4-7: CS289 | |
|---|---|
| **Pin Number** | **AGLP060 Function** |
| M6 | GEB1/IO114RSB3 |
| M7 | NC |
| M8 | NC |
| M9 | IO90RSB2 |
| M10 | NC |
| M11 | IO83RSB2 |
| M12 | NC |
| M13 | GDA1/IO76RSB1 |
| M14 | GDA0/IO77RSB1 |
| M15 | IO71RSB1 |
| M16 | IO69RSB1 |
| M17 | VCCIB1 |
| N1 | IO119RSB3 |
| N2 | IO120RSB3 |
| N3 | GEC0/IO115RSB3 |
| N4 | GEA0/IO111RSB3 |
| N5 | GND |
| N6 | NC |
| N7 | IO104RSB2 |
| N8 | IO98RSB2 |
| N9 | IO96RSB2 |
| N10 | VCCIB2 |
| N11 | NC |
| N12 | NC |
| N13 | GDB2/IO79RSB2 |
| N14 | NC |
| N15 | GND |
| N16 | GDB0/IO75RSB1 |
| N17 | GDC0/IO73RSB1 |
| P1 | IO118RSB3 |
| P2 | IO117RSB3 |
| P3 | GND |
| P4 | NC |
| P5 | NC |
| P6 | IO106RSB2 |
| P7 | IO99RSB2 |
| P8 | GND |
| P9 | IO91RSB2 |
| P10 | IO86RSB2 |
| P11 | IO81RSB2 |
| P12 | NC |
| P13 | VCCIB2 |
| P14 | NC |
| P15 | GDA2/IO78RSB2 |
| P16 | GDC2/IO80RSB2 |
| P17 | VJTAG |
| R1 | GND |
| R2 | GEA2/IO110RSB2 |

| TABLE 4-7: CS289 | |
|---|---|
| **Pin Number** | **AGLP060 Function** |
| R3 | NC |
| R4 | NC |
| R5 | NC |
| R6 | VCCIB2 |
| R7 | IO102RSB2 |
| R8 | IO97RSB2 |
| R9 | IO93RSB2 |
| R10 | IO89RSB2 |
| R11 | GND |
| R12 | NC |
| R13 | NC |
| R14 | NC |
| R15 | NC |
| R16 | TMS |
| R17 | TRST |
| T1 | GEA1/IO112RSB3 |
| T2 | GEC2/IO108RSB2 |
| T3 | NC |
| T4 | GND |
| T5 | NC |
| T6 | IO103RSB2 |
| T7 | IO100RSB2 |
| T8 | IO95RSB2 |
| T9 | VCCIB2 |
| T10 | IO88RSB2 |
| T11 | IO84RSB2 |
| T12 | IO82RSB2 |
| T13 | NC |
| T14 | GND |
| T15 | NC |
| T16 | TDI |
| T17 | TDO |
| U1 | FF/GEB2/ IO109RSB2 |
| U2 | GND |
| U3 | NC |
| U4 | IO107RSB2 |
| U5 | IO105RSB2 |
| U6 | IO101RSB2 |
| U7 | GND |
| U8 | IO94RSB2 |
| U9 | IO92RSB2 |
| U10 | IO87RSB2 |
| U11 | IO85RSB2 |
| U12 | GND |
| U13 | NC |
| U14 | NC |
| U15 | NC |

| TABLE 4-7: CS289 | |
|---|---|
| **Pin Number** | **AGLP060 Function** |
| U16 | TCK |
| U17 | VPUMP |


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| TABLE 4-8: CS289 | |
|---|---|
| **Pin Number** | **AGLP125 Function** |
| A1 | GAB1/IO03RSB0 |
| A2 | IO11RSB0 |
| A3 | IO08RSB0 |
| A4 | GND |
| A5 | IO19RSB0 |
| A6 | IO24RSB0 |
| A7 | IO26RSB0 |
| A8 | IO30RSB0 |
| A9 | GND |
| A10 | IO35RSB0 |
| A11 | IO38RSB0 |
| A12 | IO40RSB0 |
| A13 | IO42RSB0 |
| A14 | GND |
| A15 | IO48RSB0 |
| A16 | IO54RSB0 |
| A17 | GBC0/IO57RSB0 |
| B1 | GAA1/IO01RSB0 |
| B2 | GND |
| B3 | IO06RSB0 |
| B4 | IO13RSB0 |
| B5 | IO15RSB0 |
| B6 | IO21RSB0 |
| B7 | VCCIB0 |
| B8 | IO28RSB0 |
| B9 | IO31RSB0 |
| B10 | IO37RSB0 |
| B11 | IO39RSB0 |
| B12 | VCCIB0 |
| B13 | IO44RSB0 |
| B14 | IO46RSB0 |
| B15 | IO49RSB0 |
| B16 | GBC1/IO58RSB0 |
| B17 | GND |
| C1 | IO210RSB3 |
| C2 | GAA0/IO00RSB0 |
| C3 | GAC0/IO04RSB0 |
| C4 | IO09RSB0 |
| C5 | VCCIB0 |
| C6 | IO17RSB0 |
| C7 | IO23RSB0 |
| C8 | IO27RSB0 |
| C9 | IO33RSB0 |
| C10 | GND |
| C11 | IO43RSB0 |
| C12 | IO45RSB0 |
| C13 | IO50RSB0 |
| C14 | IO52RSB0 |

| TABLE 4-8: CS289 | |
|---|---|
| **Pin Number** | **AGLP125 Function** |
| C15 | GND |
| C16 | GBA0/IO61RSB0 |
| C17 | IO68RSB1 |
| D1 | IO204RSB3 |
| D2 | IO205RSB3 |
| D3 | GND |
| D4 | GAB0/IO02RSB0 |
| D5 | IO07RSB0 |
| D6 | IO10RSB0 |
| D7 | IO18RSB0 |
| D8 | GND |
| D9 | IO34RSB0 |
| D10 | IO41RSB0 |
| D11 | IO47RSB0 |
| D12 | IO55RSB0 |
| D13 | GND |
| D14 | GBB0/IO59RSB0 |
| D15 | GBA1/IO62RSB0 |
| D16 | IO66RSB1 |
| D17 | IO70RSB1 |
| E1 | VCCIB3 |
| E2 | IO200RSB3 |
| E3 | GAC2/IO207RSB3 |
| E4 | GAA2/IO211RSB3 |
| E5 | GAC1/IO05RSB0 |
| E6 | IO12RSB0 |
| E7 | IO16RSB0 |
| E8 | IO22RSB0 |
| E9 | IO32RSB0 |
| E10 | IO36RSB0 |
| E11 | VCCIB0 |
| E12 | IO56RSB0 |
| E13 | GBB1/IO60RSB0 |
| E14 | GBA2/IO63RSB1 |
| E15 | GBB2/IO65RSB1 |
| E16 | VCCIB1 |
| E17 | IO73RSB1 |
| F1 | GFC1/IO194RSB3 |
| F2 | IO196RSB3 |
| F3 | IO202RSB3 |
| F4 | VCCIB3 |
| F5 | GAB2/IO209RSB3 |
| F6 | IO208RSB3 |
| F7 | IO14RSB0 |
| F8 | IO20RSB0 |
| F9 | IO25RSB0 |
| F10 | IO29RSB0 |
| F11 | IO51RSB0 |

| TABLE 4-8: CS289 | |
|---|---|
| **Pin Number** | **AGLP125 Function** |
| F12 | IO53RSB0 |
| F13 | GBC2/IO67RSB1 |
| F14 | GND |
| F15 | IO75RSB1 |
| F16 | IO71RSB1 |
| F17 | IO77RSB1 |
| G1 | GFC0/IO193RSB3 |
| G2 | GND |
| G3 | IO198RSB3 |
| G4 | IO203RSB3 |
| G5 | IO201RSB3 |
| G6 | IO206RSB3 |
| G7 | GND |
| G8 | GND |
| G9 | VCC |
| G10 | GND |
| G11 | GND |
| G12 | IO72RSB1 |
| G13 | IO64RSB1 |
| G14 | IO69RSB1 |
| G15 | IO78RSB1 |
| G16 | IO76RSB1 |
| G17 | GND |
| H1 | VCOMPLF |
| H2 | GFB0/IO191RSB3 |
| H3 | IO195RSB3 |
| H4 | IO197RSB3 |
| H5 | IO199RSB3 |
| H6 | GFB1/IO192RSB3 |
| H7 | GND |
| H8 | GND |
| H9 | GND |
| H10 | GND |
| H11 | GND |
| H12 | GCC1/IO79RSB1 |
| H13 | IO74RSB1 |
| H14 | GCA0/IO84RSB1 |
| H15 | VCCIB1 |
| H16 | GCA2/IO85RSB1 |
| H17 | GCC0/IO80RSB1 |
| J1 | VCCPLF |
| J2 | GFA1/IO190RSB3 |
| J3 | VCCIB3 |
| J4 | IO185RSB3 |
| J5 | IO183RSB3 |
| J6 | IO181RSB3 |
| J7 | VCC |
| J8 | GND |

| TABLE 4-8: CS289 | |
|---|---|
| **Pin Number** | **AGLP125 Function** |
| J9 | GND |
| J10 | GND |
| J11 | VCC |
| J12 | GCB2/IO86RSB1 |
| J13 | GCB1/IO81RSB1 |
| J14 | IO90RSB1 |
| J15 | IO89RSB1 |
| J16 | GCB0/IO82RSB1 |
| J17 | GCA1/IO83RSB1 |
| K1 | GND |
| K2 | GFA0/IO189RSB3 |
| K3 | GFB2/IO187RSB3 |
| K4 | IO179RSB3 |
| K5 | IO175RSB3 |
| K6 | IO177RSB3 |
| K7 | GND |
| K8 | GND |
| K9 | GND |
| K10 | GND |
| K11 | GND |
| K12 | IO88RSB1 |
| K13 | IO94RSB1 |
| K14 | IO95RSB1 |
| K15 | IO93RSB1 |
| K16 | GND |
| K17 | GCC2/IO87RSB1 |
| L1 | GFA2/IO188RSB3 |
| L2 | GFC2/IO186RSB3 |
| L3 | IO182RSB3 |
| L4 | GND |
| L5 | IO173RSB3 |
| L6 | GEC1/IO170RSB3 |
| L7 | GND |
| L8 | GND |
| L9 | VCC |
| L10 | GND |
| L11 | GND |
| L12 | GDC1/IO99RSB1 |
| L13 | GDB1/IO101RSB1 |
| L14 | VCCIB1 |
| L15 | IO98RSB1 |
| L16 | IO92RSB1 |
| L17 | IO91RSB1 |
| M1 | IO184RSB3 |
| M2 | VCCIB3 |
| M3 | IO176RSB3 |
| M4 | IO172RSB3 |
| M5 | GEB0/IO167RSB3 |

| TABLE 4-8: CS289 | |
|---|---|
| **Pin Number** | **AGLP125 Function** |
| M6 | GEB1/IO168RSB3 |
| M7 | IO159RSB2 |
| M8 | IO161RSB2 |
| M9 | IO135RSB2 |
| M10 | IO128RSB2 |
| M11 | IO121RSB2 |
| M12 | IO113RSB2 |
| M13 | GDA1/IO103RSB1 |
| M14 | GDA0/IO104RSB1 |
| M15 | IO97RSB1 |
| M16 | IO96RSB1 |
| M17 | VCCIB1 |
| N1 | IO180RSB3 |
| N2 | IO178RSB3 |
| N3 | GEC0/IO169RSB3 |
| N4 | GEA0/IO165RSB3 |
| N5 | GND |
| N6 | IO156RSB2 |
| N7 | IO148RSB2 |
| N8 | IO144RSB2 |
| N9 | IO137RSB2 |
| N10 | VCCIB2 |
| N11 | IO119RSB2 |
| N12 | IO111RSB2 |
| N13 | GDB2/IO106RSB2 |
| N14 | IO109RSB2 |
| N15 | GND |
| N16 | GDB0/IO102RSB1 |
| N17 | GDC0/IO100RSB1 |
| P1 | IO174RSB3 |
| P2 | IO171RSB3 |
| P3 | GND |
| P4 | IO160RSB2 |
| P5 | IO157RSB2 |
| P6 | IO154RSB2 |
| P7 | IO152RSB2 |
| P8 | GND |
| P9 | IO132RSB2 |
| P10 | IO125RSB2 |
| P11 | IO126RSB2 |
| P12 | IO112RSB2 |
| P13 | VCCIB2 |
| P14 | IO108RSB2 |
| P15 | GDA2/IO105RSB2 |
| P16 | GDC2/IO107RSB2 |
| P17 | VJTAG |
| R1 | GND |
| R2 | GEA2/IO164RSB2 |

| TABLE 4-8: CS289 | |
|---|---|
| **Pin Number** | **AGLP125 Function** |
| R3 | IO158RSB2 |
| R4 | IO155RSB2 |
| R5 | IO150RSB2 |
| R6 | VCCIB2 |
| R7 | IO145RSB2 |
| R8 | IO141RSB2 |
| R9 | IO134RSB2 |
| R10 | IO130RSB2 |
| R11 | GND |
| R12 | IO118RSB2 |
| R13 | IO116RSB2 |
| R14 | IO114RSB2 |
| R15 | IO110RSB2 |
| R16 | TMS |
| R17 | TRST |
| T1 | GEA1/IO166RSB3 |
| T2 | GEC2/IO162RSB2 |
| T3 | IO153RSB2 |
| T4 | GND |
| T5 | IO147RSB2 |
| T6 | IO143RSB2 |
| T7 | IO140RSB2 |
| T8 | IO139RSB2 |
| T9 | VCCIB2 |
| T10 | IO131RSB2 |
| T11 | IO127RSB2 |
| T12 | IO124RSB2 |
| T13 | IO122RSB2 |
| T14 | GND |
| T15 | IO115RSB2 |
| T16 | TDI |
| T17 | TDO |
| U1 | FF/GEB2/ IO163RSB2 |
| U2 | GND |
| U3 | IO151RSB2 |
| U4 | IO149RSB2 |
| U5 | IO146RSB2 |
| U6 | IO142RSB2 |
| U7 | GND |
| U8 | IO138RSB2 |
| U9 | IO136RSB2 |
| U10 | IO133RSB2 |
| U11 | IO129RSB2 |
| U12 | GND |
| U13 | IO123RSB2 |
| U14 | IO120RSB2 |
| U15 | IO117RSB2 |


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| TABLE 4-8: CS289 | |
|---|---|
| **Pin Number** | **AGLP125 Function** |
| U16 | TCK |
| U17 | VPUMP |

# APPENDIX A: REVISION HISTORY

The following table lists critical changes that were made in each revision of the IGLOO PLUS datasheet.

## A.1 Revision B - 06/2024

The following is a summary of changes in revision B of the document:

- Updated Table 1 by adding superscript 3 to clarify the discontinuity of package CS201.
- Updated Table 2 by adding superscript 1 to clarify the discontinuity of packages CS289, CS201, and VQ176.
- Updated Table 4 by adding superscript 1 to clarify the discontinuity of AGLP060 and AGLP125.
- Updated Table 5 by adding superscript 3 for discontinuity of packages CS201, CS289, and VQ176.

## A.2 Revision A - 02/2023

The following is a summary of changes in revision A of the document:

- The document was migrated to Microchip template.
- Updated the document number to DS50003484A.
- Updated Table 1 by adding note 3 to clarify the discontinuity of CS289, CS281, and VQ176 .

## A.3 Revision 18 - 12/2022

The following is a summary of changes in revision 18 of the document:

- The document was migrated to Microchip template.
- Updated the note in Section 4.1, VQ128.
- Updated the note in Section 4.2, VQ176.

## A.4 Revision 17 - 12/2015

The following is a summary of changes in revision 17 of the document:

- Updated Commercial and Industrial temperature range to show junction temperature in IGLOO PLUS Ordering Information and Temperature Grade Offerings.
- Removed Ambient temperature parameter in Table 2-2.
- Table notes are added to Table 2-2 stating that:
  - VMV pins must be connected to the corresponding VCCI pins.
  - Software default junction temperature range in the Libero SoC software is set to 0 °C to +70 °C for commercial, and -40 °C to +85 °C for industrial.
- Updated Table 2-5.
- Added 2 mA drive strength information in the following tables:
  - Table 2-36
  - Table 2-37
  - Table 2-38
  - Table 2-39
- Fixed typo for VQ128 in Section 4.0, Package Pin Assignments

## A.5 Revision 16 - 12/2012

The following is a summary of changes in revision 16 of the document:

- The IGLOO PLUS Ordering Information has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio".
- The note in Table 2-90 and Table 2-91 referring the reader to SmartGen was revised to refer instead to the online help associated with the core.
- Live at Power-Up (LAPU) has been replaced with 'Instant On'.


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## A.6 Revision 15 - 10/2012

The following is a summary of change in revision 15 of the document:

- Values updated for IGLOO PLUS V2 or V5 Devices, 1.5 V Core Supply Voltage in Table 2-15 and for IGLOO PLUS V2 Devices, 1.2 V Core Supply Voltage in Table 2-17. Also added a new Note to the two tables.
- Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document.

## A.7 Revision 14 - 09/2012

The following is a summary of change in revision 14 of the document:

- The Section 1.2.2, Security section was modified to clarify that Microsemi does not support read-back of programmed data.

## A.8 Revision 13 - 06/2012

The following is a summary of change in revision 13 of the document:

- Table 2-30 and Table 2-31 have been added.
- Updated the terminology used in Timing Characteristics in the following tables: Table 2-96 and Table 2-97.
- The following sentence was removed from the Section 3.1.5, VMVx - I/O Supply Voltage (quiet) in the Section 3.0, Pin Descriptions and Packaging: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with “Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks”. The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.

## A.9 Revision 12 - 03/2010

The following is a summary of changes in revision 12 of the document:

- The In-System Programming (ISP) and Security and Section 1.2.2, Security were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry.
- The Y security option and Licensed DPA Logo were added to the IGLOO PLUS Ordering Information. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research.
- The Section 1.6, Specifying I/O States During Programming is new.
- The following sentence was removed from the Section 1.4, Advanced Architecture:
- "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3V) programming of IGLOO PLUS devices via an IEEE 1532 JTAG interface".
- The reference to guidelines for global spines and VersaTile rows, given in the Section 2.6.1.4, Global Clock Contribution—PCLOCK, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *IGLOO PLUS FPGA Fabric User's Guide*.
- $t_{DOUT}$ was corrected to $t_{DIN}$ in Table 2-4.
- The AC Loading figures in the Section 2.7.4, Single-Ended I/O Characteristics were updated to match tables in the Section 2.7.2.2, Summary of I/O Timing Characteristics – Default I/O Software Settings.
- Minimum pulse width High and Low values were added to the tables in the Global Tree Timing Characteristics. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency.
- Table 2-90 and Table 2-91 were updated. A note was added to both tables indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available.
- The value for serial clock was missing from these tables and has been restored. The value and units for input cycle-to-cycle jitter were incorrect and have been restored. The note to Table 2-90 giving specifications for which measurements done was corrected from VCC/VCCPLL = 1.14V to VCC/VCCPLL = 1.425V. The Delay Range in Block: Programmable Delay 2 value in Table 2-91 was corrected from 0.025 to 0.863.
- *Figure 2-28 • Write Access after Read onto Same Address* was deleted. Reference was made to a new applica-

tion note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs,* which covers these cases in detail.

- The port names in the SRAM Section 2.11.1.1, Timing Waveforms, SRAM Section 2.11.1.2, Timing Characteristics tables, Table 2-32, and the FIFO Section 2.11.2.2, Timing Characteristics tables were revised to ensure consistency with the software names.
- The Section 3.0, Pin Descriptions and Packaging chapter has been added.
- Package names used in the Section 4.0, Package Pin Assignments were revised to match standards given in *Package Mechanical Drawings*.

## A.10 Revision 11 - 07/2011

The following is a summary of changes in revision 11of the document:

- The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The IGLOO PLUS Device Status indicates the status for each device in the family.
- The Reprogrammable Flash Technology was revised to add "250 MHz (1.5V systems) and 160 MHz (1.2V systems) System Performance."
- The Section 1.4.7, I/Os with Advanced I/O Standards was revised to add definitions for hot-swap and cold-sparing.
- Conditional statements regarding hot insertion were removed from the description of VI in Table 2-1, since all IGLOO PLUS devices are hot insertion enabled.
- Table 2-2 was revised. 1.2V DC wide range supply voltage and 3.3V wide range supply voltage were added for VCCI. VJTAG DC Voltage was revised. The value range for VPUMP programming voltage for operation was changed from "0 to 3.45" to "0 to 3.6".
- Table 2-6 and Table 2-7 were revised.
- Table 2-8 is new.
- The tables in the Section 2.4.1, Quiescent Supply Current were updated. Some of the table notes were changed or deleted.
- VIH maximum values in tables were updated as needed to 3.6V.
- The values in the following tables were updated. 3.3V LVCMOS and 1.2V LVCMOS wide range were added to the tables where applicable.
  - Table 2-13
  - Table 2-14
  - Table 2-21
  - Table 2-22
  - Table 2-23
  - Table 2-25
  - Table 2-26
  - Table 2-28
- A table note was added to Table 2-16 and Table 2-18 stating the value for PDC4 is the minimum contribution of the PLL when operating at lowest frequency.
- Table 2-29 was revised, including addition of 3.3V and 1.2V LVCMOS wide range.
- The notes defining $R_{WEAK\ PULL\text{-}UP\text{-}MAX}$ and $R_{WEAK\ PULLDOWN\text{-}MAX}$ were revised.
- Table 2-30 was revised to include data for 3.3V and 1.2V LVCMOS wide range.
- Table 2-31 was revised to change the maximum temperature from 110 °C to 100 °C, with an example of six months instead of three months.
- The tables in the Section 2.7.4, Single-Ended I/O Characteristics were updated. Notes clarifying IIL and IIH were added.
- Tables for 3.3V LVCMOS and 1.2V LVCMOS wide range were added.
- Notes in the wide range tables state that the minimum drive strength for any LVCMOS 3.3V (or LVCMOS 1.2 V) software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
- The following sentence was deleted from the Section 2.7.4.3, 2.5V LVCMOS: It uses a 5V–tolerant input buffer and push-pull output buffer.


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- The tables in the Section 2.7.5.3, Input Register, Section 2.7.5.4, Output Register, and Section 2.7.5.5, Output Enable Register were updated. The tables in the Section 2.8, VersaTile Characteristics were updated.
- The following tables were updated in the Section 2.9.2, Global Tree Timing Characteristics:
  - Table 2-85 (1.5V)
  - Table 2-86 (1.5V)
  - Table 2-88 (1.2V)
  - Table 2-90 and Table 2-91 were revised. VCO output jitter and maximum peak-to-peak jitter data were changed. Three notes were added to the table in connection with these changes.
- *Figure 2-28 • Write Access after Write onto Same Address* and *Figure 2-29 • Write Access after Read onto Same Address* were deleted.
- The tables in the Section 2.11.1, SRAM, Section 2.11.2, FIFO, and Section 2.11.3, Embedded FlashROM Characteristics sections were updated.

## A.11 Revision 10 - 04/2009

The following is a summary of change in revision 10 of the document:

- The –F speed grade is no longer offered for IGLOO PLUS devices. References to it have been removed from the document. The speed grade column and note regarding –F speed grade were removed from IGLOO PLUS Ordering Information. The *Speed Grade and Temperature Grade Matrix* section was removed.

## A.12 Revision 9 - 02/2009

The following is a summary of change in revision 9 of the document:

- The Advanced I/O was revised to add two bullets regarding support of wide range power supply voltage.
- The Section 1.4.7, I/Os with Advanced I/O Standards was revised to add 3.0V wide range to the list of supported voltages. The Section 1.5, Wide Range I/O Support is new.

## A.13 Revision 8 - 01/2009

The following is a summary of change in revision 8 of the document:

- The Table 4-3 was revised to add a note regarding pins G1 and H1.

## A.14 Revision 7 - 12/2008

The following is a summary of changes in revision 7 of the document:

- A note was added to Table 1: "AGLP060 in CS201 does not support the PLL."
- Table 3 was updated to change the nominal size of VQ176 from 100 to 400 $mm^2$.

## A.15 Revision 6 - 10/2008

The following is a summary of changes in revision 6 of the document:

- Data was revised significantly in the following tables:
  - Table 2-25
  - Table 2-26
  - Table 2-50
  - Table 2-51

## A.16 Revision 5 - 08/2008

The following is a summary of changes in revision 5 of the document:

- The VQ128 and VQ176 packages were added to Table 1, the I/Os Per Package table, Table 3, IGLOO PLUS Ordering Information, and the Temperature Grade Offerings table.
- The Table 4-1 package drawing and pin table are new.
- The Table 4-2 package drawing and pin table are new.

## A.17 Revision 4 - 07/2008

The following is a summary of change in revision 4 of the document:

- As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2V/1.5V to 1.2V to 1.5V. "

## A.18 Revision 3 - 06/2008

The following is a summary of changes in revision 3 of the document:

- Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2V I/O set.
- Table note 3 was updated in Table 2-2 to add the sentence, "VCCI should be at the same voltage within a given I/O bank." References to table notes 5, 6, 7, and 8 were added. Reference to table note 3 was removed from VPUMP Operation and placed next to VCC.
- Table 2-4 was revised to remove "as measured on quiet I/Os" from the title. Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted.
- The table note for Table 2-9 to remove the sentence stating that values do not include I/O static contribution.
- The table note for Table 2-10 was updated to remove VJTAG and VCCI and the statement that values do not include I/O static contribution.
- The table note for Table 2-11 was updated to remove the statement that values do not include I/O static contribution.
- Note 2 of Table 2-12 was updated to include VCCPLL. Table note 4 was deleted.
- Table 2-13 and Table 2-14 were updated to remove static power. The table notes were updated to reflect that power was measured on $VCC_I$. Table note 2 was added to Table 2-13.
- Table 2-16 and Table 2-18 were updated to change the definition for $P_{DC5}$ from bank static power to bank quiescent power. Table subtitles were added for Table 2-16, Table 2-17, and Table 2-18.
- The Section 2.6.1.2, Total Static Power Consumption—PSTAT was revised.
- Table 2-32 is new.
- The Table 4-5 package drawing is new.
- The Table 4-5 table for the AGLP125 device is new.
- The Table 4-6 package drawing was incorrect. The graphic was showing the CS281 mechanical drawing and not the CS289 mechanical drawing. This has now been corrected.

## A.19 Revision 2 - 07/2008

The following is a summary of change in revision 2 of the document:

- The Table 4-6 table for the AGLP030 device is new.

## A.20 Revision 1 - 07/2008

The following is a summary of change in revision 1 of the document:

- The Table 4-7 table for the AGLP060 device is new.
- The Table 4-8 table for the AGLP125 device is new.


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ISBN: 978-1-6683-4681-5

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