ProASIC3 nano Flash FPGAs

Introduction (Ask a Question)

ProASIC® 3 nano reprogrammable and nonvolatile FPGAs are secure, low-power, instant-on, and single-chip solutions. When performance, cost, flexibility, and time to market are critical, ProASIC 3 nano devices are an attractive alternative to Application-Specific Integrated Circuits (ASICs) and Application-Specific Standard Products (ASSPs) in fast-moving or highly competitive markets. ProASIC 3 nano devices have up to 3K LEs and support up to 36 Kb of true dual-port SRAM and up to 71 user I/Os.

ProASIC 3 nano devices offer new features and smaller-footprint packages designed with two-layer PCBs in mind for greater value in high-volume consumer, portable, and battery-backed markets. Key features include low power consumption, hot-swap capability, and a Schmitt trigger for greater flexibility in low-cost and power-sensitive applications.

Features and Benefits (Ask a Question)

Wide Range of Features

- 10k to 250k System Gates
- Up to 36 kbits of True Dual-Port SRAM
- Up to 71 User I/Os

Reprogrammable Flash Technology

- 130 nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Instant On Level 0 Support
- Single-Chip Solution
- Retains Programmed Design when Powered Off

High Performance

- 350 MHz System Performance

In-System Programming (ISP) and Security

- ISP Using On-Chip 128 bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE® 1532–compliant)
- FlashLock® Designed to Secure FPGA Contents

Low Power

- Low Power ProASIC 3 nano Products
- 1.5V Core Voltage for Low Power
- Support for 1.5V-Only Systems
- Low-Impedance Flash Switches

High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure

Advanced I/Os

- 1.5V, 1.8V, 2.5V, and 3.3V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—up to 4 Banks per Chip

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- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3V/2.5V/1.8V/1.5V
- Wide Range Power Supply Voltage Support per JESD8-B, Allowing I/Os to Operate from 2.7V to 3.6V
- I/O Registers on Input, Output, and Enable Paths
- Selectable Schmitt Trigger Inputs
- Hot-Swappable and Cold-Sparing I/Os
- Programmable Output Slew Rate and Drive Strength
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the ProASIC 3 Family

Clock Conditioning Circuit (CCC) and PLL

- Up to Six CCC Blocks, One with an Integrated PLL
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range (1.5 MHz to 350 MHz)

Embedded Memory

- 1 kbit of FlashROM User Nonvolatile Memory
- SRAMs and FIFOs with Variable-Aspect-Ratio 4,608 bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations)
- True Dual-Port SRAM (except ×18 organization)

Enhanced Commercial Temperature Range

- T_j = –20 °C to +85 °C

Table 1. ProASIC 3 nano Devices

ProASIC 3 nano Devices	A3PN010	A3PN015[1]	A3PN020	A3PN060	A3PN125	A3PN250
System Gates	10,000	15,000	20,000	60,000	125,000	250,000
Typical Equivalent Macrocells	86	128	172	512	1,024	2,048
VersaTiles (D-flip-flops)	260	384	520	1,536	3,072	6,144
RAM Kbits (1,024 bits)[2]	—	—	—	18	36	36
4,608 bit Blocks[2]	—	—	—	4	8	8
FlashROM Kbits	1	1	1	1	1	1
Secure (AES) ISP[2]	—	—	—	Yes	Yes	Yes
Integrated PLL in CCCs[2]	—	—	—	1	1	1
VersaNet Globals	4	4	4	18	18	18
I/O Banks	2	3	3	2	2	4
Maximum User I/Os (packaged device)	34	49	49	71	71	68
Maximum User I/Os (Known Good Die)	34	—	52	71	71	68
Package Pins QFN VQFP	QN48	QN68	QN68	VQ100	VQ100	VQ100

Notes:

1. Not recommended for new designs. (CN1203)
2. For higher densities and support of additional features, see the ProASIC 3 Family Flash FPGAs Datasheet and ProASIC 3E Flash Family FPGAs Datasheet.

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I/Os per Package (Ask a Question)

Table 2. I/Os per Package

ProASIC 3 nano Devices	A3PN010	A3PN015[1]	A3PN020	A3PN060	A3PN125	A3PN250
Known Good Die	34	—	52	71	71	68
QN48	34	—	—	—	—	—
QN68	—	49	49	—	—	—
VQ100	—	—	—	71	71	68

Notes:

1. Not recommended for new designs. (CN1203)
2. When considering migrating your design to a lower- or higher-density device, see the ProASIC 3 FPGA Fabric User's Guideto ensure compliance with design and board migration requirements.
3. "G" indicates RoHS-compliant packages. For the location of the "G" in the part number, see ProASIC 3 nano Ordering Information . For nano devices, the VQ100 package is offered in both leaded and RoHS-compliant versions. All other packages are RoHS-compliant only.

Table 3. ProASIC 3 nano FPGAs Package Sizes Dimensions

Packages	QN48	QN68	VQ100
Length × Width (mm \ mm)	6 x 6	8 x 8	14 x 14
Nominal Area (mm^2)	36	64	196
Pitch (mm)	0.4	0.4	0.5
Height (mm)	0.90	0.90	1.20

ProASIC 3 nano Device Status (Ask a Question)

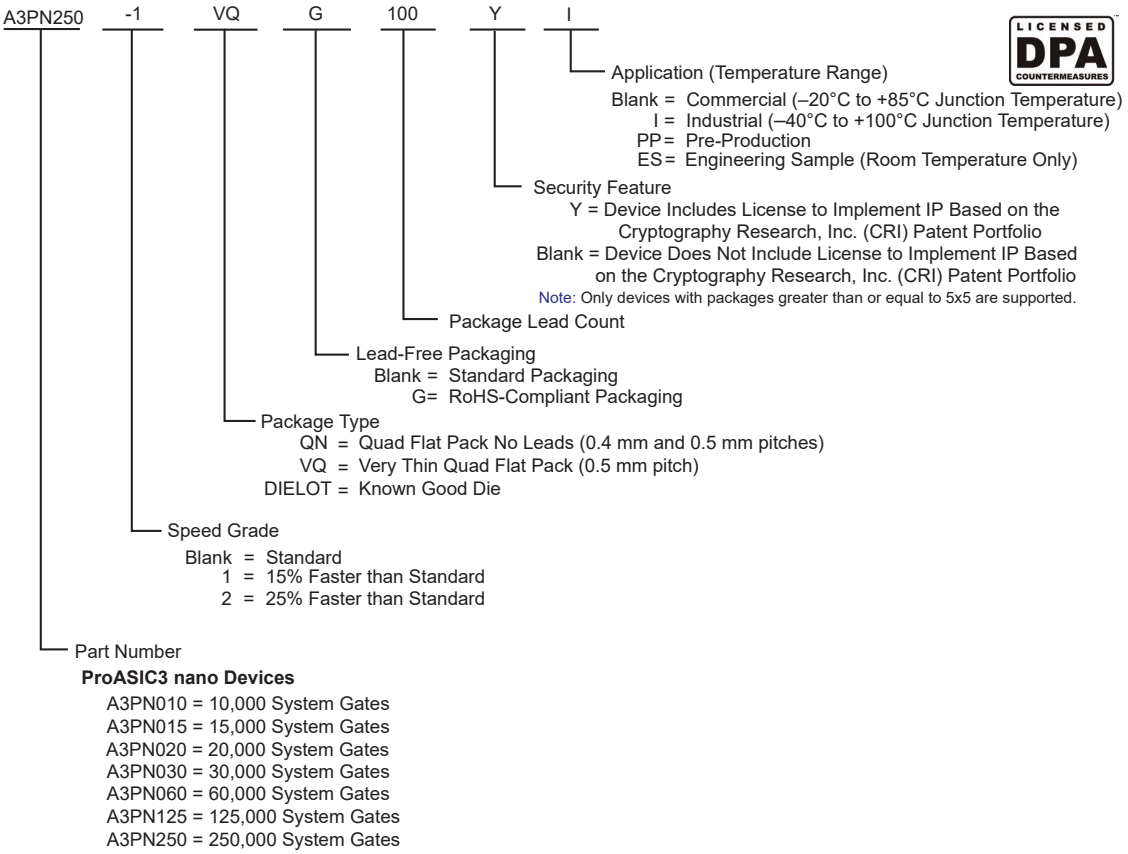
Table 4. ProASIC 3 nano Device Status

ProASIC 3 nano Devices	Status
A3PN010	Production
A3PN015	Not recommended for new designs
A3PN020	Production
A3PN060	Production
A3PN125	Production
A3PN250	Production

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ProASIC 3 nano Ordering Information (Ask a Question)

Figure 1. ProASIC 3 nano Ordering Information



Device Marking (Ask a Question)

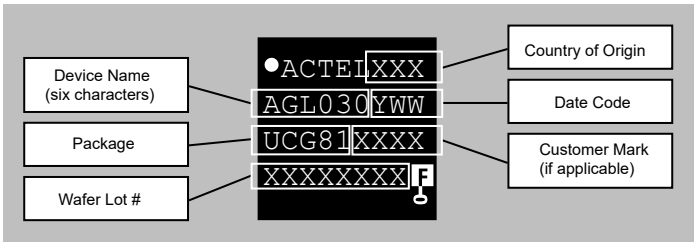
Microchip normally topside marks the full ordering part number on each device. There are some exceptions to this, such as the V2 designator for IGLOO devices, and packages where space is physically limited. Packages that have limited characters available are UC36, UC81, CS81, QN48, QN68, and QFN132. On these specific packages, a subset of the device marking will be used that includes the required legal information and as much of the part number as allowed by character limitation of the device. In this case, devices will have a truncated device marking and may exclude the applications markings, such as the I designator for Industrial Devices or the ES designator for Engineering Samples.

The following figure shows an example of device marking based on the AGL030V5-UCG81.

The actual mark will vary by the device/package combination ordered.

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Figure 2. Example of Device Marking for Small Form Factor Packages



Temperature Grade Offering (Ask a Question)

Table 5. Temperature Grade Offering

ProASIC 3 nano Devices	A3PN010	A3PN015[1]	A3PN020	A3PN060	A3PN125	A3PN250
QN48	C, I	—	—	—	—	—
QN68	—	C, I	C, I	—	—	—
VQ100	—	—	—	C, I	C, I	C, I

Note:

1. Not recommended for new designs.

C = Enhanced Commercial temperature range: –20 °C to +85 °C junction temperature.

I = Industrial temperature range: –40 °C to +100 °C junction temperature.

Speed Grade and Temperature Grade Matrix (Ask a Question)

Table 6. Speed Grade and Temperature Grade Matrix

Temperature Grade	Std.
C [1]	✓
I [2]	✓

Notes:

1. C = Enhanced Commercial temperature range: –20 °C to +85 °C junction temperature.
2. I = Industrial temperature range: –40 °C to +100 °C junction temperature.

Contact your local Microchip representative for device availability:

www.microchip.com/en-us/about/global-sales-and-distribution.

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1. ProASIC 3 nano Device Overview (Ask a Question)

1.1 General Description (Ask a Question)

ProASIC 3, the third-generation family of Microchip flash FPGAs, offers performance, density, and features beyond those of the ProASIC$^{PLUS®}$ family. Nonvolatile flash technology gives ProASIC 3 nano devices the advantage of being a secure, low power, single-chip solution that is Instant On. ProASIC 3 nano devices are reprogrammable and offer time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC 3 nano devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). A3PN030 and smaller devices do not have PLL or RAM support. ProASIC 3 nano devices have up to 250,000 system gates, supported with up to 36 kbits of true dual-port SRAM and up to 71 user I/Os.

ProASIC 3 nano devices increase the breadth of the ProASIC 3 product line by adding new features and packages for greater customer value in high volume consumer, portable, and battery-backed markets. Added features include smaller footprint packages designed with two-layer PCBs in mind, low power, hot-swap capability, and Schmitt trigger for greater flexibility in low-cost and power-sensitive applications.

1.1.1 Flash Advantages (Ask a Question)

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based ProASIC 3 nano devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property (IP) cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC 3 nano device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC 3 nano device a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

With a variety of devices under $1, ProASIC 3 nano FPGAs enable cost-effective implementation of programmable logic and quick time to market.

Security

Nonvolatile, flash-based ProASIC 3 nano devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. ProASIC 3 nano devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

ProASIC 3 nano devices utilize a 128 bit flash-based lock and a separate AES key to provide the highest level of protection in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in ProASIC 3 nano devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. ProASIC 3 nano devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC 3 nano devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

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Security, built into the FPGA fabric, is an inherent component of ProASIC 3 nano devices. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. ProASIC 3 nano devices, with FlashLock and AES security, are unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. A ProASIC 3 nano device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based ProASIC 3 nano FPGAs do not require system configuration components such as EEPROMs or micro-controllers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Instant On

Microchip flash-based ProASIC 3 nano devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based ProASIC 3 nano devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs that are used for these purposes in a system. In addition, glitches and brownouts in system power will not corrupt the ProASIC 3 nano device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC 3 nano devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of ProASIC 3 nano flash-based FPGAs. Once it is programmed, the flash cell configuration element of ProASIC 3 nano FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using Error Detection and Correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based ProASIC 3 nano devices exhibit power characteristics similar to an ASIC, making them an ideal choice for power-sensitive applications. ProASIC 3 nano devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

ProASIC 3 nano devices also have low dynamic power consumption to further maximize power savings.

1.1.2 Advanced Flash Technology (Ask a Question)

ProASIC 3 nano devices offer many benefits, including non-volatility and reprogrammability through an advanced flash-based, 130 nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

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1.1.3 Advanced Architecture (Ask a Question)

The proprietary ProASIC 3 nano architecture provides granularity comparable to standard-cell ASICs. The ProASIC 3 nano device consists of five distinct and programmable architectural features (Figure 1-3 to Figure 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- Advanced I/O structure

Figure 1-1. ProASIC 3 Device Architecture Overview with Two I/O Banks and No RAM (A3PN010 and A3PN030)

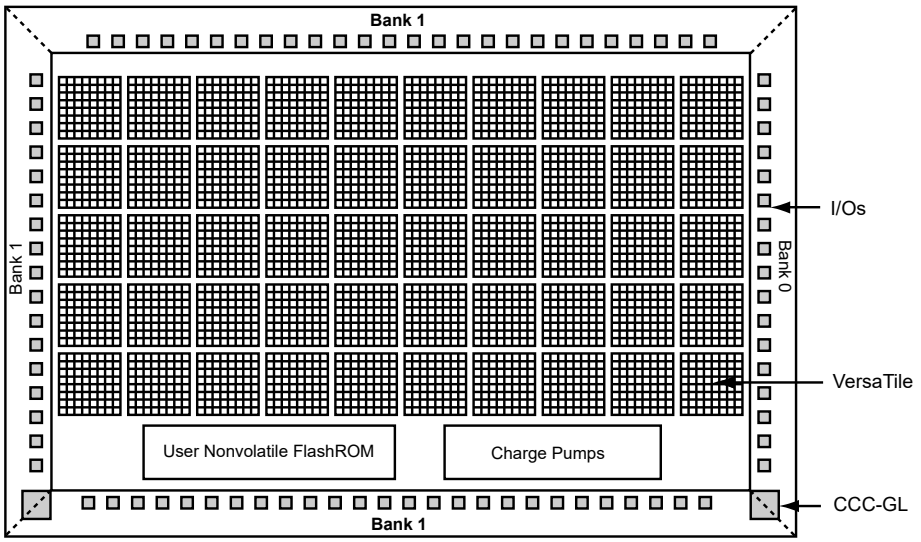
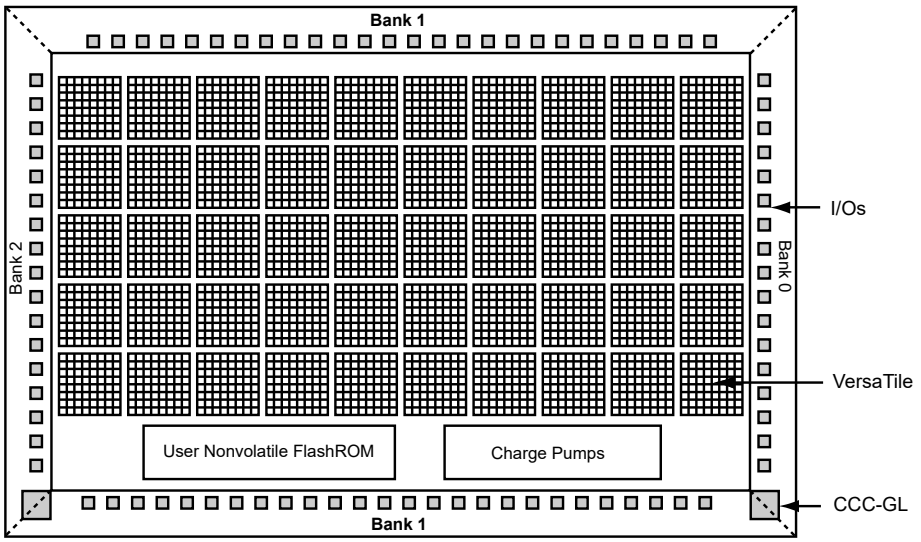


Figure 1-2. ProASIC 3 nano Architecture Overview with Three I/O Banks and No RAM (A3PN015 and A3PN020)



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Figure 1-3. ProASIC 3 nano Device Architecture Overview with Two I/O Banks (A3PN060 and A3PN125)

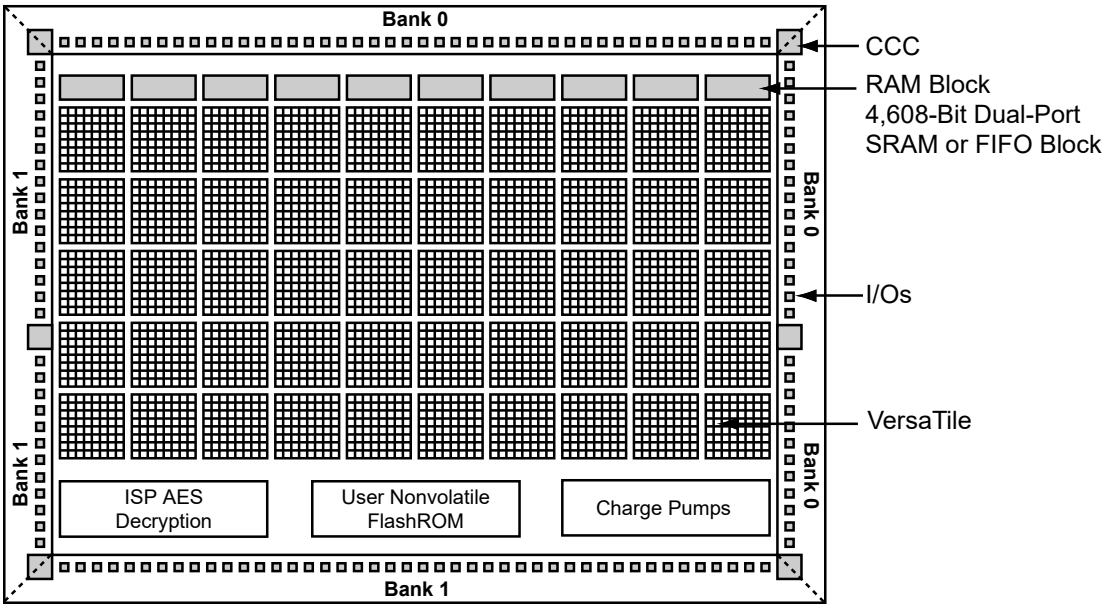
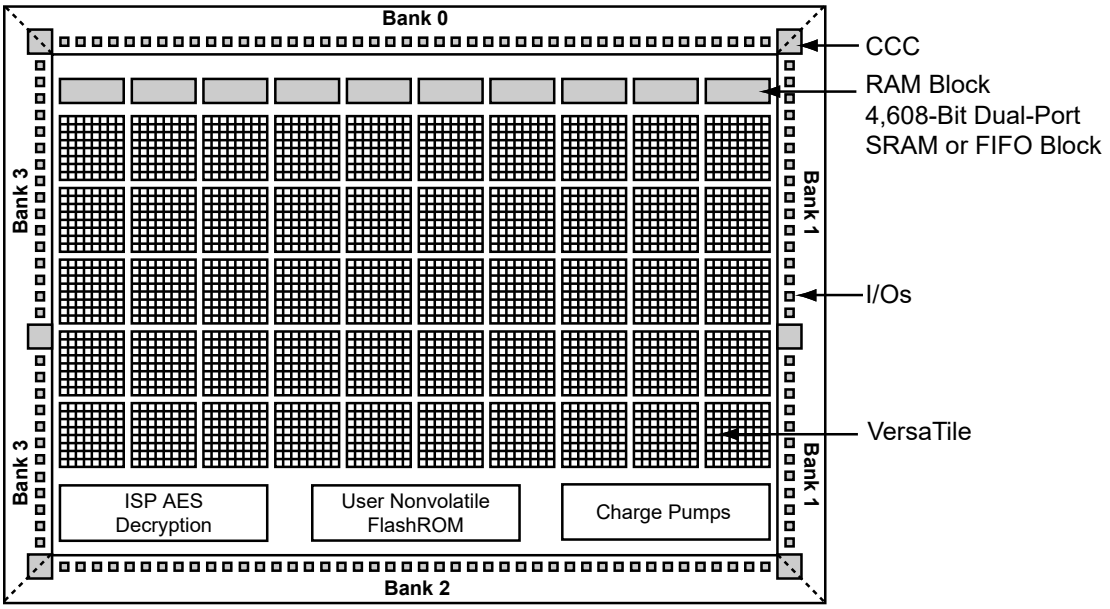


Figure 1-4. ProASIC 3 nano Device Architecture Overview with Four I/O Banks (A3PN250)



The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC 3 nano core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC 3 family of third-generation architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

VersaTiles

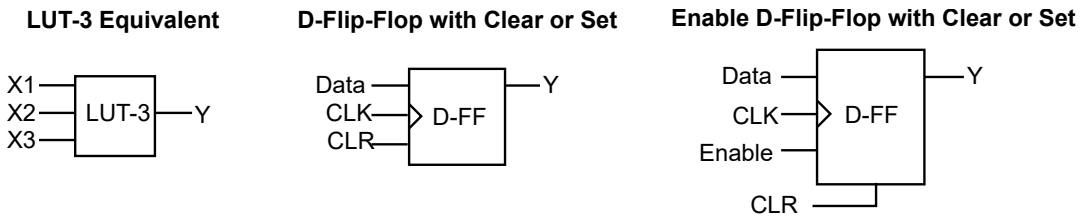
The ProASIC 3 nano core consists of VersaTiles, which have been enhanced beyond the ProASIC$^{PLUS®}$ core tiles. The ProASIC 3 nano VersaTile supports the following:

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- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

The following figure shows the VersaTile configurations.

Figure 1-5. VersaTile Configurations



User Nonvolatile FlashROM

ProASIC 3 nano devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC 3 nano IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the A3PN030 and smaller devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7 bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC 3 nano development software solutions, Libero® System-on-Chip (SoC) software and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature enables the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

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SRAM and FIFO

ProASIC 3 nano devices (except the A3PN030 and smaller devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4 bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in A3PN030 and smaller devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

Higher density ProASIC 3 nano devices using either the two I/O bank or four I/O bank architectures provide the designer with very flexible clock conditioning capabilities. A3PN060, A3PN125, and A3PN250 contain six CCCs. One CCC (center west side) has a PLL. The A3PN030 and smaller devices use different CCCs in their architecture. These CCC-GLs contain a global MUX but do not have any PLLs or programmable delays.

For devices using the six CCC block architecture, these six CCC blocks are located at the four corners and the centers of the east and west sides.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access. The inputs of the six CCC blocks are accessible from the FPGA core or from dedicated connections to the CCC block, which are located near the CCC.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from –7.56 ns to +11.12 ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time = 300 µs (for PLL only)
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × (350 MHz / f_{OUT_CCC}) (for PLL only)

Global Clocking

ProASIC 3 nano devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

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Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high fanout nets.

I/Os with Advanced I/O Standards

ProASIC 3 nano FPGAs feature a flexible I/O structure, supporting a range of voltages (1.5V, 1.8V, 2.5V, and 3.3V).

The I/Os are organized into banks, with two, three, or four banks per device. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of various single-data-rate applications for all versions of nano devices and double-data-rate applications for the A3PN060, A3PN125, and A3PN250 devices.

ProASIC 3 nano devices support LVTTL and LVCMOS I/O standards, are hot-swappable, and support cold-sparing and Schmitt trigger.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

1.1.4 Wide Range I/O Support (Ask a Question)

ProASIC 3 nano devices support JEDEC-defined wide range I/O operation. ProASIC 3 nano supports the JESD8-B specification, covering both 3V and 3.3V supplies, for an effective operating range of 2.7V to 3.6V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

1.1.5 Specifying I/O States During Programming (Ask a Question)

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the FlashPro User's Guide for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

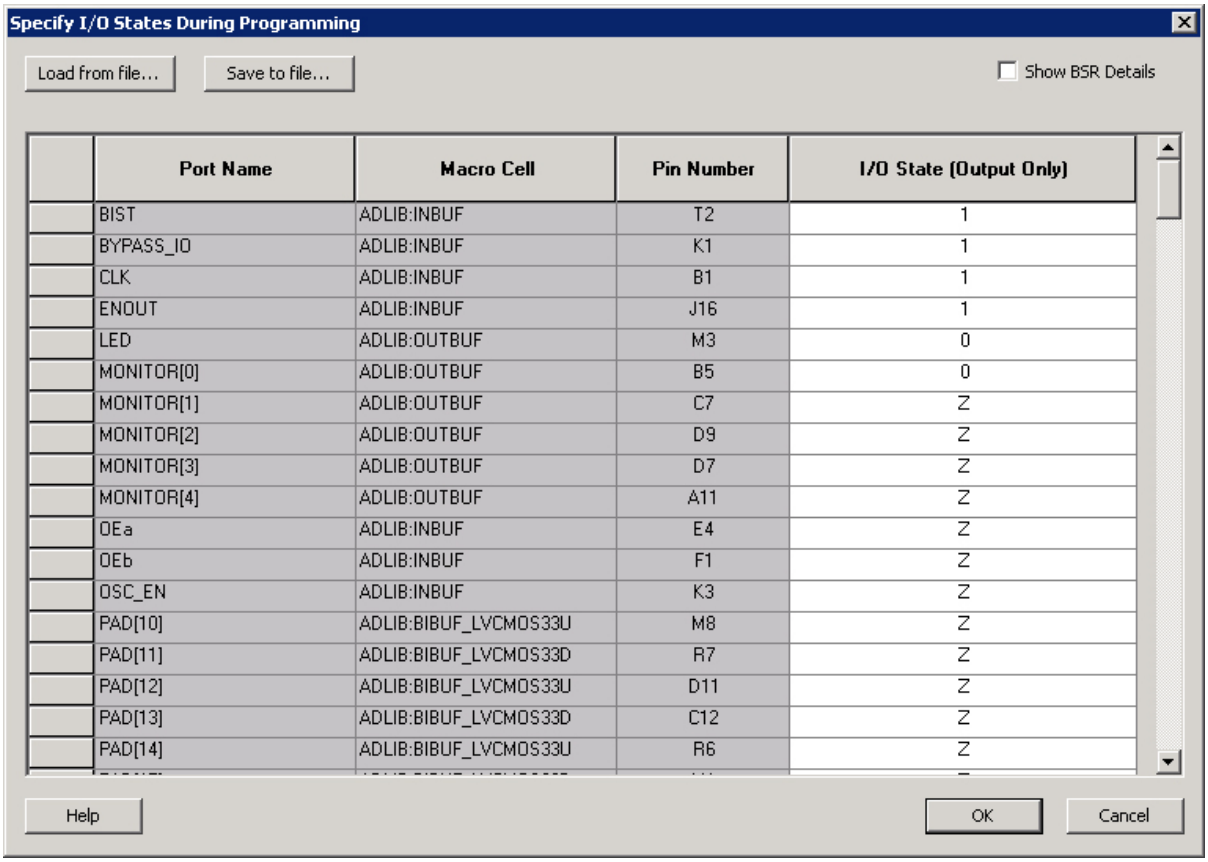
1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-6).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:
   1: I/O is set to drive out logic High
   0: I/O is set to drive out logic Low

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Last Known State: I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

Z -Tri-State: I/O is tristated

Figure 1-6. I/O States During Programming Window



6. Click **OK** to return to the FlashPoint – Programming File Generator window.

I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

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2. ProASIC 3 nano DC and Switching Characteristics (Ask a Question)

2.1 General Specification (Ask a Question)

DC and switching characteristics for –F speed grade targets are based only on simulation.

The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.

2.1.1 Operating Conditions (Ask a Question)

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 is not implied.

Table 2-1. Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 to 3.6	V
T_{STG}[1]	Storage temperature	–65 to +150	°C
T_J[1]	Junction temperature	+125	°C

Notes:

1. For flash programming and retention maximum limits, see Table 2-3, and for recommended operating limits, see Table 2-2.
2. VMV pins must be connected to the corresponding VCCI pins. For more information, see 3.1. VMVx I/O Supply Voltage (Quiet) for further information.
3. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4.

Table 2-2. Recommended Operating Conditions [1, 2]

Symbol	Parameter		Extended Commercial	Industrial	Units
T_J	Junction temperature		–20 to +85[2]	–40 to +100[2]	°C
VCC[3]	1.5V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP[4]	Programming voltage	Programming Mode[4]	3.15 to 3.45	3.15 to 3.45	V
		Operation[5]	0 to 3.6	0 to 3.6	V
VCCPLL[6]	Analog power supply (PLL)	1.5V DC core supply voltage[3]	1.425 to 1.575	1.425 to 1.575	V
VCCI and VMV[7]	1.5V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	3.3V Wide Range supply voltage[8]		2.7 to 3.6	2.7 to 3.6	V

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Notes:

1. All parameters representing voltages are measured with respect to GND unless otherwise specified.
2. Default Junction Temperature Range in the Libero SoC software is set to 0 °C to +70 °C for commercial, and -40 °C to +85 °C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microchip recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, see the New Project Dialog Box in the Libero Online Help.
3. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-14. VMV and VCCI should be at the same voltage within a given I/O bank.
4. The programming temperature range supported is Tambient = 0 °C to 85 °C.
5. VPUMP can be left floating during operation (not programming mode).
6. VCCPLL pins should be tied to VCC pins. See the 3. Pin Descriptions and Packaging chapter for further information.
7. VMV pins must be connected to the corresponding VCCI pins. See the 3. Pin Descriptions and Packaging chapter for further information.
8. 3.3V Wide Range is compliant to the JESD8-B specification and supports 3.0V VCCI operation.

Table 2-3. Flash Programming Limits—Retention, Storage and Operating Temperature[1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C)[2]	Maximum Operating Junction Temperature T_J (°C)[2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. This is a stress rating only; functional operation at any condition other than those indicated is not implied.
2. These limits apply for program/data retention only. For device operating conditions and absolute limits, see Table 2-1 and Table 2-2 .

Table 2-4. Overshoot and Undershoot Limits [1]

VCCI and VMV	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7V or less	10%	1.4V
	5%	1.49V
3V	10%	1.1V
	5%	1.19V
3.3V	10%	0.79V
	5%	0.88V
3.6V	10%	0.45V
	5%	0.54V

Notes:

1. Based on reliability requirements at 85 °C.
2. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15V.

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2.1.2 I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial) (Ask a Question)

Sophisticated power-up management circuitry is designed into every ProASIC® 3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1.

There are five regions to consider during power-up.

ProASIC 3 I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1).
2. VCCI > VCC – 0.75V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:

Ramping up: 0.6V < trip_point_up < 1.2V
Ramping down: 0.5V < trip_point_down < 1.1V

VCC Trip Point:

Ramping up: 0.6V < trip_point_up < 1.1V
Ramping down: 0.5V < trip_point_down < 1V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior

PLL Behavior at Brownout Condition

Microchip recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLLX exceed brownout activation levels. The VCC activation level is specified as 1.1V worst-case (see Figure 2-1 for more details).

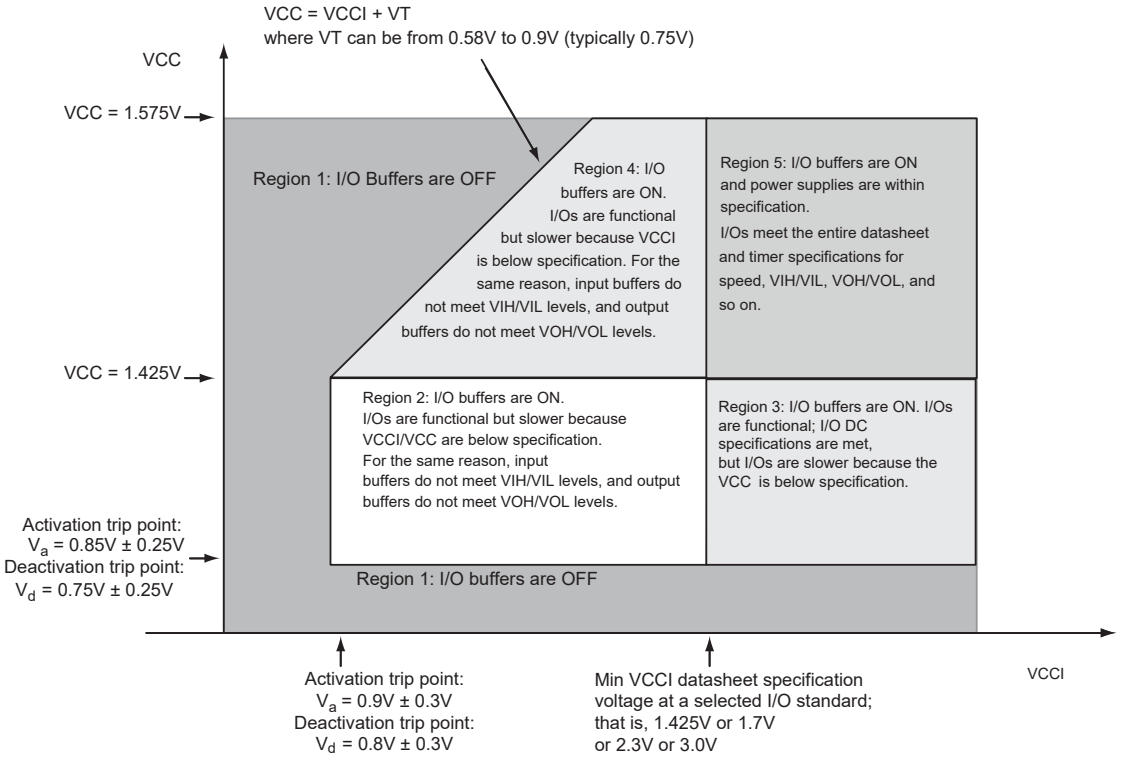
When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75V ± 0.25V), the PLL output lock signal goes low and/or the output clock is lost. For information on clock and lock recovery, see the “Power-Up/-Down Behavior of Low Power Flash Devices” chapter of the ProASIC 3 nano FPGA Fabric User’s Guide.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

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Figure 2-1. I/O State as a Function of VCCI and VCC Voltage Levels



2.1.3 Thermal Characteristics (Ask a Question)

2.1.3.1 Introduction (Ask a Question)

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

The following equation can be used to calculate junction temperature.

T_J = Junction Temperature = $\Delta T + T_A$

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-5.

P = Power dissipation

2.1.3.2 Package Thermal Characteristics (Ask a Question)

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 100 °C. The following equation shows a sample calculation of the absolute maximum power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

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$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{100\text{°C} - 70\text{°C}}{20.5\text{°C/W}} = 1.463\ \text{W}$$

Table 2-5. Package Thermal Resistivities

Package Type	Device	Pin Count	θ_{jc}	θ_{ja}			Units
				Still Air	200 ft./min.	500 ft./min.	
Quad Flat No Lead (QFN)	All devices	48	—	—	—	—	C/W
		68	—	—	—	—	C/W
		100	—	—	—	—	C/W
Very Thin Quad Flat Pack (VQFP)	All devices	100	10.0	35.3	29.4	27.1	C/W

2.1.3.3 Temperature and Voltage Derating Factors (Ask a Question)

Table 2-6. Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70 °C, VCC = 1.425V)

Array Voltage VCC (V)	Junction Temperature (°C)						
	–40 °C	–20 °C	0 °C	25 °C	70 °C	85 °C	100 °C
1.425	0.968	0.973	0.979	0.991	1.000	1.006	1.013
1.500	0.888	0.894	0.899	0.910	0.919	0.924	0.930
1.575	0.836	0.841	0.845	0.856	0.864	0.870	0.875

2.2 Calculating Power Dissipation (Ask a Question)

2.2.1 Quiescent Supply Current (Ask a Question)

Table 2-7. Quiescent Supply Current Characteristics

	A3PN010	A3PN015	A3PN020	A3PN060	A3PN125	A3PN250
Typical (25 °C)	600 µA	1 mA	1 mA	2 mA	2 mA	3 mA
Max. (Commercial)	5 mA	5 mA	5 mA	10 mA	10 mA	20 mA
Max. (Industrial)	8 mA	8 mA	8 mA	15 mA	15 mA	30 mA

Note: IDD includes VCC, VPUMP, and VCCI currents.

2.2.2 Power per I/O Pin (Ask a Question)

Table 2-8. Summary of I/O Input Buffer Power (Per Pin)—Default I/O Software Settings

	VCCI (V)	Dynamic Power, PAC9 (µW/MHz)[1]
Single-Ended		
3.3V LVTTL/3.3V LVCMOS	3.3	16.45
3.3V LVTTL/3.3V LVCMOS – Schmitt Trigger	3.3	18.93
3.3V LVCMOS wide range[2]	3.3	16.45
3.3V LVCMOS wide range – Schmitt Trigger	3.3	18.93
2.5V LVCMOS	2.5	4.73
2.5V LVCMOS – Schmitt Trigger	2.5	6.14
1.8V LVCMOS	1.8	1.68
1.8V LVCMOS – Schmitt Trigger	1.8	1.80
1.5V LVCMOS (JESD8-11)	1.5	0.99
1.5V LVCMOS (JESD8-11) – Schmitt Trigger	1.5	0.96

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Notes:

1. PAC9 is the total dynamic power measured on VCCI.
2. All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD8-B specification.

Table 2-9. Summary of I/O Output Buffer Power (per pin)—Default I/O Software Settings[1]

	C_{LOAD} (pF)[2]	VCCI (V)	Dynamic Power, PAC10 (µW/MHz)[3]
Single-Ended			
3.3V LVTTL/3.3V LVCMOS	10	3.3	162.01
3.3V LVCMOS wide range[4]	10	3.3	162.01
2.5V LVCMOS	10	2.5	91.96
1.8V LVCMOS	10	1.8	46.95
1.5V LVCMOS (JESD8-11)	10	1.5	32.22

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. Values for A3PN020, A3PN015, and A3PN010. A3PN060, A3PN125, and A3PN250 correspond to a default loading of 35 pF.
3. PAC10 is the total dynamic power measured on VCCI.
4. All LVCMOS3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD8-B specification.

2.2.3 Power Consumption of Various Internal Resources (Ask a Question)

Table 2-10. Different Components Contributing to Dynamic Power Consumption in ProASIC 3 nano Devices

Parameter	Definition	Device Specific Dynamic Contributions (µW/MHz)					
		A3PN250	A3PN125	A3PN060	A3PN020	A3PN015	A3PN010
PAC1	Clock contribution of a Global Rib	11.03	11.03	9.3	9.3	9.3	9.3
PAC2	Clock contribution of a Global Spine	1.58	0.81	0.81	0.4	0.4	0.4
PAC3	Clock contribution of a VersaTile row	0.81					
PAC4	Clock contribution of a VersaTile used as a sequential module	0.12					
PAC5	First contribution of a VersaTile used as a sequential module	0.07					
PAC6	Second contribution of a VersaTile used as a sequential module	0.29					
PAC7	Contribution of a VersaTile used as a combinatorial Module	0.29					
PAC8	Average contribution of a routing net	0.70					
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-8.					
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-9.					
PAC11	Average contribution of a RAM block during a read operation	25.00			N/A		
PAC12	Average contribution of a RAM block during a write operation	30.00			N/A		
PAC13	Dynamic contribution for PLL	2.60			N/A	N/A	N/A

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Note: For a different output load, drive strength, or slew rate, Microchip recommends using the Microchip Power spreadsheet calculator or SmartPower tool in Libero SoC.

Table 2-11. Different Components Contributing to the Static Power Consumption in ProASIC 3 nano Devices

Parameter	Definition	Device Specific Static Power (mW)					
		A3PN250	A3PN125	A3PN060	A3PN020	A3PN015	A3PN010
PDC1	Array static power in Active mode	See Table 2-7					
PDC4	Static PLL contribution [1]	2.55			N/A		
PDC5	Bank quiescent power (VCCI -dependent)	See Table 2-7					

Notes:

1. Minimum contribution of the PLL when running at lowest frequency.
2. For a different output load, drive strength, or slew rate, Microchip recommends using the Microchip Power spreadsheet calculator or SmartPower tool in Libero SoC.

2.2.4 Power Calculation Methodology (Ask a Question)

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-12.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-13.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-13. The calculation should be repeated for each clock domain defined in the design.

2.2.4.1 Methodology (Ask a Question)

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

$P_{STAT} = PDC1 + N_{INPUTS} * PDC2 + N_{OUTPUTS} * PDC3$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the “Spine Architecture” section of the Global Resources chapter in the ProASIC 3 nano FPGA Fabric User's Guide.

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N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the ProASIC 3 nano FPGA Fabric User's Guide.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-12.

F_{CLK} is the global clock signal frequency.

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-12.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-12.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-12.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-12.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-13.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

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β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-13.

PLL Contribution—P_{PLL}

$P_{PLL} = PDC4 + PAC13 * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.[1]

Note:

1. The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.

2.2.4.2 Guidelines (Ask a Question)

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8 bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - ...
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-12. Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-13. Enable Rate Guidelines Recommended for Power Calculation

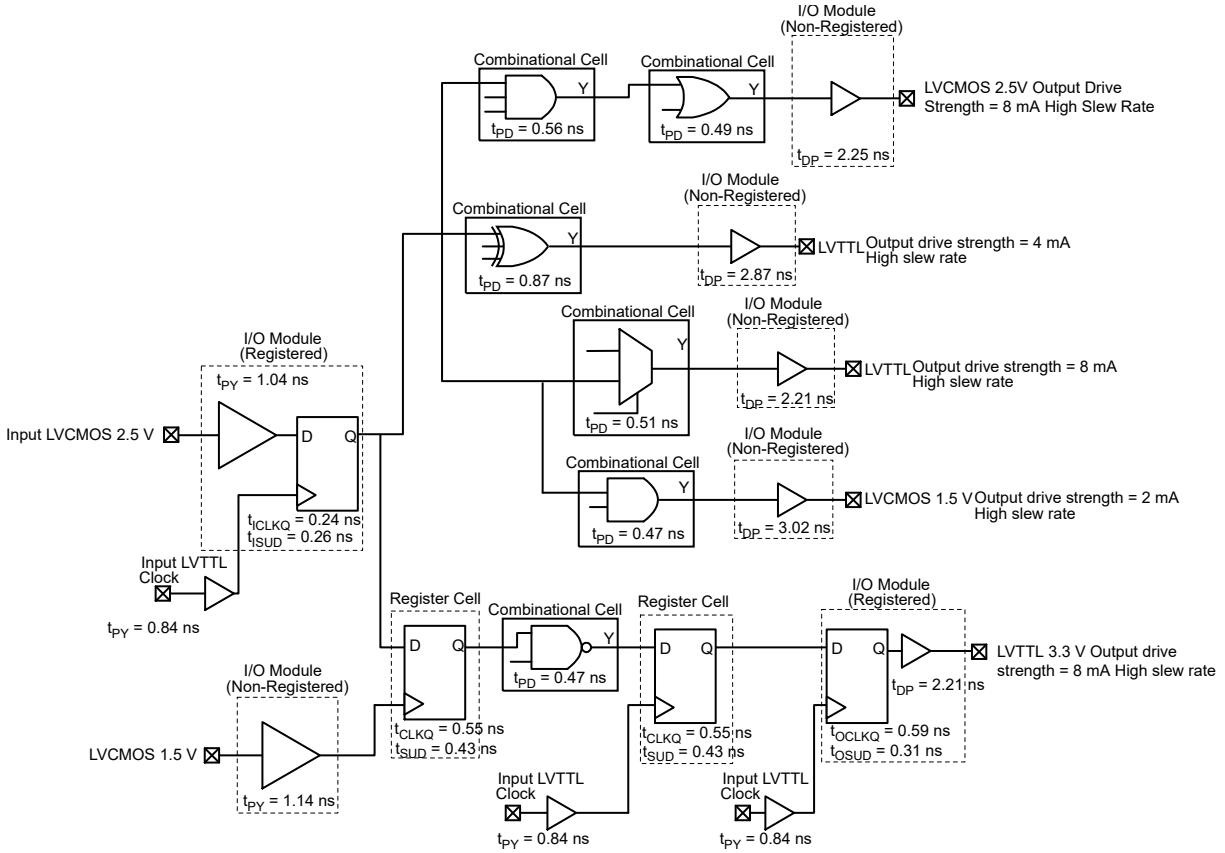
Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

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2.3 User I/O Characteristics (Ask a Question)

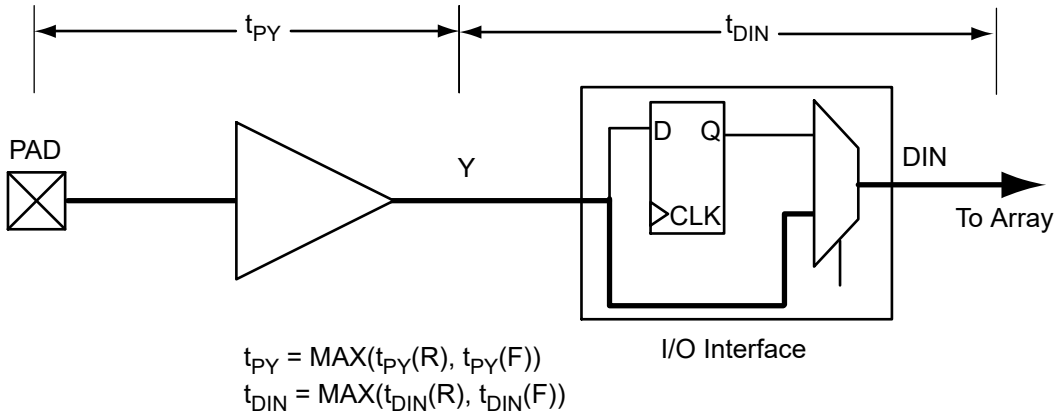
2.3.1 Timing Model (Ask a Question)

Figure 2-2. Timing Model —Operating Conditions: –2 Speed, Commercial Temperature Range (T_J = 70 °C), Worst Case VCC = 1.425V, with Default Loading at 10 pF

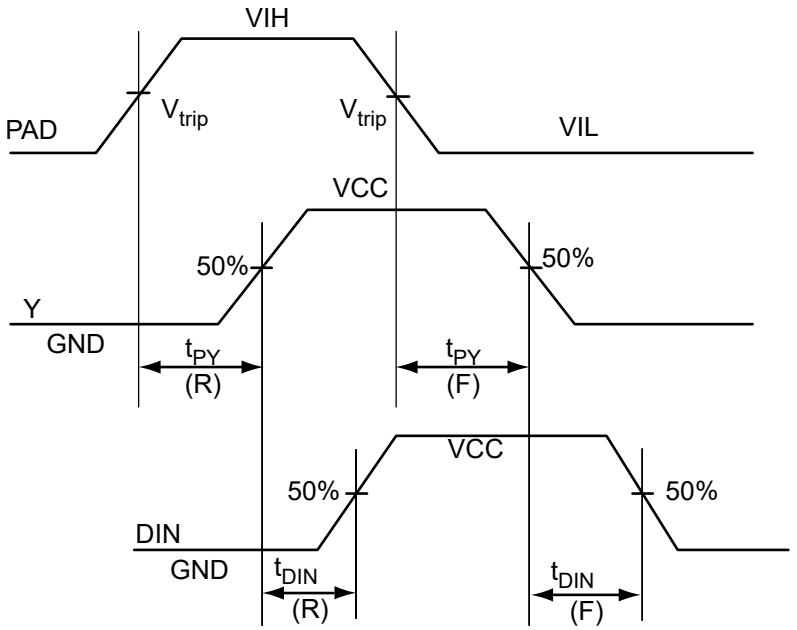


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Figure 2-3. Input Buffer Timing Model and Delays (example)

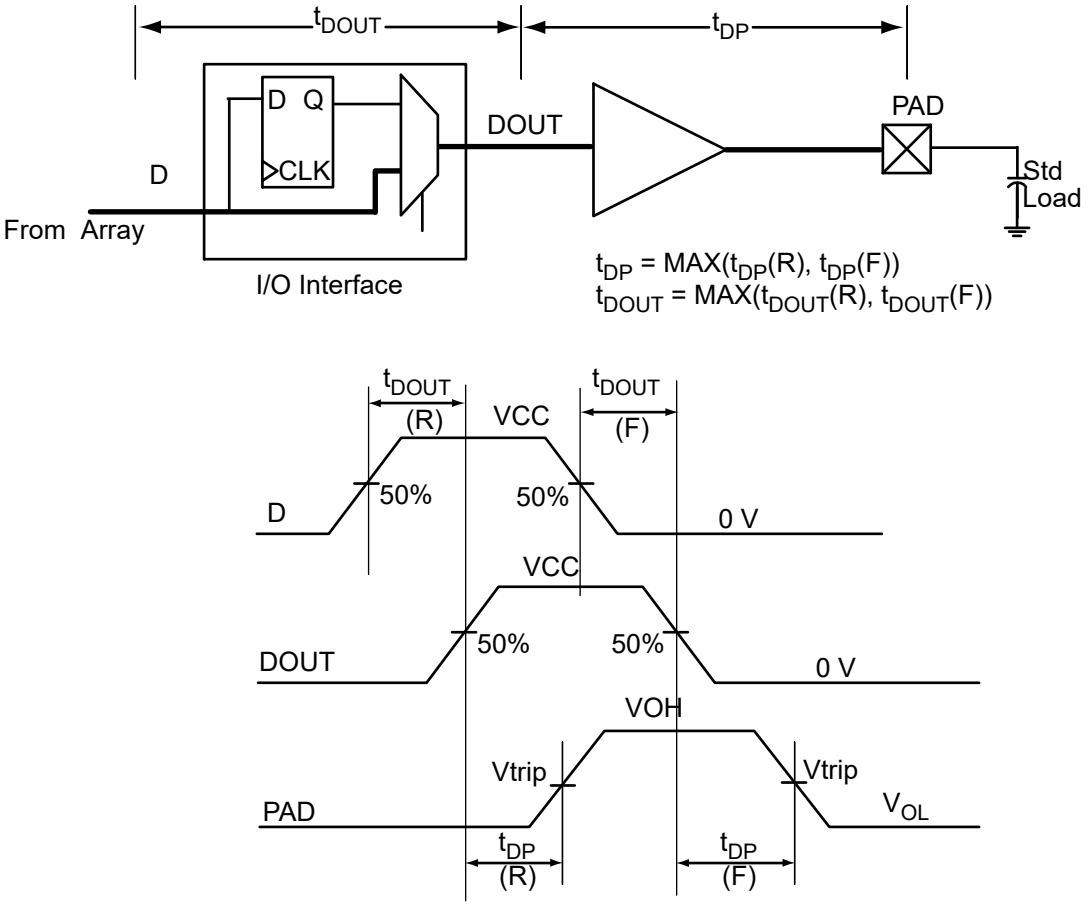


$t_{PY} = MAX(t_{PY}(R), t_{PY}(F))$
$t_{DIN} = MAX(t_{DIN}(R), t_{DIN}(F))$



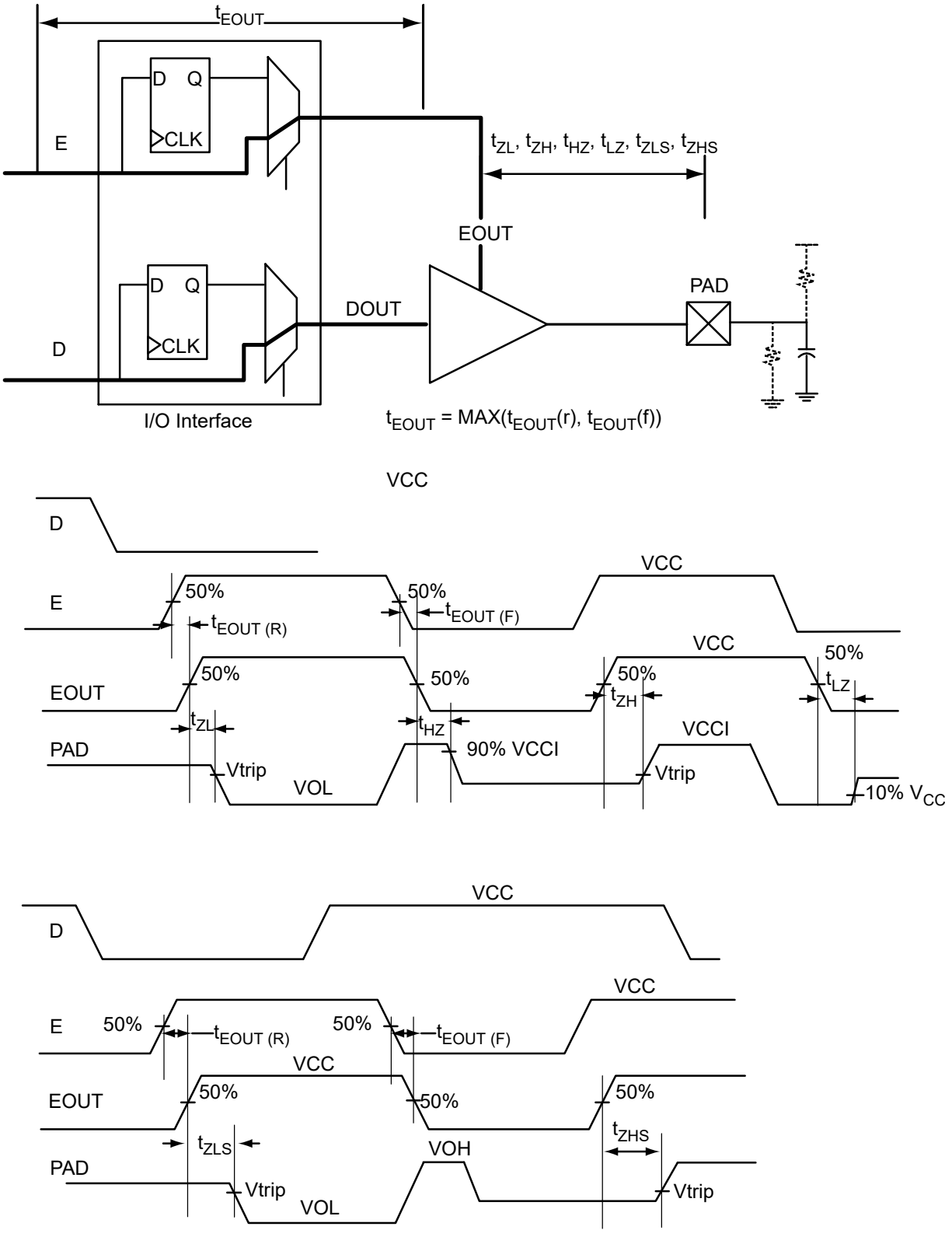
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Figure 2-4. Output Buffer Model and Delays (example)



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Figure 2-5. Tristate Output Buffer Timing Model and Delays (example)



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2.3.2 Overview of I/O Performance (Ask a Question)

2.3.2.1 Summary of I/O DC Input and Output Levels—Default I/O Software Settings (Ask a Question)

Table 2-14. Summary of Maximum and Minimum DC Input and Output Levels—Applicable to Commercial and Industrial Conditions—Software Default Settings

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[2]	Slew Rate	VIL		VIH		VOL	VOH	IOL[1]	IOH[1]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3V LVTTL/ 3.3V LVCMOS	8 mA	8 mA	High	–0.3	0.8	2	3.6	0.4	2.4	8	8
3.3V LVCMOS Wide Range	100 µA	8 mA	High	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100 µA	100 µA
2.5V LVCMOS	8 mA	8 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8V LVCMOS	4 mA	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4
1.5V LVCMOS	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2

Notes:

1. Currents are measured at 85 °C junction temperature.
2. The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.
3. All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range, as specified in the JESD8-B specification.

Table 2-15. Summary of Maximum and Minimum DC Input Levels—Applicable to Commercial and Industrial Conditions

DC I/O Standards	Commercial[1]		Industrial[2]	
	IIL[3]	IIH[4]	IIL[3]	IIH[4]
	µA	µA	µA	µA
3.3V LVTTL/3.3V LVCMOS	10	10	15	15
3.3V LVCMOS Wide Range	10	10	15	15
2.5V LVCMOS	10	10	15	15
1.8V LVCMOS	10	10	15	15
1.5V LVCMOS	10	10	15	15

Notes:

1. Commercial range (–20 °C < T_A < 70 °C)
2. Industrial range (–40 °C < T_A < 85 °C)
3. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.
4. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

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2.3.2.2 Summary of I/O Timing Characteristics—Default I/O Software Settings (Ask a Question)

Table 2-16. Summary of AC Measuring Points

Standard	Measuring Trip Point (Vtrip)
3.3V LVTTL/3.3V LVCMOS	1.4V
3.3V LVCMOS Wide Range	1.4V
2.5V LVCMOS	1.2V
1.8V LVCMOS	0.90V
1.5V LVCMOS	0.75V

Table 2-17. I/O AC Parameter Definitions

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—HIGH to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to HIGH
t_{LZ}	Enable to Pad delay through the Output Buffer—LOW to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to LOW
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to HIGH
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to LOW

Table 2-18. Summary of I/O Timing Characteristics—Software Default Settings (at 35 pF)—STD Speed Grade, Commercial-Case Conditions: T_J = 70 °C, Worst Case VCC = 1.425V—For A3PN060, A3PN125, and A3PN250

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)
3.3V LVTTL/ 3.3V LVCMOS	8	8 mA	High	35	0.60	4.57	0.04	1.13	1.52	0.43	4.64	3.92	2.60	3.14
3.3V LVCMOS Wide Range	100 µA	8 mA	High	35	0.60	6.78	0.04	1.57	2.18	0.43	6.78	5.72	3.72	4.35
2.5V LVCMOS	8	8 mA	High	35	0.60	4.94	0.04	1.43	1.63	0.43	4.71	4.94	2.60	2.98
1.8V LVCMOS	4	4 mA	High	35	0.60	6.53	0.04	1.35	1.90	0.43	5.53	6.53	2.62	2.89
1.5V LVCMOS	2	2 mA	High	35	0.60	7.86	0.04	1.56	2.14	0.43	6.45	7.86	2.66	2.83

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Notes:

1. The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.
2. All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range, as specified in the JESD8-B specification.
3. For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

Table 2-19. Summary of I/O Timing Characteristics—Software Default Settings (at 10 pF)—STD Speed Grade, Commercial-Case Conditions: TJ = 70 °C, Worst Case VCC = 1.425V—For A3PN020, A3PN015 and A3PN010

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)
3.3V LVTTL/3.3V LVCMOS	8	8 mA	High	10	0.60	2.73	0.04	1.13	1.52	0.43	2.77	2.23	2.60	3.14
3.3V LVCMOS Wide Range	100 µA	8 mA	High	10	0.60	3.94	0.04	1.57	2.18	0.43	3.94	3.16	3.72	4.35
2.5V LVCMOS	8	8 mA	High	10	0.60	2.76	0.04	1.43	1.63	0.43	2.80	2.60	2.60	2.98
1.8V LVCMOS	4	4 mA	High	10	0.60	3.22	0.04	1.35	1.90	0.43	3.24	3.22	2.62	2.89
1.5V LVCMOS	2	2 mA	High	10	0.60	3.76	0.04	1.56	2.14	0.43	3.74	3.76	2.66	2.83

Notes:

1. The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.
2. All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range, as specified in the JESD8-B specification.
3. For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.3 Detailed I/O DC Characteristics (Ask a Question)

Table 2-20. Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz	—	8	pF
C_{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz	—	8	pF

Table 2-21. I/O Output Buffer Maximum Resistances [1]

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3V LVTTL/3.3V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
3.3V LVCMOS Wide Range	100 µA	Same as equivalent software default drive	

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.....continued			
Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω)[2]	$R_{PULL-UP}$ (Ω)[3]
2.5V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5V LVCMOS	2 mA	200	224

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models, located at www.microchip.com/en-us/products/fpgas-and-plds/fpgas/proasic-3-fpgas#ibis.
2. $R_{(PULL-DOWN-MAX)}$ = (VOLspec) / IOLspec
3. $R_{(PULL-UP-MAX)}$ = (VCCImax – VOHspec) / IOHspec

Table 2-22. I/O Weak Pull-Up/Pull-Down Resistances—Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	$R_{(WEAK\ PULL-UP)}$[1] (Ω)		$R_{(WEAK\ PULL-DOWN)}$[2] (Ω)	
VCCI	Min.	Max.	Min.	Max.
3.3V	10K	45K	10K	45K
3.3V (wide range I/Os)	10K	45K	10K	45K
2.5V	11K	55K	12K	74K
1.8V	18K	70K	17K	110K
1.5V	19K	90K	19K	140K

Notes:

1. $R_{(WEAK\ PULL-UP-MAX)}$ = (VCCImax – VOHspec) / $I_{(WEAK\ PULL-UP-MIN)}$
2. $R_{(WEAK\ PULLDOWN-MAX)}$ = (VOLspec) / $I_{(WEAK\ PULLDOWN-MIN)}$

Table 2-23. I/O Short Currents IOSH/IOSL

	Drive Strength	IOSL (mA)[1]	IOSH (mA)[1]
3.3V LVTTL/3.3V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
3.3V LVCMOS Wide Range	100 µA	Same as equivalent software default drive	
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
1.5 V LVCMOS	2 mA	13	16

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Note:

1. T_J = 100 °C

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3V, 8 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100 °C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-24. Duration of Short Circuit Event before Failure

Temperature	Time before Failure
–40 °C	> 20 years
–20 °C	> 20 years
0 °C	> 20 years
25 °C	> 20 years
70 °C	5 years
85 °C	2 years
100 °C	6 months

Table 2-25. Schmitt Trigger Input Hysteresis—Hysteresis Voltage Value (Typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3V LVTTL/LVCMOS (Schmitt trigger mode)	240 mV
2.5V LVCMOS (Schmitt trigger mode)	140 mV
1.8V LVCMOS (Schmitt trigger mode)	80 mV
1.5V LVCMOS (Schmitt trigger mode)	60 mV

Table 2-26. I/O Input Rise Time, Fall Time, and Related I/O Reliability

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns [1]	20 years (100 °C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis	20 years (100 °C)

Note:

1. The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microchip recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

2.3.4 Single-Ended I/O Characteristics (Ask a Question)

2.3.4.1 3.3V LVTTL/3.3V LVCMOS (Ask a Question)

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-27. Minimum and Maximum DC Input and Output Levels

3.3V LVTTL/ 3.3V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10

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.....continued												
3.3V LVTTL/ 3.3V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA[5]	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.
2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
4. Currents are measured at 85 °C junction temperature.
5. This denotes the software default selection and is applicable for the entire row.

Figure 2-6. AC Loading

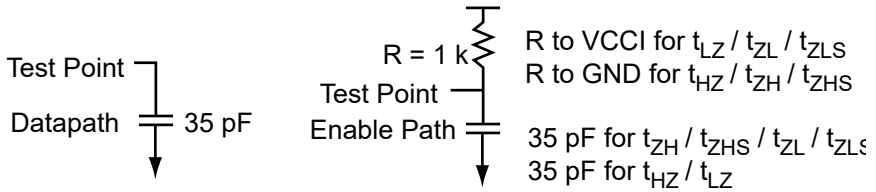


Table 2-28. 3.3V LVTTL/LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point[1](V)	C_{LOAD} (pF)[2]
0	3.3	1.4	10

Notes:

1. Measuring point = Vtrip. See Table 2-16 for a complete table of trip points.
2. Capacitive Load for A3PN060, A3PN125, and A3PN250 is 35 pF.

Timing Characteristics

Table 2-29. 3.3V LVTTL/3.3V LVCMOS Low Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 3.0V—Software Default Load at 35 pF for A3PN060, A3PN125, and A3PN250

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.60	9.70	0.04	1.13	1.52	0.43	9.88	8.82	2.31	2.50	ns
	–1	0.51	8.26	0.04	0.96	1.29	0.36	8.40	7.50	1.96	2.13	ns
	–2	0.45	7.25	0.03	0.84	1.13	0.32	7.37	6.59	1.72	1.87	ns
4 mA	Std.	0.60	9.70	0.04	1.13	1.52	0.43	9.88	8.82	2.31	2.50	ns
	–1	0.51	8.26	0.04	0.96	1.29	0.36	8.40	7.50	1.96	2.13	ns
	–2	0.45	7.25	0.03	0.84	1.13	0.32	7.37	6.59	1.72	1.87	ns
6 mA	Std.	0.60	6.90	0.04	1.13	1.52	0.43	7.01	6.22	2.61	3.01	ns
	–1	0.51	5.87	0.04	0.96	1.29	0.36	5.97	5.29	2.22	2.56	ns
	–2	0.45	5.15	0.03	0.84	1.13	0.32	5.24	4.64	1.95	2.25	ns

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.....continued												
Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	Std.	0.60	6.90	0.04	1.13	1.52	0.43	7.01	6.22	2.61	3.01	ns
	–1	0.51	5.87	0.04	0.96	1.29	0.36	5.97	5.29	2.22	2.56	ns
	–2	0.45	5.15	0.03	0.84	1.13	0.32	5.24	4.64	1.95	2.25	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

Table 2-30. 3.3V LVTTL/3.3V LVCMOS High Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 3.0V—Software Default Load at 35 pF for A3PN060, A3PN125, and A3PN250

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.60	7.19	0.04	1.13	1.52	0.43	7.32	6.40	2.30	2.62	ns
	–1	0.51	6.12	0.04	0.96	1.29	0.36	6.22	5.44	1.96	2.23	ns
	–2	0.45	5.37	0.03	0.84	1.13	0.32	5.46	4.78	1.72	1.96	ns
4 mA	Std.	0.60	7.19	0.04	1.13	1.52	0.43	7.32	6.40	2.30	2.62	ns
	–1	0.51	6.12	0.04	0.96	1.29	0.36	6.22	5.44	1.96	2.23	ns
	–2	0.45	5.37	0.03	0.84	1.13	0.32	5.46	4.78	1.72	1.96	ns
6 mA	Std.	0.60	4.57	0.04	1.13	1.52	0.43	4.64	3.92	2.60	3.14	ns
	–1	0.51	3.89	0.04	0.96	1.29	0.36	3.95	3.33	2.22	2.67	ns
	–2	0.45	3.41	0.03	0.84	1.13	0.32	3.47	2.93	1.95	2.34	ns
8 mA[1]	Std.	0.60	4.57	0.04	1.13	1.52	0.43	4.64	3.92	2.60	3.14	ns
	–1	0.51	3.89	0.04	0.96	1.29	0.36	3.95	3.33	2.22	2.67	ns
	–2	0.45	3.41	0.03	0.84	1.13	0.32	3.47	2.93	1.95	2.34	ns

Notes:

1. This denotes the software default selection and is applicable for the entire row.
2. For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

Table 2-31. 3.3V LVTTL/3.3V LVCMOS Low Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 3.0V—Software Default Load at 10 pF for A3PN020, A3PN015, and A3PN010

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.60	5.48	0.04	1.13	1.52	0.43	5.58	5.21	2.31	2.50	ns
	–1	0.51	4.66	0.04	0.96	1.29	0.36	4.74	4.43	1.96	2.13	ns
	–2	0.45	4.09	0.03	0.84	1.13	0.32	4.16	3.89	1.72	1.87	ns
4 mA	Std.	0.60	5.48	0.04	1.13	1.52	0.43	5.58	5.21	2.31	2.50	ns
	–1	0.51	4.66	0.04	0.96	1.29	0.36	4.74	4.43	1.96	2.13	ns
	–2	0.45	4.09	0.03	0.84	1.13	0.32	4.16	3.89	1.72	1.87	ns
6 mA	Std.	0.60	4.33	0.04	1.13	1.52	0.43	4.40	4.14	2.61	3.01	ns
	–1	0.51	3.69	0.04	0.96	1.29	0.36	3.75	3.52	2.22	2.56	ns
	–2	0.45	3.24	0.03	0.84	1.13	0.32	3.29	3.09	1.95	2.25	ns
8 mA	Std.	0.60	4.33	0.04	1.13	1.52	0.43	4.40	4.14	2.61	3.01	ns
	–1	0.51	3.69	0.04	0.96	1.29	0.36	3.75	3.52	2.22	2.56	ns
	–2	0.45	3.24	0.03	0.84	1.13	0.32	3.29	3.09	1.95	2.25	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

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Table 2-32. 3.3V LVTTL/3.3V LVCMOS High Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 3.0V—Software Default Load at 10 pF for A3PN020, A3PN015, and A3PN010

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.60	3.56	0.04	1.13	1.52	0.43	3.62	3.03	2.30	2.62	ns
	–1	0.51	3.03	0.04	0.96	1.29	0.36	3.08	2.58	1.96	2.23	ns
	–2	0.45	2.66	0.03	0.84	1.13	0.32	2.70	2.26	1.72	1.96	ns
4 mA	Std.	0.60	3.56	0.04	1.13	1.52	0.43	3.62	3.03	2.30	2.62	ns
	–1	0.51	3.03	0.04	0.96	1.29	0.36	3.08	2.58	1.96	2.23	ns
	–2	0.45	2.66	0.03	0.84	1.13	0.32	2.70	2.26	1.72	1.96	ns
6 mA	Std.	0.60	2.73	0.04	1.13	1.52	0.43	2.77	2.23	2.60	3.14	ns
	–1	0.51	2.32	0.04	0.96	1.29	0.36	2.36	1.90	2.22	2.67	ns
	–2	0.45	2.04	0.03	0.84	1.13	0.32	2.07	1.67	1.95	2.34	ns
8 mA[1]	Std.	0.60	2.73	0.04	1.13	1.52	0.43	2.77	2.23	2.60	3.14	ns
	–1	0.51	2.32	0.04	0.96	129	0.36	2.36	1.90	2.22	2.67	ns
	–2	0.45	2.04	0.03	0.84	1.13	0.32	2.07	1.67	1.95	2.34	ns

Notes:

1. This denotes the software default selection and is applicable for the entire row.
2. For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.4.2 3.3V LVCMOS Wide Range (Ask a Question)

Table 2-33. Minimum and Maximum DC Input and Output Levels for 3.3V LVCMOS Wide Range

3.3V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	I_{OH}	IIL[1]	IIH[2]
Drive Strength	Equivalent Software Default Drive Strength Option[3]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	µA[4]	µA[4]
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	10	10
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	10	10
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	10	10
100 µA[6]	8 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.
2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.
3. The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.
4. Currents are measured at 85 °C junction temperature.
5. All LVMCOS 3.3V software macros support LVCMOS 3.3V Wide Range, as specified in the JESD8-B specification.
6. This denotes the software default selection and is applicable for the entire row.

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Timing Characteristics

Table 2-34. 3.3V LVCMOS Wide Range Low Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.7V—Software Default Load at 35 pF for A3PN060, A3PN125, and A3PN250

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	Std.	0.60	14.73	0.04	1.57	2.18	0.43	14.73	13.16	3.26	3.38	ns
		–1	0.51	12.53	0.04	1.33	1.85	0.36	12.53	11.19	2.77	2.87	ns
		–2	0.45	11.00	0.03	1.17	1.62	0.32	11.00	9.83	2.43	2.52	ns
100 µA	4 mA	Std.	0.60	14.73	0.04	1.57	2.18	0.43	14.73	13.16	3.26	3.38	ns
		–1	0.51	12.53	0.04	1.33	1.85	0.36	12.53	11.19	2.77	2.87	ns
		–2	0.45	11.00	0.03	1.17	1.62	0.32	11.00	9.83	2.43	2.52	ns
100 µA	6 mA	Std.	0.60	10.38	0.04	1.57	2.18	0.43	10.38	9.21	3.72	4.16	ns
		–1	0.51	8.83	0.04	1.33	1.85	0.36	8.83	7.83	3.17	3.54	ns
		–2	0.45	7.75	0.03	1.17	1.62	0.32	7.75	6.88	2.78	3.11	ns
100 µA	8 mA	Std.	0.60	10.38	0.04	1.57	2.18	0.43	10.38	9.21	3.72	4.16	ns
		–1	0.51	8.83	0.04	1.33	1.85	0.36	8.83	7.83	3.17	3.54	ns
		–2	0.45	7.75	0.03	1.17	1.62	0.32	7.75	6.88	2.78	3.11	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.
2. For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

Table 2-35. 3.3V LVCMOS Wide Range High Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.7V—Software Default Load at 35 pF for A3PN060, A3PN125, and A3PN250

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	Std.	0.60	10.83	0.04	1.57	2.18	0.43	10.83	9.48	3.25	3.56	ns
		–1	0.51	9.22	0.04	1.33	1.85	0.36	9.22	8.06	2.77	3.03	ns
		–2	0.45	8.09	0.03	1.17	1.62	0.32	8.09	7.08	2.43	2.66	ns
100 µA	4 mA	Std.	0.60	10.83	0.04	1.57	2.18	0.43	10.83	9.48	3.25	3.56	ns
		–1	0.51	9.22	0.04	1.33	1.85	0.36	9.22	8.06	2.77	3.03	ns
		–2	0.45	8.09	0.03	1.17	1.62	0.32	8.09	7.08	2.43	2.66	ns
100 µA	6 mA	Std.	0.60	6.78	0.04	1.57	2.18	0.43	6.78	5.72	3.72	4.35	ns
		–1	0.51	5.77	0.04	1.33	1.85	0.36	5.77	4.87	3.16	3.70	ns
		–2	0.45	5.06	0.03	1.17	1.62	0.32	5.06	4.27	2.78	3.25	ns
100 µA[3]	8 mA	Std.	0.60	6.78	0.04	1.57	2.18	0.43	6.78	5.72	3.72	4.35	ns
		–1	0.51	5.77	0.04	1.33	1.85	0.36	5.77	4.87	3.16	3.70	ns
		–2	0.45	5.06	0.03	1.17	1.62	0.32	5.06	4.27	2.78	3.25	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.
2. For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.
3. This denotes the software default selection and is applicable for the entire row.

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Table 2-36. 3.3V LVCMOS Wide Range Low Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.7V—Software Default Load at 35 pF for A3PN020, A3PN015, and A3PN010

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	Std.	0.60	8.20	0.04	1.57	2.18	0.43	8.20	7.68	3.26	3.38	ns
		–1	0.51	6.97	0.04	1.33	1.85	0.36	6.97	6.53	2.77	2.87	ns
		–2	0.45	6.12	0.03	1.17	1.62	0.32	6.12	5.73	2.43	2.52	ns
100 µA	4 mA	Std.	0.60	8.20	0.04	1.57	2.18	0.43	8.20	7.68	3.26	3.38	ns
		–1	0.51	6.97	0.04	1.33	1.85	0.36	6.97	6.53	2.77	2.87	ns
		–2	0.45	6.12	0.03	1.17	1.62	0.32	6.12	5.73	2.43	2.52	ns
100 µA	6 mA	Std.	0.60	6.42	0.04	1.57	2.18	0.43	6.42	6.05	3.72	4.16	ns
		–1	0.51	5.46	0.04	1.33	1.85	0.36	5.46	5.14	3.17	3.54	ns
		–2	0.45	4.79	0.03	1.17	1.62	0.32	4.79	4.52	2.78	3.11	ns
100 µA	8 mA	Std.	0.60	6.42	0.04	1.57	2.18	0.43	6.42	6.05	3.72	4.16	ns
		–1	0.51	5.46	0.04	1.33	1.85	0.36	5.46	5.14	3.17	3.54	ns
		–2	0.45	4.79	0.03	1.17	1.62	0.32	4.79	4.52	2.78	3.11	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.
2. For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

Table 2-37. 3.3V LVCMOS Wide Range High Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.7V—Software Default Load at 35 pF for A3PN020, A3PN015, and A3PN010

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	Std.	0.60	5.23	0.04	1.57	2.18	0.43	5.23	4.37	3.25	3.56	ns
		–1	0.51	4.45	0.04	1.33	1.85	0.36	4.45	3.71	2.77	3.03	ns
		–2	0.45	3.90	0.03	1.17	1.62	0.32	3.90	3.26	2.43	2.66	ns
100 µA	4 mA	Std.	0.60	5.23	0.04	1.57	2.18	0.43	5.23	4.37	3.25	3.56	ns
		–1	0.51	4.45	0.04	1.33	1.85	0.36	4.45	3.71	2.77	3.03	ns
		–2	0.45	3.90	0.03	1.17	1.62	0.32	3.90	3.26	2.43	2.66	ns
100 µA	6 mA	Std.	0.60	3.94	0.04	1.57	2.18	0.43	3.94	3.16	3.72	4.35	ns
		–1	0.51	3.35	0.04	1.33	1.85	0.36	3.35	2.69	3.16	3.70	ns
		–2	0.45	2.94	0.03	1.17	1.62	0.32	2.94	2.36	2.78	3.25	ns
100 µA[3]	8 mA	Std.	0.60	3.94	0.04	1.57	2.18	0.43	3.94	3.16	3.72	4.35	ns
		–1	0.51	3.35	0.04	1.33	1.85	0.36	3.35	2.69	3.16	3.70	ns
		–2	0.45	2.94	0.03	1.17	1.62	0.32	2.94	2.36	2.78	3.25	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.
2. For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.
3. This denotes the software default selection and is applicable for the entire row.

2.3.4.3 2.5V LVCMOS (Ask a Question)

Low-Voltage CMOS for 2.5V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5V applications.

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Table 2-38. Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA[5]	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.
2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
4. Currents are measured at 85 °C junction temperature.
5. This denotes the software default selection and is applicable for the entire row.

Figure 2-7. AC Loading

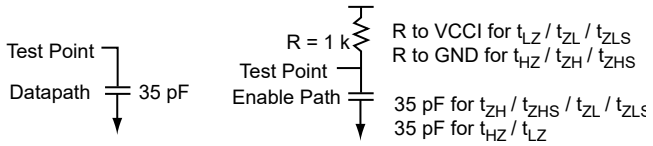


Table 2-39. 2.5V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point[1] (V)	C_{LOAD}[2] (pF)
0	2.5	1.2	10

Notes:

1. Measuring point = Vtrip. See Table 2-16 for a complete table of trip points.
2. Capacitive Load for A3PN060, A3PN125, and A3PN250 is 35 pF.

Timing Characteristics

Table 2-40. 2.5V LVCMOS Low Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.3V—Software Default Load at 35 pF for A3PN060, A3PN125, and A3PN250

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.60	11.29	0.04	1.43	1.63	0.43	10.64	11.29	2.27	2.29	ns
	–1	0.51	9.61	0.04	1.22	1.39	0.36	9.05	9.61	1.93	1.95	ns
	–2	0.45	8.43	0.03	1.07	1.22	0.32	7.94	8.43	1.70	1.71	ns
4 mA	Std.	0.60	11.29	0.04	1.43	1.63	0.43	10.64	11.29	2.27	2.29	ns
	–1	0.51	9.61	0.04	1.22	1.39	0.36	9.05	9.61	1.93	1.95	ns
	–2	0.45	8.43	0.03	1.07	1.22	0.32	7.94	8.43	1.70	1.71	ns
6 mA	Std.	0.60	7.73	0.04	1.43	1.63	0.43	7.70	7.73	2.60	2.89	ns
	–1	0.51	6.57	0.04	1.22	1.39	0.36	6.55	6.57	2.21	2.46	ns
	–2	0.45	5.77	0.03	1.07	1.22	0.32	5.75	5.77	1.94	2.16	ns

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.....continued												
Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	Std.	0.60	7.73	0.04	1.43	1.63	0.43	7.70	7.73	2.60	2.89	ns
	–1	0.51	6.57	0.04	1.22	1.39	0.36	6.55	6.57	2.21	2.46	ns
	–2	0.45	5.77	0.03	1.07	1.22	0.32	5.75	5.77	1.94	2.16	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

Table 2-41. 2.5V LVCMOS High Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.3V—Software Default Load at 35 pF for A3PN060, A3PN125, and A3PN250

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.60	8.38	0.04	1.43	1.63	0.43	7.36	8.38	2.27	2.37	ns
	–1	0.51	7.13	0.04	1.22	1.39	0.36	6.26	7.13	1.93	2.02	ns
	–2	0.45	6.26	0.03	1.07	1.22	0.32	5.50	6.26	1.69	1.77	ns
4 mA	Std.	0.60	8.38	0.04	1.43	1.63	0.43	7.36	8.38	2.27	2.37	ns
	–1	0.51	7.13	0.04	1.22	1.39	0.36	6.26	7.13	1.93	2.02	ns
	–2	0.45	6.26	0.03	1.07	1.22	0.32	5.50	6.26	1.69	1.77	ns
6 mA	Std.	0.60	4.94	0.04	1.43	1.63	0.43	4.71	4.94	2.60	2.98	ns
	–1	0.51	4.20	0.04	1.22	1.39	0.36	4.01	4.20	2.21	2.54	ns
	–2	0.45	3.69	0.03	1.07	1.22	0.32	3.52	3.69	1.94	2.23	ns
8 mA[1]	Std.	0.60	4.94	0.04	1.43	1.63	0.43	4.71	4.94	2.60	2.98	ns
	–1	0.51	4.20	0.04	1.22	1.39	0.36	4.01	4.20	2.21	2.54	ns
	–2	0.45	3.69	0.03	1.07	1.22	0.32	3.52	3.69	1.94	2.23	ns

Notes:

1. This denotes the software default selection and is applicable for the entire row.
2. For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

Table 2-42. 2.5V LVCMOS Low Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.3V—Software Default Load at 10 pF for A3PN020, A3PN015, and A3PN010

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.60	6.40	0.04	1.43	1.63	0.43	6.16	6.40	2.27	2.29	ns
	–1	0.51	5.45	0.04	1.22	1.39	0.36	5.24	5.45	1.93	1.95	ns
	–2	0.45	4.78	0.03	1.07	1.22	0.32	4.60	4.78	1.70	1.71	ns
4 mA	Std.	0.60	6.40	0.04	1.43	1.63	0.43	6.16	6.40	2.27	2.29	ns
	–1	0.51	5.45	0.04	1.22	1.39	0.36	5.24	5.45	1.93	1.95	ns
	–2	0.45	4.78	0.03	1.07	1.22	0.32	4.60	4.78	1.70	1.71	ns
6 mA	Std.	0.60	5.00	0.04	1.43	1.63	0.43	4.90	5.00	2.60	2.89	ns
	–1	0.51	4.26	0.04	1.22	1.39	0.36	4.17	4.26	2.21	2.46	ns
	–2	0.45	3.74	0.03	1.07	1.22	0.32	3.66	3.74	1.94	2.16	ns
8 mA	Std.	0.60	5.00	0.04	1.43	1.63	0.43	4.90	5.00	2.60	2.89	ns
	–1	0.51	4.26	0.04	1.22	1.39	0.36	4.17	4.26	2.21	2.46	ns
	–2	0.45	3.74	0.03	1.07	1.22	0.32	3.66	3.74	1.94	2.16	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

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Table 2-43. 2.5 V LVCMOS High Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.3V—Software Default Load at 10 pF for A3PN020, A3PN015, and A3PN010

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.60	3.70	0.04	1.43	1.63	0.43	3.66	3.70	2.27	2.37	ns
	–1	0.51	3.15	0.04	1.22	1.39	0.36	3.12	3.15	1.93	2.02	ns
	–2	0.45	2.77	0.03	1.07	1.22	0.32	2.74	2.77	1.69	1.77	ns
4 mA	Std.	0.60	3.70	0.04	1.43	1.63	0.43	3.66	3.70	2.27	2.37	ns
	–1	0.51	3.15	0.04	1.22	1.39	0.36	3.12	3.15	1.93	2.02	ns
	–2	0.45	2.77	0.03	1.07	1.22	0.32	2.74	2.77	1.69	1.77	ns
6 mA	Std.	0.60	2.76	0.04	1.43	1.63	0.43	2.80	2.60	2.60	2.98	ns
	–1	0.51	2.35	0.04	1.22	1.39	0.36	2.38	2.21	2.21	2.54	ns
	–2	0.45	2.06	0.03	1.07	1.22	0.32	2.09	1.94	1.94	2.23	ns
8 mA[1]	Std.	0.60	2.76	0.04	1.43	1.63	0.43	2.80	2.60	2.60	2.98	ns
	–1	0.51	2.35	0.04	1.22	1.39	0.36	2.38	2.21	2.21	2.54	ns
	–2	0.45	2.06	0.03	1.07	1.22	0.32	2.09	1.94	1.94	2.23	ns

Notes:

1. This denotes the software default selection and is applicable for the entire row.
2. For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.4.4 1.8V LVCMOS (Ask a Question)

Low-voltage CMOS for 1.8V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8V applications. It uses a 1.8V input buffer and a push-pull output buffer.

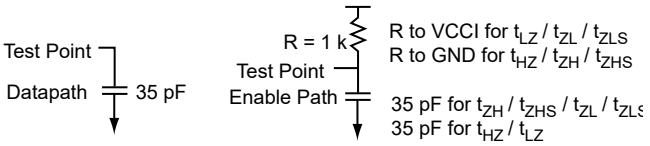
Table 2-44. Minimum and Maximum DC Input and Output Levels

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	9	11	10	10
4 mA[5]	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	17	22	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.
2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
4. Currents are measured at 85 °C junction temperature.
5. This denotes the software default selection and is applicable for the entire row.

Figure 2-8. AC Loading



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Table 2-45. 1.8V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point[1] (V)	C_{LOAD}[2] (pF)
0	1.8	0.9	10

Notes:

1. Measuring point = Vtrip. See Table 2-16 for a complete table of trip points.
2. Capacitive Load for A3PN060, A3PN125, and A3PN250 is 35 pF.

Timing Characteristics

Table 2-46. 1.8V LVCMOS Low Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.7V—Software Default Load at 35 pF for A3PN060, A3PN125, and A3PN250

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.60	15.36	0.04	1.35	1.90	0.43	13.46	15.36	2.23	1.78	ns
	–1	0.51	13.07	0.04	1.15	1.61	0.36	11.45	13.07	1.90	1.51	ns
	–2	0.45	11.47	0.03	1.01	1.42	0.32	10.05	11.47	1.67	1.33	ns
4 mA	Std.	0.60	10.32	0.04	1.35	1.90	0.43	9.92	10.32	2.63	2.78	ns
	–1	0.51	8.78	0.04	1.15	1.61	0.36	8.44	8.78	2.23	2.37	ns
	–2	0.45	7.71	0.03	1.01	1.42	0.32	7.41	7.71	1.96	2.08	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

Table 2-47. 1.8V LVCMOS High Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.7V—Software Default Load at 35 pF for A3PN060, A3PN125, and A3PN250

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.60	11.42	0.04	1.35	1.90	0.43	8.65	11.42	2.23	1.84	ns
	–1	0.51	9.71	0.04	1.15	1.61	0.36	7.36	9.71	1.89	1.57	ns
	–2	0.45	8.53	0.03	1.01	1.42	0.32	6.46	8.53	1.66	1.37	ns
4 mA[1]	Std.	0.60	6.53	0.04	1.35	1.90	0.43	5.53	6.53	2.62	2.89	ns
	–1	0.51	5.56	0.04	1.15	1.61	0.36	4.70	5.56	2.23	2.45	ns
	–2	0.45	4.88	0.03	1.01	1.42	0.32	4.13	4.88	1.96	2.15	ns

Notes:

1. This denotes the software default selection and is applicable for the entire row.
2. For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

Table 2-48. 1.8V LVCMOS Low Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.7V—Software Default Load at 10 pF for A3PN020, A3PN015, and A3PN010

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.60	8.52	0.04	1.35	1.90	0.43	7.99	8.52	2.23	1.78	ns
	–1	0.51	7.25	0.04	1.15	1.61	0.36	6.80	7.25	1.90	1.51	ns
	–2	0.45	6.36	0.03	1.01	1.42	0.32	5.97	6.36	1.67	1.33	ns
4 mA	Std.	0.60	6.59	0.04	1.35	1.90	0.43	6.44	6.59	2.63	2.78	ns
	–1	0.51	5.60	0.04	1.15	1.61	0.36	5.48	5.60	2.23	2.37	ns
	–2	0.45	4.92	0.03	1.01	1.42	0.32	4.81	4.92	1.96	2.08	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

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Table 2-49. 1.8 V LVCMOS High Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.7V—Software Default Load at 10 pF for A3PN020, A3PN015, and A3PN010

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.60	4.79	0.04	1.35	1.90	0.43	4.27	4.79	2.23	1.84	ns
	–1	0.51	4.08	0.04	1.15	1.61	0.36	3.63	4.08	1.89	1.57	ns
	–2	0.45	3.58	0.03	1.01	1.42	0.32	3.19	3.58	1.66	1.37	ns
4 mA[1]	Std.	0.60	3.22	0.04	1.35	1.90	0.43	3.24	3.22	2.62	2.89	ns
	–1	0.51	2.74	0.04	1.15	1.61	0.36	2.75	2.74	2.23	2.45	ns
	–2	0.45	2.40	0.03	1.01	1.42	0.32	2.42	2.40	1.95	2.15	ns

Notes:

1. This denotes the software default selection and is applicable for the entire row.
2. For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.4.5 1.5V LVCMOS (JESD8-11) (Ask a Question)

Low-Voltage CMOS for 1.5V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5V applications. It uses a 1.5V input buffer and a push-pull output buffer.

Table 2-50. Minimum and Maximum DC Input and Output Levels

1.5V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA[5]	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.
2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
4. Currents are measured at 85 °C junction temperature.
5. This denotes the software default selection and is applicable for the entire row.

Figure 2-9. AC Loading

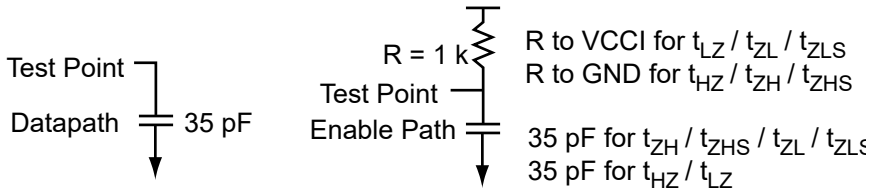


Table 2-51. 1.5V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point[1] (V)	C_{LOAD}[2] (pF)
0	1.5	0.75	10

Notes:

1. Measuring point = Vtrip. See Table 2-16 for a complete table of trip points.
2. Capacitive Load for A3PN060, A3PN125, and A3PN250 is 35 pF.

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Timing Characteristics

Table 2-52. 1.5V LVCMOS Low Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.4V—Software Default Load at 35 pF for A3PN060, A3PN125, and A3PN250

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.60	12.58	0.04	1.56	2.14	0.43	12.18	12.58	2.67	2.71	ns
	–1	0.51	10.70	0.04	1.32	1.82	0.36	10.36	10.70	2.27	2.31	ns
	–2	0.45	9.39	0.03	1.16	1.59	0.32	9.09	9.39	1.99	2.03	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

Table 2-53. 1.5 V LVCMOS High Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.4V—Software Default Load at 35 pF for A3PN060, A3PN125, and A3PN250

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA[1]	Std.	0.60	7.86	0.04	1.56	2.14	0.43	6.45	7.86	2.66	2.83	ns
	–1	0.51	6.68	0.04	1.32	1.82	0.36	5.49	6.68	2.26	2.41	ns
	–2	0.45	5.87	0.03	1.16	1.59	0.32	4.82	5.87	1.99	2.12	ns

Notes:

1. This denotes the software default selection and is applicable for the entire row.
2. For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

Table 2-54. 1.5V LVCMOS Low Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.4V—Software Default Load at 10 pF for A3PN020, A3PN015, and A3PN010

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.60	8.01	0.04	1.56	2.14	0.43	8.03	8.01	2.67	2.71	ns
	–1	0.51	6.81	0.04	1.32	1.82	0.36	6.83	6.81	2.27	2.31	ns
	–2	0.45	5.98	0.03	1.16	1.58	0.32	6.00	5.98	2.10	2.03	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

Table 2-55. 1.5V LVCMOS High Slew—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.4V—Software Default Load at 10 pF for A3PN020, A3PN015, and A3PN010

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA[1]	Std.	0.60	3.76	0.04	1.52	2.14	0.43	3.74	3.76	2.66	2.83	ns
	–1	0.51	3.20	0.04	1.32	1.82	0.36	3.18	3.20	2.26	2.41	ns
	–2	0.45	2.81	0.03	1.16	1.59	0.32	2.79	2.81	1.99	2.12	ns

Notes:

1. This denotes the software default selection and is applicable for the entire row.
2. For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

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2.3.5 I/O Register Specifications (Ask a Question)

2.3.5.1 Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset (Ask a Question)

Figure 2-10. Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

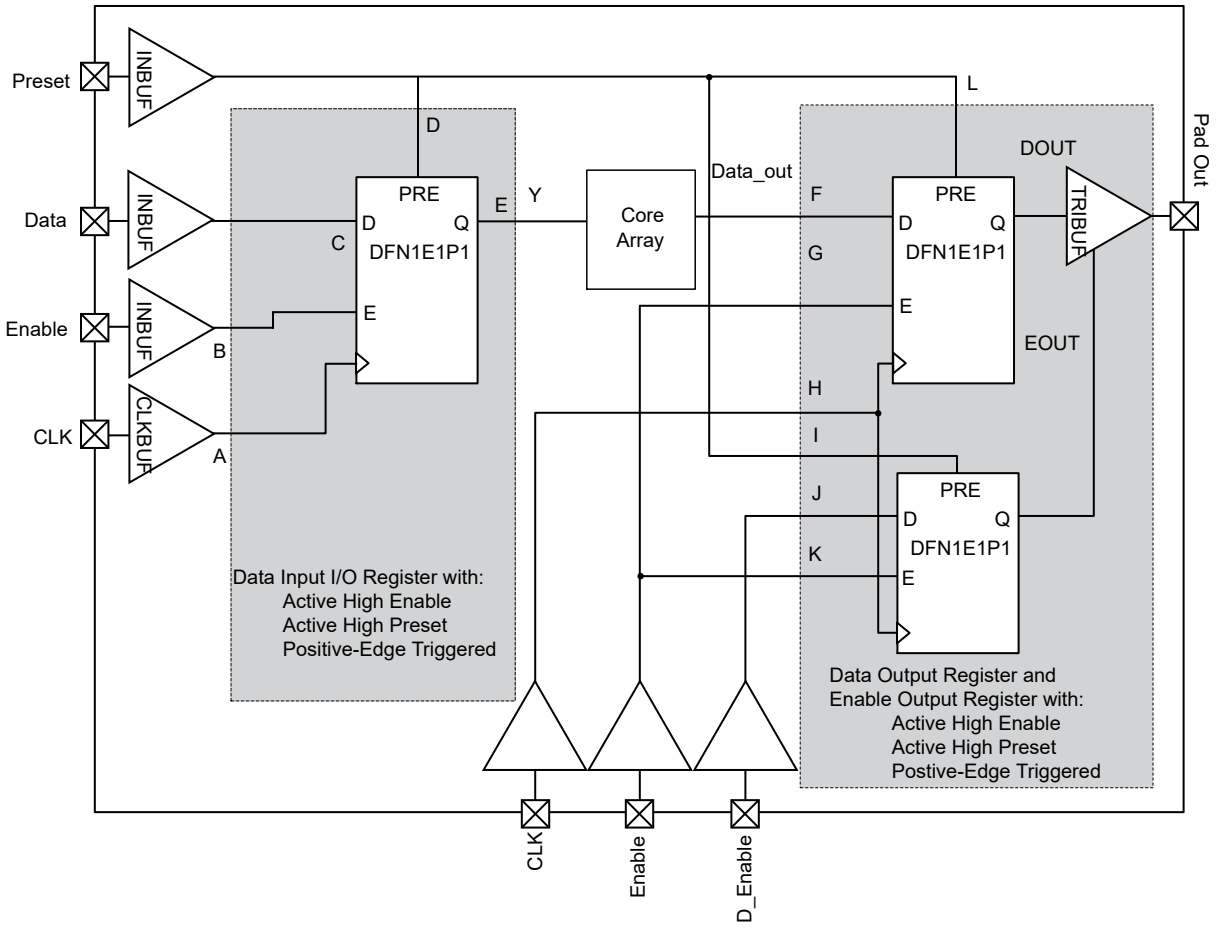


Table 2-56. Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)[1]
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H

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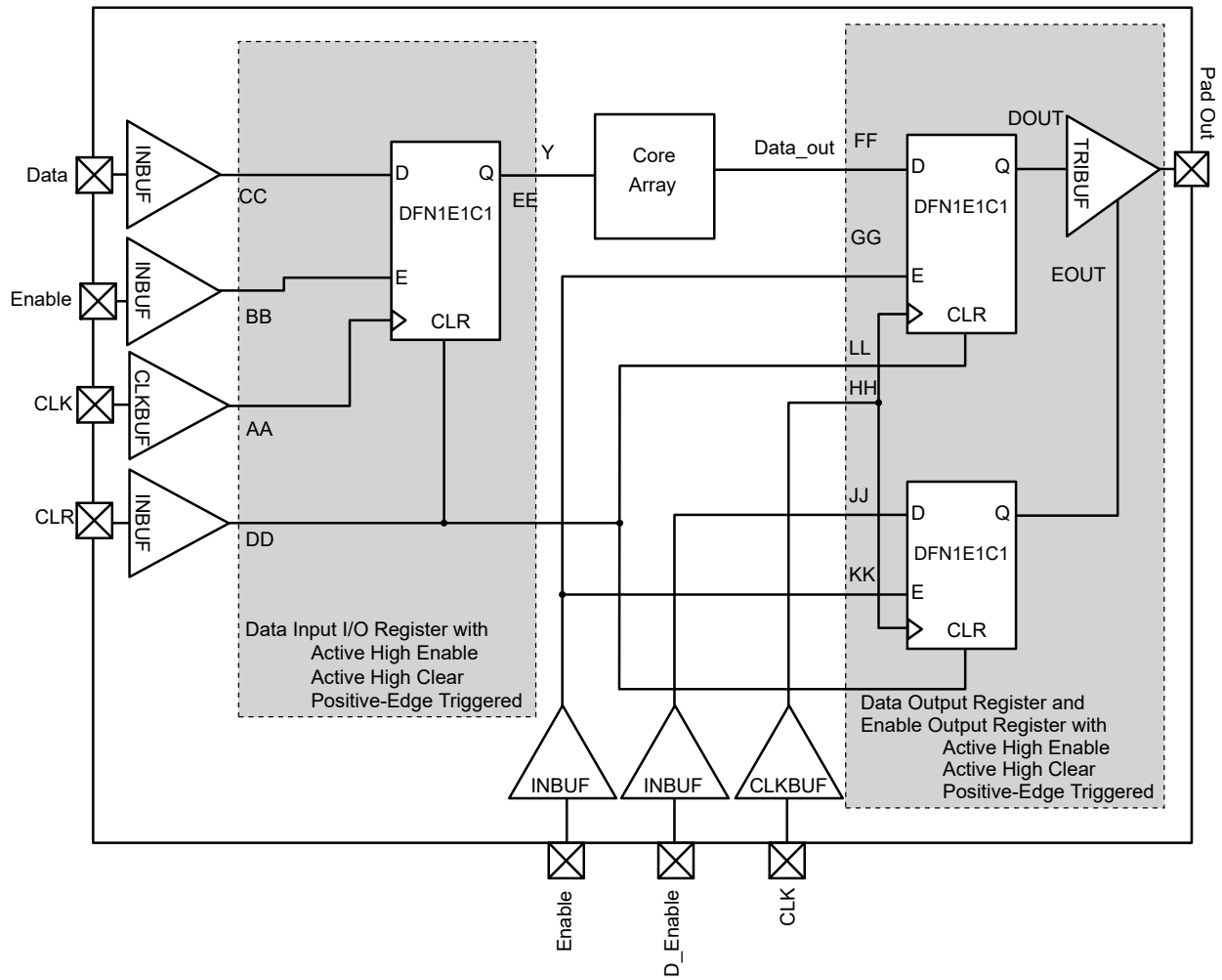
.....continued		
Parameter Name	Parameter Definition	Measuring Nodes (from, to)[1]
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note:

1. See Figure 2-10 for more information.

2.3.5.2 Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear (Ask a Question)

Figure 2-11. Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear



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Table 2-57. Parameter Definition and Measuring Nodes

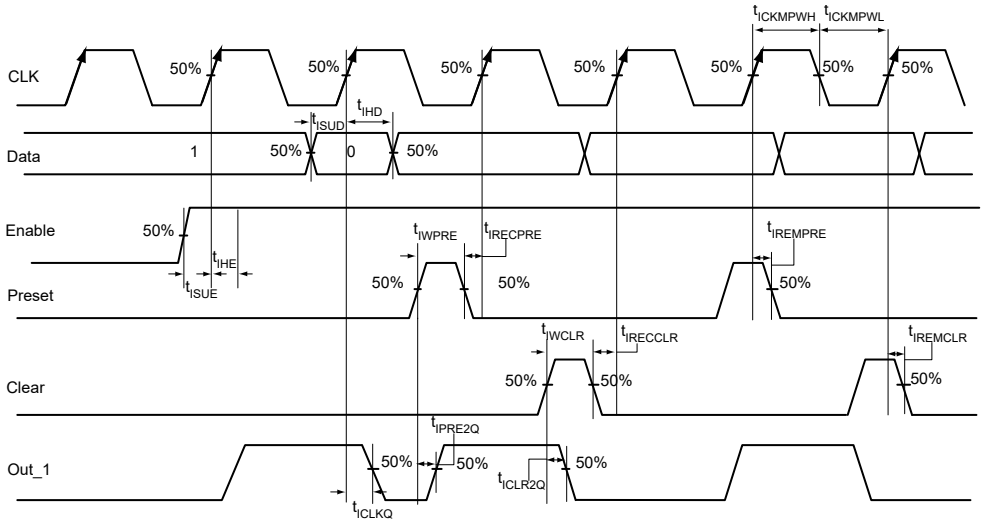
Parameter Name	Parameter Definition	Measuring Nodes (from, to)[1]
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

Note:

1. See Figure 2-11 for more information.

2.3.5.3 Input Register (Ask a Question)

Figure 2-12. Input Register Timing Diagram



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Timing Characteristics

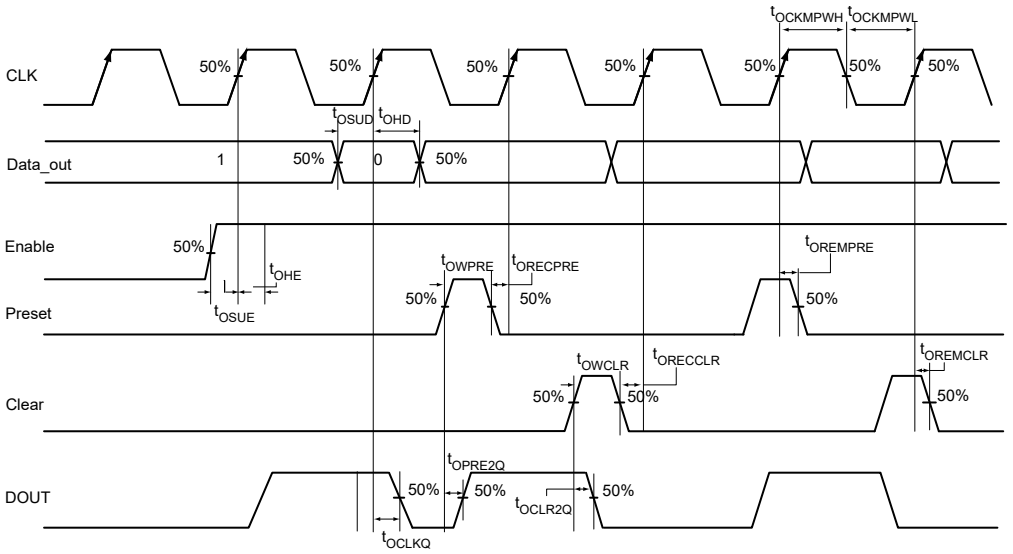
Table 2-58. Input Data Register Propagation Delays—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V

Parameter	Description	–2	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.27	0.32	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.26	0.30	0.35	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.45	0.52	0.61	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.45	0.52	0.61	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.36	0.41	0.48	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.32	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.5.4 Output Register (Ask a Question)

Figure 2-13. Output Register Timing Diagram



Timing Characteristics

Table 2-59. Output Data Register Propagation Delays—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V

Parameter	Description	–2	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.59	0.67	0.79	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.31	0.36	0.42	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.80	0.91	1.07	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.80	0.91	1.07	ns

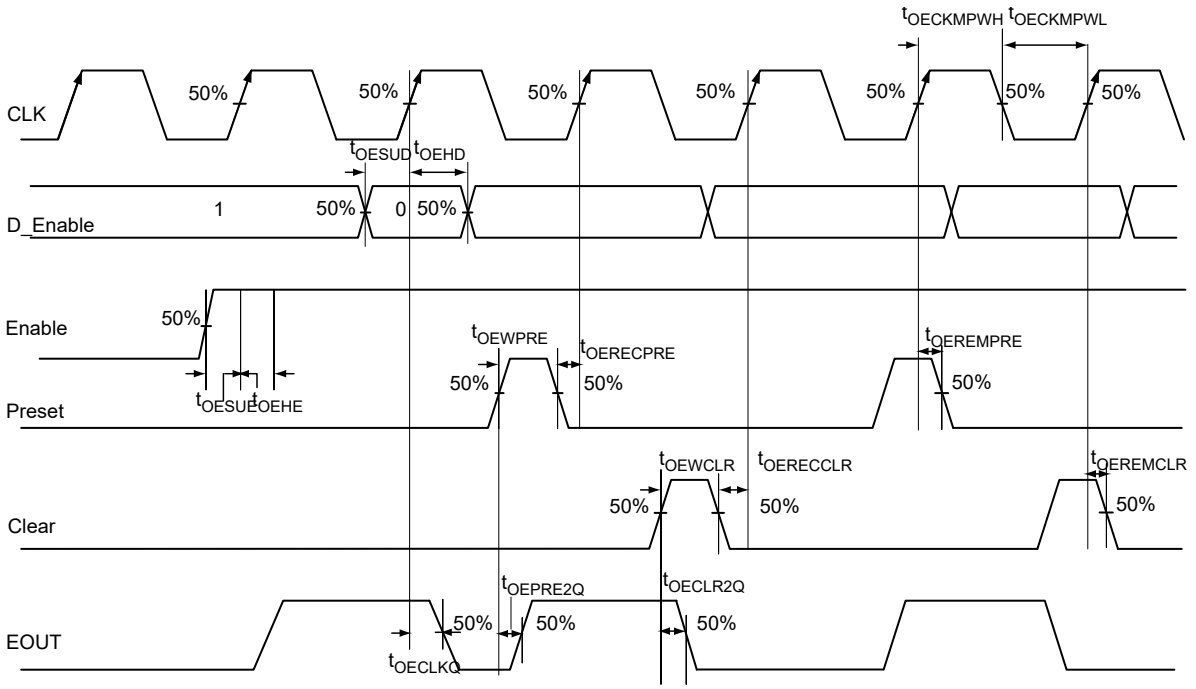
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Parameter	Description	–2	–1	Std.	Units
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.36	0.41	0.48	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.32	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.5.5 Output Enable Register (Ask a Question)

Figure 2-14. Output Enable Register Timing Diagram



Timing Characteristics

Table 2-60. Output Enable Register Propagation Delays—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V

Parameter	Description	–2	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.44	0.51	0.59	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.31	0.36	0.42	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.67	0.76	0.89	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.67	0.76	0.89	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.22	0.25	0.30	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.22	0.25	0.30	ns

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.....continued					
Parameter	Description	–2	–1	Std.	Units
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.36	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.32	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.6 DDR Module Specifications (Ask a Question)

2.3.6.1 Input DDR Module (Ask a Question)

Figure 2-15. Input DDR Timing Model

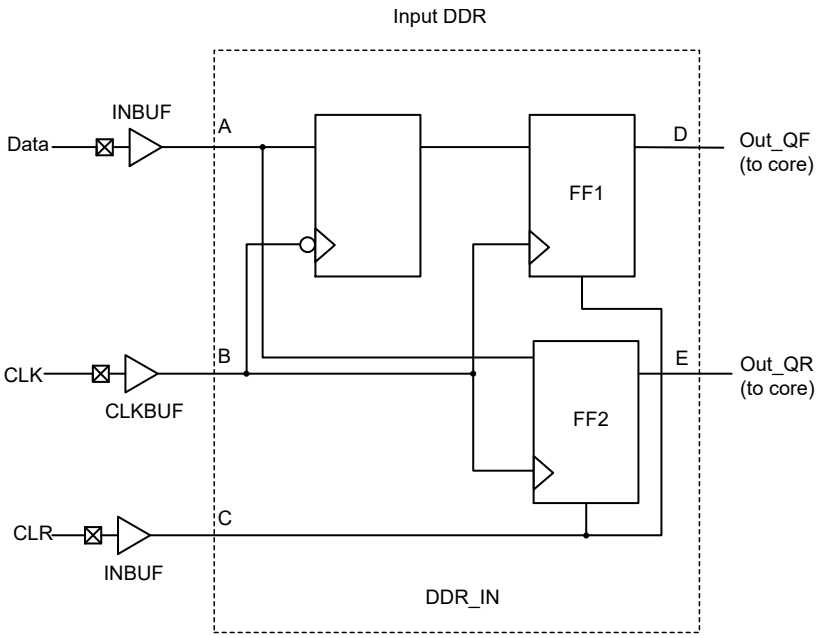
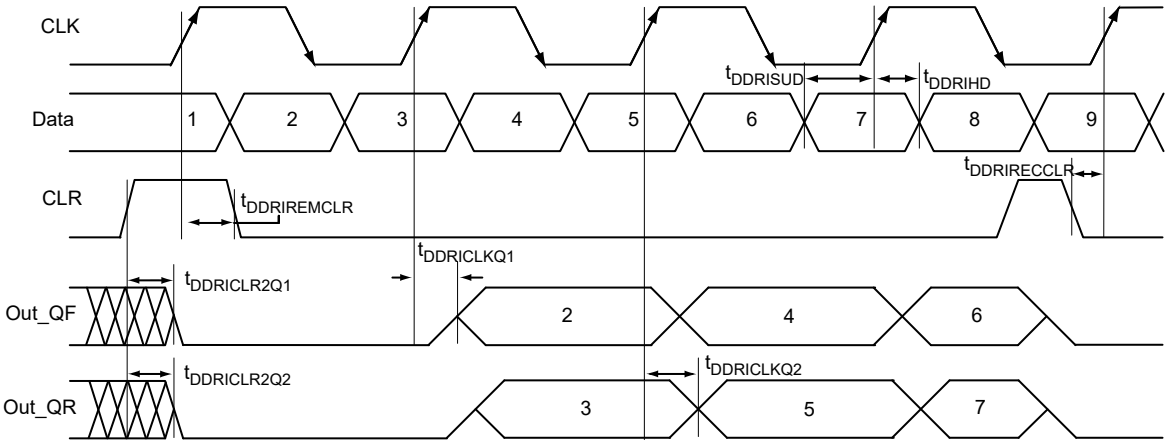


Table 2-61. Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

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Figure 2-16. Input DDR Timing Diagram



Timing Characteristics

Table 2-62. Input DDR Propagation Delays—Commercial-Case Conditions: T_J = 70 °C, Worst Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.27	0.31	0.37	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.39	0.44	0.52	ns
$t_{DDRISUD}$	Data Setup for Input DDR (Fall)	0.28	0.32	0.38	ns
	Data Setup for Input DDR (Rise)	0.25	0.28	0.33	ns
t_{DDRIHD}	Data Hold for Input DDR (Fall)	0.00	0.00	0.00	ns
	Data Hold for Input DDR (Rise)	0.00	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.46	0.53	0.62	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.57	0.65	0.76	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal time for Input DDR	0.00	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery time for Input DDR	0.22	0.25	0.30	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.22	0.25	0.30	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.36	0.41	0.48	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.32	0.37	0.43	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	350.00	350.00	350.00	MHz

Note: For specific junction temperature and voltage-supply levels, see Table 2-6 for derating values.

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2.3.6.2 Output DDR Module (Ask a Question)

Figure 2-17. Output DDR Timing Model

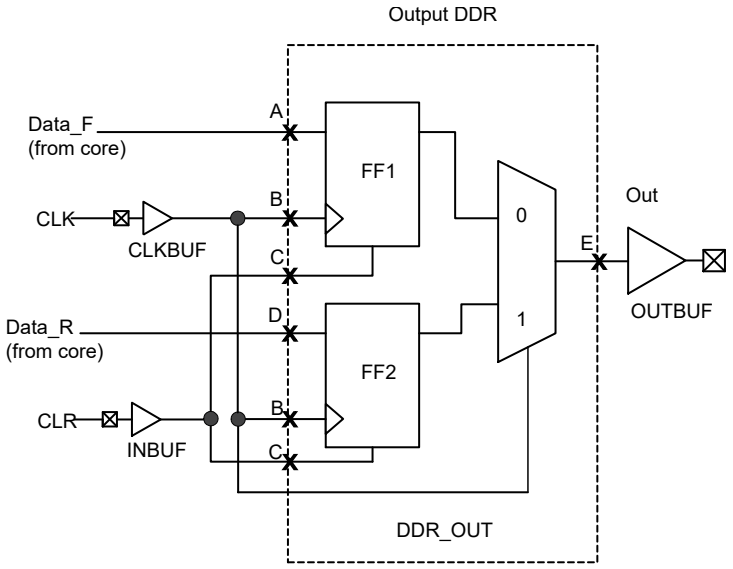
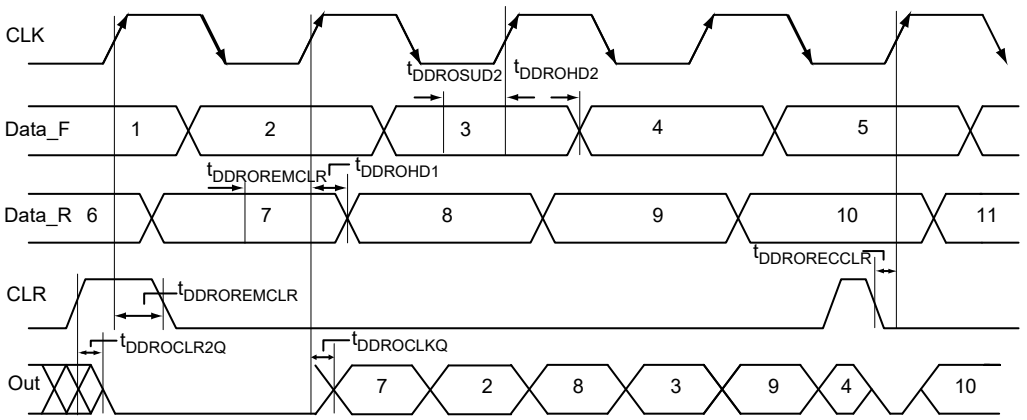


Table 2-63. Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

Figure 2-18. Output DDR Timing Diagram



Timing Characteristics

Table 2-64. Output DDR Propagation Delays—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V

Parameter	Description	–2	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.70	0.80	0.94	ns

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.....continued					
Parameter	Description	–2	–1	Std.	Units
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.38	0.43	0.51	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.38	0.43	0.51	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.80	0.91	1.07	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.22	0.25	0.30	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	0.25	0.30	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.36	0.41	0.48	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.32	0.37	0.43	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	350.00	350.00	350.00	MHz

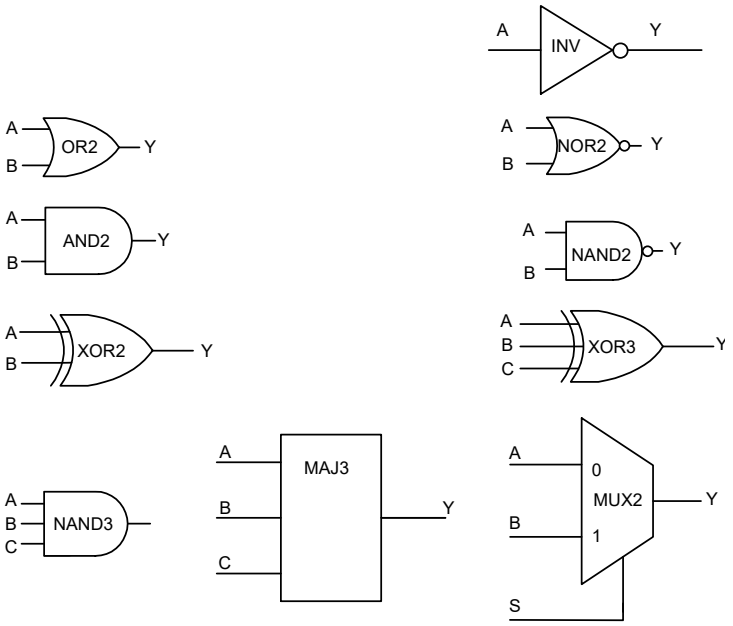
Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.4 VersaTile Characteristics (Ask a Question)

2.4.1 VersaTile Specifications as a Combinatorial Module (Ask a Question)

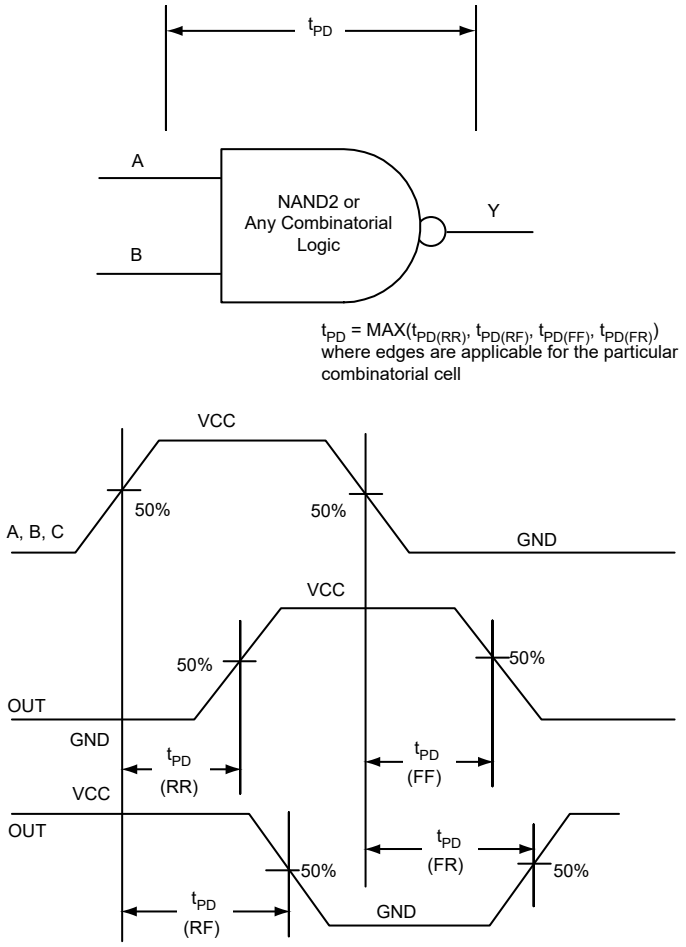
The ProASIC 3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, see the IGLOO, ProASIC 3, SmartFusion and Fusion Macro Library Guide.

Figure 2-19. Sample of Combinatorial Cells



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Figure 2-20. Timing Model and Waveforms



Timing Characteristics

Table 2-65. Combinatorial Cell Propagation Delays—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V

Combinatorial Cell	Equation	Parameter	–2	–1	Std.	Units
INV	Y = !A	t_{PD}	0.40	0.46	0.54	ns
AND2	Y = A · B	t_{PD}	0.47	0.54	0.63	ns
NAND2	Y = !(A · B)	t_{PD}	0.47	0.54	0.63	ns
OR2	Y = A + B	t_{PD}	0.49	0.55	0.65	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.55	0.65	ns
XOR2	Y = A ⊕ B	t_{PD}	0.74	0.84	0.99	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.70	0.79	0.93	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.87	1.00	1.17	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.58	0.68	ns
AND3	Y = A · B · C	t_{PD}	0.56	0.64	0.75	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.4.2 VersaTile Specifications as a Sequential Module (Ask a Question)

The ProASIC 3 library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are

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presented for a representative sample from the library. For more details, see the IGLOO, ProASIC 3, SmartFusion and Fusion Macro Library Guide.

Figure 2-21. Sample of Sequential Cells

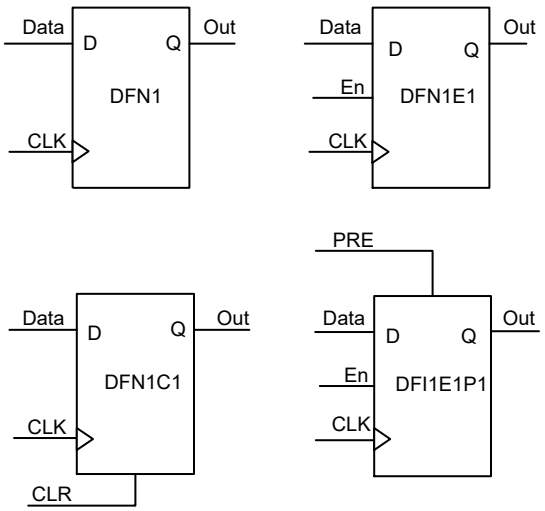
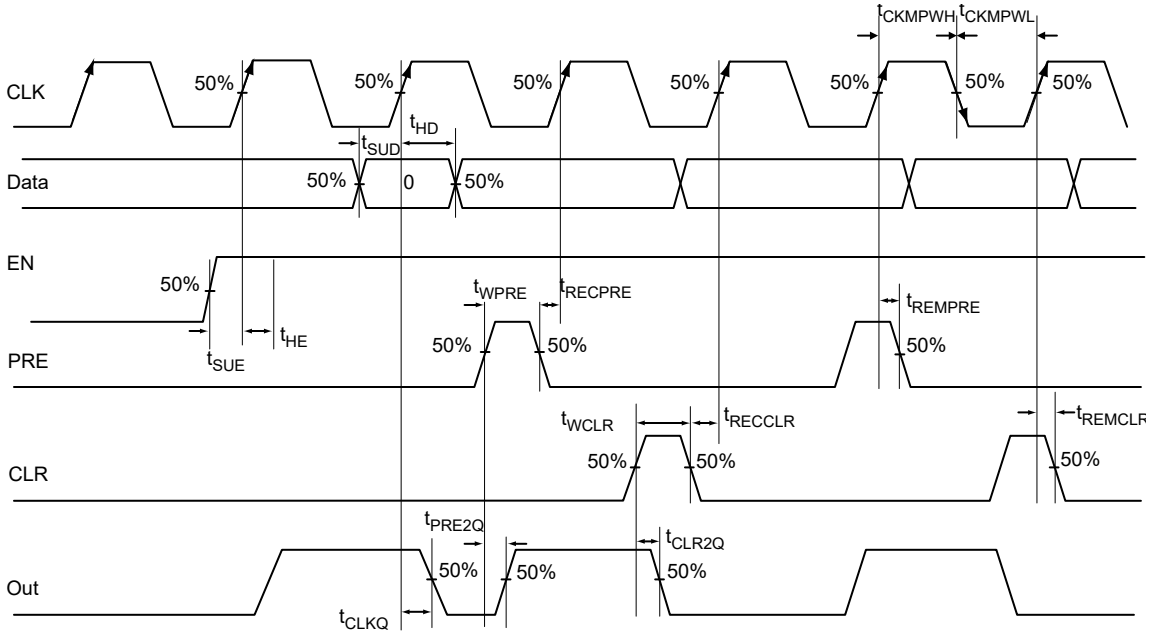


Figure 2-22. Timing Model and Waveforms



Timing Characteristics

Table 2-66. Register Delays—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V

Parameter	Description	–2	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.55	0.63	0.74	ns
t_{SUD}	Data Setup Time for the Core Register	0.43	0.49	0.57	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.45	0.52	0.61	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.40	0.45	0.53	ns

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.....continued					
Parameter	Description	–2	–1	Std.	Units
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.40	0.45	0.53	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.22	0.25	0.30	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.22	0.25	0.30	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.36	0.41	0.48	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.32	0.37	0.43	ns

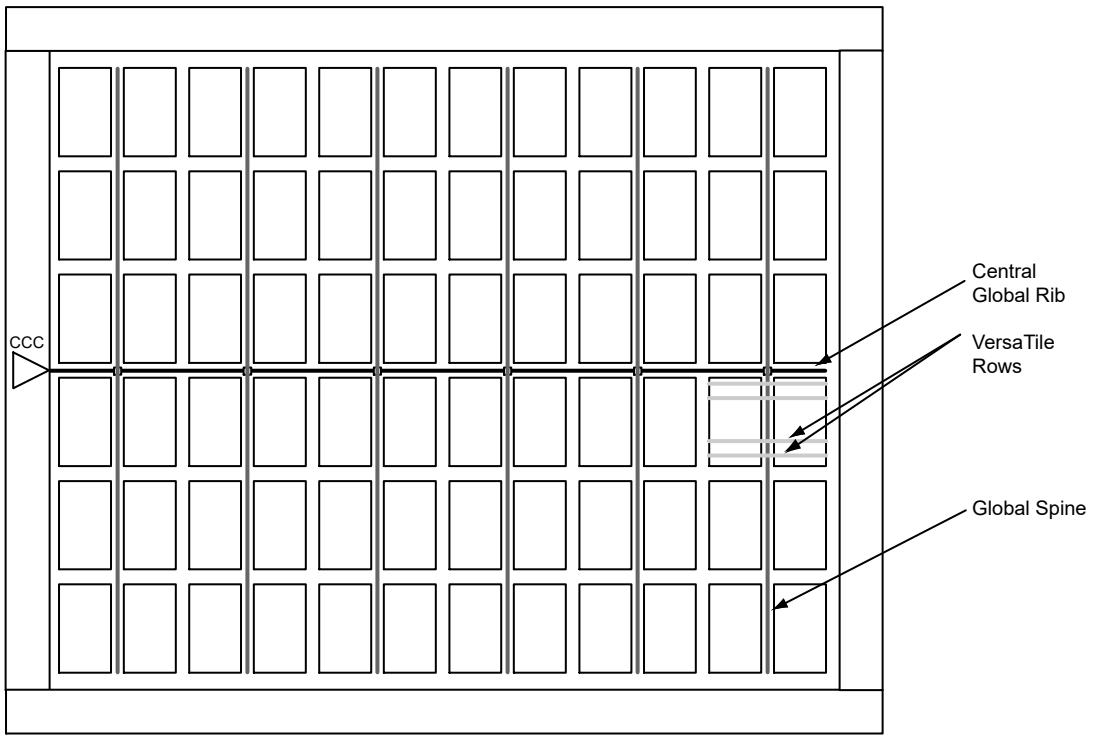
Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.5 Global Resource Characteristics (Ask a Question)

2.5.1 A3PN250 Clock Tree Topology (Ask a Question)

Clock delays are device-specific. The following figure is an example of a global tree used for clock routing. The global tree presented in the following figure is driven by a CCC located on the west side of the A3PN250 device. It is used to drive all D-flip-flops in the device.

Figure 2-23. Example of Global Tree Use in an A3PN250 Device for Clock Routing



2.5.2 Global Tree Timing Characteristics (Ask a Question)

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, see the 2.6. Clock Conditioning Circuits. Table 2-67 to Table 2-72 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

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Timing Characteristics

Table 2-67. A3PN010 Global Resource—Commercial-Case Conditions: T_J = 70 °C, VCC = 1.425V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	0.60	0.79	0.69	0.90	0.81	1.06	ns
t_{RCKH}	Input HIGH Delay for Global Clock	0.62	0.84	0.70	0.96	0.82	1.12	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock	0.75	—	0.85	—	1.00	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock	0.85	—	0.96	—	1.13	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.22	—	0.26	—	0.30	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, see Table 2-6 for derating values.

Table 2-68. A3PN015 Global Resource—Commercial-Case Conditions: TJ = 70 °C, VCC = 1.425V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	0.66	0.91	0.75	1.04	0.89	1.22	ns
t_{RCKH}	Input HIGH Delay for Global Clock	0.67	0.96	0.77	1.10	0.90	1.29	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock	0.75	—	0.85	—	1.00	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock	0.85	—	0.96	—	1.13	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.29	—	0.33	—	0.39	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, see Table 2-6 for derating values.

Table 2-69. A3PN020 Global Resource—Commercial-Case Conditions: T_J = 70 °C, VCC = 1.425V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	0.66	0.91	0.75	1.04	0.89	1.22	ns
t_{RCKH}	Input HIGH Delay for Global Clock	0.67	0.96	0.77	1.10	0.90	1.29	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock	0.75	—	0.85	—	1.00	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock	0.85	—	0.96	—	1.13	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.29	—	0.33	—	0.39	ns

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Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, see Table 2-6 for derating values.

Table 2-70. A3PN060 Global Resource—Commercial-Case Conditions: T_J = 70 °C, VCC = 1.425V

Parameter	Description	–2		–1		Std.		Units
		Min. [1]	Max. [2]	Min. [1]	Max. [2]	Min. [1]	Max. [2]	
t_{RCKL}	Input LOW Delay for Global Clock	0.72	0.91	0.82	1.04	0.96	1.22	ns
t_{RCKH}	Input HIGH Delay for Global Clock	0.71	0.94	0.81	1.07	0.96	1.26	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock	0.75	—	0.85	—	1.00	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock	0.85	—	0.96	—	1.13	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.23	—	0.26	—	0.31	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, see Table 2-6 for derating values.

Table 2-71. A3PN125 Global Resource—Commercial-Case Conditions: T_J = 70 °C, VCC = 1.425V

Parameter	Description	–2		–1		Std.		Units
		Min. [1]	Max. [2]	Min. [1]	Max. [2]	Min. [1]	Max. [2]	
t_{RCKL}	Input LOW Delay for Global Clock	0.76	0.99	0.87	1.12	1.02	1.32	ns
t_{RCKH}	Input HIGH Delay for Global Clock	0.76	1.02	0.87	1.17	1.02	1.37	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock	0.75	—	0.85	—	1.00	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock	0.85	—	0.96	—	1.13	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.26	—	0.30	—	0.35	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, see Table 2-6 for derating values.

Table 2-72. A3PN250 Global Resource—Commercial-Case Conditions: T_J = 70 °C, VCC = 1.425V

Parameter	Description	–2		–1		Std.		Units
		Min. [1]	Max. [2]	Min. [1]	Max. [2]	Min. [1]	Max. [2]	
t_{RCKL}	Input LOW Delay for Global Clock	0.79	1.02	0.90	1.16	1.06	1.36	ns
t_{RCKH}	Input HIGH Delay for Global Clock	0.78	1.04	0.88	1.18	1.04	1.39	ns

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.....continued

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock	0.75	—	0.85	—	1.00	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock	0.85	—	0.96	—	1.13	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.26	—	0.30	—	0.35	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, see Table 2-6 for derating values.

2.6 Clock Conditioning Circuits (Ask a Question)

2.6.1 CCC Electrical Specifications (Ask a Question)

Timing Characteristics

Table 2-73. ProASIC 3 nano CCC/PLL Specification

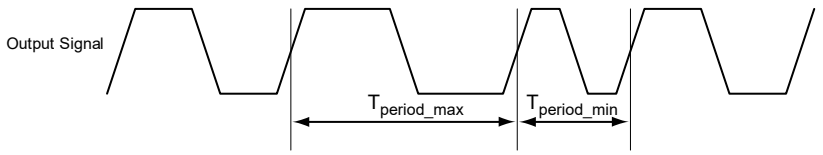
Parameter		Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}		1.5	—	350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}		0.75	—	350	MHz
Delay Increments in Programmable Delay Blocks [1,2]		—	200[3]	—	ps
Number of Programmable Values in Each Programmable Delay Block		—	—	32	
Serial Clock (SCLK) for Dynamic PLL [4,5]		—	—	125	MHz
Input Cycle-to-Cycle Jitter (peak magnitude)		—	—	1.5	ns
Acquisition Time	LockControl = 0	—	—	300	µs
	LockControl = 1	—	—	6.0	ms
Tracking Jitter [7]	LockControl = 0	—	—	1.6	ns
	LockControl = 1	—	—	0.8	ns
Output Duty Cycle		48.5	—	51.5	%
Delay Range in Block: Programmable Delay 1 [1,2]		1.25	—	15.65	ns
Delay Range in Block: Programmable Delay 2 [1,2]		0.025	—	15.65	ns
Delay Range in Block: Fixed Delay [1,2]		—	2.2	—	ns
VCO Output Peak-to-Peak Period Jitter F_{CCC_OUT} [6]		Max Peak-to-Peak Jitter Data [6,8,9]			
—		SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16
0.75 MHz to 50MHz		0.50%	0.50%	0.70%	1.00%
50 MHz to 250 MHz		1.00%	3.00%	5.00%	9.00%
250 MHz to 350 MHz		2.50%	4.00%	6.00%	12.00%

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Notes:

1. This delay is a function of voltage and temperature. See Table 2-6 for deratings.
2. T_J = 25 °C, VCC = 1.5V
3. When the CCC/PLL core is generated by Microchip core generator software, not all delay values of the specified delay increments are available. For more information, see the Libero SoC Online Help.
4. Maximum value obtained for a –2 speed-grade device in worst-case commercial conditions. For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.
5. The A3PN010, A3PN015, and A3PN020 devices do not support PLLs.
6. VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.
7. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.
8. Measurements done with LVTTL 3.3V 8 mA I/O drive strength and high slew rate. VCC/VCCPLL = 1.425V, VCCI = 3.3 , VQ/PQ/TQ type of packages, 20 pF load.
9. SSOs are outputs that are synchronous to a single clock domain, and have their clock-to-out times within ± 200 ps of each other.

Figure 2-24. Peak-to-Peak Jitter Definition



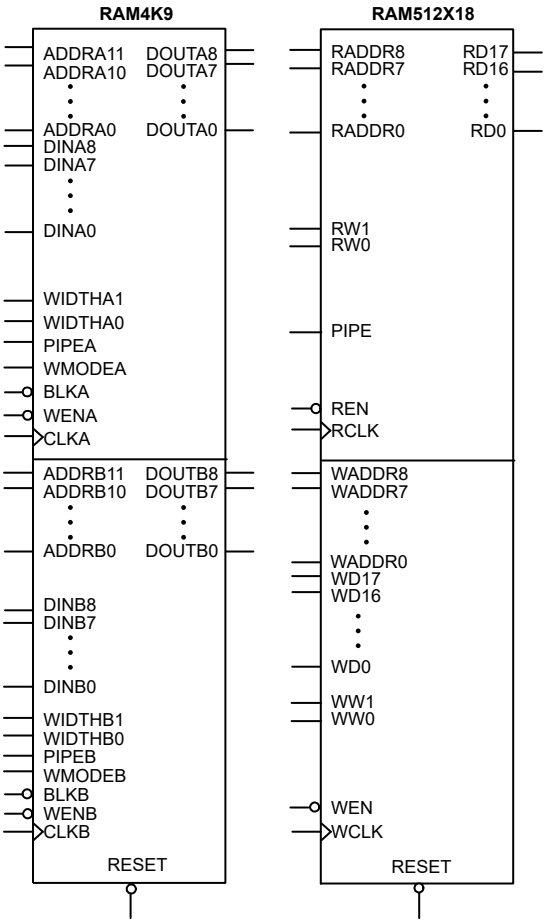
Note:
Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period_max} - T_{period_min}$.

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2.7 Embedded SRAM and FIFO Characteristics (Ask a Question)

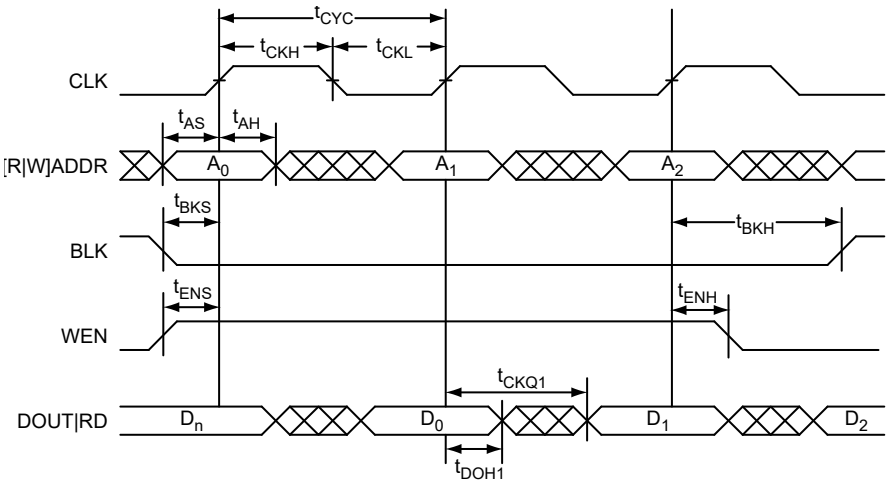
2.7.1 SRAM (Ask a Question)

Figure 2-25. RAM Models



2.7.1.1 Timing Waveforms (Ask a Question)

Figure 2-26. RAM Read for Pass-Through Output. Applicable to both RAM4K9 and RAM512x18



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Figure 2-27. RAM Read for Pipelined Output. Applicable to both RAM4K9 and RAM512x18

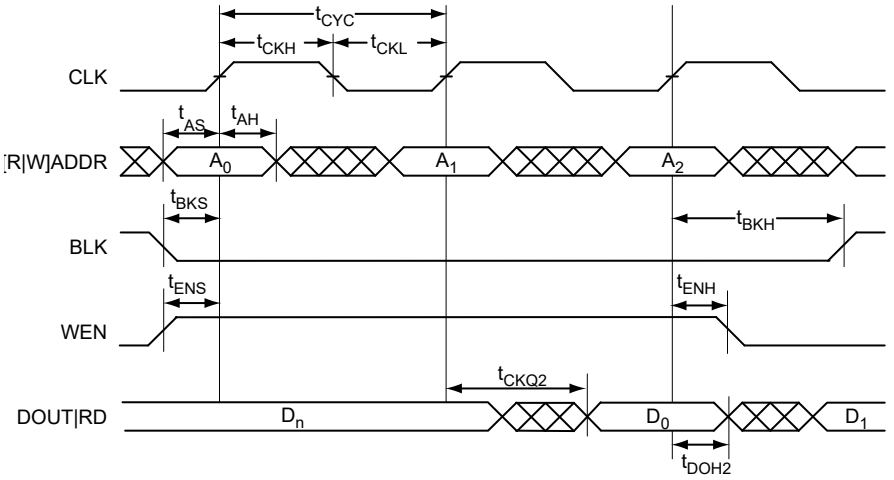
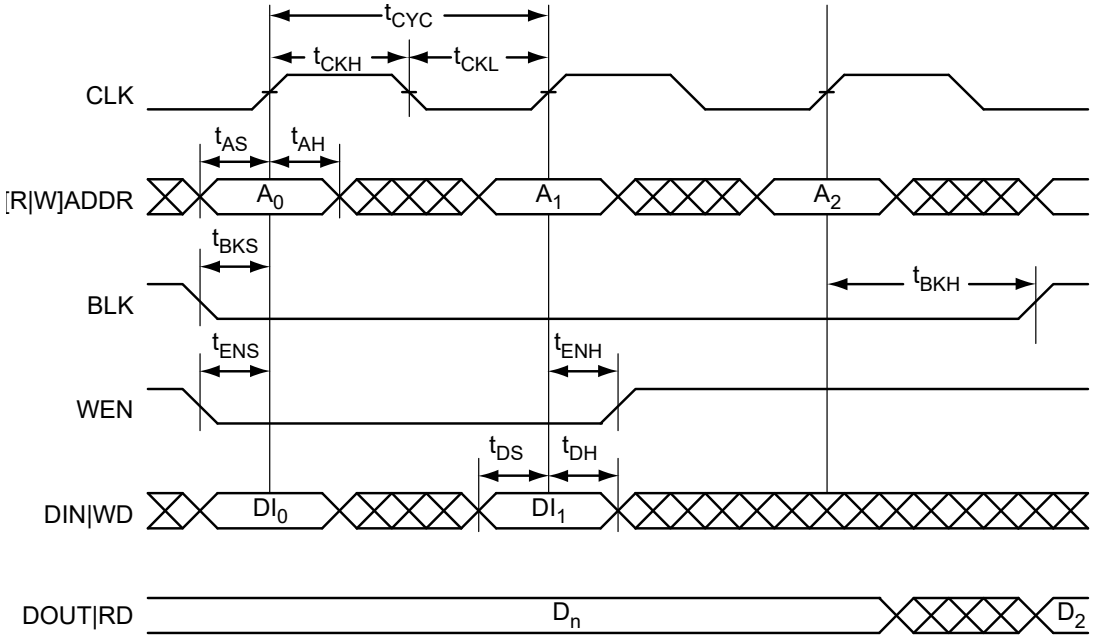


Figure 2-28. RAM Write, Output Retained. Applicable to both RAM4K9 and RAM512x18



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Figure 2-29. RAM Write, Output as Write Data (WMODE = 1). Applicable to both RAM4K9 only

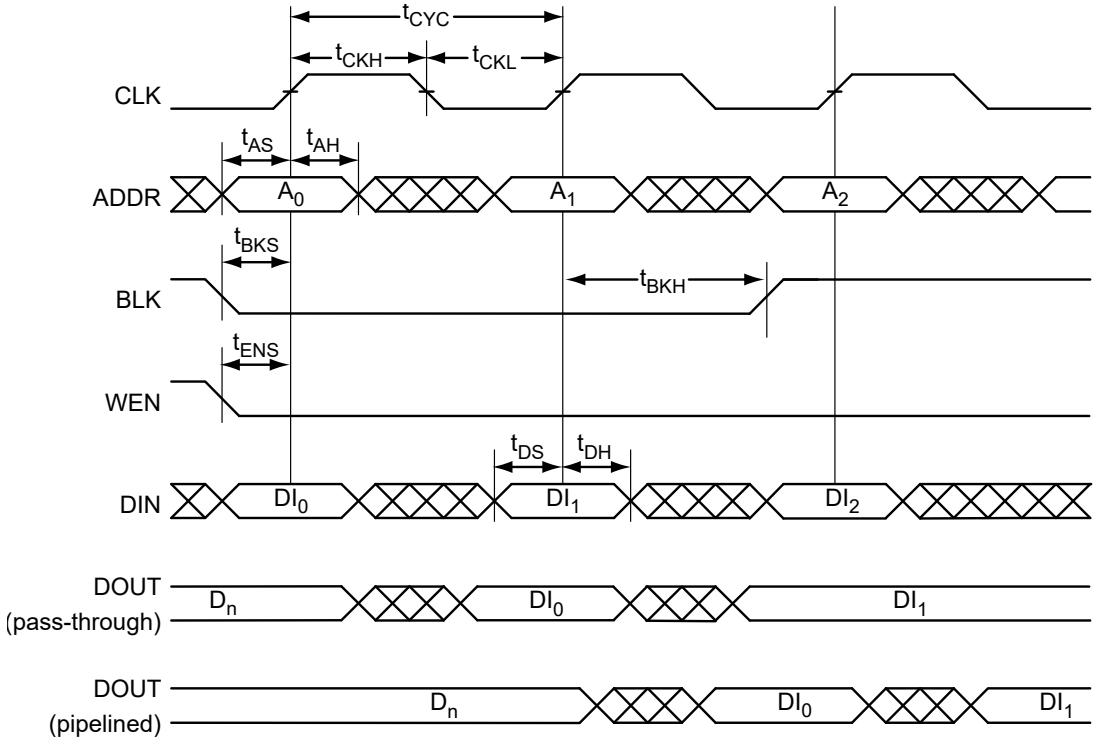
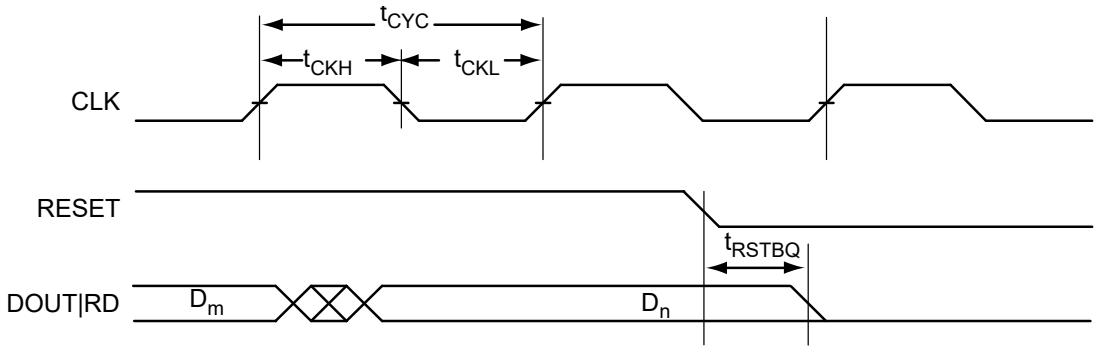


Figure 2-30. RAM Reset. Applicable to both RAM4K9 and RAM512x18



2.7.1.2 Timing Characteristics (Ask a Question)

Table 2-74. RAM4K9—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address Setup time	0.25	0.28	0.33	ns
t_{AH}	Address Hold time	0.00	0.00	0.00	ns
t_{ENS}	REN, WEN Setup time	0.14	0.16	0.19	ns
t_{ENH}	REN, WEN Hold time	0.10	0.11	0.13	ns
t_{BKS}	BLK Setup time	0.23	0.27	0.31	ns
t_{BKH}	BLK Hold time	0.02	0.02	0.02	ns
t_{DS}	Input data (DIN) Setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (DIN) Hold time	0.00	0.00	0.00	ns

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.....continued					
Parameter	Description	–2	–1	Std.	Units
t_{CKQ1}	Clock High to New Data Valid on DOUT (output retained, WMODE = 0)	1.79	2.03	2.39	ns
	Clock High to New Data Valid on DOUT (flow-through, WMODE = 1)	2.36	2.68	3.15	ns
t_{CKQ2}	Clock High to New Data Valid on DOUT (pipelined)	0.89	1.02	1.20	ns
t_{C2CWWL}[1]	Address collision clk-to-clk delay for reliable write after write on same address; applicable to closing edge	0.33	0.28	0.25	ns
t_{C2CWWH}[1]	Address collision clk-to-clk delay for reliable write after write on same address; applicable to rising edge	0.30	0.26	0.23	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.45	0.38	0.34	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	0.49	0.42	0.37	ns
t_{RSTBQ}	RESET Low to Data Out Low on DOUT (flow through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on DOUT (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET Recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency	310	272	231	MHz

Notes:

1. For more information, see the application note AC374: Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based FPGAs and SoC FPGAs App Note.
2. For specific junction temperature and voltage-supply levels, refer Table 2-6 for derating values.

Table 2-75. RAM512X18—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.28	0.33	ns
t_{AH}	Address hold time	0.00	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.09	0.10	0.12	ns
t_{ENH}	REN, WEN hold time	0.06	0.07	0.08	ns
t_{DS}	Input data (WD) setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	2.16	2.46	2.89	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.90	1.02	1.20	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.50	0.43	0.38	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	0.59	0.50	0.44	ns
t_{RSTBQ}	RESET LOW to data out LOW on RD (flow-through)	0.92	1.05	1.23	ns
	RESET LOW to data out LOW on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.21	0.24	0.29	ns
t_{CYC}	Clock cycle time	3.23	3.68	4.32	ns
F_{MAX}	Maximum frequency	310	272	231	MHz

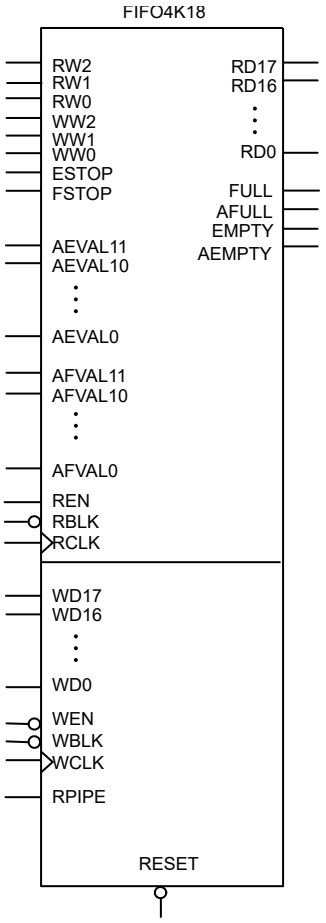
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Notes:

1. For more information, see the application note AC374: Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based FPGAs and SoC FPGAs App Note.
2. For specific junction temperature and voltage-supply levels, refer Table 2-6 for derating values.

2.7.2 FIFO (Ask a Question)

Figure 2-31. FIFO Model



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2.7.2.1 Timing Waveform (Ask a Question)

Figure 2-32. FIFO Read

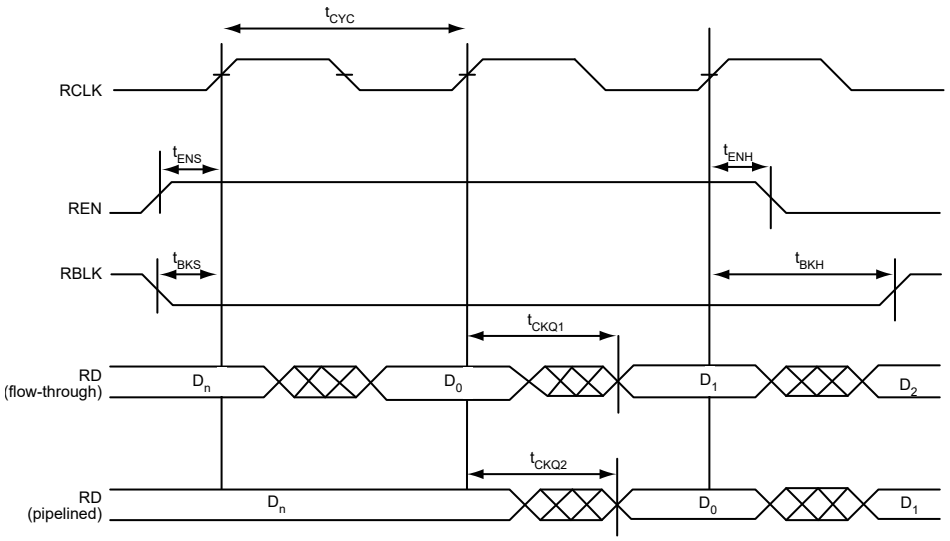
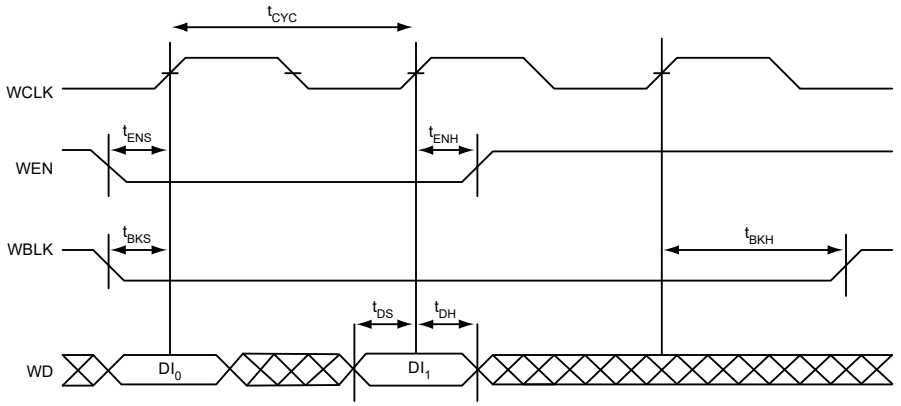


Figure 2-33. FIFO Write



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Figure 2-34. FIFO Reset

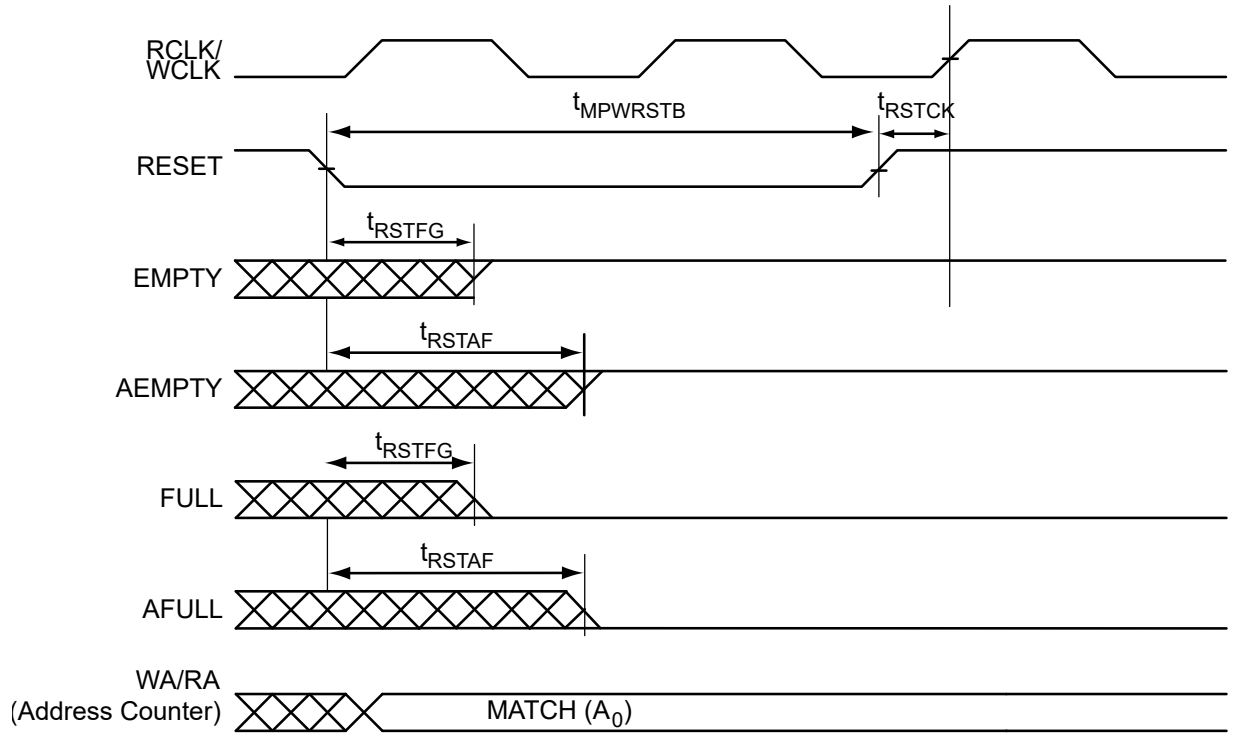
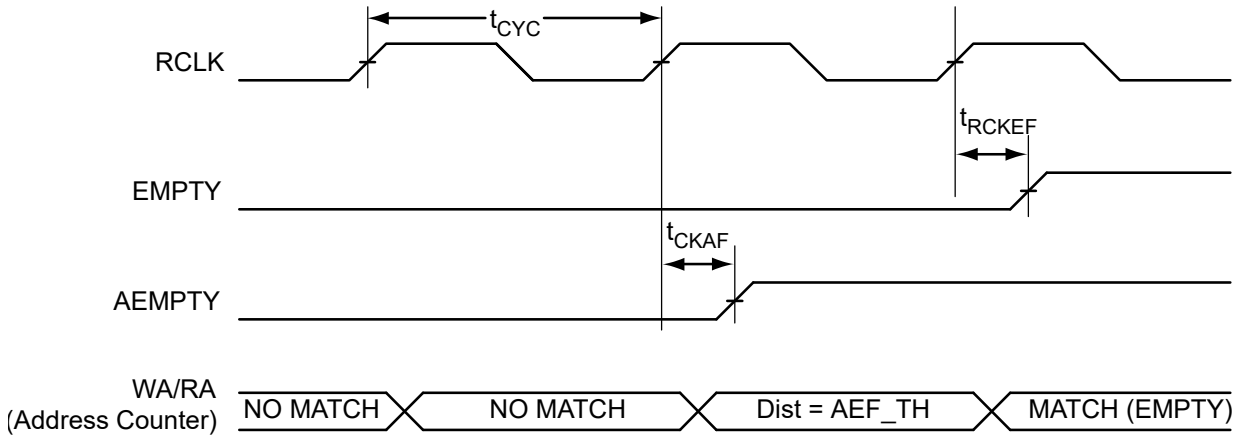


Figure 2-35. FIFO EMPTY Flag and AEMPTY Flag Assertion



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Figure 2-36. FIFO FULL Flag and AFULL Flag Assertion

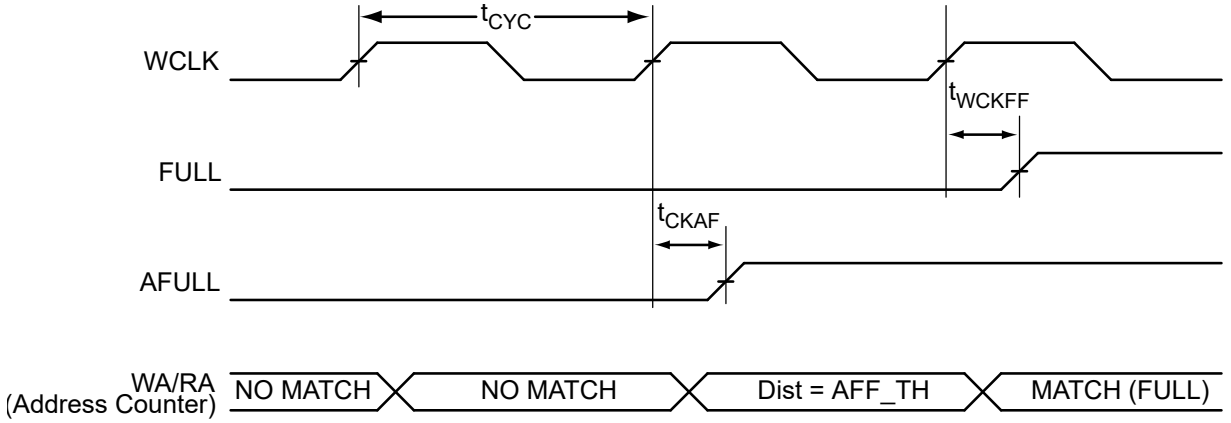


Figure 2-37. FIFO EMPTY Flag and AEMPTY Flag Deassertion

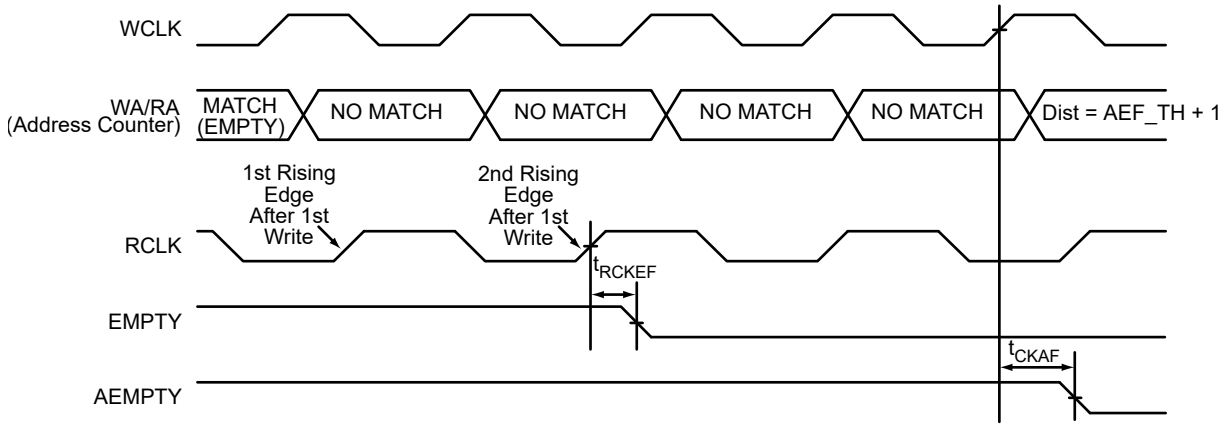
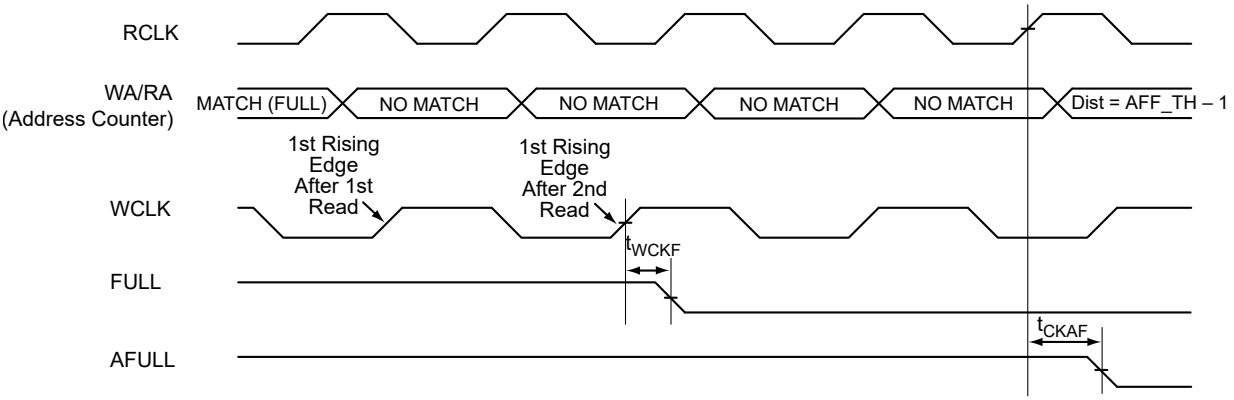


Figure 2-38. FIFO FULL Flag and AFULL Flag Deassertion



2.7.2.2 Timing Characteristics (Ask a Question)

Table 2-76. FIFO—Worst Commercial-Case Conditions: T_J = 70 °C, VCC = 1.425V

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.38	1.57	1.84	ns
t_{ENH}	REN, WEN Hold Time	0.02	0.02	0.02	ns
t_{BKS}	BLK Setup Time	0.22	0.25	0.30	ns

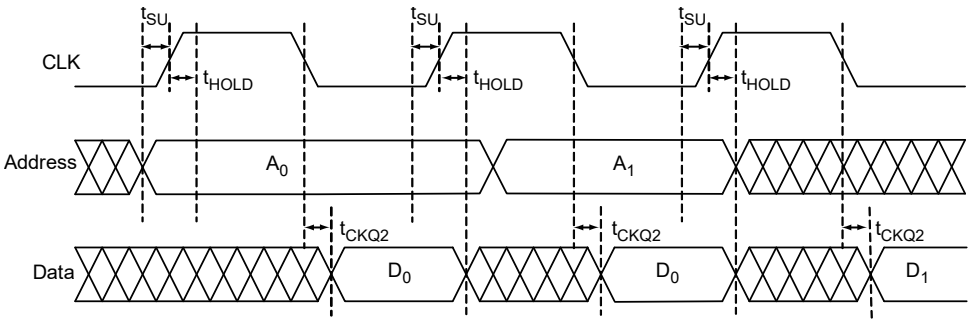
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.....continued					
Parameter	Description	–2	–1	Std.	Units
t_{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.36	2.68	3.15	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.89	1.02	1.20	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t_{RSTFG}	RESET LOW to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t_{RSTAF}	RESET LOW to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET Recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency for FIFO	310	272	231	MHz

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.8 Embedded FlashROM Characteristics (Ask a Question)

Figure 2-39. Timing Diagram



2.8.1 Timing Characteristics (Ask a Question)

Table 2-77. Embedded FlashROM Access Time—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V

Parameter	Description	–2	–1	Std.	Units
t_{SU}	Address Setup Time	0.53	0.61	0.71	ns
t_{HOLD}	Address Hold Time	0.00	0.00	0.00	ns
t_{CK2Q}	Clock to Out	16.23	18.48	21.73	ns
F_{MAX}	Maximum Clock Frequency	15.00	15.00	15.00	MHz

2.9 JTAG 1532 Characteristics (Ask a Question)

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; see the I/O timing characteristics in the 2.6. Clock Conditioning Circuits for more details.

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2.9.1 Timing Characteristics (JTAG 1532 Characteristics) (Ask a Question)

Table 2-78. JTAG 1532—Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V

Parameter	Description	–2	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.53	0.60	0.71	ns
t_{DIHD}	Test Data Input Hold Time	1.07	1.21	1.42	ns
t_{TMSSU}	Test Mode Select Setup Time	0.53	0.60	0.71	ns
t_{TMDHD}	Test Mode Select Hold Time	1.07	1.21	1.42	ns
t_{TCK2Q}	Clock to Q (data out)	6.39	7.24	8.52	ns
t_{RSTB2Q}	Reset to Q (data out)	21.31	24.15	28.41	ns
F_{TCKMAX}	TCK Maximum Frequency	23.00	20.00	17.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.00	0.00	0.00	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.21	0.24	0.28	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	—	—	—	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

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3. Pin Descriptions and Packaging (Ask a Question)

3.1 Supply Pins (Ask a Question)

GND Ground

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ Ground (Quiet)

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC Core Supply Voltage

Supply voltage to the FPGA core, nominally 1.5V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

VCCIBx I/O Supply Voltage

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5V, 1.8V, 2.5V, or 3.3V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VMVx I/O Supply Voltage (Quiet)

Quiet supply voltage to the input buffers of each I/O bank. x is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5V, 1.8V, 2.5V, or 3.3V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (That is, VMV0 to VCCIB0, VMV1 to VCCIB1, and so on).

VCCPLA/B/C/D/E/F PLL Supply Voltage

Supply voltage to analog PLL, nominally 1.5V.

When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microchip recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. For a complete board solution for the PLL analog power supply and ground, see the PLL Power Supply Decoupling section of the “Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs” chapter of the ProASIC 3 nano FPGA Fabric User's Guide.

There is one VCCPLF pin on ProASIC 3 nano devices.

VCOMPLA/B/C/D/E/F PLL Ground

Ground to analog PLL power supplies. When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on ProASIC 3 nano devices.

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VJTAG JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5V to 3.3V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microchip recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

VPUMP Programming Supply Voltage

ProASIC 3 devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microchip recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

3.2 User Pins (Ask a Question)

I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the “Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs” chapter of the ProASIC 3 nano FPGA Fabric User's Guide. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

For an explanation of the naming of global pins, see the I/O Structure chapter of the ProASIC 3 nano FPGA Fabric User's Guide .

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3.3 JTAG Pins (Ask a Question)

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5V to 3.3V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microchip recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500Ω to 1 kΩ will satisfy the requirements. For more information, see Table 3-1 .

Table 3-1. Recommended Tie-Off Values for the TCK and TRST Pins

VJTAG	Tie-Off Resistance
VJTAG at 3.3V	200Ω to 1 kΩ
VJTAG at 2.5V	200Ω to 1 kΩ
VJTAG at 1.8V	500Ω to 1 kΩ
VJTAG at 1.5V	500Ω to 1 kΩ

Notes:

1. Equivalent parallel resistance if more than one device is on the JTAG chain
2. The TCK pin can be pulled up/down.
3. The TRST pin is pulled down.

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-1 and must satisfy the parallel resistance value requirement. The values in Table 3-1 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microchip recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500W to 1 kW will satisfy the requirements.

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3.4 Special Function Pins (Ask a Question)

NC No Connect

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC Do Not Connect

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

3.5 Packaging (Ask a Question)

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microchip consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microchip IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Microchip offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

3.6 Related Documents (Ask a Question)

User's Guides

ProASIC 3 nano FPGA Fabric User's Guide

Packaging

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

This document contains the package mechanical drawings for all packages currently or previously supplied by Microchip. Use the bookmarks to navigate to the package mechanical drawings.

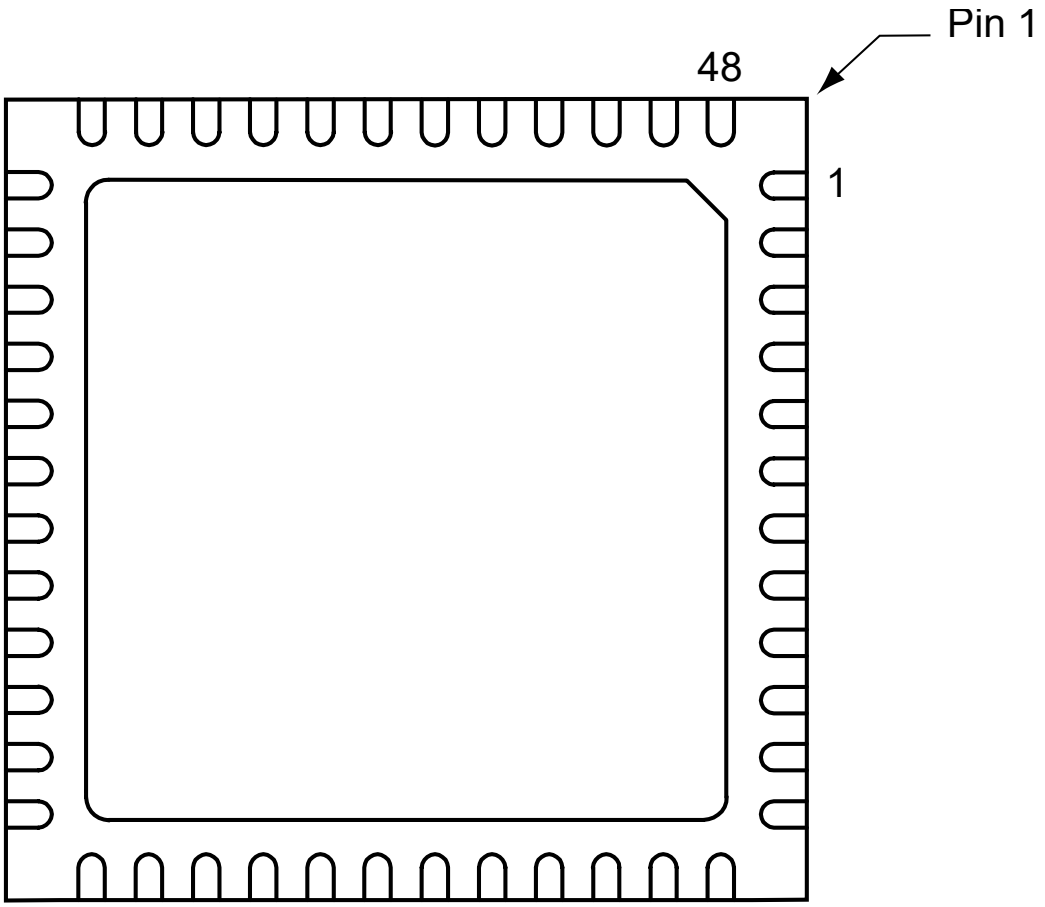
Additional packaging materials: www.microchip.com/en-us/support/package-drawings/fpga-packaging .

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4. Package Pin Assignments (Ask a Question)

4.1 48-Pin QFN (Ask a Question)

Figure 4-1. 48-Pin QFN



Notes:

1. This is the bottom view of the package.
2. The die attach paddle of the package is tied to ground (GND).

Note:
For Package Manufacturing and Environmental information, visit the Resource Center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

48-Pin QFN	
Pin Number	**A3PN010 Function**
1	GEC0/IO37RSB1
2	IO36RSB1
3	GEA0/IO34RSB1
4	IO22RSB1
5	GND
6	VCCIB1
7	IO24RSB1
8	IO33RSB1

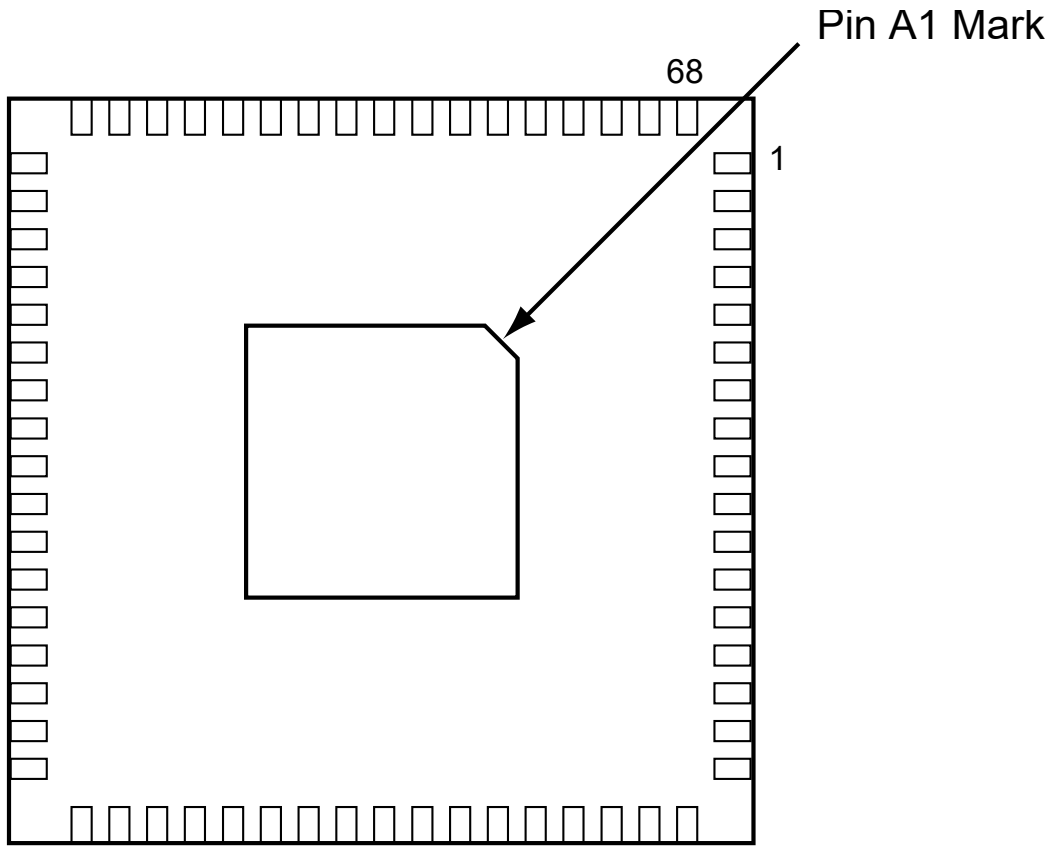
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.....continued	
48-Pin QFN	
Pin Number	**A3PN010 Function**
9	IO26RSB1
10	IO32RSB1
11	IO27RSB1
12	IO29RSB1
13	IO30RSB1
14	IO31RSB1
15	IO28RSB1
16	IO25RSB1
17	IO23RSB1
18	VCC
19	VCCIB1
20	IO17RSB1
21	IO14RSB1
22	TCK
23	TDI
24	TMS
25	VPUMP
26	TDO
27	TRST
28	VJTAG
29	IO11RSB0
30	IO10RSB0
31	IO09RSB0
32	IO08RSB0
33	VCCIB0
34	GND
35	VCC
36	IO07RSB0
37	IO06RSB0
38	GDA0/IO05RSB0
39	IO03RSB0
40	GDC0/IO01RSB0
41	IO12RSB1
42	IO13RSB1
43	IO15RSB1
44	IO16RSB1
45	IO18RSB1
46	IO19RSB1
47	IO20RSB1
48	IO21RSB1

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4.2 68-Pin QFN (Ask a Question)

Figure 4-2. 68-Pin QFN



Notes:

1. This is the bottom view of the package.
2. The die attach paddle of the package is tied to ground (GND).

Note:
For Package Manufacturing and Environmental information, visit the Resource Center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

68-Pin QFN	
Pin Number	**A3PN015 Function**
1	IO60RSB2
2	IO54RSB2
3	IO52RSB2
4	IO50RSB2
5	IO49RSB2
6	GEC0/IO48RSB2
7	GEA0/IO47RSB2
8	VCC
9	GND
10	VCCIB2
11	IO46RSB2
12	IO45RSB2

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.....continued	
68-Pin QFN	
Pin Number	**A3PN015 Function**
13	IO44RSB2
14	IO43RSB2
15	IO42RSB2
16	IO41RSB2
17	IO40RSB2
18	IO39RSB1
19	IO37RSB1
20	IO35RSB1
21	IO33RSB1
22	IO31RSB1
23	IO30RSB1
24	VCC
25	GND
26	VCCIB1
27	IO27RSB1
28	IO25RSB1
29	IO23RSB1
30	IO21RSB1
31	IO19RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO
37	TRST
38	VJTAG
39	IO17RSB0
40	IO16RSB0
41	GDA0/IO15RSB0
42	GDC0/IO14RSB0
43	IO13RSB0
44	VCCIB0
45	GND
46	VCC
47	IO12RSB0
48	IO11RSB0
49	IO09RSB0
50	IO05RSB0
51	IO00RSB0
52	IO07RSB0
53	IO03RSB0
54	IO18RSB1
55	IO20RSB1
56	IO22RSB1

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.....continued	
68-Pin QFN	
Pin Number	**A3PN015 Function**
57	IO24RSB1
58	IO28RSB1
59	NC
60	GND
61	NC
62	IO32RSB1
63	IO34RSB1
64	IO36RSB1
65	IO61RSB2
66	IO58RSB2
67	IO56RSB2
68	IO63RSB2

68-Pin QFN	
Pin Number	**A3PN020 Function**
1	IO60RSB2
2	IO54RSB2
3	IO52RSB2
4	IO50RSB2
5	IO49RSB2
6	GEC0/IO48RSB2
7	GEA0/IO47RSB2
8	VCC
9	GND
10	VCCIB2
11	IO46RSB2
12	IO45RSB2
13	IO44RSB2
14	IO43RSB2
15	IO42RSB2
16	IO41RSB2
17	IO40RSB2
18	IO39RSB1
19	IO37RSB1
20	IO35RSB1
21	IO33RSB1
22	IO31RSB1
23	IO30RSB1
24	VCC
25	GND
26	VCCIB1
27	IO27RSB1
28	IO25RSB1
29	IO23RSB1

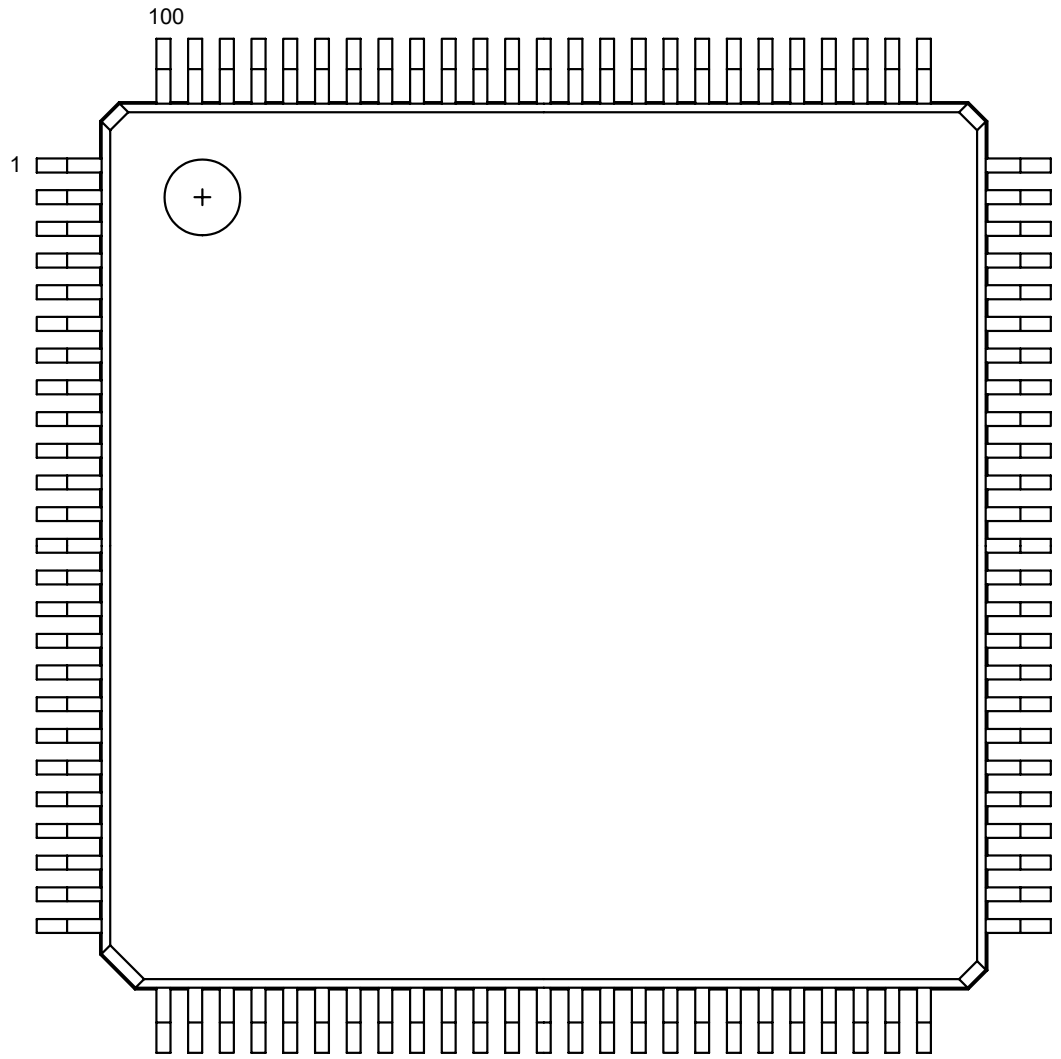
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.....continued	
68-Pin QFN	
Pin Number	**A3PN020 Function**
30	IO21RSB1
31	IO19RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO
37	TRST
38	VJTAG
39	IO17RSB0
40	IO16RSB0
41	GDA0/IO15RSB0
42	GDC0/IO14RSB0
43	IO13RSB0
44	VCCIB0
45	GND
46	VCC
47	IO12RSB0
48	IO11RSB0
49	IO09RSB0
50	IO05RSB0
51	IO00RSB0
52	IO07RSB0
53	IO03RSB0
54	IO18RSB1
55	IO20RSB1
56	IO22RSB1
57	IO24RSB1
58	IO28RSB1
59	NC
60	GND
61	NC
62	IO32RSB1
63	IO34RSB1
64	IO36RSB1
65	IO61RSB2
66	IO58RSB2
67	IO56RSB2
68	IO63RSB2

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4.3 100-Pin VQFP (Ask a Question)

Figure 4-3. 100-Pin VQFP



Note: This is the top view of the package.

Note: For Package Manufacturing and Environmental information, visit the Resource Center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

100-Pin VQFP	
Pin Number	**A3PN060 Function**
1	GND
2	GAA2/IO51RSB1
3	IO52RSB1
4	GAB2/IO53RSB1
5	IO95RSB1
6	GAC2/IO94RSB1
7	IO93RSB1
8	IO92RSB1
9	GND

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.....continued	
100-Pin VQFP	
Pin Number	**A3PN060 Function**
10	GFB1/IO87RSB1
11	GFB0/IO86RSB1
12	VCOMPLF
13	GFA0/IO85RSB1
14	VCCPLF
15	GFA1/IO84RSB1
16	GFA2/IO83RSB1
17	VCC
18	VCCIB1
19	GEC1/IO77RSB1
20	GEB1/IO75RSB1
21	GEB0/IO74RSB1
22	GEA1/IO73RSB1
23	GEA0/IO72RSB1
24	VMV1
25	GNDQ
26	GEA2/IO71RSB1
27	GEB2/IO70RSB1
28	GEC2/IO69RSB1
29	IO68RSB1
30	IO67RSB1
31	IO66RSB1
32	IO65RSB1
33	IO64RSB1
34	IO63RSB1
35	IO62RSB1
36	IO61RSB1
37	VCC
38	GND
39	VCCIB1
40	IO60RSB1
41	IO59RSB1
42	IO58RSB1
43	IO57RSB1
44	GDC2/IO56RSB1
45	GDB2/IO55RSB1
46	GDA2/IO54RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC

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.....continued	
100-Pin VQFP	
Pin Number	**A3PN060 Function**
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO49RSB0
58	GDC0/IO46RSB0
59	GDC1/IO45RSB0
60	GCC2/IO43RSB0
61	GCB2/IO42RSB0
62	GCA0/IO40RSB0
63	GCA1/IO39RSB0
64	GCC0/IO36RSB0
65	GCC1/IO35RSB0
66	VCCIB0
67	GND
68	VCC
69	IO31RSB0
70	GBC2/IO29RSB0
71	GBB2/IO27RSB0
72	IO26RSB0
73	GBA2/IO25RSB0
74	VMV0
75	GNDQ
76	GBA1/IO24RSB0
77	GBA0/IO23RSB0
78	GBB1/IO22RSB0
79	GBB0/IO21RSB0
80	GBC1/IO20RSB0
81	GBC0/IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO15RSB0
85	IO13RSB0
86	IO11RSB0
87	VCCIB0
88	GND
89	VCC
90	IO10RSB0
91	IO09RSB0
92	IO08RSB0
93	GAC1/IO07RSB0
94	GAC0/IO06RSB0
95	GAB1/IO05RSB0
96	GAB0/IO04RSB0
97	GAA1/IO03RSB0

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.....continued	
100-Pin VQFP	
Pin Number	**A3PN060 Function**
98	GAA0/IO02RSB0
99	IO01RSB0
100	IO00RSB0

100-Pin VQFP	
Pin Number	**A3PN125 Function**
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	VCOMPLF
13	GFA0/IO122RSB1
14	VCCPLF
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	VCC
18	VCCIB1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	GEB2/IO105RSB1
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1
36	IO93RSB1
37	VCC
38	GND

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.....continued	
100-Pin VQFP	
Pin Number	**A3PN125 Function**
39	VCCIB1
40	IO87RSB1
41	IO84RSB1
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	VCCIB0
67	GND
68	VCC
69	IO47RSB0
70	GBC2/IO45RSB0
71	GBB2/IO43RSB0
72	IO42RSB0
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0

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.....continued	
100-Pin VQFP	
Pin Number	**A3PN125 Function**
83	IO28RSB0
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0

100-Pin VQFP	
Pin Number	**A3PN250 Function**
1	GND
2	GAA2/IO67RSB3
3	IO66RSB3
4	GAB2/IO65RSB3
5	IO64RSB3
6	GAC2/IO63RSB3
7	IO62RSB3
8	IO61RSB3
9	GND
10	GFB1/IO60RSB3
11	GFB0/IO59RSB3
12	VCOMPLF
13	GFA0/IO57RSB3
14	VCCPLF
15	GFA1/IO58RSB3
16	GFA2/IO56RSB3
17	VCC
18	VCCIB3
19	GFC2/IO55RSB3
20	GEC1/IO54RSB3
21	GEC0/IO53RSB3
22	GEA1/IO52RSB3
23	GEA0/IO51RSB3

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.....continued	
100-Pin VQFP	
Pin Number	**A3PN250 Function**
24	VMV3
25	GNDQ
26	GEA2/IO50RSB2
27	GEB2/IO49RSB2
28	GEC2/IO48RSB2
29	IO47RSB2
30	IO46RSB2
31	IO45RSB2
32	IO44RSB2
33	IO43RSB2
34	IO42RSB2
35	IO41RSB2
36	IO40RSB2
37	VCC
38	GND
39	VCCIB2
40	IO39RSB2
41	IO38RSB2
42	IO37RSB2
43	GDC2/IO36RSB2
44	GDB2/IO35RSB2
45	GDA2/IO34RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO33RSB1
58	GDC0/IO32RSB1
59	GDC1/IO31RSB1
60	IO30RSB1
61	GCB2/IO29RSB1
62	GCA1/IO27RSB1
63	GCA0/IO28RSB1
64	GCC0/IO26RSB1
65	GCC1/IO25RSB1
66	VCCIB1
67	GND

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.....continued	
100-Pin VQFP	
Pin Number	**A3PN250 Function**
68	VCC
69	IO24RSB1
70	GBC2/IO23RSB1
71	GBB2/IO22RSB1
72	IO21RSB1
73	GBA2/IO20RSB1
74	VMV1
75	GNDQ
76	GBA1/IO19RSB0
77	GBA0/IO18RSB0
78	GBB1/IO17RSB0
79	GBB0/IO16RSB0
80	GBC1/IO15RSB0
81	GBC0/IO14RSB0
82	IO13RSB0
83	IO12RSB0
84	IO11RSB0
85	IO10RSB0
86	IO09RSB0
87	VCCIB0
88	GND
89	VCC
90	IO08RSB0
91	IO07RSB0
92	IO06RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

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5. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
Revision A	02/2024	The following is the summary of changes in revision A of this document: • Migrated this document into Microchip template format and updated the hyperlinks with the recent references. • Added Introduction • Updated the following tables to include A3PN015 device which was removed in the previous revision: – Table 1, Table 2, Table 4, and Table 5 • Added table note stating “Not recommended for new designs. (CN1203)” in Table 1 and Table 2. • Updated Figure 1 to include A3PN015 device. • Updated the following tables to include A3PN015 device: – Table 2-7, Table 2-10, and Table 2-11 • Updated note 2 in Table 2-9 to include A3PN015 device. The revised note states that the values for A3PN020, A3PN015, and A3PN010. A3PN060, A3PN125, and A3PN250 correspond to a default loading of 35 pF. • Added Table 2-68 • Updated the titles of the following tables to include a reference to the A3PN015 device: – Table 2-19, Table 2-31, Table 2-32, Table 2-36, Table 2-37, Table 2-42, Table 2-43, Table 2-48, Table 2-49, Table 2-54, and Table 2-55 • Updated note 5 in Table 2-73. The revised note states that the A3PN010, A3PN015, and A3PN020 devices do not support PLLs. • Added A3PN015 Function tables in 4.2. 68-Pin QFN.
Revision 13	11/2019	The following is the summary of changes in revision 13 of this document: • Removed the device A3PN015 and A3PN030Z names from across the document as they are obsolete. • Removed the nano device names across the document. • Updated the ProASIC 3 nano Ordering Information as required.
Revision 12	09/2015	The following is the summary of changes in revision 12 of this document: • Changed Temperature Range of Commercial from “0 °C to 85 °C” to “-20 °C to 85 °C” in ProASIC 3 nano Ordering Information • Modified the enhanced commercial temperature range in Features and Benefits . • Modified the note to include device/package obsoletion information in Table 1 . • Added a note under Security Feature “Y” in ProASIC 3 nano Ordering Information. • Modified the note in Temperature Grade Offering. • Modified the note in Speed Grade and Temperature Grade Matrix. • Deleted details related to Ambient temperature and modified junction temperature range in Table 2-2 .

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Revision	Date	Description
Revision 11	01/2013	The following is the summary of changes in revision 11 of this document: • The ProASIC 3 nano Ordering Information has been updated to mention “Y” as “Blank” mentioning “Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio” . • Added a Note stating “VMV pins must be connected to the corresponding VCCI pins. See the 3.1. VMVx I/O Supply Voltage (Quiet) for further information” to Table 2-1 . • Added a note to Table 2-2: The programming temperature range supported is $T_{ambient}$ = 0 °C to 85 °C. • The note in Table 2-73 referring the reader to SmartGen was revised to refer instead to the online help associated with the core . • Figure 2-32 and Figure 2-33 are new . • Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document . Live at Power-Up (LAPU) has been replaced with ’Instant On’.
Revision 10	09/2012	The following is the summary of changes in revision 10 of this document: • The Security section was modified to clarify that Microchip does not support read-back of programmed data.

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Revision	Date	Description
Revision 9	03/2012	The following is the summary of changes in revision 9 of this document: • The In-System Programming (ISP) and Security and Security sections were revised to clarify that although no existing security measures can give an absolute guarantee, Microchip FPGAs implement the best security available in the industry . • Notes indicating that A3P015 is not recommended for new designs have been added . Notes indicating that nano-Z devices are not recommended for use in new designs have been added. The “Devices Not Recommended For New Designs” section is new. • The Y security option and Licensed DPA Logo were added to the ProASIC 3 nano Ordering Information. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research . • Corrected the Commercial Temperature range to reflect a range of 0 °C to 70 °C instead of –20 °C to 70 °C in the ProASIC 3 nano Ordering Information, Temperature Grade Offering, and the Speed Grade and Temperature Grade Matrix sections. • The following sentence was removed from the 1.1.3. Advanced Architecture: “In addition, extensive on-chip programming circuitry enables rapid, single-voltage (3.3V) programming of IGLOO nano devices via an IEEE 1532 JTAG interface” . • The 1.1.5. Specifying I/O States During Programming is new . • The reference to guidelines for global spines and VersaTile rows, given in the Global Clock contribution—PCLOCK, was corrected to the “Spine Architecture” section of the Global Resources chapter in the IProASIC 3 nano FPGA Fabric User's Guide . • Figure 2-3 has been modified for the DIN waveform; the Rise and Fall time label has been changed to t_{DIN} (37114). • The notes regarding drive strength in the 2.3.2.2. Summary of I/O Timing Characteristics—Default I/O Software Settings and 2.3.4.2. 3.3V LVCMOS Wide Range tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is ±100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, see the IBIS models . • The AC Loading figures in the 2.3.4. Single-Ended I/O Characteristics were updated to match tables in the 2.3.2.2. Summary of I/O Timing Characteristics—Default I/O Software Settings. • Added values for minimum pulse width and removed the FRMAX row from Table 2-67 through Table 2-72 in the 2.5.2. Global Tree Timing Characteristics. Use the software to determine the FRMAX for the device you are using. • Table 2-73 was updated. A note was added indicating that when the CCC/PLL core is generated by Microchip core generator software, not all delay values of the specified delay increments are available. • The port names in the SRAM 2.7.1.1. Timing Waveforms, SRAM 2.7.1.2. Timing Characteristics tables, Figure 2-34, and the FIFO 2.7.2.2. Timing Characteristics tables were revised to ensure consistency with the software names . Reference was made to a new application note, Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs, which covers these cases in detail. • The 3. Pin Descriptions and Packaging chapter has been added.

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Revision	**Date**	**Description**
	07/2010	• The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The ProASIC 3 nano Device Status indicates the status for each device in the device family.
Revision 8	04/2010	The following is the summary of changes in revision 8 of this document: • References to differential inputs were removed from the datasheet, since ProASIC 3 nano devices do not support differential inputs. • The Table 4 is new. • The JTAG DC voltage was revised in Table 2-2. The maximum value for VPUMP programming voltage (operation mode) was changed from 3.45V to 3.6V. • The highest temperature in Table 2-6 was changed to 100 °C. • The typical value for A3PN010 was revised in Table 2-7. The note was revised to remove the statement that values do not include I/O static contribution. • The following tables were updated with available information: Table 2-8; Table 2-9; Table 2-10; Table 2-14; Table 2-18; Table 2-19 • Table 2-22 was revised to add wide range data and correct the formulas in the table notes. • The text introducing Table 2-24 was revised to state six months at 100° instead of three months at 110° for reliability concerns. The row for 110° was removed from the table. • Table 2-26 was revised to give values with Schmitt trigger disabled and enabled. The temperature for reliability was changed to 100 °C. • Table 2-33 and the timing tables in the 2.3.4. Single-Ended I/O Characteristics were updated with available information. The timing tables for 3.3V LVCMOS wide range are new. • The following sentence was deleted from the 2.3.4.3. 2.5V LVCMOS: “It uses a 5 V–tolerant input buffer and push-pull output buffer.” • Values for $t_{DDRISUD}$ and $F_{DDRIMAX}$ were updated in Table 2-62. Values for F_{DDOMAX} were added to Table 2-64. • Table 2-67 through Table 2-70 were updated with available information. • Table 2-73 was revised.
Revision 7 Product Brief Advance v0.7 Packaging Advance v0.6	01/2010	The following is the summary of changes in revision 7 of this document: • All product tables and pin tables were updated to show clearly that A3PN030 is available only in the Z feature at this time, as A3PN030Z. The nano-Z feature grade devices are designated with a Z at the end of the part number. • The “68-Pin QFN” and “100-Pin VQFP” pin tables for A3PN030 were removed. Only the Z grade for A3PN030 is available at this time.

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Revision	Date	Description
Revision 6 Product Brief Advance v0.6 Packaging Advance v0.5	08/2009	The following is the summary of changes in revision 6 of this document: • The note for A3PN030 in the Table 1 table was revised. It states A3PN030 is available in the Z feature grade only. • The "68-Pin QFN" pin table for A3PN030 is new. • The 4.1. 48-Pin QFN, 4.2. 68-Pin QFN, and 4.3. 100-Pin VQFP pin tables for A3PN030Z are new. • The 4.3. 100-Pin VQFP pin table for A3PN060Z is new. • The 4.3. 100-Pin VQFP pin table for A3PN125Z is new • The 4.3. 100-Pin VQFP pin table for A3PN250Z is new.
Revision 5 Product Brief Advance v0.5	03/2009	The following is the summary of changes in revision 5 of this document: • All references to speed grade –F were removed from this document. • The 1.1.3. I/Os with Advanced I/O Standards was revised to add definitions of hot-swap and cold-sparing.
Revision 4 Packaging Advance v0.4	02/2009	The following is the summary of changes in revision 4 of this document: • The 4.3. 100-Pin VQFP pin table for A3PN030 is new.
Revision 3 Packaging Advance v0.3	02/2009	The following is the summary of changes in revision 3 of this document: • The "100-Pin QFN" section was removed.
Revision 2 Product Brief Advance v0.4	11/2008	The following is the summary of changes in revision 2 of this document: • The Table 1 was revised to change the maximum user I/Os for A3PN020 and A3PN030. The following table note was removed: "Six chip (main) and three quadrant global networks are available for A3PN060 and above." • The QN100 package was removed for all devices. • The Device Marking is new.

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Revision	**Date**	**Description**
Revision 1 Product Brief Advance v0.3 DC and Switching Characteristics Advance v0.2 Packaging Advance v0.2	10/2008	The following is the summary of changes in revision 1 of this document: • The A3PN030 device was added to product tables and replaces A3P030 entries that were formerly in the tables. • The 1.1.4. Wide Range I/O Support is new. • The I/Os per Package table was updated to add the following information to table note 4: "For nano devices, the VQ100 package is offered in both leaded and RoHS-compliant versions. All other packages are RoHS-compliant only." • The "ProASIC 3 nano Products Available in the Z Feature Grade" section was updated to remove QN100 for A3PN250. • The 1.1. General Description was updated to give correct information about number of gates and dual-port RAM for ProASIC 3 nano devices. • The device architecture figures, Figure 1-3 through Figure 1-4, were revised. Figure 1-1 is new. • The 1.1.3. PLL and CCC was revised to include information about CCC-GLs in A3PN020 and smaller devices. • Table 2-2 was revised to add VMV to the VCCI row. The following table note was added: "VMV pins must be connected to the corresponding VCCI pins." • The values in Table 2-7 were revised for A3PN010, A3PN015, and A3PN020. • A table note, "All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range, as specified in the JESD8-B specification," was added to Table 2-14, Table 2-18, and Table 2-19. • 3.3V LVCMOS Wide Range was added to Table 2-21 and Table 2-23. • The Figure 4-1 pin diagram was revised. • Note 2 for the Figure 4-1, Figure 4-2, and Figure 4-3 pin diagrams was added/changed to "The die attach paddle of the package is tied to ground (GND)." • The Figure 4-3 pin diagram was revised to move the pin IDs to the upper left corner instead of the upper right corner.

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