

SY898530U

500 MHz, 1:16, 3.3V-to-2.5V/3.3V LVPECL Fanout Buffer

Features

- 16 Differential 2.5V/3.3V LVPECL Outputs
- Differential CLK Inputs. Accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL Logic Levels
- Translates Any Single-Ended Input Signal to 2.5V/3.3V LVPECL Levels with a Resistor Bias on /CLK Input
- 500 MHz Maximum Output Frequency
- <50 ps Output Skew
- <250 ps Part-to-Part Skew
- <2 ns Propagation Delay
- · 3.3V Core, 2.5V/3.3V Output Operating Supply
- 0°C to +70°C Operating Temperature
- Available in a 48-Lead TQFP Package
- Pin-to-Pin Compatible with ICS8530

Applications

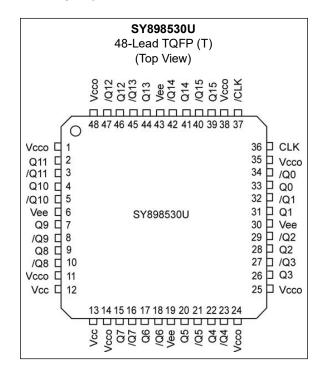
- · Data Distribution
- · High-Performance PCs
- · Communications
- · Parallel Processor-Based Systems

General Description

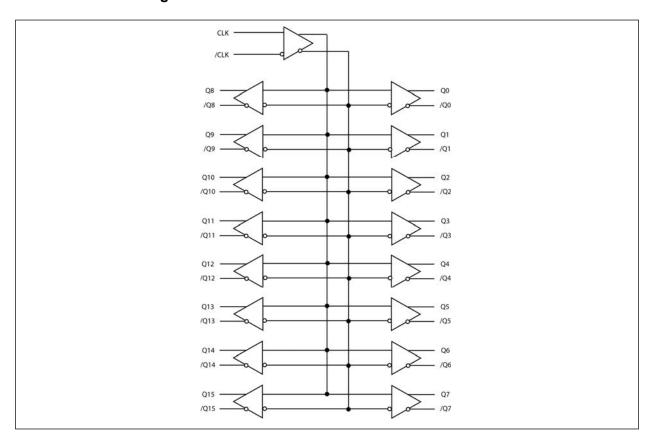
The SY898530U is a 1:16 fanout buffer that can accept most standard differential logic levels and outputs the signal as a differential 2.5V or 3.3V LVPECL signal. The part can amplify input signals as small as 150 mV_{PP} to the full LVPECL output swing. The SY898530U is well suited for clock distribution applications which demand versatility and low-skew performance. It is pin-to-pin compatible with IDT's ICS8530 fanout buffer.

The SY898530U operates from a $3.3V \pm 5\%$ core power supply and a $2.5V \pm 5\%$ or a $3.3V \pm 5\%$ output supply. The SY898530U is ensured over the full commercial temperature range (0°C to +70°C). It is available in a 48-lead TQFP lead-free package.

Package Type



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V _{CC})	+4.6V
Input Voltage (V _{IN})	
LVPECL Continuous Output Current (I _{OUT})	50 mA
LVPECL Surge Output Current (I _{OUT})	100 mA

Operating Ratings ‡

Supply Voltage (V _{CC})	+3.135V to +3.465V
Output Supply Voltage (Vcco)	+2.375V to +3.465V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

DC ELECTRICAL CHARACTERISTICS

 V_{CC} = 3.135V to 3.465V, V_{CCO} = 2.375V to 3.465V, T_A = 0°C to +70°C, unless otherwise stated. Note 1

_ 00							
Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions	
Power Supply Voltage Range	V _{CC}	3.135	3.3	3.465	V	_	
Output Power Supply	V _{cco}	2.375	_	3.465	V	_	
Power Supply Current	I _{EE}	_	_	125	mA	Maximum V _{CC} , V _{CCO}	
CLK Input High Current		_	_	150		V _{CC} = V _{IN} = 3.465V	
/CLK Input High Current	I _{IH}	_	_	5	μA	V _{CC} - V _{IN} - 3.465V	
CLK Input Low Current		- 5	_	_		V = 2.465V V = 0.5V	
/CLK Input Low Current	l IIL	-150	_	_	μA	$V_{CC} = 3.465V, V_{IN} = 0.5V$	
Peak-to-Peak Input Swing	V _{PP}	0.15	_	1.3	V	_	
Common Mode Input Voltage	V _{CMR}	0.5	_	V _{CC} – 0.85	V	Note 2, Note 3	

- **Note 1:** The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.
 - 2: For single-ended applications, the maximum input voltage for CLK, /CLK is V_{CC} + 0.3V.
 - 3: Common mode voltage is defined as V_{IH}.

PECL OUTPUTS DC ELECTRICAL CHARACTERISTICS

 V_{CC} = 3.135V to 3.465V, V_{CCO} = 2.375V to 3.465V, T_A = 0°C to +70°C, Outputs terminated with 50 Ω to V_{CCO} – 2V unless otherwise stated. Note 1

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions
Output High Voltage	V _{OH}	V _{CCO} – 1.1	_	V _{CCO} – 0.7	V	_
Output Low Voltage	V _{OL}	V _{CCO} – 2.0	_	V _{CCO} – 1.4	V	_
Output Voltage Swing	V _{OUT}	0.55	_	0.93	V	_

Note 1: The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS

 V_{CC} = 3.135V to 3.465V, V_{CCO} = 2.375V to 3.465V, T_A = 0°C to +70°C, unless otherwise stated.

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions
Maximum Frequency	f _{MAX}	500	_	_	MHz	_
Propagation Delay	t _{PD}	1	_	2	ns	Note 1
Output-to-Output Skew	+	_	26	50	ps	Note 2, Note 4
Part-to-Part Skew	^t SKEW	_	_	250	ps	Note 3, Note 4
RMS Phase Jitter	t _{JITTER}	_	127	_	fs _{RMS}	Output = 500 MHz, Integration Range: 12 kHz to 20 MHz
Output Rise/Fall Time	t _r , t _f	300	_	700	ps	At full output swing
Duty Cycle	DC	47	50	53	%	_

- Note 1: Measured from the differential input crossing point to the differential output crossing point.
 - 2: Output-to-Output skew is the difference in time between outputs, receiving data from the same input, for the same temperature, voltage, and transition.
 - **3:** Part-to-Part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
 - 4: This parameter is defined in accordance with JEDEC Standard 65.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Тур.	Max.	Units	Conditions		
Temperature Ranges			- 71					
Storage Temperature Range	T _S	-65	_	+150	°C	_		
Lead Temperature	T _{LEAD}	_	_	+260	°C	Soldering, 20 sec.		
Ambient Temperature Range	T _A	0	_	+70	°C	_		
Package Thermal Resistances								
Thermal Resistance, TQFP 48-Ld	θ_{JA}	_	48	_	°C/W	Still-Air		
(Note 1)	θ_{JC}	_	13	_	°C/W	Junction-to-Case		

Note 1: θ_{JA} and θ_{JC} values are determined for a 4-layer board in still-air.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

 V_{CC} = 3.3V, V_{CCO} = 2.5V or 3.3V, T_A = +25°C, Input Signal = 800 mV.

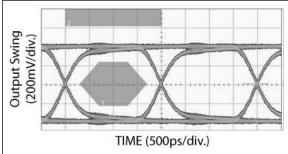


FIGURE 2-1: 500 Mbps PRBS-23 Signal.

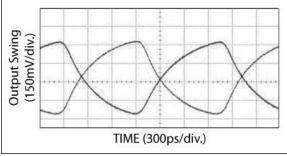


FIGURE 2-2: 500 MHz Clock Signal.

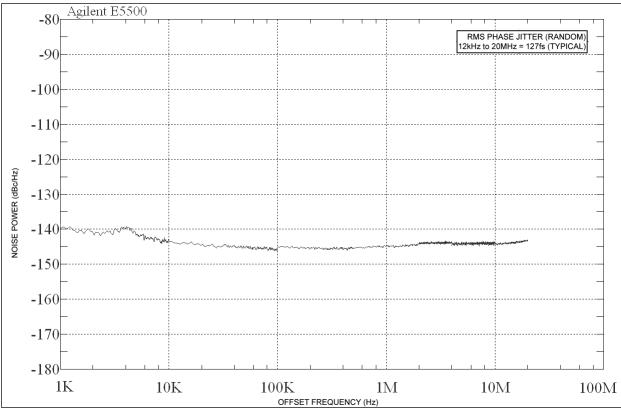


FIGURE 2-3: Phase Noise Graph.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Dia Name	Din Name	Dog and of the co
Pin Number	Pin Name	Description
36, 37	CLK, /CLK	Differential Clock Inputs. Accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL logic levels. CLK is internally connected to a pull-down resistor, /CLK is internally connected to a pull-up resistor. See Table 3-2 for typical values.
33, 34	Q0, /Q0	
31, 32	Q1, /Q1	
28, 29	Q2, /Q2	
26, 27	Q3, /Q3	
22, 23	Q4, /Q4	
20, 21	Q5, /Q5	
17, 18	Q6, /Q6	LVPECL Differential Output Pairs. Differential buffered copies of the input signal.
15, 16	Q7, /Q7	The output swing is typically 740 mV. See the Interface Applications section for
9, 10	Q8, /Q8	termination information.
7, 8	Q9, /Q9	termination information.
4, 5	Q10, /Q10	
2, 3	Q11, /Q11	
46, 47	Q12, /Q12	
44, 45	Q13, /Q13	
41, 42	Q14, /Q14	
39, 40	Q15, /Q15	
1, 11, 14, 24, 25, 35, 38, 48	VCCO	Output Power Supply: Bypass with 0.1 μ F//0.01 μ F low-ESR capacitors as close to the VCCO pins as possible. Supplies the output buffers.
12, 13	VCC	Core Power Supply: Bypass with 0.1 μ F//0.01 μ F low-ESR capacitors as close to the VCC pins as possible. Supplies input and core circuitry.
6, 19, 30, 43	VEE	Ground.

TABLE 3-2: PIN CHARACTERISTICS

Symbol	Description	Typical Value
C _{IN}	Input Capacitance	4 pF
R _{PULLUP}	Input Pull-Up Resistor	50 kΩ
R _{PULLDOWN}	Input Pull-Down Resistor	30 kΩ

TABLE 3-3: CLOCK INPUT FUNCTION

Inp	uts	Out	puts	Innut to Output Made	Dolority
CLK	/CLK	Qx	/Qx	Input to Output Mode	Polarity
0	1	Low	High	Differential to Differential	Non-Inverting
1	0	High	Low	Differential to Differential	Non-Inverting
0	Biased ⁽¹⁾	Low	High	Single-Ended to Differential	Non-Inverting
1	Biased ⁽¹⁾	High	Low	Single-Ended to Differential	Non-Inverting
Biased ⁽¹⁾	0	High	Low	Single-Ended to Differential	Inverting
Biased ⁽¹⁾	1	Low	High	Single-Ended to Differential	Inverting

Note 1: Refer to the Interface Applications section for Single-Ended interfaces.

4.0 TEST CIRCUITS

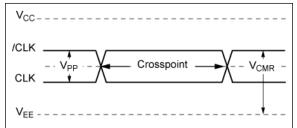


FIGURE 4-1: Differential Input Level.

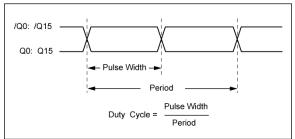


FIGURE 4-2: Output Duty Cycle.

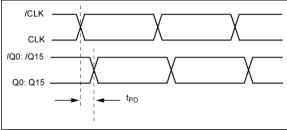


FIGURE 4-3: Propagation Delay.



FIGURE 4-4: Output Rise/Fall Times.

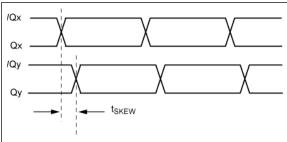


FIGURE 4-5: Output-to-Output Skew.

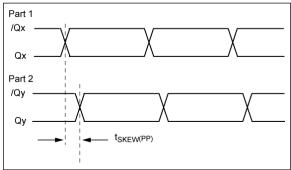


FIGURE 4-6: Part-to-Part Skew.

5.0 JUNCTION TEMPERATURE

The maximum recommended junction temperature is T_J = +125°C. The outputs are terminated with 50 Ω to V_{CCO} – 2V. Below is a calculation of the worst case scenario with zero airflow:

5.1 Terms

- T_J = Junction temperature.
- T_A = Ambient temperature.
- θ_{JA} = Junction-to-Ambient thermal resistance.
- P_D = Power dissipation.

5.2 Calculations

PD =
$$P_{D_CORE} + P_{D_OUTPUTS}$$
 $P_{D_CORE} = V_{CC(MAX)} \times I_{EE(MAX)}$
 $P_{D_CORE} = 3.465V \times 125 \text{ mA} = 433 \text{ mW}$
 $P_{D_OUTPUT} = P_{D_H} + P_{D_L}$
 $P_{D_H} = [(V_{OH} - (V_{CCO} - 2V))/R_L] \times (V_{CCO} - V_{OH(MAX)})$
 $P_{D_H} = 18.2 \text{ mW}$
 $P_{D_L} = [(V_{OL} - (V_{CCO} - 2V))/R_L] \times (V_{CCO} - V_{OL(MAX)})$
 $P_{D_L} = [(2V - 1.4V)/50\Omega] \times 1.4V$
 $P_{D_L} = 16.8 \text{ mW}$
 $P_{D_OUTPUT} = 35 \text{ mW}$
 $P_{D_OUTPUTS} = 16 \times 35 \text{ mW}$
 $P_{D_OUTPUTS} = 560 \text{ mW}$
 $P_{D_OUTPUTS} = 560 \text{ mW}$
 $P_{D} = 433 \text{ mW} + 560 \text{ mW}$
 $P_{D} = 0.993 \text{ W}$
 $T_{J} = T_{A} + \theta_{JA} \times P_{D}$
 $T_{J_WORST_CASE} = 70^{\circ}\text{C} + 0.993W \times 48^{\circ}\text{C/W}$
 $T_{J_WORST_CASE} = 118^{\circ}\text{C} \text{ in still air.}$

The worst case junction temperature is below 125°C.

6.0 INPUT INTERFACE APPLICATIONS

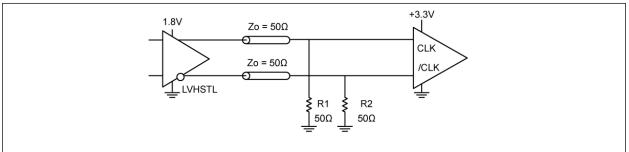


FIGURE 6-1: CLK and /CLK Input Driven by 1.8V LVHSTL.

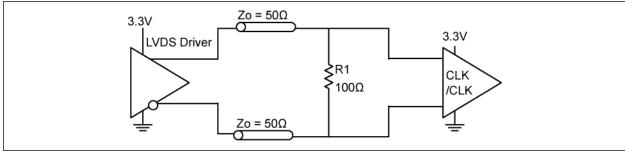


FIGURE 6-2: CLK and /CLK Input Driven by 3.3V LVDS.

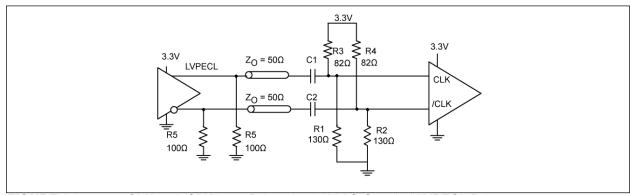


FIGURE 6-3: CLK and /CLK Input Driven by 3.3V AC-Coupled LVPECL Driver.

Note: For +2.5V systems: R5 = 50Ω , R1 & R2 = 220Ω , R3 & R4 = 68Ω .

7.0 OUTPUT INTERFACE APPLICATIONS

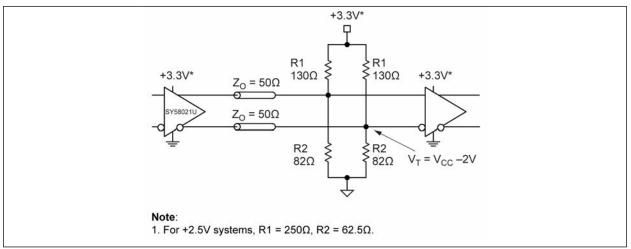


FIGURE 7-1: Parallel Termination: Thevenin Equivalent.

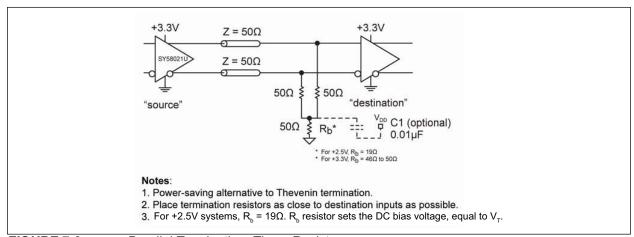


FIGURE 7-2: Parallel Termination: Three-Resistor.

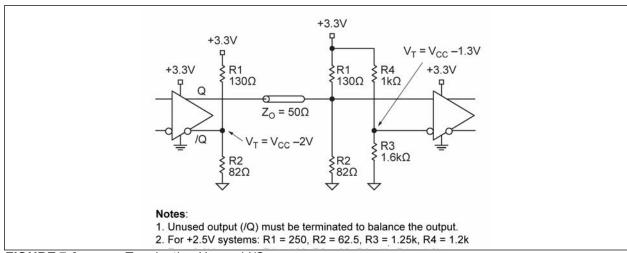


FIGURE 7-3: Terminating Unused I/O.

8.0 PACKAGING INFORMATION

8.1 Package Marking Information

48-Lead TQFP*



Example



Legend: XX...X Product code or customer-specific information

Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')

NNN Alphanumeric traceability code

Pb-free JEDEC® designator for Matte Tin (Sn)

* This package is Pb-free. The Pb-free JEDEC designator (@3)

can be found on the outer packaging for this package.

Pin one index is identified by a dot, delta up, or delta down (triangle)

•, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

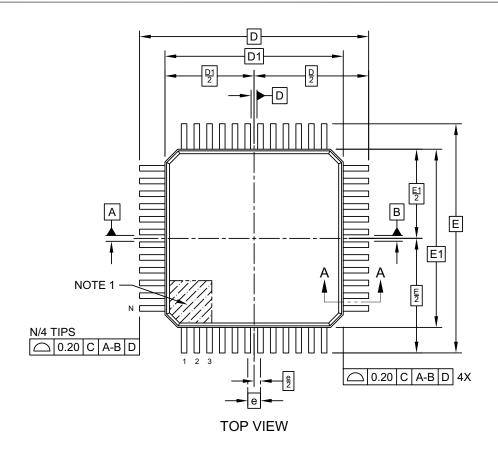
Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:

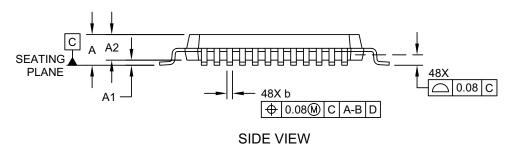
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;

2 Characters = NN; 1 Character = N

48-Lead Plastic Thin Quad Flatpack (CQA) - 7x7x1.0 mm Body [TQFP] Micrel Legacy Package TQFP7x7-48L

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

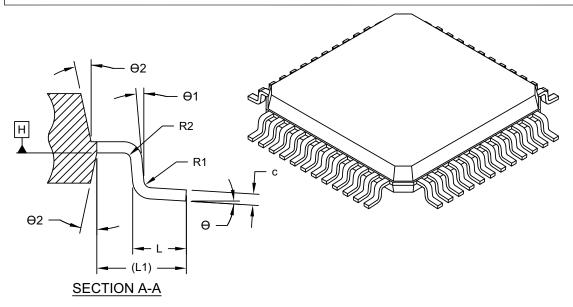




Microchip Technology Drawing C04-1175 Rev A Sheet 1 of 2

48-Lead Plastic Thin Quad Flatpack (CQA) - 7x7x1.0 mm Body [TQFP] Micrel Legacy Package TQFP7x7-48L

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS			
	Dimension Limits	MIN	NOM	MAX	
Number of Terminals	N		48		
Pitch	е		0.50 BSC		
Overall Height	Α	-	-	1.20	
Standoff	A1	0.05	-	0.15	
Molded Package Thickness	A2	0.95	1.00	1.05	
Overall Length	D		9.00 BSC		
Molded Package Length	D1	7.00 BSC			
Overall Width	E	9.00 BSC			
Molded Package Width	E1		7.00 BSC		
Terminal Width	b	0.17	0.22	0.27	
Terminal Thickness	С	0.12	-	0.21	
Terminal Length	L	0.45	0.60	0.75	
Footprint	L1		1.00 REF		
Lead Bend Radius	R1	0.08	-	-	
Lead Bend Radius	R2	0.08	-	0.20	
Foot Angle	θ	0°	3.5°	7°	
Lead Angle	θ1	0°	-	-	
Terminal-to-Exposed-Pad	Θ2	11°	12°	13°	

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
 Dimensioning and tolerancing per ASME Y14.5M

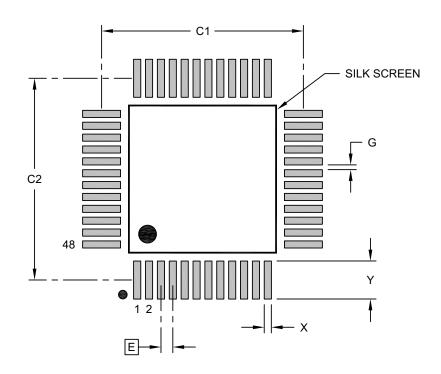
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1175 Rev A Sheet 2 of 2

48-Lead Plastic Thin Quad Flat Pack (CQA) - 7x7x1.0 mm Body [TQFP] Micrel Legacy Package Code TQFP7x7-48LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	Е		0.50 BSC	
Contact Pad Spacing	C1		8.50	
Contact Pad Spacing	C2		8.50	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.60
Contact Pad to Contact Pad (X44)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3175 Rev A

APPENDIX A: REVISION HISTORY

Revision A (September 2023)

- Converted Micrel document SY898530U to Microchip data sheet template DS20006818A.
- · Minor text changes throughout.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part No.	<u>X</u>	<u>x</u>		<u>X</u>	[- <u>XX</u>]	Exampl	es:
Device	Supply Voltage	Packa	age	Temperature Range	Media Type	a) SY89	98530UTZ:
	voltage			range			SY898530, 2.5V/3 Lead TQFP, 0°C to
Device:	SY898530:		Hz, 1:16 It Buffer	S, 3.3V-to-2.5V/3.	3V LVPECL	b) SY89	Range, 250/Tray 98530UTZ-TR:
Supply Voltage:	U	=	2.5V/3.	3V			SY898530, 2.5V/3 Lead TQFP, 0°C to Range, 1,000/Ree
Package:	Т	=	48-Lea	d TQFP		Note 1:	Tape and Reel identificatelog part number
Temperature Range:	Z	=	0°C to	+70°C			used for ordering pur the device package. Sales Office for pack and Reel option.
Media Type:	<blank> TR</blank>	= =	250/Tra 1,000/F				

/3.3V Supply Voltage, 48-to +70°C Temperature

/3.3V Supply Voltage, 48to +70°C Temperature

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