DC – 26 GHz GaAs Distributed LNA

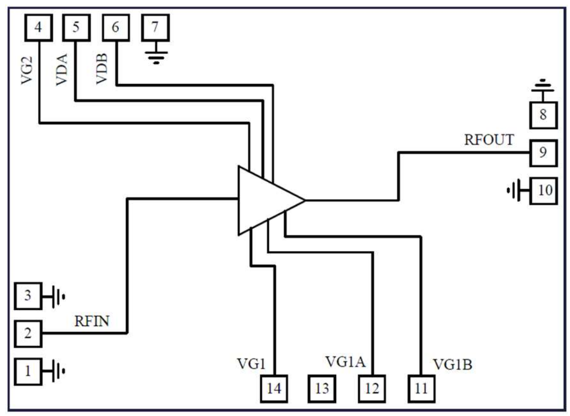
Product Overview

MMA041AA is a Gallium Arsenide (GaAs) monolithic microwave integrated circuit (MMIC) Pseudomorphic High Electron Mobility Transistor (PHEMT) distributed amplifier die that operates between DC and 26 GHz. It is ideal for test instrumentation, defense, aero-space and communications infrastructure applications. The amplifier provides a flat gain of 18.5 dB, 2 dB noise figure, 22 dBm of output power at 1 dB gain compression, and 36 dBm output IP3. The MMA041AA amplifier features RF I/O's that are internally matched to 50 Ohm, which allows for easy integration into multi-chip modules (MCMs).

Key Features

- **Frequency range: DC to 26 GHz**
- **High Gain: 18.5 dB**
- **Low Noise figure: 2 dB**
- **High Output IP3: + 36 dBm**
- **High Input Power: +22dBm**
- **Positive Supply: +7V @ 150 mA**
- **50 Ohm matched input/output**
- **Die size: 3.0 x 1.3 x 0.1 mm**

Functional Block Diagram



Applications

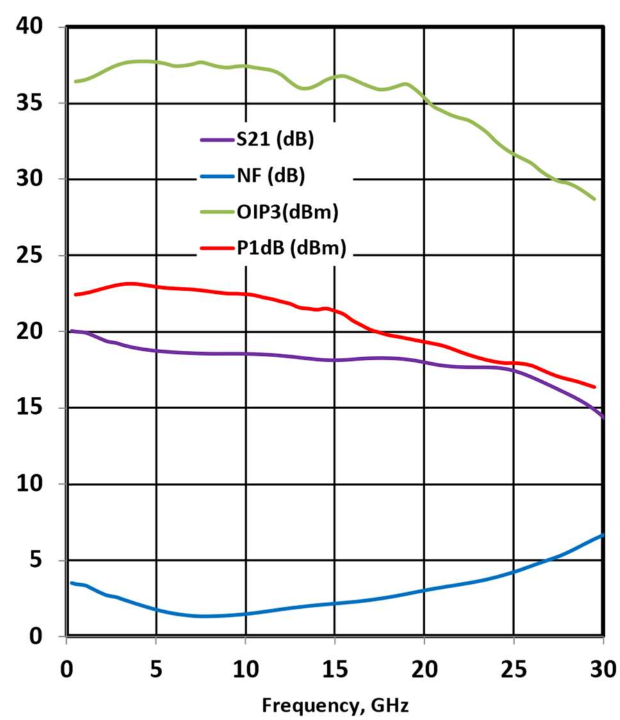
- Test and measurement instrumentation
- Electronic warfare (EW), electronic countermeasures (ECM), and electronic counter-countermeasures (ECCM)
- Military, A&D, space, SATCOM
- Telecom infrastructure
- Wideband microwave radios
- Microwave and millimeter-wave communications systems

Performance Overview

Parameter	Typ.	Units
Operational frequency range	DC-26	GHz
Gain	18.5	dB
OIP3	36	dBm
NF	2	dB
P1dB	22	dBm

Export Classification: EAR-99

Figure 1 - Typical Responses



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1. Electrical Specifications

1.1. Typical Electrical Performance

Table 1 - Typical Electrical Performance at 25 C, Vdd=7V, Idd=150 mA (Unless otherwise mentioned)

Parameter	Frequency Range	Min	Typ.	Max	Units
Frequency range		DC		26	GHz
Gain	DC - 6 GHz	18	20		dB
	6 - 12 GHz	17	18.5		
	12 - 20 GHz	17	18		
	20 – 26 GHz		16.5		
Gain flatness	4 - 12 GHz		± 0.5		dB
	12 - 20 GHz		± 0.25		
Noise figure	2 - 6 GHz		2.7	4	dB
	6 - 12 GHz		2	3	
	12 - 20 GHz		2.5	4	
	20 – 26 GHz		5		
Input return loss	DC - 6 GHz		17		dB
	6 - 12 GHz		20		
	12 - 20 GHz		20		
	20 – 26 GHz		10		
Output return loss	DC - 6 GHz		15		dB
	6 - 12 GHz		17		
	12 - 20 GHz		13		
	20 – 26 GHz		12		
P1dB	DC - 6 GHz	21.5	22.5		dBm
	6 - 12 GHz	20	22		
	12 - 20 GHz	18	20		
	20 – 26 GHz		16		
Psat (Measured at 3dB Gain Compression)	DC - 6 GHz		24		dBm
	6 - 12 GHz		24		
	12 - 20 GHz		22		
	20 – 26 GHz		18		
OIP3	DC - 6 GHz		36		dBm
	6 - 12 GHz		36		
	12 - 20 GHz		35		
	20 – 26 GHz		30		
Phase Noise			TBD		dBm/Hz
OIP2(low) (2-nd Order Intercept point F2-F1)			TBD		dBm
VDD (drain voltage supply)			7		V
IDD (drain current)			150		mA
VGG (Gate Voltage Bias)			-0.4		V

1.2. Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the MMA041AA device at 25 °C, unless otherwise specified. Exceeding one or any of the maximum ratings potentially could cause damage or latent defects to the device.

Table 2 - Absolute Maximum Ratings

Parameter	Rating
Drain bias voltage (V_{DD})	8 V
Gate bias voltage (V_G)	–2 V to 0.5 V
RF input power (Pin)	22 dBm
Channel temperature	150 °C
V_{DD} current (I_{DD})	300 mA
DC power dissipation (T = 85 °C)	2.4 W
Thermal resistance	18°C/W
Storage temperature	–65 °C to 150 °C
Operating temperature	–55 °C to 85 °C

ESD Sensitive Device

1.3. Typical Performance Curves

1.3.1 Typical Performances vs. Temperature

The following graphs show the typical performance curves of the MMA041AA device at specific bias conditions, measurements performed using application circuit shown on Figure 53 - below.

Figure 2 - Gain vs. Temperature @ 5V/100mA

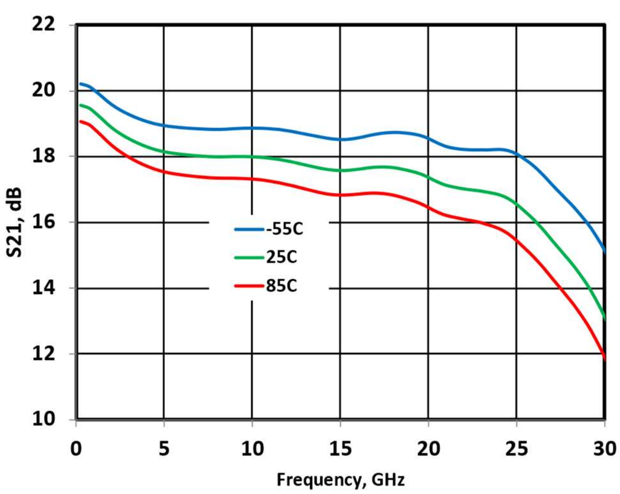


Figure 3 - Gain vs. Temperature @ 6V/150mA

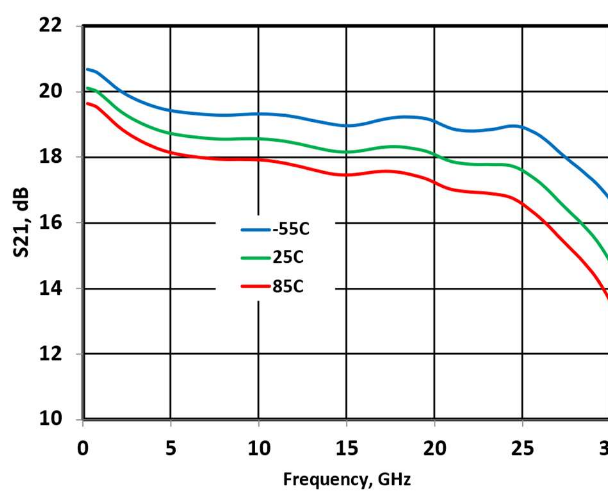


Figure 4 - Gain vs. Temperature @ 7V/180mA

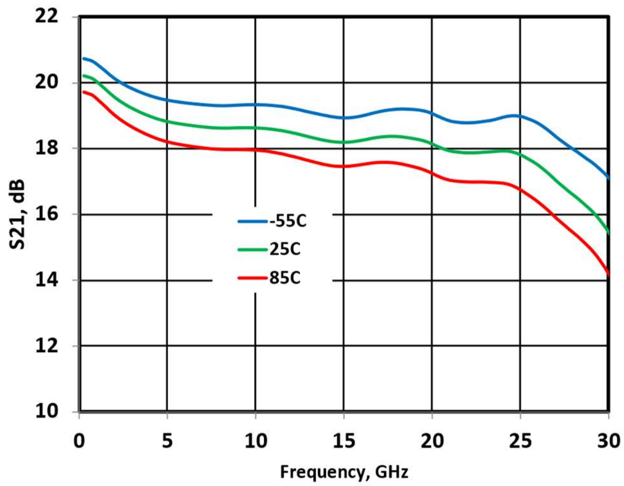


Figure 5 - S11 vs. Temperature @ 5V/100mA

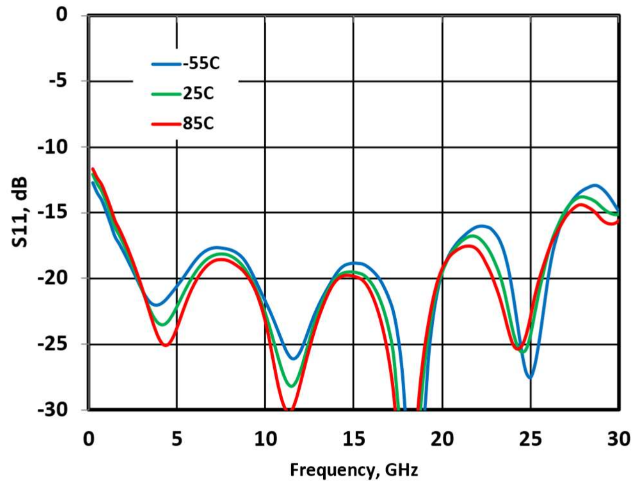


Figure 6 - S11 vs. Temperature @ 6V/150mA

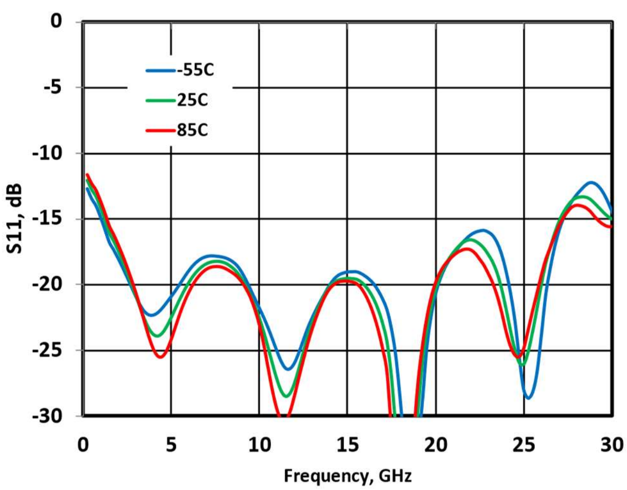


Figure 7 - S11 vs. Temperature @ 7V/180mA

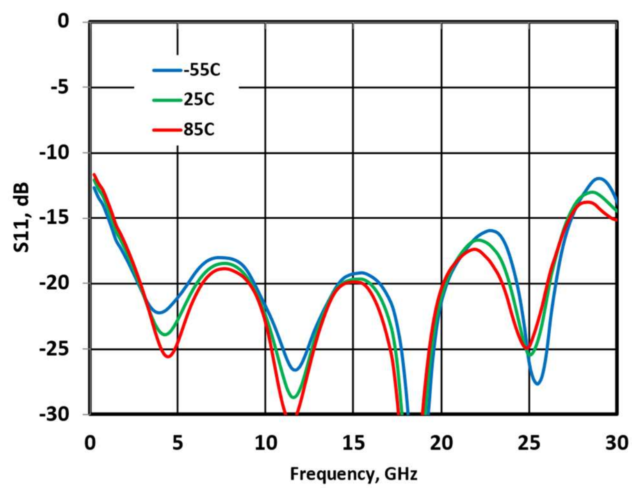


Figure 8 - S22 vs. Temperature @ 5V/100mA

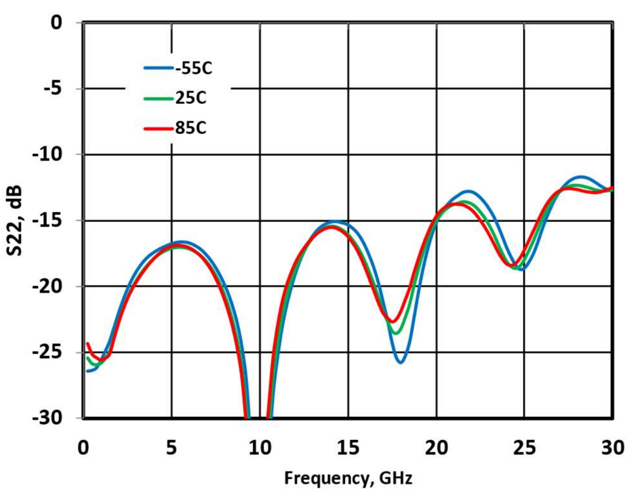


Figure 9 - S22 vs. Temperature @ 6V/150mA

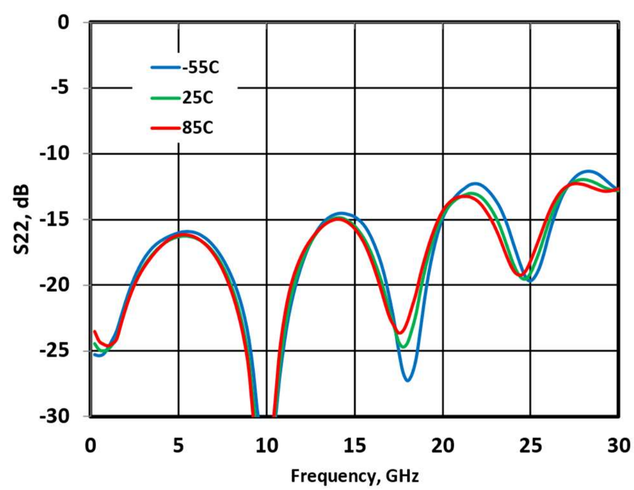


Figure 10 - S22 vs. Temperature @ 7V/180mA

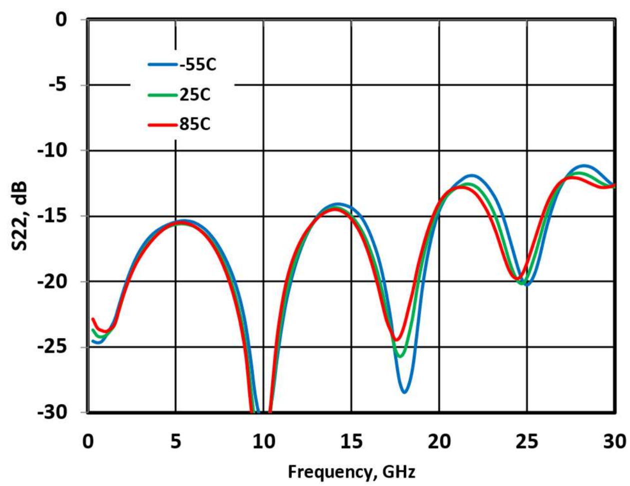


Figure 11 - S12 vs. Temperature @ 5V/100mA

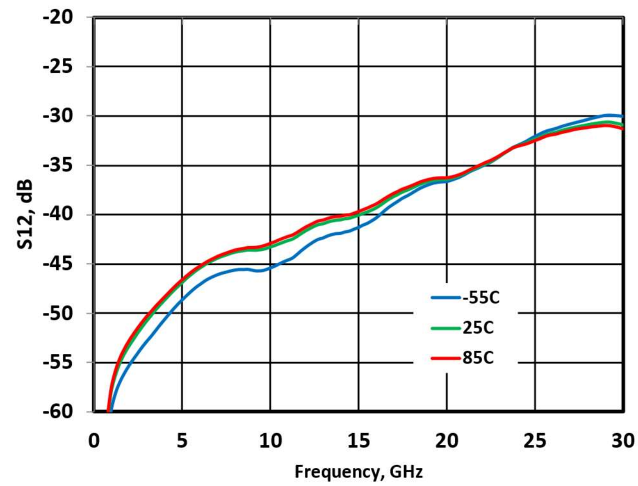


Figure 12 - S12 vs. Temperature @ 6V/150mA

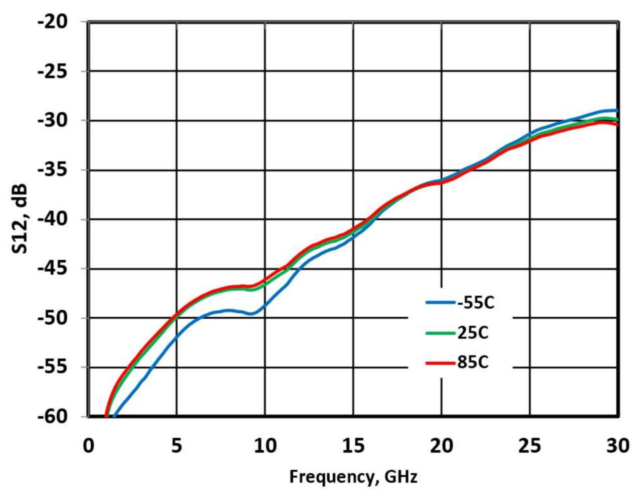


Figure 13 - S12 vs. Temperature @ 7V/180mA

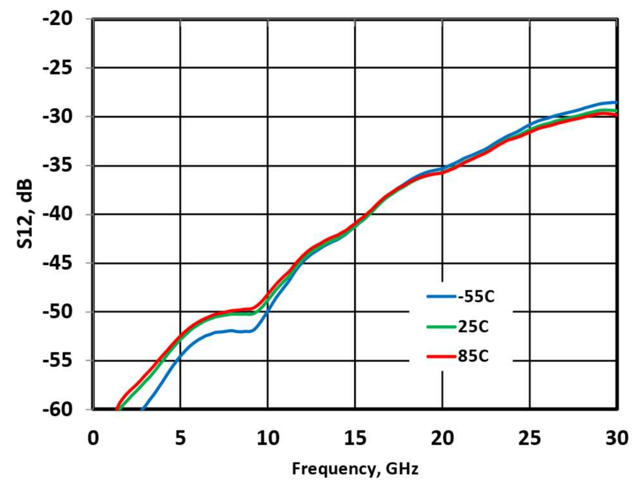


Figure 14 - NF vs. Temperature @ 5V/100mA

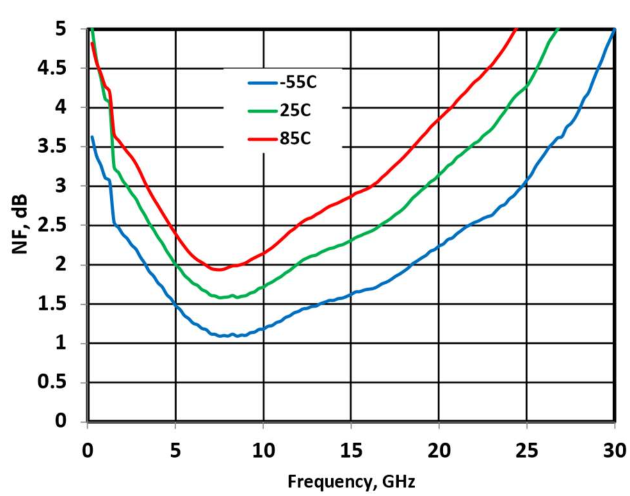


Figure 15 - NF vs. Temperature @ 6V/150mA

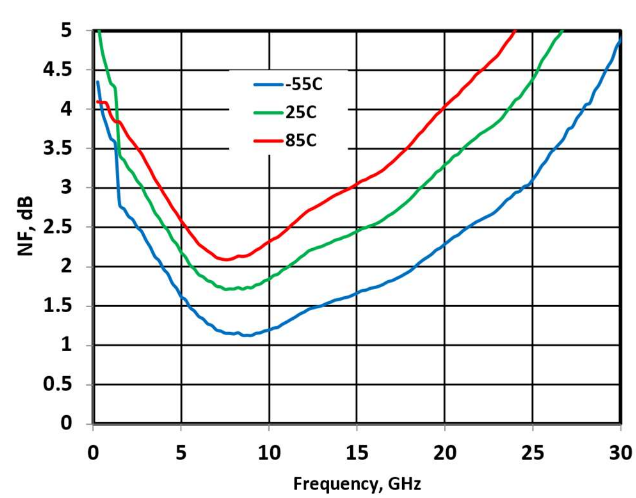


Figure 16 - NF vs. Temperature @ 7V/180mA

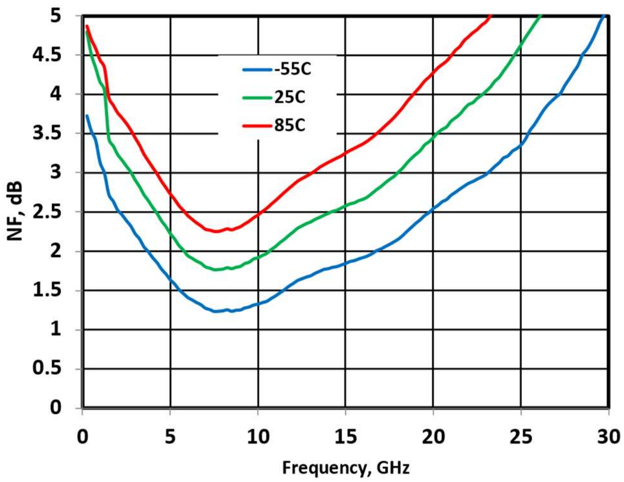


Figure 17 - P1dB vs. Temperature @ 5V/100mA

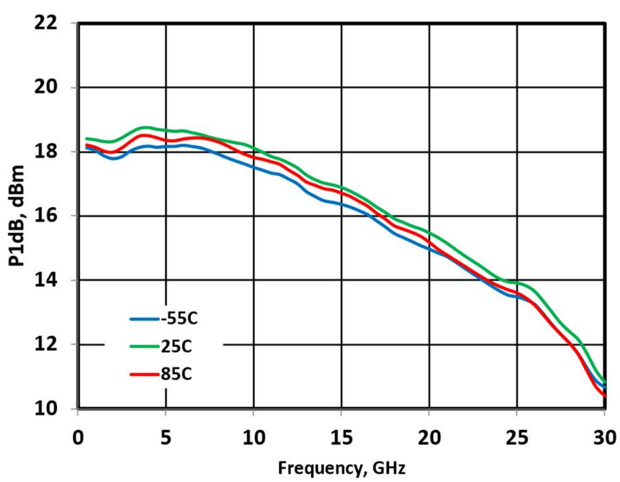


Figure 18 - P1dB vs. Temperature @ 6V/150mA

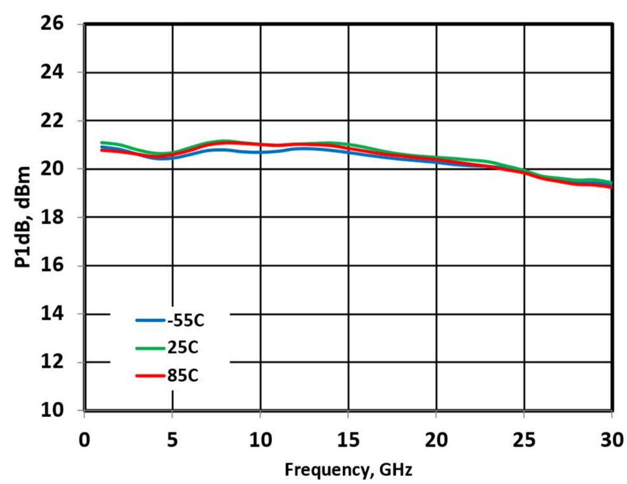


Figure 19 - P1dB vs. Temperature @ 7V/180mA

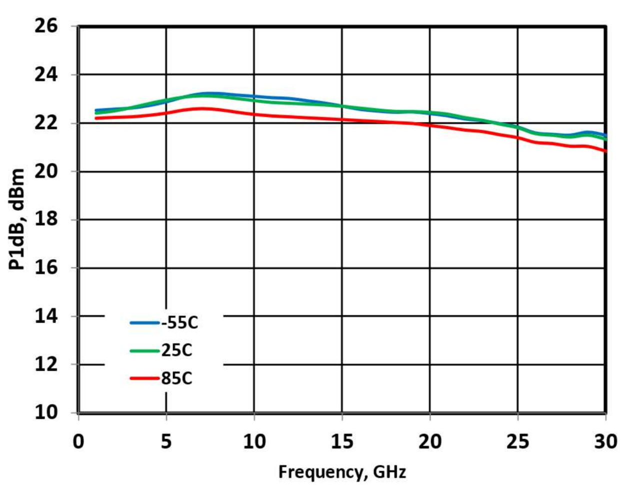


Figure 20 - Psat vs. Temperature @ 5V/100mA

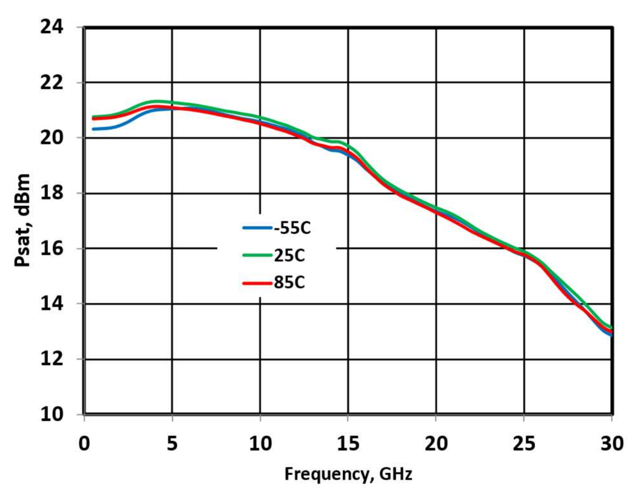


Figure 21 - Psat vs. Temperature @ 6V/150mA

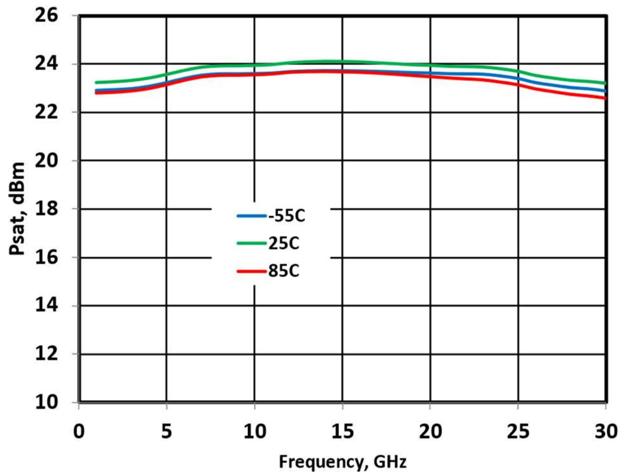


Figure 22 - Psat vs. Temperature @ 7V/180mA

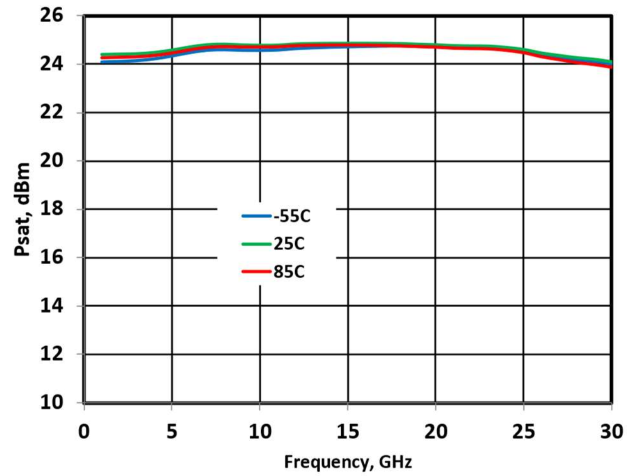


Figure 23 - OIP3 vs. Temperature @ 5V/100mA

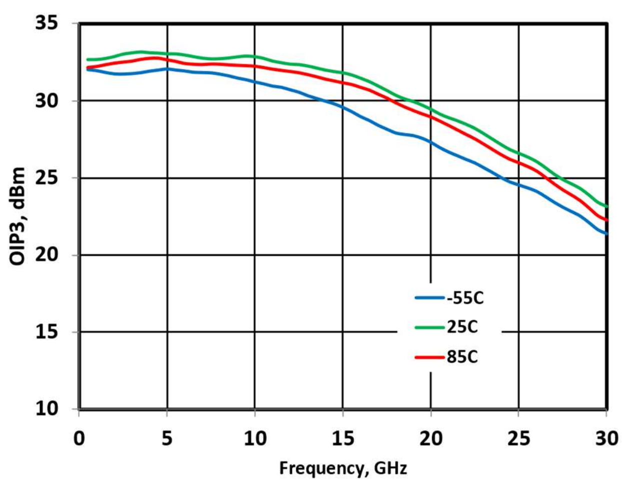


Figure 24 - OIP3 vs. Temperature @ 6V/150mA

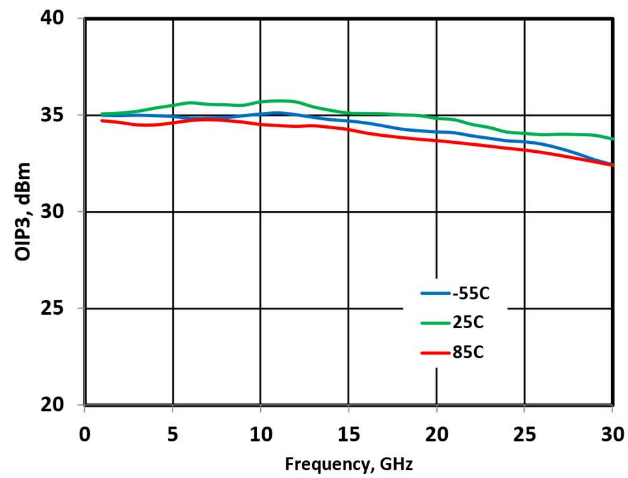


Figure 25 - OIP3 vs. Temperature @ 7V/180mA

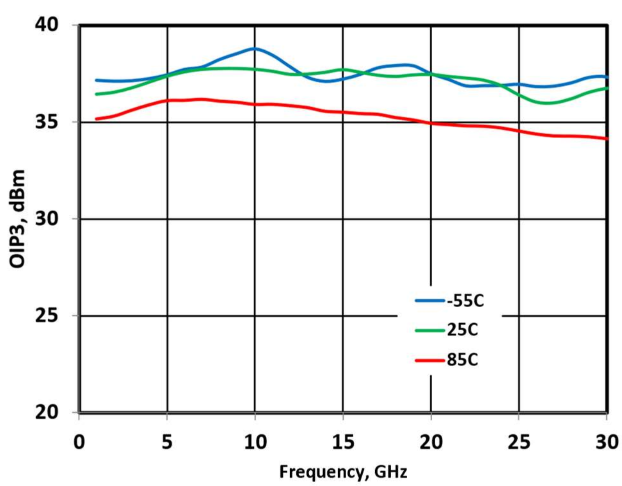


Figure 26 - OIP2(low) vs. Temperature @ 5V/100mA

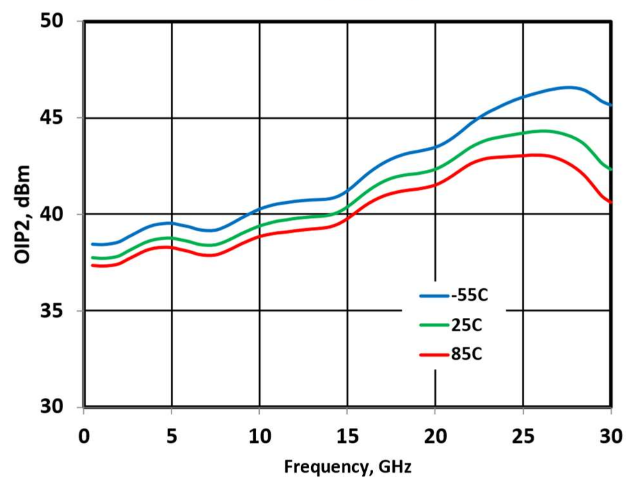


Figure 27 - OIP2(low) vs. Temperature @ 6V/150mA

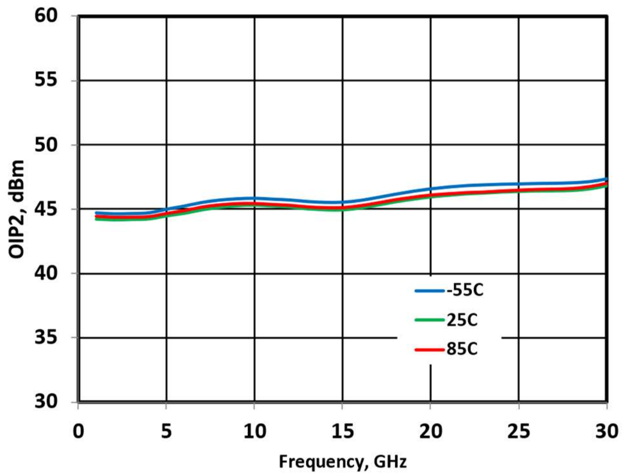


Figure 28 - OIP2(low) vs. Temperature @ 7V/180mA

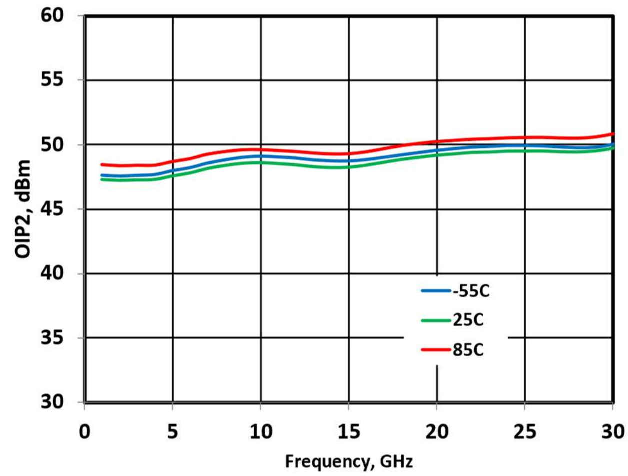


Figure 29 - IM3 vs. Temperature @ 5V/100mA, 10dBm(per tone)

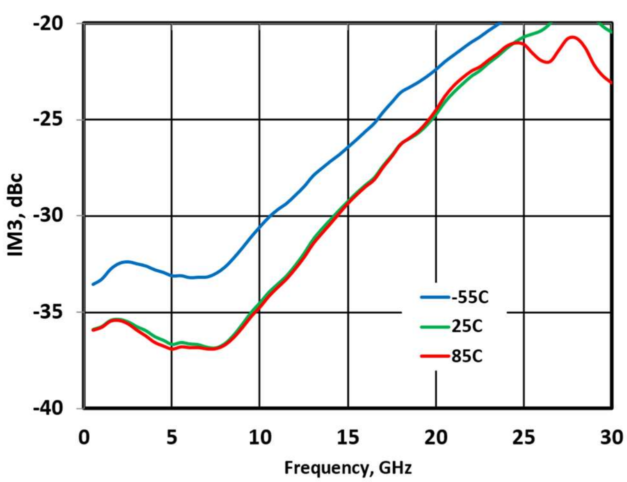


Figure 30 - IM3 vs. Temperature @ 6V/150mA, 10dBm(per tone)

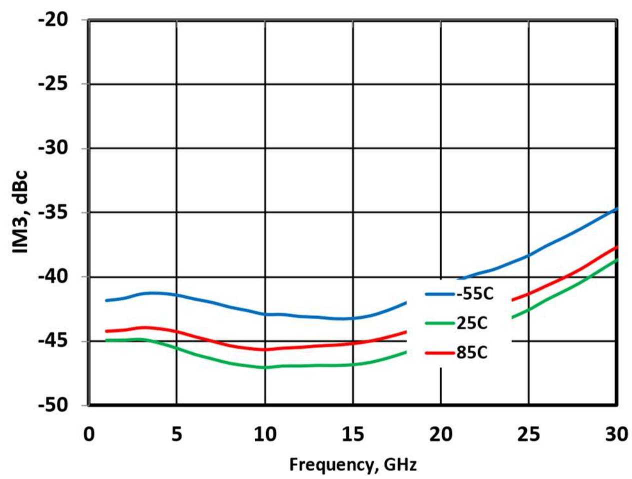
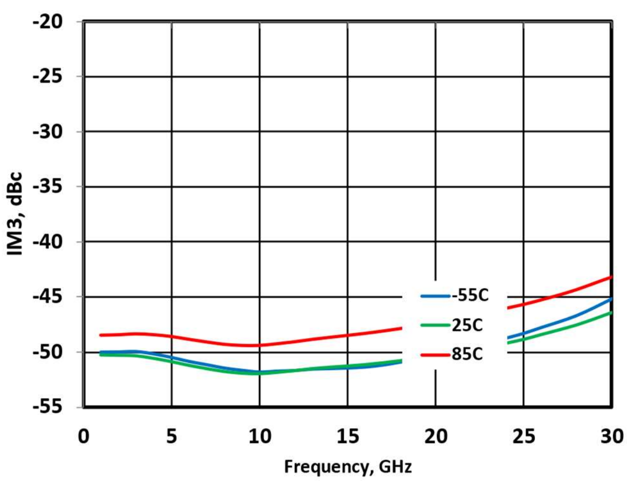


Figure 31 - IM3 vs. Temperature @ 7V/180mA, 10dBm(per tone)



1.3.2 Typical Performances vs. Bias

The following graphs show the typical performance curves of the MMA041AA device at 25 °C vs. Bias conditions, measurements performed using application circuit shown on Figure 53 - below.

Figure 32 - Gain vs. V_{DD} / I_{DD}

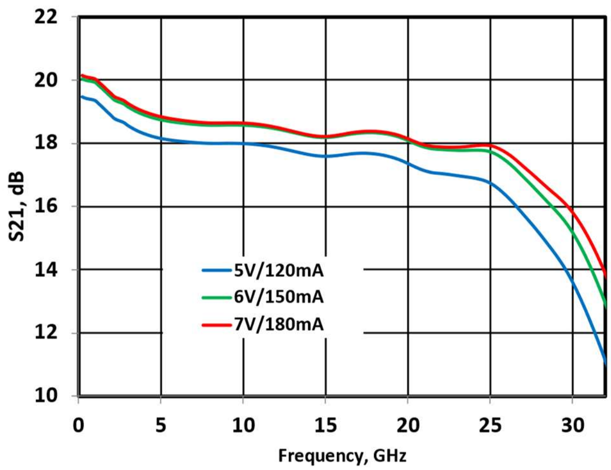


Figure 33 - NF vs. V_{DD} / I_{DD}

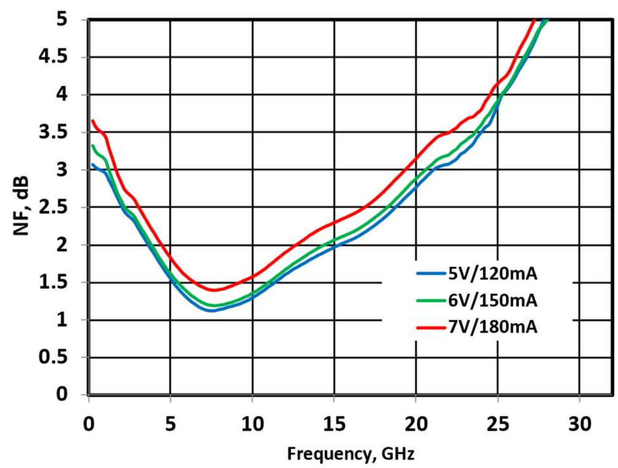


Figure 34 - S11 vs. V_{DD} / I_{DD}

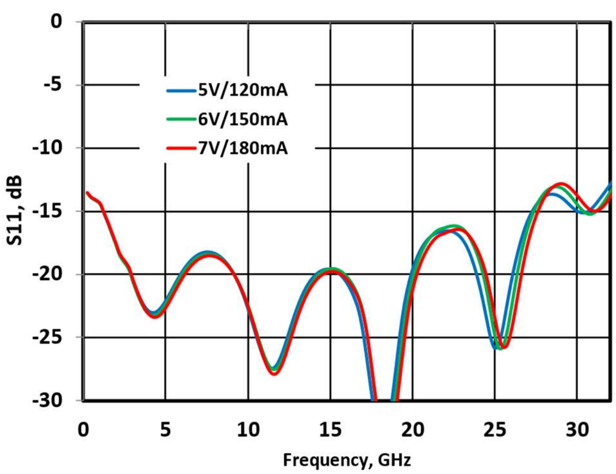


Figure 35 - S22 vs. V_{DD} / I_{DD}

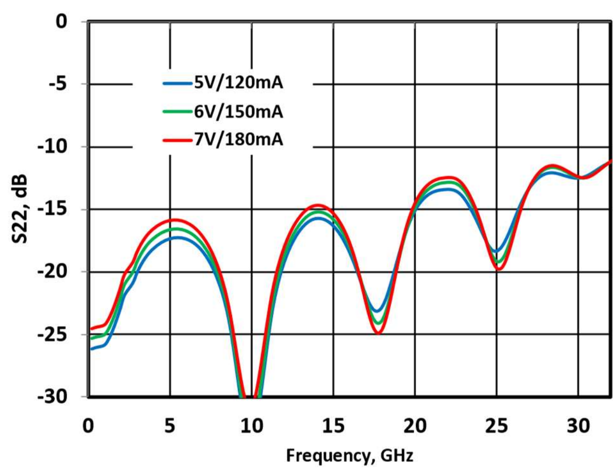


Figure 36 - S12 vs . V_{DD} / I_{DD}

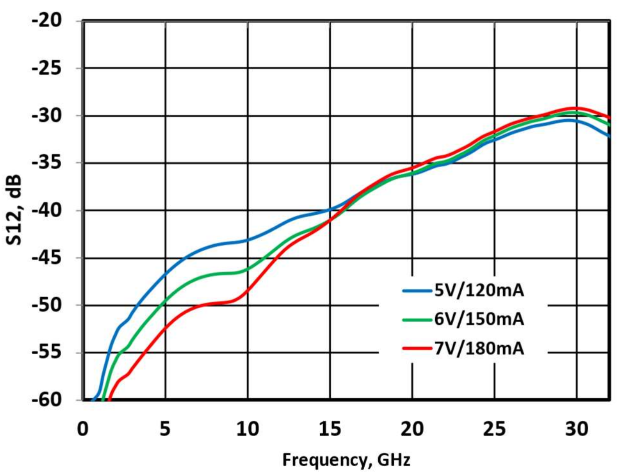


Figure 37 - P1dB vs. V_{DD}/I_{DD}

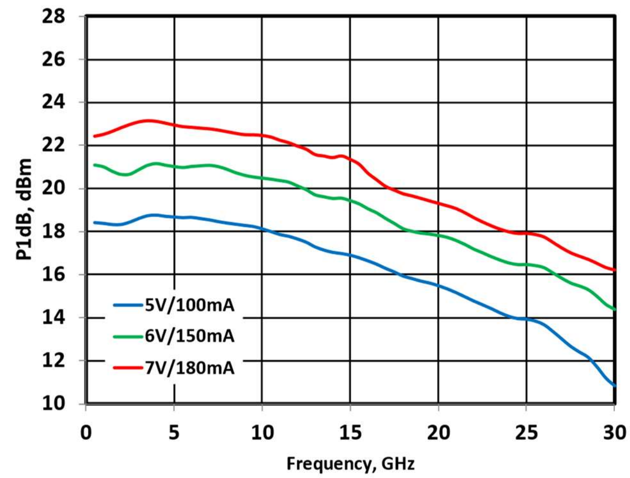


Figure 38 - Psat vs. V_{DD}/I_{DD}

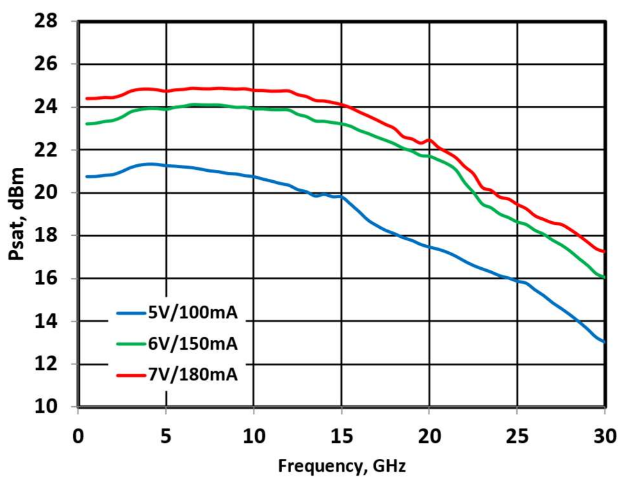


Figure 39 - OIP3 vs. V_{DD}/I_{DD}

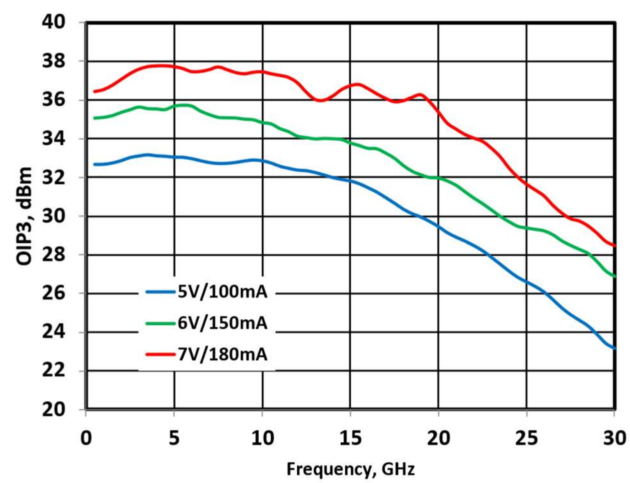


Figure 40 - OIP2 Low at Δ=10MHz vs. V_{DD}/I_{DD}

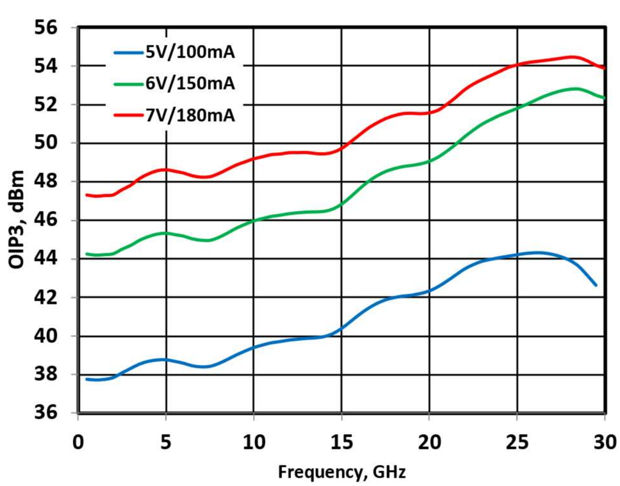
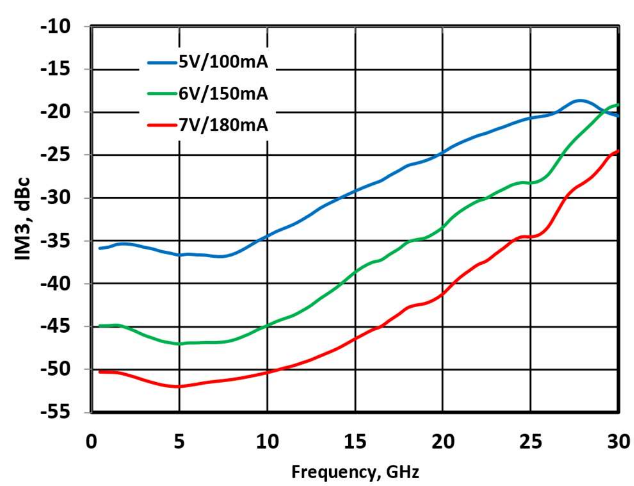


Figure 41 - IM3 vs. V_{DD}/I_{DD}, 10dBm(per tone)



1.3.3 Typical Performances vs. Output Power

The following graphs show the typical performance curves of the MMA041AA device at 25 °C vs. Output Power conditions, measurements performed using application circuit shown on Figure 53 - below.

Figure 42 - IM2 vs. Power @ 5V/100mA

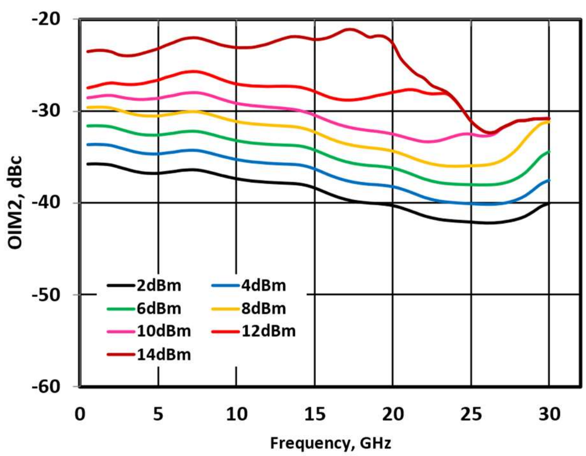


Figure 43 - IM2 vs. Power @ 6V/150mA

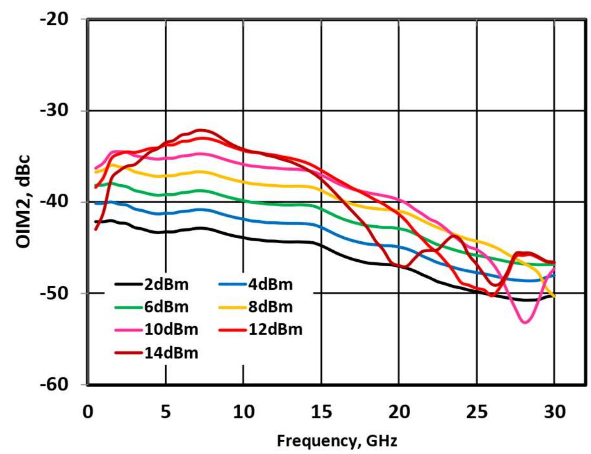


Figure 44 - IM2 vs. Power @ 7V/180mA

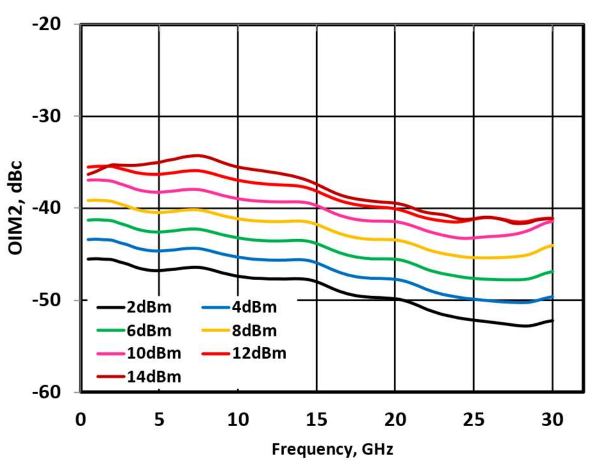


Figure 45 - IM3 vs. Power @ 5V/100mA

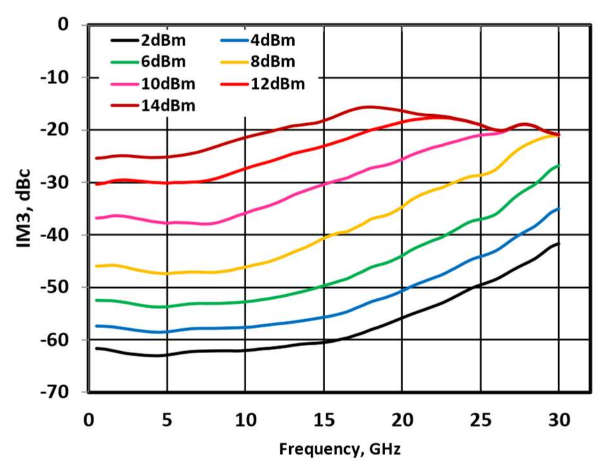


Figure 46 - IM3 vs. Power @ 6V/150mA

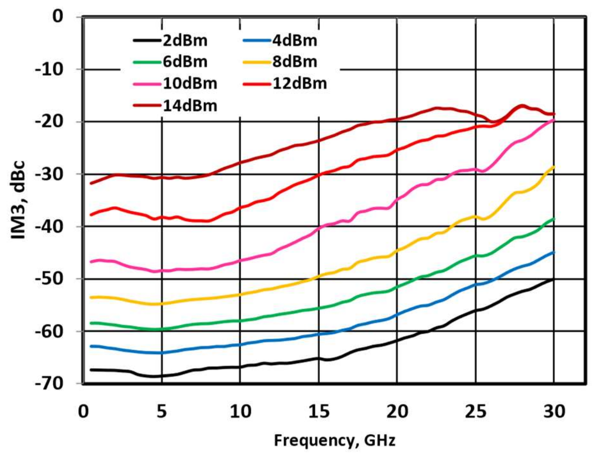


Figure 47 - IM3 vs. Power @ 7V/180mA

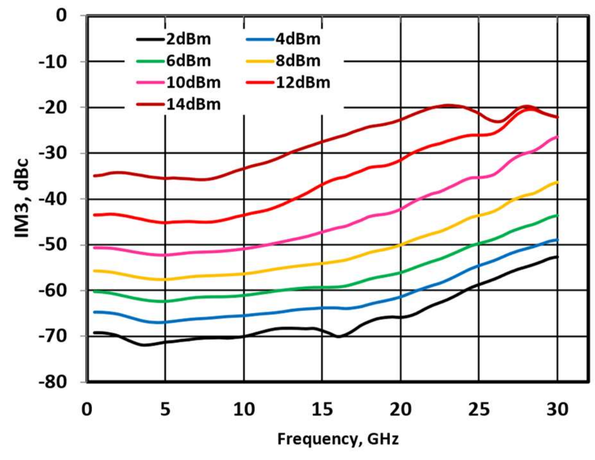


Figure 48 - 2-nd Harmonic vs. Power @ 5V/100mA

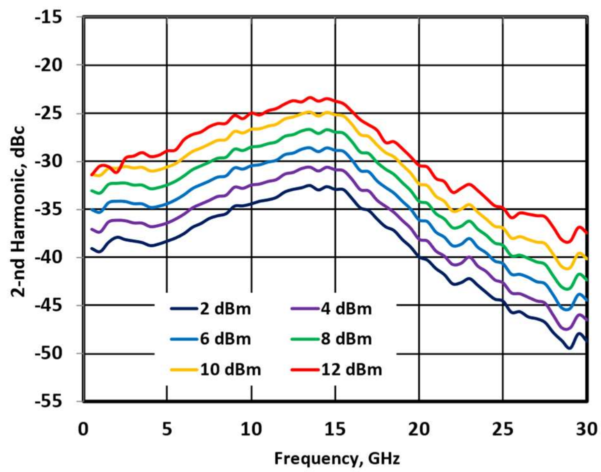


Figure 49 - 2-nd Harmonic vs. Power @ 6V/150mA

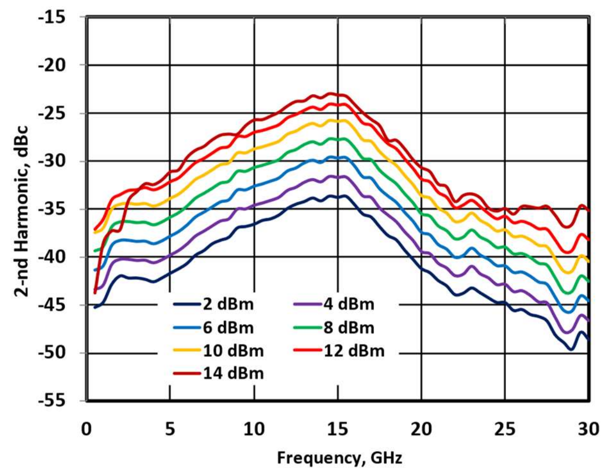
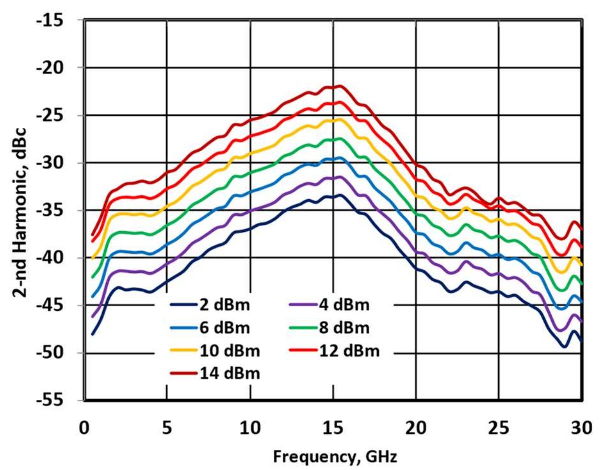


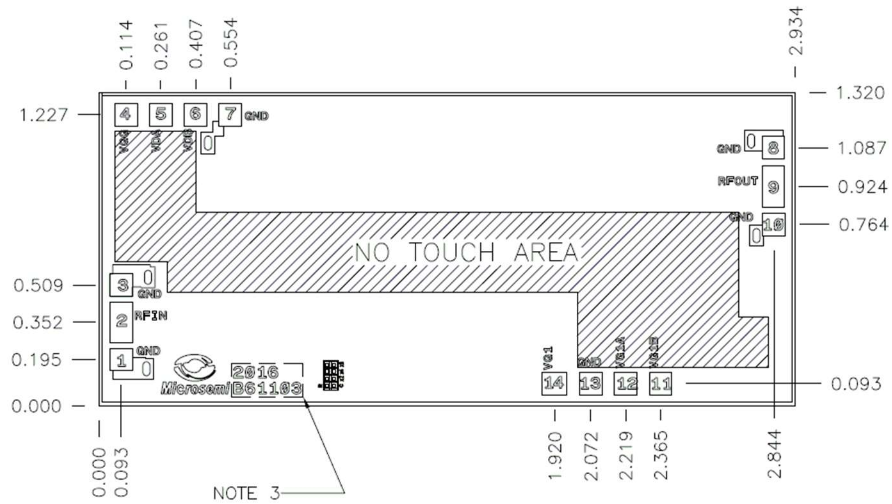
Figure 50 - 2-nd Harmonic vs. Power @ 7V/180mA



1.4. Die Specifications

The following illustration shows the chip outline of the MMA041AA device. Dimensions are in millimeters and are relative to the zero datum locations shown in the drawing. The minimum bond pad size is 0.1 mm × 0.1 mm. Both the bond pad surface and the backside metal have 3 µm thick gold. The die thickness is 0.1 mm. The backside is the DC/RF ground. The airbridge keep-out polygon region is shown inside.

PAD NO.	DESCRIPTION	PAD SIZE
1	GND	.100x.100
2	RFIN	.100x.180
3	GND	.100x.100
4	VGG	.100x.100
5	VDA	.100x.100
6	VDB	.100x.100
7	GND	.100x.100
8	GND	.100x.100
9	RFOUT	.100x.180
10	GND	.100x.100
11	VG1B	.100x.100
12	VG1A	.100x.100
13	GND	.100x.100
14	VG1	.100x.100



For additional packaging information, contact your Microchip sales representative.

Figure 51 - Die Outline Drawing (mm)

Table 3 - I/O Description

Pad Number	Pad Name	Pad Description
2	RFIN	DC-decoupled and matched to 50 Ohm.
9	RFOUT+VDD	DC-decoupled and matched to 50 Ohm; Used for VDD Bias
4	VG2	Second Gate Bias. Connect to VD1A (Optionally could be used for gain control by applying external bias in the range of VDD +/-30%)
5, 6	VD1A, VD1B	Low-frequency termination. Connect bypass capacitors per application circuit below. (Do NOT apply VDD bias to this connections)
11, 12	VG1A, VG1B	Low-frequency termination. Connect bypass capacitors per application circuit below.
14	VG1	Gate control for amplifier. Adjust to achieve IDD = 150 mA
1, 3, 7, 8, 10, 13	Ground	RF/DC Ground pads, not used in typical applications
Backside Paddle	RF/DC GND	Must be connected to RF/DC Ground

2. Application Circuits

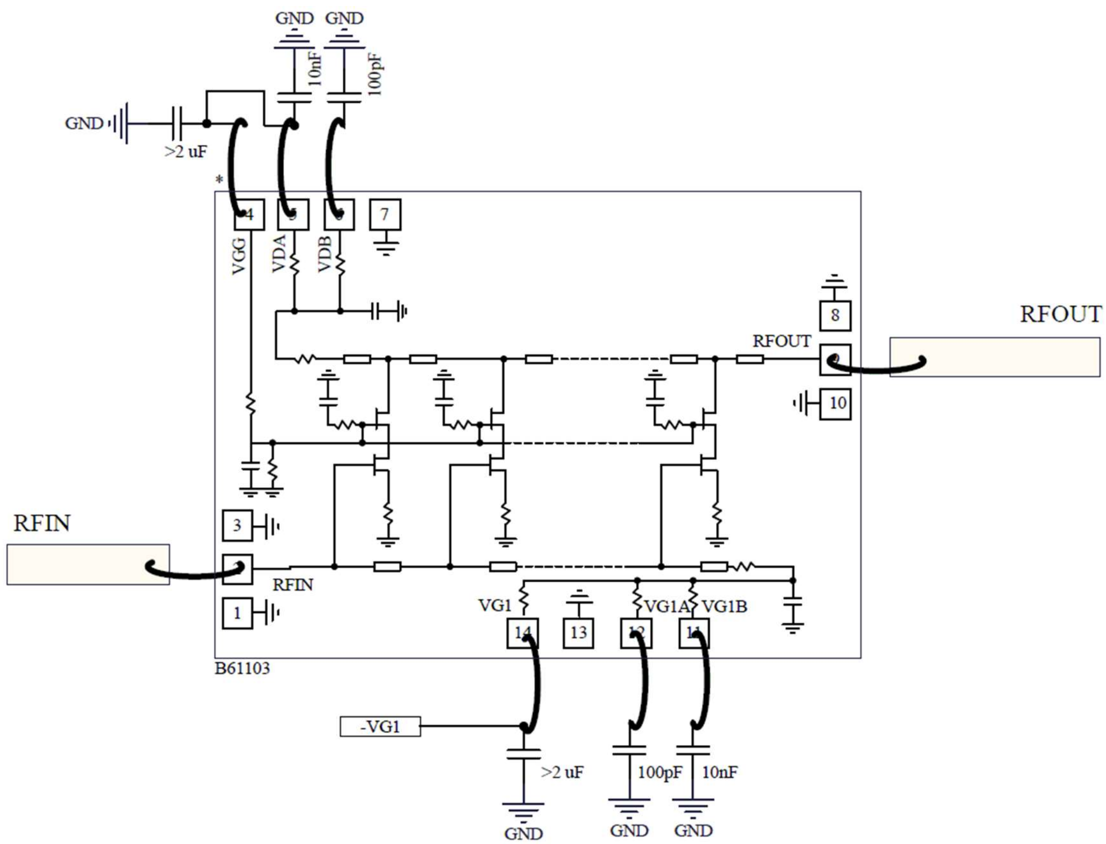


Figure 52 - Application Circuit: Schematic

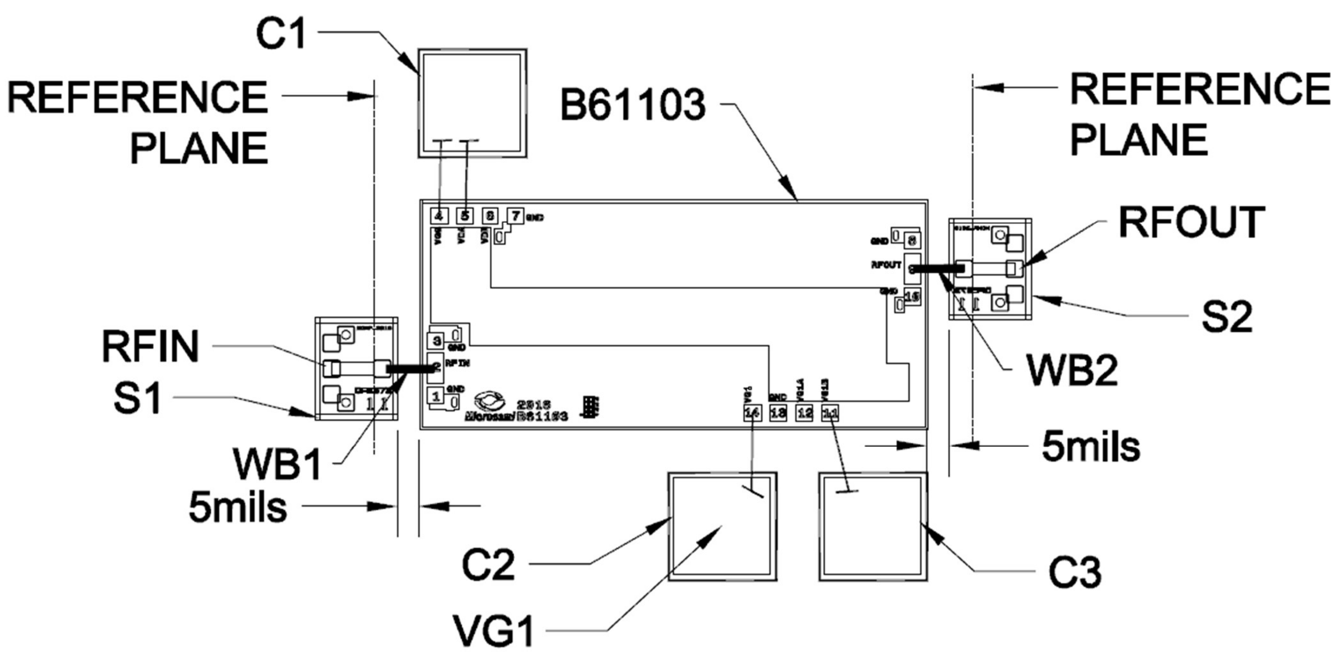


Figure 53 - Test Circuits DC-26 GHz: Assembly Drawing

Table 4 – List of Material for Figure 70: Assembly Drawing

Reference	Part Number	Description
B61103	MMA041AA	Amplifier Die
C1…C3	160U02A102MT4W	Johanson Dielectric SLC 1nF (Values could be different from the Application Circuit Schematic for ease of Test Circuit Assembly)
S1, S2	E57311	Microchip Probe Launchers, calibrated with TRL kit to Ref. Planes shown
WB1, WB2	744-903-06	Microchip 2mils Gold Ribbon, Should be as short as possible
RFIN/RFOUT		Location of the Input/Output GSG (150um) probes
VG1		Needle contact location for DC connection to VG1 (should be grounded if not used)

Table 4 – Bias Sequence

Bias Sequence
1) Set the gate voltage VG1 at -1V
2) Set Drain Voltage VDD at 7V (or as applications require)
3) Adjust the Gate Voltage by increments <0.01V until current reaches required value

3. Handling Recommendations

Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

4. Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package
MMA041AA	Die

4.1. Packing Information

Standard Format
Gel Pack
50 Pieces per Pack

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