ICP1543

12 – 18 GHz 20W GaN PA MMIC

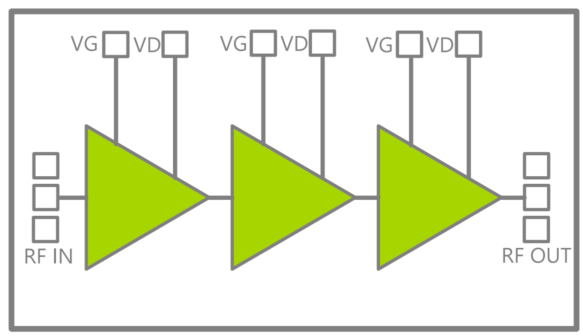
Product Overview

Microchip`s ICP1543 is a 3 stage MMIC power amplifier in bare die form, fabricated using GaN on SiC technology. ICP1543 operates from 12 – 18 GHz with 43 dBm output power, >30% PAE and 22 dB small signal gain. ICP1543 is well suited to a variety of Test and Measurement and Aerospace & Defense applications.

Key Features

- Frequency Range: 12 – 18 GHz
- Pout: 43 dBm @ 24 dBm Pin
- PAE: > 30 %
- Small Signal Gain: 22 dB
- Bias: VD = 24V IDQ = 150 mA
- Technology: GaN on SiC
- Lead – Free and RoHS compliant
- Die Size = 3.75 mm x 3.45 mm

Functional Block Diagram



Applications

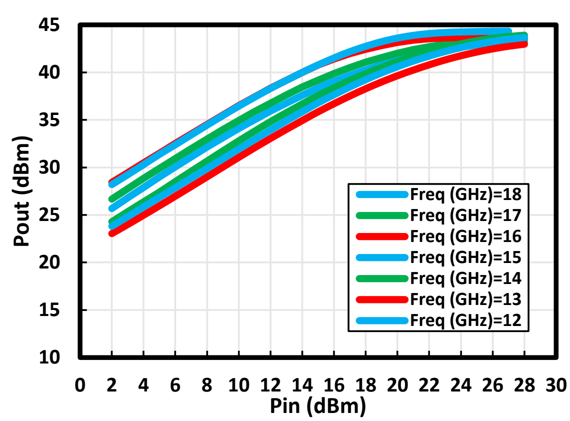
- Test and Measurement
- Aerospace & Defense

Performance Overview

Parameter	Typ.	Units
Frequency Range	12 – 18	GHz
Output Power @ Psat	43	dBm
Input Return Loss	10	dB
Output Return Loss	7	dB

Pout vs. Pin

(V_{DS} = 24V, I_{DQ} = 150 mA, Temp = 25 °C, CW)



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1. Electrical Specifications

1.1 Typical Electrical Performance

Table 1-1. Typical Electrical Performance at V_D = 24V, I_{DQ} = 150 mA, T_A = 25 °C, CW

Parameters	Conditions	Min	Typ	Max	Units
Frequency		12		18	GHz
Output Power @ P_{sat}	P_{in} = 25 dBm		43		dBm
PAE @ P_{sat}	P_{in} = 25 dBm		30		%
Small Signal Gain			22		dB
Input Return Loss			10		dB
Output Return Loss			7		dB

Table 1-2. Recommended Operating Conditions

Parameters	Values
Drain Voltage (V_D)	20V – 24V
Drain Quiescent Current (I_{DQ})	150 – 300 mA
Gate Voltage Range (V_G)	-2 to -1.5V
Operating Temperature (T_A)	-40 to +85 °C

1.2 Typical Performance Curves

The following graphs show the typical performance curves of the ICP1543 device at 25 °C, unless otherwise specified.

1.2.1 Typical Small Signal Data | Test conditions unless otherwise stated V_D = 20V, I_{DQ} = 150 mA

Figure 1-1. Input Return Loss

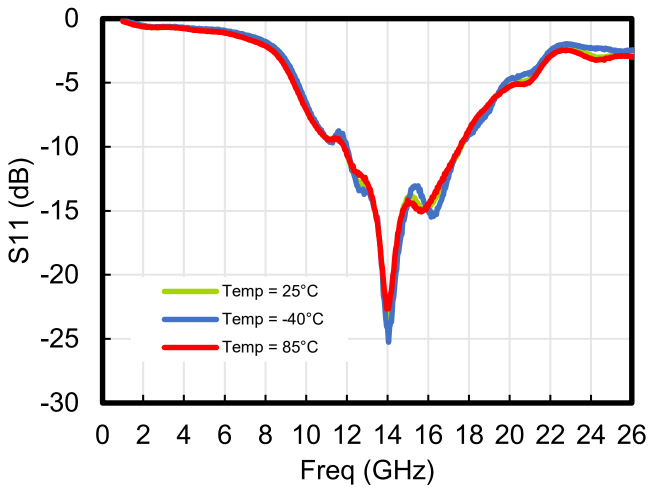


Figure 1-2. Gain

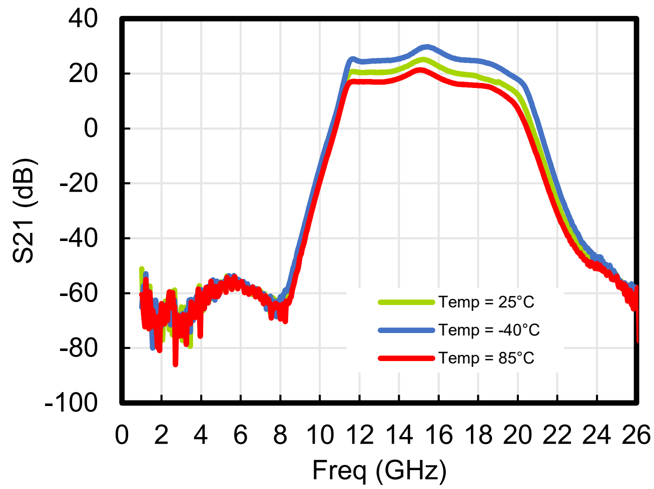


Figure 1-3. Reverse Isolation

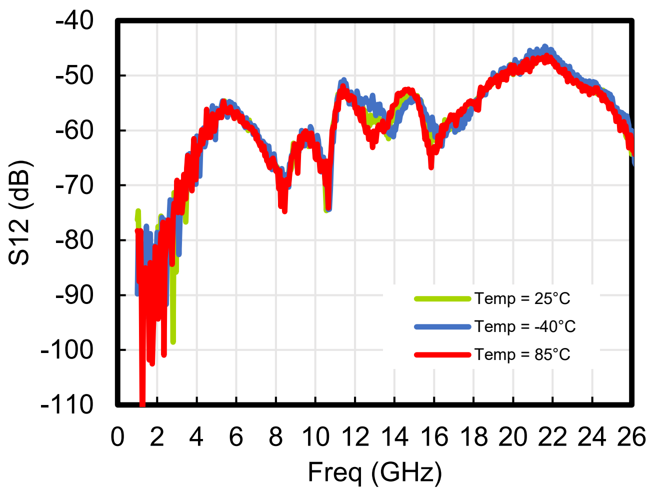
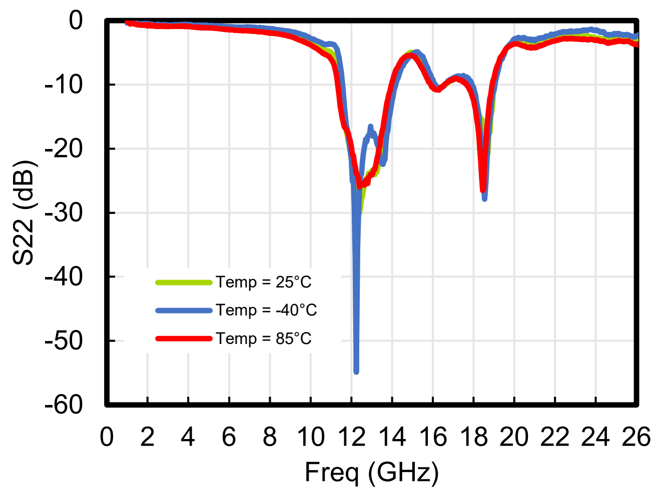


Figure 1-4. Output Return Loss



1.2.2 Typical Small Signal Data | Test conditions unless otherwise stated V_D = 24V, I_{DQ} = 150 mA

Figure 1-5. Input Return Loss

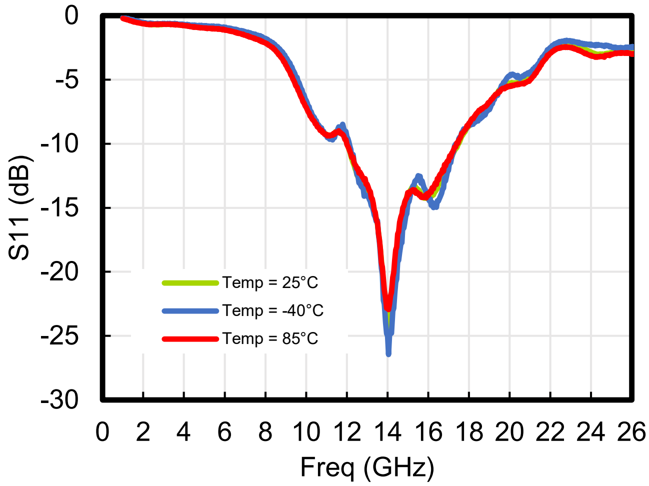


Figure 1-6. Gain

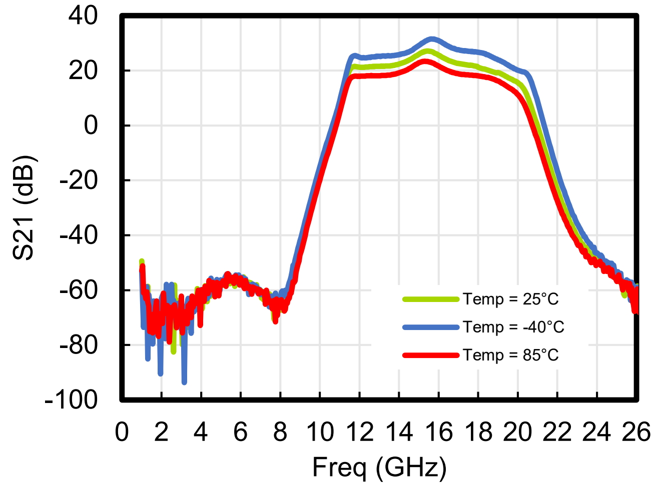


Figure 1-7. Reverse Isolation

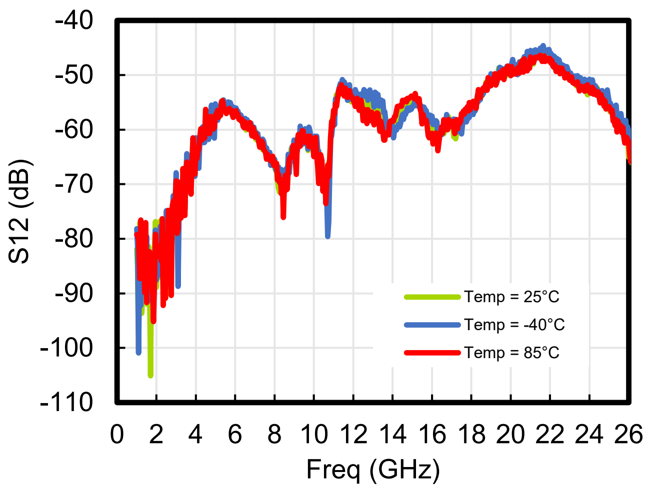
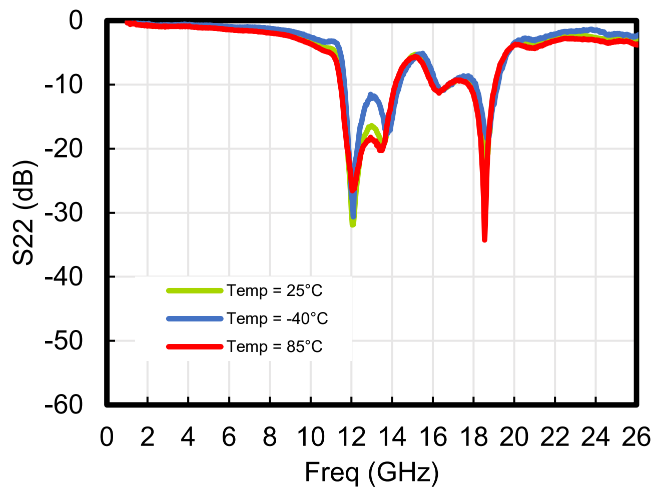


Figure 1-8. Output Return Loss



1.2.3 Typical Large Signal Data | Test conditions unless otherwise stated V_D = 20V, I_{DQ} = 150 mA, T_A = 25 °C, Pulse width = 100 µs, Pulse period = 1 ms

Figure 1-9. P_{out} **vs.** P_{in}

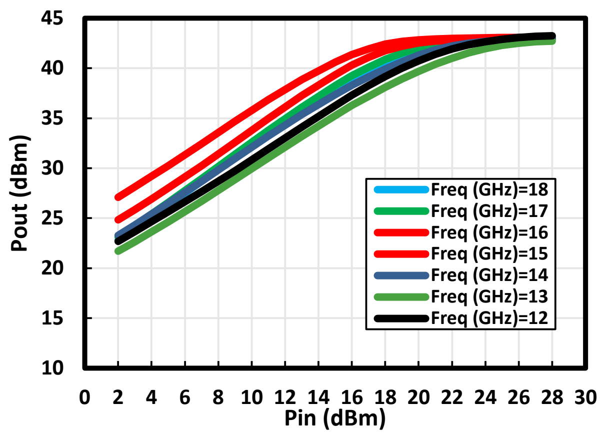


Figure 1-10. Gain vs. P_{in}

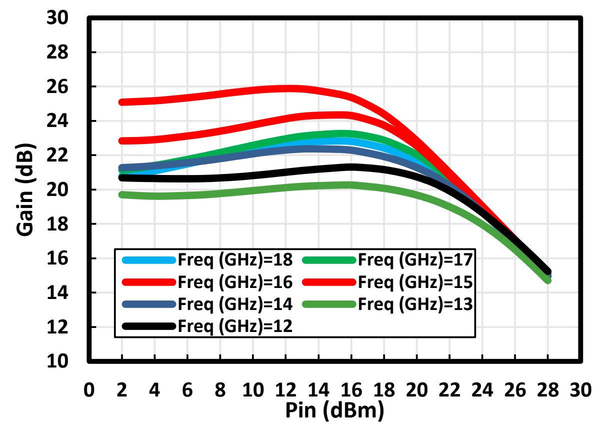


Figure 1-11. PAE vs. P_{in}

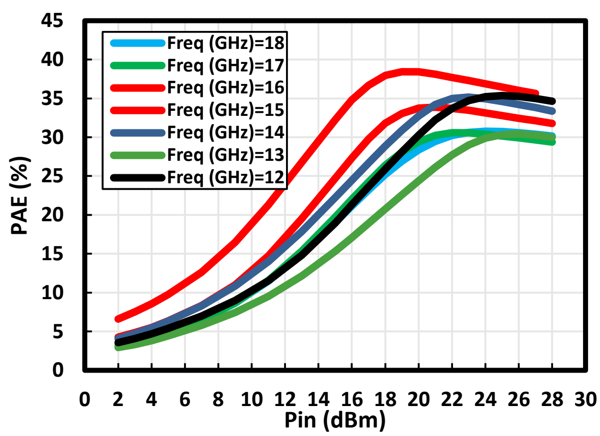


Figure 1-12. Drain Current vs. P_{in}

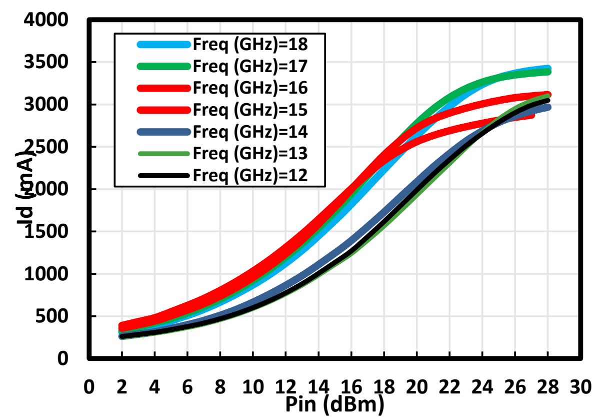


Figure 1-13. P_{out} **vs. Freq**

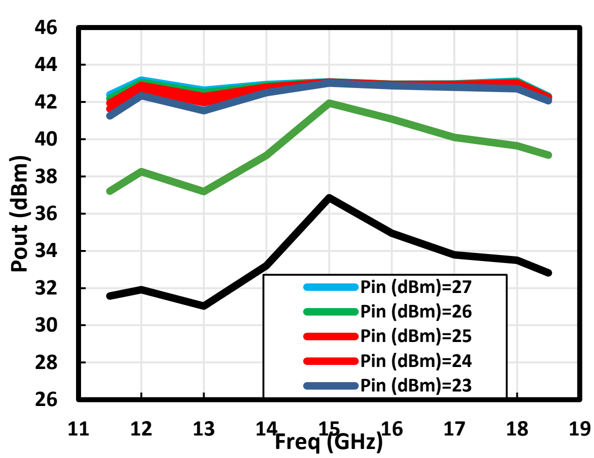
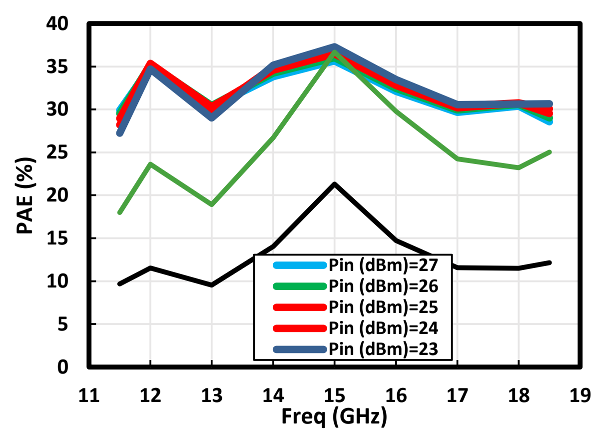


Figure 1-14. PAE vs. Freq



1.2.4 Typical Large Signal Data | Test conditions unless otherwise stated V_D = 24V, I_{DQ} = 150 mA, TA = 25 °C, Pulse width = 100 µs, Pulse Period = 1 ms

Figure 1-15. P_{out} vs. P_{in}

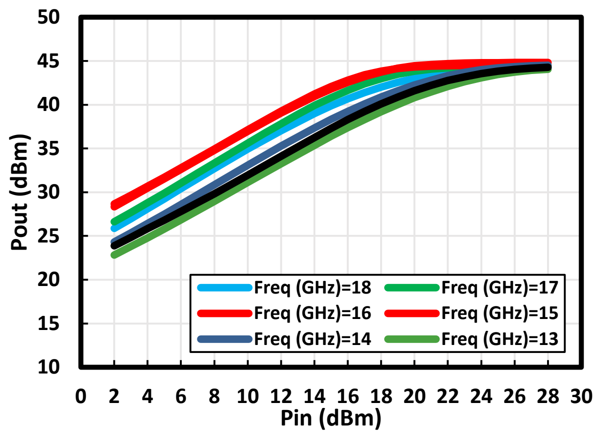


Figure 1-16. Gain vs. P_{in}

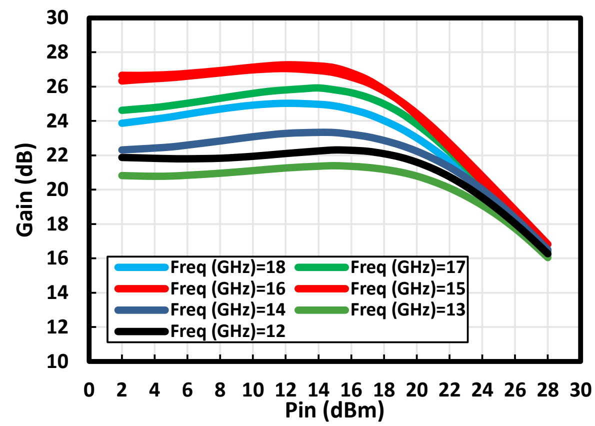


Figure 1-17. PAE vs. P_{in}

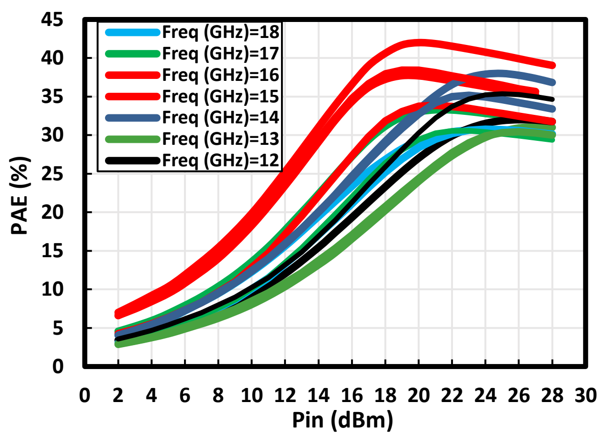


Figure 1-18. Drain Current vs. P_{in}

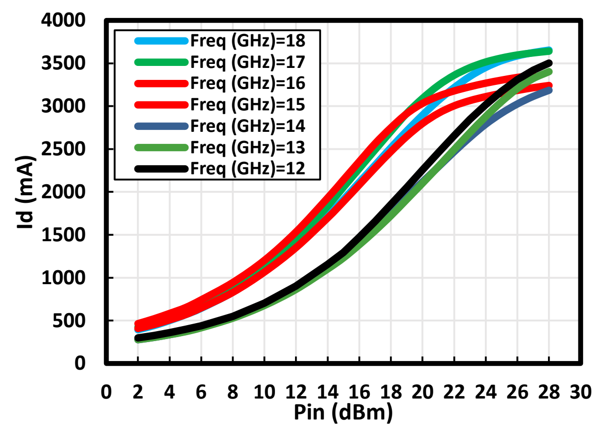


Figure 1-19. P_{out} vs. Freq

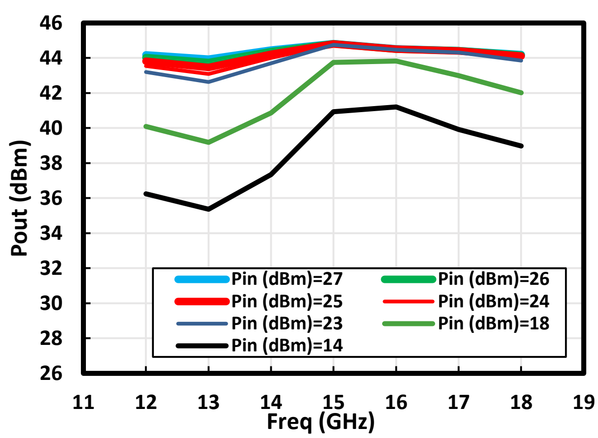
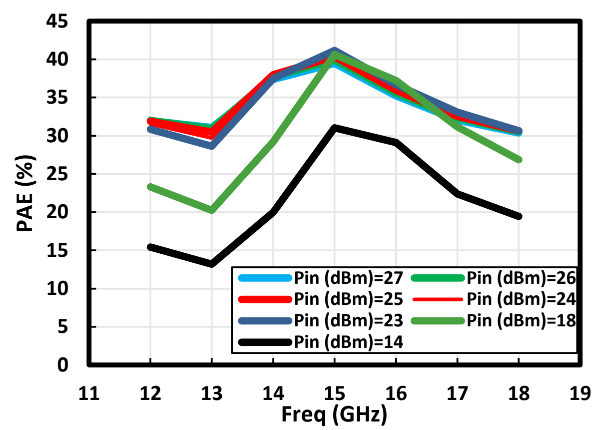


Figure 1-20. PAE vs. Freq



1.2.5 Typical Large Signal Data | Test conditions unless otherwise stated V_D = 20V, I_{DQ} = 150 mA, TA = 25 °C, CW

Figure 1-21. P_{out} vs. P_{in}

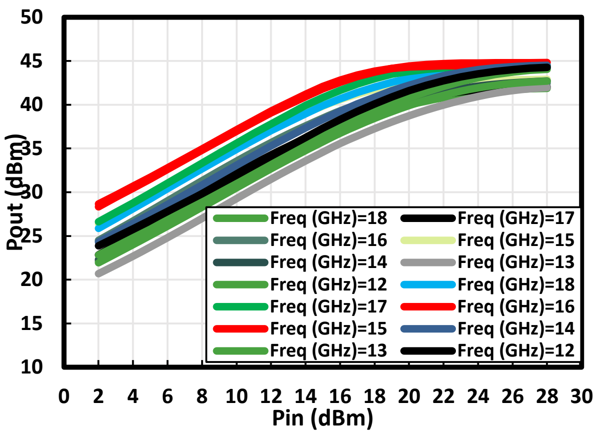


Figure 1-22. Gain vs. P_{in}

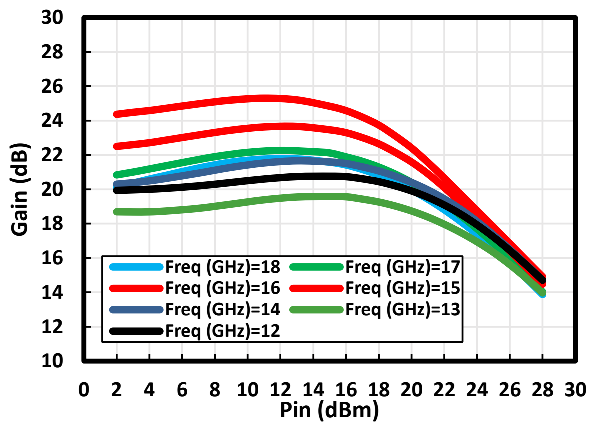


Figure 1-23. PAE vs. P_{in}

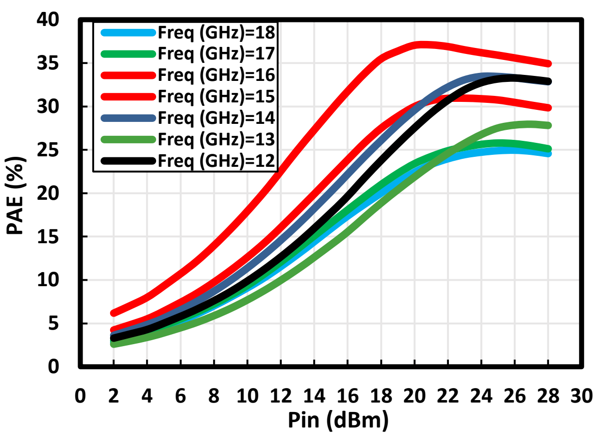


Figure 1-24. Drain Current vs. P_{in}

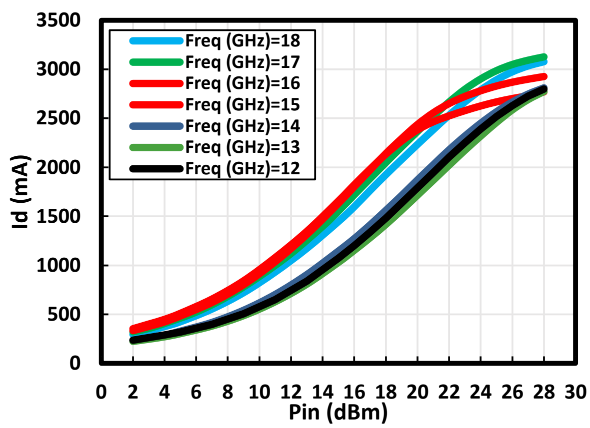


Figure 1-25. P_{out} vs. Freq

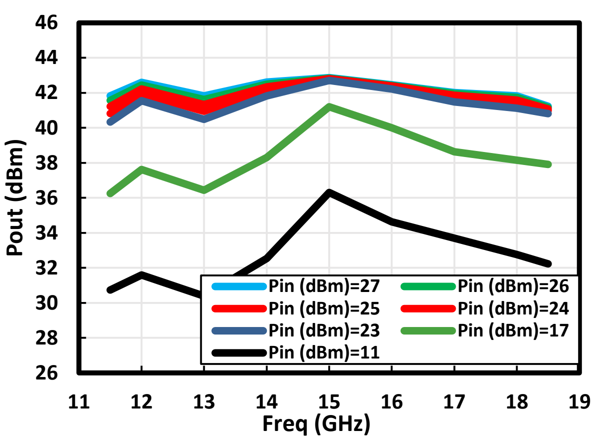
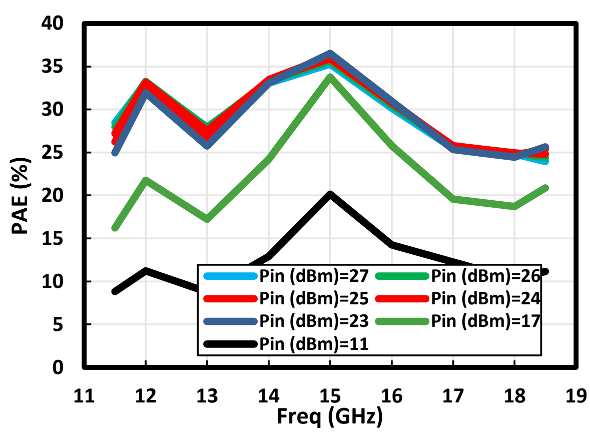


Figure 1-26. PAE vs. Freq



1.2.6 Typical Large Signal Data | Test conditions unless otherwise stated V_D = 24V, I_{DQ} = 150 mA, TA = 25 °C, CW

Figure 1-27. P_{out} vs. P_{in}

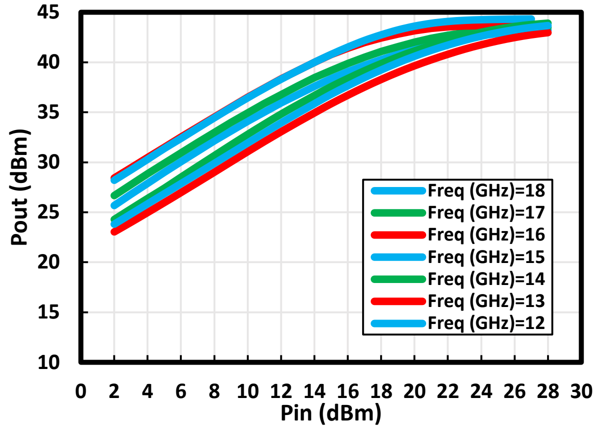


Figure 1-28. Gain vs. P_{in}

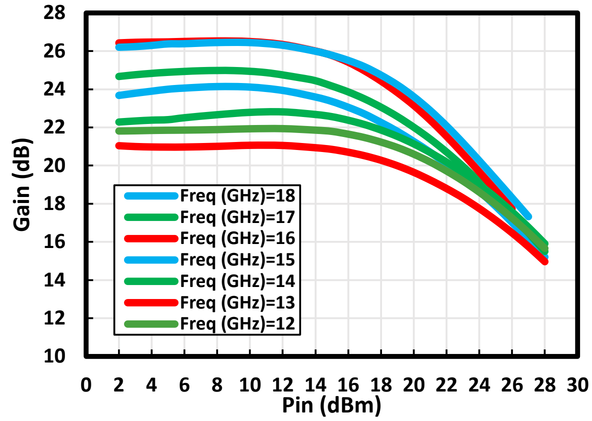


Figure 1-29. PAE vs. P_{in}

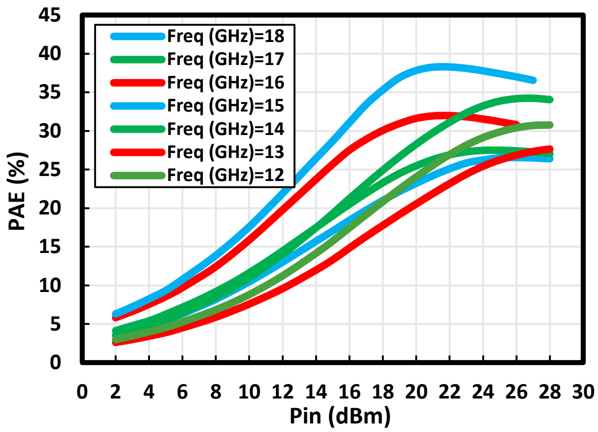


Figure 1-30. Drain Current vs. P_{in}

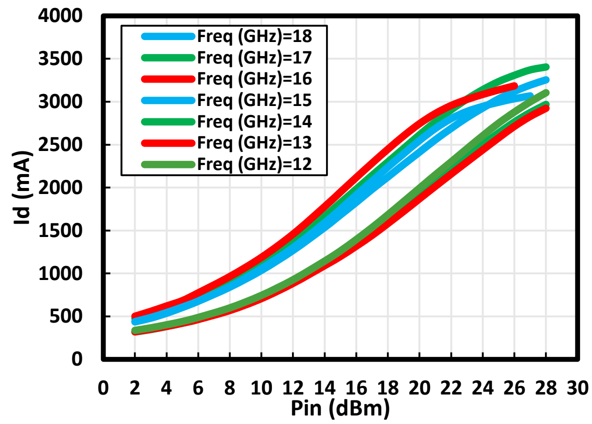


Figure 1-31. P_{out} vs. Freq

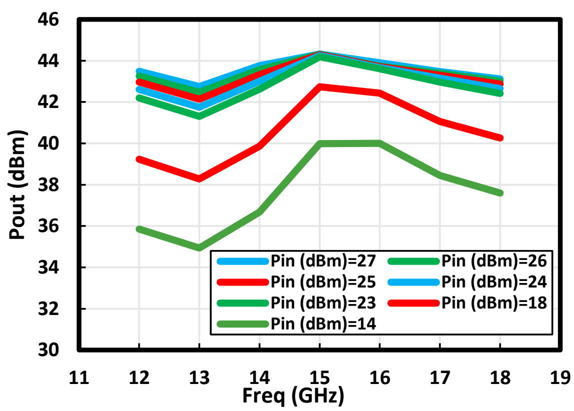
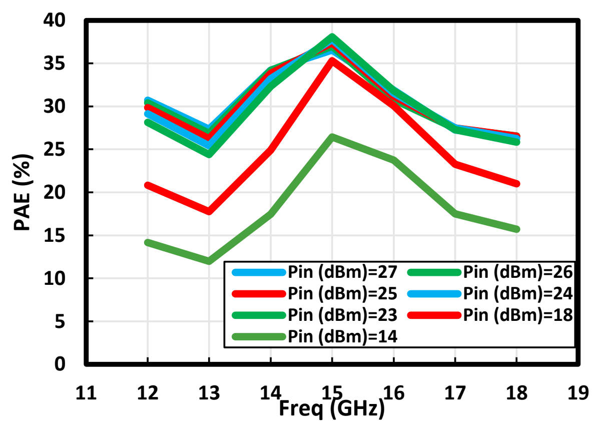


Figure 1-32. PAE vs. Freq



1.2.7 Typical Large Signal Data | Test conditions unless otherwise stated V_D = 24V, I_{DQ} = 150 mA, Freq = 12 GHz, Pulse width = 100 µs, Pulse period = 1 ms

Figure 1-33. P_{out} vs. P_{in}

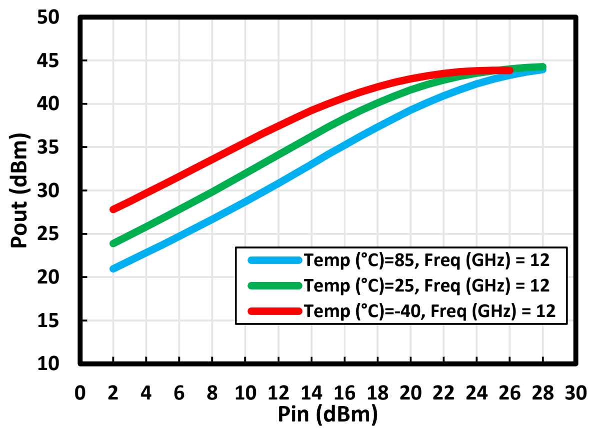


Figure 1-34. Gain vs. P_{in}

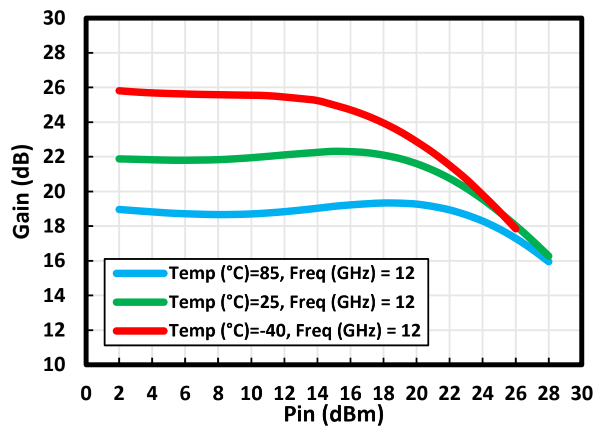


Figure 1-35. PAE vs. P_{in}

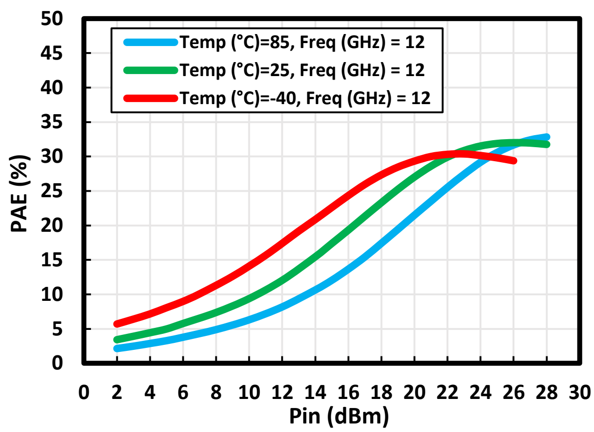


Figure 1-36. Drain Current vs. P_{in}

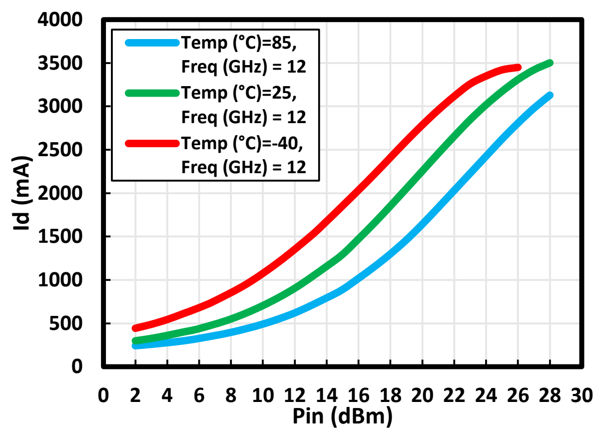
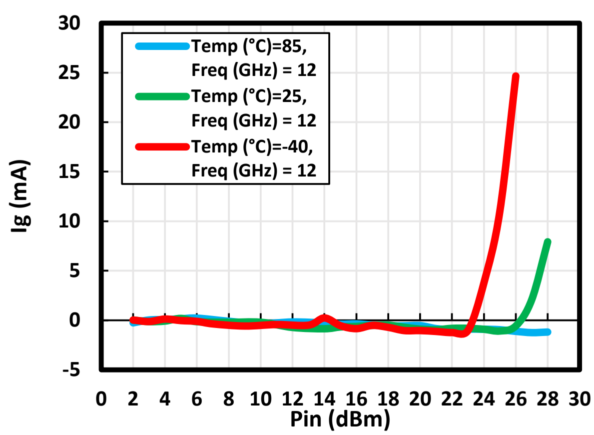


Figure 1-37. Gate Current vs. P_{in}



1.2.8 Typical Large Signal Data | Test conditions unless otherwise stated V_D = 24V, I_{DQ} = 150 mA, Freq = 15 GHz, Pulse width = 100 µs, Pulse period = 1 ms

Figure 1-38. P_{out} vs. P_{in}

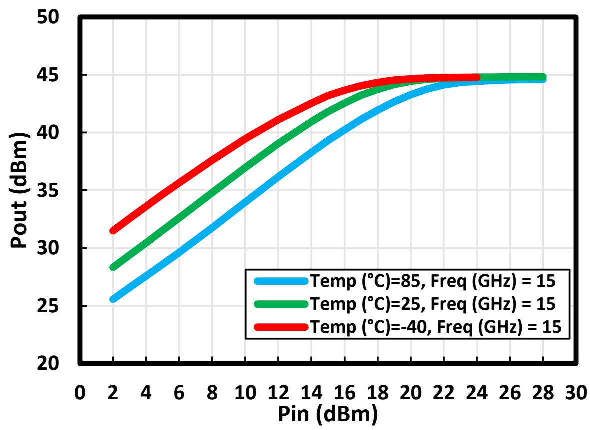


Figure 1-39. Gain vs. P_{in}

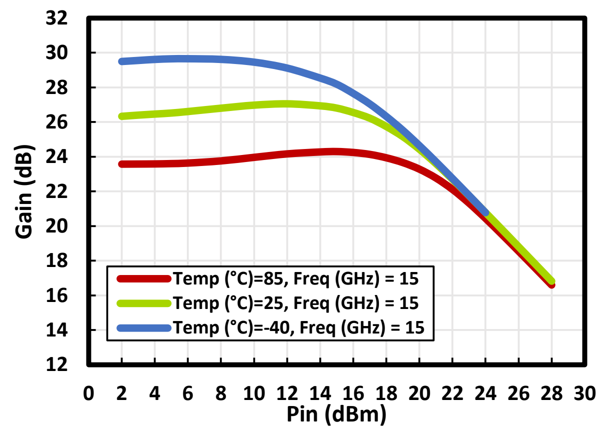


Figure 1-40. PAE vs. P_{in}

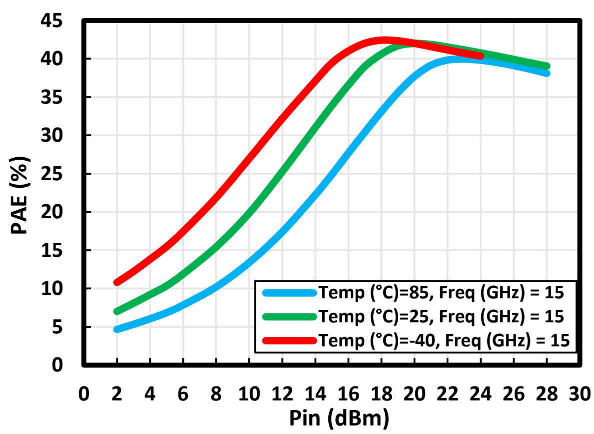


Figure 1-41. Drain Current vs. P_{in}

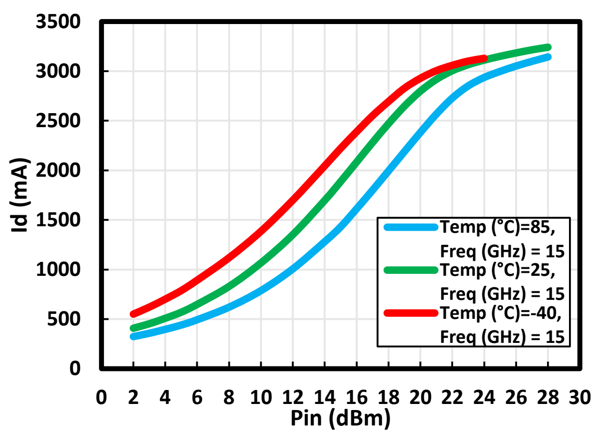
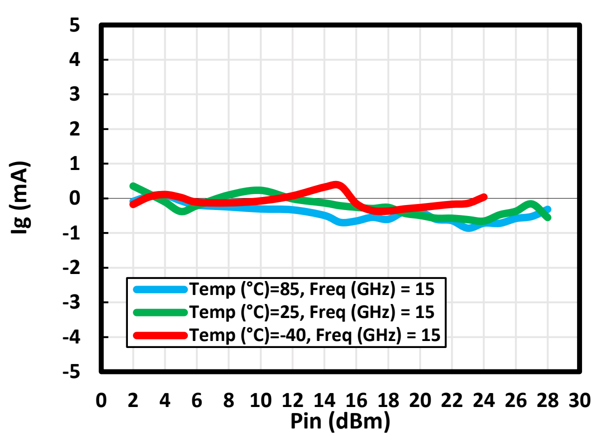


Figure 1-42. Gate Current vs. P_{in}



1.2.9 Typical Large Signal Data | Test conditions unless otherwise stated V_D = 24V, I_{DQ} = 150 mA, Freq = 18 GHz, Pulse width = 100 µs, Pulse period = 1 ms

Figure 1-43. P_{out} vs. P_{in}

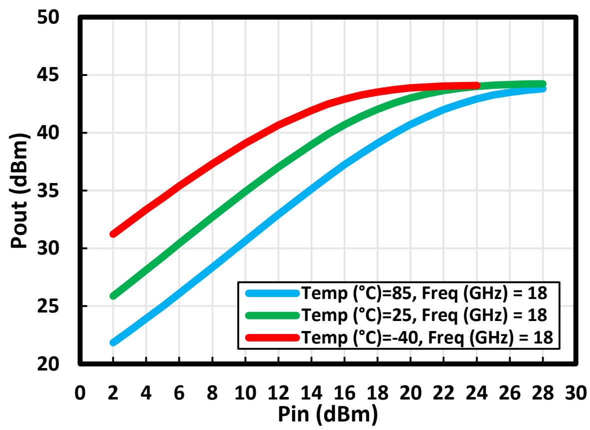


Figure 1-44. Gain vs. P_{in}

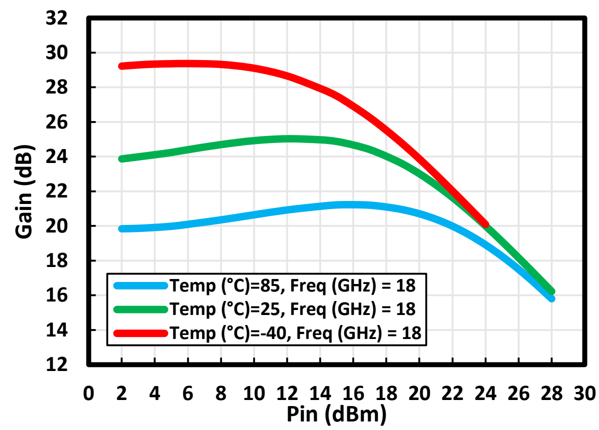


Figure 1-45. PAE vs. P_{in}

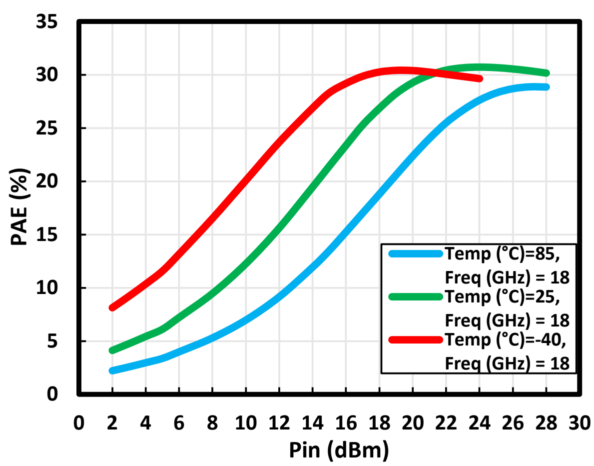


Figure 1-46. Drain Current vs. P_{in}

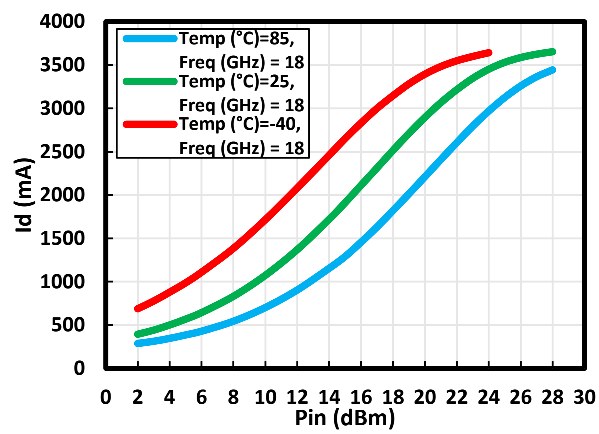
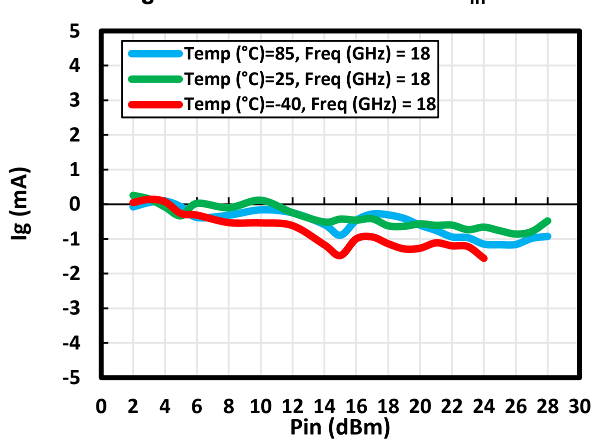


Figure 1-47. Gate Current vs. P_{in}



1.2.10 Typical Large Signal Data | Test condition unless otherwise stated I_{DQ} = 150 mA, Pulse width = 100 µs, Pulse period = 1 ms

Figure 1-48. P_{out} vs. Freq

(V_{DS} = 20V, I_{DQ} = 150 mA, Pulse = 100 µs / 1 ms)

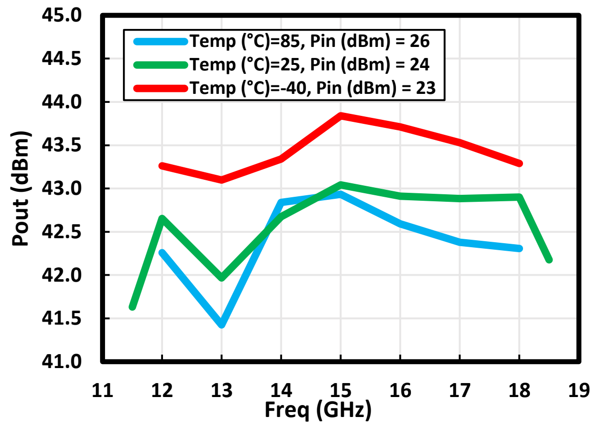


Figure 1-49. P_{out} vs. Freq

(V_{DS} = 24V, I_{DQ} = 150 mA, Pulse = 100 µs / 1 ms)

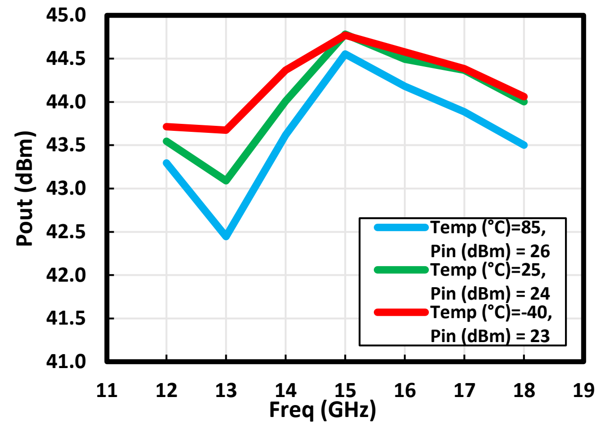


Figure 1-50. PAE vs. Freq

(V_{DS} = 20V, I_{DQ} = 150 mA, Pulse = 100 µs / 1 ms)

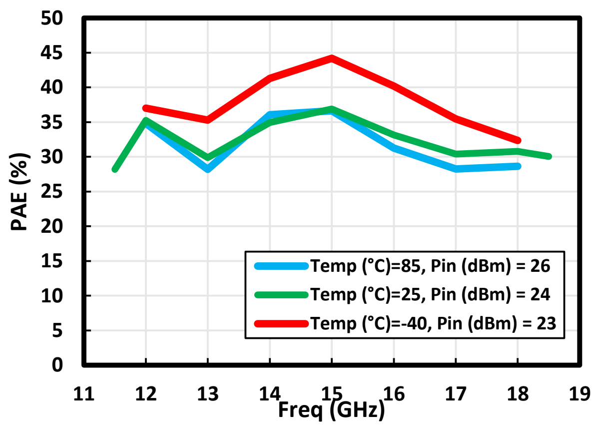


Figure 1-51. PAE vs. Freq

(V_{DS} = 24V, I_{DQ} = 150 mA, Pulse = 100 µs / 1 ms)

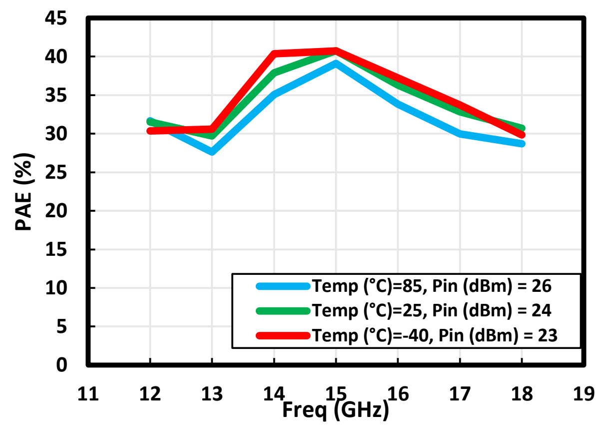


Figure 1-52.

(V_{DS} = 20V, I_{DQ} = 150 mA, Pulse = 100 µs / 1 ms)

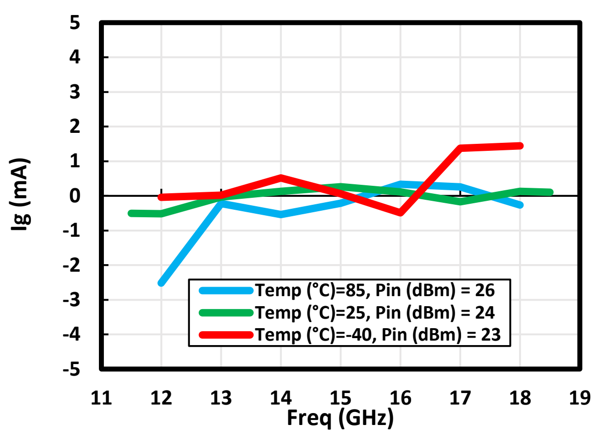
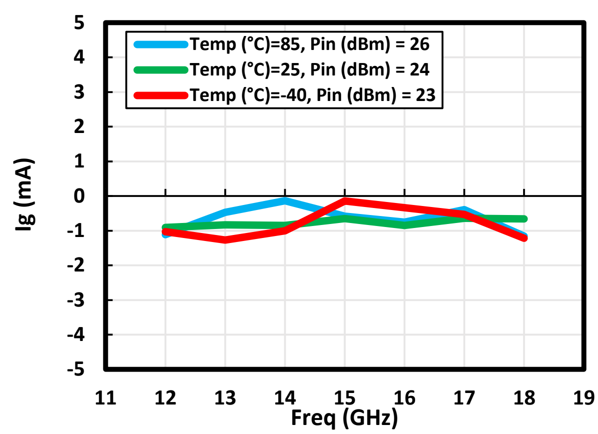


Figure 1-53. Gate Current vs. Freq

(V_{DS} = 24V, I_{DQ} = 150 mA, Pulse = 100 µs / 1 ms)



1.2.11 Typical Large Signal Data | Test conditions unless otherwise stated I_{DQ} = 150 mA, CW

Figure 1-54. P_{out} vs. Freq
(V_{DS} = 20V, I_{DQ} = 150 mA, CW)

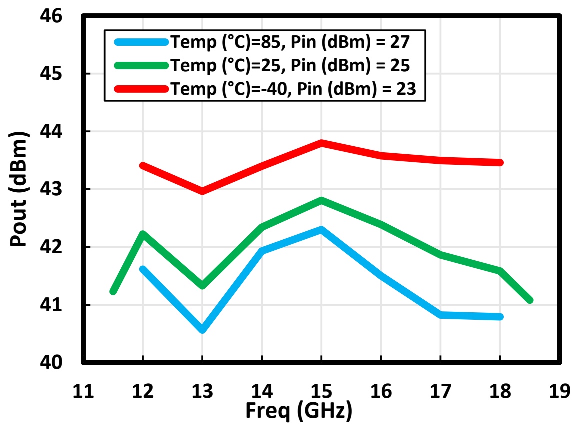


Figure 1-55. P_{out} vs. Freq
(V_{DS} = 24V, I_{DQ} = 150 mA, CW)

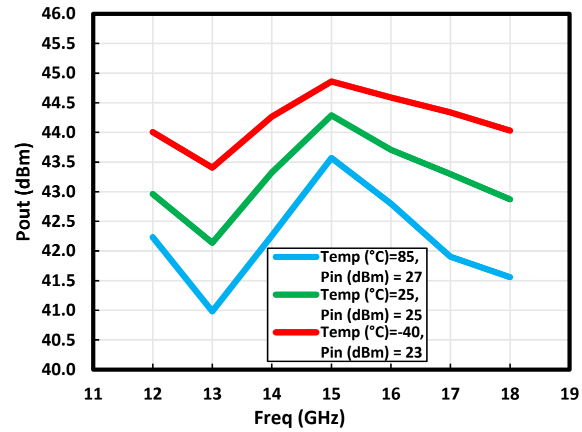


Figure 1-56. PAE vs. Freq
(V_{DS} = 20V, I_{DQ} = 150 mA, CW)

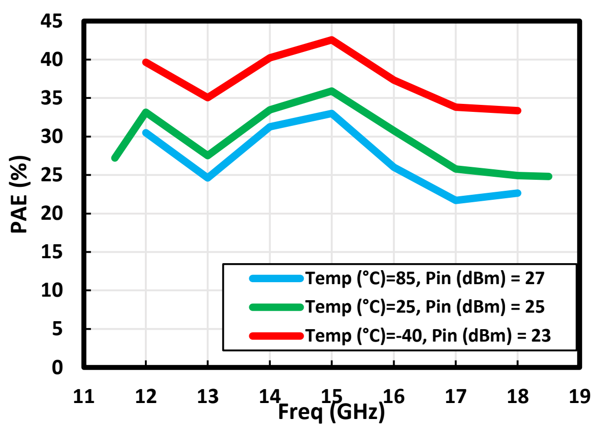


Figure 1-57. PAE vs. Freq
(V_{DS} = 24V, I_{DQ} = 150 mA, CW)

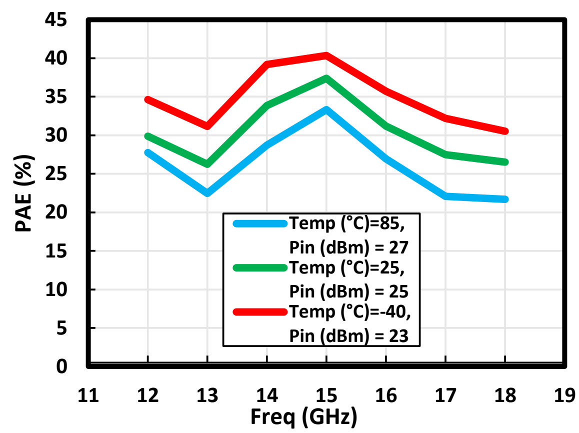


Figure 1-58. Gate Current vs. Freq
(V_{DS} = 20V, I_{DQ} = 150 mA, CW)

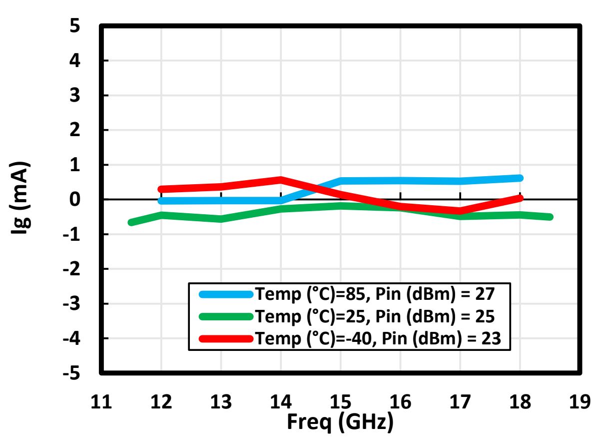
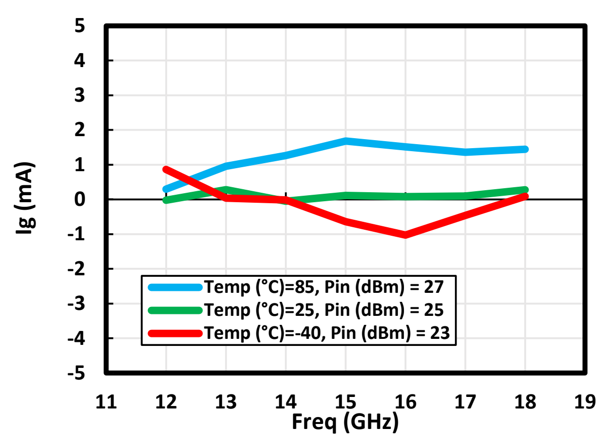


Figure 1-59. Gate Current vs. Freq
(V_{DS} = 24V, I_{DQ} = 150 mA, CW)



1.2.12 Typical Two Tone Data | Test condition unless otherwise stated V_D = 24V, I_{DQ} = 150 mA, Tone Spacing = 1 MHz

Figure 1-60. IM3 vs. P_{out}

(Freq = 12 GHz, V_{DS} = 24V, Temp = 25 °C)

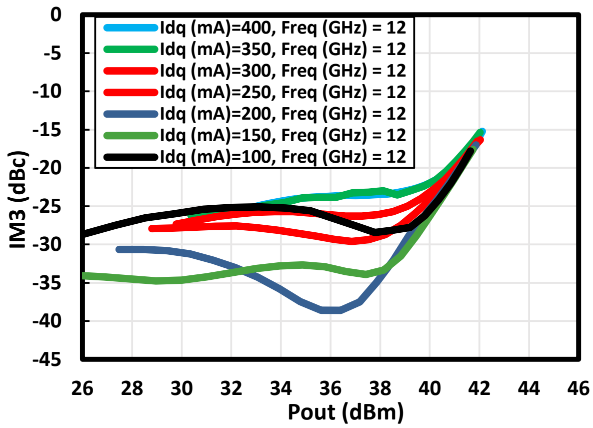


Figure 1-61. IM3 vs. P_{out}

(V_{DS} = 24V, I_{DQ} = 150 mA, Temp = 25 °C)

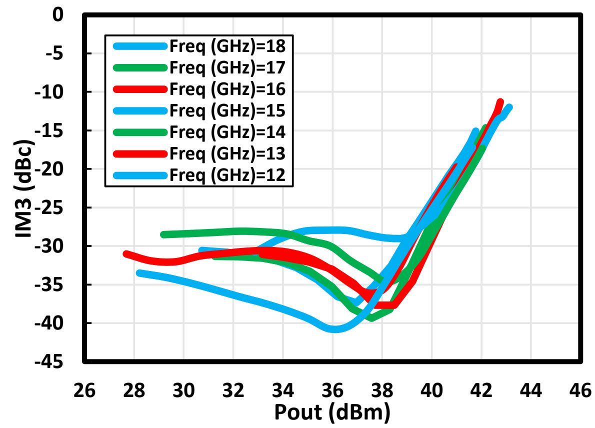


Figure 1-62. IM3 vs. P_{out}

(Freq = 15 GHz, V_{DS} = 24V, Temp = 25 °C)

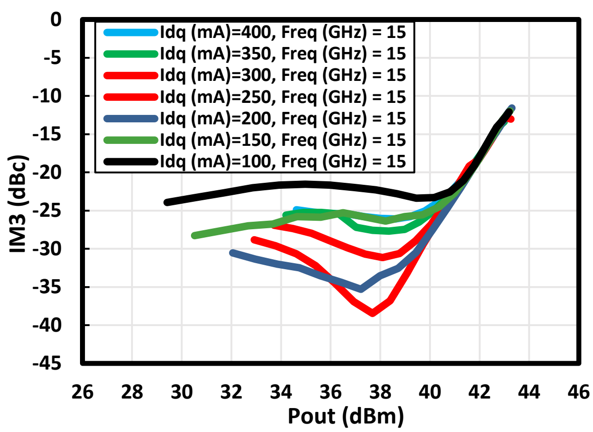


Figure 1-63. IM3 vs. P_{out}

(V_{DS} = 24V, I_{DQ} = 150 mA, Temp = -40 °C)

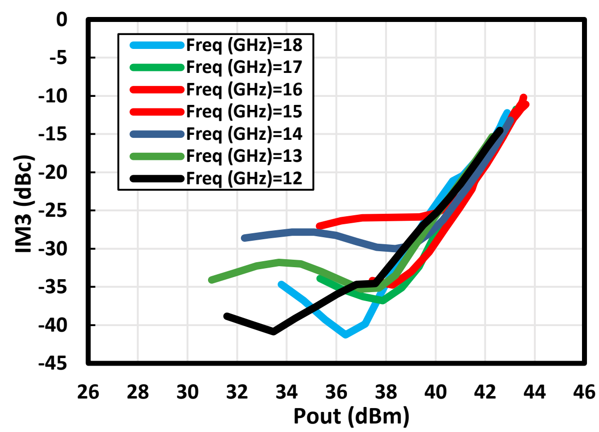


Figure 1-64. IM3 vs. P_{out}

(Freq = 18 GHz, V_{DS} = 24V, Temp = 25 °C)

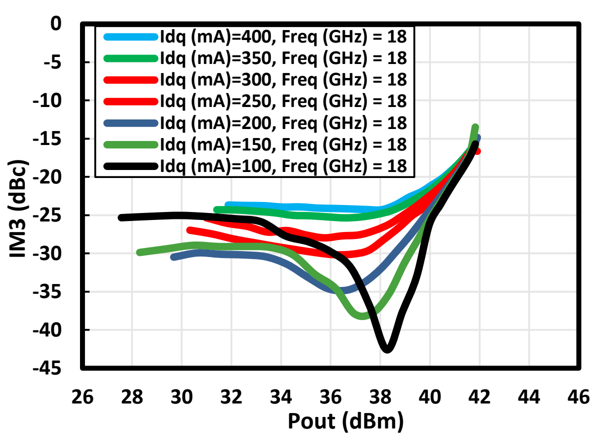
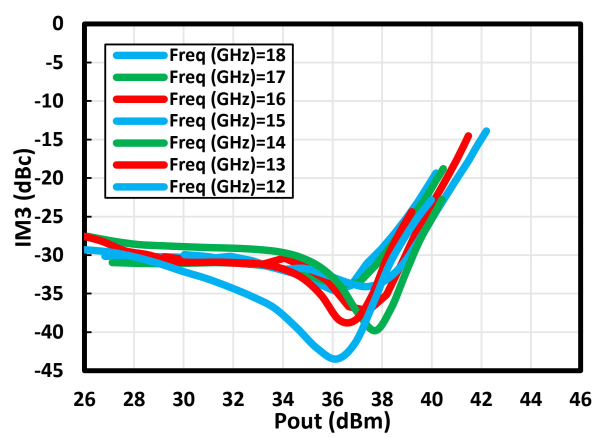


Figure 1-65. IM3 vs. P_{out}

(V_{DS} = 24V, I_{DQ} = 150 mA, Temp = 85 °C)



1.3 Absolute Maximum Ratings

Table 1-3. Thermal and Reliability

Parameter	Value
Thermal Resistance	1.1 °C/W

Notes:
1. Assumes silver sintered epoxy attach (20 µm thick) mounted on CuMo carrier.
2. Base temperature is assumed at the top of the CuMo carrier.
3. Thermal resistance calculated using IR measurement of the channel temperature.

Exceeding any one or combination of the absolute maximum limits may cause permanent damage to this device. ICONICRF does not recommend sustained operation near these survivability limits.

Table 1-4. Absolute Maximum Ratings

Parameters	Absolute Maximums
Drain Voltage (VDG)	30V
Gate Voltage Range (VG)	- 5V to 0V
Drain Current (ID) TA = 25 °C	8A
Gate Current (IG)	6.0 mA
Power Dissipation (CW) TA = 25 °C	180W
Power Dissipation (CW) TA = 85 °C	125W
CW Input Power	+ 28 dBm
Channel Temperature	275 °C
Eutectic Die Attach Temperature (30s)	320 °C
Storage Temperature	- 65 °C to + 150 °C

ESD Sensitive Device

2. Die Specifications

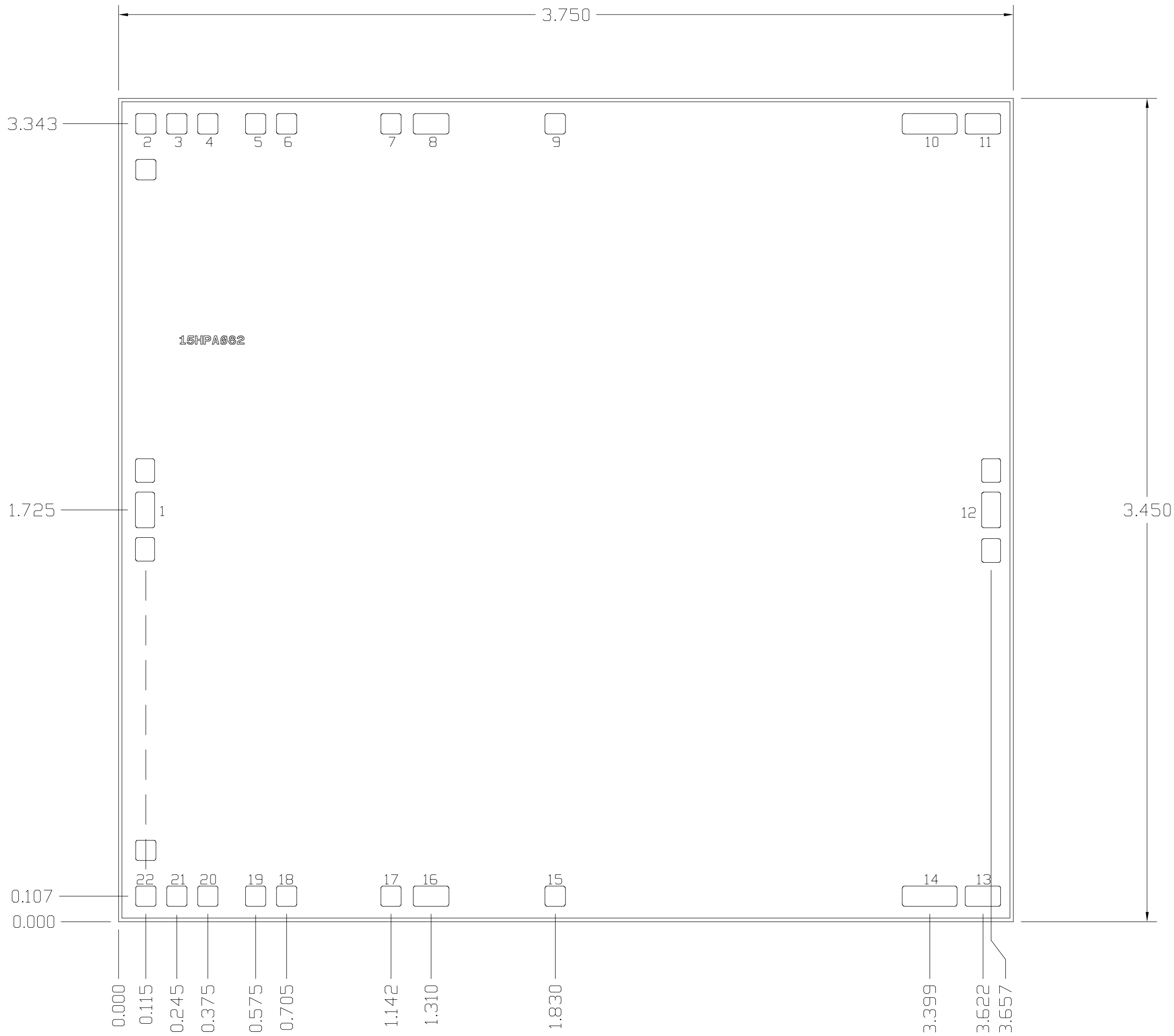


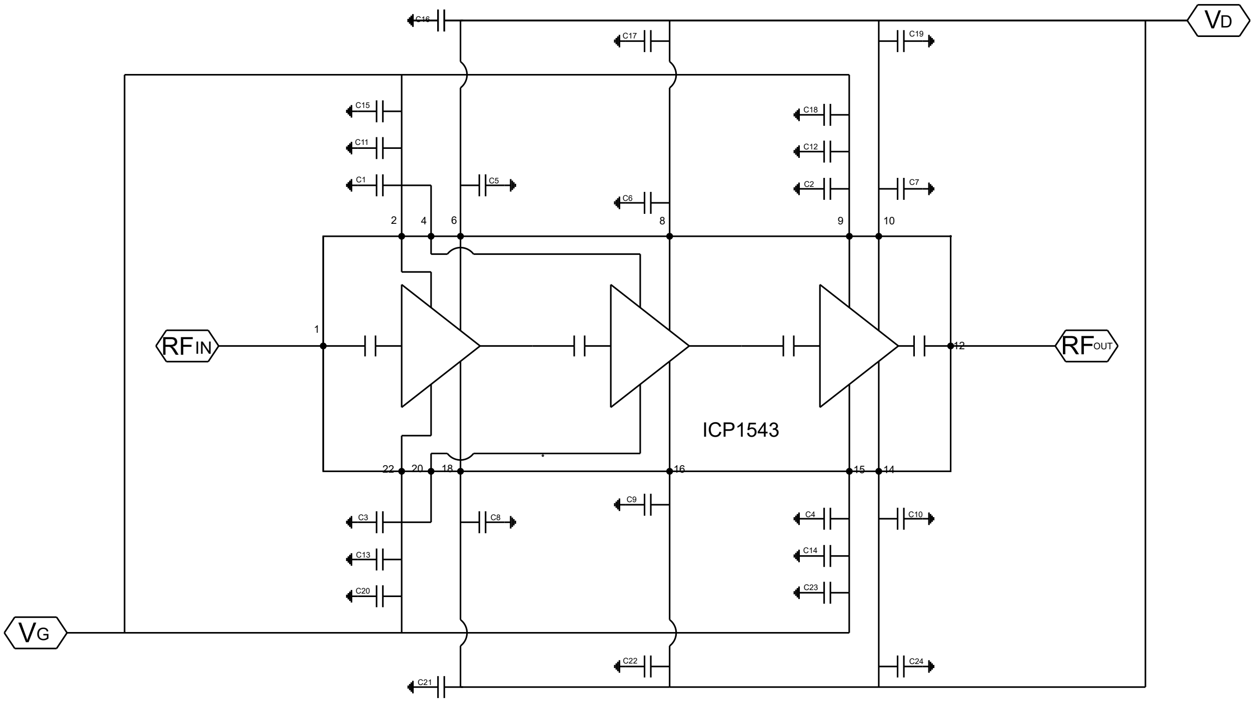
Table 2-1. Pad Description

Pad No	Pad Size (µm)	Function	Description
1	80 x 150	RFIN	50 ohm RF input, DC blocked
2, 22	85 x 85	VG1	First stage gate bias, decoupling and bypass caps required, must be biased from both sides
4, 20	85 x 85	VG2	Second stage gate bias, decoupling and bypass caps required, must be biased from both sides

...........continued

Pad No	Pad Size (µm)	Function	Description
6, 18	85 x 85	VD1	First stage drain voltage, decoupling and bypass caps required, must be biased from both sides
8, 16	150 x 80	VD2	Second stage drain voltage, decoupling and bypass caps required, must be biased from both sides
9, 15	85 x 85	VG3	Third stage gate bias, decoupling and bypass caps required, must be biased from both sides
10, 14	230 x 85	VD3	Third stage drain voltage, decoupling and bypass caps required, must be biased from both sides
12	80 x 150	RFOUT	50 ohm RF output, DC blocked, pad is DC grounded
3, 5, 7, 17, 19, 21	85 x 85	GND	Topside ground
11, 13	150 x 85	GND	Topside ground

3. Application Circuits



Component ID	Value	Quantity	Description	Manufacturer Part No.
C1 – C10	1000 pF	10	1000 pF Capacitor 0402, COG, 50V	Various
C11 – C14	10 nF	4	10 nF Capacitor 0402, COG, 50V	Various
C15 – C24	1 µF	10	1 µF Capacitor 0603, 35V	Various

Assembly Guidance

Amplifier must be biased from both sides. Optimum RF power performance achieved by minimizing output RF bond wire length.

Interconnect assembly Notes:
- Ball bonding or wedge bonding is preferred technique.
- Force, time and ultrasonic parameters are critical
- Aluminum wire bonding is not recommended
- Bond Wire diameter of 1mil is recommended

Die attach of component using adhesive
- Vacuum collets are preferred method of pickup.
- Pickup method must be consider the avoidance of die are bridges.
- Silver sintered epoxy is recommended– Namics H9890–11, Kyocera CT2700R7S

Die attach of component using Eutectic
- Flux-less gold–tin (AuSn) (80% Au, 20% Sn with melting point of 280 °C) preform is preferred between the die and attached surface.
- Recommended preform should be approximately 0.0012” thick.

- Die bonder using heated collet with a temperature of 310 °C and die scrubbing should be used to ensure wetting and prevent formation of voids.
- Exposure to extreme temperature should be kept to a minimum.
- The optimum die attach environment is nitrogen atmosphere.

Reflow Process

- Maximum temperature 320 °C for 30 seconds
- Material matching for Coefficient of thermal expansion is crucial for long–term reliability

Bias–Up Procedure

1. Set V_G = –5V
2. Set V_D 24V
3. Adjust V_G positive until I_D quiescent is 150 mA (Typical V_G = –1.9V)
4. Limit I_D to 5A
5. Apply RF Signal

Bias–down Procedure

1. Turn off RF
2. Turn off V_D, allow drain capacitor to discharge
3. Turn off V_G

4. Ordering, Shipping and Handling

4.1 Handling Recommendations

Please observe the following precautions to avoid damage:

Static Sensitivity

Integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

4.2 Ordering Information

Part number	Description
ICP1543–1–110I	Bare die in Gel–Pack trays
ICP1543–1–501U	Evaluation Board with SMA connectors

4.3 Packing Information

Standard Format
Gel Packs

Note: Contact your Microchip sales representative for the minimum Die quantity order.

5. Revision History

Table Revision History

Revision	Date	Description
F	08/2022	Document Created.

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