IGLOO Low Power Flash FPGAs with Flash*Freeze Technology

INTRODUCTION

The IGLOO® family of flash FPGAs, based on a 130-nm flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOO devices enables entering and exiting an ultra-low power mode that consumes as little as 5 µW while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low power consumption (from 12 µW) while the IGLOO device is completely functional in the system. This allows the IGLOO device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOO devices the advantage of being a secure, low power, single-chip solution that is Instant On. IGLOO is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The AGL015 and AGL030 devices have no PLL or RAM support. IGLOO devices have up to 1 million system gates, supported with up to 144 kbits of true dual-port SRAM and up to 300 user I/Os.

M1 IGLOO devices support the high-performance, 32-bit Cortex-M1 processor developed by ARM for implementation in FPGAs. Cortex-M1 is a soft processor that is fully implemented in the FPGA fabric. It has a three-stage pipeline that offers a good balance between low power consumption and speed when implemented in an M1 IGLOO device. The processor runs the ARMv6-M instruction set, has a configurable nested interrupt controller, and can be implemented with or without the debug block. Cortex-M1 is available for free from MicrochipMicrochip for use in M1 IGLOO FPGAs. The ARM-enabled devices have ordering numbers that begin with M1AGL and do not support AES decryption.

Features

LOW POWER

- 1.2V to 1.5V Core Voltage Support for Low Power
- Supports Single-Voltage System Operation
- 5 µW Power Consumption in Flash*Freeze Mode
- Low Power Active FPGA Operation
- Flash*Freeze Technology Enables Ultra-Low Power Consumption while Maintaining FPGA Content
- Easy Entry to/Exit from Ultra-Low Power Flash*Freeze Mode

HIGH CAPACITY

- 15K to 1 Million System Gates
- Up to 144 Kbits of True Dual-Port SRAM
- Up to 300 User I/Os

REPROGRAMMABLE FLASH TECHNOLOGY

- 130-nm, 7-Layer Metal, Flash-Based CMOS Process
- Instant On Level 0 Support
- Single-Chip Solution
- Retains Programmed Design When Powered Off

- 250 MHz (1.5V systems) and 160 MHz (1.2V systems) System Performance

IN-SYSTEM PROGRAMMING (ISP) AND SECURITY

- ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption (except ARM®-enabled IGLOO® devices) via JTAG (IEEE 1532–compliant)•
- FlashLock® Designed to Secure FPGA Contents

HIGH-PERFORMANCE ROUTING HIERARCHY

- Segmented, Hierarchical Routing and Clock Structure

ADVANCED I/O

- 700 Mbps DDR, LVDS-Capable I/Os (AGL250 and above)
- 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—up to 4 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3V/2.5V/1.8V/1.5V/1.2V, 3.3V PCI/3.3V PCI-X[1], and LVCMOS 2.5V / 5.0V Input•
- Differential I/O Standards: LVPECL, LVDS, B-LVDS, and M-LVDS (AGL250 and above)
- Wide Range Power Supply Voltage Support per JESD8-B, Allowing I/Os to Operate from 2.7V to 3.6V
- Wide Range Power Supply Voltage Support per JESD8-12, Allowing I/Os to Operate from 1.14V to 1.575V
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold-Sparing I/Os
- Programmable Output Slew Rate• and Drive Strength
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the IGLOO Family[2]

CLOCK CONDITIONING CIRCUIT (CCC) AND PLL•

- Six CCC Blocks, One with an Integrated PLL
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range (1.5 MHz up to 250 MHz)

EMBEDDED MEMORY

- 1 kbit of FlashROM User Nonvolatile Memory
- SRAMs and FIFOs with Variable-Aspect-Ratio 4,608-Bit• RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations)
- True Dual-Port SRAM (except ×18)•

1.AGL015 and AGL030 devices do not support this feature.
2.Supported only by AGL015 and AGL030 devices.

ARM Processor Support in IGLOO FPGAs

- M1 IGLOO Devices—Cortex®-M1 Soft Processor Available with or without Debug

TABLE 1: IGLOO DEVICES

IGLOO Devices	AGL015[1]	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000
ARM-Enabled IGLOO Devices[2]					M1AGL250		M1AGL600	M1AGL1000
System Gates	15,000	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000
Typical Equivalent Macrocells	128	256	512	1,024	2,048	——	—	—
VersaTiles (D-flip-flops)	384	768	1,536	3,072	6,144	9,216	13,824	24,576
Flash*Freeze Mode (typical, µW)	5	5	10	16	24	32	36	53
RAM kbits (1,024 bits)	—	—	18	36	36	54	108	144
4,608-Bit Blocks	—	—	4	8	8	12	24	32
FlashROM Kbits (1,024 bits)	1	1	1	1	1	1	1	1
AES-Protected ISP [2]	—	—	Yes	Yes	Yes	Yes	Yes	Yes
Integrated PLL in CCCs [3]	—	—	1	1	1	1	1	1
VersaNet Globals [4]	6	6	18	18	18	18	18	18
I/O Banks	2	2	2	2	4	4	4	4
Maximum User I/Os	49	81	96	133	143	194	235	300
Package Pins								
UC/CS		UC81[6], CS81	CS121 [3]	CS196	CS196 [5]	CS196	CS281	CS281
QFN	QN68	QN48, QN68[6], QN132[6]	QN132[6]	QN132[6]	QN132[6]			
VQFP		VQ100	VQ100	VQ100	VQ100			
FBGA				FG144	FG144	FG144, FG256, FG484[6]	FG144, FG256, FG484[6]	FG144, FG256, FG484

Note 1: AGL015 is not recommended for new designs

2: AES is not available for ARM-enabled IGLOO devices.

3: AGL060 in CS121 does not support the PLL.

4: Six chip (main) and twelve quadrant global networks are available for AGL060 and above.

5: The M1AGL250 device does not support this package.

6: Package not available.

7: The IGLOOe datasheet and IGLOOe FPGA Fabric User Guide provide information on higher densities and additional features.

I/Os Per Package[1]

TABLE 2: I/OS PER PACKAGE

IGLOO Devices	AGL015[2]	AGL030	AGL060	AGL125	AGL250		AGL400		AGL600		AGL1000	
ARM-Enabled IGLOO Devices					M1AGL250				M1AGL600		M1AGL1000	
Package	I/O Type[3]											
	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O[4]	Differential I/O Pairs	Single-Ended I/O[4]	Differential I/O Pairs	Single-Ended I/O[4]	Differential I/O Pairs	Single-Ended I/O[4]	Differential I/O Pairs
QN48	—	34	—	—	—	—	—	—	——	—	—	—
QN68[6]	49	49	—	—	—	—	—	—	—	—	—	—
UC81[6]	—	66	—	—	—	—	—	—	—	—	—	—
CS81	—	66	—	—	—	—	—	—	—	—	—	—
CS121[6]	—	—	96	96	—	—	—	—	—	—	—	—
VQ100	—	77	71	71	68	13	—	—	—	—	—	—
QN132[6]	—	81	80	84	—	—	—	—	—	—	—	—
CS196	—	—	—	133	143[5]	35[5]	143	35	—	—	—	—
FG144	—	—	—	97	97	24	97[6]	25[6]	97	25	97	25
FG256[7]	—	—	—	—	—	—	178	38	177	43	177	44
CS281	—	—	—	—	—	—	—	—	215	53	215	53
FG484[7]	—	—	—	—	—	—	194[6]	38[6]	235[6]	60[6]	300	74

Note 1: When considering migrating your design to a lower- or higher-density device, refer to the IGLOO FPGA Fabric User Guide to ensure compliance with design and board migration requirements.

2: AGL015 is not recommended for new designs.

3: When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.

4: Each used differential I/O pair reduces the number of single-ended I/Os available by two.

5: The M1AGL250 device does not support QN132 or CS196 packages.

6: Package not available.

7: FG256 and FG484 are footprint-compatible packages.

TABLE 3: IGLOO FPGAS PACKAGE SIZES DIMENSIONS

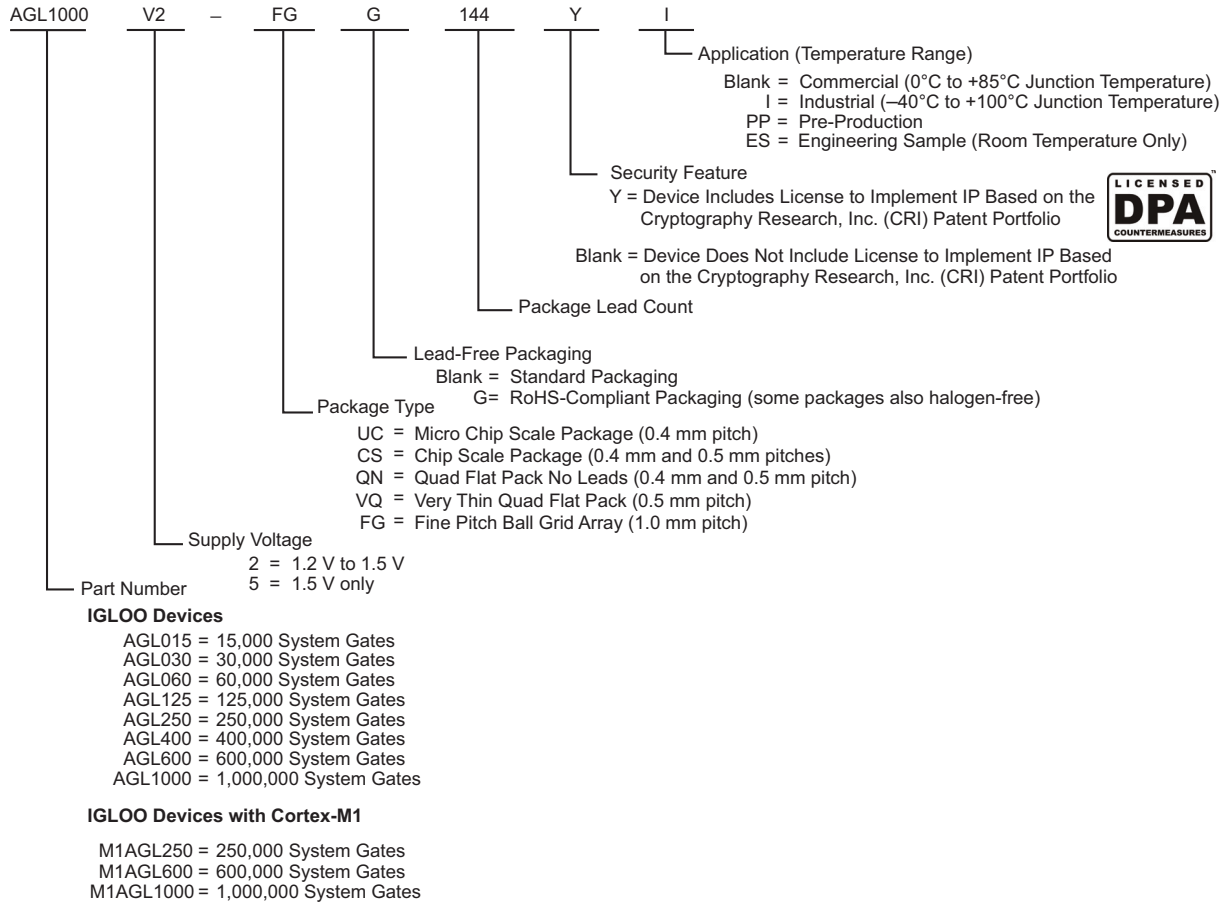
Package	UC81*	CS81	CS121	QN48	QN68	QN132*	CS196	CS281	FG144	VQ100	FG256	FG484
Length × Width (mm\mm)	4 × 4	5 × 5	6 × 6	6 × 6	8 × 8	8 × 8	8 × 8	10 × 10	13 × 13	14 × 14	17 × 17	23 × 23

TABLE 3: IGLOO FPGAS PACKAGE SIZES DIMENSIONS

Package	UC81*	CS81	CS121	QN48	QN68	QN132*	CS196	CS281	FG144	VQ100	FG256	FG484
Nominal Area (mm^2)	16	25	36	36	64	64	64	100	169	196	289	529
Pitch (mm)	0.4	0.5	0.5	0.4	0.4	0.5	0.5	0.5	1.0	0.5	1.0	1.0
Height (mm)	0.80	0.80	0.99	0.90	0.90	0.75	1.20	1.05	1.45	1.00	1.60	2.23

Note: * Package not available.

IGLOO Ordering Information



Note: Marking Information: IGLOO V2 devices do not have V2 marking, but IGLOO V5 devices are marked accordingly.

Temperature Grade Offerings

TABLE 4: Temperature Grade Offerings

Package	AGL015 [1]	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000
					M1AGL250		M1AGL600	M1AGL1000
QN48	—	C, I	—	—	—	—	—	—
QN68	C, I	—	—	—	—	—	—	—
UC81[2]	—	C, I	—	—	—	—	—	—
CS81	—	C, I	—	—	—	—	—	—
CS121	—	—	C, I	C, I	—	—	—	—
VQ100	—	C, I	C, I	C, I	C, I	—	—	—
QN132[2]	—	C, I	C, I [2]	C, I	—	—	—	—
CS196	—	—	—	C, I	C, I	C, I	—	—
FG144	—	—	—	C, I	C, I	C, I	C, I	C, I

TABLE 4: Temperature Grade Offerings

Package	AGL015 [1]	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000
					M1AGL250		M1AGL600	M1AGL1000
FG256	—	—	—	—	—	C, I	C, I	C, I
CS281	—	—	—	—	—	—	C, I	C, I
FG484	—	—	—	—	—	C, I[2]	C, I[2]	C, I

Note 1: AGL015 is not recommended for new designs.
2: Package not available.
3: C = Commercial temperature range: 0°C to 85°C junction temperature.
4: I = Industrial temperature range: –40°C to 100°C junction temperature.

IGLOO Device Status

TABLE 5: IGLOO DEVICE STATUS

IGLOO Devices	Status	M1 IGLOO Devices	Status
AGL015	Not recommended for new designs.		
AGL030	Production		
AGL060	Production		
AGL125	Production		
AGL250	Production	M1AGL250	Production
AGL400	Production		
AGL600	Production	M1AGL600	Production
AGL1000	Production	M1AGL1000	Production

References made to IGLOO devices also apply to ARM-enabled IGLOOe devices. The ARM-enabled part numbers start with M1 (Cortex-M1).

AGL015 and AGL030

The AGL015 and AGL030 are architecturally compatible; there are no RAM or PLL features.

Devices Not Recommended For New Designs

AGL015 is not recommended for new designs.

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include -literature number) you are using.

Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

Contents

1.0 PRODUCT OVERVIEW

1.1 Flash*Freeze Technology

The IGLOO device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low power Flash*Freeze mode. IGLOO devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOO V2 devices to support a wide range of core voltage (1.2V to 1.5V) allows further reduction in power consumption, thus achieving the lowest total system power.

When the IGLOO device enters Flash*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash*Freeze mode, all activity resumes and data is retained.

The availability of low power modes, combined with reprogrammability, a single-chip and single-voltage solution, and availability of small-footprint, high pin-count packages, make IGLOO devices the best fit for portable electronics.

1.2 Flash Advantages

1.2.1 LOW POWER

Flash-based IGLOO devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO devices also have low dynamic power consumption to further maximize power savings; power is even further reduced by the use of a 1.2V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOO device the lowest total system power offered by any FPGA.

1.2.2 SECURITY

Nonvolatile, flash-based IGLOO devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of protection in the FPGA industry for intellectual property and configuration data. In addition, all FlashROM data in IGLOO devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of the IGLOO family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The IGLOO family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An IGLOO device provides the best available security for programmable logic designs.

1.2.3 SINGLE CHIP

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

1.2.4 INSTANT ON

Flash-based IGLOO devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based IGLOO devices greatly

simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO flash FPGAs allow the user to quickly enter and exit Flash*Freeze mode. This is done almost instantly (within 1 µs) and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs the device does not need to reload configuration and design state from external memory components; instead it retains all necessary information to resume operation immediately.

1.2.5 REDUCED COST OF OWNERSHIP

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, Flash-based IGLOO devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOO family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOO family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

1.2.6 FIRM-ERROR IMMUNITY

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

1.2.7 ADVANCED FLASH TECHNOLOGY

The IGLOO family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

1.2.8 ADVANCED ARCHITECTURE

The proprietary IGLOO architecture provides granularity comparable to standard-cell ASICs. The IGLOO device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-12 and Figure 1-2 on page 1-12):

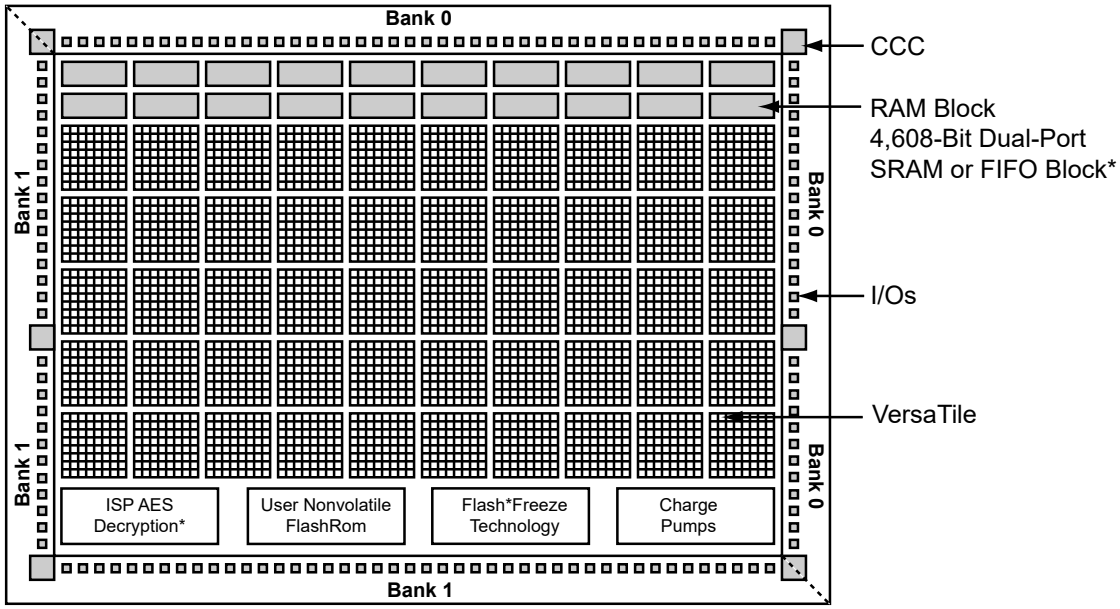
- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory[3]
- Extensive CCCs and PLLs[3]
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC® family of third-generation-architecture flash FPGAs.

3. The AGL015 and AGL030 do not support PLL or SRAM.

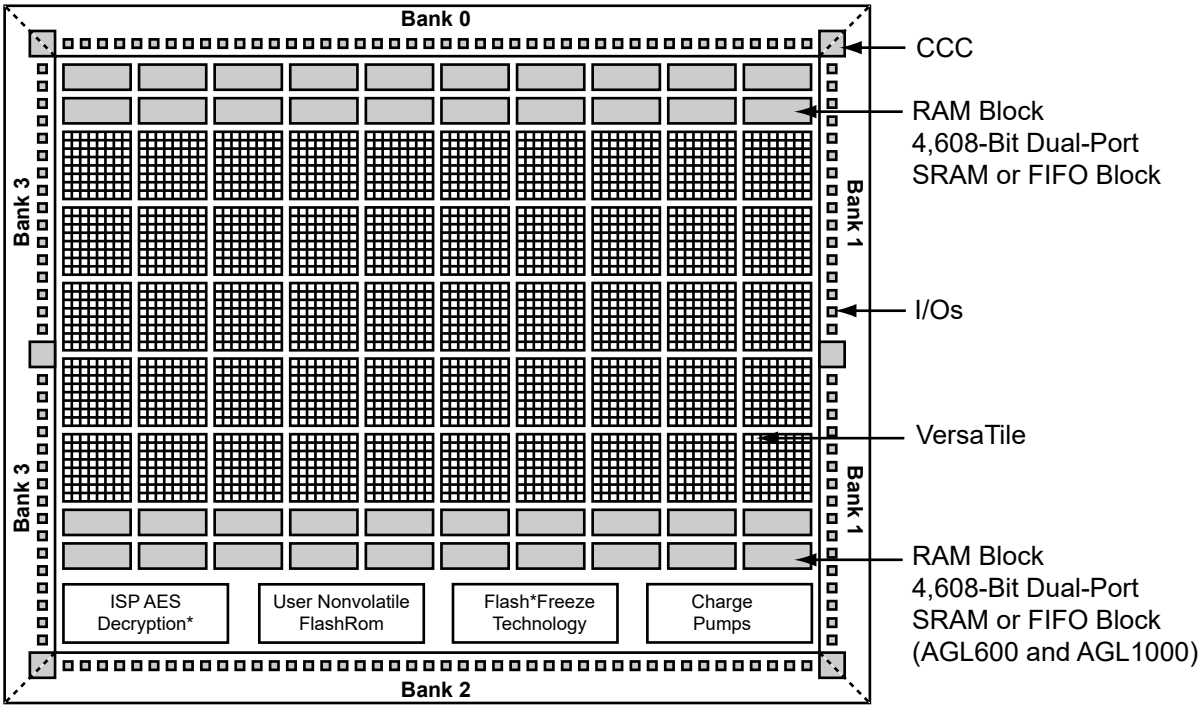
VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

FIGURE 1-1: IGLOO DEVICE ARCHITECTURE OVERVIEW WITH TWO I/O BANKS (AGL015, AGL030, AGL060, AND AGL125)



Note: *Not supported by AGL015 and AGL030 devices

FIGURE 1-2: IGLOO DEVICE ARCHITECTURE OVERVIEW WITH FOUR I/O BANKS (AGL250, AGL600, AGL400, AND AGL1000)



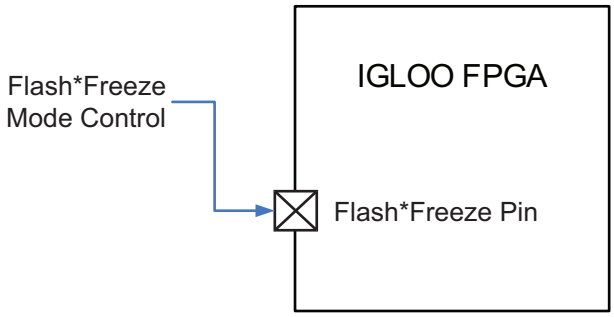
1.2.9 FLASH*FREEZE TECHNOLOGY

The IGLOO device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and states. I/O states are tristated during Flash*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 5 µW in this mode.

Flash*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device. The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned, which is advantageous because of the inherent low power static (as low as 12 µW) and dynamic capabilities of the IGLOO device. Refer to Figure 1-3, for an illustration of entering/exiting Flash*Freeze mode

.

FIGURE 1-3: IGLOO FLASH*FREEZE MODE



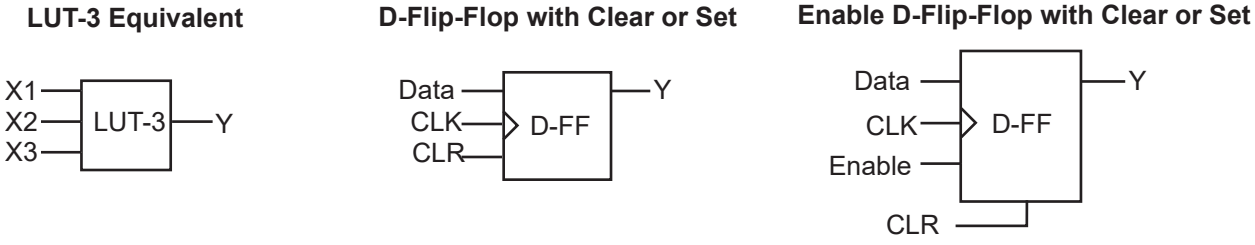
1.2.10 VERSATILES

The IGLOO core consists of VersaTiles, which have been enhanced beyond the ProASIC$^{PLUS®}$ core tiles. The IGLOO VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-4, for VersaTile configurations.

FIGURE 1-4: VERSATILE CONFIGURATIONS



1.2.11 USER NONVOLATILE FLASHROM

IGLOO devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)

- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOO IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the AGL015 and AGL030 devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Microchip development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

1.2.12 SRAM AND FIFO

IGLOO devices (except the AGL015 and AGL030 devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in the AGL015 and AGL030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

1.2.13 PLL AND CCC

IGLOO devices provide designers with very flexible clock conditioning circuit (CCC) capabilities. Each member of the IGLOO family contains six CCCs. One CCC (center west side) has a PLL. The AGL015 and AGL030 do not have a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 µs (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz/f_{OUT_CCC} (for PLL only)

1.2.13.1 Global Clocking

IGLOO devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

1.2.14 I/OS WITH ADVANCED I/O STANDARDS

The IGLOO family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2V, 1.5V, 1.8V, 2.5V, 3.0V wide range, and 3.3V). IGLOO FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported (Table 1-1).

TABLE 1-1: I/O STANDARDS SUPPORTED

I/O Bank Type	Device and Bank Location	I/O Standards Supported		
		LVTTL/ LVCMOS	PCI/PCI-X	LVPECL, LVDS, B-LVDS, M-LVDS
Advanced	East and west banks of AGL250 and larger devices	P	P	P
Standard Plus	North and south banks of AGL250 and larger devices All banks of AGL060 and AGL125K	P	P	Not supported
Standard	All banks of AGL015 and AGL030	P	Not supported	Not supported

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

IGLOO banks for the AGL250 device and above support LVPECL, LVDS, B-LVDS, and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

1.3 Wide Range I/O Support

IGLOO devices support JEDEC-defined wide range I/O operation. IGLOO devices support both the JESD8-B specification, covering 3V and 3.3V supplies, for an effective operating range of 2.7V to 3.6V, and JESD8-12 with its 1.2V nominal, supporting an effective operating range of 1.14V to 1.575V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

1.4 Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User Guide* for more information.

PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-5,).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

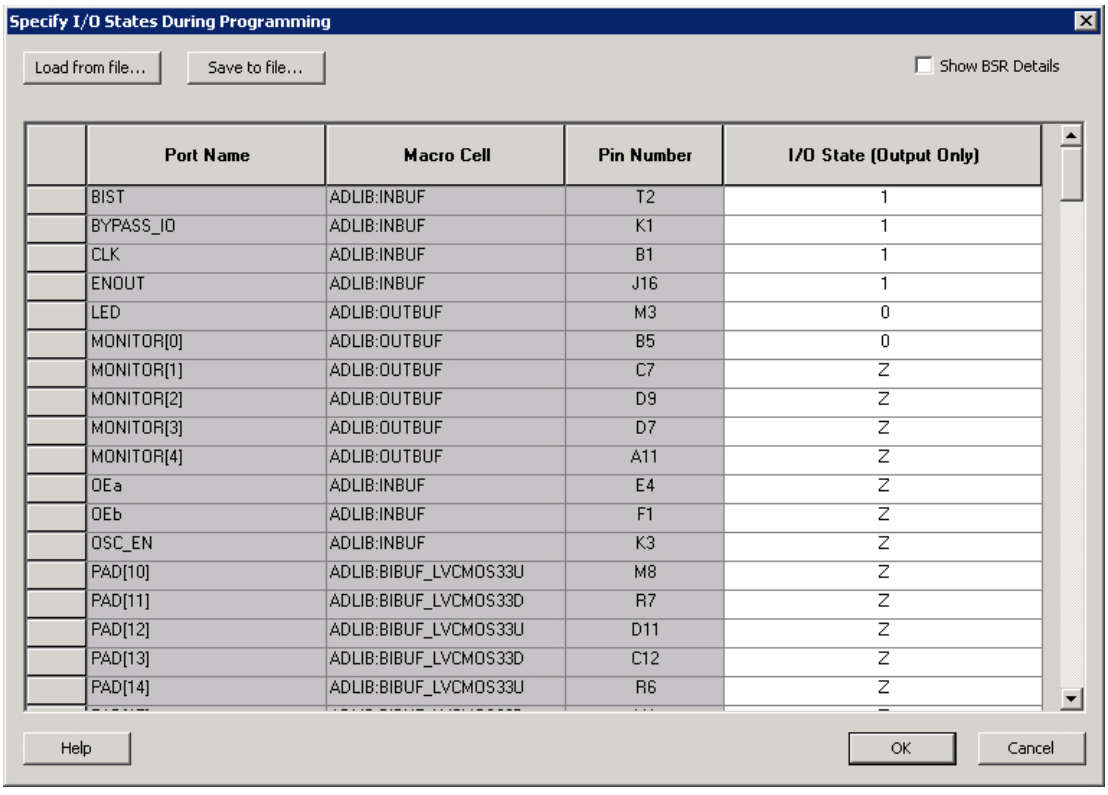
   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated

FIGURE 1-5: I/O STATES DURING PROGRAMMING WINDOW



6. Click OK to return to the FlashPoint – Programming File Generator window.

I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

2.0 IGLOO DC AND SWITCHING CHARACTERISTICS

2.1 General Specifications

2.1.1 OPERATING CONDITIONS

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Figure 2-2, is not implied.

TABLE 2-1: ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Limits[1]	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI and VMV [2]	DC I/O buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3V to 3.6V (when I/O hot insertion mode is enabled) –0.3V to (VCCI + 1V) or 3.6V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [3]	Storage Temperature	–65 to +150	°C
T_J [3]	Junction Temperature	+125	°C

Note 1: The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4.

2: VMV pins must be connected to the corresponding VCCI pins. See the "Pin Descriptions" chapter of the *IGLOO FPGA Fabric User Guide* for further information.

3: For flash programming and retention, maximum limits refer to Table 2-3, and for recommended operating limits, refer to Table 2-2.

TABLE 2-2: RECOMMENDED OPERATING CONDITIONS [1]

Symbol	Parameter		Commercial	Industrial	Units
T_J	Junction Temperature [2]		0 to +85	–40 to +100	°C
VCC[3]	1.5V DC core supply voltage[5]		1.425 to 1.575	1.425 to 1.575	V
	1.2V–1.5V wide range DC core supply voltage [4,6]		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation [7]	0 to 3.6	0 to 3.6	V
VCCPLL[8]	Analog power supply (PLL)	1.5V DC core supply voltage[5]	1.425 to 1.575	1.425 to 1.575	V
		1.2V–1.5V DC core supply voltage[4,6]	1.14 to 1.575	1.14 to 1.575	V

TABLE 2-2: RECOMMENDED OPERATING CONDITIONS [1]

Symbol	Parameter		Commercial	Industrial	Units
VCCI and VMV [9]	1.2V DC core supply voltage[6]		1.14 to 1.26	1.14 to 1.26	V
	1.2V DC wide range DC supply voltage[6]		1.14 to 1.575	1.14 to 1.575	V
	1.5V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.0V DC supply voltage [10]		2.7 to 3.6	2.7 to 3.6	V
	3.3V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Note 1: All parameters representing voltages are measured with respect to GND unless otherwise specified.

2: Software Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microchip recommends using custom settings for temperature range before running timing and power analysis tools. For more information on custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help.

3: The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Figure 2-25, . VCCI should be at the same voltage within a given I/O bank.

4: All IGLOO devices (V5 and V2) must be programmed with the VCC core voltage at 1.5V. Applications using the V2 devices powered by 1.2V supply must switch the core supply to 1.5V for in-system programming.

5: For IGLOO® V5 devices

6: For IGLOO V2 devices only, operating at VCCI ≥ VCC.

7: VPUMP can be left floating during operation (not programming mode).

8: VCCPLL pins should be tied to VCC pins. See the "Pin Descriptions" chapter of the IGLOO FPGA Fabric User Guide for further information.

9: VMV and VCCI must be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the Section 3.1.5, VMVx - I/O Supply Voltage (quiet) for further information.

10: 3.3V wide range is compliant to the JESD-8B specification and supports 3.0V VCCI operation.

TABLE 2-3: FLASH PROGRAMMING LIMITS – RETENTION, STORAGE, AND OPERATING TEMPERATURE[1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Note 1: This is a stress rating only; functional operation at any condition other than those indicated is not implied.

2: These limits apply for program/data retention only. Refer to Table 2-1 and Table 2-2 for device operating conditions and absolute limits.

TABLE 2-4: OVERSHOOT AND UNDERSHOOT LIMITS [1]

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7V or less	10%	1.4V
	5%	1.49V
3V	10%	1.1V
	5%	1.19V
3.3V	10%	0.79V
	5%	0.88V
3.6V	10%	0.45V
	5%	0.54V

Note 1: Based on reliability requirements at junction temperature at 85°C.

2: The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15V.

3: This table does not provide PCI overshoot/undershoot limits.

2.1.2 I/O POWER-UP AND SUPPLY VOLTAGE THRESHOLDS FOR POWER-ON RESET (COMMERCIAL AND INDUSTRIAL)

Sophisticated power-up management circuitry is designed into every IGLOO device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1, and Figure 2-2,.

There are five regions to consider during power-up.

IGLOO I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1, and Figure 2-2,).
2. VCCI > VCC – 0.75V (typical)
3. Chip is in the operating mode.

VCC Trip Point:

- Ramping up (V5 devices): 0.6V < trip_point_up < 1.2V
- Ramping down (V5 Devices): 0.5V < trip_point_down < 1.1V
- Ramping up (V2 devices): 0.75V < trip_point_up < 1.05V
- Ramping down (V2 devices): 0.65V < trip_point_down < 0.95V

VCC Trip Point:

- Ramping up (V5 devices): 0.6V < trip_point_up < 1.1V
- Ramping down (V5 devices): 0.5V < trip_point_down < 1.0V
- Ramping up (V2 devices): 0.65V < trip_point_up < 1.05V
- Ramping down (V2 devices): 0.55V < trip_point_down < 0.95V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

2.1.2.1 PLL Behavior at Brownout Condition

Microchip recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1, and Figure 2-2, for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75V ± 0.25V for V5 devices, and 0.75V ± 0.2V for V2 devices), the PLL output lock signal goes low and/or the output clock is lost. Refer to the Brown-out Voltage section in the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *ProASIC®3* and *ProASIC3E* FPGA fabric user guides for information on clock and lock recovery.

2.1.2.2 Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

FIGURE 2-1: V5 DEVICES – I/O STATE AS A FUNCTION OF VCCI AND VCC VOLTAGE LEVELS

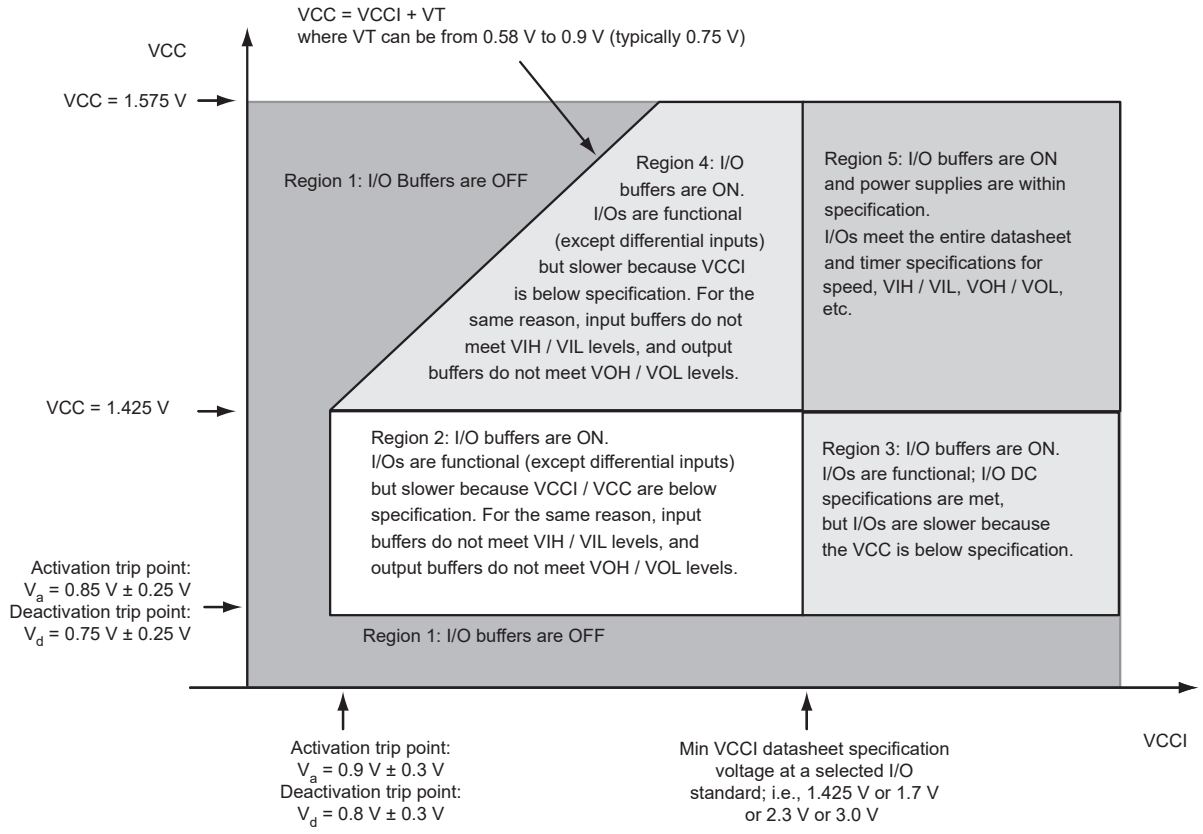
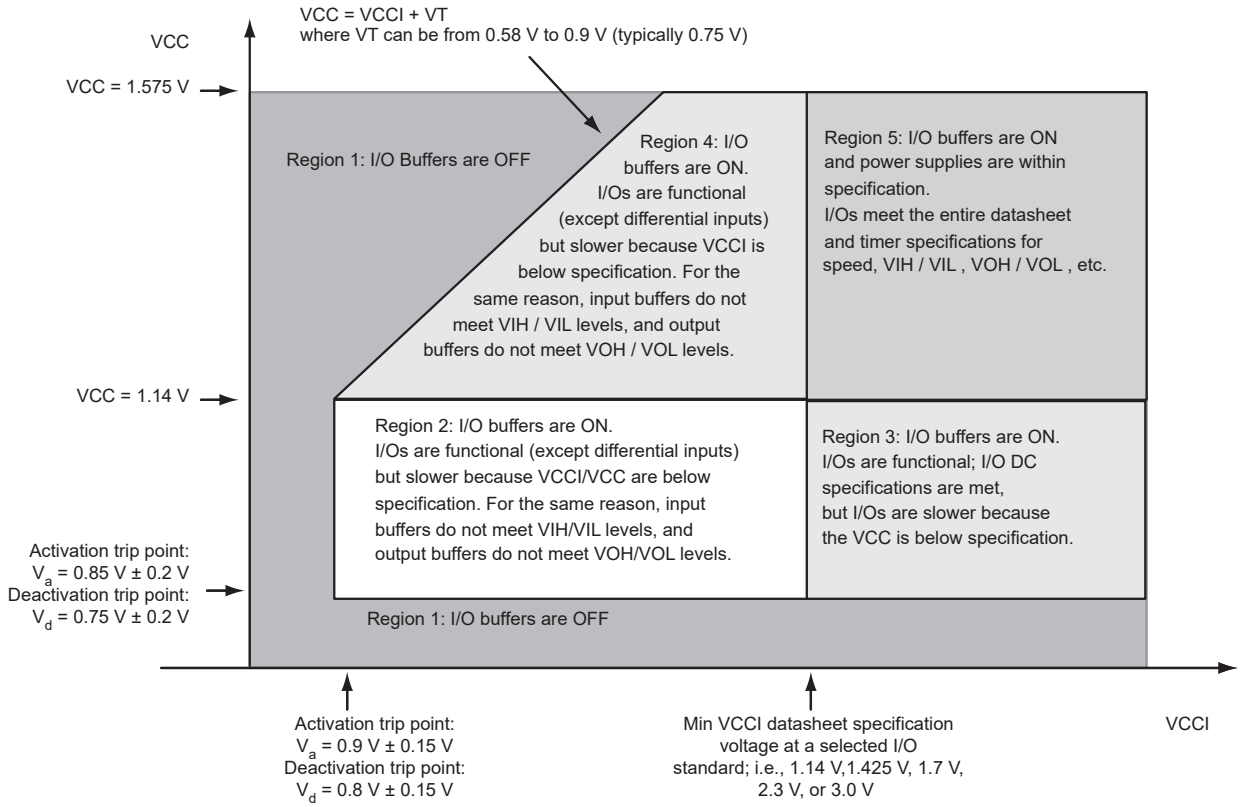


FIGURE 2-2: V2 DEVICES – I/O STATE AS A FUNCTION OF VCCI AND VCC VOLTAGE LEVELS



2.1.3 THERMAL CHARACTERISTICS

2.1.3.1 Introduction

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ can be used to calculate junction temperature.

T_J = Junction Temperature = $\Delta T + T_A$

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-5.

P = Power dissipation

2.1.3.2 Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 100°C. EQ shows a sample calculation of the absolute maximum power dissipation allowed for the AGL1000-FG484 package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{100\text{°C} - 70\text{°C}}{23.3\text{°C/W}} = 1.28\text{ W}$$

TABLE 2-5: PACKAGE THERMAL RESISTIVITIES

Package Type	Device	Pin Count	θj_c	θ_{ja}			Unit
				Still Air	1 m/s	2.5 m/s	
Quad Flat No Lead (QN)	AGL030	132	13.1	21.4	16.8	15.3	C/W
	AGL060	132	11.0	21.2	16.6	15.0	C/W
	AGL125	132	9.2	21.1	16.5	14.9	C/W
	AGL250	132	8.9	21.0	16.4	14.8	C/W
	AGL030	68	13.4	68.4	45.8	43.1	C/W
Very Thin Quad Flat Pack (VQ)*		100	10.0	35.3	29.4	27.1	C/W
Chip Scale Package (CS)	AGL1000	281	6.0	28.0	22.8	21.5	C/W
	AGL400	196	7.2	37.1	31.1	28.9	C/W
	AGL250	196	7.6	38.3	32.2	30.0	C/W
	AGL125	196	8.0	39.5	33.4	31.1	C/W
	AGL030	81	12.4	32.8	28.5	27.2	C/W
	AGL060	81	11.1	28.8	24.8	23.5	C/W
	AGL250	81	10.4	26.9	22.3	20.9	C/W
Micro Chip Scale Package (UC)	AGL030	81	16.9	40.6	35.2	33.7	C/W
Fine Pitch Ball Grid Array (FG)	AGL060	144	18.6	55.2	49.4	47.2	C/W
	AGL1000	144	6.3	31.6	26.2	24.2	C/W
	AGL400	144	6.8	37.6	31.2	29.0	C/W
	AGL250	256	12.0	38.6	34.7	33.0	C/W
	AGL1000	256	6.6	28.1	24.4	22.7	C/W
	AGL1000	484	8.0	23.3	19.0	16.7	C/W

Note: *Thermal resistances for other device-package combinations will be posted in a later revision.

2.1.3.3 Disclaimer:

The simulation for determining the junction-to-air thermal resistance is based on JEDEC standards (JESD51) and assumptions made in building the model. Junction-to-case is based on SEMI G38-88. JESD51 is only used for comparing one package to another package, provided the two tests uses the same condition. They have little relevance in actual application and therefore should be used with a degree of caution.

2.1.3.4 Temperature and Voltage Derating Factors

TABLE 2-6: TEMPERATURE AND VOLTAGE DERATING FACTORS FOR TIMING DELAYS (NORMALIZED TO T_J = 70°C, VCC = 1.425V)

For IGLOO V2 or V5 devices, 1.5V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.934	0.953	0.971	1.000	1.007	1.013
1.500	0.855	0.874	0.891	0.917	0.924	0.929
1.575	0.799	0.816	0.832	0.857	0.864	0.868

TABLE 2-7: TEMPERATURE AND VOLTAGE DERATING FACTORS FOR TIMING DELAYS (NORMALIZED TO T_J = 70°C, VCC = 1.14V)

For IGLOO V2, 1.2V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.14	0.967	0.978	0.991	1.000	1.006	1.010
1.20	0.864	0.874	0.885	0.894	0.899	0.902
1.26	0.794	0.803	0.814	0.821	0.827	0.830

2.2 Calculating Power Dissipation

2.2.1 QUIESCENT SUPPLY CURRENT

Quiescent supply current (IDD) calculation depends on multiple factors, including operating voltages (VCC, VCCI, and VJTAG), operating temperature, system clock frequency, and power modes usage. Microchip recommends using the PowerCalculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

TABLE 2-8: POWER SUPPLY STATE PER MODE

	Power Supply Configurations				
Modes/power supplies	VCC	VCCPLL	VCCI	VJTAG	VPUMP
Flash*Freeze	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
No Flash*Freeze	On	On	On	On	On/off/floating

Note: Off: Power supply level = 0V

TABLE 2-9: QUIESCENT SUPPLY CURRENT (IDD) CHARACTERISTICS, IGLOO FLASH*FREEZE MODE*

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
Typical (25°C)	1.2V	4	4	8	13	20	27	30	44	µA
	1.5V	6	6	10	18	34	51	72	127	µA

Note: *IDD includes VCC, VPUMP, VCCI, VCCPLL, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-13 through Table 2-15 and Table 2-16 through Table 2-18 (PDC6 and PDC7).

TABLE 2-10: QUIESCENT SUPPLY CURRENT (IDD) CHARACTERISTICS, IGLOO SLEEP MODE*

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
VCCI/VJTAG = 1.2V (per bank) Typical (25°C)	1.2V	1.7	1.7	1.7	1.7	1.7	1.7	1.7	1.7	µA
VCCI/VJTAG = 1.5V (per bank) Typical (25°C)	1.2V/ 1.5V	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	µA
VCCI/VJTAG = 1.8V (per bank) Typical (25°C)	1.2V/ 1.5V	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	µA

TABLE 2-10: QUIESCENT SUPPLY CURRENT (IDD) CHARACTERISTICS, IGLOO SLEEP MODE*

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
VCCI/VJTAG = 2.5V (per bank) Typical (25°C)	1.2V/ 1.5V	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	µA
VCCI/VJTAG = 3.3V (per bank) Typical (25°C)	1.2V/ 1.5V	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	µA

Note: IDD = N_{BANKS} × ICCI. Values do not include I/O static contribution, which is shown in Table 2-13 through Table 2-15 and Table 2-16 through Table 2-18 (PDC6 and PDC7).

TABLE 2-11: QUIESCENT SUPPLY CURRENT (IDD) CHARACTERISTICS, IGLOO SHUTDOWN MODE

	Core Voltage	AGL015	AGL030	Units
Typical (25°C)	1.2V/1.5V	0	0	µA

TABLE 2-12: QUIESCENT SUPPLY CURRENT (IDD), NO IGLOO FLASH*FREEZE MODE[1]

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
ICCA Current[2]										
Typical (25°C)	1.2V	5	6	10	13	18	25	28	42	µA
	1.5V	14	16	20	28	44	66	82	137	µA
ICCI or IJTAG Current[3]										
VCCI/VJTAG = 1.2V (per bank) Typical (25°C)	1.2V	1.7	1.7	1.7	1.7	1.7	1.7	1.7	1.7	µA
VCCI/VJTAG = 1.5V (per bank) Typical (25°C)	1.2V/ 1.5V	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	µA
VCCI/VJTAG = 1.8V (per bank) Typical (25°C)	1.2V/ 1.5V	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	µA
VCCI/VJTAG = 2.5V (per bank) Typical (25°C)	1.2V/ 1.5V	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	µA
VCCI/VJTAG = 3.3V (per bank) Typical (25°C)	1.2V/ 1.5V	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	µA

Note 1: IDD = N_{BANKS} × ICCI + ICCA. JTAG counts as one bank when powered.

2: Includes VCC, VPUMP, and VCCPLL currents.

3: Values do not include I/O static contribution (PDC6 and PDC7).

2.2.2 POWER PER I/O PIN

TABLE 2-13: SUMMARY OF I/O INPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS

Applicable to Advanced I/O Banks

	VCCI (V)	Static Power PDC6 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3V LVTTL/3.3V LVCMOS	3.3	——	16.27
3.3V LVCMOS Wide Range[3]	3.3	—	16.27
2.5V LVCMOS	2.5	—	4.65
1.8V LVCMOS	1.8	—	1.61
1.5V LVCMOS (JESD8-11)	1.5	—	0.96
1.2V LVCMOS[4]	1.2	—	0.58
1.2V LVCMOS Wide Range[4]	1.2	—	0.58
3.3V PCI	3.3	—	17.67
3.3V PCI-X	3.3	—	17.67
Differential			
LVDS	2.5	2.26	23.39
LVPECL	3.3	5.72	59.05

Note 1: P_{DC6} is the static power (where applicable) measured on VCCI.

2: P_{AC9} is the total dynamic power measured on VCCI.

3: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

4: Applicable for IGLOO V2 devices only

TABLE 2-14: SUMMARY OF I/O INPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS

Applicable to Standard Plus I/O Banks

	VCCI (V)	Static Power PDC6 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3V LVTTL/3.3V LVCMOS	3.3	—	16.41
3.3V LVCMOS Wide Range[3]	3.3	—	16.41
2.5V LVCMOS	2.5	—	4.75
1.8V LVCMOS	1.8	—	1.66
1.5V LVCMOS (JESD8-11)	1.5	—	1.00
1.2V LVCMOS[4]	1.2	—	0.61
1.2V LVCMOS Wide Range[4]	1.2	—	0.61
3.3V PCI	3.3	—	17.78
3.3V PCI-X	3.3	—	17.78

Note 1: PDC6 is the static power (where applicable) measured on VCCI.

2: PAC9 is the total dynamic power measured on VCCI.

3: Applicable for IGLOO V2 devices only.

4: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

TABLE 2-15: SUMMARY OF I/O INPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS

Applicable to Standard I/O Banks

	VCCI (V)	Static Power PDC6 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3V LVTTL/3.3V LVCMOS	3.3	—	17.24
3.3V LVCMOS Wide Range[3]	3.3	—	17.24
2.5V LVCMOS	2.5	—	5.64
1.8V LVCMOS	1.8	—	2.63
1.5V LVCMOS (JESD8-11)	1.5	—	1.97
1.2V LVCMOS[4]	1.2	—	0.57
1.2V LVCMOS Wide Range[4]	1.2	—	0.57

Note 1: PDC6 is the static power (where applicable) measured on VCCI.

2: PAC9 is the total dynamic power measured on VCCI.

3: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

4: Applicable for IGLOO V2 devices only.

TABLE 2-16: SUMMARY OF I/O OUTPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS[1]

Applicable to Advanced I/O Banks

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3V LVTTL/3.3V LVCMOS	5	3.3	—	136.95
3.3V LVCMOS Wide Range[4]	5	3.3	—	136.95
2.5V LVCMOS	5	2.5	—	76.84
1.8V LVCMOS	5	1.8	—	49.31
1.5V LVCMOS (JESD8-11)	5	1.5	—	33.36
1.2V LVCMOS[5]	5	1.2	—	16.24
1.2V LVCMOS Wide Range[5]	5	1.2	—	16.24
3.3V PCI	10	3.3	—	194.05
3.3V PCI-X	10	3.3	—	194.05
Differential				
LVDS	—	2.5	7.74	156.22
LVPECL	—	3.3	19.54	339.35

Note 1: Dynamic power consumption is given for standard load and software default drive strength and output slew.

2: PDC7 is the static power (where applicable) measured on VCCI.

3: PAC10 is the total dynamic power measured on VCCI.

4: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

5: Applicable for IGLOO V2 devices only.

TABLE 2-17: SUMMARY OF I/O OUTPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS[1]

Applicable to Standard Plus I/O Banks

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3V LVTTL/3.3V LVCMOS	5	3.3	—	122.16
3.3V LVCMOS Wide Range[4]	5	3.3	—	122.16
2.5V LVCMOS	5	2.5	—	68.37
1.8V LVCMOS	5	1.8	—	34.53
1.5V LVCMOS (JESD8-11)	5	1.5	—	23.66
1.2V LVCMOS[5]	5	1.2	—	14.90
1.2V LVCMOS Wide Range[5]	5	1.2	—	14.90
3.3V PCI	10	3.3	—	181.06
3.3V PCI-X	10	3.3	—	181.06

Note 1: Dynamic power consumption is given for standard load and software default drive strength and output slew.

2: P_{DC7} is the static power (where applicable) measured on VCCI.

3: P_{AC10} is the total dynamic power measured on VCCI.

4: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

5: Applicable for IGLOO V2 devices only.

TABLE 2-18: SUMMARY OF I/O OUTPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS[1] APPLICABLE TO STANDARD I/O BANKS

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3V LVTTL/3.3V LVCMOS	5	3.3	—	104.38
3.3V LVCMOS Wide Range[4]	5	3.3	—	104.38
2.5V LVCMOS	5	2.5	—	59.86
1.8V LVCMOS	5	1.8	—	31.26
1.5V LVCMOS (JESD8-11)	5	1.5	—	21.96
1.2V LVCMOS[5]	5	1.2	—	13.49
1.2V LVCMOS Wide Range[5]	5	1.2	—	13.49

Note 1: Dynamic power consumption is given for standard load and software default drive strength and output slew.

2: PDC7 is the static power (where applicable) measured on VCCI.

3: PAC10 is the total dynamic power measured on VCCI.

4: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

5: Applicable for IGLOO V2 devices only.

2.2.3 POWER CONSUMPTION OF VARIOUS INTERNAL RESOURCES

TABLE 2-19: DIFFERENT COMPONENTS CONTRIBUTING TO DYNAMIC POWER CONSUMPTION IN IGLOO DEVICES FOR IGLOO V2 OR V5 DEVICES, 1.5V DC CORE SUPPLY VOLTAGE

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)							
		AGL1000	AGL600	AGL400	AGL250	AGL125	AGL060	AGL030	AGL015
PAC1	Clock contribution of a Global Rib	7.778	6.221	6.082	4.460	4.446	2.736	0.000	0.000
PAC2	Clock contribution of a Global Spine	4.334	3.512	2.759	2.718	1.753	1.971	3.483	3.483
PAC3	Clock contribution of a VersaTile row	1.379	1.445	1.377	1.483	1.467	1.503	1.472	1.472
PAC4	Clock contribution of a VersaTile used as a sequential module	0.151	0.149	0.151	0.149	0.149	0.151	0.146	0.146
PAC5	First contribution of a VersaTile used as a sequential module	0.057							
PAC6	Second contribution of a VersaTile used as a sequential module	0.207							
PAC7	Contribution of a VersaTile used as a combinatorial module	0.276	0.262	0.279	0.277	0.280	0.300	0.281	0.273
PAC8	Average contribution of a routing net	1.161	1.147	1.193	1.273	1.076	1.088	1.134	1.153
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13 through Table 2-15.							
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-16 through Table 2-18.							
PAC11	Average contribution of a RAM block during a read operation	25.00							
PAC12	Average contribution of a RAM block during a write operation	30.00							
PAC13	Dynamic PLL contribution	2.70							

Note: For a different output load, drive strength, or slew rate, Microchip recommends using the Microchip power spreadsheet calculator or SmartPower tool in Libero SoC.

TABLE 2-20: DIFFERENT COMPONENTS CONTRIBUTING TO THE STATIC POWER CONSUMPTION IN IGLOO DEVICES FOR IGLOO V2 OR V5 DEVICES, 1.5V DC CORE SUPPLY VOLTAGE

Parameter	Definition	Device-Specific Static Power (mW)							
		AGL1000	AGL600	AGL400	AGL250	AGL125	AGL060	AGL030	AGL015
PDC1	Array static power in Active mode	See Table 2-12.							
PDC2	Array static power in Static (Idle) mode	See Table 2-11.							
PDC3	Array static power in Flash*Freeze mode	See Table 2-9.							
PDC4	Static PLL contribution	1.84							
PDC5	Bank quiescent power (V_{CCI}-dependent)	See Table 2-12.							
PDC6	I/O input pin static power (standard-dependent)	See Table 2-13 through Table 2-15.							
PDC7	I/O output pin static power (standard-dependent)	See Table 2-16 through Table 2-18.							

Note: *For a different output load, drive strength, or slew rate, Microchip recommends using the Microchip power spreadsheet calculator or SmartPower tool in Libero SoC.

TABLE 2-21: DIFFERENT COMPONENTS CONTRIBUTING TO DYNAMIC POWER CONSUMPTION IN IGLOO DEVICES FOR IGLOO V2 DEVICES, 1.2V DC CORE SUPPLY VOLTAGE

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)							
		AGL1000	AGL600	AGL400	AGL250	AGL125	AGL060	AGL030	AGL015
PAC1	Clock contribution of a Global Rib	4.978	3.982	3.892	2.854	2.845	1.751	0.000	0.000
PAC2	Clock contribution of a Global Spine	2.773	2.248	1.765	1.740	1.122	1.261	2.229	2.229
PAC3	Clock contribution of a VersaTile row	0.883	0.924	0.881	0.949	0.939	0.962	0.942	0.942
PAC4	Clock contribution of a VersaTile used as a sequential module	0.096	0.095	0.096	0.095	0.095	0.096	0.094	0.094
PAC5	First contribution of a VersaTile used as a sequential module	0.045							
PAC6	Second contribution of a VersaTile used as a sequential module	0.186							
PAC7	Contribution of a VersaTile used as a combinatorial module	0.158	0.149	0.158	0.157	0.160	0.170	0.160	0.155
PAC8	Average contribution of a routing net	0.756	0.729	0.753	0.817	0.678	0.692	0.738	0.721
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13 through Table 2-15.							

TABLE 2-21: DIFFERENT COMPONENTS CONTRIBUTING TO DYNAMIC POWER CONSUMPTION IN IGLOO DEVICES FOR IGLOO V2 DEVICES, 1.2V DC CORE SUPPLY VOLTAGE

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)							
		AGL1000	AGL600	AGL400	AGL250	AGL125	AGL060	AGL030	AGL015
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-16 through Table 2-18.							
PAC11	Average contribution of a RAM block during a read operation	25.00							
PAC12	Average contribution of a RAM block during a write operation	30.00							
PAC13	Dynamic PLL contribution	2.10							

Note: For a different output load, drive strength, or slew rate, Microchip recommends using the Microchip power spreadsheet calculator or SmartPower tool in Libero SoC.

TABLE 2-22: DIFFERENT COMPONENTS CONTRIBUTING TO THE STATIC POWER CONSUMPTION IN IGLOO DEVICE FOR IGLOO V2 DEVICES, 1.2V DC CORE SUPPLY VOLTAGE

Parameter	Definition	Device Specific Static Power (mW)							
		AGL1000	AGL600	AGL400	AGL250	AGL125	AGL060	AGL030	AGL015
PDC1	Array static power in Active mode	See Table 2-12.							
PDC2	Array static power in Static (Idle) mode	See Table 2-11.							
PDC3	Array static power in Flash*Freeze mode	See Table 2-9.							
PDC4	Static PLL contribution	0.90							
PDC5	Bank quiescent power (VCCI-Dependent)	See Table 2-12.							
PDC6	I/O input pin static power (standard-dependent)	See Table 2-13 through Table 2-15.							
PDC7	I/O output pin static power (standard-dependent)	See Table 2-16 through Table 2-18.							

Note: For a different output load, drive strength, or slew rate, Microchip recommends using the Microchip power spreadsheet calculator or SmartPower tool in Libero SoC.

2.3 Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Microchip Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design

- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-23.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-24.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-24. The calculation should be repeated for each clock domain defined in the design.

2.3.1 METHODOLOGY

2.3.1.1 Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

2.3.1.2 Total Static Power Consumption—P_{STAT}

$P_{STAT} = (P_{DC1}$ or P_{DC2} or $P_{DC3}) + N_{BANKS} * P_{DC5} + N_{INPUTS} * P_{DC6} + N_{OUTPUTS} * P_{DC7}$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{BANKS} is the number of I/O banks powered in the design.

2.3.1.3 Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

2.3.1.4 Global Clock Contribution—P_{CLOCK}

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the *IGLOO FPGA Fabric User Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the *IGLOO FPGA Fabric User Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

P_{AC1}, P_{AC2}, P_{AC3}, and P_{AC4} are device-dependent.

2.3.1.5 Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23.

F_{CLK} is the global clock signal frequency.

2.3.1.6 Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23.

F_{CLK} is the global clock signal frequency.

2.3.1.7 Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23.

F_{CLK} is the global clock signal frequency.

2.3.1.8 I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-23.

F_{CLK} is the global clock signal frequency.

2.3.1.9 I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-23.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-24.

F_{CLK} is the global clock signal frequency.

2.3.1.10 RAM Contribution—P_{MEMORY}

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-24.

2.3.1.11 PLL Contribution—P_{PLL}

$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.[4]

2.3.2 GUIDELINES

2.3.2.1 Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
- Bit 0 (LSB) = 100%
- Bit 1 = 50%
- Bit 2 = 25%
- …
- Bit 7 (MSB) = 0.78125%
- Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

2.3.2.2 Enable Rate Definition

4. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

TABLE 2-23: TOGGLE RATE GUIDELINES RECOMMENDED FOR POWER CALCULATION

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

TABLE 2-24: ENABLE RATE GUIDELINES RECOMMENDED FOR POWER CALCULATION

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

2.4 User I/O Characteristics

2.4.1 TIMING MODEL

FIGURE 2-3: TIMING MODEL OPERATING CONDITIONS: STD. SPEED, COMMERCIAL TEMPERATURE RANGE (T_J = 70°C), WORST-CASE VCC = 1.425V, FOR DC 1.5V CORE VOLTAGE, APPLICABLE TO V2 AND V5 DEVICES

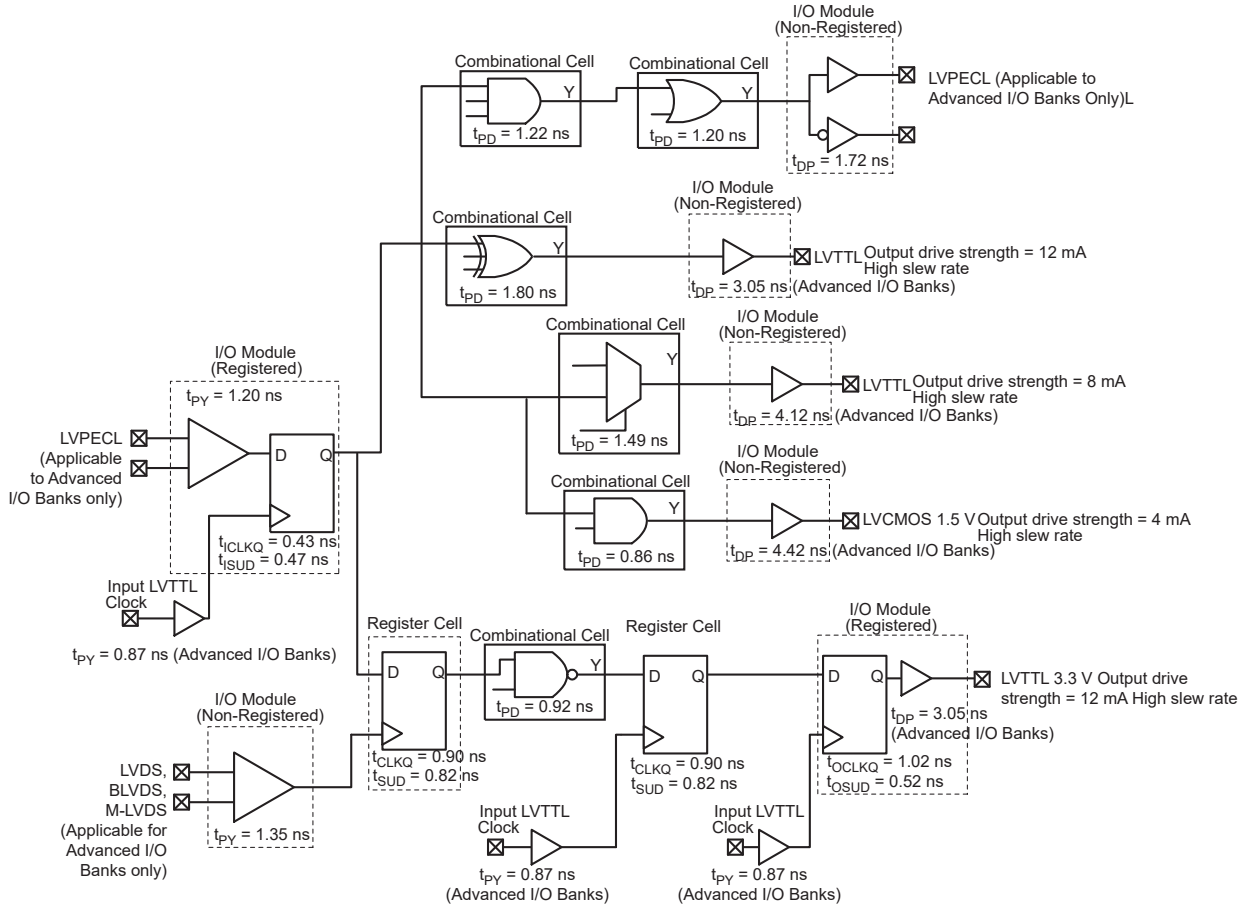
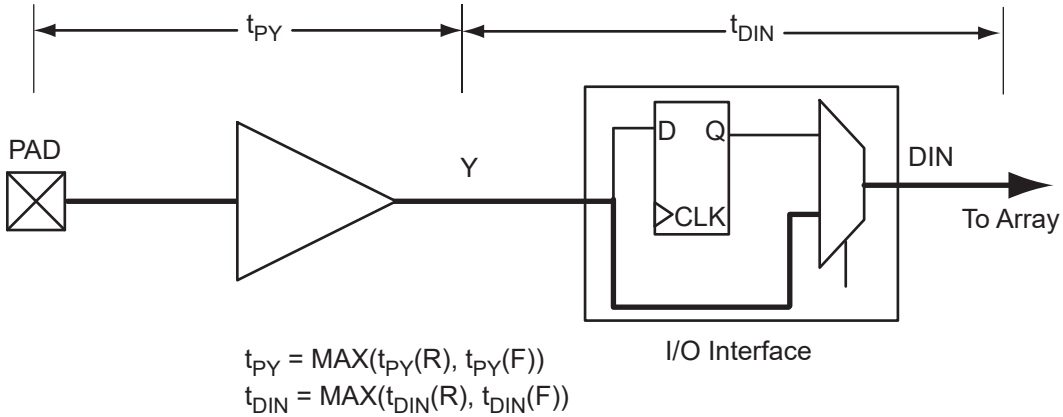


FIGURE 2-4: INPUT BUFFER TIMING MODEL AND DELAYS (EXAMPLE)



$t_{PY} = MAX(t_{PY}(R), t_{PY}(F))$
$t_{DIN} = MAX(t_{DIN}(R), t_{DIN}(F))$

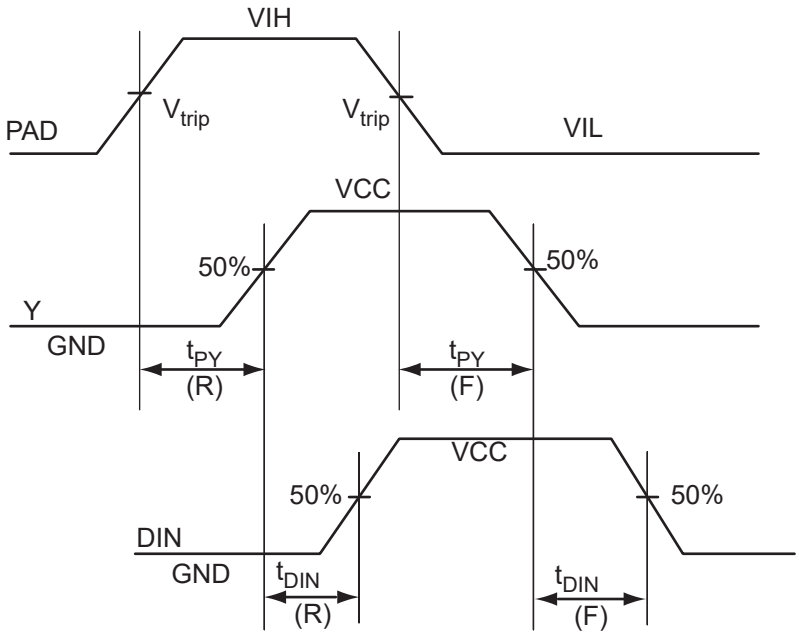


FIGURE 2-5: OUTPUT BUFFER MODEL AND DELAYS (EXAMPLE)

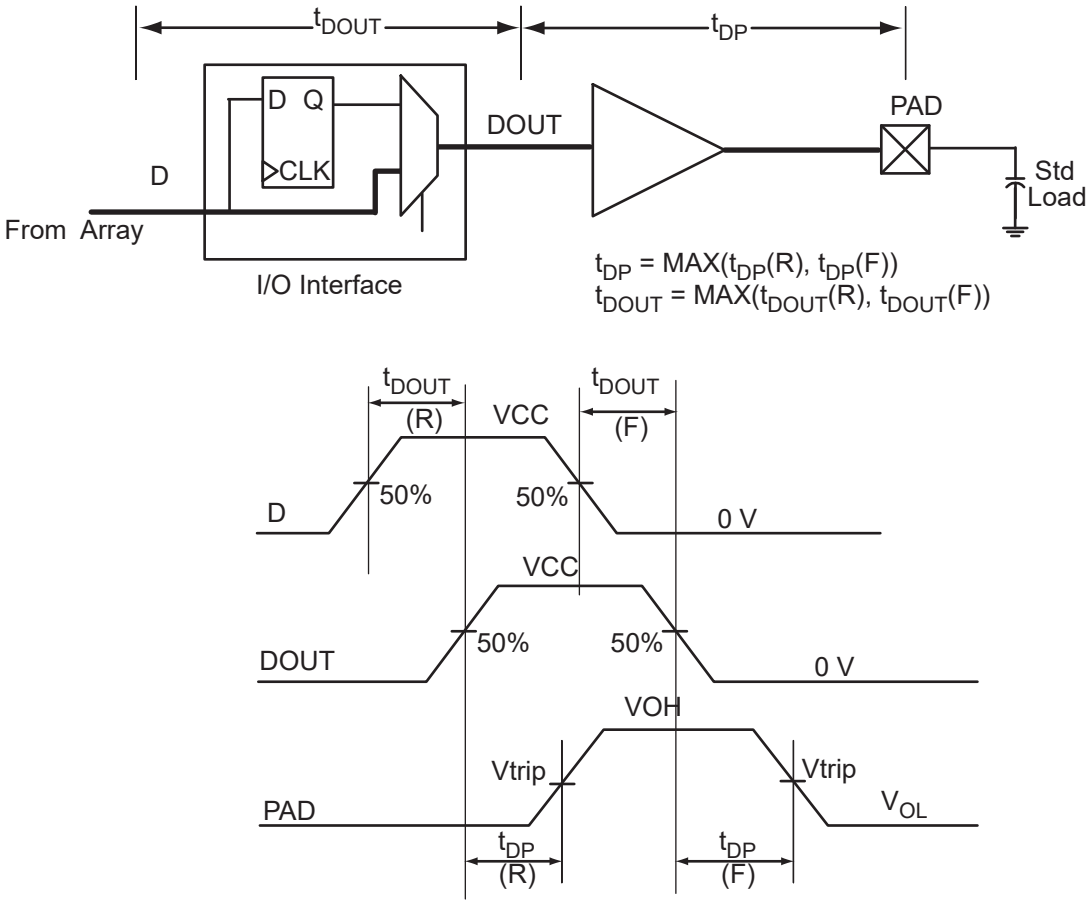
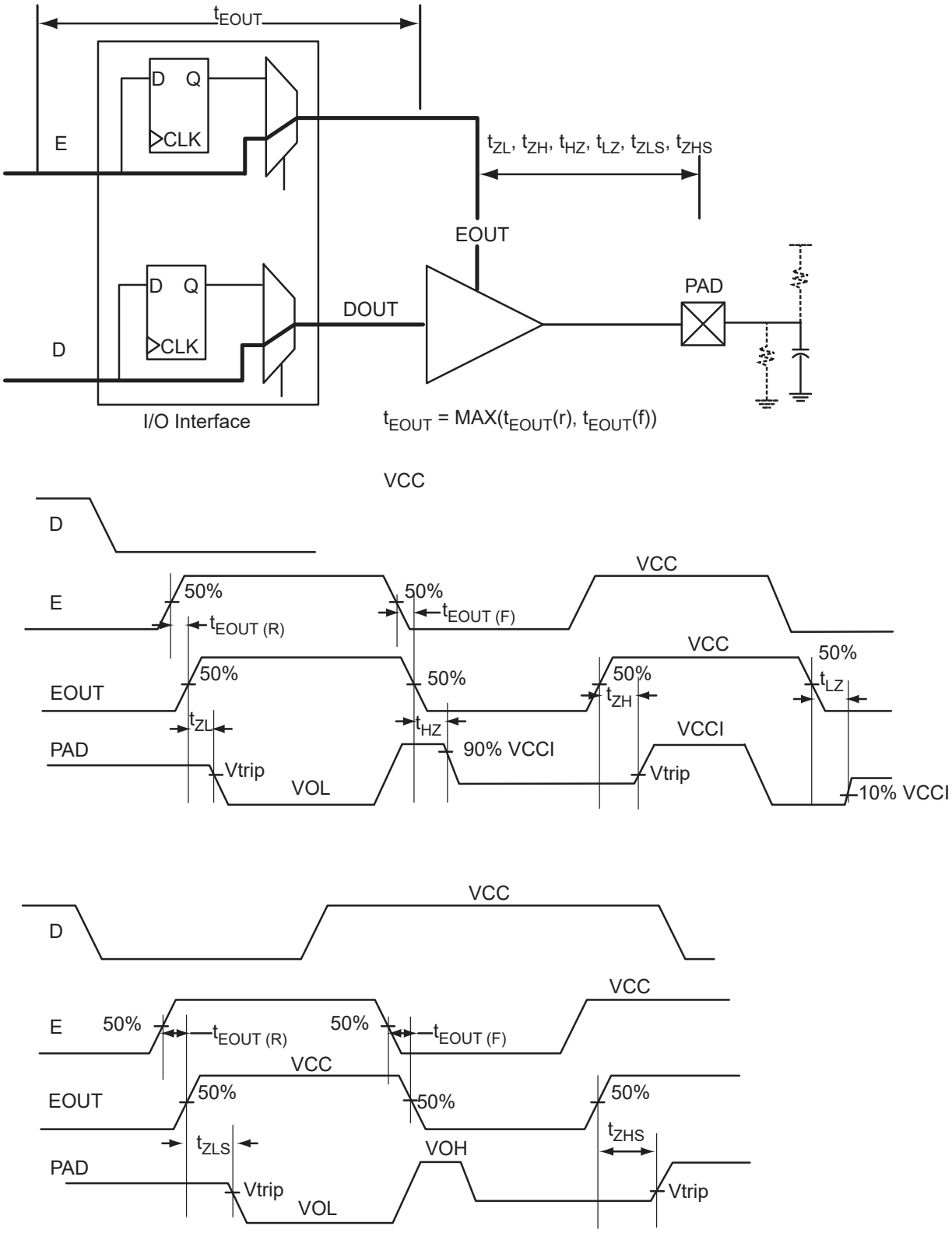


FIGURE 2-6: TRISTATE OUTPUT BUFFER TIMING MODEL AND DELAYS (EXAMPLE)



2.4.2 OVERVIEW OF I/O PERFORMANCE

2.4.3 SUMMARY OF I/O DC INPUT AND OUTPUT LEVELS – DEFAULT I/O SOFTWARE SETTINGS

TABLE 2-25: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS—SOFTWARE DEFAULT SETTINGS APPLICABLE TO ADVANCED I/O BANKS

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[2]	Slew Rate	VIL		VIH		VOL	VOH	IOL[1]	IOH[1]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3V LVTTL / 3.3V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3V LVCMOS Wide Range[3]	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	0.1	0.1
2.5V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8V LVCMOS	12 mA	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12
1.5V LVCMOS	12 mA	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12
1.2V LVC-MOS[4]	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2
1.2V LVCMOS Wide Range[4,5]	100 µA	2 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	1.575	0.1	VCCI – 0.1	0.1	0.1
3.3V PCI	Per PCI specifications										
3.3V PCI-X	Per PCI-X specifications										

Note 1: Currents are measured at 85°C junction temperature.

2: The minimum drive strength for any LVCMOS 1.2V or LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

3: All LVMCOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

4: Applicable to V2 Devices operating at VCCI ≥ VCC.

5: All LVCMOS 1.2V software macros support LVCMOS 1.2V wide range as specified in the JESD8-12 specification.

TABLE 2-26: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS—SOFTWARE DEFAULT SETTINGS

Applicable to Standard Plus I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[2]	Slew Rate	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3V LVTTL / 3.3V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3V LVCMOS Wide Range[3]	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VDD-0.2	0.1	0.1
2.5V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8V LVCMOS	8 mA	8 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8
1.5V LVCMOS	4 mA	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4
1.2V LVC-MOS[4]	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2
1.2V LVCMOS Wide Range[4]	100 µA	2 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	1.575	0.1	VCCI – 0.1	0.1	0.1
3.3V PCI	Per PCI specifications										
3.3V PCI-X	Per PCI-X specifications										

Note 1: Currents are measured at 85°C junction temperature.

2: The minimum drive strength for any LVCMOS 1.2V or LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

3: All LVMCOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

4: Applicable to V2 Devices operating at VCCI ≥ VCC.

5: All LVCMOS 1.2V software macros support LVCMOS 1.2V wide range as specified in the JESD8-12 specification.

TABLE 2-27: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS—SOFTWARE DEFAULT SETTINGS APPLICABLE TO STANDARD I/O BANKS

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[2]	Slew Rate	VIL		V_{IH}		VOL	V_{OH}	I_{OL}[1]	I_{OH}[1]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3V LVTTL / 3.3V LVCMOS	8 mA	8 mA	High	–0.3	0.8	2	3.6	0.4	2.4	8	8
3.3V LVCMOS Wide Range[3]	100 µA	8 mA	High	–0.3	0.8	2	3.6	0.2	VDD-0.2	0.1	0.1
2.5V LVCMOS	8 mA	8 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8V LVCMOS	4 mA	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4
1.5V LVCMOS	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2
1.2V LVCMOS[4]	1 mA	1 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	1	1
1.2V LVCMOS Wide Range[4,5]	100 µA	1 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI – 0.1	0.1	0.1

Note 1: Currents are measured at 85°C junction temperature.

2: The minimum drive strength for any LVCMOS 1.2V or LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

3: All LVMCOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

4: Applicable to V2 Devices operating at VCCI ≥ VCC.

5: All LVCMOS 1.2V software macros support LVCMOS 1.2V wide range as specified in the JESD8-12 specification.

TABLE 2-28: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT LEVELS APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS

DC I/O Standards	Commercial[1]		Industrial[2]	
	IIL[4]	IIH[5]	IIL[4]	IIH[5]
	µA	µA	µA	µA
3.3V LVTTL/3.3V LVCMOS	10	10	15	15
3.3V LVCMOS Wide Range	10	10	15	15
2.5V LVCMOS	10	10	15	15
1.8V LVCMOS	10	10	15	15
1.5V LVCMOS	10	10	15	15
1.2V LVCMOS[3]	10	10	15	15
1.2V LVCMOS Wide Range[3]	10	10	15	15
3.3V PCI	10	10	15	15
3.3V PCI-X	10	10	15	15

Note 1: Commercial range (0°C < T_A < 70°C)

2: Industrial range (–40°C < T_A < 85°C)

3: Applicable to V2 Devices operating at VCCI ≥ VCC.

4: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

5: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

2.4.4 SUMMARY OF I/O TIMING CHARACTERISTICS – DEFAULT I/O SOFTWARE SETTINGS

TABLE 2-29: SUMMARY OF AC MEASURING POINTS

Standard	Measuring Trip Point (Vtrip)
3.3V LVTTL/3.3V LVCMOS	1.4V
3.3V VCMOS Wide Range	1.4V
2.5V LVCMOS	1.2V
1.8V LVCMOS	0.90V
1.5V LVCMOS	0.75V
1.2V LVCMOS	0.60V
1.2V LVCMOS Wide Range	0.60V
3.3V PCI	0.285 * VCCI (RR)
	0.615 * VCCI (FF)
3.3V PCI-X	0.285 * VCCI (RR)
	0.615 * VCCI (FF)

TABLE 2-30: I/O AC PARAMETER DEFINITIONS

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z

TABLE 2-30: I/O AC PARAMETER DEFINITIONS

Parameter	Parameter Definition
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

TABLE 2-31: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS, STD. SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI (PER STANDARD) APPLICABLE TO ADVANCED I/O BANKS

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1] (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3V LVTTL / 3.3V LVCMOS	12 mA	12	High	5	— —	0.97	2.09	0.18	0.85	0.66	2.14	1.68	2.67	3.05	5.73	5.27	ns
3.3V LVCMOS Wide Range[2]	100 µA	12	High	5	—	0.97	2.93	0.18	1.19	0.66	2.95	2.27	3.81	4.30	6.54	5.87	ns
2.5V LVCMOS	12 mA	12	High	5	—	0.97	2.09	0.18	1.08	0.66	2.14	1.83	2.73	2.93	5.73	5.43	ns
1.8V LVCMOS	12 mA	12	High	5	—	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns
1.5V LVCMOS	12 mA	12	High	5	—	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns
3.3V PCI	Per PCI spec	—	High	10	25 [2]	0.97	2.32	0.18	0.74	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns
3.3V PCI-X	Per PCI-X spec	—	High	10	25 [2]	0.97	2.32	0.19	0.70	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns
LVDS	24 mA	—	High	—	—	0.97	1.74	0.19	1.35	—	—	—	—	—	—	—	ns
LVPECL	24 mA	—	High	—	—	0.97	1.68	0.19	1.16	—	—	—	—	—	—	—	ns

TABLE 2-31: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS, STD. SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI (PER STANDARD) APPLICABLE TO ADVANCED I/O BANKS

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1] (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

3: Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12, for connectivity. This resistor is not required during normal operation.

4: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-32: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS, STD. SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI (PER STANDARD) APPLICABLE TO STANDARD PLUS I/O BANKS

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1] (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3V LVTTL / 3.3V LVCMOS	12 mA	12	High	5	—	0.97	1.75	0.18	0.85	0.66	1.79	1.40	2.36	2.79	5.38	4.99	ns
3.3V LVCMOS Wide Range[2]	100 µA	12	High	5	—	0.97	2.45	0.18	1.20	0.66	2.47	1.92	3.33	3.90	6.06	5.51	ns
2.5V LVCMOS	12 mA	12	High	5	—	0.97	1.75	0.18	1.08	0.66	1.79	1.52	2.38	2.70	5.39	5.11	ns
1.8V LVCMOS	8 mA	8	High	5	—	0.97	1.97	0.18	1.01	0.66	2.02	1.76	2.46	2.66	5.61	5.36	ns
1.5V LVCMOS	4 mA	4	High	5	—	0.97	2.25	0.18	1.18	0.66	2.30	2.00	2.53	2.68	5.89	5.59	ns

TABLE 2-32: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS, STD. SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI (PER STANDARD) APPLICABLE TO STANDARD PLUS I/O BANKS

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1] (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3V PCI	Per PCI spec	—	High	10	25[2]	0.97	1.97	0.18	0.73	0.66	2.01	1.50	2.36	2.79	5.61	5.10	ns
3.3V PCI-X	Per PCI-X spec	—	High	10	25[2]	0.97	1.97	0.19	0.70	0.66	2.01	1.50	2.36	2.79	5.61	5.10	ns

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

3: Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12, for connectivity. This resistor is not required during normal operation.

4: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-33: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS, STD. SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI (PER STANDARD) APPLICABLE TO STANDARD I/O BANKS

I/O Standard	Drive Strength)	Equivalent Software Default Drive Strength Option[1] (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3V LVTTL / 3.3V LVCMOS	8 mA	8	High	5	—	0.97	1.85	0.18	0.83	0.66	1.89	1.46	1.96	2.26	ns
3.3V LVCMOS Wide Range[2]	100 µA	8	High	5	—	0.97	2.62	0.18	1.17	0.66	2.63	2.02	2.79	3.17	ns

TABLE 2-33: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS, STD. SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI (PER STANDARD) APPLICABLE TO STANDARD I/O BANKS

I/O Standard	Drive Strength)	Equivalent Software Default Drive Strength Option[1] (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
2.5V LVCMOS	8 mA	8	High	5	—	0.97	1.88	0.18	1.04	0.66	1.92	1.63	1.95	2.15	ns
1.8V LVCMOS	4 mA	4	High	5	—	0.97	2.18	0.18	0.98	0.66	2.22	1.93	1.97	2.06	ns
1.5V LVCMOS	2 mA	2	High	5	—	0.97	2.51	0.18	1.14	0.66	2.56	2.21	1.99	2.03	ns

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-34: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS, STD. SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI (PER STANDARD)

Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3V LVTTL / 3.3V LVCMOS	12 mA	12 mA	High	5	—	1.55	2.67	0.26	0.98	1.10	2.71	2.18	3.25	3.93	8.50	7.97	ns
3.3V LVC-MOS Wide Range[2]	100 µA	12 mA	High	5	—	1.55	3.73	0.26	1.32	1.10	3.73	2.91	4.51	5.43	9.52	8.69	ns
2.5V LVCMOS	12 mA	12 mA	High	5	—	1.55	2.64	0.26	1.20	1.10	2.67	2.29	3.30	3.79	8.46	8.08	ns

TABLE 2-34: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS, STD. SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI (PER STANDARD)

Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
1.8V LVCMOS	12 mA	12 mA	High	5	—	1.55	2.72	0.26	1.11	1.10	2.76	2.43	3.58	4.19	8.55	8.22	ns
1.5V LVCMOS	12 mA	12 mA	High	5	—	1.55	2.96	0.26	1.27	1.10	3.00	2.70	3.75	4.23	8.78	8.48	ns
1.2V LVCMOS	2 mA	2 mA	High	5	—	1.55	3.60	0.26	1.60	1.10	3.47	3.36	3.93	3.65	9.26	9.14	ns
1.2V LVC-MOS Wide Range[3]	100 µA	2 mA	High	5	—	1.55	3.60	0.26	1.60	1.10	3.47	3.36	3.93	3.65	9.26	9.14	ns
3.3V PCI	Per PCI spec	—	High	10	25[2]	1.55	2.91	0.26	0.86	1.10	2.95	2.29	3.25	3.93	8.74	8.08	ns
3.3V PCI-X	Per PCI-X spec	—	High	10	25[2]	1.55	2.91	0.25	0.86	1.10	2.95	2.29	3.25	3.93	8.74	8.08	ns
LVDS	24 mA	—	High	—	—	1.55	2.27	0.25	1.57	—	—	—	—	—	—	—	ns
LVPECL	24 mA	—	High	—	—	1.55	2.24	0.25	1.38	—	—	—	—	—	—	—	ns

Note 1: The minimum drive strength for any LVCMOS 1.2V or LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

3: All LVCMOS 1.2V software macros support LVCMOS 1.2V wide range as specified in the JESD8-12 specification

4: Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12, for connectivity. This resistor is not required during normal operation.

5: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-35: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS, STD. SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI (PER STANDARD) APPLICABLE TO STANDARD PLUS I/O BANKS

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1] (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3V LVTTL / 3.3V LVCMOS	12 mA	12	High	5	—	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns
3.3V LVCMOS Wide Range[2]	100 µA	12	High	5	—	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns
2.5V LVCMOS	12 mA	12	High	5	—	1.55	2.29	0.26	1.19	1.10	2.32	1.94	2.94	3.52	8.10	7.73	ns
1.8V LVCMOS	8 mA	8	High	5	—	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns
1.5V LVCMOS	4 mA	4	High	5	—	1.55	2.68	0.26	1.27	1.10	2.72	2.39	3.07	3.37	8.50	8.18	ns
1.2V LVCMOS	2 mA	2	High	5	—	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns
1.2V LVCMOS Wide Range[3]	100 µA	2	High	5	—	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns
3.3V PCI	Per PCI spec	—	High	10	25[2]	1.55	2.53	0.26	0.84	1.10	2.57	1.98	2.93	3.64	8.35	7.76	ns
3.3V PCI-X	Per PCI-X spec	—	High	10	25[2]	1.55	2.53	0.25	0.85	1.10	2.57	1.98	2.93	3.64	8.35	7.76	ns

Note 1: The minimum drive strength for any LVCMOS 1.2V or LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

3: All LVCMOS 1.2V software macros support LVCMOS 1.2V wide range as specified in the JESD8-12 specification

4: Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12, for connectivity. This resistor is not required during normal operation.

5: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-36: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS, STD. SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE V_{CC} = 1.14V, WORST-CASE VCCI (PER STANDARD) APPLICABLE TO STANDARD I/O BANKS

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1] (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3V LVTTL / 3.3V LVCMOS	8 mA	8	High	5	—	1.55	2.38	0.26	0.94	1.10	2.41	1.92	2.40	2.96	ns
3.3V LVCMOS Wide Range[3]	100 µA	8	High	5	—	1.55	3.33	0.26	1.29	1.10	3.33	2.62	3.34	4.07	ns
2.5V LVCMOS	8 mA	8	High	5	—	1.55	2.39	0.26	1.15	1.10	2.42	2.05	2.38	2.80	ns
1.8V LVCMOS	4 mA	4	High	5	—	1.55	2.60	0.26	1.08	1.10	2.64	2.33	2.38	2.62	ns
1.5V LVCMOS	2 mA	2	High	5	—	1.55	2.92	0.26	1.22	1.10	2.96	2.60	2.40	2.56	ns
1.2V LVCMOS	1 mA	1	High	5	—	1.55	3.59	0.26	1.53	1.10	3.47	3.06	2.51	2.49	ns
1.2V LVCMOS Wide Range[3]	100 µA	1	High	5	—	1.55	3.59	0.26	1.53	1.10	3.47	3.06	2.51	2.49	ns

Note 1: The minimum drive strength for any LVCMOS 1.2V or LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD-8B specification.

3: All LVCMOS 1.2V software macros support LVCMOS 1.2V wide range as specified in the JESD8-12 specification

4: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.5 Detailed I/O DC Characteristics

TABLE 2-37: INPUT CAPACITANCE

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

TABLE 2-38: I/O OUTPUT BUFFER MAXIMUM RESISTANCES[1]

Applicable to Advanced I/O Banks

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3V LVTTL/3.3V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
3.3V LVCMOS Wide Range	100 µA	Same as regular 3.3V LVCMOS	Same as regular 3.3V LVCMOS
2.5V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
1.5V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
1.2V LVCMOS[4]	2 mA	158	164
1.2V LVCMOS Wide Range[4]	100 µA	Same as regular 1.2V LVCMOS	Same as regular 1.2V LVCMOS
3.3V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Note 1: These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-fpgas#IGLOO/e%20FPGAs.

2: $R_{(PULL\text{-}DOWN\text{-}MAX)} = (VOLspec) / I_{OLspec}$

3: $R_{(PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / I_{OHspec}$

4: Applicable to IGLOO V2 Devices operating at VCCI ≥ VCC

TABLE 2-39: I/O OUTPUT BUFFER MAXIMUM RESISTANCES[1] APPLICABLE TO STANDARD PLUS I/O BANKS

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3V LVTTL/3.3V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
3.3V LVCMOS Wide Range	100 µA	Same as regular 3.3V LVCMOS	Same as regular 3.3V LVCMOS
2.5V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5V LVCMOS	2 mA	200	224
	4 mA	100	112
1.2V LVCMOS[4]	2 mA	158	164
1.2V LVCMOS Wide Range[4]	100 µA	Same as regular 1.2V LVCMOS	Same as regular 1.2V LVCMOS
3.3V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Note 1: These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-fpgas#IGLOO/e%20FPGAs.

2: $R_{(PULL\text{-}DOWN\text{-}MAX)} = (VOLspec) / I_{OLspec}$

3: $R_{(PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / I_{OHspec}$

4: Applicable to IGLOO V2 Devices operating at VCCI ≥ VCC

TABLE 2-40: I/O OUTPUT BUFFER MAXIMUM RESISTANCES[1] APPLICABLE TO STANDARD I/O BANKS

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3V LVTTL/3.3V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
3.3V LVCMOS Wide Range	100 µA	Same as regular 3.3V LVCMOS	Same as regular 3.3V LVCMOS
2.5V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5V LVCMOS	2 mA	200	224
1.2V LVCMOS	1 mA	158	164
1.2V LVCMOS Wide Range[4]	100 µA	Same as regular 1.2V LVCMOS	Same as regular 1.2V LVCMOS

Note 1: These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-fpgas#IGLOO/e%20FPGAs.

2: $R_{(PULL\text{-}DOWN\text{-}MAX)} = (VOLspec) / I_{OLspec}$

3: $R_{(PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / I_{OHspec}$

TABLE 2-41: I/O WEAK PULL-UP/PULL-DOWN RESISTANCES MINIMUM AND MAXIMUM WEAK PULL-UP/PULL-DOWN RESISTANCE VALUES

VCCI	$R_{(WEAK\ PULL\text{-}UP)}$[1] ($\Omega$)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] ($\Omega$)	
	Min.	Max.	Min.	Max.
3.3V	10 K	45 K	10 K	45 K
3.3V Wide Range I/Os	10 K	45 K	10 K	45 K
2.5V	11 K	55 K	12 K	74 K
1.8V	18 K	70 K	17 K	110 K
1.5V	19 K	90 K	19 K	140 K
1.2V	25 K	110 K	25 K	150 K
1.2V Wide Range I/Os	19 K	110 K	19 K	150 K

Note 1: $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$

2: $R_{(WEAK\ PULLDOWN\text{-}MAX)} = (VOLspec) / I_{(WEAK\ PULLDOWN\text{-}MIN)}$

TABLE 2-42: I/O SHORT CURRENTS IOSH/IOSL

Applicable to Advanced I/O Banks

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3V LVTTL/3.3V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3V LVCMOS Wide Range	100 µA	Same as regular 3.3V LVCMOS	Same as regular 3.3V LVCMOS
2.5V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2V LVCMOS	2 mA	20	26
1.2V LVCMOS Wide Range	100 µA	20	26
3.3V PCI/PCI-X	Per PCI/PCI-X specification	103	109

Note: *T_J = 100°C

TABLE 2-43: I/O SHORT CURRENTS IOSH/IOSL

Applicable to Standard Plus I/O Banks

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3V LVTTL/3.3V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	103	109
3.3V LVCMOS Wide Range	100 µA	Same as regular 3.3V LVCMOS	Same as regular 3.3V LVCMOS

TABLE 2-43: I/O SHORT CURRENTS IOSH/IOSL

Applicable to Standard Plus I/O Banks

	Drive Strength	IOSL (mA)*	IOSH (mA)*
2.5V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
1.8V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	35	44
1.5V LVCMOS	2 mA	13	16
	4 mA	25	33
1.2V LVCMOS	2 mA	20	26
1.2V LVCMOS Wide Range	100 µA	20	26
3.3V PCI/PCI-X	Per PCI/PCI-X specification	103	109

Note: *T_J = 100°C

TABLE 2-44: I/O SHORT CURRENTS IOSH/IOSL APPLICABLE TO STANDARD I/O BANKS

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3V LVTTL/3.3V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
3.3V LVCMOS Wide Range	100 µA	Same as regular 3.3V LVCMOS	Same as regular 3.3V LVCMOS
2.5V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
1.8V LVCMOS	2 mA	9	11
	4 mA	17	22
1.5V LVCMOS	2 mA	13	16
1.2V LVCMOS	1 mA	20	26
1.2V LVCMOS Wide Range	100 µA	20	26

Note: *T_J = 100°C

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

TABLE 2-45: DURATION OF SHORT CIRCUIT EVENT BEFORE FAILURE

Temperature	Time before Failure
–40°C	> 20 years
–20°C	> 20 years

TABLE 2-45: DURATION OF SHORT CIRCUIT EVENT BEFORE FAILURE

Temperature	Time before Failure
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months

TABLE 2-46: I/O INPUT RISE TIME, FALL TIME, AND RELATED I/O RELIABILITY1

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (100°C)
LVDS/B-LVDS/M-LVDS/ LVPECL	No requirement	10 ns *	10 years (100°C)

Note: The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microchip recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

2.6 Single-Ended I/O Characteristics

2.6.1 3.3V LVTTL/3.3V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3V applications. It uses an LVTTL input buffer and push-pull output buffer. Furthermore, all LVCMOS 3.3V software macros comply with LVCMOS 3.3V wide range as specified in the JESD8a specification.

TABLE 2-47: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

Applicable to Advanced I/O Banks

3.3V LVTTL / 3.3V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL [1]	IIH [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA [4]	µA [4]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	10	10
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	10	10

Note 1: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3: Currents are measured at 100°C junction temperature and maximum voltage.

4: Currents are measured at 85°C junction temperature.

5: Software default selection highlighted in gray.

TABLE 2-48: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

Applicable to Standard Plus I/O Banks

3.3V LVTTL / 3.3V LVCMOS	VIL		VIH		V_{OL}	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	103	109	10	10

Note 1: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

2: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3: Currents are measured at 100°C junction temperature and maximum voltage.

4: Currents are measured at 85°C junction temperature.

5: Software default selection highlighted in gray.

TABLE 2-49: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

Applicable to Standard I/O Banks

3.3V LVTTL / 3.3V LVCMOS	VIL		VIH		V_{OL}	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10

Note 1: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

2: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3: Currents are measured at 100°C junction temperature and maximum voltage.

4: Currents are measured at 85°C junction temperature.

5: Software default selection highlighted in gray.

FIGURE 2-7: AC LOADING

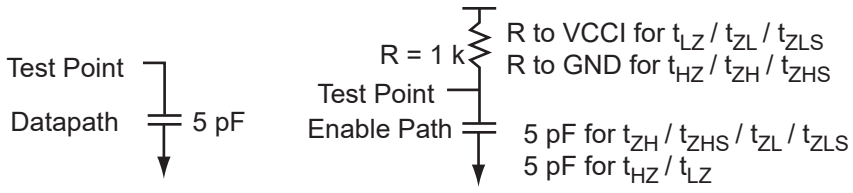


TABLE 2-50: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	5

Note: *Measuring point = Vtrip. See Table 2-29 for a complete table of trip points.

2.6.1.1 Timing Characteristics

2.6.1.1.1 Applies to 1.5V DC Core Voltage

TABLE 2-51: 3.3V LVTTL/3.3V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 3.0V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	4.47	0.18	0.85	0.66	4.56	3.89	2.24	2.19	8.15	7.48	ns
4 mA	Std.	0.97	4.47	0.18	0.85	0.66	4.56	3.89	2.24	2.19	8.15	7.48	ns
6 mA	Std.	0.97	3.74	0.18	0.85	0.66	3.82	3.37	2.49	2.63	7.42	6.96	ns
8 mA	Std.	0.97	3.74	0.18	0.85	0.66	3.82	3.37	2.49	2.63	7.42	6.96	ns
12 mA	Std.	0.97	3.23	0.18	0.85	0.66	3.30	2.98	2.66	2.91	6.89	6.57	ns
16 mA	Std.	0.97	3.08	0.18	0.85	0.66	3.14	2.89	2.70	2.99	6.74	6.48	ns
24 mA	Std.	0.97	3.00	0.18	0.85	0.66	3.06	2.91	2.74	3.27	6.66	6.50	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-52: 3.3V LVTTL/3.3V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 3.0V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.73	0.18	0.85	0.66	2.79	2.22	2.25	2.32	6.38	5.82	ns
4 mA	Std.	0.97	2.73	0.18	0.85	0.66	2.79	2.22	2.25	2.32	6.38	5.82	ns
6 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.85	2.50	2.76	5.96	5.45	ns
8 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.85	2.50	2.76	5.96	5.45	ns
12 mA	Std.	0.97	2.09	0.18	0.85	0.66	2.14	1.68	2.67	3.05	5.73	5.27	ns
16 mA	Std.	0.97	2.05	0.18	0.85	0.66	2.10	1.64	2.70	3.12	5.69	5.24	ns
24 mA	Std.	0.97	2.07	0.18	0.85	0.66	2.12	1.60	2.75	3.41	5.71	5.20	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-53: 3.3V LVTTL/3.3V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 3.0V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	3.94	0.18	0.85	0.66	4.02	3.46	1.98	2.03	7.62	7.05	ns
4 mA	Std.	0.97	3.94	0.18	0.85	0.66	4.02	3.46	1.98	2.03	7.62	7.05	ns
6 mA	Std.	0.97	3.24	0.18	0.85	0.66	3.31	2.99	2.21	2.42	6.90	6.59	ns
8 mA	Std.	0.97	3.24	0.18	0.85	0.66	3.31	2.99	2.21	2.42	6.90	6.59	ns
12 mA	Std.	0.97	2.76	0.18	0.85	0.66	2.82	2.63	2.36	2.68	6.42	6.22	ns
16 mA	Std.	0.97	2.76	0.18	0.85	0.66	2.82	2.63	2.36	2.68	6.42	6.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-54: 3.3V LVTTL/3.3V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 3.0V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.90	1.98	2.13	5.96	5.49	ns
4 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.90	1.98	2.13	5.96	5.49	ns
6 mA	Std.	0.97	1.94	0.18	0.85	0.66	1.99	1.57	2.20	2.53	5.58	5.16	ns
8 mA	Std.	0.97	1.94	0.18	0.85	0.66	1.99	1.57	2.20	2.53	5.58	5.16	ns
12 mA	Std.	0.97	1.75	0.18	0.85	0.66	1.79	1.40	2.36	2.79	5.38	4.99	ns
16 mA	Std.	0.97	1.75	0.18	0.85	0.66	1.79	1.40	2.36	2.79	5.38	4.99	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-55: 3.3V LVTTL/3.3V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 3.0V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	3.80	0.18	0.83	0.66	3.88	3.41	1.74	1.78	ns
4 mA	Std.	0.97	3.80	0.18	0.83	0.66	3.88	3.41	1.74	1.78	ns
6 mA	Std.	0.97	3.15	0.18	0.83	0.66	3.21	2.94	1.96	2.17	ns
8 mA	Std.	0.97	3.15	0.18	0.83	0.66	3.21	2.94	1.96	2.17	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-56: 3.3V LVTTL/3.3V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 3.0V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	2.19	0.18	0.83	0.66	2.24	1.79	1.74	1.87	ns
4 mA	Std.	0.97	2.19	0.18	0.83	0.66	2.24	1.79	1.74	1.87	ns
6 mA	Std.	0.97	1.85	0.18	0.83	0.66	1.89	1.46	1.96	2.26	ns
8 mA	Std.	0.97	1.85	0.18	0.83	0.66	1.89	1.46	1.96	2.26	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.6.1.1.2 Applies to 1.2V DC Core Voltage

TABLE 2-57: 3.3V LVTTL/3.3V LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 3.0V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	5.12	0.26	0.98	1.10	5.20	4.46	2.81	3.02	10.99	10.25	ns
4 mA	Std.	1.55	5.12	0.26	0.98	1.10	5.20	4.46	2.81	3.02	10.99	10.25	ns
6 mA	Std.	1.55	4.38	0.26	0.98	1.10	4.45	3.93	3.07	3.48	10.23	9.72	ns
8 mA	Std.	1.55	4.38	0.26	0.98	1.10	4.45	3.93	3.07	3.48	10.23	9.72	ns
12 mA	Std.	1.55	3.85	0.26	0.98	1.10	3.91	3.53	3.24	3.77	9.69	9.32	ns
16 mA	Std.	1.55	3.69	0.26	0.98	1.10	3.75	3.44	3.28	3.84	9.54	9.23	ns
24 mA	Std.	1.55	3.61	0.26	0.98	1.10	3.67	3.46	3.33	4.13	9.45	9.24	ns

Note: For specific junction temperature and voltage supply levels, refer to Figure 2-7, for derating values.

TABLE 2-58: 3.3V LVTTL/3.3V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 3.0V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.33	0.26	0.98	1.10	3.38	2.75	2.82	3.18	9.17	8.54	ns
4 mA	Std.	1.55	3.33	0.26	0.98	1.10	3.38	2.75	2.82	3.18	9.17	8.54	ns
6 mA	Std.	1.55	2.91	0.26	0.98	1.10	2.95	2.37	3.07	3.64	8.73	8.15	ns
8 mA	Std.	1.55	2.91	0.26	0.98	1.10	2.95	2.37	3.07	3.64	8.73	8.15	ns
12 mA	Std.	1.55	2.67	0.26	0.98	1.10	2.71	2.18	3.25	3.93	8.50	7.97	ns
16 mA	Std.	1.55	2.63	0.26	0.98	1.10	2.67	2.14	3.28	4.01	8.45	7.93	ns
24 mA	Std.	1.55	2.65	0.26	0.98	1.10	2.69	2.10	3.33	4.31	8.47	7.89	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-59: 3.3V LVTTL/3.3V LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 3.0V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	4.56	0.26	0.97	1.10	4.63	3.98	2.54	2.83	10.42	9.76	ns
4 mA	Std.	1.55	4.56	0.26	0.97	1.10	4.63	3.98	2.54	2.83	10.42	9.76	ns
6 mA	Std.	1.55	3.84	0.26	0.97	1.10	3.90	3.50	2.77	3.24	9.69	9.29	ns
8 mA	Std.	1.55	3.84	0.26	0.97	1.10	3.90	3.50	2.77	3.24	9.69	9.29	ns
12 mA	Std.	1.55	3.35	0.26	0.97	1.10	3.40	3.13	2.93	3.51	9.19	8.91	ns
16 mA	Std.	1.55	3.35	0.26	0.97	1.10	3.40	3.13	2.93	3.51	9.19	8.91	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-60: 3.3V LVTTL/3.3V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 3.0V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	2.89	0.26	0.97	1.10	2.93	2.38	2.53	2.96	8.72	8.17	ns
4 mA	Std.	1.55	2.89	0.26	0.97	1.10	2.93	2.38	2.53	2.96	8.72	8.17	ns
6 mA	Std.	1.55	2.50	0.26	0.97	1.10	2.54	2.04	2.77	3.37	8.33	7.82	ns
8 mA	Std.	1.55	2.50	0.26	0.97	1.10	2.54	2.04	2.77	3.37	8.33	7.82	ns
12 mA	Std.	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns
16 mA	Std.	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-61: 3.3V LVTTL/3.3V LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 3.0V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	4.39	0.26	0.94	1.10	4.46	3.91	2.17	2.44	ns
4 mA	Std.	1.55	4.39	0.26	0.94	1.10	4.46	3.91	2.17	2.44	ns
6 mA	Std.	1.55	3.72	0.26	0.94	1.10	3.78	3.43	2.40	2.85	ns
8 mA	Std.	1.55	3.72	0.26	0.94	1.10	3.78	3.43	2.40	2.85	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-62: 3.3V LVTTL/3.3V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 3.0V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	2.74	0.26	0.94	1.10	2.78	2.26	2.17	2.55	ns
4 mA	Std.	1.55	2.74	0.26	0.94	1.10	2.78	2.26	2.17	2.55	ns
6 mA	Std.	1.55	2.38	0.26	0.94	1.10	2.41	1.92	2.40	2.96	ns
8 mA	Std.	1.55	2.38	0.26	0.94	1.10	2.41	1.92	2.40	2.96	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

2.6.2 3.3V LVCMOS WIDE RANGE

TABLE 2-63: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS FOR LVCMOS 3.3V WIDE RANGE

Applicable to Advanced I/O Banks

3.3V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[1]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	8 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	12 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	103	109	10	10
100 µA	16 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	132	127	10	10
100 µA	24 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	268	181	10	10

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

3: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

4: Currents are measured at 100°C junction temperature and maximum voltage.

5: Currents are measured at 85°C junction temperature.

6: Software default selection highlighted in gray.

TABLE 2-64: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS FOR LVCMOS 3.3V WIDE RANGE

Applicable to Standard Plus I/O Banks

3.3V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[1]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10

TABLE 2-64: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS FOR LVCMOS 3.3V WIDE RANGE

Applicable to Standard Plus I/O Banks

3.3V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[1]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	8 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	12 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	103	109	10	10
100 µA	16 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	103	109	10	10

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

3: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

4: Currents are measured at 100°C junction temperature and maximum voltage.

5: Currents are measured at 85°C junction temperature.

6: Software default selection highlighted in gray.

TABLE 2-65: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS FOR LVCMOS 3.3V WIDE RANGE

Applicable to Standard I/O Banks

3.3V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[1]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	8 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10

TABLE 2-65: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS FOR LVCMOS 3.3V WIDE RANGE

Applicable to Standard I/O Banks

3.3V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL [2]	IIH [3]
Drive Strength	Equivalent Software Default Drive Strength Option[1]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[4]	Max. mA[4]	µA [5]	µA [5]

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

3: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

4: Currents are measured at 100°C junction temperature and maximum voltage.

5: Currents are measured at 85°C junction temperature.

6: Software default selection highlighted in gray.

TABLE 2-66: 3.3V LVCMOS WIDE RANGE AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	5

Note: *Measuring point = Vtrip. See Table 2-29 for a complete table of trip points.

2.6.2.1 Timing Characteristics

2.6.2.1.1 Applies to 1.5V DC Core Voltage

TABLE 2-67: 3.3V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.7V

Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	0.97	6.61	0.18	1.19	0.66	6.63	5.63	3.15	2.98	10.22	9.23	ns
100 µA	4 mA	Std.	0.97	6.61	0.18	1.19	0.66	6.63	5.63	3.15	2.98	10.22	9.23	ns
100 µA	6 mA	Std.	0.97	5.49	0.18	1.19	0.66	5.51	4.84	3.54	3.66	9.10	8.44	ns
100 µA	8 mA	Std.	0.97	5.49	0.18	1.19	0.66	5.51	4.84	3.54	3.66	9.10	8.44	ns
100 µA	12 mA	Std.	0.97	4.69	0.18	1.19	0.66	4.71	4.25	3.80	4.10	8.31	7.85	ns
100 µA	16 mA	Std.	0.97	4.46	0.18	1.19	0.66	4.48	4.11	3.86	4.21	8.07	7.71	ns
100 µA	24 mA	Std.	0.97	4.34	0.18	1.19	0.66	4.36	4.14	3.93	4.64	7.95	7.74	ns

TABLE 2-67: 3.3V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.7V
Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-68: 3.3V LVCMOS WIDE RANGE HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.7V
Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	0.97	3.92	0.18	1.19	0.66	3.94	3.10	3.16	3.17	7.54	6.70	ns
100 µA	4 mA	Std.	0.97	3.92	0.18	1.19	0.66	3.94	3.10	3.16	3.17	7.54	6.70	ns
100 µA	6 mA	Std.	0.97	3.28	0.18	1.19	0.66	3.30	2.54	3.54	3.86	6.90	6.14	ns
100 µA	8 mA	Std.	0.97	3.28	0.18	1.19	0.66	3.30	2.54	3.54	3.86	6.90	6.14	ns
100 µA	12 mA	Std.	0.97	2.93	0.18	1.19	0.66	2.95	2.27	3.81	4.30	6.54	5.87	ns
100 µA	16 mA	Std.	0.97	2.87	0.18	1.19	0.66	2.89	2.22	3.86	4.41	6.49	5.82	ns
100 µA	24 mA	Std.	0.97	2.90	0.18	1.19	0.66	2.92	2.16	3.94	4.86	6.51	5.75	ns

Note 1: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2: Software default selection highlighted in gray.

3: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

TABLE 2-69: 3.3V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.7V
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	0.97	5.84	0.18	1.20	0.66	5.86	5.04	2.74	2.71	9.46	8.64	ns
100 µA	4 mA	Std.	0.97	5.84	0.18	1.20	0.66	5.86	5.04	2.74	2.71	9.46	8.64	ns
100 µA	6 mA	Std.	0.97	4.76	0.18	1.20	0.66	4.78	4.33	3.09	3.33	8.37	7.93	ns
100 µA	8 mA	Std.	0.97	4.76	0.18	1.20	0.66	4.78	4.33	3.09	3.33	8.37	7.93	ns
100 µA	12 mA	Std.	0.97	4.02	0.18	1.20	0.66	4.04	3.78	3.33	3.73	7.64	7.37	ns

TABLE 2-69: 3.3V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.7V
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	16 mA	Std.	0.97	4.02	0.18	1.20	0.66	4.04	3.78	3.33	3.73	7.64	7.37	ns

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-70: 3.3V LVCMOS WIDE RANGE HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.7V
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	0.97	3.33	0.18	1.20	0.66	3.35	2.68	2.73	2.88	6.94	6.27	ns
100 µA	4 mA	Std.	0.97	3.33	0.18	1.20	0.66	3.35	2.68	2.73	2.88	6.94	6.27	ns
100 µA	6 mA	Std.	0.97	2.75	0.18	1.20	0.66	2.77	2.17	3.08	3.50	6.36	5.77	ns
100 µA	8 mA	Std.	0.97	2.75	0.18	1.20	0.66	2.77	2.17	3.08	3.50	6.36	5.77	ns
100 µA	12 mA	Std.	0.97	2.45	0.18	1.20	0.66	2.47	1.92	3.33	3.90	6.06	5.51	ns
100 µA	16 mA	Std.	0.97	2.45	0.18	1.20	0.66	2.47	1.92	3.33	3.90	6.06	5.51	ns

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

3: Software default selection highlighted in gray.

TABLE 2-71: 3.3V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.7V
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	Std.	0.97	5.64	0.18	1.17	0.66	5.65	4.98	2.45	2.42	ns
100 µA	4 mA	Std.	0.97	5.64	0.18	1.17	0.66	5.65	4.98	2.45	2.42	ns
100 µA	6 mA	Std.	0.97	4.63	0.18	1.17	0.66	4.64	4.26	2.80	3.02	ns
100 µA	8 mA	Std.	0.97	4.63	0.18	1.17	0.66	4.64	4.26	2.80	3.02	ns

TABLE 2-71: 3.3V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.7V
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-72: 3.3V LVCMOS WIDE RANGE HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.7V
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	0.97	3.16	0.18	1.17	0.66	3.17	2.53	2.45	2.56	0.97	ns
100 µA	4 mA	0.97	3.16	0.18	1.17	0.66	3.17	2.53	2.45	2.56	0.97	ns
100 µA	6 mA	0.97	2.62	0.18	1.17	0.66	2.63	2.02	2.79	3.17	0.97	ns
100 µA	8 mA	0.97	2.62	0.18	1.17	0.66	2.63	2.02	2.79	3.17	0.97	ns

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

3: Software default selection highlighted in gray.

2.6.2.1.2 Applies to 1.2V DC Core Voltage

TABLE 2-73: 3.3V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 2.7V
Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	1.55	7.52	0.26	1.32	1.10	7.52	6.38	3.84	4.02	13.31	12.16	ns
100 µA	4 mA	Std.	1.55	7.52	0.26	1.32	1.10	7.52	6.38	3.84	4.02	13.31	12.16	ns
100 µA	6 mA	Std.	1.55	6.37	0.26	1.32	1.10	6.37	5.57	4.23	4.73	12.16	11.35	ns
100 µA	8 mA	Std.	1.55	6.37	0.26	1.32	1.10	6.37	5.57	4.23	4.73	12.16	11.35	ns
100 µA	12 mA	Std.	1.55	5.55	0.26	1.32	1.10	5.55	4.96	4.50	5.18	11.34	10.75	ns
100 µA	16 mA	Std.	1.55	5.32	0.26	1.32	1.10	5.32	4.82	4.56	5.29	11.10	10.61	ns

TABLE 2-73: 3.3V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 2.7V
Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	24 mA	Std.	1.55	5.19	0.26	1.32	1.10	5.19	4.85	4.63	5.74	10.98	10.63	ns

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-74: 3.3V LVCMOS WIDE RANGE HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 2.7V
Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	1.55	4.75	0.26	1.32	1.10	4.75	3.77	3.84	4.27	10.54	9.56	ns
100 µA	4 mA	Std.	1.55	4.75	0.26	1.32	1.10	4.75	3.77	3.84	4.27	10.54	9.56	ns
100 µA	6 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.19	4.24	4.98	9.88	8.98	ns
100 µA	8 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.19	4.24	4.98	9.88	8.98	ns
100 µA	12 mA	Std.	1.55	3.73	0.26	1.32	1.10	3.73	2.91	4.51	5.43	9.52	8.69	ns
100 µA	16 mA	Std.	1.55	3.67	0.26	1.32	1.10	3.67	2.85	4.57	5.55	9.46	8.64	ns
100 µA	24 mA	Std.	1.55	3.70	0.26	1.32	1.10	3.70	2.79	4.65	6.01	9.49	8.58	ns

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

3: Software default selection highlighted in gray.

TABLE 2-75: 3.3V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 2.7V
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	1.55	6.69	0.26	1.32	1.10	6.69	5.73	3.41	3.72	12.48	11.52	ns
100 µA	4 mA	Std.	1.55	6.69	0.26	1.32	1.10	6.69	5.73	3.41	3.72	12.48	11.52	ns
100 µA	6 mA	Std.	1.55	5.58	0.26	1.32	1.10	5.58	5.01	3.77	4.35	11.36	10.79	ns
100 µA	8 mA	Std.	1.55	5.58	0.26	1.32	1.10	5.58	5.01	3.77	4.35	11.36	10.79	ns

TABLE 2-75: 3.3V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 2.7V
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	12 mA	Std.	1.55	4.82	0.26	1.32	1.10	4.82	4.44	4.02	4.76	10.61	10.23	ns
100 µA	16 mA	Std.	1.55	4.82	0.26	1.32	1.10	4.82	4.44	4.02	4.76	10.61	10.23	ns

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-76: 3.3V LVCMOS WIDE RANGE HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 2.7V
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.30	3.40	3.92	9.89	9.09	ns
100 µA	4 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.30	3.40	3.92	9.89	9.09	ns
100 µA	6 mA	Std.	1.55	3.51	0.26	1.32	1.10	3.51	2.79	3.76	4.56	9.30	8.57	ns
100 µA	8 mA	Std.	1.55	3.51	0.26	1.32	1.10	3.51	2.79	3.76	4.56	9.30	8.57	ns
100 µA	12 mA	Std.	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns
100 µA	16 mA	Std.	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

3: Software default selection highlighted in gray.

TABLE 2-77: 3.3V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14V, Worst-Case VCCI = 2.7V
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	Std.	1.55	6.44	0.26	1.29	1.10	6.44	5.64	2.99	3.28	ns
100 µA	4 mA	Std.	1.55	6.44	0.26	1.29	1.10	6.44	5.64	2.99	3.28	ns
100 µA	6 mA	Std.	1.55	5.41	0.26	1.29	1.10	5.41	4.91	3.35	3.89	ns
100 µA	8 mA	Std.	1.55	5.41	0.26	1.29	1.10	5.41	4.91	3.35	3.89	ns

TABLE 2-77: 3.3V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14V, Worst-Case VCCI = 2.7V
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-78: 3.3V LVCMOS WIDE RANGE HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 2.7V
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	Std.	1.55	3.89	0.26	1.29	1.10	3.89	3.13	2.99	3.45	ns
100 µA	4 mA	Std.	1.55	3.89	0.26	1.29	1.10	3.89	3.13	2.99	3.45	ns
100 µA	6 mA	Std.	1.55	3.33	0.26	1.29	1.10	3.33	2.62	3.34	4.07	ns
100 µA	8 mA	Std.	1.55	3.33	0.26	1.29	1.10	3.33	2.62	3.34	4.07	ns

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

3: Software default selection highlighted in gray.

2.6.3 2.5V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5V applications.

TABLE 2-79: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO ADVANCED I/O BANKS

2.5V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	10	10

TABLE 2-79: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO ADVANCED I/O BANKS

2.5V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	10	10

Note 1: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

2: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3: Currents are measured at 100°C junction temperature and maximum voltage.

4: Currents are measured at 85°C junction temperature.

5: Software default selection highlighted in gray.

TABLE 2-80: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS
Applicable to Standard Plus I/O Banks

2.5V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10

Note 1: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

2: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3: Currents are measured at 100°C junction temperature and maximum voltage.

4: Currents are measured at 85°C junction temperature.

5: Software default selection highlighted in gray.

TABLE 2-81: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS
Applicable to Standard I/O Banks

2.5V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10

TABLE 2-81: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

Applicable to Standard I/O Banks

2.5V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]

Note 1: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

2: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3: Currents are measured at 100°C junction temperature and maximum voltage.

4: Currents are measured at 85°C junction temperature.

5: Software default selection highlighted in gray.

FIGURE 2-8: AC LOADING

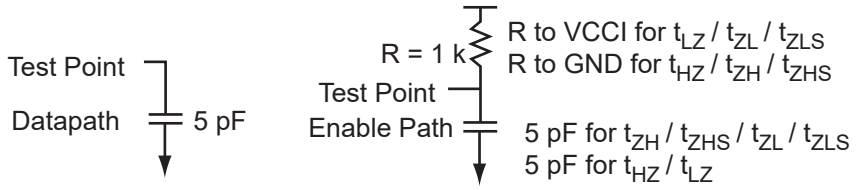


TABLE 2-82: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	2.5	1.2	5

Note: *Measuring point = Vtrip. See Table 2-29 for a complete table of trip points.

2.6.3.1 Timing Characteristics

2.6.3.1.1 Applies to 1.5V DC Core Voltage

TABLE 2-83: 2.5V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.3V

Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	4.96	0.18	1.08	0.66	5.06	4.59	2.26	2.00	8.66	8.19	ns
4 mA	Std.	0.97	4.96	0.18	1.08	0.66	5.06	4.59	2.26	2.00	8.66	8.19	ns
6 mA	Std.	0.97	4.15	0.18	1.08	0.66	4.24	3.94	2.54	2.51	7.83	7.53	ns
8 mA	Std.	0.97	4.15	0.18	1.08	0.66	4.24	3.94	2.54	2.51	7.83	7.53	ns
12 mA	Std.	0.97	3.57	0.18	1.08	0.66	3.65	3.47	2.73	2.84	7.24	7.06	ns
16 mA	Std.	0.97	3.39	0.18	1.08	0.66	3.46	3.36	2.78	2.92	7.06	6.95	ns
24 mA	Std.	0.97	3.38	0.18	1.08	0.66	3.38	3.38	2.83	3.25	6.98	6.98	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-84: 2.5V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.3V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.77	0.18	1.08	0.66	2.83	2.60	2.26	2.08	6.42	6.19	ns
4 mA	Std.	0.97	2.77	0.18	1.08	0.66	2.83	2.60	2.26	2.08	6.42	6.19	ns
6 mA	Std.	0.97	2.34	0.18	1.08	0.66	2.39	2.08	2.54	2.60	5.99	5.68	ns
8 mA	Std.	0.97	2.34	0.18	1.08	0.66	2.39	2.08	2.54	2.60	5.99	5.68	ns
12 mA	Std.	0.97	2.09	0.18	1.08	0.66	2.14	1.83	2.73	2.93	5.73	5.43	ns
16 mA	Std.	0.97	2.05	0.18	1.08	0.66	2.09	1.78	2.78	3.02	5.69	5.38	ns
24 mA	Std.	0.97	2.06	0.18	1.08	0.66	2.10	1.72	2.83	3.35	5.70	5.32	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-85: 2.5V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.3V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	4.42	0.18	1.08	0.66	4.51	4.10	1.96	1.85	8.10	7.69	ns
4 mA	Std.	0.97	4.42	0.18	1.08	0.66	4.51	4.10	1.96	1.85	8.10	7.69	ns
6 mA	Std.	0.97	3.62	0.18	1.08	0.66	3.70	3.52	2.21	2.32	7.29	7.11	ns
8 mA	Std.	0.97	3.62	0.18	1.08	0.66	3.70	3.52	2.21	2.32	7.29	7.11	ns
12 mA	Std.	0.97	3.09	0.18	1.08	0.66	3.15	3.09	2.39	2.61	6.74	6.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-86: 2.5V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.3V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.36	0.18	1.08	0.66	2.41	2.21	1.96	1.92	6.01	5.81	ns
4 mA	Std.	0.97	2.36	0.18	1.08	0.66	2.41	2.21	1.96	1.92	6.01	5.81	ns
6 mA	Std.	0.97	1.97	0.18	1.08	0.66	2.01	1.75	2.21	2.40	5.61	5.34	ns
8 mA	Std.	0.97	1.97	0.18	1.08	0.66	2.01	1.75	2.21	2.40	5.61	5.34	ns
12 mA	Std.	0.97	1.75	0.18	1.08	0.66	1.79	1.52	2.38	2.70	5.39	5.11	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-87: 2.5V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.3V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	4.27	0.18	1.04	0.66	4.36	4.06	1.71	1.62	ns
4 mA	Std.	0.97	4.27	0.18	1.04	0.66	4.36	4.06	1.71	1.62	ns
6 mA	Std.	0.97	3.54	0.18	1.04	0.66	3.61	3.48	1.95	2.08	ns
8 mA	Std.	0.97	3.54	0.18	1.04	0.66	3.61	3.48	1.95	2.08	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-88: 2.5V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.3V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	2.24	0.18	1.04	0.66	2.29	2.09	1.71	1.68	ns
4 mA	Std.	0.97	2.24	0.18	1.04	0.66	2.29	2.09	1.71	1.68	ns
6 mA	Std.	0.97	1.88	0.18	1.04	0.66	1.92	1.63	1.95	2.15	ns
8 mA	Std.	0.97	1.88	0.18	1.04	0.66	1.92	1.63	1.95	2.15	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.6.3.1.2 Applies to 1.2V Core Voltage

TABLE 2-89: 2.5V LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 2.3V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	5.59	0.26	1.20	1.10	5.68	5.14	2.82	2.80	11.47	10.93	ns
4 mA	Std.	1.55	5.59	0.26	1.20	1.10	5.68	5.14	2.82	2.80	11.47	10.93	ns
6 mA	Std.	1.55	4.76	0.26	1.20	1.10	4.84	4.47	3.10	3.33	10.62	10.26	ns
8 mA	Std.	1.55	4.76	0.26	1.20	1.10	4.84	4.47	3.10	3.33	10.62	10.26	ns
12 mA	Std.	1.55	4.17	0.26	1.20	1.10	4.23	3.99	3.30	3.67	10.02	9.77	ns
16 mA	Std.	1.55	3.98	0.26	1.20	1.10	4.04	3.88	3.34	3.76	9.83	9.66	ns
24 mA	Std.	1.55	3.90	0.26	1.20	1.10	3.96	3.90	3.40	4.09	9.75	9.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-90: 2.5V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 2.3V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.33	0.26	1.20	1.10	3.38	3.09	2.82	2.91	9.17	8.88	ns
4 mA	Std.	1.55	3.33	0.26	1.20	1.10	3.38	3.09	2.82	2.91	9.17	8.88	ns
6 mA	Std.	1.55	2.89	0.26	1.20	1.10	2.93	2.56	3.10	3.45	8.72	8.34	ns
8 mA	Std.	1.55	2.89	0.26	1.20	1.10	2.93	2.56	3.10	3.45	8.72	8.34	ns
12 mA	Std.	1.55	2.64	0.26	1.20	1.10	2.67	2.29	3.30	3.79	8.46	8.08	ns
16 mA	Std.	1.55	2.59	0.26	1.20	1.10	2.63	2.24	3.34	3.88	8.41	8.03	ns
24 mA	Std.	1.55	2.60	0.26	1.20	1.10	2.64	2.18	3.40	4.22	8.42	7.97	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-91: 2.5V LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 2.3V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	5.02	0.26	1.19	1.10	5.11	4.60	2.50	2.62	10.89	10.38	ns
4 mA	Std.	1.55	5.02	0.26	1.19	1.10	5.11	4.60	2.50	2.62	10.89	10.38	ns
6 mA	Std.	1.55	4.21	0.26	1.19	1.10	4.27	4.00	2.76	3.10	10.06	9.79	ns
8 mA	Std.	1.55	4.21	0.26	1.19	1.10	4.27	4.00	2.76	3.10	10.06	9.79	ns
12 mA	Std.	1.55	3.66	0.26	1.19	1.10	3.71	3.55	2.94	3.41	9.50	9.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-92: 2.5V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 2.3V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	2.91	0.26	1.19	1.10	2.95	2.66	2.50	2.72	8.74	8.45	ns
4 mA	Std.	1.55	2.91	0.26	1.19	1.10	2.95	2.66	2.50	2.72	8.74	8.45	ns
6 mA	Std.	1.55	2.51	0.26	1.19	1.10	2.54	2.18	2.75	3.21	8.33	7.97	ns
8 mA	Std.	1.55	2.51	0.26	1.19	1.10	2.54	2.18	2.75	3.21	8.33	7.97	ns
12 mA	Std.	1.55	2.29	0.26	1.19	1.10	2.32	1.94	2.94	3.52	8.10	7.73	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-93: 2.5V LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 2.3V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	4.85	0.26	1.15	1.10	4.93	4.55	2.13	2.24	ns
4 mA	Std.	1.55	4.85	0.26	1.15	1.10	4.93	4.55	2.13	2.24	ns
6 mA	Std.	1.55	4.09	0.26	1.15	1.10	4.16	3.95	2.38	2.71	ns
8 mA	Std.	1.55	4.09	0.26	1.15	1.10	4.16	3.95	2.38	2.71	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-94: 2.5V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 2.3V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	2.76	0.26	1.15	1.10	2.80	2.52	2.13	2.32	ns
4 mA	Std.	1.55	2.76	0.26	1.15	1.10	2.80	2.52	2.13	2.32	ns
6 mA	Std.	1.55	2.39	0.26	1.15	1.10	2.42	2.05	2.38	2.80	ns
8 mA	Std.	1.55	2.39	0.26	1.15	1.10	2.42	2.05	2.38	2.80	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

2.6.4 1.8V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

TABLE 2-95: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

Applicable to Advanced I/O Banks

1.8V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	4	4	17	22	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	6	6	35	44	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8	45	51	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12	91	74	10	10
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	16	16	91	74	10	10

Note 1: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3: Currents are measured at 100°C junction temperature and maximum voltage.

4: Currents are measured at 85°C junction temperature.

5: Software default selection highlighted in gray.

TABLE 2-96: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

Applicable to Standard Plus I/O Banks

1.8V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	4	4	17	22	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	6	6	35	44	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8	35	44	10	10

TABLE 2-96: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

Applicable to Standard Plus I/O Banks

1.8V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL [1]	IIH [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]

Note 1: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3: Currents are measured at 100°C junction temperature and maximum voltage.

4: Currents are measured at 85°C junction temperature.

5: Software default selection highlighted in gray.

TABLE 2-97: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

Applicable to Standard I/O Banks

1.8V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL [1]	IIH [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	17	22	10	10

Note 1: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3: Currents are measured at 100°C junction temperature and maximum voltage.

4: Currents are measured at 85°C junction temperature.

5: Software default selection highlighted in gray.

FIGURE 2-9: AC LOADING

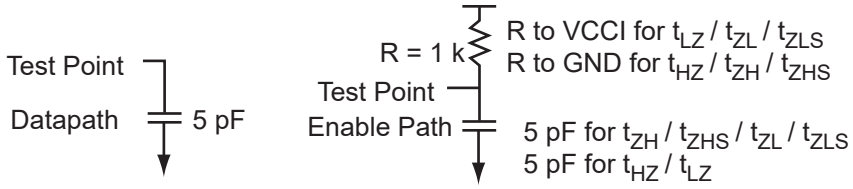


TABLE 2-98: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.8	0.9	5

Note: *Measuring point = Vtrip. See Table 2-29 for a complete table of trip points.

2.6.4.1 Timing Characteristics

2.6.4.1.1 1.5V DC Core Voltage

TABLE 2-99: 1.8V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.7V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	6.38	0.18	1.01	0.66	6.51	5.93	2.33	1.56	10.10	9.53	ns
4 mA	Std.	0.97	5.35	0.18	1.01	0.66	5.46	5.04	2.67	2.38	9.05	8.64	ns
6 mA	Std.	0.97	4.62	0.18	1.01	0.66	4.71	4.44	2.90	2.79	8.31	8.04	ns
8 mA	Std.	0.97	4.37	0.18	1.01	0.66	4.46	4.31	2.95	2.89	8.05	7.90	ns
12 mA	Std.	0.97	4.32	0.18	1.01	0.66	4.37	4.32	3.03	3.30	7.97	7.92	ns
16 mA	Std.	0.97	4.32	0.18	1.01	0.66	4.37	4.32	3.03	3.30	7.97	7.92	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-100: 1.8V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.7V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	3.25	0.18	1.01	0.66	3.21	3.25	2.33	1.61	6.80	6.85	ns
4 mA	Std.	0.97	2.62	0.18	1.01	0.66	2.68	2.51	2.66	2.46	6.27	6.11	ns
6 mA	Std.	0.97	2.31	0.18	1.01	0.66	2.36	2.15	2.90	2.87	5.95	5.75	ns
8 mA	Std.	0.97	2.25	0.18	1.01	0.66	2.30	2.08	2.95	2.98	5.89	5.68	ns
12 mA	Std.	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns
16 mA	Std.	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-101: 1.8V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.7V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	5.78	0.18	1.01	0.66	5.90	5.32	1.95	1.47	9.49	8.91	ns
4 mA	Std.	0.97	4.75	0.18	1.01	0.66	4.85	4.54	2.25	2.21	8.44	8.13	ns
6 mA	Std.	0.97	4.07	0.18	1.01	0.66	4.15	3.98	2.46	2.58	7.75	7.57	ns
8 mA	Std.	0.97	4.07	0.18	1.01	0.66	4.15	3.98	2.46	2.58	7.75	7.57	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-102: 1.8V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.7V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.76	0.18	1.01	0.66	2.79	2.76	1.94	1.51	6.39	6.35	ns
4 mA	Std.	0.97	2.25	0.18	1.01	0.66	2.30	2.09	2.24	2.29	5.89	5.69	ns
6 mA	Std.	0.97	1.97	0.18	1.01	0.66	2.02	1.76	2.46	2.66	5.61	5.36	ns
8 mA	Std.	0.97	1.97	0.18	1.01	0.66	2.02	1.76	2.46	2.66	5.61	5.36	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-103: 1.8V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.7V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	5.63	0.18	0.98	0.66	5.74	5.30	1.68	1.24	ns
4 mA	Std.	0.97	4.69	0.18	0.98	0.66	4.79	4.52	1.97	1.98	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-104: 1.8V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.7V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	2.62	0.18	0.98	0.66	2.67	2.59	1.67	1.29	2.62	ns
4 mA	Std.	2.18	0.18	0.98	0.66	2.22	1.93	1.97	2.06	2.18	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.6.4.1.2 1.2V DC Core Voltage

TABLE 2-105: 1.8V LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.7V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	6.97	0.26	1.11	1.10	7.08	6.48	2.87	2.29	12.87	12.27	ns
4 mA	Std.	1.55	5.91	0.26	1.11	1.10	6.01	5.57	3.21	3.14	11.79	11.36	ns
6 mA	Std.	1.55	5.16	0.26	1.11	1.10	5.24	4.95	3.45	3.55	11.03	10.74	ns
8 mA	Std.	1.55	4.90	0.26	1.11	1.10	4.98	4.81	3.50	3.66	10.77	10.60	ns
12 mA	Std.	1.55	4.83	0.26	1.11	1.10	4.90	4.83	3.58	4.08	10.68	10.61	ns
16 mA	Std.	1.55	4.83	0.26	1.11	1.10	4.90	4.83	3.58	4.08	10.68	10.61	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-106: 1.8V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.7V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.73	0.26	1.11	1.10	3.71	3.73	2.86	2.34	9.49	9.51	ns
4 mA	Std.	1.55	3.12	0.26	1.11	1.10	3.16	2.97	3.21	3.22	8.95	8.75	ns
6 mA	Std.	1.55	2.79	0.26	1.11	1.10	2.83	2.59	3.45	3.65	8.62	8.38	ns
8 mA	Std.	1.55	2.73	0.26	1.11	1.10	2.77	2.52	3.50	3.75	8.56	8.30	ns
12 mA	Std.	1.55	2.72	0.26	1.11	1.10	2.76	2.43	3.58	4.19	8.55	8.22	ns
16 mA	Std.	1.55	2.72	0.26	1.11	1.10	2.76	2.43	3.58	4.19	8.55	8.22	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-107: 1.8V LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.7V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	6.32	0.26	1.11	1.10	6.43	5.81	2.47	2.16	12.22	11.60	ns
4 mA	Std.	1.55	5.27	0.26	1.11	1.10	5.35	5.01	2.78	2.92	11.14	10.79	ns
6 mA	Std.	1.55	4.56	0.26	1.11	1.10	4.64	4.44	3.00	3.30	10.42	10.22	ns
8 mA	Std.	1.55	4.56	0.26	1.11	1.10	4.64	4.44	3.00	3.30	10.42	10.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-108: 1.8V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.7V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.22	0.26	1.11	1.10	3.26	3.18	2.47	2.20	9.05	8.97	ns
4 mA	Std.	1.55	2.72	0.26	1.11	1.10	2.75	2.50	2.78	3.01	8.54	8.29	ns
6 mA	Std.	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns
8 mA	Std.	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-109: 1.8V LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.7V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	6.13	0.26	1.08	1.10	6.24	5.79	2.08	1.78	ns
4 mA	Std.	1.55	5.17	0.26	1.08	1.10	5.26	4.98	2.38	2.54	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-110: 1.8V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.7V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	3.06	0.26	1.08	1.10	3.10	3.01	2.08	1.83	3.06	ns
4 mA	Std.	2.60	0.26	1.08	1.10	2.64	2.33	2.38	2.62	2.60	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

2.6.5 1.5V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5V input buffer and a push-pull output buffer.

TABLE 2-111: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

Applicable to Advanced I/O Banks

1.5V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	6	6	32	39	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	8	8	66	55	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12	66	55	10	10

Note 1: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

2: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3: Currents are measured at 100°C junction temperature and maximum voltage.

4: Currents are measured at 85°C junction temperature.

5: Software default selection highlighted in gray.

TABLE 2-112: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

Applicable to Standard Plus I/O Banks

1.5V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10

TABLE 2-112: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

Applicable to Standard Plus I/O Banks

1.5V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10

Note 1: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

2: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3: Currents are measured at 100°C junction temperature and maximum voltage.

4: Currents are measured at 85°C junction temperature.

5: Software default selection highlighted in gray.

TABLE 2-113: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

Applicable to Standard I/O Banks

1.5V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10

Note 1: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

2: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN <V CCI. Input current is larger when operating outside recommended ranges

3: Currents are measured at 100°C junction temperature and maximum voltage.

4: Currents are measured at 85°C junction temperature.

5: Software default selection highlighted in gray.

FIGURE 2-10: AC LOADING

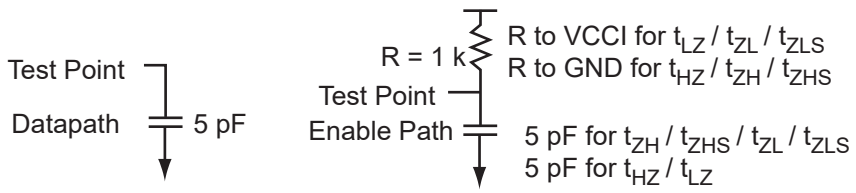


TABLE 2-114: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.5	0.75	5

TABLE 2-114: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)

Note: *Measuring point = Vtrip. See Table 2-29 for a complete table of trip points.

2.6.5.1 Timing Characteristics

2.6.5.1.1 1.5V DC Core Voltage

TABLE 2-115: 1.5V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.4V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	6.62	0.18	1.17	0.66	6.75	6.06	2.79	2.31	10.35	9.66	ns
4 mA	Std.	0.97	5.75	0.18	1.17	0.66	5.86	5.34	3.06	2.78	9.46	8.93	ns
6 mA	Std.	0.97	5.43	0.18	1.17	0.66	5.54	5.19	3.12	2.90	9.13	8.78	ns
8 mA	Std.	0.97	5.35	0.18	1.17	0.66	5.46	5.20	2.63	3.36	9.06	8.79	ns
12 mA	Std.	0.97	5.35	0.18	1.17	0.66	5.46	5.20	2.63	3.36	9.06	8.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-116: 1.5V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.4V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.97	0.18	1.17	0.66	3.04	2.90	2.78	2.40	6.63	6.50	ns
4 mA	Std.	0.97	2.60	0.18	1.17	0.66	2.65	2.45	3.05	2.88	6.25	6.05	ns
6 mA	Std.	0.97	2.53	0.18	1.17	0.66	2.58	2.37	3.11	3.00	6.18	5.96	ns
8 mA	Std.	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns
12 mA	Std.	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-117: 1.5V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.4V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	5.93	0.18	1.18	0.66	6.04	5.46	2.30	2.15	9.64	9.06	ns
4 mA	Std.	0.97	5.11	0.18	1.18	0.66	5.21	4.80	2.54	2.58	8.80	8.39	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-118: 1.5V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.4V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.58	0.18	1.18	0.66	2.64	2.41	2.29	2.24	6.23	6.01	ns
4 mA	Std.	0.97	2.25	0.18	1.18	0.66	2.30	2.00	2.53	2.68	5.89	5.59	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-119: 1.5V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.4V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	5.88	0.18	1.14	0.66	6.00	5.45	2.00	1.94	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-120: 1.5V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 1.4V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	2.51	0.18	1.14	0.66	2.56	2.21	1.99	2.03	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.6.5.2 1.2V DC Core Voltage

TABLE 2-121: 1.5V LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.4V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	7.17	0.26	1.27	1.10	7.29	6.60	3.33	3.03	13.07	12.39	ns
4 mA	Std.	1.55	6.27	0.26	1.27	1.10	6.37	5.86	3.61	3.51	12.16	11.64	ns
6 mA	Std.	1.55	5.94	0.26	1.27	1.10	6.04	5.70	3.67	3.64	11.82	11.48	ns
8 mA	Std.	1.55	5.86	0.26	1.27	1.10	5.96	5.71	2.83	4.11	11.74	11.50	ns
12 mA	Std.	1.55	5.86	0.26	1.27	1.10	5.96	5.71	2.83	4.11	11.74	11.50	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-122: 1.5V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.4V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.44	0.26	1.27	1.10	3.49	3.35	3.32	3.12	9.28	9.14	ns
4 mA	Std.	1.55	3.06	0.26	1.27	1.10	3.10	2.89	3.60	3.61	8.89	8.67	ns
6 mA	Std.	1.55	2.98	0.26	1.27	1.10	3.02	2.80	3.66	3.74	8.81	8.58	ns
8 mA	Std.	1.55	2.96	0.26	1.27	1.10	3.00	2.70	3.75	4.23	8.78	8.48	ns
12 mA	Std.	1.55	2.96	0.26	1.27	1.10	3.00	2.70	3.75	4.23	8.78	8.48	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-123: 1.5V LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.4V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	6.43	0.26	1.27	1.10	6.54	5.95	2.82	2.83	12.32	11.74	ns
4 mA	Std.	1.55	5.59	0.26	1.27	1.10	5.68	5.27	3.07	3.27	11.47	11.05	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-124: 1.5V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.4V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.02	0.26	1.27	1.10	3.07	2.81	2.82	2.92	8.85	8.59	ns
4 mA	Std.	1.55	2.68	0.26	1.27	1.10	2.72	2.39	3.07	3.37	8.50	8.18	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-125: 1.5V LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.4V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	6.35	0.26	1.22	1.10	6.46	5.93	2.40	2.46	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-126: 1.5V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.4V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	2.92	0.26	1.22	1.10	2.96	2.60	2.40	2.56	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

2.6.6 1.2V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2V complies with the LVCMOS standard JESD8-12A for general purpose 1.2V applications. It uses a 1.2V input buffer and a push-pull output buffer. Furthermore, all LVCMOS 1.2V software macros comply with LVCMOS 1.2V wide range as specified in the JESD8-12A specification.

TABLE 2-127: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

Applicable to Advanced I/O Banks

1.2V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Note 1: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.
2: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges
3: Currents are measured at 100°C junction temperature and maximum voltage.
4: Currents are measured at 85°C junction temperature.
5: Software default selection highlighted in gray.

TABLE 2-128: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

Applicable to Standard Plus I/O Banks

1.2V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	IOH	IOSH	IOSL	IIL [1]	IIH [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Note 1: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

2: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3: Currents are measured at 100°C junction temperature and maximum voltage.

4: Currents are measured at 85°C junction temperature.

5: Software default selection highlighted in gray.

TABLE 2-129: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

Applicable to Standard I/O Banks

1.2V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL [1]	IIH [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
1 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	1	1	20	26	10	10

Note 1: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3: Currents are measured at 100°C junction temperature and maximum voltage.

4: Currents are measured at 85°C junction temperature.

5: Software default selection highlighted in gray.

FIGURE 2-11: AC LOADING

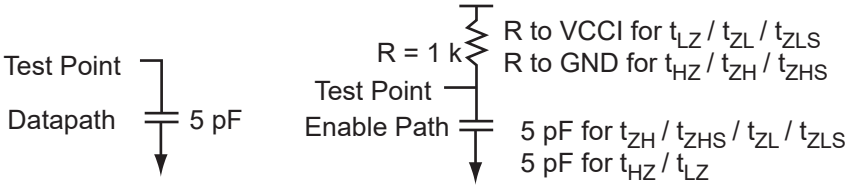


TABLE 2-130: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.2	0.6	5

Note: *Measuring point = Vtrip. See Table 2-29 for a complete table of trip points.

2.6.6.1 Timing Characteristics

2.6.6.1.1 1.2V DC Core Voltage

TABLE 2-131: 1.2V LVCMOS LOW SLEW

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.4V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	8.37	0.26	1.60	1.10	8.04	7.17	3.94	3.52	13.82	12.95	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-132: 1.2V LVCMOS HIGH SLEW

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.14V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.60	0.26	1.60	1.10	3.47	3.36	3.93	3.65	9.26	9.14	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-133: 1.2V LVCMOS HIGH SLEW

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.14V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	7.59	0.26	1.59	1.10	7.29	6.54	3.30	3.35	13.08	12.33	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-134: 1.2V LVCMOS HIGH SLEW

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.14V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-135: 1.2V LVCMOS HIGH SLEW

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.14V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
1 mA	Std.	1.55	8.57	0.26	1.53	1.10	8.23	7.38	2.51	2.39	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-136: 1.2V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 1.14V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
1 mA	Std.	1.55	3.59	0.26	1.53	1.10	3.47	3.06	2.51	2.49	ns

Note 1: Software default selection highlighted in gray.
2: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

2.6.7 1.2V LVCMOS WIDE RANGE

TABLE 2-137: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS FOR LVCMOS 1.2V WIDE RANGE

Applicable to Advanced I/O Banks

1.2V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[1]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Note 1: The minimum drive strength for the default LVCMOS 1.2V software configuration when run in wide range is ± 100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models.

2: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

3: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

4: Currents are measured at 100°C junction temperature and maximum voltage.

5: Currents are measured at 85°C junction temperature.

6: Software default selection highlighted in gray.

TABLE 2-138: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS FOR LVCMOS 1.2V WIDE RANGE

Applicable to Standard Plus I/O Banks

1.2V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[1]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	2mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Note 1: The minimum drive strength for the default LVCMOS 1.2V software configuration when run in wide range is ± 100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models.

2: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

3: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

4: Currents are measured at 100°C junction temperature and maximum voltage.

5: Currents are measured at 85°C junction temperature.

6: Software default selection highlighted in gray.

TABLE 2-139: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS FOR LVCMOS 1.2V WIDE RANGE

Applicable to Standard I/O Banks

1.2V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[1]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	1 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Note 1: The minimum drive strength for the default LVCMOS 1.2V software configuration when run in wide range is ± 100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models.

2: IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3V < VIN < VIL.

3: IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

4: Currents are measured at 100°C junction temperature and maximum voltage.

5: Currents are measured at 85°C junction temperature.

6: Software default selection highlighted in gray.

TABLE 2-140: 1.2V LVCMOS WIDE RANGE AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.2	0.6	5

Note: *Measuring point = Vtrip. See Table 2-29 for a complete table of trip points.

2.6.7.1 Timing Characteristics

Refer to LVCMOS 1.2V (normal range) "Timing Characteristics" on page 2-84 for worst-case timing.

2.6.8 3.3V PCI, 3.3V PCI-X

Peripheral Component Interface for 3.3V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

TABLE 2-141: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

Applicable to Advanced and Standard Plus I/Os

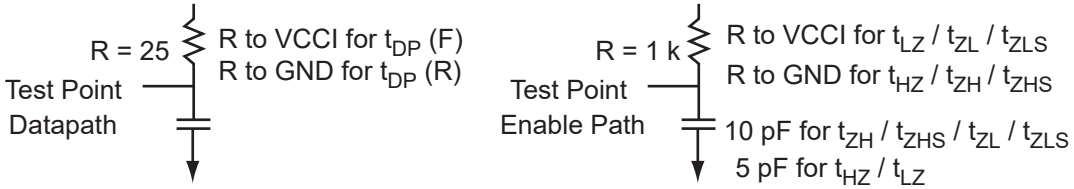
3.3V PCI/PCI-X	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
Per PCI specification	Per PCI curves										10	10

Note 1: Currents are measured at 100°C junction temperature and maximum voltage.

2: Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microchip loadings for enable path characterization are described in Figure 2-12, .

FIGURE 2-12: AC LOADING



AC loadings are defined per PCI/PCI-X specifications for the datapath; Microchip loading for tristate is described in Table 2-142.

TABLE 2-142: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	0.285 * VCCI for $t_{DP(R)}$ 0.615 * VCCI for $t_{DP(F)}$	10

Note: *Measuring point = Vtrip. See Table 2-29 for a complete table of trip points.

2.6.8.1 Timing Characteristics

2.6.8.1.1 1.5V DC Core Voltage

TABLE 2-143: 3.3V PCI/PCI-X
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 3.0V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.97	2.32	0.19	0.70	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-144: 3.3V PCI/PCI-X
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 3.0V
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.97	1.97	0.19	0.70	0.66	2.01	1.50	2.36	2.79	5.61	5.10	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.6.8.1.2 1.2V DC Core Voltage

TABLE 2-145: 3.3V PCI/PCI-X
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 3.0V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.91	0.25	0.86	1.10	2.95	2.29	3.25	3.93	8.74	8.08	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-146: 3.3V PCI/PCI-X

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 3.0V
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.53	0.25	0.85	1.10	2.57	1.98	2.93	3.64	8.35	7.76	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

2.6.9 DIFFERENTIAL I/O CHARACTERISTICS

2.6.10 PHYSICAL IMPLEMENTATION

Configuration of the I/O modules as a differential pair is handled by Microchip Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

2.6.11 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-13, . The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, IGLOO also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

FIGURE 2-13: LVDS CIRCUIT DIAGRAM AND BOARD-LEVEL IMPLEMENTATION

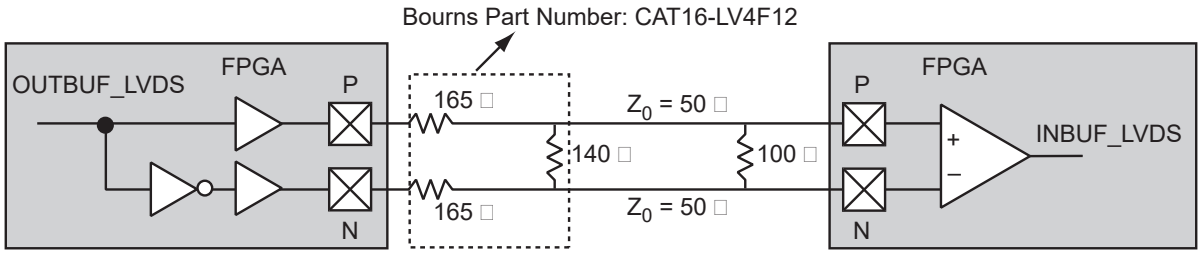


TABLE 2-147: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL[1]	Output Lower Current	0.65	0.91	1.16	mA
IOH[1]	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIH[2]	Input High Leakage Current			10	µA
IIL[2]	Input Low Leakage Current			10	µA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common-Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common-Mode Voltage	0.05	1.25	2.35	V
VIDIFF[4]	Input Differential Voltage	100	350		mV

TABLE 2-147: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

DC Parameter	Description	Min.	Typ.	Max.	Units

Note 1: IOL/IOH is defined by VODIFF/(resistor network)

2: Currents are measured at 85°C junction temperature.

TABLE 2-148: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)
1.075	1.325	Cross point

Note: *Measuring point = Vtrip. See Table 2-29 for a complete table of trip points.

2.6.11.1 Timing Characteristics

2.6.11.1.1 1.5V DC Core Voltage

TABLE 2-149: LVDS – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.3V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.97	1.67	0.19	1.31	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 and Table 2-7 for derating values.

2.6.11.1.2 1.2V DC Core Voltage

TABLE 2-150: LVDS – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 2.3V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	1.55	2.19	0.25	1.52	ns

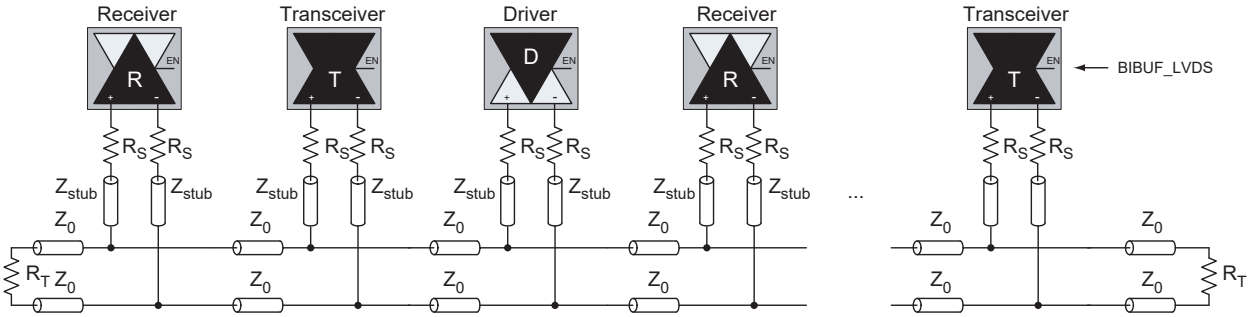
Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 and Table 2-7 for derating values.

2.6.12 B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microchip LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microchip LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-14, . The input and output buffer delays are available in the LVDS section in Table 2-149 and Table 2-150.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and Z_{stub} = 50 Ω (~1.5").

FIGURE 2-14: B-LVDS/M-LVDS MULTIPOINT APPLICATION USING LVDS I/O BUFFERS



2.6.13 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-15, . The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

FIGURE 2-15: LVPECL CIRCUIT DIAGRAM AND BOARD-LEVEL IMPLEMENTATION

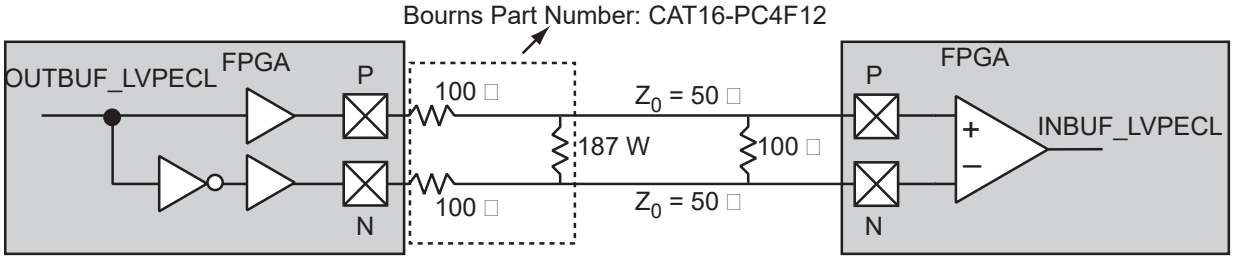


TABLE 2-151: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
V_{ODIFF}	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V_{OCM}	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V_{ICM}	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V_{IDIFF}	Input Differential Voltage	300		300		300		mV

TABLE 2-152: AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input Low (V)	Input High (V)	Measuring Point* (V)
1.64	1.94	Cross point

Note: *Measuring point = Vtrip. See Table 2-28 for a complete table of trip points.

2.6.13.1 Timing Characteristics

2.6.13.1.1 1.5V DC Core Voltage

TABLE 2-153: LVPECL – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 3.0V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.97	1.67	0.19	1.16	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.6.13.1.2 1.2V DC Core Voltage

TABLE 2-154: LVPECL – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 3.0V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	1.55	2.24	0.25	1.37	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

2.7 I/O Register Specifications

2.7.1 FULLY REGISTERED I/O BUFFERS WITH SYNCHRONOUS ENABLE AND D ASYNCHRONOUS PRESET

FIGURE 2-16: TIMING MODEL OF REGISTERED I/O BUFFERS WITH SYNCHRONOUS ENABLE AND ASYNCHRONOUS PRESET

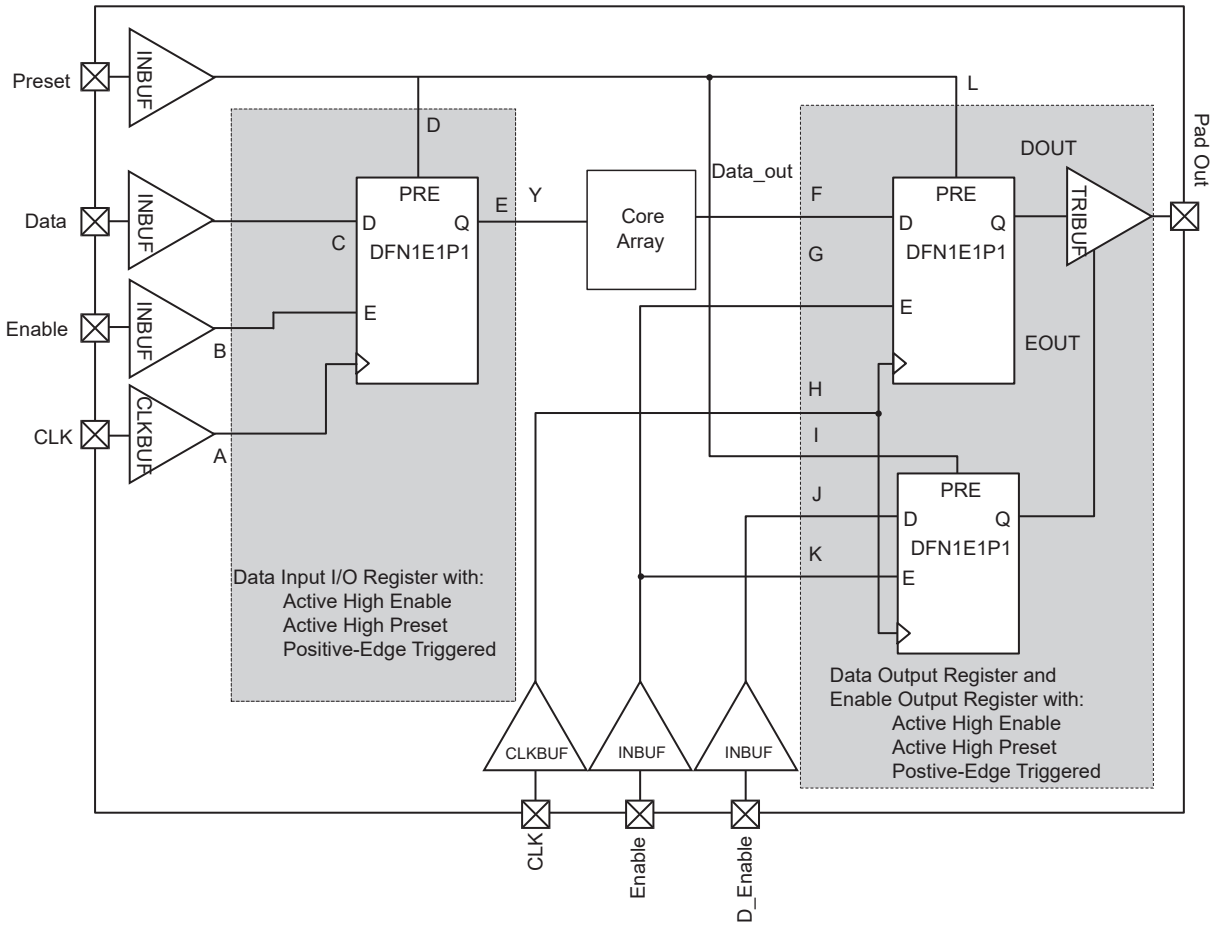


TABLE 2-155: PARAMETER DEFINITION AND MEASURING NODES

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H

TABLE 2-155: PARAMETER DEFINITION AND MEASURING NODES

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: *See Figure 2-16, for more information.

2.7.2 FULLY REGISTERED I/O BUFFERS WITH SYNCHRONOUS ENABLE AND ASYNCHRONOUS CLEAR

FIGURE 2-17: TIMING MODEL OF THE REGISTERED I/O BUFFERS WITH SYNCHRONOUS ENABLE AND ASYNCHRONOUS CLEAR

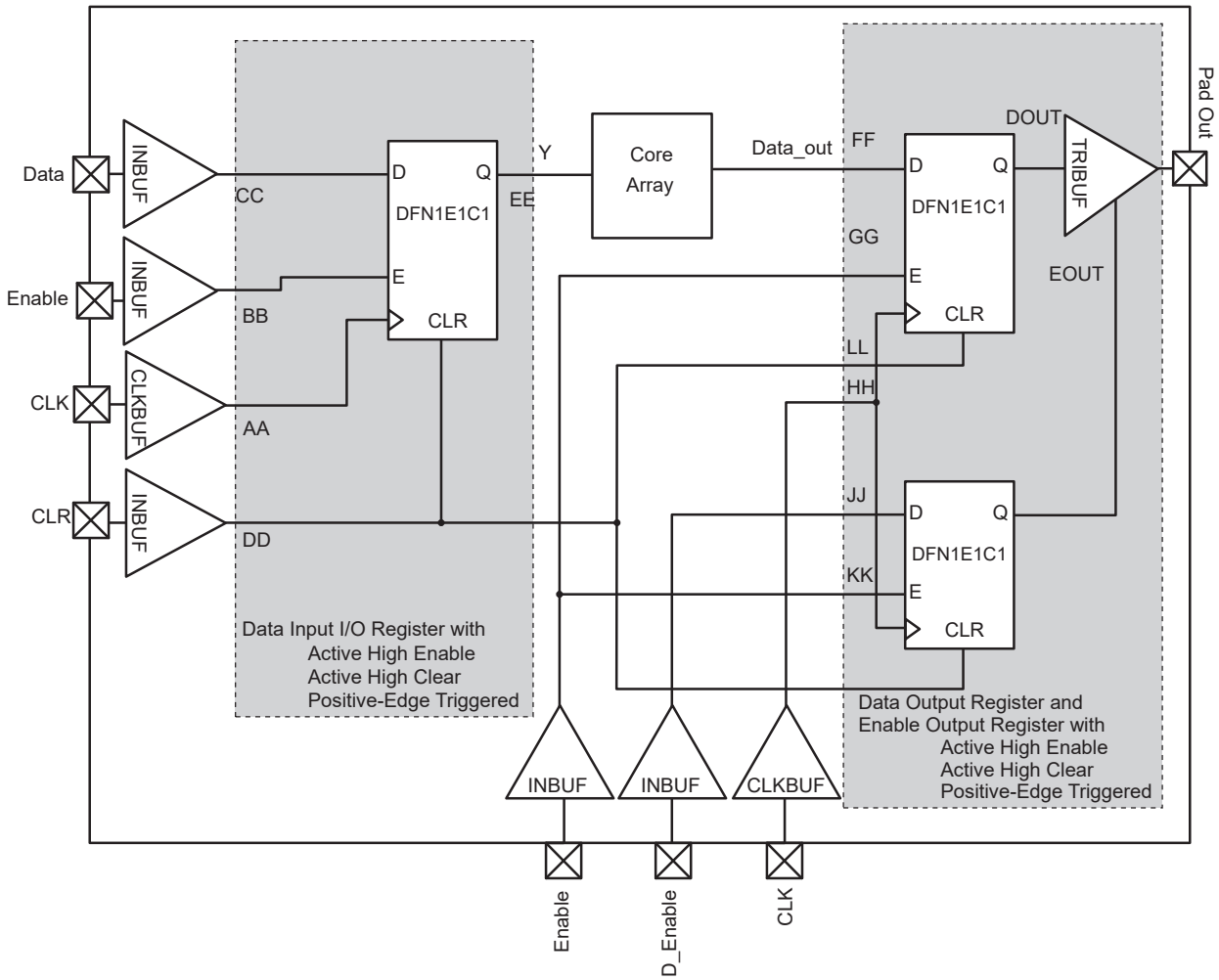


TABLE 2-156: PARAMETER DEFINITION AND MEASURING NODES

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH

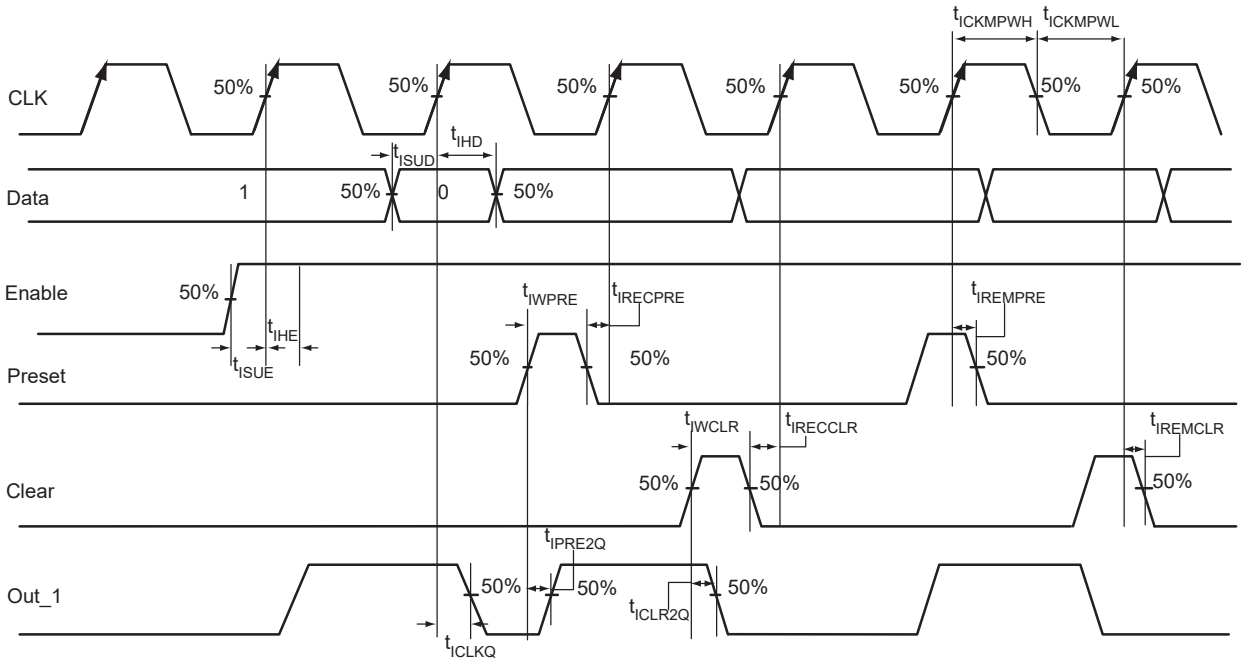
TABLE 2-156: PARAMETER DEFINITION AND MEASURING NODES

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

Note: *See Figure 2-17, for more information.

2.7.3 INPUT REGISTER

FIGURE 2-18: INPUT REGISTER TIMING DIAGRAM



2.7.3.1 Timing Characteristics

2.7.3.1.1 1.5V DC Core Voltage

TABLE 2-157: INPUT DATA REGISTER PROPAGATION DELAYS

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.42	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.47	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.67	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.79	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.79	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.7.3.1.2 1.2V DC Core Voltage

TABLE 2-158: INPUT DATA REGISTER PROPAGATION DELAYS

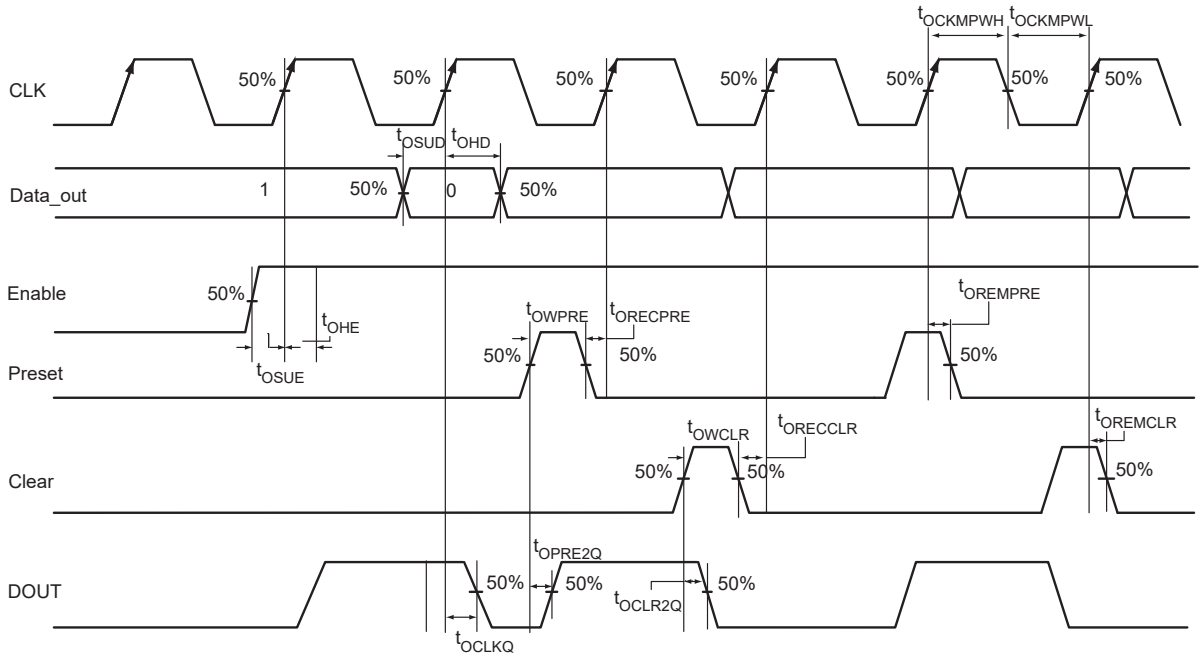
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.68	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.97	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	1.02	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	1.19	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	1.19	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

2.7.4 OUTPUT REGISTER

FIGURE 2-19: OUTPUT REGISTER TIMING DIAGRAM



2.7.4.1 Timing Characteristics

2.7.4.1.1 1.5V DC Core Voltage

TABLE 2-159: OUTPUT DATA REGISTER PROPAGATION DELAYS

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.00	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.51	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.70	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.34	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.34	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.7.4.1.2 1.2V DC Core Voltage

TABLE 2-160: OUTPUT DATA REGISTER PROPAGATION DELAYS

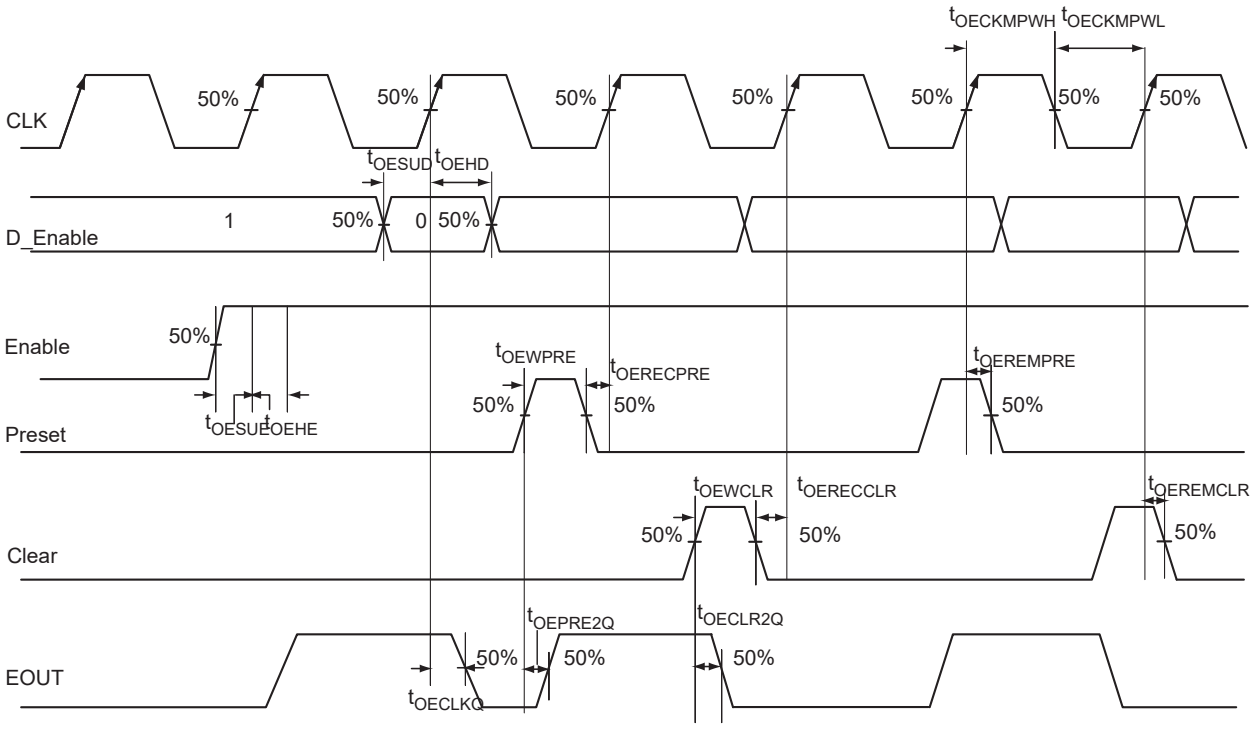
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.52	ns
t_{OSUD}	Data Setup Time for the Output Data Register	1.15	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	1.11	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.96	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.96	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

2.7.5 OUTPUT ENABLE REGISTER

FIGURE 2-20: OUTPUT ENABLE REGISTER TIMING DIAGRAM



2.7.5.1 Timing Characteristics

2.7.5.1.1 1.5V DC Core Voltage

TABLE 2-161: OUTPUT ENABLE REGISTER PROPAGATION DELAYS

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.75	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.51	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.73	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.13	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.13	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.7.5.1.2 1.2V DC Core Voltage

TABLE 2-162: OUTPUT ENABLE REGISTER PROPAGATION DELAYS

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	1.10	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	1.15	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	1.22	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.65	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.65	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

2.8 DDR Module Specifications

2.8.1 INPUT DDR MODULE

FIGURE 2-21: INPUT DDR TIMING MODEL

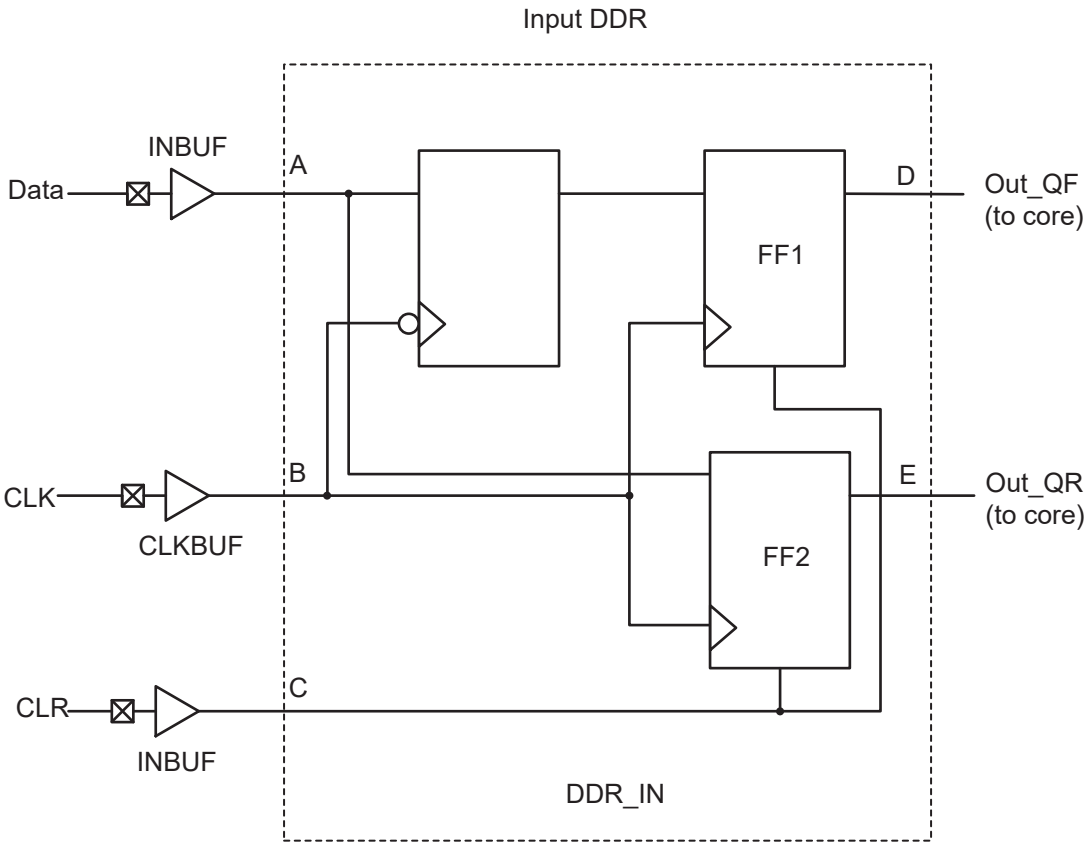
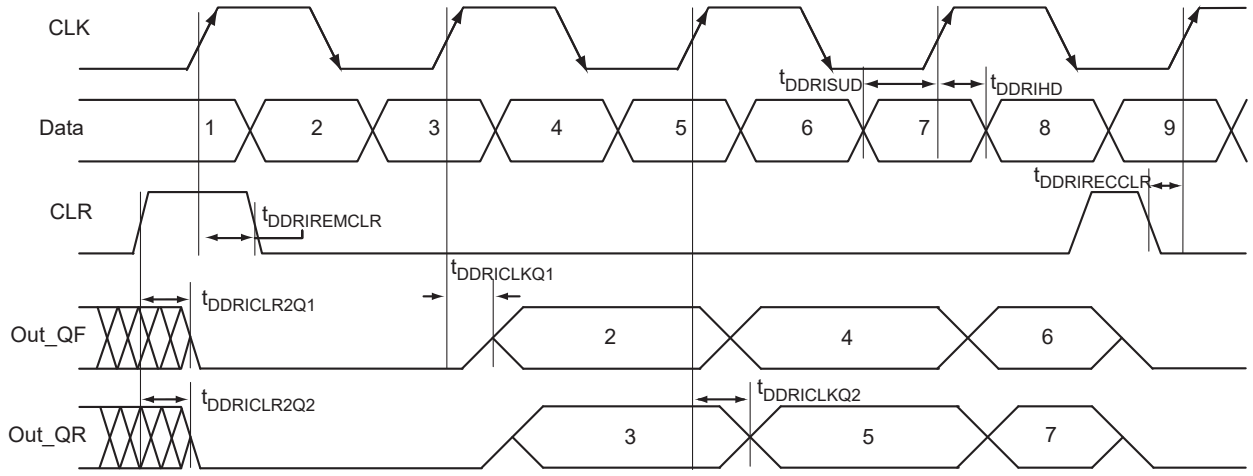


TABLE 2-163: PARAMETER DEFINITIONS

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

FIGURE 2-22: INPUT DDR TIMING DIAGRAM



2.8.1.1 Timing Characteristics

2.8.1.1.1 1.5V DC Core Voltage

TABLE 2-164: INPUT DDR PROPAGATION DELAYS

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V

Parameter	Description	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.48	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.65	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (negedge)	0.50	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (posedge)	0.40	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (negedge)	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (posedge)	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.82	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.98	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.23	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

2.8.1.1.2 1.2V DC Core Voltage

TABLE 2-165: INPUT DDR PROPAGATION DELAYS

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V

Parameter	Description	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.76	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.94	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (negedge)	0.93	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (posedge)	0.84	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-165: INPUT DDR PROPAGATION DELAYS

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V

Parameter	Description	Std.	Units
$t_{DDRIHD1}$	Data Hold for Input DDR (negedge)	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (posedge)	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	1.23	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	1.42	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.24	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	160.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

2.8.2 OUTPUT DDR MODULE

FIGURE 2-23: OUTPUT DDR TIMING MODEL

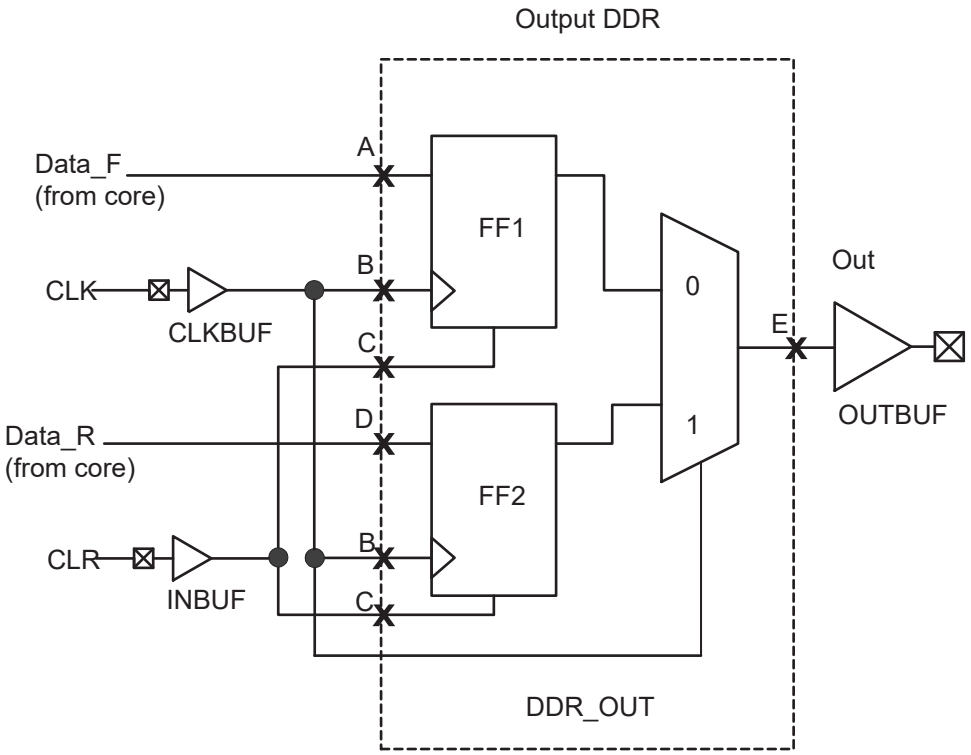


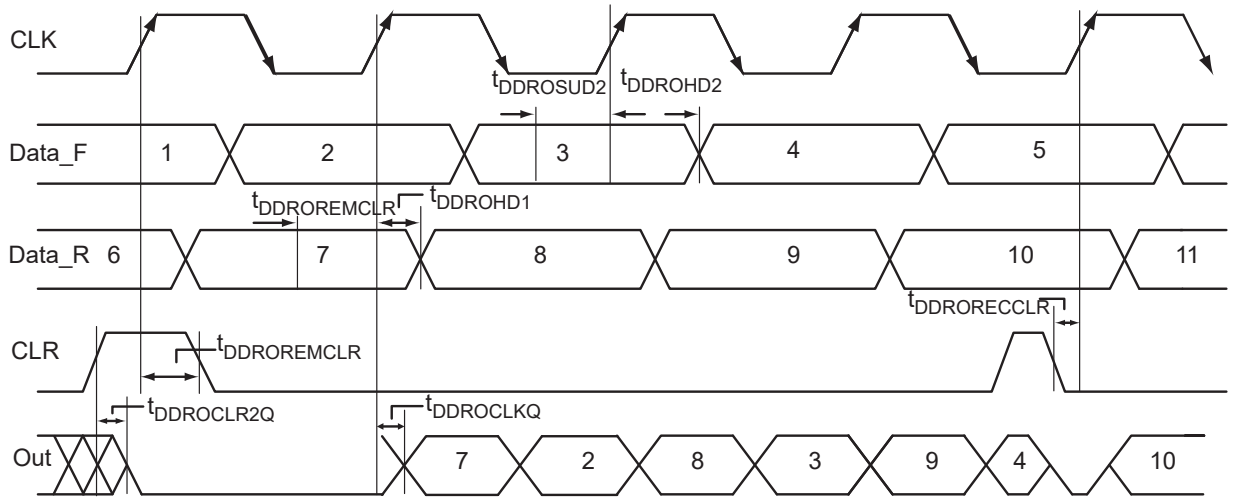
TABLE 2-166: PARAMETER DEFINITIONS

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B

TABLE 2-166: PARAMETER DEFINITIONS

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

FIGURE 2-24: OUTPUT DDR TIMING DIAGRAM



2.8.2.1 Timing Characteristics

2.8.2.1.1 1.5V DC Core Voltage

TABLE 2-167: OUTPUT DDR PROPAGATION DELAYS

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.07	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.67	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.67	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.38	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.8.2.1.2 1.2V DC Core Voltage

TABLE 2-168: OUTPUT DDR PROPAGATION DELAYS

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.60	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	1.09	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	1.16	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.99	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.24	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	160.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

2.9 VersaTile Characteristics

2.9.1 VERSATILE SPECIFICATIONS AS A COMBINATORIAL MODULE

The IGLOO library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

FIGURE 2-25: SAMPLE OF COMBINATORIAL CELLS

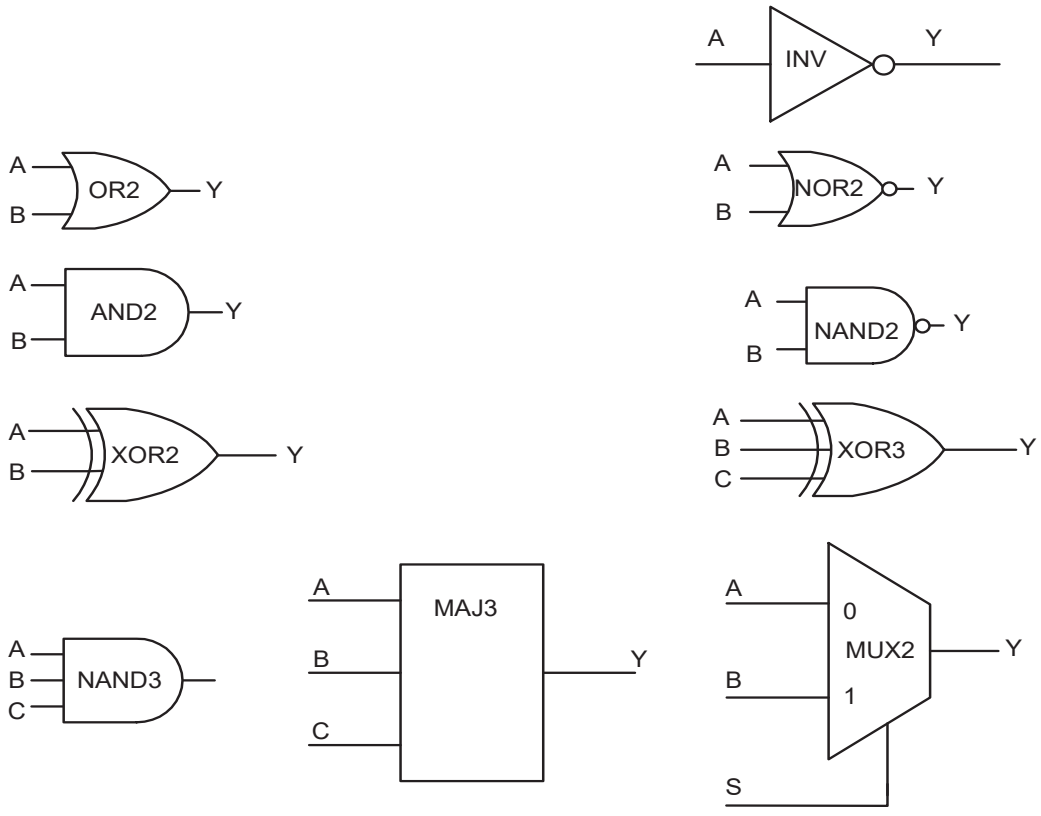
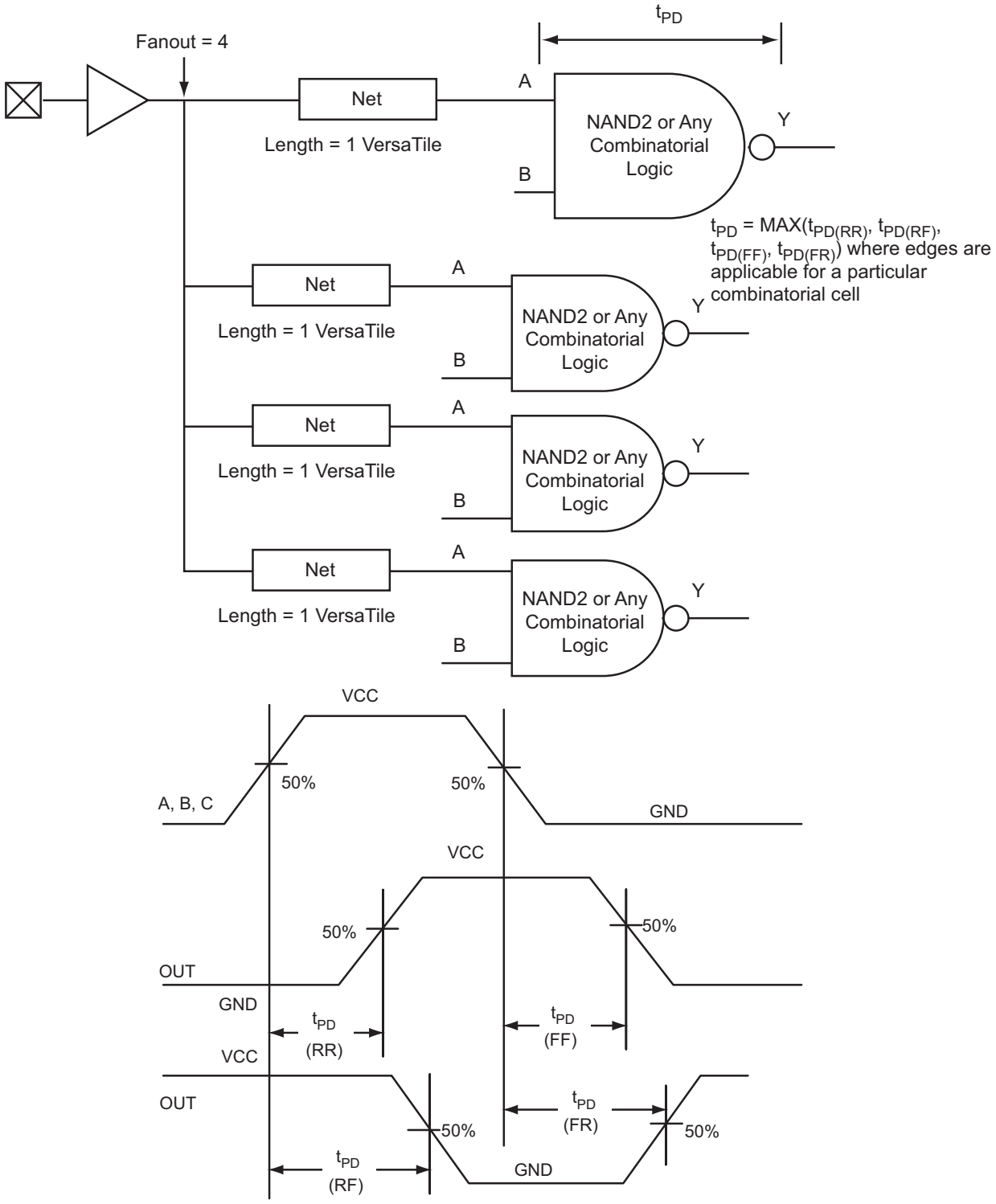


FIGURE 2-26: TIMING MODEL AND WAVEFORMS



2.9.2 TIMING CHARACTERISTICS

2.9.2.1 1.5V DC Core Voltage

TABLE 2-169: COMBINATORIAL CELL PROPAGATION DELAYS

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y =!A	t_{PD}	0.80	ns
AND2	Y = A · B	t_{PD}	0.84	ns
NAND2	Y =!(A · B)	t_{PD}	0.90	ns
OR2	Y = A + B	t_{PD}	1.19	ns
NOR2	Y = !(A + B)	t_{PD}	1.10	ns
XOR2	Y = A ⊕ B	t_{PD}	1.37	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	1.33	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.79	ns
MUX2	Y = A !S + B S	t_{PD}	1.48	ns
AND3	Y = A · B · C	t_{PD}	1.21	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.9.2.2 1.2V DC Core Voltage

TABLE 2-170: COMBINATORIAL CELL PROPAGATION DELAYS

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	1.34	ns
AND2	Y = A · B	t_{PD}	1.43	ns
NAND2	Y = !(A · B)	t_{PD}	1.59	ns
OR2	Y = A + B	t_{PD}	2.30	ns
NOR2	Y = !(A + B)	t_{PD}	2.07	ns
XOR2	Y = A ⊕ B	t_{PD}	2.46	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	2.46	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	3.12	ns
MUX2	Y = A !S + B S	t_{PD}	2.83	ns
AND3	Y = A · B · C	t_{PD}	2.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

2.9.3 VERSATILE SPECIFICATIONS AS A SEQUENTIAL MODULE

The IGLOO library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

FIGURE 2-27: SAMPLE OF SEQUENTIAL CELLS

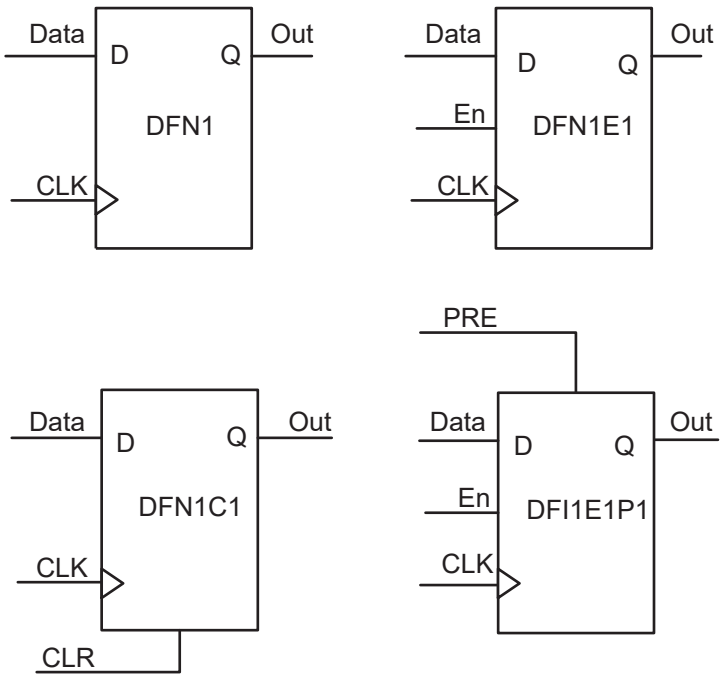
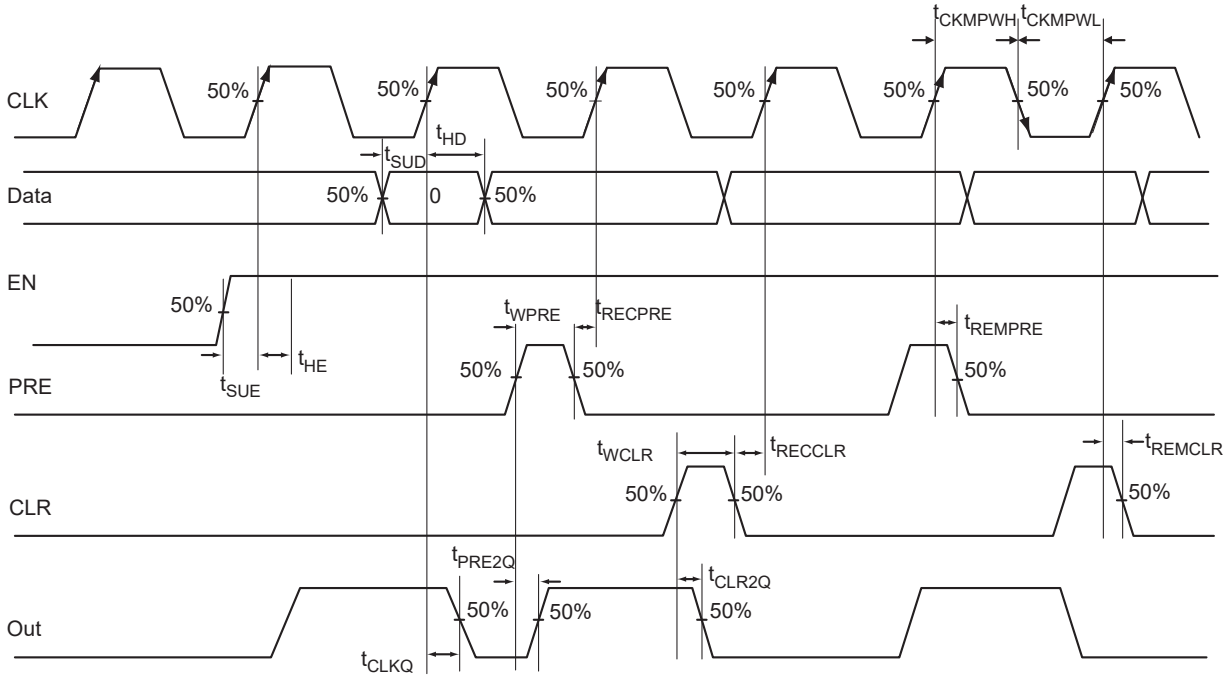


FIGURE 2-28: TIMING MODEL AND WAVEFORMS



2.9.4 TIMING CHARACTERISTICS

2.9.4.1 1.5V DC Core Voltage

TABLE 2-171: REGISTER DELAYS

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.89	ns
t_{SUD}	Data Setup Time for the Core Register	0.81	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.60	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.62	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.56	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.9.4.2 1.2V DC Core Voltage

TABLE 2-172: REGISTER DELAYS

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	1.61	ns
t_{SUD}	Data Setup Time for the Core Register	1.17	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	1.29	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.87	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.89	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.46	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.46	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.95	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.95	ns

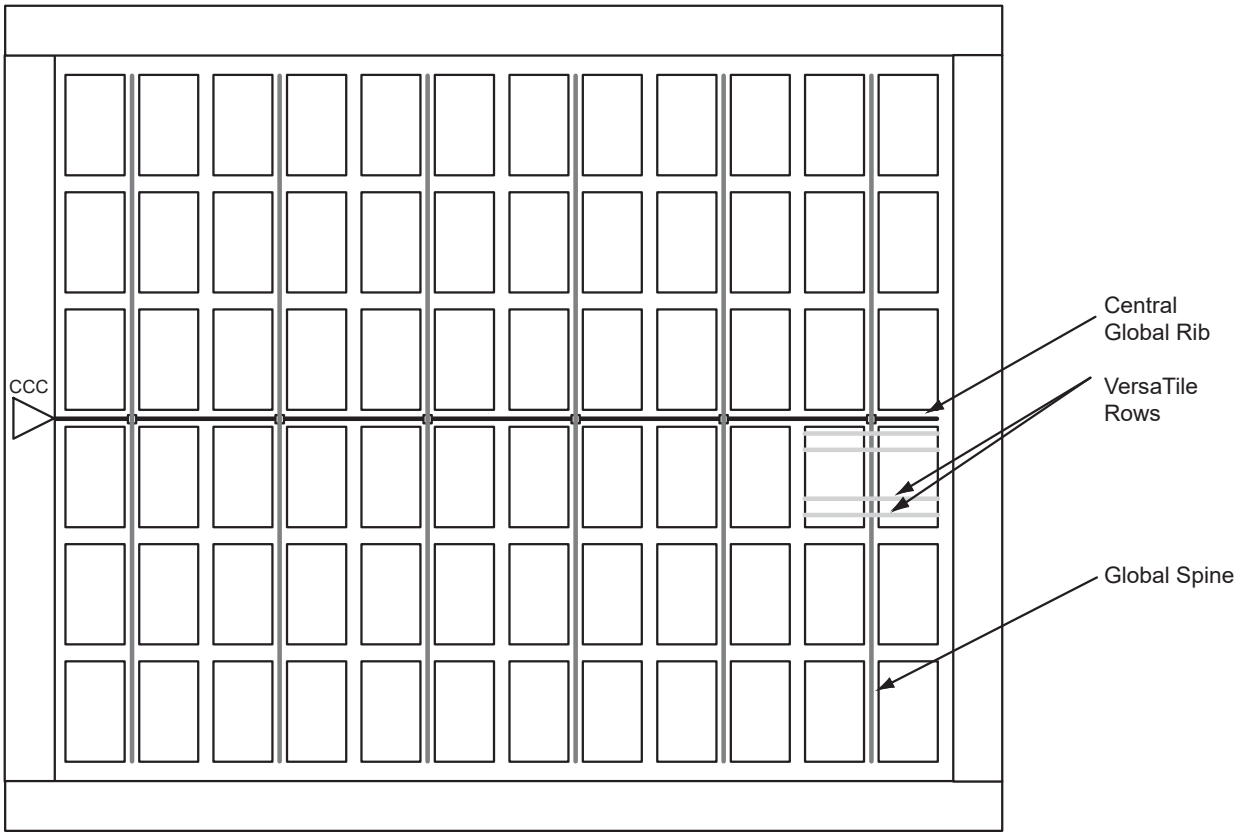
Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

2.10 Global Resource Characteristics

2.10.1 AGL250 CLOCK TREE TOPOLOGY

Clock delays are device-specific. Figure 2-29, is an example of a global tree used for clock routing. The global tree presented in Figure 2-29, is driven by a CCC located on the west side of the AGL250 device. It is used to drive all D-flip-flops in the device.

FIGURE 2-29: EXAMPLE OF GLOBAL TREE USE IN AN AGL250 DEVICE FOR CLOCK ROUTING



2.10.2 GLOBAL TREE TIMING CHARACTERISTICS

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-116. Table 2-173 to Table 2-188 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

2.10.2.1 Timing Characteristics

2.10.2.1.1 1.5V DC Core Voltage

TABLE 2-173: AGL015 GLOBAL RESOURCE
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns

TABLE 2-173: AGL015 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.425V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-174: AGL030 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.425V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-175: AGL060 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.425V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.33	1.55	ns
t_{RCKH}	Input High Delay for Global Clock	1.35	1.62	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-176: AGL125 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.425V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.36	1.71	ns
t_{RCKH}	Input High Delay for Global Clock	1.39	1.82	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-177: AGL250 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.425V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.39	1.73	ns
t_{RCKH}	Input High Delay for Global Clock	1.41	1.84	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-178: AGL400 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.425V

Parameter	Description	Std.		Units
		Min. [1]	Max. [2]	
t_{RCKL}	Input Low Delay for Global Clock	1.45	1.79	ns
t_{RCKH}	Input High Delay for Global Clock	1.48	1.91	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage-supply levels, refer to Table 2-6 for derating values.

TABLE 2-179: AGL600 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.425V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.48	1.82	ns
t_{RCKH}	Input High Delay for Global Clock	1.52	1.94	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.42	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-180: AGL1000 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.425V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.55	1.89	ns
t_{RCKH}	Input High Delay for Global Clock	1.60	2.02	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.42	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.10.2.1.2 1.2V DC Core Voltage

TABLE 2-181: AGL015 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.14V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.79	2.09	ns
t_{RCKH}	Input High Delay for Global Clock	1.87	2.26	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.39	ns

TABLE 2-181: AGL015 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.14V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-182: AGL030 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.14V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.80	2.09	ns
t_{RCKH}	Input High Delay for Global Clock	1.88	2.27	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.39	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-183: AGL060 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.14V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.04	2.33	ns
t_{RCKH}	Input High Delay for Global Clock	2.10	2.51	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.40	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-184: AGL125 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.14V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.08	2.54	ns

TABLE 2-184: AGL125 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.14V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKH}	Input High Delay for Global Clock	2.15	2.77	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-185: AGL250 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.14V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.11	2.57	ns
t_{RCKH}	Input High Delay for Global Clock	2.19	2.81	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-186: AGL400 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.14V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.18	2.64	ns
t_{RCKH}	Input High Delay for Global Clock	2.27	2.89	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-187: AGL600 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.14V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.22	2.67	ns
t_{RCKH}	Input High Delay for Global Clock	2.32	2.93	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-188: AGL1000 GLOBAL RESOURCE

Commercial-Case Conditions: T_J = 70°C, VCC = 1.14V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.31	2.76	ns
t_{RCKH}	Input High Delay for Global Clock	2.42	3.03	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.11 Clock Conditioning Circuits

2.11.1 CCC ELECTRICAL SPECIFICATIONS

2.11.1.1 Timing Characteristics

TABLE 2-189: IGLOO CCC/PLL SPECIFICATION

For IGLOO V2 or V5 Devices, 1.5V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		250	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		360[3]		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[4, 5]			100	ns
Input Cycle-to-Cycle Jitter (peak magnitude)			1	ns

TABLE 2-189: IGLOO CCC/PLL SPECIFICATION

For IGLOO V2 or V5 Devices, 1.5V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[6]				
LockControl = 0			2.5	ns
LockControl = 1			1.5	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	1.25		15.65	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.469		15.65	ns
Delay Range in Block: Fixed Delay [1, 2]		3.5		ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Maximum Peak-to-Peak Jitter Data[7]			
	SSO ≥ 4[8]	SSO ≥ 8[8]	SSO ≥ 16[8]	
0.75 MHz to 50 MHz	0.60%	0.80%	1.20%	
50 MHz to 160 MHz	4.00%	6.00%	12.00%	

Note 1: This delay is a function of voltage and temperature. See Table 2-6 and Table 2-7 for deratings.

2: T_J = 25°C, V_{CC} = 1.5V

3: When the CCC/PLL core is generated by Microchip core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.

4: The AGL030 device does not support a PLL.

5: Maximum value obtained for a Std. speed grade device in Worst-Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

6: Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.

7: Measurements done with LVTTL 3.3V, 8 mA I/O drive strength, and high slew Rate. VCC/VCCPLL = 1.14V, VQ/PQ/TQ type of packages, 20 pF load.

8: Simultaneously Switching Outputs (SSOs) are outputs that are synchronous to a single clock domain and have clock-to-out times that are within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the *IGLOO FPGA Fabric User Guide*.

TABLE 2-190: IGLOO CCC/PLL SPECIFICATION

For IGLOO V2 Devices, 1.2V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		160	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		160	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		580[3]		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[4,5]			60	ns
Input Cycle-to-Cycle Jitter (peak magnitude)			0.25	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[6]				

TABLE 2-190: IGLOO CCC/PLL SPECIFICATION

For IGLOO V2 Devices, 1.2V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
LockControl = 0			4	ns
LockControl = 1			3	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1[1,2]	2.3		20.86	ns
Delay Range in Block: Programmable Delay 2[1,2]	0.863		20.86	ns
Delay Range in Block: Fixed Delay [1, 2, 5]		5.7		ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Maximum Peak-to-Peak Jitter Data[7,8]			
	SSO ≥ 4[9]	SSO ≥ 8[9]	SSO ≥ 16[9]	
0.75 MHz to 50 MHz	1.20%	2.00%	3.00%	
50 MHz to 160 MHz	5.00%	7.00%	15.00%	

Note 1: This delay is a function of voltage and temperature. See Table 2-6 and Table 2-7 for deratings.

2: T_J = 25°C, V_{CC} = 1.2V

3: When the CCC/PLL core is generated by Microchip core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.

4: Maximum value obtained for a Std. speed grade device in Worst-Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

5: The AGL030 device does not support a PLL.

6: Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.

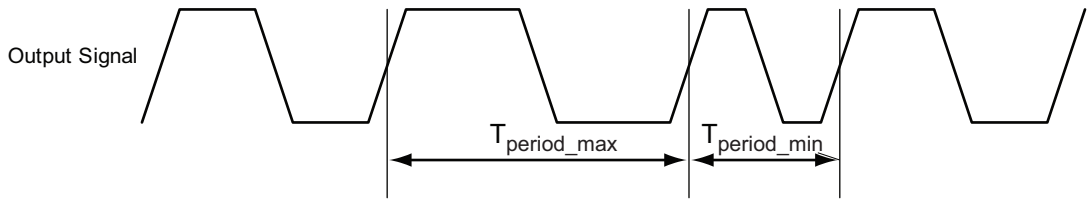
7: VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the per cent jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.

8: Measurements done with LVTTL 3.3V, 8 mA I/O drive strength, and high slew Rate. VCC/VCCPLL = 1.14V, VQ/PQ/TQ type of packages, 20 pF load.

9: SSO are outputs that are synchronous to a single clock domain and have clock-to-out times that are within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the *IGLOO FPGA Fabric User Guide*.

10: For definitions of Type 1 and Type 2, refer to the PLL Block Diagram in the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the *GLOO FPGA Fabric User Guide*.

FIGURE 2-30: PEAK-TO-PEAK JITTER DEFINITION

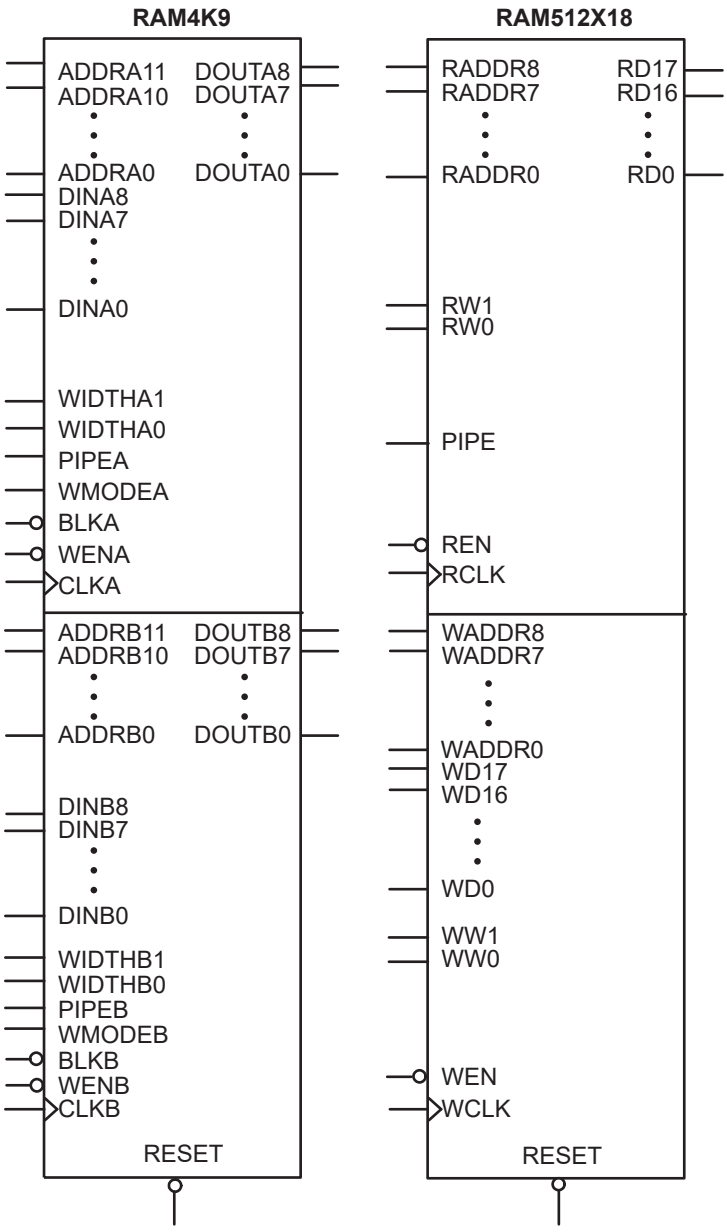


Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

2.12 Embedded SRAM and FIFO Characteristics

2.12.1 SRAM

FIGURE 2-31: RAM MODELS



2.12.2 TIMING WAVEFORMS

FIGURE 2-32: RAM READ FOR PASS-THROUGH OUTPUT. APPLICABLE TO BOTH RAM4K9 AND RAM512X18.

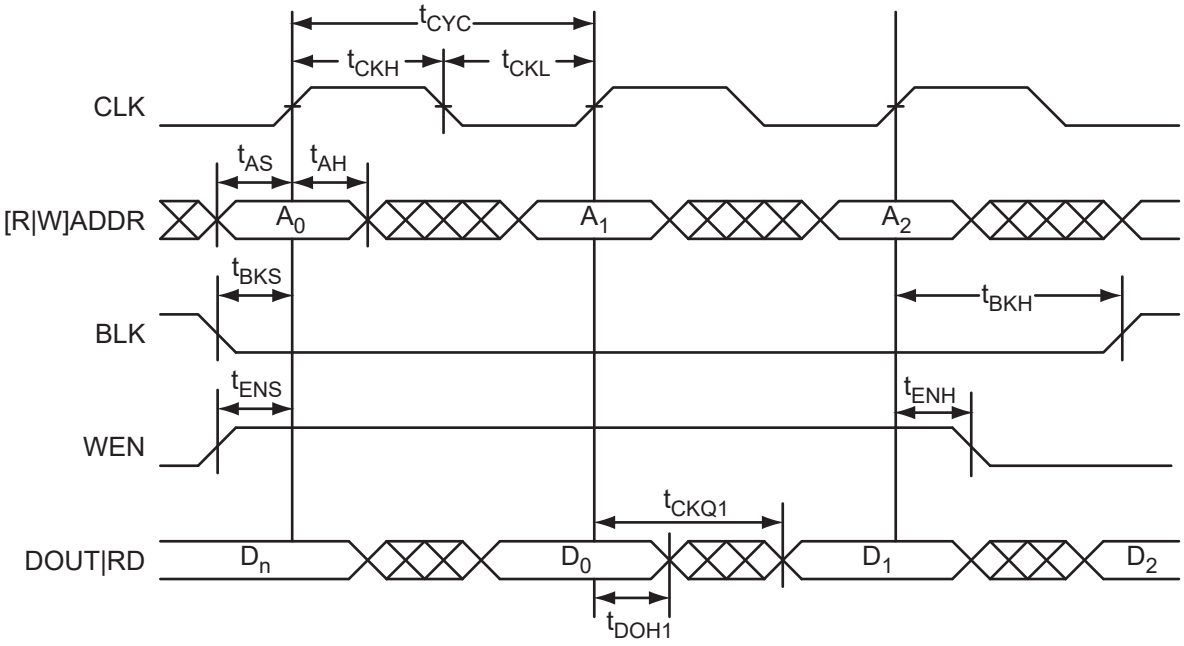


FIGURE 2-33: RAM READ FOR PIPELINED OUTPUT. APPLICABLE TO BOTH RAM4K9 AND RAM512X18.

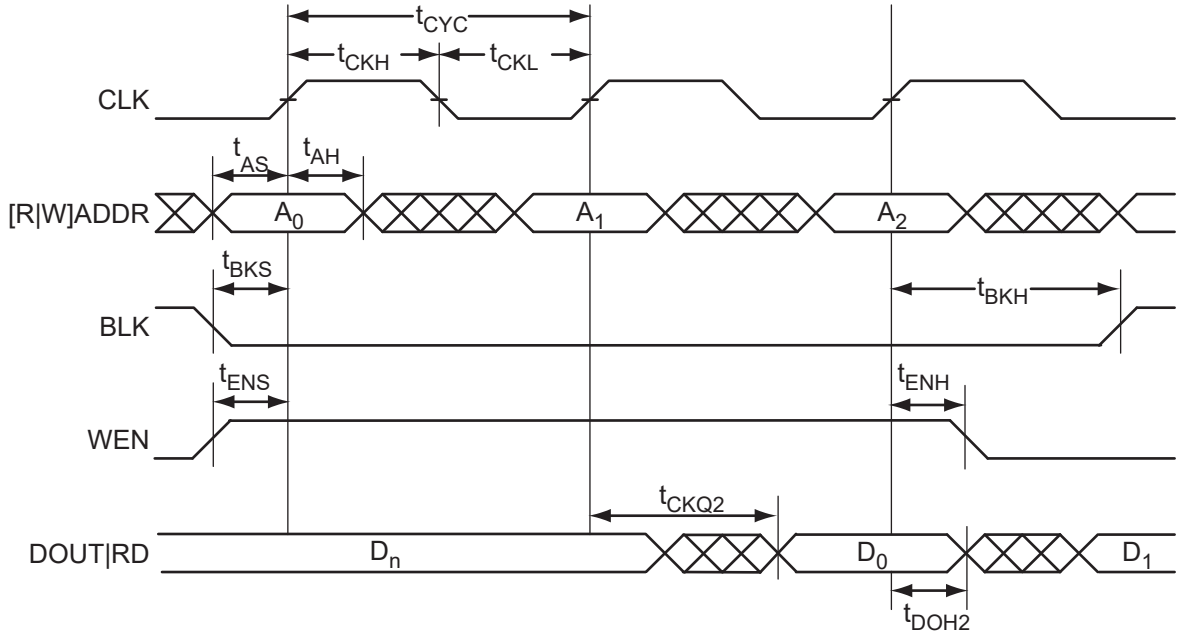


FIGURE 2-34: RAM WRITE, OUTPUT RETAINED. APPLICABLE TO BOTH RAM4K9 AND RAM512X18.

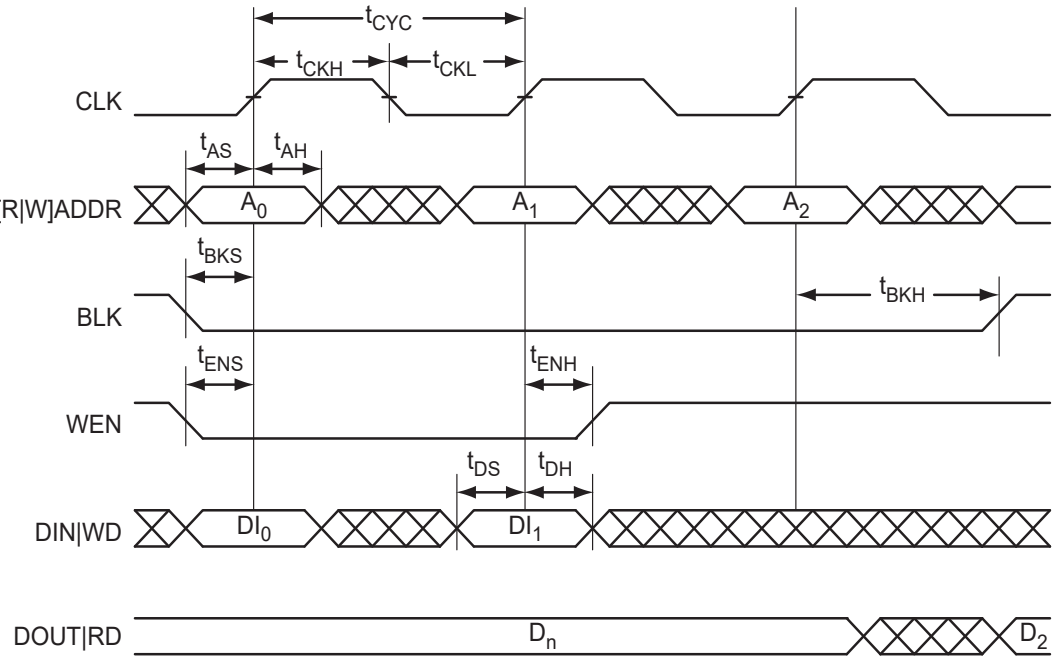


FIGURE 2-35: RAM WRITE, OUTPUT AS WRITE DATA (WMODE = 1). APPLICABLE TO RAM4K9 ONLY.

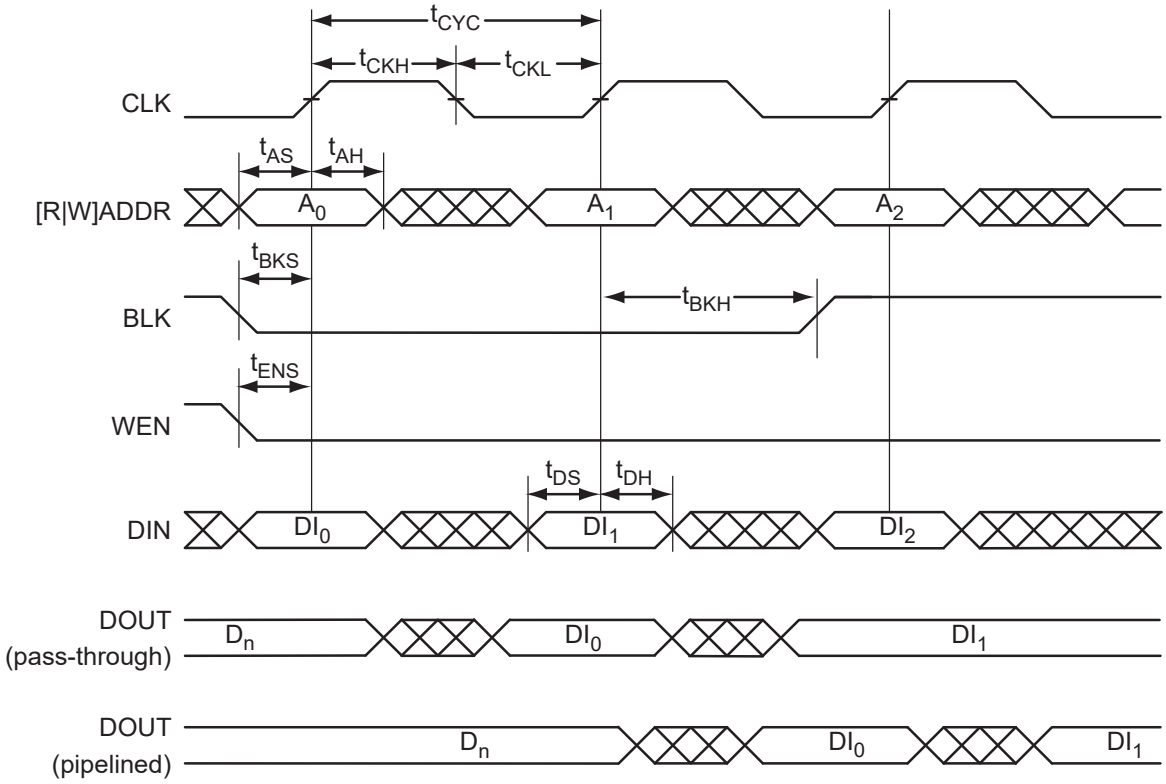
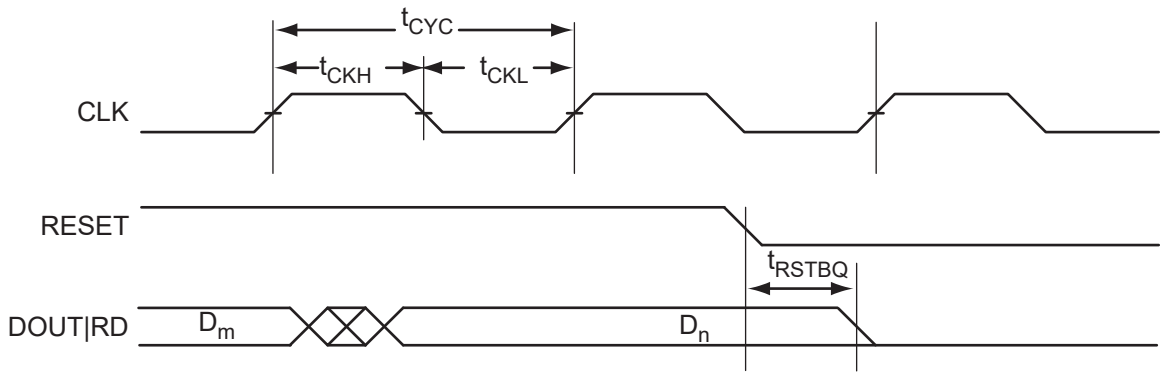


FIGURE 2-36: RAM RESET. APPLICABLE TO BOTH RAM4K9 AND RAM512X18.



2.12.3 TIMING CHARACTERISTICS

2.12.3.1 1.5V DC Core Voltage

TABLE 2-191: RAM4K9

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.83	ns
t_{AH}	Address hold time	0.16	ns
t_{ENS}	REN, WEN setup time	0.81	ns
t_{ENH}	REN, WEN hold time	0.16	ns
t_{BKS}	BLK setup time	1.65	ns
t_{BKH}	BLK hold time	0.16	ns
t_{DS}	Input data (DIN) setup time	0.71	ns
t_{DH}	Input data (DIN) hold time	0.36	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	3.53	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	3.06	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	1.81	ns
t_{C2CWWL} [1]	Address collision clk-to-clk delay for reliable write after write on same address – Applicable to Closing Edge	0.23	ns
t_{C2CRWL} [1]	Address collision clk-to-clk delay for reliable read access after write on same address – Applicable to Opening Edge	0.35	ns
t_{C2CWRH} [1]	Address collision clk-to-clk delay for reliable write access after read on same address – Applicable to Opening Edge	0.41	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	2.06	ns
	RESET Low to data out Low on DOUT (pipelined)	2.06	ns
$t_{REMRSTB}$	RESET removal	0.61	ns
$t_{RECRSTB}$	RESET recovery	3.21	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Note 1: For more information, refer to the application note *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-192: RAM512X18

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.83	ns
t_{AH}	Address hold time	0.16	ns
t_{ENS}	REN, WEN setup time	0.73	ns
t_{ENH}	REN, WEN hold time	0.08	ns
t_{DS}	Input data (WD) setup time	0.71	ns
t_{DH}	Input data (WD) hold time	0.36	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	4.21	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	1.71	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address - Applicable to Opening Edge	0.35	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address - Applicable to Opening Edge	0.42	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	2.06	ns
	RESET Low to data out Low on RD (pipelined)	2.06	ns
$t_{REMRSTB}$	RESET removal	0.61	ns
$t_{RECRSTB}$	RESET recovery	3.21	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Note 1: For more information, refer to the *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs Application Note*.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.12.3.2 1.2V DC Core Voltage

TABLE 2-193: RAM4K9

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.53	ns
t_{AH}	Address hold time	0.29	ns
t_{ENS}	REN WEN setup time	1.50	ns
t_{ENH}	REN, WEN hold time	0.29	ns
t_{BKS}	BLK setup time	3.05	ns
t_{BKH}	BLK hold time	0.29	ns
t_{DS}	Input data (DIN) setup time	1.33	ns
t_{DH}	Input data (DIN) hold time	0.66	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	6.61	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	5.72	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	3.38	ns

Note 1: For more information, refer to the *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs Application Note*.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-193: RAM4K9

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V

Parameter	Description	Std.	Units
t_{C2CWWL}[1]	Address collision clk-to-clk delay for reliable write after write on same address –Applicable to Closing Edge	0.30	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address – Applicable to Opening Edge	0.89	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address – Applicable to Opening Edge	1.01	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	3.86	ns
	RESET Low to data out Low on DOUT (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET removal	1.12	ns
$t_{RECRSTB}$	RESET recovery	5.93	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Note 1: For more information, refer to the *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs Application Note*.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-194: RAM512X18

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14V

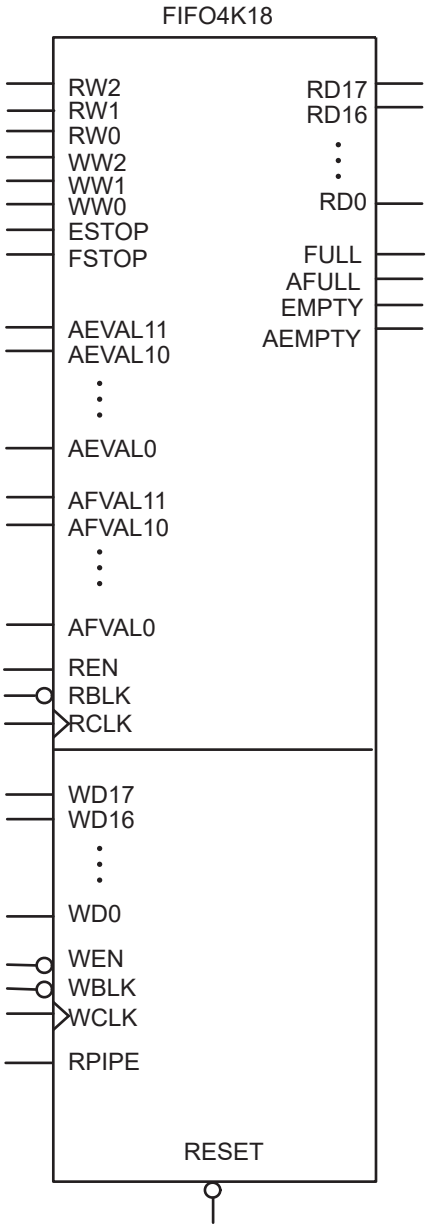
Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.53	ns
t_{AH}	Address hold time	0.29	ns
t_{ENS}	REN, WEN setup time	1.36	ns
t_{ENH}	REN, WEN hold time	0.15	ns
t_{DS}	Input data (WD) setup time	1.33	ns
t_{DH}	Input data (WD) hold time	0.66	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	7.88	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	3.20	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address – Applicable to Opening Edge	0.87	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address – Applicable to Opening Edge	1.04	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow through)	3.86	ns
	RESET Low to data out Low on RD (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET removal	1.12	ns
$t_{RECRSTB}$	RESET recovery	5.93	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Note 1: For more information, refer to the application note *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.

2: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.12.4 FIFO

FIGURE 2-37: FIFO MODEL



2.12.5 TIMING WAVEFORMS

FIGURE 2-38: FIFO READ

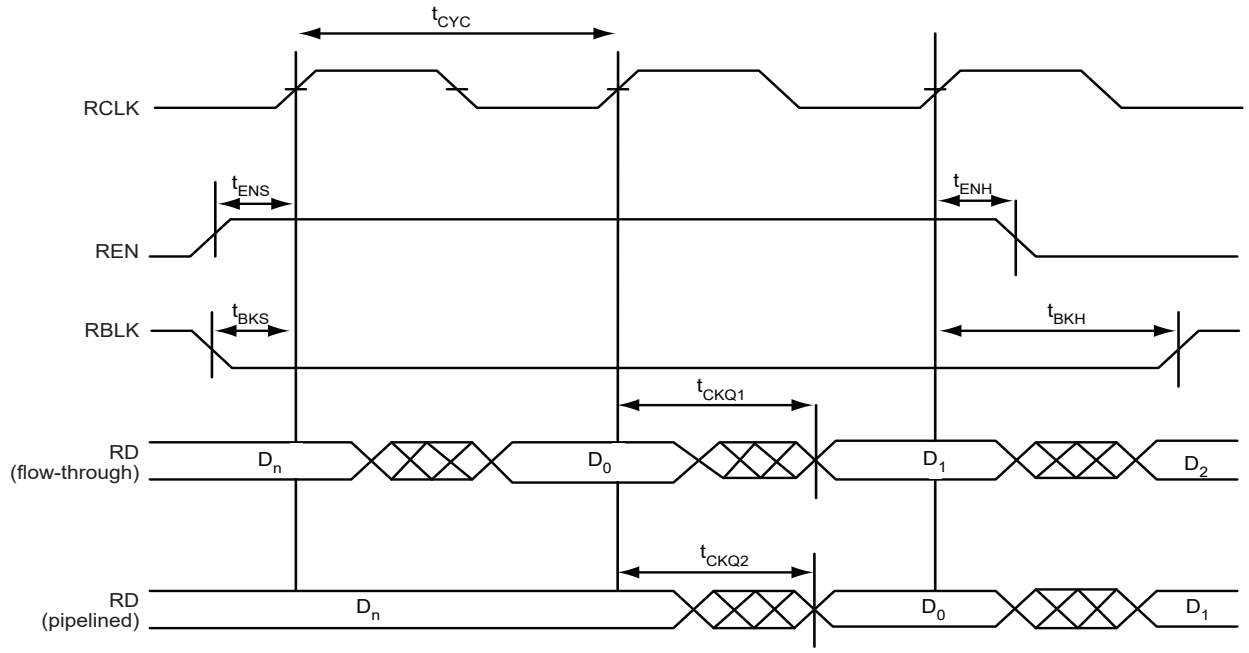


FIGURE 2-39: FIFO WRITE

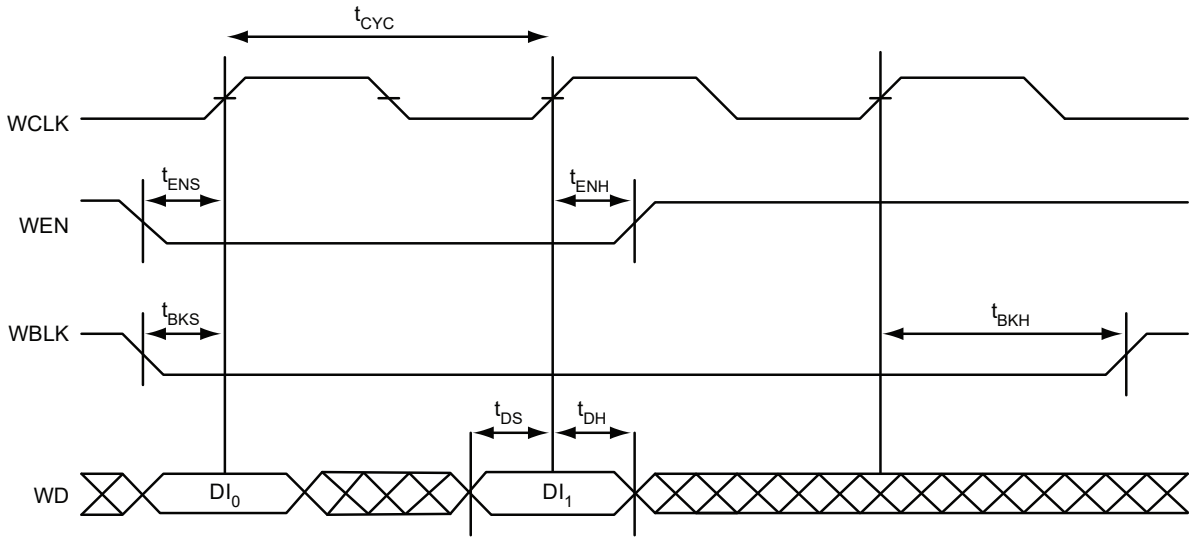


FIGURE 2-40: FIFO RESET

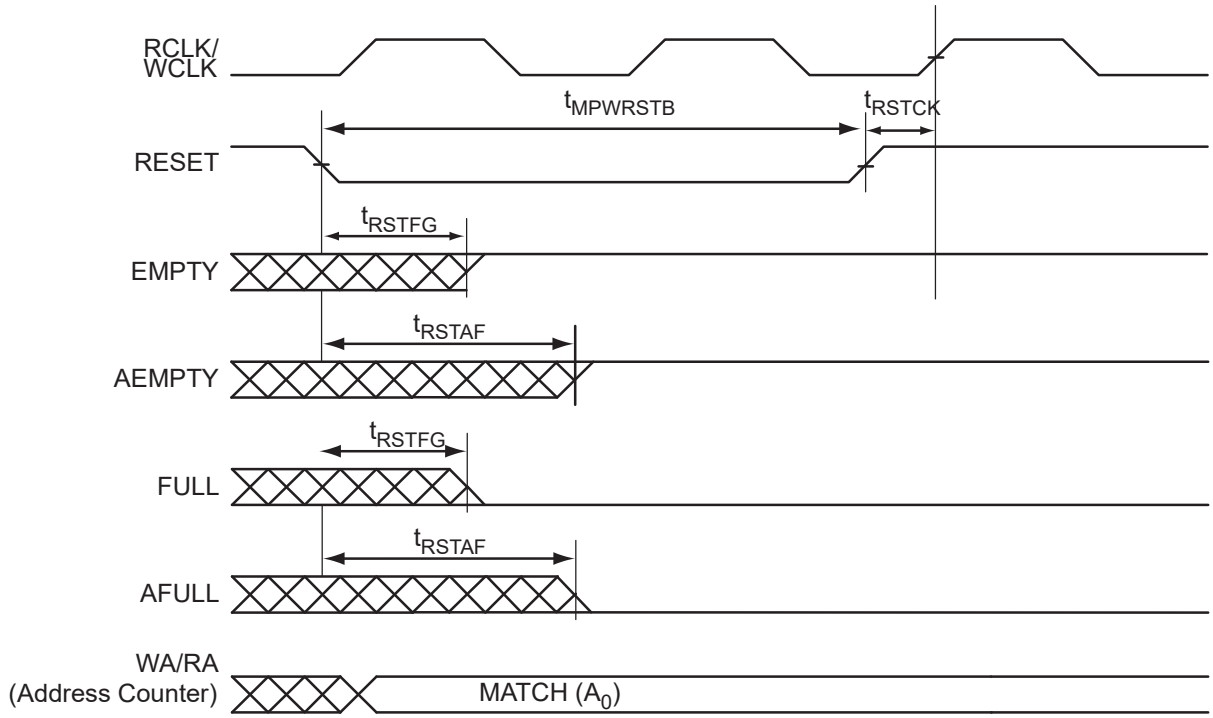


FIGURE 2-41: FIFO EMPTY FLAG AND AEMPTY FLAG ASSERTION

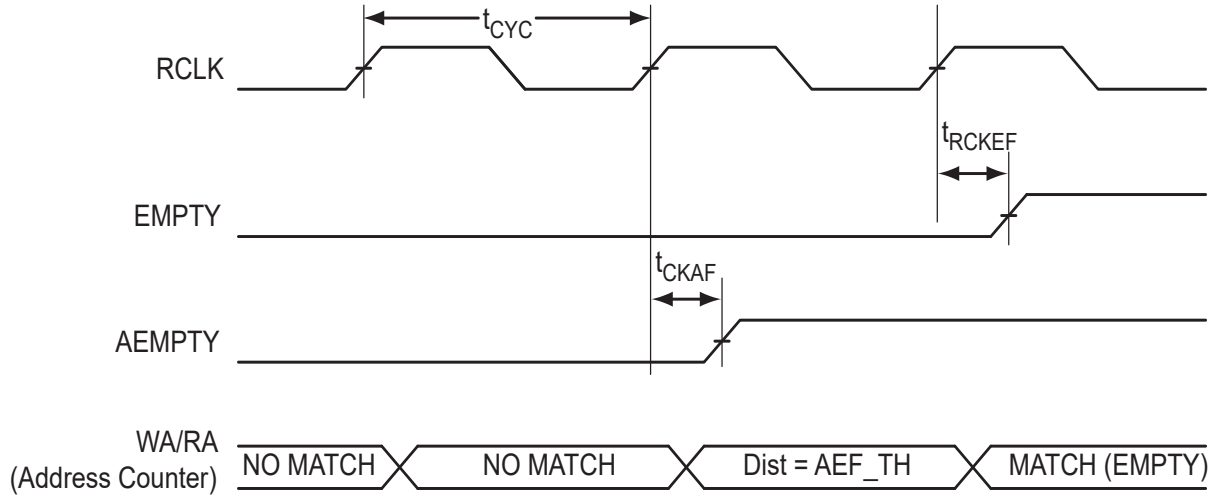


FIGURE 2-42: FIFO FULL FLAG AND AFULL FLAG ASSERTION

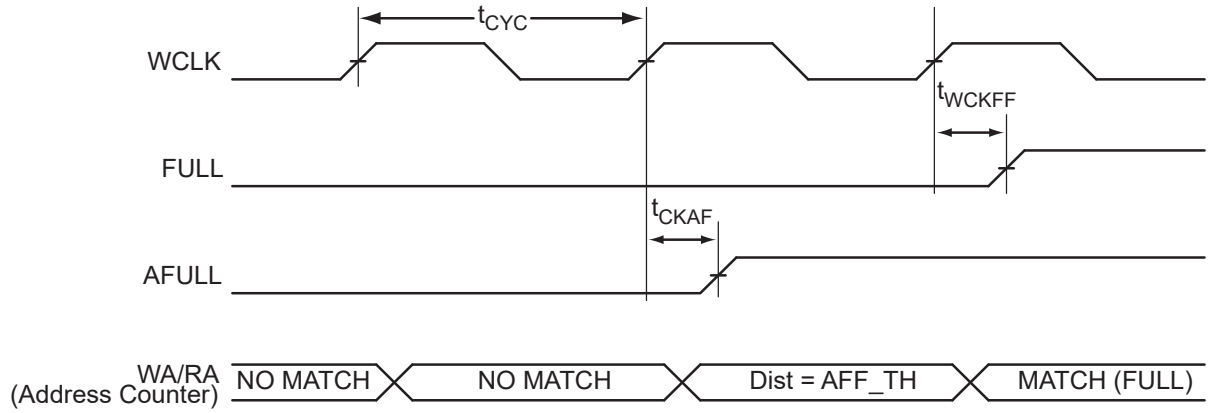


FIGURE 2-43: FIFO EMPTY FLAG AND AEMPTY FLAG DEASSERTION

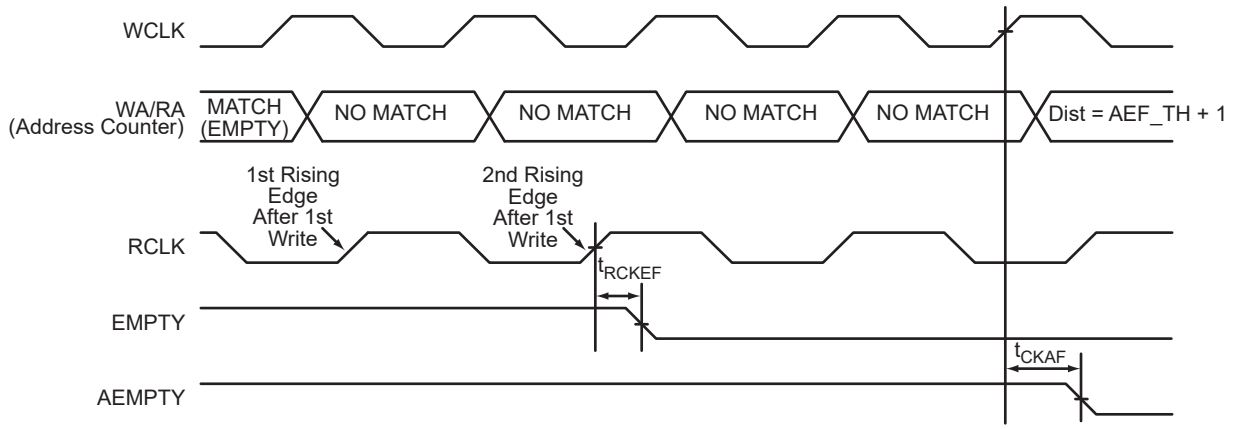
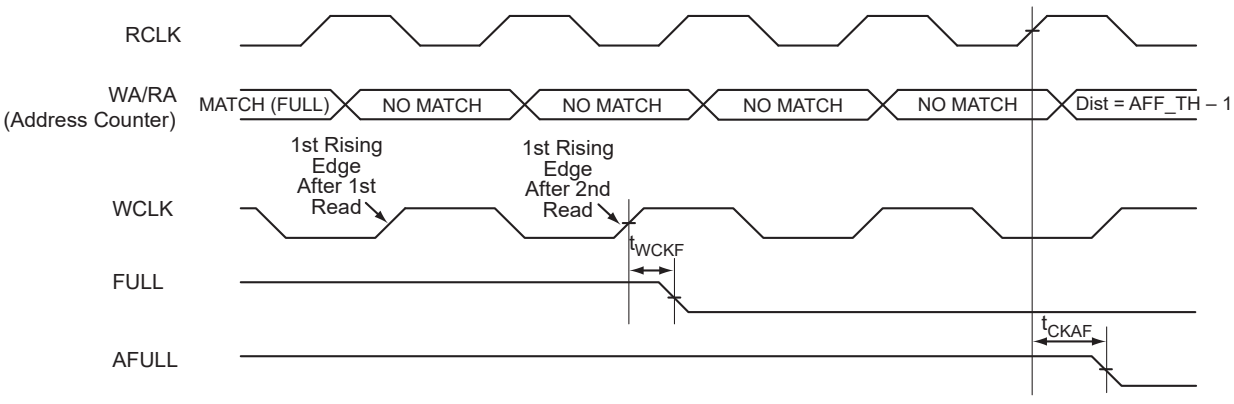


FIGURE 2-44: FIFO FULL FLAG AND AFULL FLAG DEASSERTION



2.12.6 TIMING CHARACTERISTICS

2.12.6.1 1.5V DC Core Voltage

TABLE 2-195: FIFO

Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425V

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.99	ns
t_{ENH}	REN, WEN Hold Time	0.16	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.76	ns
t_{DH}	Input Data (WD) Hold Time	0.25	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	3.33	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	1.80	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	3.53	ns
t_{WCKFF}	WCLK High to Full Flag Valid	3.35	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	12.85	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	3.48	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	12.72	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	2.02	ns
	RESET Low to Data Out Low on RD (pipelined)	2.02	ns
$t_{REMRSTB}$	RESET Removal	0.61	ns
$t_{RECRSTB}$	RESET Recovery	3.21	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency for FIFO	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

2.12.6.2 1.2V DC Core Voltage

TABLE 2-196: FIFO

Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.14V

Parameter	Descriptmion	Std.	Units
t_{ENS}	REN, WEN Setup Time	4.13	ns
t_{ENH}	REN, WEN Hold Time	0.31	ns
t_{BKS}	BLK Setup Time	0.47	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	1.56	ns
t_{DH}	Input Data (WD) Hold Time	0.49	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	6.80	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	3.62	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	7.23	ns
t_{WCKFF}	WCLK High to Full Flag Valid	6.85	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	26.61	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	7.12	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	26.33	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	4.09	ns
	RESET Low to Data Out Low on RD (pipelined)	4.09	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

TABLE 2-196: FIFO

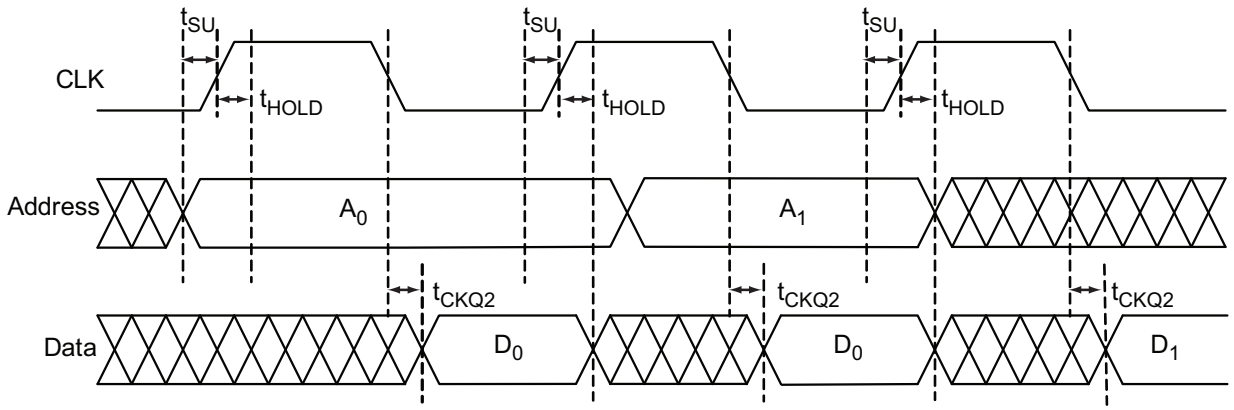
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.14V

Parameter	Descriptmion	Std.	Units
$t_{REMRSTB}$	RESET Removal	1.23	ns
$t_{RECRSTB}$	RESET Recovery	6.58	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency for FIFO	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 for derating values.

2.12.7 EMBEDDED FLASHROM CHARACTERISTICS

FIGURE 2-45: TIMING DIAGRAM



2.12.8 TIMING CHARACTERISTICS

2.12.8.1 1.5V DC Core Voltage

TABLE 2-197: EMBEDDED FLASHROM ACCESS TIME

Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.57	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	34.14	ns
F_{MAX}	Maximum Clock Frequency	15	MHz

2.12.8.2 1.2V DC Core Voltage

TABLE 2-198: EMBEDDED FLASHROM ACCESS TIME

Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.14V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.59	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	52.90	ns
F_{MAX}	Maximum Clock Frequency	10	MHz

2.13 JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the Section 2.4, User I/O Characteristics for more details.

2.13.1 TIMING CHARACTERISTICS

TABLE 2-199: JTAG 1532

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.00	ns
t_{DIHD}	Test Data Input Hold Time	2.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.00	ns
t_{TMDHD}	Test Mode Select Hold Time	2.00	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	25.00	ns
F_{TCKMAX}	TCK Maximum Frequency	15	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.58	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

TABLE 2-200: JTAG 1532 COMMERCIAL-CASE CONDITIONS: T_J = 70°C, WORST-CASE VCC = 1.14V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.50	ns
t_{DIHD}	Test Data Input Hold Time	3.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.50	ns
t_{TMDHD}	Test Mode Select Hold Time	3.00	ns
t_{TCK2Q}	Clock to Q (data out)	11.00	ns
t_{RSTB2Q}	Reset to Q (data out)	30.00	ns
F_{TCKMAX}	TCK Maximum Frequency	9.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	1.18	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 for derating values.

3.0 PIN DESCRIPTIONS

3.1 Supply Pins

3.1.1 GND - GROUND

Ground supply voltage to the core, I/O outputs, and I/O logic.

3.1.2 GNDQ - GROUND (QUIET)

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

3.1.3 VCC - CORE SUPPLY VOLTAGE

Supply voltage to the FPGA core, nominally 1.5V for IGLOO V5 devices, and 1.2V or 1.5V for IGLOO V2 devices. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

For IGLOO V2 devices, VCC can be switched dynamically from 1.2V to 1.5V or vice versa. This allows in-system programming (ISP) when VCC is at 1.5V and the benefit of low power operation when VCC is at 1.2V.

3.1.4 VCCIBX - I/O SUPPLY VOLTAGE

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on IGLOO devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

3.1.5 VMVX - I/O SUPPLY VOLTAGE (QUIET)

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

3.1.6 VCCPLA/B/C/D/E/F - PLL SUPPLY VOLTAGE

Supply voltage to analog PLL, nominally 1.5V or 1.2V.

- 1.5V for IGLOO V5 devices
- 1.2V or 1.5V for IGLOO V2 devices

When the PLLs are not used, the Microchip Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microchip recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOO FPGA Fabric User Guide* for a complete board solution for the PLL analog power supply and ground.

- There is one VCCPLF pin on IGLOO devices.

3.1.7 VCOMPLA/B/C/D/E/F- PLL GROUND

Ground to analog PLL power supplies. When the PLLs are not used, the Microchip Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on IGLOO devices.

3.1.8 VJTAG - JTAG SUPPLY VOLTAGE

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5V to 3.3V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microchip recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

3.1.9 VPUMP - PROGRAMMING SUPPLY VOLTAGE

IGLOO devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microchip recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

3.2 User Pins

3.2.1 I/O - USER INPUT/OUTPUT

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

3.2.2 GL - GLOBALS

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOO FPGA Fabric User Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the "I/O Structures in IGLOO and ProASIC3 Devices" chapter of the *IGLOO FPGA Fabric User Guide* for an explanation of the naming of global pins.

3.2.3 FF - FLASH*FREEZE MODE ACTIVATION PIN

Flash*Freeze mode is available on IGLOO devices. The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

Table 3-1 shows the Flash*Freeze pin location on the available packages for IGLOO a devices. The Flash*Freeze pin location is independent of device, allowing migration to larger or smaller IGLOO devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOO FPGA Fabric User Guide* for more information on I/O states during Flash*Freeze mode.

TABLE 3-1: FLASH*FREEZE PIN LOCATION IN IGLOO FAMILY PACKAGES (DEVICE-INDEPENDENT)

IGLOO Packages	Flash*Freeze Pin
CS81/UC81	H2
CS121	J5
CS196	P3
CS281	W2
QN48	14
QN68	18
QN132	B12
VQ100	27
FG144	L3
FG256	T3
FG484	W6

3.3 JTAG Pins

IGLOO devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5V to 3.3V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

3.3.1 TCK - TEST CLOCK

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microchip recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 3-2 for more information.

TABLE 3-2: RECOMMENDED TIE-OFF VALUES FOR THE TCK AND TRST PINS

VJTAG	Tie-Off Resistance [1,2]
VJTAG at 3.3V	200Ω to 1 kΩ
VJTAG at 2.5V	200Ω to 1 kΩ
VJTAG at 1.8V	500Ω to 1 kΩ
VJTAG at 1.5V	500Ω to 1 kΩ

TABLE 3-2: RECOMMENDED TIE-OFF VALUES FOR THE TCK AND TRST PINS

VJTAG	Tie-Off Resistance [1,2]

Note 1: The TCK pin can be pulled-up or pulled-down.
2: The TRST pin is pulled-down.
3: Equivalent parallel resistance if more than one device is on the JTAG chain

TABLE 3-3: TRST AND TCK PULL-DOWN RECOMMENDATIONS

VJTAG	Tie-Off Resistance*
VJTAG at 3.3V	200Ω to 1 kΩ
VJTAG at 2.5V	200Ω to 1 kΩ
VJTAG at 1.8V	500Ω to 1 kΩ
VJTAG at 1.5V	500Ω to 1 kΩ

Note: Equivalent parallel resistance if more than one device is on the JTAG chain

3.3.2 TDI - TEST DATA INPUT

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

3.3.3 TDO - TEST DATA OUTPUT

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

3.3.4 TMS - TEST MODE SELECT

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

3.3.5 TRST - BOUNDARY SCAN RESET PIN

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-2 and must satisfy the parallel resistance value requirement. The values in Table 3-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microchip recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

3.4 Special Function Pins

3.4.1 NC - NO CONNECT

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

3.4.2 DC - DO NOT CONNECT

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

3.5 Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microchip consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microchip IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Microchip offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

3.6 Related Documents

3.6.1 USER GUIDES

IGLOO FPGA Fabric User Guide

3.6.2 PACKAGING DOCUMENTS

The following documents provide packaging information and device selection for low power flash devices.

3.6.2.1 *Product Catalog*

https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/ProductDocuments/Brochures/igloo_low-power_flash_fpgas_brochure.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

3.6.2.2 *Package Mechanical Drawings*

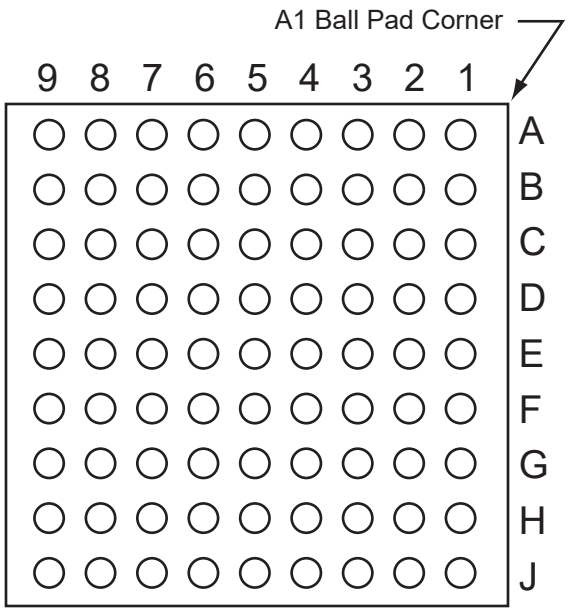
https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/ProductDocuments/PackagingSpecifications/PD3068-Package_Mechanical_Drawings_Datasheet_V62.pdf

This document contains the package mechanical drawings for all packages currently or previously supplied by Microchip. Use the bookmarks to navigate to the package mechanical drawings.

4.0 PACKAGE PIN ASSIGNMENTS

4.1 UC81

FIGURE 4-1: UC81—BOTTOM-VIEW



Note: For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

TABLE 4-1: UC81 PIN DETAILS

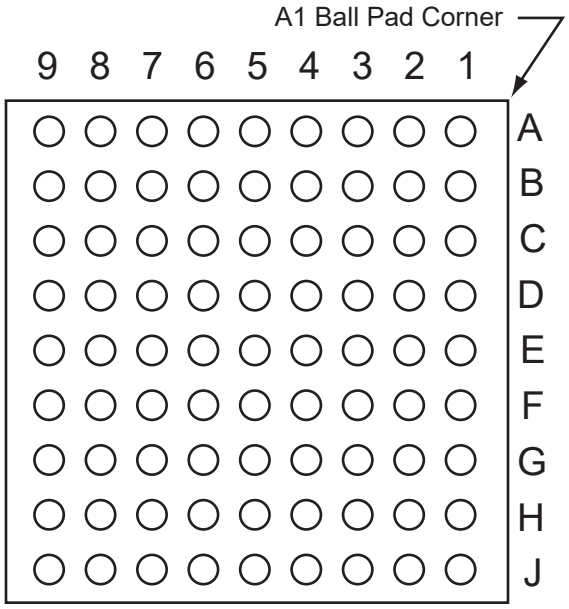
UC81	
Pin Number	**AGL030 Function**
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	IO23RSB0
D8	IO31RSB0
D9	IO30RSB0
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0

TABLE 4-1: UC81 PIN DETAILS

UC81	
Pin Number	**AGL030 Function**
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	VCCIB1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO45RSB1
G7	IO46RSB1
G8	VJTAG
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1
H8	TDI
H9	TDO
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO44RSB1
J7	TCK
J8	TMS
J9	VPUMP

4.2 CS81

FIGURE 4-2: CS81—BOTTOM-VIEW



Note: For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

TABLE 4-2: CS81 PIN DETAILS

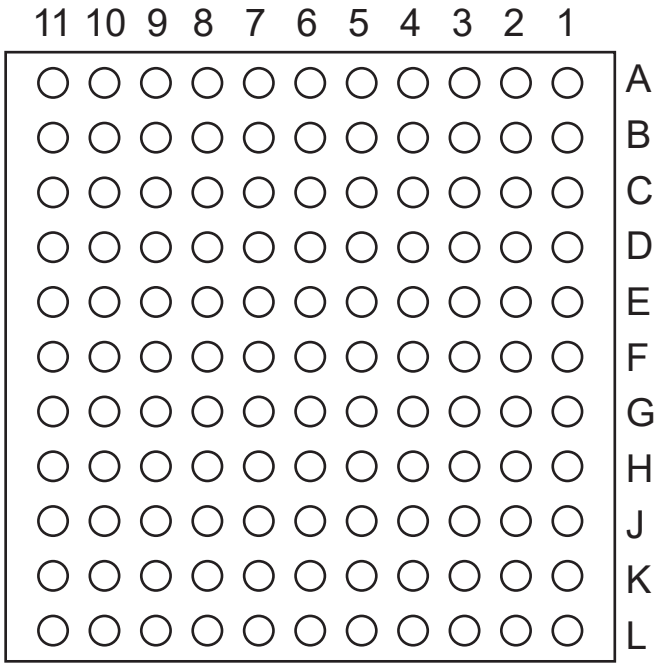
CS81	
Pin Number	**AGL030 Function**
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	IO23RSB0
D8	IO31RSB0
D9	IO30RSB0
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0

TABLE 4-2: CS81 PIN DETAILS

CS81	
Pin Number	**AGL030 Function**
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	VCCIB1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO44RSB1
G7	IO46RSB1
G8	VJTAG
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1
H8	TDI
H9	TDO
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO45RSB1
J7	TCK
J8	TMS
J9	VPUMP

4.3 CS121

FIGURE 4-3: CS121—BOTTOM-VIEW



Note: For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

TABLE 4-3: CS121 PIN DETAILS

CS121	
Pin Number	**AGL060 Function**
A1	GNDQ
A2	IO01RSB0
A3	GAA1/IO03RSB0
A4	GAC1/IO07RSB0
A5	IO15RSB0
A6	IO13RSB0
A7	IO17RSB0
A8	GBB1/IO22RSB0
A9	GBA1/IO24RSB0
A10	GNDQ
A11	VMV0
B1	GAA2/IO95RSB1
B2	IO00RSB0
B3	GAA0/IO02RSB0
B4	GAC0/IO06RSB0
B5	IO08RSB0
B6	IO12RSB0
B7	IO16RSB0
B8	GBC1/IO20RSB0
B9	GBB0/IO21RSB0
B10	GBB2/IO27RSB0
B11	GBA2/IO25RSB0
C1	IO89RSB1
C2	GAC2/IO91RSB1
C3	GAB1/IO05RSB0
C4	GAB0/IO04RSB0
C5	IO09RSB0
C6	IO14RSB0
C7	GBA0/IO23RSB0
C8	GBC0/IO19RSB0
C9	IO26RSB0
C10	IO28RSB0
C11	GBC2/IO29RSB0
D1	IO88RSB1
D2	IO90RSB1
D3	GAB2/IO93RSB1
D4	IO10RSB0
D5	IO11RSB0
D6	IO18RSB0
D7	IO32RSB0
D8	IO31RSB0
D9	GCA2/IO41RSB0

TABLE 4-3: CS121 PIN DETAILS

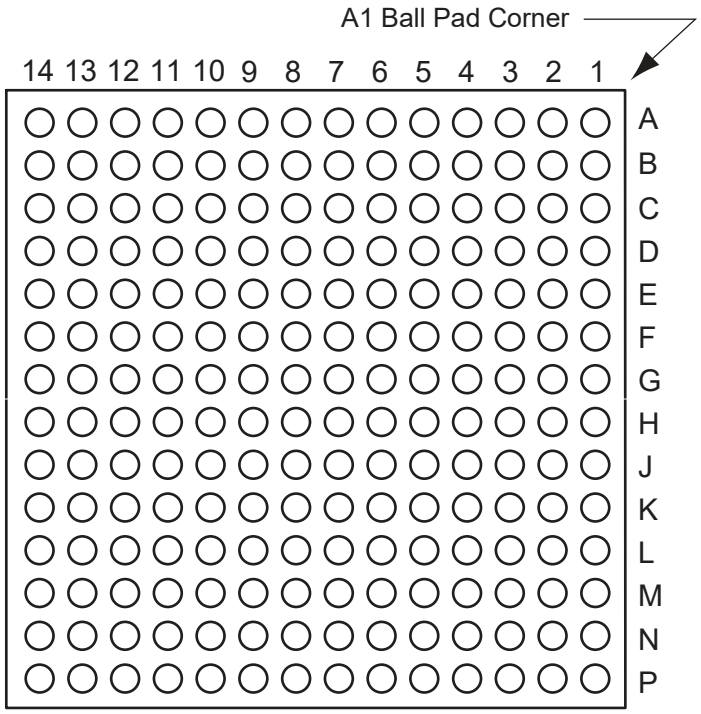
CS121	
Pin Number	**AGL060 Function**
D10	IO30RSB0
D11	IO33RSB0
E1	IO87RSB1
E2	GFC0/IO85RSB1
E3	IO92RSB1
E4	IO94RSB1
E5	VCC
E6	VCCIB0
E7	GND
E8	GCC0/IO36RSB0
E9	IO34RSB0
E10	GCB1/IO37RSB0
E11	GCC1/IO35RSB0
F1*	VCOMPLF
F2	GFB0/IO83RSB1
F3	GFA0/IO82RSB1
F4	GFC1/IO86RSB1
F5	VCCIB1
F6	VCC
F7	VCCIB0
F8	GCB2/IO42RSB0
F9	GCC2/IO43RSB0
F10	GCB0/IO38RSB0
F11	GCA1/IO39RSB0
G1*	VCCPLF
G2	GFB2/IO79RSB1
G3	GFA1/IO81RSB1
G4	GFB1/IO84RSB1
G5	GND
G6	VCCIB1
G7	VCC
G8	GDC0/IO46RSB0
G9	GDA1/IO49RSB0
G10	GDB0/IO48RSB0
G11	GCA0/IO40RSB0
H1	IO75RSB1
H2	IO76RSB1
H3	GFC2/IO78RSB1
H4	GFA2/IO80RSB1
H5	IO77RSB1
H6	GEC2/IO66RSB1
H7	IO54RSB1

TABLE 4-3: CS121 PIN DETAILS

CS121	
Pin Number	**AGL060 Function**
H8	GDC2/IO53RSB1
H9	VJTAG
H10	TRST
H11	IO44RSB0
J1	GEC1/IO74RSB1
J2	GEC0/IO73RSB1
J3	GEB1/IO72RSB1
J4	GEA0/IO69RSB1
J5	FF/GEB2/IO67RSB1
J6	IO62RSB1
J7	GDA2/IO51RSB1
J8	GDB2/IO52RSB1
J9	TDI
J10	TDO
J11	GDC1/IO45RSB0
K1	GEB0/IO71RSB1
K2	GEA1/IO70RSB1
K3	GEA2/IO68RSB1
K4	IO64RSB1
K5	IO60RSB1
K6	IO59RSB1
K7	IO56RSB1
K8	TCK
K9	TMS
K10	VPUMP
K11	GDB1/IO47RSB0
L1	VMV1
L2	GNDQ
L3	IO65RSB1
L4	IO63RSB1
L5	IO61RSB1
L6	IO58RSB1
L7	IO57RSB1
L8	IO55RSB1
L9	GNDQ
L10	GDA0/IO50RSB0
L11	VMV1

4.4 CS196

FIGURE 4-4: CS196—BOTTOM-VIEW



Note: For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

TABLE 4-4: CS196 PIN DETAILS

CS196	
Pin Number	**AGL125 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	GAC1/IO05RSB0
A5	IO09RSB0
A6	IO15RSB0
A7	IO18RSB0
A8	IO22RSB0
A9	IO27RSB0
A10	GBC0/IO35RSB0
A11	GBB0/IO37RSB0
A12	GBB1/IO38RSB0
A13	GBA1/IO40RSB0
A14	GND
B1	VCCIB1
B2	VMV0
B3	GAA1/IO01RSB0
B4	GAB1/IO03RSB0
B5	GND
B6	IO16RSB0
B7	IO20RSB0
B8	IO24RSB0
B9	IO28RSB0
B10	GND
B11	GBC1/IO36RSB0
B12	GBA0/IO39RSB0
B13	GBA2/IO41RSB0
B14	GBB2/IO43RSB0
C1	GAC2/IO128RSB1
C2	GAB2/IO130RSB1
C3	GNDQ
C4	VCCIB0
C5	GAB0/IO02RSB0
C6	IO14RSB0
C7	VCCIB0
C8	NC
C9	IO23RSB0
C10	IO29RSB0
C11	VCCIB0
C12	IO42RSB0
C13	GNDQ
C14	IO44RSB0

TABLE 4-4: CS196 PIN DETAILS

CS196	
Pin Number	**AGL125 Function**
D1	IO127RSB1
D2	IO129RSB1
D3	GAA2/IO132RSB1
D4	IO126RSB1
D5	IO06RSB0
D6	IO13RSB0
D7	IO19RSB0
D8	IO21RSB0
D9	IO26RSB0
D10	IO31RSB0
D11	IO30RSB0
D12	VMV0
D13	IO46RSB0
D14	GBC2/IO45RSB0
E1	IO125RSB1
E2	GND
E3	IO131RSB1
E4	VCCIB1
E5	NC
E6	IO08RSB0
E7	IO17RSB0
E8	IO12RSB0
E9	IO11RSB0
E10	NC
E11	VCCIB0
E12	IO32RSB0
E13	GND
E14	IO34RSB0
F1	IO124RSB1
F2	IO114RSB1
F3	IO113RSB1
F4	IO112RSB1
F5	IO111RSB1
F6	NC
F7	VCC
F8	VCC
F9	NC
F10	IO07RSB0
F11	IO25RSB0
F12	IO10RSB0
F13	IO33RSB0
F14	IO47RSB0

TABLE 4-4: CS196 PIN DETAILS

CS196	
Pin Number	**AGL125 Function**
G1	GFB1/IO121RSB1
G2	GFA0/IO119RSB1
G3	GFA2/IO117RSB1
G4	VCOMPLF
G5	GFC0/IO122RSB1
G6	VCC
G7	GND
G8	GND
G9	VCC
G10	GCC0/IO52RSB0
G11	GCB1/IO53RSB0
G12	GCA0/IO56RSB0
G13	IO48RSB0
G14	GCC2/IO59RSB0
H1	GFB0/IO120RSB1
H2	GFA1/IO118RSB1
H3	VCCPLF
H4	GFB2/IO116RSB1
H5	GFC1/IO123RSB1
H6	VCC
H7	GND
H8	GND
H9	VCC
H10	GCC1/IO51RSB0
H11	GCB0/IO54RSB0
H12	GCA1/IO55RSB0
H13	IO49RSB0
H14	GCA2/IO57RSB0
J1	GFC2/IO115RSB1
J2	IO110RSB1
J3	IO94RSB1
J4	IO93RSB1
J5	IO89RSB1
J6	NC
J7	VCC
J8	VCC
J9	NC
J10	IO60RSB0
J11	GCB2/IO58RSB0
J12	IO50RSB0
J13	GDC1/IO61RSB0
J14	GDC0/IO62RSB0

TABLE 4-4: CS196 PIN DETAILS

CS196	
Pin Number	**AGL125 Function**
K1	IO99RSB1
K2	GND
K3	IO95RSB1
K4	VCCIB1
K5	NC
K6	IO86RSB1
K7	IO80RSB1
K8	IO74RSB1
K9	IO72RSB1
K10	NC
K11	VCCIB0
K12	GDA1/IO65RSB0
K13	GND
K14	GDB1/IO63RSB0
L1	GEB1/IO107RSB1
L2	GEC1/IO109RSB1
L3	GEC0/IO108RSB1
L4	IO96RSB1
L5	IO91RSB1
L6	IO90RSB1
L7	IO83RSB1
L8	IO81RSB1
L9	IO71RSB1
L10	IO70RSB1
L11	VPUMP
L12	VJTAG
L13	GDA0/IO66RSB0
L14	GDB0/IO64RSB0
M1	GEB0/IO106RSB1
M2	GEA1/IO105RSB1
M3	GNDQ
M4	VCCIB1
M5	IO92RSB1
M6	IO88RSB1
M7	NC
M8	VCCIB1
M9	IO76RSB1
M10	GDB2/IO68RSB1
M11	VCCIB1
M12	VMV1
M13	TRST
M14	VCCIB0

TABLE 4-4: CS196 PIN DETAILS

CS196	
Pin Number	**AGL125 Function**
N1	GEA0/IO104RSB1
N2	VMV1
N3	GEC2/IO101RSB1
N4	IO100RSB1
N5	GND
N6	IO87RSB1
N7	IO82RSB1
N8	IO78RSB1
N9	IO73RSB1
N10	GND
N11	TCK
N12	TDI
N13	GNDQ
N14	TDO
P1	GND
P2	GEA2/IO103RSB1
P3	FF/GEB2/IO102RSB1
P4	IO98RSB1
P5	IO97RSB1
P6	IO85RSB1
P7	IO84RSB1
P8	IO79RSB1
P9	IO77RSB1
P10	IO75RSB1
P11	GDC2/IO69RSB1
P12	GDA2/IO67RSB1
P13	TMS
P14	GND

TABLE 4-5: CS196 PIN DETAILS

CS196	
Pin Number	**AGL250 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	GAC1/IO05RSB0
A5	IO10RSB0
A6	IO13RSB0
A7	IO17RSB0
A8	IO19RSB0
A9	IO23RSB0
A10	GBC0/IO35RSB0
A11	GBB0/IO37RSB0
A12	GBB1/IO38RSB0
A13	GBA1/IO40RSB0
A14	GND
B1	VCCIB3
B2	VMV0
B3	GAA1/IO01RSB0
B4	GAB1/IO03RSB0
B5	GND
B6	IO12RSB0
B7	IO16RSB0
B8	IO22RSB0
B9	IO24RSB0
B10	GND
B11	GBC1/IO36RSB0
B12	GBA0/IO39RSB0
B13	GBA2/IO41PPB1
B14	GBB2/IO42PDB1
C1	GAC2/IO116UDB3
C2	GAB2/IO117UDB3
C3	GNDQ
C4	VCCIB0
C5	GAB0/IO02RSB0
C6	IO11RSB0
C7	VCCIB0
C8	IO20RSB0
C9	IO30RSB0
C10	IO33RSB0
C11	VCCIB0
C12	IO41NPB1
C13	GNDQ

TABLE 4-5: CS196 PIN DETAILS

CS196	
Pin Number	**AGL250 Function**
C14	IO42NDB1
D1	IO116VDB3
D2	IO117VDB3
D3	GAA2/IO118UDB3
D4	IO113PPB3
D5	IO08RSB0
D6	IO14RSB0
D7	IO15RSB0
D8	IO18RSB0
D9	IO25RSB0
D10	IO32RSB0
D11	IO44PPB1
D12	VMV1
D13	IO43NDB1
D14	GBC2/IO43PDB1
E1	IO112PDB3
E2	GND
E3	IO118VDB3
E4	VCCIB3
E5	IO114USB3
E6	IO07RSB0
E7	IO09RSB0
E8	IO21RSB0
E9	IO31RSB0
E10	IO34RSB0
E11	VCCIB1
E12	IO44NPB1
E13	GND
E14	IO45PDB1
F1	IO112NDB3
F2	IO107NPB3
F3	IO111PDB3
F4	IO111NDB3
F5	IO113NPB3
F6	IO06RSB0
F7	VCC
F8	VCC
F9	IO28RSB0
F10	IO54PDB1
F11	IO54NDB1
F12	IO47NDB1
F13	IO47PDB1

TABLE 4-5: CS196 PIN DETAILS

CS196	
Pin Number	**AGL250 Function**
F14	IO45NDB1
G1	GFB1/IO109PDB3
G2	GFA0/IO108NDB3
G3	GFA2/IO107PPB3
G4	VCOMPLF
G5	GFC0/IO110NDB3
G6	VCC
G7	GND
G8	GND
G9	VCC
G10	GCC0/IO48NDB1
G11	GCB1/IO49PDB1
G12	GCA0/IO50NDB1
G13	IO53NDB1
G14	GCC2/IO53PDB1
H1	GFB0/IO109NDB3
H2	GFA1/IO108PDB3
H3	VCCPLF
H4	GFB2/IO106PPB3
H5	GFC1/IO110PDB3
H6	VCC
H7	GND
H8	GND
H9	VCC
H10	GCC1/IO48PDB1
H11	GCB0/IO49NDB1
H12	GCA1/IO50PDB1
H13	IO51NDB1
H14	GCA2/IO51PDB1
J1	GFC2/IO105PDB3
J2	IO104PPB3
J3	IO106NPB3
J4	IO103PDB3
J5	IO103NDB3
J6	IO80RSB2
J7	VCC
J8	VCC
J9	IO64RSB2
J10	IO56PDB1
J11	GCB2/IO52PDB1
J12	IO52NDB1
J13	GDC1/IO58UDB1

TABLE 4-5: CS196 PIN DETAILS

CS196	
Pin Number	**AGL250 Function**
J14	GDC0/IO58VDB1
K1	IO105NDB3
K2	GND
K3	IO104NPB3
K4	VCCIB3
K5	IO101PPB3
K6	IO91RSB2
K7	IO81RSB2
K8	IO73RSB2
K9	IO77RSB2
K10	IO56NDB1
K11	VCCIB1
K12	GDA1/IO60UPB1
K13	GND
K14	GDB1/IO59UDB1
L1	GEB1/IO99PDB3
L2	GEC1/IO100PDB3
L3	GEC0/IO100NDB3
L4	IO101NPB3
L5	IO89RSB2
L6	IO92RSB2
L7	IO75RSB2
L8	IO66RSB2
L9	IO65RSB2
L10	IO71RSB2
L11	VPUMP
L12	VJTAG
L13	GDA0/IO60VPB1
L14	GDB0/IO59VDB1
M1	GEB0/IO99NDB3
M2	GEA1/IO98PPB3
M3	GNDQ
M4	VCCIB2
M5	IO88RSB2
M6	IO87RSB2
M7	IO82RSB2
M8	VCCIB2
M9	IO67RSB2
M10	GDB2/IO62RSB2
M11	VCCIB2
M12	VMV2
M13	TRST

TABLE 4-5: CS196 PIN DETAILS

CS196	
Pin Number	**AGL250 Function**
M14	VCCIB1
N1	GEA0/IO98NPB3
N2	VMV3
N3	GEC2/IO95RSB2
N4	IO94RSB2
N5	GND
N6	IO86RSB2
N7	IO78RSB2
N8	IO74RSB2
N9	IO69RSB2
N10	GND
N11	TCK
N12	TDI
N13	GNDQ
N14	TDO
P1	GND
P2	GEA2/IO97RSB2
P3	FF/GEB2/IO96RSB2
P4	IO90RSB2
P5	IO85RSB2
P6	IO83RSB2
P7	IO79RSB2
P8	IO76RSB2
P9	IO72RSB2
P10	IO68RSB2
P11	GDC2/IO63RSB2
P12	GDA2/IO61RSB2
P13	TMS
P14	GND

TABLE 4-6: CS196 PIN DETAILS

CS196	
Pin Number	**AGL400 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	GAC1/IO05RSB0
A5	IO14RSB0
A6	IO18RSB0
A7	IO26RSB0
A8	IO29RSB0
A9	IO36RSB0
A10	GBC0/IO54RSB0
A11	GBB0/IO56RSB0
A12	GBB1/IO57RSB0
A13	GBA1/IO59RSB0
A14	GND
B1	VCCIB3
B2	VMV0
B2	VMV0
B3	GAA1/IO01RSB0
B4	GAB1/IO03RSB0
B5	GND
B6	IO17RSB0
B7	IO25RSB0
B8	IO34RSB0
B9	IO39RSB0
B10	GND
B11	GBC1/IO55RSB0
B12	GBA0/IO58RSB0
B13	GBA2/IO60PPB1
B14	GBB2/IO61PDB1
C1	GAC2/IO153UDB3
C2	GAB2/IO154UDB3
C3	GNDQ
C4	VCCIB0
C5	GAB0/IO02RSB0
C6	IO15RSB0
C7	VCCIB0
C8	IO31RSB0
C9	IO44RSB0
C10	IO49RSB0
C11	VCCIB0
C12	IO60NPB1
C13	GNDQ

TABLE 4-6: CS196 PIN DETAILS

CS196	
Pin Number	**AGL400 Function**
C14	IO61NDB1
D1	IO153VDB3
D2	IO154VDB3
D3	GAA2/IO155UDB3
D4	IO150PPB3
D5	IO11RSB0
D6	IO20RSB0
D7	IO23RSB0
D8	IO28RSB0
D9	IO41RSB0
D10	IO47RSB0
D11	IO63PPB1
D12	VMV1
D13	IO62NDB1
D14	GBC2/IO62PDB1
E1	IO149PDB3
E2	GND
E3	IO155VDB3
E4	VCCIB3
E5	IO151USB3
E6	IO09RSB0
E7	IO12RSB0
E8	IO32RSB0
E9	IO46RSB0
E10	IO51RSB0
E11	VCCIB1
E12	IO63NPB1
E13	GND
E14	IO64PDB1
F1	IO149NDB3
F2	IO144NPB3
F3	IO148PDB3
F4	IO148NDB3
F5	IO150NPB3
F6	IO07RSB0
F7	VCC
F8	VCC
F9	IO43RSB0
F10	IO73PDB1
F11	IO73NDB1
F12	IO66NDB1
F13	IO66PDB1

TABLE 4-6: CS196 PIN DETAILS

CS196	
Pin Number	**AGL400 Function**
F14	IO64NDB1
G1	GFB1/IO146PDB3
G2	GFA0/IO145NDB3
G3	GFA2/IO144PPB3
G4	VCOMPLF
G5	GFC0/IO147NDB3
G6	VCC
G7	GND
G8	GND
G9	VCC
G10	GCC0/IO67NDB1
G11	GCB1/IO68PDB1
G12	GCA0/IO69NDB1
G13	IO72NDB1
G14	GCC2/IO72PDB1
H1	GFB0/IO146NDB3
H2	GFA1/IO145PDB3
H3	VCCPLF
H4	GFB2/IO143PPB3
H5	GFC1/IO147PDB3
H6	VCC
H7	GND
H8	GND
H9	VCC
H10	GCC1/IO67PDB1
H11	GCB0/IO68NDB1
H12	GCA1/IO69PDB1
H13	IO70NDB1
H14	GCA2/IO70PDB1
J1	GFC2/IO142PDB3
J2	IO141PPB3
J3	IO143NPB3
J4	IO140PDB3
J5	IO140NDB3
J6	IO109RSB2
J7	VCC
J8	VCC
J9	IO84RSB2
J10	IO75PDB1
J11	GCB2/IO71PDB1
J12	IO71NDB1
J13	GDC1/IO77UDB1

TABLE 4-6: CS196 PIN DETAILS

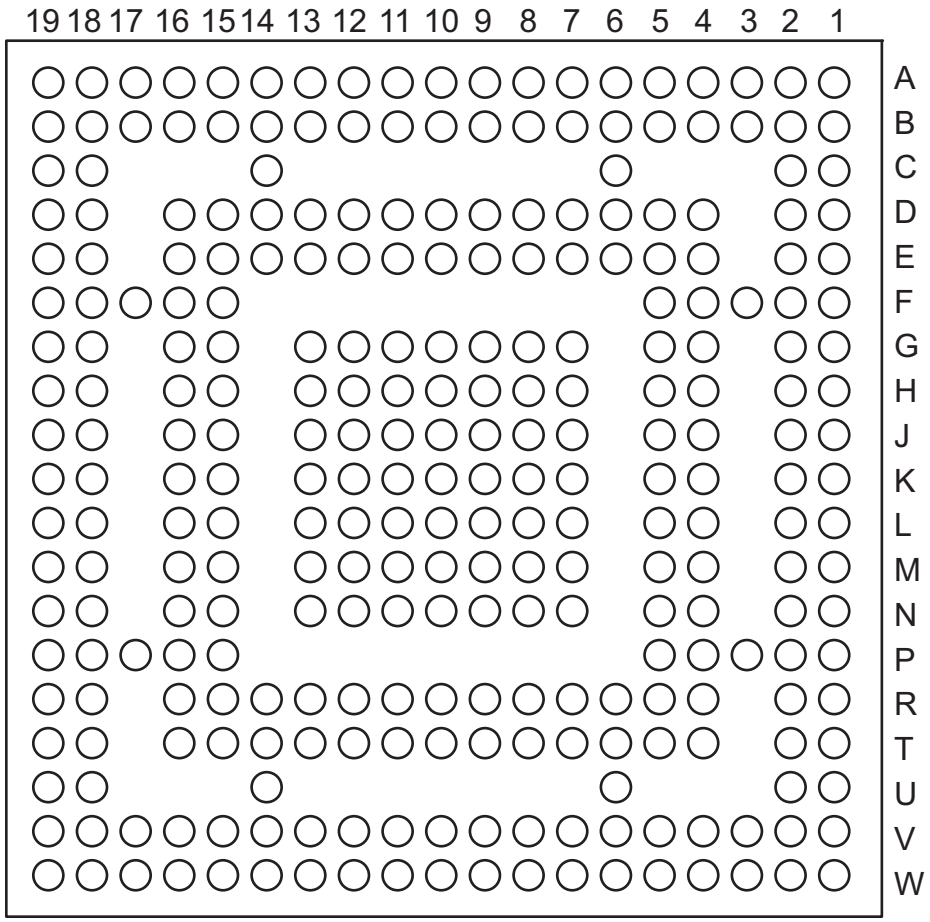
CS196	
Pin Number	**AGL400 Function**
J14	GDC0/IO77VDB1
K1	IO142NDB3
K2	GND
K3	IO141NPB3
K4	VCCIB3
K5	IO138PPB3
K6	IO125RSB2
K7	IO110RSB2
K8	IO98RSB2
K9	IO104RSB2
K10	IO75NDB1
K11	VCCIB1
K12	GDA1/IO79UPB1
K13	GND
K14	GDB1/IO78UDB1
L1	GEB1/IO136PDB3
L2	GEC1/IO137PDB3
L3	GEC0/IO137NDB3
L4	IO138NPB3
L5	IO122RSB2
L6	IO128RSB2
L7	IO101RSB2
L8	IO88RSB2
L9	IO86RSB2
L10	IO94RSB2
L11	VPUMP
L12	VJTAG
L13	GDA0/IO79VPB1
L14	GDB0/IO78VDB1
M1	GEB0/IO136NDB3
M2	GEA1/IO135PPB3
M3	GNDQ
M4	VCCIB2
M5	IO120RSB2
M6	IO119RSB2
M7	IO112RSB2
M8	VCCIB2
M9	IO89RSB2
M10	GDB2/IO81RSB2
M11	VCCIB2
M12	VMV2
M12	VMV2

TABLE 4-6: CS196 PIN DETAILS

CS196	
Pin Number	**AGL400 Function**
M13	TRST
M14	VCCIB1
N1	GEA0/IO135NPB3
N2	VMV3
N3	GEC2/IO132RSB2
N4	IO130RSB2
N5	GND
N6	IO117RSB2
N7	IO106RSB2
N8	IO100RSB2
N9	IO92RSB2
N10	GND
N11	TCK
N12	TDI
N13	GNDQ
N14	TDO
P1	GND
P2	GEA2/IO134RSB2
P3	FF/GEB2/ IO133RSB2
P4	IO123RSB2
P5	IO116RSB2
P6	IO114RSB2
P7	IO107RSB2
P8	IO103RSB2
P9	IO95RSB2
P10	IO91RSB2
P11	GDC2/IO82RSB2
P12	GDA2/IO80RSB2
P13	TMS
P14	GND

4.5 CS281

FIGURE 4-5: CS281—BOTTOM-VIEW



Note: For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

TABLE 4-7: CS281 PIN DETAILS

CS281	
Pin Number	AGL600 Function
A1	GND
A2	GAB0/IO02RSB0
A3	GAC1/IO05RSB0
A4	IO07RSB0
A5	IO10RSB0
A6	IO14RSB0
A7	IO18RSB0
A8	IO21RSB0
A9	IO22RSB0
A10	VCCIB0
A11	IO33RSB0
A12	IO40RSB0
A13	IO37RSB0
A14	IO48RSB0
A15	IO51RSB0
A16	IO53RSB0
A17	GBC1/IO55RSB0
A18	GBA0/IO58RSB0
A19	GND
B1	GAA2/IO174PPB3
B2	VCCIB0
B3	GAB1/IO03RSB0
B4	GAC0/IO04RSB0
B5	IO06RSB0
B6	GND
B7	IO15RSB0
B8	IO20RSB0
B9	IO23RSB0
B10	IO24RSB0
B11	IO36RSB0
B12	IO35RSB0
B13	IO44RSB0
B14	GND
B15	IO52RSB0
B16	GBC0/IO54RSB0
B17	GBA1/IO59RSB0
B18	VCCIB1
B19	IO61NDB1
C1	GAB2/IO173PPB3
C2	IO174NPB3
C6	IO12RSB0

TABLE 4-7: CS281 PIN DETAILS

CS281	
Pin Number	AGL600 Function
C14	IO50RSB0
C18	IO60NPB1
C19	GBB2/IO61PDB1
D1	IO170PPB3
D2	IO172NPB3
D4	GAA0/IO00RSB0
D5	GAA1/IO01RSB0
D6	IO09RSB0
D7	IO16RSB0
D8	IO19RSB0
D9	IO26RSB0
D10	GND
D11	IO34RSB0
D12	IO45RSB0
D13	IO49RSB0
D14	IO47RSB0
D15	GBB0/IO56RSB0
D16	GBA2/IO60PPB1
D18	GBC2/IO62PPB1
D19	IO66NPB1
E1	IO169NPB3
E2	IO171PPB3
E4	IO171NPB3
E5	IO08RSB0
E6	IO11RSB0
E7	IO13RSB0
E8	IO17RSB0
E9	IO25RSB0
E10	IO30RSB0
E11	IO41RSB0
E12	IO42RSB0
E13	IO46RSB0
E14	GBB1/IO57RSB0
E15	IO62NPB1
E16	IO63PPB1
E18	IO64PPB1
E19	IO65NPB1
F1	IO168NPB3
F2	GND
F3	IO169PPB3
F4	IO170NPB3

TABLE 4-7: CS281 PIN DETAILS

CS281	
Pin Number	AGL600 Function
F5	IO173NPB3
F15	IO63NPB1
F16	IO65PPB1
F17	IO64NPB1
F18	GND
F19	IO68PPB1
G1	IO167NPB3
G2	IO165NDB3
G4	IO168PPB3
G5	IO167PPB3
G7	GAC2/IO172PPB3
G8	VCCIB0
G9	IO28RSB0
G10	IO32RSB0
G11	IO43RSB0
G12	VCCIB0
G13	IO66PPB1
G15	IO67NDB1
G16	IO67PDB1
G18	GCC0/IO69NPB1
G19	GCB1/IO70PPB1
H1	GFB0/IO163NPB3
H2	IO165PDB3
H4	GFC1/IO164PPB3
H5	GFB1/IO163PPB3
H7	VCCIB3
H8	VCC
H9	VCCIB0
H10	VCC
H11	VCCIB0
H12	VCC
H13	VCCIB1
H15	IO68NPB1
H16	GCB0/IO70NPB1
H18	GCA1/IO71PPB1
H19	GCA2/IO72PPB1
J1	VCOMPLF
J2	GFA0/IO162NDB3
J4	VCCPLF
J5	GFC0/IO164NPB3
J7	GFA2/IO161PDB3

TABLE 4-7: CS281 PIN DETAILS

CS281	
Pin Number	AGL600 Function
J8	VCCIB3
J9	GND
J10	GND
J11	GND
J12	VCCIB1
J13	GCC1/IO69PPB1
J15	GCA0/IO71NPB1
J16	GCB2/IO73PPB1
J18	IO72NPB1
J19	IO75PSB1
K1	VCCIB3
K2	GFA1/IO162PDB3
K4	GND
K5	IO159NPB3
K7	IO161NDB3
K8	VCC
K9	GND
K10	GND
K11	GND
K12	VCC
K13	GCC2/IO74PPB1
K15	IO73NPB1
K16	GND
K18	IO74NPB1
K19	VCCIB1
L1	GFB2/IO160PDB3
L2	IO160NDB3
L4	GFC2/IO159PPB3
L5	IO153PPB3
L7	IO153NPB3
L8	VCCIB3
L9	GND
L10	GND
L11	GND
L12	VCCIB1
L13	IO76PPB1
L15	IO76NPB1
L16	IO77PPB1
L18	IO78NPB1
L19	IO77NPB1
M1	IO158PDB3

TABLE 4-7: CS281 PIN DETAILS

CS281	
Pin Number	AGL600 Function
M2	IO158NDB3
M4	IO154NPB3
M5	IO152PPB3
M7	VCCIB3
M8	VCC
M9	VCCIB2
M10	VCC
M11	VCCIB2
M12	VCC
M13	VCCIB1
M15	IO79NPB1
M16	IO81NPB1
M18	IO79PPB1
M19	IO78PPB1
N1	IO154PPB3
N2	IO152NPB3
N4	IO150PPB3
N5	IO148NPB3
N7	GEA2/IO143RSB2
N8	VCCIB2
N9	IO117RSB2
N10	IO115RSB2
N11	IO114RSB2
N12	VCCIB2
N13	VPUMP
N15	IO82PPB1
N16	IO85PPB1
N18	IO82NPB1
N19	IO81PPB1
P1	IO151PDB3
P2	GND
P3	IO151NDB3
P4	IO149PPB3
P5	GEA0/IO144NPB3
P15	IO83NDB1
P16	IO83PDB1
P17	GDC1/IO86PPB1
P18	GND
P19	IO85NPB1
R1	IO150NPB3
R2	IO149NPB3

TABLE 4-7: CS281 PIN DETAILS

CS281	
Pin Number	AGL600 Function
R4	GEC1/IO146PPB3
R5	GEB1/IO145PPB3
R6	IO138RSB2
R7	IO127RSB2
R8	IO123RSB2
R9	IO118RSB2
R10	IO111RSB2
R11	IO106RSB2
R12	IO103RSB2
R13	IO97RSB2
R14	IO95RSB2
R15	IO94RSB2
R16	GDA1/IO88PPB1
R18	GDB0/IO87NPB1
R19	GDC0/IO86NPB1
T1	IO148PPB3
T2	GEC0/IO146NPB3
T4	GEB0/IO145NPB3
T5	IO132RSB2
T6	IO136RSB2
T7	IO130RSB2
T8	IO126RSB2
T9	IO120RSB2
T10	GND
T11	IO113RSB2
T12	IO104RSB2
T13	IO101RSB2
T14	IO98RSB2
T15	GDC2/IO91RSB2
T16	TMS
T18	VJTAG
T19	GDB1/IO87PPB1
U1	IO147PDB3
U2	GEA1/IO144PPB3
U6	IO131RSB2
U14	IO99RSB2
U18	TRST
U19	GDA0/IO88NPB1
V1	IO147NDB3
V2	VCCIB3
V3	GEC2/IO141RSB2

TABLE 4-7: CS281 PIN DETAILS

CS281	
Pin Number	**AGL600 Function**
V4	IO140RSB2
V5	IO135RSB2
V6	GND
V7	IO125RSB2
V8	IO122RSB2
V9	IO116RSB2
V10	IO112RSB2
V11	IO110RSB2
V12	IO108RSB2
V13	IO102RSB2
V14	GND
V15	IO93RSB2
V16	GDA2/IO89RSB2
V17	TDI
V18	VCCIB2
V19	TDO
W1	GND
W2	FF/GEB2/IO142RSB2
W3	IO139RSB2
W4	IO137RSB2
W5	IO134RSB2
W6	IO133RSB2
W7	IO128RSB2
W8	IO124RSB2
W9	IO119RSB2
W10	VCCIB2
W11	IO109RSB2
W12	IO107RSB2
W13	IO105RSB2
W14	IO100RSB2
W15	IO96RSB2
W16	IO92RSB2
W17	GDB2/IO90RSB2
W18	TCK
W19	GND

TABLE 4-8: CS281 PIN DETAILS

CS281	
Pin Number	AGL1000 Function
A1	GND
A2	GAB0/IO02RSB0
A3	GAC1/IO05RSB0
A4	IO13RSB0
A5	IO11RSB0
A6	IO16RSB0
A7	IO20RSB0
A8	IO24RSB0
A9	IO29RSB0
A10	VCCIB0
A11	IO39RSB0
A12	IO45RSB0
A13	IO48RSB0
A14	IO58RSB0
A15	IO61RSB0
A16	IO62RSB0
A17	GBC1/IO73RSB0
A18	GBA0/IO76RSB0
A19	GND
B1	GAA2/IO225PPB3
B2	VCCIB0
B3	GAB1/IO03RSB0
B4	GAC0/IO04RSB0
B5	IO12RSB0
B6	GND
B7	IO21RSB0
B8	IO26RSB0
B9	IO34RSB0
B10	IO35RSB0
B11	IO36RSB0
B12	IO46RSB0
B13	IO52RSB0
B14	GND
B15	IO59RSB0
B16	GBC0/IO72RSB0
B17	GBA1/IO77RSB0
B18	VCCIB1
B19	IO79NDB1
C1	GAB2/IO224PPB3
C2	IO225NPB3
C6	IO18RSB0

TABLE 4-8: CS281 PIN DETAILS

CS281	
Pin Number	AGL1000 Function
C14	IO63RSB0
C18	IO78NPB1
C19	GBB2/IO79PDB1
D1	IO219PPB3
D2	IO223NPB3
D4	GAA0/IO00RSB0
D5	GAA1/IO01RSB0
D6	IO15RSB0
D7	IO19RSB0
D8	IO27RSB0
D9	IO32RSB0
D10	GND
D11	IO38RSB0
D12	IO44RSB0
D13	IO47RSB0
D14	IO60RSB0
D15	GBB0/IO74RSB0
D16	GBA2/IO78PPB1
D18	GBC2/IO80PPB1
D19	IO88NPB1
E1	IO217NPB3
E2	IO221PPB3
E4	IO221NPB3
E5	IO10RSB0
E6	IO14RSB0
E7	IO25RSB0
E8	IO28RSB0
E9	IO31RSB0
E10	IO33RSB0
E11	IO42RSB0
E12	IO49RSB0
E13	IO53RSB0
E14	GBB1/IO75RSB0
E15	IO80NPB1
E16	IO85PPB1
E18	IO83PPB1
E19	IO84NPB1
F1	IO214NPB3
F2	GND
F3	IO217PPB3
F4	IO219NPB3

TABLE 4-8: CS281 PIN DETAILS

CS281	
Pin Number	AGL1000 Function
F5	IO224NPB3
F15	IO85NPB1
F16	IO84PPB1
F17	IO83NPB1
F18	GND
F19	IO90PPB1
G1	IO212NPB3
G2	IO211NDB3
G4	IO214PPB3
G5	IO212PPB3
G7	GAC2/IO223PPB3
G8	VCCIB0
G9	IO30RSB0
G10	IO37RSB0
G11	IO43RSB0
G12	VCCIB0
G13	IO88PPB1
G15	IO89NDB1
G16	IO89PDB1
G18	GCC0/IO91NPB1
G19	GCB1/IO92PPB1
H1	GFB0/IO208NPB3
H2	IO211PDB3
H4	GFC1/IO209PPB3
H5	GFB1/IO208PPB3
H7	VCCIB3
H8	VCC
H9	VCCIB0
H10	VCC
H11	VCCIB0
H12	VCC
H13	VCCIB1
H15	IO90NPB1
H16	GCB0/IO92NPB1
H18	GCA1/IO93PPB1
H19	GCA2/IO94PPB1
J1	VCOMPLF
J2	GFA0/IO207NDB3
J4	VCCPLF
J5	GFC0/IO209NPB3
J7	GFA2/IO206PDB3

TABLE 4-8: CS281 PIN DETAILS

CS281	
Pin Number	AGL1000 Function
J8	VCCIB3
J9	GND
J10	GND
J11	GND
J12	VCCIB1
J13	GCC1/IO91PPB1
J15	GCA0/IO93NPB1
J16	GCB2/IO95PPB1
J18	IO94NPB1
J19	IO102PSB1
K1	VCCIB3
K2	GFA1/IO207PDB3
K4	GND
K5	IO204NPB3
K7	IO206NDB3
K8	VCC
K9	GND
K10	GND
K11	GND
K12	VCC
K13	GCC2/IO96PPB1
K15	IO95NPB1
K16	GND
K18	IO96NPB1
K19	VCCIB1
L1	GFB2/IO205PDB3
L2	IO205NDB3
L4	GFC2/IO204PPB3
L5	IO203PPB3
L7	IO203NPB3
L8	VCCIB3
L9	GND
L10	GND
L11	GND
L12	VCCIB1
L13	IO103PPB1
L15	IO103NPB1
L16	IO97PPB1
L18	IO98NPB1
L19	IO97NPB1
M1	IO202PDB3

TABLE 4-8: CS281 PIN DETAILS

CS281	
Pin Number	AGL1000 Function
M2	IO202NDB3
M4	IO201NPB3
M5	IO198PPB3
M7	VCCIB3
M8	VCC
M9	VCCIB2
M10	VCC
M11	VCCIB2
M12	VCC
M13	VCCIB1
M15	IO104NPB1
M16	IO100NPB1
M18	IO104PPB1
M19	IO98PPB1
N1	IO201PPB3
N2	IO198NPB3
N4	IO196PPB3
N5	IO197NPB3
N7	GEA2/IO187RSB2
N8	VCCIB2
N9	IO155RSB2
N10	IO154RSB2
N11	IO150RSB2
N12	VCCIB2
N13	VPUMP
N15	IO107PPB1
N16	IO105PPB1
N18	IO107NPB1
N19	IO100PPB1
P1	IO195PDB3
P2	GND
P3	IO195NDB3
P4	IO194PPB3
P5	GEA0/IO188NPB3
P15	IO108NDB1
P16	IO108PDB1
P17	GDC1/IO111PPB1
P18	GND
P19	IO105NPB1
R1	IO196NPB3
R2	IO194NPB3

TABLE 4-8: CS281 PIN DETAILS

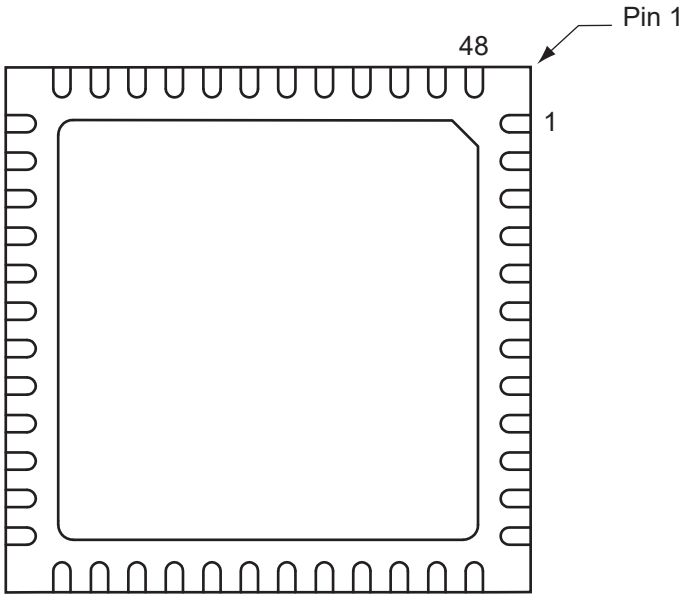
CS281	
Pin Number	AGL1000 Function
R4	GEC1/IO190PPB3
R5	GEB1/IO189PPB3
R6	IO184RSB2
R7	IO173RSB2
R8	IO168RSB2
R9	IO160RSB2
R10	IO151RSB2
R11	IO141RSB2
R12	IO136RSB2
R13	IO127RSB2
R14	IO124RSB2
R15	IO122RSB2
R16	GDA1/IO113PPB1
R18	GDB0/IO112NPB1
R19	GDC0/IO111NPB1
T1	IO197PPB3
T2	GEC0/IO190NPB3
T4	GEB0/IO189NPB3
T5	IO181RSB2
T6	IO172RSB2
T7	IO171RSB2
T8	IO156RSB2
T9	IO159RSB2
T10	GND
T11	IO139RSB2
T12	IO138RSB2
T13	IO129RSB2
T14	IO123RSB2
T15	GDC2/IO116RSB2
T16	TMS
T18	VJTAG
T19	GDB1/IO112PPB1
U1	IO193PDB3
U2	GEA1/IO188PPB3
U6	IO167RSB2
U14	IO128RSB2
U18	TRST
U19	GDA0/IO113NPB1
V1	IO193NDB3
V2	VCCIB3
V3	GEC2/IO185RSB2

TABLE 4-8: CS281 PIN DETAILS

CS281	
Pin Number	**AGL1000 Function**
V4	IO182RSB2
V5	IO175RSB2
V6	GND
V7	IO161RSB2
V8	IO143RSB2
V9	IO146RSB2
V10	IO145RSB2
V11	IO144RSB2
V12	IO134RSB2
V13	IO133RSB2
V14	GND
V15	IO119RSB2
V16	GDA2/IO114RSB2
V17	TDI
V18	VCCIB2
V19	TDO
W1	GND
W2	FF/GEB2/IO186RSB2
W3	IO183RSB2
W4	IO176RSB2
W5	IO170RSB2
W6	IO162RSB2
W7	IO157RSB2
W8	IO152RSB2
W9	IO149RSB2
W10	VCCIB2
W11	IO140RSB2
W12	IO135RSB2
W13	IO130RSB2
W14	IO125RSB2
W15	IO120RSB2
W16	IO118RSB2
W17	GDB2/IO115RSB2
W18	TCK
W19	GND

4.6 QN48

FIGURE 4-6: QN48—BOTTOM-VIEW



Note: The die attach paddle center of the package is tied to ground (GND).

Note: For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

TABLE 4-9: QN48 PIN DETAILS

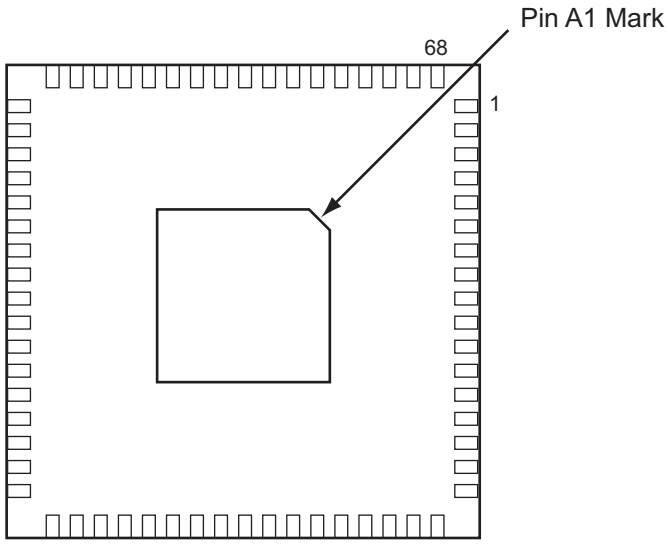
QN48	
Pin Number	**AGL030 Function**
1	IO82RSB1
2	GEC0/IO73RSB1
3	GEA0/IO72RSB1
4	GEB0/IO71RSB1
5	GND
6	VCCIB1
7	IO68RSB1
8	IO67RSB1
9	IO66RSB1
10	IO65RSB1
11	IO64RSB1
12	IO62RSB1
13	IO61RSB1
14	FF/IO60RSB1
15	IO57RSB1
16	IO55RSB1
17	IO53RSB1
18	VCC
19	VCCIB1
20	IO46RSB1
21	IO42RSB1
22	TCK
23	TDI
24	TMS
25	VPUMP
26	TDO
27	TRST
28	VJTAG
29	IO38RSB0
30	GDB0/IO34RSB0
31	GDA0/IO33RSB0
32	GDC0/IO32RSB0
33	VCCIB0
34	GND
35	VCC
36	IO25RSB0
37	IO24RSB0
38	IO22RSB0
39	IO20RSB0
40	IO18RSB0
41	IO16RSB0
42	IO14RSB0

TABLE 4-9: QN48 PIN DETAILS

QN48	
Pin Number	**AGL030 Function**
43	IO10RSB0
44	IO08RSB0
45	IO06RSB0
46	IO04RSB0
47	IO02RSB0
48	IO00RSB0

4.7 QN68

FIGURE 4-7: QN68—BOTTOM-VIEW



Note: The die attach paddle center of the package is tied to ground (GND).

Note: For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

TABLE 4-10: QN68 PIN DETAILS

QN68	
Pin Number	**AGL015 Function**
1	IO82RSB1
2	IO80RSB1
3	IO78RSB1
4	IO76RSB1
5	GEC0/IO73RSB1
6	GEA0/IO72RSB1
7	GEB0/IO71RSB1
8	VCC
9	GND
10	VCCIB1
11	IO68RSB1
12	IO67RSB1
13	IO66RSB1
14	IO65RSB1
15	IO64RSB1
16	IO63RSB1
17	IO62RSB1
18	FF/IO60RSB1
19	IO58RSB1
20	IO56RSB1
21	IO54RSB1
22	IO52RSB1
23	IO51RSB1
24	VCC
25	GND
26	VCCIB1
27	IO50RSB1
28	IO48RSB1
29	IO46RSB1
30	IO44RSB1
31	IO42RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO
37	TRST
38	VJTAG
39	IO40RSB0
40	IO37RSB0
41	GDB0/IO34RSB0
42	GDA0/IO33RSB0

TABLE 4-10: QN68 PIN DETAILS

QN68	
Pin Number	**AGL015 Function**
43	GDC0/IO32RSB0
44	VCCIB0
45	GND
46	VCC
47	IO31RSB0
48	IO29RSB0
49	IO28RSB0
50	IO27RSB0
51	IO25RSB0
52	IO24RSB0
53	IO22RSB0
54	IO21RSB0
55	IO19RSB0
56	IO17RSB0
57	IO15RSB0
58	IO14RSB0
59	VCCIB0
60	GND
61	VCC
62	IO12RSB0
63	IO10RSB0
64	IO08RSB0
65	IO06RSB0
66	IO04RSB0
67	IO02RSB0
68	IO00RSB0

TABLE 4-11: QN68 PIN DETAILS

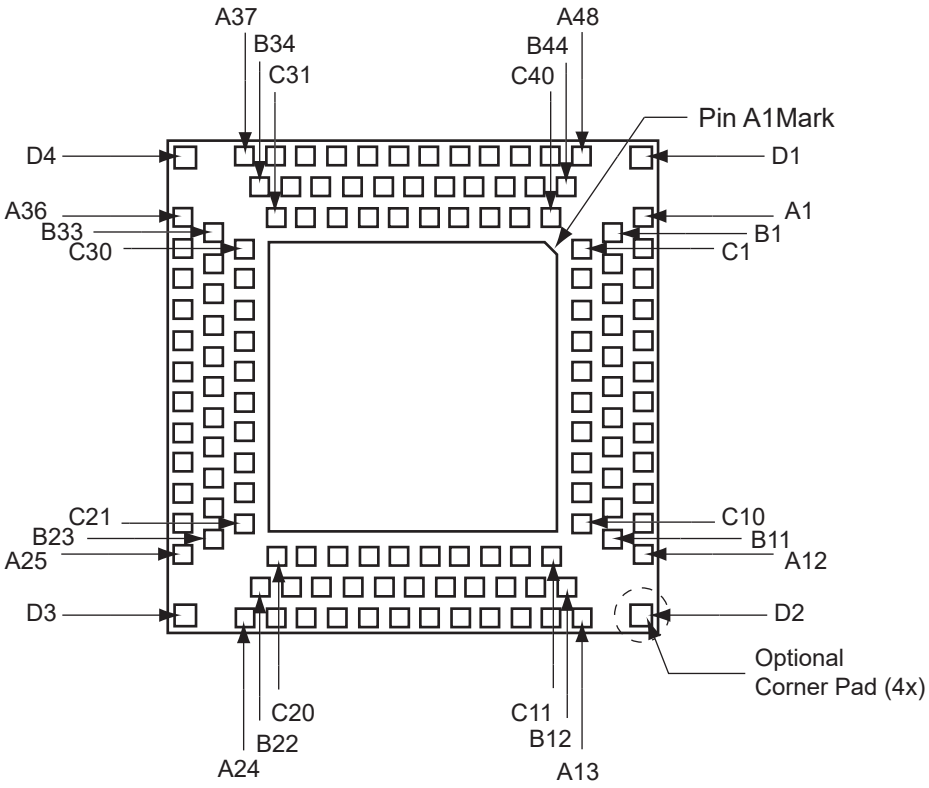
QN68	
Pin Number	**AGL030 Function**
1	IO82RSB1
2	IO80RSB1
3	IO78RSB1
4	IO76RSB1
5	GEC0/IO73RSB1
6	GEA0/IO72RSB1
7	GEB0/IO71RSB1
8	VCC
9	GND
10	VCCIB1
11	IO68RSB1
12	IO67RSB1
13	IO66RSB1
14	IO65RSB1
15	IO64RSB1
16	IO63RSB1
17	IO62RSB1
18	FF/IO60RSB1
19	IO58RSB1
20	IO56RSB1
21	IO54RSB1
22	IO52RSB1
23	IO51RSB1
24	VCC
25	GND
26	VCCIB1
27	IO50RSB1
28	IO48RSB1
29	IO46RSB1
30	IO44RSB1
31	IO42RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO
37	TRST
38	VJTAG
39	IO40RSB0
40	IO37RSB0
41	GDB0/IO34RSB0
42	GDA0/IO33RSB0

TABLE 4-11: QN68 PIN DETAILS

QN68	
Pin Number	**AGL030 Function**
43	GDC0/IO32RSB0
44	VCCIB0
45	GND
46	VCC
47	IO31RSB0
48	IO29RSB0
49	IO28RSB0
50	IO27RSB0
51	IO25RSB0
52	IO24RSB0
53	IO22RSB0
54	IO21RSB0
55	IO19RSB0
56	IO17RSB0
57	IO15RSB0
58	IO14RSB0
59	VCCIB0
60	GND
61	VCC
62	IO12RSB0
63	IO10RSB0
64	IO08RSB0
65	IO06RSB0
66	IO04RSB0
67	IO02RSB0
68	IO00RSB0

4.8 QN132

FIGURE 4-8: QN132—BOTTOM-VIEW



Note: The die attach paddle center of the package is tied to ground (GND).

Note: QN132 package is discontinued and is not available for IGLOO devices. For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

TABLE 4-12: QN132 PIN DETAILS

QN132	
Pin Number	**AGL030 Function**
A1	IO80RSB1
A2	IO77RSB1
A3	NC
A4	IO76RSB1
A5	GEC0/IO73RSB1
A6	NC
A7	GEB0/IO71RSB1
A8	IO69RSB1
A9	NC
A10	VCC
A11	IO67RSB1
A12	IO64RSB1
A13	IO59RSB1
A14	IO56RSB1
A15	NC
A16	IO55RSB1
A17	IO53RSB1
A18	VCC
A19	IO50RSB1
A20	IO48RSB1
A21	IO45RSB1
A22	IO44RSB1
A23	IO43RSB1
A24	TDI
A25	TRST
A26	IO40RSB0
A27	NC
A28	IO39RSB0
A29	IO38RSB0
A30	IO36RSB0
A31	IO35RSB0
A32	GDC0/IO32RSB0
A33	NC
A34	VCC
A35	IO30RSB0
A36	IO27RSB0
A37	IO22RSB0
A38	IO19RSB0
A39	NC
A40	IO18RSB0
A41	IO16RSB0
A42	IO14RSB0

TABLE 4-12: QN132 PIN DETAILS

QN132	
Pin Number	**AGL030 Function**
A43	VCC
A44	IO11RSB0
A45	IO08RSB0
A46	IO06RSB0
A47	IO05RSB0
A48	IO02RSB0
B1	IO81RSB1
B2	IO78RSB1
B3	GND
B4	IO75RSB1
B5	NC
B6	GND
B7	IO70RSB1
B8	NC
B9	GND
B10	IO66RSB1
B11	IO63RSB1
B12	FF/IO60RSB1
B13	IO57RSB1
B14	GND
B15	IO54RSB1
B16	IO52RSB1
B17	GND
B18	IO49RSB1
B19	IO46RSB1
B20	GND
B21	IO42RSB1
B22	TMS
B23	TDO
B24	IO41RSB0
B25	GND
B26	NC
B27	IO37RSB0
B28	GND
B29	GDA0/IO33RSB0
B30	NC
B31	GND
B32	IO29RSB0
B33	IO26RSB0
B34	IO23RSB0
B35	IO20RSB0
B36	GND

TABLE 4-12: QN132 PIN DETAILS

QN132	
Pin Number	**AGL030 Function**
B37	IO17RSB0
B38	IO15RSB0
B39	GND
B40	IO12RSB0
B41	IO09RSB0
B42	GND
B43	IO04RSB0
B44	IO01RSB0
C1	IO82RSB1
C2	IO79RSB1
C3	NC
C4	IO74RSB1
C5	GEA0/IO72RSB1
C6	NC
C7	NC
C8	VCCIB1
C9	IO65RSB1
C10	IO62RSB1
C11	IO61RSB1
C12	IO58RSB1
C13	NC
C14	NC
C15	IO51RSB1
C16	VCCIB1
C17	IO47RSB1
C18	NC
C19	TCK
C20	NC
C21	VPUMP
C22	VJTAG
C23	NC
C24	NC
C25	NC
C26	GDB0/IO34RSB0
C27	NC
C28	VCCIB0
C29	IO28RSB0
C30	IO25RSB0
C31	IO24RSB0
C32	IO21RSB0
C33	NC
C34	NC

TABLE 4-12: QN132 PIN DETAILS

QN132	
Pin Number	**AGL030 Function**
C35	VCCIB0
C36	IO13RSB0
C37	IO10RSB0
C38	IO07RSB0
C39	IO03RSB0
C40	IO00RSB0
D1	GND
D2	GND
D3	GND
D4	GND

TABLE 4-13: QN132 PIN DETAILS

QN132	
Pin Number	**AGL060 Function**
A1	GAB2/IO00RSB1
A2	IO93RSB1
A3	VCCIB1
A4	GFC1/IO89RSB1
A5	GFB0/IO86RSB1
A6	VCCPLF
A7	GFA1/IO84RSB1
A8	GFC2/IO81RSB1
A9	IO78RSB1
A10	VCC
A11	GEB1/IO75RSB1
A12	GEA0/IO72RSB1
A13	GEC2/IO69RSB1
A14	IO65RSB1
A15	VCC
A16	IO64RSB1
A17	IO63RSB1
A18	IO62RSB1
A19	IO61RSB1
A20	IO58RSB1
A21	GDB2/IO55RSB1
A22	NC
A23	GDA2/IO54RSB1
A24	TDI
A25	TRST
A26	GDC1/IO48RSB0
A27	VCC
A28	IO47RSB0
A29	GCC2/IO46RSB0
A30	GCA2/IO44RSB0
A31	GCA0/IO43RSB0
A32	GCB1/IO40RSB0
A33	IO36RSB0
A34	VCC
A35	IO31RSB0
A36	GBA2/IO28RSB0
A37	GBB1/IO25RSB0
A38	GBC0/IO22RSB0
A39	VCCIB0
A40	IO21RSB0
A41	IO18RSB0
A42	IO15RSB0

TABLE 4-13: QN132 PIN DETAILS

QN132	
Pin Number	**AGL060 Function**
A43	IO14RSB0
A44	IO11RSB0
A45	GAB1/IO08RSB0
A46	NC
A47	GAB0/IO07RSB0
A48	IO04RSB0
B1	IO01RSB1
B2	GAC2/IO94RSB1
B3	GND
B4	GFC0/IO88RSB1
B5	VCOMPLF
B6	GND
B7	GFB2/IO82RSB1
B8	IO79RSB1
B9	GND
B10	GEB0/IO74RSB1
B11	VMV1
B12	FF/GEB2/ IO70RSB1
B13	IO67RSB1
B14	GND
B15	NC
B16	NC
B17	GND
B18	IO59RSB1
B19	GDC2/IO56RSB1
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO49RSB0
B25	GND
B26	NC
B27	GCB2/IO45RSB0
B28	GND
B29	GCB0/IO41RSB0
B30	GCC1/IO38RSB0
B31	GND
B32	GBB2/IO30RSB0
B33	VMV0
B34	GBA0/IO26RSB0
B35	GBC1/IO23RSB0

TABLE 4-13: QN132 PIN DETAILS

QN132	
Pin Number	**AGL060 Function**
B36	GND
B37	IO20RSB0
B38	IO17RSB0
B39	GND
B40	IO12RSB0
B41	GAC0/IO09RSB0
B42	GND
B43	GAA1/IO06RSB0
B44	GNDQ
C1	GAA2/IO02RSB1
C2	IO95RSB1
C3	VCC
C4	GFB1/IO87RSB1
C5	GFA0/IO85RSB1
C6	GFA2/IO83RSB1
C7	IO80RSB1
C8	VCCIB1
C9	GEA1/IO73RSB1
C10	GNDQ
C11	GEA2/IO71RSB1
C12	IO68RSB1
C13	VCCIB1
C14	NC
C15	NC
C16	IO60RSB1
C17	IO57RSB1
C18	NC
C19	TCK
C20	VMV1
C21	VPUMP
C22	VJTAG
C23	VCCIB0
C24	NC
C25	NC
C26	GCA1/IO42RSB0
C27	GCC0/IO39RSB0
C28	VCCIB0
C29	IO29RSB0
C30	GNDQ
C31	GBA1/IO27RSB0
C32	GBB0/IO24RSB0
C33	VCC

TABLE 4-13: QN132 PIN DETAILS

QN132	
Pin Number	**AGL060 Function**
C34	IO19RSB0
C35	IO16RSB0
C36	IO13RSB0
C37	GAC1/IO10RSB0
C38	NC
C39	GAA0/IO05RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

TABLE 4-14: QN132 PIN DETAILS

QN132	
Pin Number	**AGL125 Function**
A1	GAB2/IO69RSB1
A2	IO130RSB1
A3	VCCIB1
A4	GFC1/IO126RSB1
A5	GFB0/IO123RSB1
A6	VCCPLF
A7	GFA1/IO121RSB1
A8	GFC2/IO118RSB1
A9	IO115RSB1
A10	VCC
A11	GEB1/IO110RSB1
A12	GEA0/IO107RSB1
A13	GEC2/IO104RSB1
A14	IO100RSB1
A15	VCC
A16	IO99RSB1
A17	IO96RSB1
A18	IO94RSB1
A19	IO91RSB1
A20	IO85RSB1
A21	IO79RSB1
A22	VCC
A23	GDB2/IO71RSB1
A24	TDI
A25	TRST
A26	GDC1/IO61RSB0
A27	VCC
A28	IO60RSB0
A29	GCC2/IO59RSB0
A30	GCA2/IO57RSB0
A31	GCA0/IO56RSB0
A32	GCB1/IO53RSB0
A33	IO49RSB0
A34	VCC
A35	IO44RSB0
A36	GBA2/IO41RSB0
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0

TABLE 4-14: QN132 PIN DETAILS

QN132	
Pin Number	**AGL125 Function**
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO68RSB1
B2	GAC2/IO131RSB1
B3	GND
B4	GFC0/IO125RSB1
B5	VCOMPLF
B6	GND
B7	GFB2/IO119RSB1
B8	IO116RSB1
B9	GND
B10	GEB0/IO109RSB1
B11	VMV1
B12	FF/GEB2/ IO105RSB1
B13	IO101RSB1
B14	GND
B15	IO98RSB1
B16	IO95RSB1
B17	GND
B18	IO87RSB1
B19	IO81RSB1
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO62RSB0
B25	GND
B26	NC
B27	GCB2/IO58RSB0
B28	GND
B29	GCB0/IO54RSB0
B30	GCC1/IO51RSB0
B31	GND
B32	GBB2/IO43RSB0
B33	VMV0
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0

TABLE 4-14: QN132 PIN DETAILS

QN132	
Pin Number	**AGL125 Function**
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO67RSB1
C2	IO132RSB1
C3	VCC
C4	GFB1/IO124RSB1
C5	GFA0/IO122RSB1
C6	GFA2/IO120RSB1
C7	IO117RSB1
C8	VCCIB1
C9	GEA1/IO108RSB1
C10	GNDQ
C11	GEA2/IO106RSB1
C12	IO103RSB1
C13	VCCIB1
C14	IO97RSB1
C15	IO93RSB1
C16	IO89RSB1
C17	IO83RSB1
C18	VCCIB1
C19	TCK
C20	VMV1
C21	VPUMP
C22	VJTAG
C23	VCCIB0
C24	NC
C25	NC
C26	GCA1/IO55RSB0
C27	GCC0/IO52RSB0
C28	VCCIB0
C29	IO42RSB0
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	VCC

TABLE 4-14: QN132 PIN DETAILS

QN132	
Pin Number	**AGL125 Function**
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	VCCIB0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

TABLE 4-15: QN132 PIN DETAILS

QN132	
Pin Number	**AGL250 Function**
A1	GAB2/IO117UPB3
A2	IO117VPB3
A3	VCCIB3
A4	GFC1/IO110PDB3
A5	GFB0/IO109NPB3
A6	VCCPLF
A7	GFA1/IO108PPB3
A8	GFC2/IO105PPB3
A9	IO103NDB3
A10	VCC
A11	GEA1/IO98PPB3
A12	GEA0/IO98NPB3
A13	GEC2/IO95RSB2
A14	IO91RSB2
A15	VCC
A16	IO90RSB2
A17	IO87RSB2
A18	IO85RSB2
A19	IO82RSB2
A20	IO76RSB2
A21	IO70RSB2
A22	VCC
A23	GDB2/IO62RSB2
A24	TDI
A25	TRST
A26	GDC1/IO58UDB1
A27	VCC
A28	IO54NDB1
A29	IO52NDB1
A30	GCA2/IO51PPB1
A31	GCA0/IO50NPB1
A32	GCB1/IO49PDB1
A33	IO47NSB1
A34	VCC
A35	IO41NPB1
A36	GBA2/IO41PPB1
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0

TABLE 4-15: QN132 PIN DETAILS

QN132	
Pin Number	**AGL250 Function**
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO118VDB3
B2	GAC2/IO116UDB3
B3	GND
B4	GFC0/IO110NDB3
B5	VCOMPLF
B6	GND
B7	GFB2/IO106PSB3
B8	IO103PDB3
B9	GND
B10	GEB0/IO99NDB3
B11	VMV3
B12	FF/GEB2/IO96RSB2
B13	IO92RSB2
B14	GND
B15	IO89RSB2
B16	IO86RSB2
B17	GND
B18	IO78RSB2
B19	IO72RSB2
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO58VDB1
B25	GND
B26	IO54PDB1
B27	GCB2/IO52PDB1
B28	GND
B29	GCB0/IO49NDB1
B30	GCC1/IO48PDB1
B31	GND
B32	GBB2/IO42PDB1
B33	VMV1
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND

TABLE 4-15: QN132 PIN DETAILS

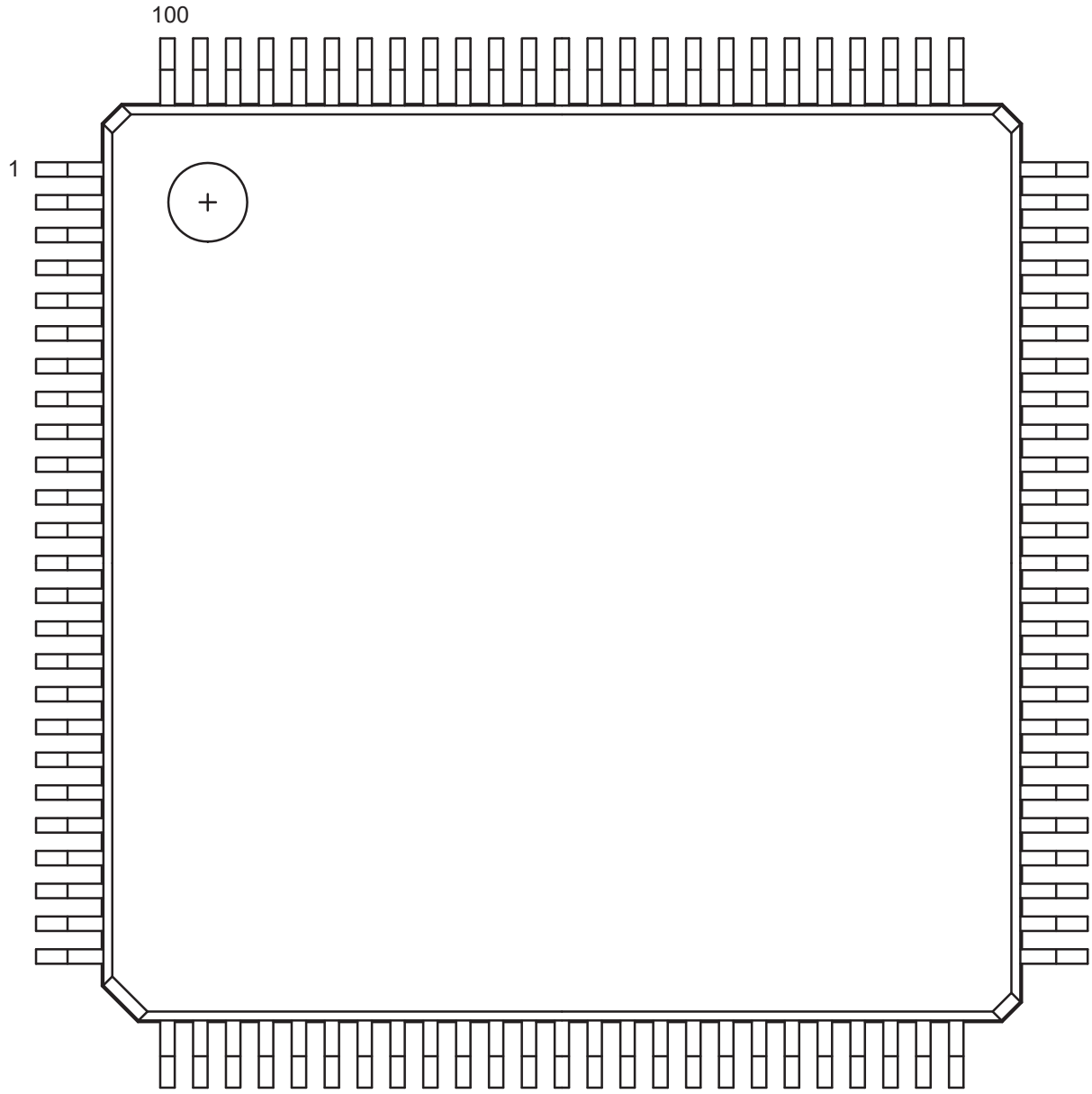
QN132	
Pin Number	**AGL250 Function**
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO118UDB3
C2	IO116VDB3
C3	VCC
C4	GFB1/IO109PPB3
C5	GFA0/IO108NPB3
C6	GFA2/IO107PSB3
C7	IO105NPB3
C8	VCCIB3
C9	GEB1/IO99PDB3
C10	GNDQ
C11	GEA2/IO97RSB2
C12	IO94RSB2
C13	VCCIB2
C14	IO88RSB2
C15	IO84RSB2
C16	IO80RSB2
C17	IO74RSB2
C18	VCCIB2
C19	TCK
C20	VMV2
C21	VPUMP
C22	VJTAG
C23	VCCIB1
C24	IO53NSB1
C25	IO51NPB1
C26	GCA1/IO50PPB1
C27	GCC0/IO48NDB1
C28	VCCIB1
C29	IO42NDB1
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	VCC
C34	IO24RSB0

TABLE 4-15: QN132 PIN DETAILS

QN132	
Pin Number	**AGL250 Function**
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	VCCIB0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

4.9 VQ100

FIGURE 4-9: VQ100—BOTTOM-VIEW



Note: For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

TABLE 4-16: VQ100 PIN DETAILS

VQ100	
Pin Number	**AGL030 Function**
1	GND
2	IO82RSB1
3	IO81RSB1
4	IO80RSB1
5	IO79RSB1
6	IO78RSB1
7	IO77RSB1
8	IO76RSB1
9	GND
10	IO75RSB1
11	IO74RSB1
12	GEC0/IO73RSB1
13	GEA0/IO72RSB1
14	GEB0/IO71RSB1
15	IO70RSB1
16	IO69RSB1
17	VCC
18	VCCIB1
19	IO68RSB1
20	IO67RSB1
21	IO66RSB1
22	IO65RSB1
23	IO64RSB1
24	IO63RSB1
25	IO62RSB1
26	IO61RSB1
27	FF/IO60RSB1
28	IO59RSB1
29	IO58RSB1
30	IO57RSB1
31	IO56RSB1
32	IO55RSB1
33	IO54RSB1
34	IO53RSB1
35	IO52RSB1
36	IO51RSB1
37	VCC
38	GND
39	VCCIB1
40	IO49RSB1
41	IO47RSB1
42	IO46RSB1

TABLE 4-16: VQ100 PIN DETAILS

VQ100	
Pin Number	**AGL030 Function**
43	IO45RSB1
44	IO44RSB1
45	IO43RSB1
46	IO42RSB1
47	TCK
48	TDI
49	TMS
50	NC
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	IO41RSB0
58	IO40RSB0
59	IO39RSB0
60	IO38RSB0
61	IO37RSB0
62	IO36RSB0
63	GDB0/IO34RSB0
64	GDA0/IO33RSB0
65	GDC0/IO32RSB0
66	VCCIB0
67	GND
68	VCC
69	IO31RSB0
70	IO30RSB0
71	IO29RSB0
72	IO28RSB0
73	IO27RSB0
74	IO26RSB0
75	IO25RSB0
76	IO24RSB0
77	IO23RSB0
78	IO22RSB0
79	IO21RSB0
80	IO20RSB0
81	IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO16RSB0

TABLE 4-16: VQ100 PIN DETAILS

VQ100	
Pin Number	**AGL030 Function**
85	IO15RSB0
86	IO14RSB0
87	VCCIB0
88	GND
89	VCC
90	IO12RSB0
91	IO10RSB0
92	IO08RSB0
93	IO07RSB0
94	IO06RSB0
95	IO05RSB0
96	IO04RSB0
97	IO03RSB0
98	IO02RSB0
99	IO01RSB0
100	IO00RSB0

TABLE 4-17: VQ100 PIN DETAILS

VQ100	
Pin Number	**AGL060 Function**
1	GND
2	GAA2/IO51RSB1
3	IO52RSB1
4	GAB2/IO53RSB1
5	IO95RSB1
6	GAC2/IO94RSB1
7	IO93RSB1
8	IO92RSB1
9	GND
10	GFB1/IO87RSB1
11	GFB0/IO86RSB1
12	VCOMPLF
13	GFA0/IO85RSB1
14	VCCPLF
15	GFA1/IO84RSB1
16	GFA2/IO83RSB1
17	VCC
18	VCCIB1
19	GEC1/IO77RSB1
20	GEB1/IO75RSB1
21	GEB0/IO74RSB1
22	GEA1/IO73RSB1
23	GEA0/IO72RSB1
24	VMV1
25	GNDQ
26	GEA2/IO71RSB1
27	FF/GEB2/IO70RSB1
28	GEC2/IO69RSB1
29	IO68RSB1
30	IO67RSB1
31	IO66RSB1
32	IO65RSB1
33	IO64RSB1
34	IO63RSB1
35	IO62RSB1
36	IO61RSB1
37	VCC
38	GND
39	VCCIB1
40	IO60RSB1
41	IO59RSB1
42	IO58RSB1

TABLE 4-17: VQ100 PIN DETAILS

VQ100	
Pin Number	**AGL060 Function**
43	IO57RSB1
44	GDC2/IO56RSB1
45	GDB2/IO55RSB1
46	GDA2/IO54RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO49RSB0
58	GDC0/IO46RSB0
59	GDC1/IO45RSB0
60	GCC2/IO43RSB0
61	GCB2/IO42RSB0
62	GCA0/IO40RSB0
63	GCA1/IO39RSB0
64	GCC0/IO36RSB0
65	GCC1/IO35RSB0
66	VCCIB0
67	GND
68	VCC
69	IO31RSB0
70	GBC2/IO29RSB0
71	GBB2/IO27RSB0
72	IO26RSB0
73	GBA2/IO25RSB0
74	VMV0
75	GNDQ
76	GBA1/IO24RSB0
77	GBA0/IO23RSB0
78	GBB1/IO22RSB0
79	GBB0/IO21RSB0
80	GBC1/IO20RSB0
81	GBC0/IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO15RSB0

TABLE 4-17: VQ100 PIN DETAILS

VQ100	
Pin Number	**AGL060 Function**
85	IO13RSB0
86	IO11RSB0
87	VCCIB0
88	GND
89	VCC
90	IO10RSB0
91	IO09RSB0
92	IO08RSB0
93	GAC1/IO07RSB0
94	GAC0/IO06RSB0
95	GAB1/IO05RSB0
96	GAB0/IO04RSB0
97	GAA1/IO03RSB0
98	GAA0/IO02RSB0
99	IO01RSB0
100	IO00RSB0

TABLE 4-18: VQ100 PIN DETAILS

VQ100	
Pin Number	**AGL125 Function**
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	VCOMPLF
13	GFA0/IO122RSB1
14	VCCPLF
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	VCC
18	VCCIB1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	FF/GEB2/ IO105RSB1
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1
36	IO93RSB1
37	VCC
38	GND
39	VCCIB1
40	IO87RSB1
41	IO84RSB1

TABLE 4-18: VQ100 PIN DETAILS

VQ100	
Pin Number	**AGL125 Function**
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	VCCIB0
67	GND
68	VCC
69	IO47RSB0
70	GBC2/IO45RSB0
71	GBB2/IO43RSB0
72	IO42RSB0
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0
83	IO28RSB0

TABLE 4-18: VQ100 PIN DETAILS

VQ100	
Pin Number	**AGL125 Function**
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0

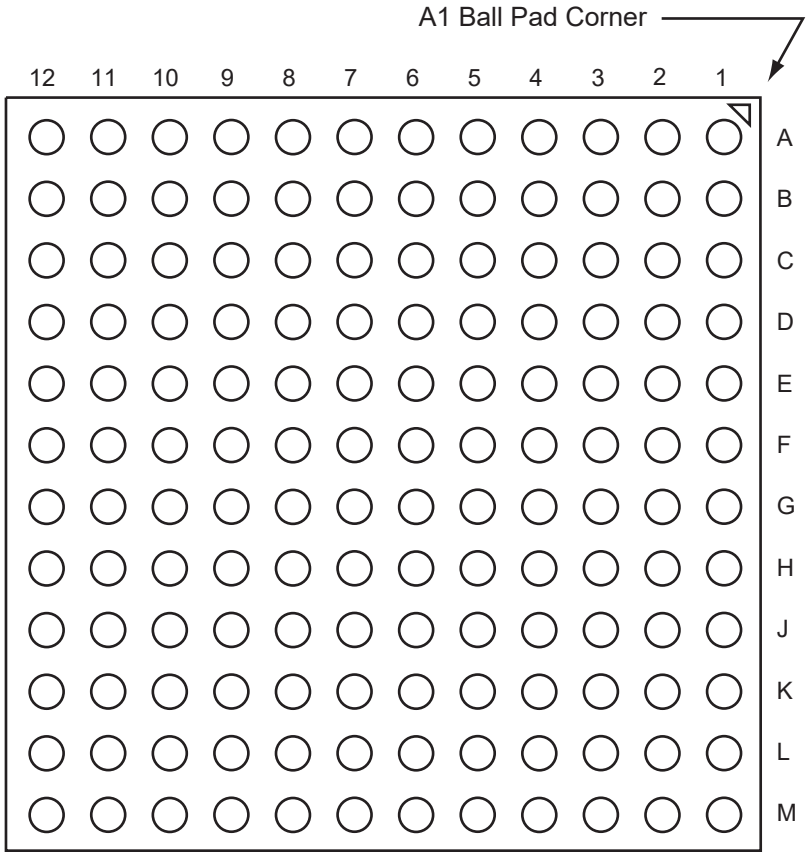
VQ100	
Pin Number	AGL250 Function
1	GND
2	GAA2/IO118UDB3
3	IO118VDB3
4	GAB2/IO117UDB3
5	IO117VDB3
6	GAC2/IO116UDB3
7	IO116VDB3
8	IO112PSB3
9	GND
10	GFB1/IO109PDB3
11	GFB0/IO109NDB3
12	VCOMPLF
13	GFA0/IO108NPB3
14	VCCPLF
15	GFA1/IO108PPB3
16	GFA2/IO107PSB3
17	VCC
18	VCCIB3
19	GFC2/IO105PSB3
20	GEC1/IO100PDB3
21	GEC0/IO100NDB3
22	GEA1/IO98PDB3
23	GEA0/IO98NDB3
24	VMV3
25	GNDQ
26	GEA2/IO97RSB2
27	FF/GEB2/IO96RSB2
28	GEC2/IO95RSB2
29	IO93RSB2
30	IO92RSB2
31	IO91RSB2
32	IO90RSB2
33	IO88RSB2
34	IO86RSB2
35	IO85RSB2
36	IO84RSB2
37	VCC
38	GND
39	VCCIB2
40	IO77RSB2
41	IO74RSB2
42	IO71RSB2
43	GDC2/IO63RSB2
44	GDB2/IO62RSB2

VQ100	
Pin Number	AGL250 Function
45	GDA2/IO61RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO60USB1
58	GDC0/IO58VDB1
59	GDC1/IO58UDB1
60	IO52NDB1
61	GCB2/IO52PDB1
62	GCA1/IO50PDB1
63	GCA0/IO50NDB1
64	GCC0/IO48NDB1
65	GCC1/IO48PDB1
66	VCCIB1
67	GND
68	VCC
69	IO43NDB1
70	GBC2/IO43PDB1
71	GBB2/IO42PSB1
72	IO41NDB1
73	GBA2/IO41PDB1
74	VMV1
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO29RSB0
83	IO27RSB0
84	IO25RSB0
85	IO23RSB0
86	IO21RSB0
87	VCCIB0
88	GND

VQ100	
Pin Number	AGL250 Function
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

4.10 FG144

FIGURE 4-10: FG144—BOTTOM-VIEW



Note: For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

TABLE 4-19: FG144 PIN DETAILS

FG144	
Pin Number	**AGL125 Function**
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO11RSB0
A6	GND
A7	IO18RSB0
A8	VCC
A9	IO25RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO69RSB1
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO08RSB0
B6	IO14RSB0
B7	IO19RSB0
B8	IO22RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV0
C1	IO132RSB1
C2	GFA2/IO120RSB1
C3	GAC2/IO131RSB1
C4	VCC
C5	IO10RSB0
C6	IO12RSB0
C7	IO21RSB0
C8	IO24RSB0
C9	IO27RSB0
C10	GBA2/IO41RSB0
C11	IO42RSB0
C12	GBC2/IO45RSB0
D1	IO128RSB1
D2	IO129RSB1
D3	IO130RSB1
D4	GAA2/IO67RSB1
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0

TABLE 4-19: FG144 PIN DETAILS

FG144	
Pin Number	**AGL125 Function**
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO43RSB0
D10	IO28RSB0
D11	IO44RSB0
D12	GCB1/IO53RSB0
E1	VCC
E2	GFC0/IO125RSB1
E3	GFC1/IO126RSB1
E4	VCCIB1
E5	IO68RSB1
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO51RSB0
E9	VCCIB0
E10	VCC
E11	GCA0/IO56RSB0
E12	IO46RSB0
F1	GFB0/IO123RSB1
F2	VCOMPLF
F3	GFB1/IO124RSB1
F4	IO127RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO52RSB0
F9	GCB0/IO54RSB0
F10	GND
F11	GCA1/IO55RSB0
F12	GCA2/IO57RSB0
G1	GFA1/IO121RSB1
G2	GND
G3	VCCPLF
G4	GFA0/IO122RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO61RSB0
G9	IO48RSB0
G10	GCC2/IO59RSB0
G11	IO47RSB0
G12	GCB2/IO58RSB0

TABLE 4-19: FG144 PIN DETAILS

FG144	
Pin Number	**AGL125 Function**
H1	VCC
H2	GFB2/IO119RSB1
H3	GFC2/IO118RSB1
H4	GEC1/IO112RSB1
H5	VCC
H6	IO50RSB0
H7	IO60RSB0
H8	GDB2/IO71RSB1
H9	GDC0/IO62RSB0
H10	VCCIB0
H11	IO49RSB0
H12	VCC
J1	GEB1/IO110RSB1
J2	IO115RSB1
J3	VCCIB1
J4	GEC0/IO111RSB1
J5	IO116RSB1
J6	IO117RSB1
J7	VCC
J8	TCK
J9	GDA2/IO70RSB1
J10	TDO
J11	GDA1/IO65RSB0
J12	GDB1/IO63RSB0
K1	GEB0/IO109RSB1
K2	GEA1/IO108RSB1
K3	GEA0/IO107RSB1
K4	GEA2/IO106RSB1
K5	IO100RSB1
K6	IO98RSB1
K7	GND
K8	IO73RSB1
K9	GDC2/IO72RSB1
K10	GND
K11	GDA0/IO66RSB0
K12	GDB0/IO64RSB0
L1	GND
L2	VMV1
L3	FF/GEB2/ IO105RSB1
L4	IO102RSB1
L5	VCCIB1

TABLE 4-19: FG144 PIN DETAILS

FG144	
Pin Number	**AGL125 Function**
L6	IO95RSB1
L7	IO85RSB1
L8	IO74RSB1
L9	TMS
L10	VJTAG
L11	VMV1
L12	TRST
M1	GNDQ
M2	GEC2/IO104RSB1
M3	IO103RSB1
M4	IO101RSB1
M5	IO97RSB1
M6	IO94RSB1
M7	IO86RSB1
M8	IO75RSB1
M9	TDI
M10	VCCIB1
M11	VPUMP
M12	GNDQ

TABLE 4-20: FG144 PIN DETAILS

FG144	
Pin Number	**AGL250 Function**
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO16RSB0
A6	GND
A7	IO29RSB0
A8	VCC
A9	IO33RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO117UDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO14RSB0
B6	IO19RSB0
B7	IO22RSB0
B8	IO30RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV1
C1	IO117VDB3
C2	GFA2/IO107PPB3
C3	GAC2/IO116UDB3
C4	VCC
C5	IO12RSB0
C6	IO17RSB0
C7	IO24RSB0
C8	IO31RSB0
C9	IO34RSB0
C10	GBA2/IO41PDB1
C11	IO41NDB1
C12	GBC2/IO43PPB1
D1	IO112NDB3
D2	IO112PDB3
D3	IO116VDB3
D4	GAA2/IO118UPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0

TABLE 4-20: FG144 PIN DETAILS

FG144	
Pin Number	**AGL250 Function**
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO42PDB1
D10	IO42NDB1
D11	IO43NPB1
D12	GCB1/IO49PPB1
E1	VCC
E2	GFC0/IO110NDB3
E3	GFC1/IO110PDB3
E4	VCCIB3
E5	IO118VPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO48PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO50NDB1
E12	IO51NDB1
F1	GFB0/IO109NPB3
F2	VCOMPLF
F3	GFB1/IO109PPB3
F4	IO107NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO48NDB1
F9	GCB0/IO49NPB1
F10	GND
F11	GCA1/IO50PDB1
F12	GCA2/IO51PDB1
G1	GFA1/IO108PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO108NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO58UPB1
G9	IO53NDB1
G10	GCC2/IO53PDB1
G11	IO52NDB1
G12	GCB2/IO52PDB1

TABLE 4-20: FG144 PIN DETAILS

FG144	
Pin Number	**AGL250 Function**
H1	VCC
H2	GFB2/IO106PDB3
H3	GFC2/IO105PSB3
H4	GEC1/IO100PDB3
H5	VCC
H6	IO79RSB2
H7	IO65RSB2
H8	GDB2/IO62RSB2
H9	GDC0/IO58VPB1
H10	VCCIB1
H11	IO54PSB1
H12	VCC
J1	GEB1/IO99PDB3
J2	IO106NDB3
J3	VCCIB3
J4	GEC0/IO100NDB3
J5	IO88RSB2
J6	IO81RSB2
J7	VCC
J8	TCK
J9	GDA2/IO61RSB2
J10	TDO
J11	GDA1/IO60UDB1
J12	GDB1/IO59UDB1
K1	GEB0/IO99NDB3
K2	GEA1/IO98PDB3
K3	GEA0/IO98NDB3
K4	GEA2/IO97RSB2
K5	IO90RSB2
K6	IO84RSB2
K7	GND
K8	IO66RSB2
K9	GDC2/IO63RSB2
K10	GND
K11	GDA0/IO60VDB1
K12	GDB0/IO59VDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO96RSB2
L4	IO91RSB2
L5	VCCIB2
L6	IO82RSB2

TABLE 4-20: FG144 PIN DETAILS

FG144	
Pin Number	**AGL250 Function**
L7	IO80RSB2
L8	IO72RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO95RSB2
M3	IO92RSB2
M4	IO89RSB2
M5	IO87RSB2
M6	IO85RSB2
M7	IO78RSB2
M8	IO76RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG144	
Pin Number	**AGL400 Function**
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO16RSB0
A6	GND
A7	IO30RSB0
A8	VCC
A9	IO34RSB0
A10	GBA0/IO58RSB0
A11	GBA1/IO59RSB0
A12	GNDQ
B1	GAB2/IO154UDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO14RSB0
B6	IO19RSB0
B7	IO23RSB0
B8	IO31RSB0
B9	GBB0/IO56RSB0
B10	GBB1/IO57RSB0
B11	GND
B12	VMV1
C1	IO154VDB3
C2	GFA2/IO144PPB3
C3	GAC2/IO153UDB3
C4	VCC
C5	IO12RSB0
C6	IO17RSB0
C7	IO25RSB0
C8	IO32RSB0
C9	IO53RSB0
C10	GBA2/IO60PDB1
C11	IO60NDB1
C12	GBC2/IO62PPB1
D1	IO149NDB3
D2	IO149PDB3
D3	IO153VDB3
D4	GAA2/IO155UPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO54RSB0
D8	GBC1/IO55RSB0

FG144	
Pin Number	**AGL400 Function**
D9	GBB2/IO61PDB1
D10	IO61NDB1
D11	IO62NPB1
D12	GCB1/IO68PPB1
E1	VCC
E2	GFC0/IO147NDB3
E3	GFC1/IO147PDB3
E4	VCCIB3
E5	IO155VPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO67PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO69NDB1
E12	IO70NDB1
F1	GFB0/IO146NPB3
F2	VCOMPLF
F3	GFB1/IO146PPB3
F4	IO144NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO67NDB1
F9	GCB0/IO68NPB1
F10	GND
F11	GCA1/IO69PDB1
F12	GCA2/IO70PDB1
G1	GFA1/IO145PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO145NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO77UPB1
G9	IO72NDB1
G10	GCC2/IO72PDB1
G11	IO71NDB1
G12	GCB2/IO71PDB1
H1	VCC
H2	GFB2/IO143PDB3
H3	GFC2/IO142PSB3
H4	GEC1/IO137PDB3

FG144	
Pin Number	**AGL400 Function**
H5	VCC
H6	IO75PDB1
H7	IO75NDB1
H8	GDB2/IO81RSB2
H9	GDC0/IO77VPB1
H10	VCCIB1
H11	IO73PSB1
H12	VCC
J1	GEB1/IO136PDB3
J2	IO143NDB3
J3	VCCIB3
J4	GEC0/IO137NDB3
J5	IO125RSB2
J6	IO116RSB2
J7	VCC
J8	TCK
J9	GDA2/IO80RSB2
J10	TDO
J11	GDA1/IO79UDB1
J12	GDB1/IO78UDB1
K1	GEB0/IO136NDB3
K2	GEA1/IO135PDB3
K3	GEA0/IO135NDB3
K4	GEA2/IO134RSB2
K5	IO127RSB2
K6	IO121RSB2
K7	GND
K8	IO104RSB2
K9	GDC2/IO82RSB2
K10	GND
K11	GDA0/IO79VDB1
K12	GDB0/IO78VDB1
L1	GND
L2	VMV3
L3	FF/GEB2/ IO133RSB2
L4	IO128RSB2
L5	VCCIB2
L6	IO119RSB2
L7	IO114RSB2
L8	IO110RSB2
L9	TMS
L10	VJTAG
L11	VMV2

FG144	
Pin Number	**AGL400 Function**
L12	TRST
M1	GNDQ
M2	GEC2/IO132RSB2
M3	IO129RSB2
M4	IO126RSB2
M5	IO124RSB2
M6	IO122RSB2
M7	IO117RSB2
M8	IO115RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

TABLE 4-21: FG144 PIN DETAILS

FG144	
Pin Number	**AGL600 Function**
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO34RSB0
A8	VCC
A9	IO50RSB0
A10	GBA0/IO58RSB0
A11	GBA1/IO59RSB0
A12	GNDQ
B1	GAB2/IO173PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO19RSB0
B7	IO31RSB0
B8	IO39RSB0
B9	GBB0/IO56RSB0
B10	GBB1/IO57RSB0
B11	GND
B12	VMV1
C1	IO173NDB3
C2	GFA2/IO161PPB3
C3	GAC2/IO172PDB3
C4	VCC
C5	IO16RSB0
C6	IO25RSB0
C7	IO28RSB0
C8	IO42RSB0
C9	IO45RSB0
C10	GBA2/IO60PDB1
C11	IO60NDB1
C12	GBC2/IO62PPB1
D1	IO169PDB3
D2	IO169NDB3
D3	IO172NDB3
D4	GAA2/IO174PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0

TABLE 4-21: FG144 PIN DETAILS

FG144	
Pin Number	**AGL600 Function**
D7	GBC0/IO54RSB0
D8	GBC1/IO55RSB0
D9	GBB2/IO61PDB1
D10	IO61NDB1
D11	IO62NPB1
D12	GCB1/IO70PPB1
E1	VCC
E2	GFC0/IO164NDB3
E3	GFC1/IO164PDB3
E4	VCCIB3
E5	IO174NPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO69PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO71NDB1
E12	IO72NDB1
F1	GFB0/IO163NPB3
F2	VCOMPLF
F3	GFB1/IO163PPB3
F4	IO161NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO69NDB1
F9	GCB0/IO70NPB1
F10	GND
F11	GCA1/IO71PDB1
F12	GCA2/IO72PDB1
G1	GFA1/IO162PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO162NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO86PPB1
G9	IO74NDB1
G10	GCC2/IO74PDB1
G11	IO73NDB1
G12	GCB2/IO73PDB1

TABLE 4-21: FG144 PIN DETAILS

FG144	
Pin Number	**AGL600 Function**
H1	VCC
H2	GFB2/IO160PDB3
H3	GFC2/IO159PSB3
H4	GEC1/IO146PDB3
H5	VCC
H6	IO80PDB1
H7	IO80NDB1
H8	GDB2/IO90RSB2
H9	GDC0/IO86NPB1
H10	VCCIB1
H11	IO84PSB1
H12	VCC
J1	GEB1/IO145PDB3
J2	IO160NDB3
J3	VCCIB3
J4	GEC0/IO146NDB3
J5	IO129RSB2
J6	IO131RSB2
J7	VCC
J8	TCK
J9	GDA2/IO89RSB2
J10	TDO
J11	GDA1/IO88PDB1
J12	GDB1/IO87PDB1
K1	GEB0/IO145NDB3
K2	GEA1/IO144PDB3
K3	GEA0/IO144NDB3
K4	GEA2/IO143RSB2
K5	IO119RSB2
K6	IO111RSB2
K7	GND
K8	IO94RSB2
K9	GDC2/IO91RSB2
K10	GND
K11	GDA0/IO88NDB1
K12	GDB0/IO87NDB1
L1	GND
L2	VMV3
L3	FF/GEB2/ IO142RSB2
L4	IO136RSB2
L5	VCCIB2

TABLE 4-21: FG144 PIN DETAILS

FG144	
Pin Number	**AGL600 Function**
L6	IO115RSB2
L7	IO103RSB2
L8	IO97RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO141RSB2
M3	IO138RSB2
M4	IO123RSB2
M5	IO126RSB2
M6	IO134RSB2
M7	IO108RSB2
M8	IO99RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

TABLE 4-22: FG144 PIN DETAILS

FG144	
Pin Number	**AGL1000 Function**
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO44RSB0
A8	VCC
A9	IO69RSB0
A10	GBA0/IO76RSB0
A11	GBA1/IO77RSB0
A12	GNDQ
B1	GAB2/IO224PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO26RSB0
B7	IO35RSB0
B8	IO60RSB0
B9	GBB0/IO74RSB0
B10	GBB1/IO75RSB0
B11	GND
B12	VMV1
C1	IO224NDB3
C2	GFA2/IO206PPB3
C3	GAC2/IO223PDB3
C4	VCC
C5	IO16RSB0
C6	IO29RSB0
C7	IO32RSB0
C8	IO63RSB0
C9	IO66RSB0
C10	GBA2/IO78PDB1
C11	IO78NDB1
C12	GBC2/IO80PPB1
D1	IO213PDB3
D2	IO213NDB3
D3	IO223NDB3
D4	GAA2/IO225PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0

TABLE 4-22: FG144 PIN DETAILS

FG144	
Pin Number	**AGL1000 Function**
D7	GBC0/IO72RSB0
D8	GBC1/IO73RSB0
D9	GBB2/IO79PDB1
D10	IO79NDB1
D11	IO80NPB1
D12	GCB1/IO92PPB1
E1	VCC
E2	GFC0/IO209NDB3
E3	GFC1/IO209PDB3
E4	VCCIB3
E5	IO225NPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO91PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO93NDB1
E12	IO94NDB1
F1	GFB0/IO208NPB3
F2	VCOMPLF
F3	GFB1/IO208PPB3
F4	IO206NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO91NDB1
F9	GCB0/IO92NPB1
F10	GND
F11	GCA1/IO93PDB1
F12	GCA2/IO94PDB1
G1	GFA1/IO207PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO207NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO111PPB1
G9	IO96NDB1
G10	GCC2/IO96PDB1
G11	IO95NDB1
G12	GCB2/IO95PDB1

TABLE 4-22: FG144 PIN DETAILS

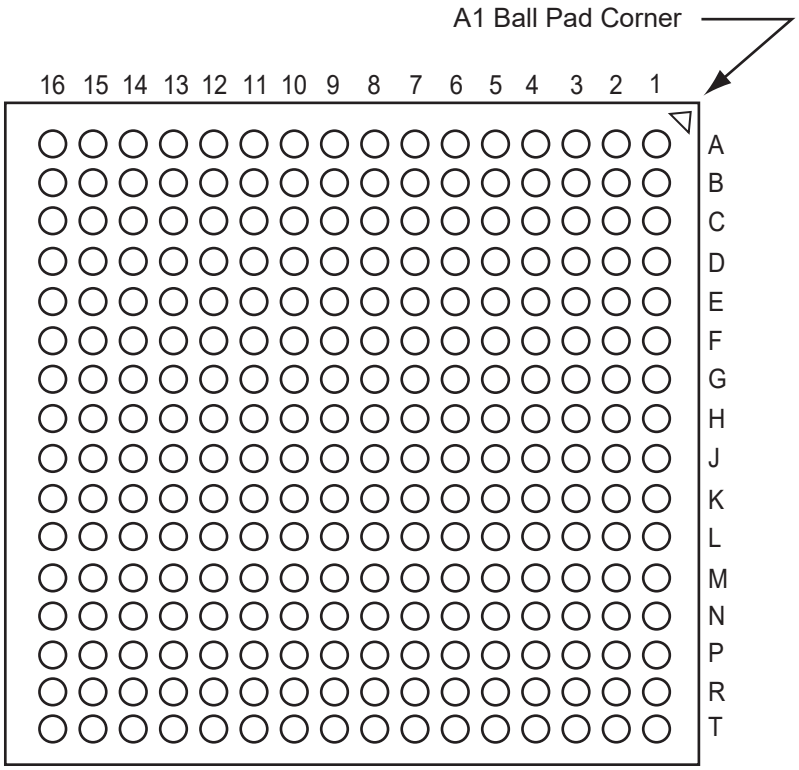
FG144	
Pin Number	**AGL1000 Function**
H1	VCC
H2	GFB2/IO205PDB3
H3	GFC2/IO204PSB3
H4	GEC1/IO190PDB3
H5	VCC
H6	IO105PDB1
H7	IO105NDB1
H8	GDB2/IO115RSB2
H9	GDC0/IO111NPB1
H10	VCCIB1
H11	IO101PSB1
H12	VCC
J1	GEB1/IO189PDB3
J2	IO205NDB3
J3	VCCIB3
J4	GEC0/IO190NDB3
J5	IO160RSB2
J6	IO157RSB2
J7	VCC
J8	TCK
J9	GDA2/IO114RSB2
J10	TDO
J11	GDA1/IO113PDB1
J12	GDB1/IO112PDB1
K1	GEB0/IO189NDB3
K2	GEA1/IO188PDB3
K3	GEA0/IO188NDB3
K4	GEA2/IO187RSB2
K5	IO169RSB2
K6	IO152RSB2
K7	GND
K8	IO117RSB2
K9	GDC2/IO116RSB2
K10	GND
K11	GDA0/IO113NDB1
K12	GDB0/IO112NDB1
L1	GND
L2	VMV3
L3	FF/GEB2/ IO186RSB2
L4	IO172RSB2
L5	VCCIB2

TABLE 4-22: FG144 PIN DETAILS

FG144	
Pin Number	**AGL1000 Function**
L6	IO153RSB2
L7	IO144RSB2
L8	IO140RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO185RSB2
M3	IO173RSB2
M4	IO168RSB2
M5	IO161RSB2
M6	IO156RSB2
M7	IO145RSB2
M8	IO141RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

4.11 FG256

FIGURE 4-11: FG256—BOTTOM-VIEW



Note: For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

TABLE 4-23: FG256 PIN DETAILS

FG256	
Pin Number	**AGL400 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO17RSB0
A7	IO22RSB0
A8	IO28RSB0
A9	IO34RSB0
A10	IO37RSB0
A11	IO41RSB0
A12	IO43RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO154UDB3
B2	GAA2/IO155UDB3
B3	IO12RSB0
B4	GAB1/IO03RSB0
B5	IO13RSB0
B6	IO14RSB0
B7	IO21RSB0
B8	IO27RSB0
B9	IO32RSB0
B10	IO38RSB0
B11	IO42RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO44RSB0
B15	GBA2/IO60PDB1
B16	IO60NDB1
C1	IO154VDB3
C2	IO155VDB3
C3	IO11RSB0
C4	IO07RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO20RSB0
C8	IO24RSB0
C9	IO33RSB0
C10	IO39RSB0

TABLE 4-23: FG256 PIN DETAILS

FG256	
Pin Number	**AGL400 Function**
C11	IO45RSB0
C12	GBC0/IO54RSB0
C13	IO48RSB0
C14	VMV0
C15	IO61NPB1
C16	IO63PDB1
D1	IO151VDB3
D2	IO151UDB3
D3	GAC2/IO153UDB3
D4	IO06RSB0
D5	GNDQ
D6	IO10RSB0
D7	IO19RSB0
D8	IO26RSB0
D9	IO30RSB0
D10	IO40RSB0
D11	IO46RSB0
D12	GNDQ
D13	IO47RSB0
D14	GBB2/IO61PPB1
D15	IO53RSB0
D16	IO63NDB1
E1	IO150PDB3
E2	IO08RSB0
E3	IO153VDB3
E4	IO152VDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO25RSB0
E9	IO31RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO62PDB1
E14	IO65RSB1
E15	IO52RSB0
E16	IO66PDB1
F1	IO150NDB3
F2	IO149NPB3
F3	IO09RSB0
F4	IO152UDB3

TABLE 4-23: FG256 PIN DETAILS

FG256	
Pin Number	**AGL400 Function**
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO62NDB1
F14	IO49RSB0
F15	IO64PPB1
F16	IO66NDB1
G1	IO148NDB3
G2	IO148PDB3
G3	IO149PPB3
G4	GFC1/IO147PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1
G13	GCC1/IO67PPB1
G14	IO64NPB1
G15	IO73PDB1
G16	IO73NDB1
H1	GFB0/IO146NPB3
H2	GFA0/IO145NDB3
H3	GFB1/IO146PPB3
H4	VCOMPLF
H5	GFC0/IO147NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO67NPB1
H13	GCB1/IO68PPB1
H14	GCA0/IO69NPB1

TABLE 4-23: FG256 PIN DETAILS

FG256	
Pin Number	**AGL400 Function**
H15	NC
H16	GCB0/IO68NPB1
J1	GFA2/IO144PPB3
J2	GFA1/IO145PDB3
J3	VCCPLF
J4	IO143NDB3
J5	GFB2/IO143PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO71PPB1
J13	GCA1/IO69PPB1
J14	GCC2/IO72PPB1
J15	NC
J16	GCA2/IO70PDB1
K1	GFC2/IO142PDB3
K2	IO144NPB3
K3	IO141PPB3
K4	IO120RSB2
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO71NPB1
K14	IO74RSB1
K15	IO72NPB1
K16	IO70NDB1
L1	IO142NDB3
L2	IO141NPB3
L3	IO125RSB2
L4	IO139RSB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC

TABLE 4-23: FG256 PIN DETAILS

FG256	
Pin Number	**AGL400 Function**
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO78VPB1
L14	IO76VDB1
L15	IO76UDB1
L16	IO75PDB1
M1	IO140PDB3
M2	IO130RSB2
M3	IO138NPB3
M4	GEC0/IO137NPB3
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO108RSB2
M9	IO101RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO83RSB2
M14	GDB1/IO78UPB1
M15	GDC1/IO77UDB1
M16	IO75NDB1
N1	IO140NDB3
N2	IO138PPB3
N3	GEC1/IO137PPB3
N4	IO131RSB2
N5	GNDQ
N6	GEA2/IO134RSB2
N7	IO117RSB2
N8	IO111RSB2
N9	IO99RSB2
N10	IO94RSB2
N11	IO87RSB2
N12	GNDQ
N13	IO93RSB2
N14	VJTAG
N15	GDC0/IO77VDB1
N16	GDA1/IO79UDB1
P1	GEB1/IO136PDB3
P2	GEB0/IO136NDB3

TABLE 4-23: FG256 PIN DETAILS

FG256	
Pin Number	**AGL400 Function**
P3	VMV2
P4	IO129RSB2
P5	IO128RSB2
P6	IO122RSB2
P7	IO115RSB2
P8	IO110RSB2
P9	IO98RSB2
P10	IO95RSB2
P11	IO88RSB2
P12	IO84RSB2
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO79VDB1
R1	GEA1/IO135PDB3
R2	GEA0/IO135NDB3
R3	IO127RSB2
R4	GEC2/IO132RSB2
R5	IO123RSB2
R6	IO118RSB2
R7	IO112RSB2
R8	IO106RSB2
R9	IO100RSB2
R10	IO96RSB2
R11	IO89RSB2
R12	IO85RSB2
R13	GDB2/IO81RSB2
R14	TDI
R15	NC
R16	TDO
T1	GND
T2	IO126RSB2
T3	FF/GEB2/ IO133RSB2
T4	IO124RSB2
T5	IO116RSB2
T6	IO113RSB2
T7	IO107RSB2
T8	IO105RSB2
T9	IO102RSB2
T10	IO97RSB2
T11	IO92RSB2

TABLE 4-23: FG256 PIN DETAILS

FG256	
Pin Number	**AGL400 Function**
T12	GDC2/IO82RSB2
T13	IO86RSB2
T14	GDA2/IO80RSB2
T15	TMS
T16	GND

TABLE 4-24: FG256 PIN DETAILS

FG256	
Pin Number	**AGL600 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO11RSB0
A6	IO16RSB0
A7	IO18RSB0
A8	IO28RSB0
A9	IO34RSB0
A10	IO37RSB0
A11	IO41RSB0
A12	IO43RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO173PDB3
B2	GAA2/IO174PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO13RSB0
B6	IO14RSB0
B7	IO21RSB0
B8	IO27RSB0
B9	IO32RSB0
B10	IO38RSB0
B11	IO42RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO52RSB0
B15	GBA2/IO60PDB1
B16	IO60NDB1
C1	IO173NDB3
C2	IO174NDB3
C3	VMV3
C4	IO07RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO20RSB0
C8	IO24RSB0
C9	IO33RSB0
C10	IO39RSB0

TABLE 4-24: FG256 PIN DETAILS

FG256	
Pin Number	**AGL600 Function**
C11	IO44RSB0
C12	GBC0/IO54RSB0
C13	IO51RSB0
C14	VMV0
C15	IO61NPB1
C16	IO63PDB1
D1	IO171NDB3
D2	IO171PDB3
D3	GAC2/IO172PDB3
D4	IO06RSB0
D5	GNDQ
D6	IO10RSB0
D7	IO19RSB0
D8	IO26RSB0
D9	IO30RSB0
D10	IO40RSB0
D11	IO45RSB0
D12	GNDQ
D13	IO50RSB0
D14	GBB2/IO61PPB1
D15	IO53RSB0
D16	IO63NDB1
E1	IO166PDB3
E2	IO167NPB3
E3	IO172NDB3
E4	IO169NDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO25RSB0
E9	IO31RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO62PDB1
E14	IO67PPB1
E15	IO64PPB1
E16	IO66PDB1
F1	IO166NDB3
F2	IO168NPB3
F3	IO167PPB3
F4	IO169PDB3

TABLE 4-24: FG256 PIN DETAILS

FG256	
Pin Number	**AGL600 Function**
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO62NDB1
F14	IO64NPB1
F15	IO65PPB1
F16	IO66NDB1
G1	IO165NDB3
G2	IO165PDB3
G3	IO168PPB3
G4	GFC1/IO164PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1
G13	GCC1/IO69PPB1
G14	IO65NPB1
G15	IO75PDB1
G16	IO75NDB1
H1	GFB0/IO163NPB3
H2	GFA0/IO162NDB3
H3	GFB1/IO163PPB3
H4	VCOMPLF
H5	GFC0/IO164NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO69NPB1
H13	GCB1/IO70PPB1
H14	GCA0/IO71NPB1

TABLE 4-24: FG256 PIN DETAILS

FG256	
Pin Number	**AGL600 Function**
H15	IO67NPB1
H16	GCB0/IO70NPB1
J1	GFA2/IO161PPB3
J2	GFA1/IO162PDB3
J3	VCCPLF
J4	IO160NDB3
J5	GFB2/IO160PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO73PPB1
J13	GCA1/IO71PPB1
J14	GCC2/IO74PPB1
J15	IO80PPB1
J16	GCA2/IO72PDB1
K1	GFC2/IO159PDB3
K2	IO161NPB3
K3	IO156PPB3
K4	IO129RSB2
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO73NPB1
K14	IO80NPB1
K15	IO74NPB1
K16	IO72NDB1
L1	IO159NDB3
L2	IO156NPB3
L3	IO151PPB3
L4	IO158PSB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC

TABLE 4-24: FG256 PIN DETAILS

FG256	
Pin Number	**AGL600 Function**
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO87NPB1
L14	IO85NDB1
L15	IO85PDB1
L16	IO84PDB1
M1	IO150PDB3
M2	IO151NPB3
M3	IO147NPB3
M4	GEC0/IO146NPB3
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO117RSB2
M9	IO110RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO94RSB2
M14	GDB1/IO87PPB1
M15	GDC1/IO86PDB1
M16	IO84NDB1
N1	IO150NDB3
N2	IO147PPB3
N3	GEC1/IO146PPB3
N4	IO140RSB2
N5	GNDQ
N6	GEA2/IO143RSB2
N7	IO126RSB2
N8	IO120RSB2
N9	IO108RSB2
N10	IO103RSB2
N11	IO99RSB2
N12	GNDQ
N13	IO92RSB2
N14	VJTAG
N15	GDC0/IO86NDB1
N16	GDA1/IO88PDB1
P1	GEB1/IO145PDB3
P2	GEB0/IO145NDB3

TABLE 4-24: FG256 PIN DETAILS

FG256	
Pin Number	**AGL600 Function**
P3	VMV2
P4	IO138RSB2
P5	IO136RSB2
P6	IO131RSB2
P7	IO124RSB2
P8	IO119RSB2
P9	IO107RSB2
P10	IO104RSB2
P11	IO97RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO88NDB1
R1	GEA1/IO144PDB3
R2	GEA0/IO144NDB3
R3	IO139RSB2
R4	GEC2/IO141RSB2
R5	IO132RSB2
R6	IO127RSB2
R7	IO121RSB2
R8	IO114RSB2
R9	IO109RSB2
R10	IO105RSB2
R11	IO98RSB2
R12	IO96RSB2
R13	GDB2/IO90RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO137RSB2
T3	FF/GEB2/ IO142RSB2
T4	IO134RSB2
T5	IO125RSB2
T6	IO123RSB2
T7	IO118RSB2
T8	IO115RSB2
T9	IO111RSB2
T10	IO106RSB2
T11	IO102RSB2

TABLE 4-24: FG256 PIN DETAILS

FG256	
Pin Number	**AGL600 Function**
T12	GDC2/IO91RSB2
T13	IO93RSB2
T14	GDA2/IO89RSB2
T15	TMS
T16	GND

TABLE 4-25: FG256 PIN DETAILS

FG256	
Pin Number	**AGL1000 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO22RSB0
A7	IO28RSB0
A8	IO35RSB0
A9	IO45RSB0
A10	IO50RSB0
A11	IO55RSB0
A12	IO61RSB0
A13	GBB1/IO75RSB0
A14	GBA0/IO76RSB0
A15	GBA1/IO77RSB0
A16	GND
B1	GAB2/IO224PDB3
B2	GAA2/IO225PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO17RSB0
B6	IO21RSB0
B7	IO27RSB0
B8	IO34RSB0
B9	IO44RSB0
B10	IO51RSB0
B11	IO57RSB0
B12	GBC1/IO73RSB0
B13	GBB0/IO74RSB0
B14	IO71RSB0
B15	GBA2/IO78PDB1
B16	IO81PDB1
C1	IO224NDB3
C2	IO225NDB3
C3	VMV3
C4	IO11RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO25RSB0
C8	IO36RSB0
C9	IO42RSB0
C10	IO49RSB0

TABLE 4-25: FG256 PIN DETAILS

FG256	
Pin Number	**AGL1000 Function**
C11	IO56RSB0
C12	GBC0/IO72RSB0
C13	IO62RSB0
C14	VMV0
C15	IO78NDB1
C16	IO81NDB1
D1	IO222NDB3
D2	IO222PDB3
D3	GAC2/IO223PDB3
D4	IO223NDB3
D5	GNDQ
D6	IO23RSB0
D7	IO29RSB0
D8	IO33RSB0
D9	IO46RSB0
D10	IO52RSB0
D11	IO60RSB0
D12	GNDQ
D13	IO80NDB1
D14	GBB2/IO79PDB1
D15	IO79NDB1
D16	IO82NSB1
E1	IO217PDB3
E2	IO218PDB3
E3	IO221NDB3
E4	IO221PDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO38RSB0
E9	IO47RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO80PDB1
E14	IO83PPB1
E15	IO86PPB1
E16	IO87PDB1
F1	IO217NDB3
F2	IO218NDB3
F3	IO216PDB3
F4	IO216NDB3

TABLE 4-25: FG256 PIN DETAILS

FG256	
Pin Number	**AGL1000 Function**
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO83NPB1
F14	IO86NPB1
F15	IO90PPB1
F16	IO87NDB1
G1	IO210PSB3
G2	IO213NDB3
G3	IO213PDB3
G4	GFC1/IO209PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1
G13	GCC1/IO91PPB1
G14	IO90NPB1
G15	IO88PDB1
G16	IO88NDB1
H1	GFB0/IO208NPB3
H2	GFA0/IO207NDB3
H3	GFB1/IO208PPB3
H4	VCOMPLF
H5	GFC0/IO209NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO91NPB1
H13	GCB1/IO92PPB1
H14	GCA0/IO93NPB1

TABLE 4-25: FG256 PIN DETAILS

FG256	
Pin Number	**AGL1000 Function**
H15	IO96NPB1
H16	GCB0/IO92NPB1
J1	GFA2/IO206PSB3
J2	GFA1/IO207PDB3
J3	VCCPLF
J4	IO205NDB3
J5	GFB2/IO205PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO95PPB1
J13	GCA1/IO93PPB1
J14	GCC2/IO96PPB1
J15	IO100PPB1
J16	GCA2/IO94PSB1
K1	GFC2/IO204PDB3
K2	IO204NDB3
K3	IO203NDB3
K4	IO203PDB3
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO95NPB1
K14	IO100NPB1
K15	IO102NDB1
K16	IO102PDB1
L1	IO202NDB3
L2	IO202PDB3
L3	IO196PPB3
L4	IO193PPB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC

TABLE 4-25: FG256 PIN DETAILS

FG256	
Pin Number	**AGL1000 Function**
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO112NPB1
L14	IO106NDB1
L15	IO106PDB1
L16	IO107PDB1
M1	IO197NSB3
M2	IO196NPB3
M3	IO193NPB3
M4	GEC0/IO190NPB3
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO147RSB2
M9	IO136RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO110NDB1
M14	GDB1/IO112PPB1
M15	GDC1/IO111PDB1
M16	IO107NDB1
N1	IO194PSB3
N2	IO192PPB3
N3	GEC1/IO190PPB3
N4	IO192NPB3
N5	GNDQ
N6	GEA2/IO187RSB2
N7	IO161RSB2
N8	IO155RSB2
N9	IO141RSB2
N10	IO129RSB2
N11	IO124RSB2
N12	GNDQ
N13	IO110PDB1
N14	VJTAG
N15	GDC0/IO111NDB1
N16	GDA1/IO113PDB1
P1	GEB1/IO189PDB3
P2	GEB0/IO189NDB3

TABLE 4-25: FG256 PIN DETAILS

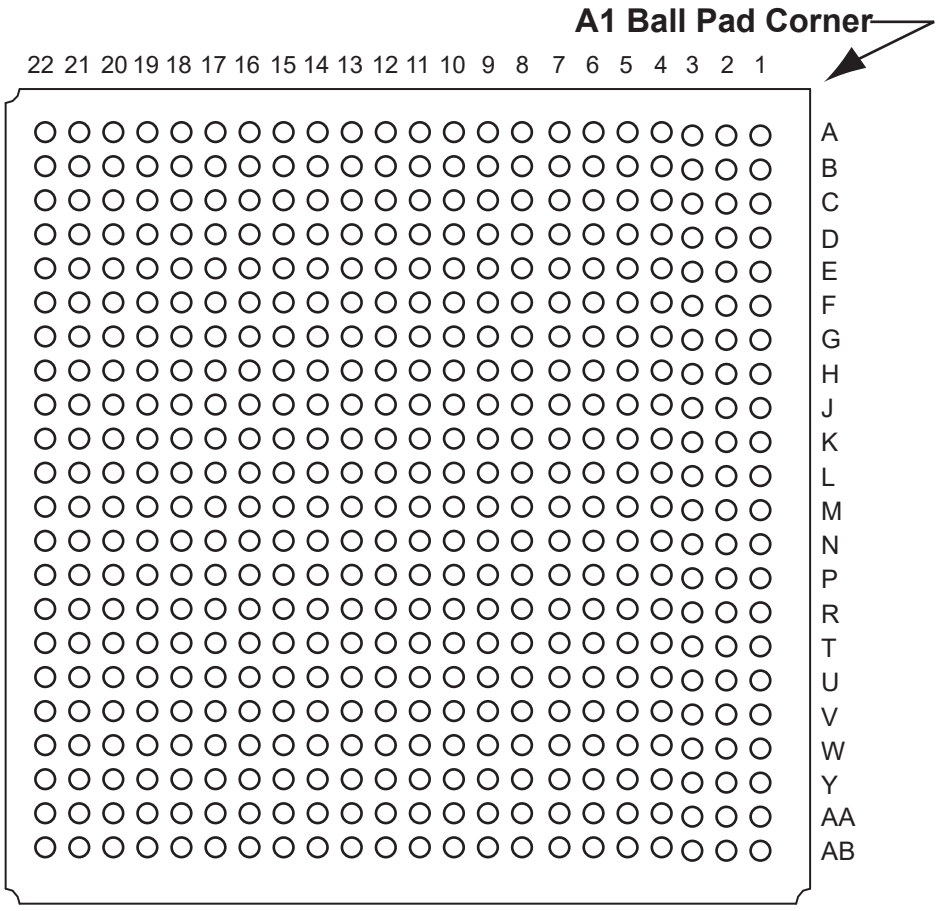
FG256	
Pin Number	**AGL1000 Function**
P3	VMV2
P4	IO179RSB2
P5	IO171RSB2
P6	IO165RSB2
P7	IO159RSB2
P8	IO151RSB2
P9	IO137RSB2
P10	IO134RSB2
P11	IO128RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO113NDB1
R1	GEA1/IO188PDB3
R2	GEA0/IO188NDB3
R3	IO184RSB2
R4	GEC2/IO185RSB2
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	FF/GEB2/ IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2

TABLE 4-25: FG256 PIN DETAILS

FG256	
Pin Number	**AGL1000 Function**
T12	GDC2/IO116RSB2
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

4.12 FG484

FIGURE 4-12: FG484—BOTTOM-VIEW



Note: For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

TABLE 4-26: FG484 PIN DETAILS

FG484	
Pin Number	**AGL400 Function**
A1	GND
A2	GND
A3	VCCIB0
A4	NC
A5	NC
A6	IO15RSB0
A7	IO18RSB0
A8	NC
A9	NC
A10	IO23RSB0
A11	IO29RSB0
A12	IO35RSB0
A13	IO36RSB0
A14	NC
A15	NC
A16	IO50RSB0
A17	IO51RSB0
A18	NC
A19	NC
A20	VCCIB0
A21	GND
A22	GND
AA1	GND
AA2	VCCIB3
AA3	NC
AA4	NC
AA5	NC
AA6	NC
AA7	NC
AA8	NC
AA9	NC
AA10	NC
AA11	NC
AA12	NC
AA13	NC
AA14	NC
AA15	NC
AA16	NC
AA17	NC
AA18	NC
AA19	NC
AA20	NC

TABLE 4-26: FG484 PIN DETAILS

FG484	
Pin Number	**AGL400 Function**
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	NC
AB5	NC
AB6	IO121RSB2
AB7	IO119RSB2
AB8	IO114RSB2
AB9	IO109RSB2
AB10	NC
AB11	NC
AB12	IO104RSB2
AB13	IO103RSB2
AB14	NC
AB15	NC
AB16	IO91RSB2
AB17	IO90RSB2
AB18	NC
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	NC
B5	NC
B6	NC
B7	NC
B8	NC
B9	NC
B10	NC
B11	NC
B12	NC
B13	NC
B14	NC
B15	NC
B16	NC
B17	NC
B18	NC

TABLE 4-26: FG484 PIN DETAILS

FG484	
Pin Number	**AGL400 Function**
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	NC
C8	VCC
C9	VCC
C10	NC
C11	NC
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC
C21	NC
C22	VCCIB1
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO16RSB0
D9	IO17RSB0
D10	IO22RSB0
D11	IO28RSB0
D12	IO34RSB0
D13	IO37RSB0
D14	IO41RSB0
D15	IO43RSB0
D16	GBB1/IO57RSB0

TABLE 4-26: FG484 PIN DETAILS

FG484	
Pin Number	**AGL400 Function**
D17	GBA0/IO58RSB0
D18	GBA1/IO59RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO154UDB3
E5	GAA2/IO155UDB3
E6	IO12RSB0
E7	GAB1/IO03RSB0
E8	IO13RSB0
E9	IO14RSB0
E10	IO21RSB0
E11	IO27RSB0
E12	IO32RSB0
E13	IO38RSB0
E14	IO42RSB0
E15	GBC1/IO55RSB0
E16	GBB0/IO56RSB0
E17	IO44RSB0
E18	GBA2/IO60PDB1
E19	IO60NDB1
E20	GND
E21	NC
E22	NC
F1	NC
F2	NC
F3	NC
F4	IO154VDB3
F5	IO155VDB3
F6	IO11RSB0
F7	IO07RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO20RSB0
F11	IO24RSB0
F12	IO33RSB0
F13	IO39RSB0
F14	IO45RSB0

TABLE 4-26: FG484 PIN DETAILS

FG484	
Pin Number	**AGL400 Function**
F15	GBC0/IO54RSB0
F16	IO48RSB0
F17	VMV0
F18	IO61NPB1
F19	IO63PDB1
F20	NC
F21	NC
F22	NC
G1	NC
G2	NC
G3	NC
G4	IO151VDB3
G5	IO151UDB3
G6	GAC2/IO153UDB3
G7	IO06RSB0
G8	GNDQ
G9	IO10RSB0
G10	IO19RSB0
G11	IO26RSB0
G12	IO30RSB0
G13	IO40RSB0
G14	IO46RSB0
G15	GNDQ
G16	IO47RSB0
G17	GBB2/IO61PPB1
G18	IO53RSB0
G19	IO63NDB1
G20	NC
G21	NC
G22	NC
H1	NC
H2	NC
H3	VCC
H4	IO150PDB3
H5	IO08RSB0
H6	IO153VDB3
H7	IO152VDB3
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO25RSB0
H12	IO31RSB0

TABLE 4-26: FG484 PIN DETAILS

FG484	
Pin Number	**AGL400 Function**
H13	VCCIB0
H14	VCCIB0
H15	VMV1
H16	GBC2/IO62PDB1
H17	IO65RSB1
H18	IO52RSB0
H19	IO66PDB1
H20	VCC
H21	NC
H22	NC
J1	NC
J2	NC
J3	NC
J4	IO150NDB3
J5	IO149NPB3
J6	IO09RSB0
J7	IO152UDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO62NDB1
J17	IO49RSB0
J18	IO64PPB1
J19	IO66NDB1
J20	NC
J21	NC
J22	NC
K1	NC
K2	NC
K3	NC
K4	IO148NDB3
K5	IO148PDB3
K6	IO149PPB3
K7	GFC1/IO147PPB3
K8	VCCIB3
K9	VCC
K10	GND

TABLE 4-26: FG484 PIN DETAILS

FG484	
Pin Number	**AGL400 Function**
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO67PPB1
K17	IO64NPB1
K18	IO73PDB1
K19	IO73NDB1
K20	NC
K21	NC
K22	NC
L1	NC
L2	NC
L3	NC
L4	GFB0/IO146NPB3
L5	GFA0/IO145NDB3
L6	GFB1/IO146PPB3
L7	VCOMPLF
L8	GFC0/IO147NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO67NPB1
L16	GCB1/IO68PPB1
L17	GCA0/IO69NPB1
L18	NC
L19	GCB0/IO68NPB1
L20	NC
L21	NC
L22	NC
M1	NC
M2	NC
M3	NC
M4	GFA2/IO144PPB3
M5	GFA1/IO145PDB3
M6	VCCPLF
M7	IO143NDB3
M8	GFB2/IO143PDB3

TABLE 4-26: FG484 PIN DETAILS

FG484	
Pin Number	**AGL400 Function**
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO71PPB1
M16	GCA1/IO69PPB1
M17	GCC2/IO72PPB1
M18	NC
M19	GCA2/IO70PDB1
M20	NC
M21	NC
M22	NC
N1	NC
N2	NC
N3	NC
N4	GFC2/IO142PDB3
N5	IO144NPB3
N6	IO141PPB3
N7	IO120RSB2
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO71NPB1
N17	IO74RSB1
N18	IO72NPB1
N19	IO70NDB1
N20	NC
N21	NC
N22	NC
P1	NC
P2	NC
P3	NC
P4	IO142NDB3
P5	IO141NPB3
P6	IO125RSB2

TABLE 4-26: FG484 PIN DETAILS

FG484	
Pin Number	**AGL400 Function**
P7	IO139RSB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO78VPB1
P17	IO76VDB1
P18	IO76UDB1
P19	IO75PDB1
P20	NC
P21	NC
P22	NC
R1	NC
R2	NC
R3	VCC
R4	IO140PDB3
R5	IO130RSB2
R6	IO138NPB3
R7	GEC0/IO137NPB3
R8	VMV3
R9	VCCIB2
R10	VCCIB2
R11	IO108RSB2
R12	IO101RSB2
R13	VCCIB2
R14	VCCIB2
R15	VMV2
R16	IO83RSB2
R17	GDB1/IO78UPB1
R18	GDC1/IO77UDB1
R19	IO75NDB1
R20	VCC
R21	NC
R22	NC
T1	NC
T2	NC
T3	NC
T4	IO140NDB3

TABLE 4-26: FG484 PIN DETAILS

FG484	
Pin Number	**AGL400 Function**
T5	IO138PPB3
T6	GEC1/IO137PPB3
T7	IO131RSB2
T8	GNDQ
T9	GEA2/IO134RSB2
T10	IO117RSB2
T11	IO111RSB2
T12	IO99RSB2
T13	IO94RSB2
T14	IO87RSB2
T15	GNDQ
T16	IO93RSB2
T17	VJTAG
T18	GDC0/IO77VDB1
T19	GDA1/IO79UDB1
T20	NC
T21	NC
T22	NC
U1	NC
U2	NC
U3	NC
U4	GEB1/IO136PDB3
U5	GEB0/IO136NDB3
U6	VMV2
U7	IO129RSB2
U8	IO128RSB2
U9	IO122RSB2
U10	IO115RSB2
U11	IO110RSB2
U12	IO98RSB2
U13	IO95RSB2
U14	IO88RSB2
U15	IO84RSB2
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO79VDB1
U20	NC
U21	NC
U22	NC
V1	NC
V2	NC

TABLE 4-26: FG484 PIN DETAILS

FG484	
Pin Number	**AGL400 Function**
V3	GND
V4	GEA1/IO135PDB3
V5	GEA0/IO135NDB3
V6	IO127RSB2
V7	GEC2/IO132RSB2
V8	IO123RSB2
V9	IO118RSB2
V10	IO112RSB2
V11	IO106RSB2
V12	IO100RSB2
V13	IO96RSB2
V14	IO89RSB2
V15	IO85RSB2
V16	GDB2/IO81RSB2
V17	TDI
V18	NC
V19	TDO
V20	GND
V21	NC
V22	NC
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO126RSB2
W6	FF/GEB2/ IO133RSB2
W7	IO124RSB2
W8	IO116RSB2
W9	IO113RSB2
W10	IO107RSB2
W11	IO105RSB2
W12	IO102RSB2
W13	IO97RSB2
W14	IO92RSB2
W15	GDC2/IO82RSB2
W16	IO86RSB2
W17	GDA2/IO80RSB2
W18	TMS
W19	GND
W20	NC
W21	NC

TABLE 4-26: FG484 PIN DETAILS

FG484	
Pin Number	**AGL400 Function**
W22	NC
Y1	VCCIB3
Y2	NC
Y3	NC
Y4	NC
Y5	GND
Y6	NC
Y7	NC
Y8	VCC
Y9	VCC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1

TABLE 4-27: FG484 PIN DETAILS

FG484	
Pin Number	**AGL600 Function**
A1	GND
A2	GND
A3	VCCIB0
A4	NC
A5	NC
A6	IO09RSB0
A7	IO15RSB0
A8	NC
A9	NC
A10	IO22RSB0
A11	IO23RSB0
A12	IO29RSB0
A13	IO35RSB0
A14	NC
A15	NC
A16	IO46RSB0
A17	IO48RSB0
A18	NC
A19	NC
A20	VCCIB0
A21	GND
A22	GND
AA1	GND
AA2	VCCIB3
AA3	NC
AA4	NC
AA5	NC
AA6	IO135RSB2
AA7	IO133RSB2
AA8	NC
AA9	NC
AA10	NC
AA11	NC
AA12	NC
AA13	NC
AA14	NC
AA15	NC
AA16	IO101RSB2
AA17	NC
AA18	NC
AA19	NC
AA20	NC

TABLE 4-27: FG484 PIN DETAILS

FG484	
Pin Number	**AGL600 Function**
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	NC
AB5	NC
AB6	IO130RSB2
AB7	IO128RSB2
AB8	IO122RSB2
AB9	IO116RSB2
AB10	NC
AB11	NC
AB12	IO113RSB2
AB13	IO112RSB2
AB14	NC
AB15	NC
AB16	IO100RSB2
AB17	IO95RSB2
AB18	NC
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	NC
B5	NC
B6	IO08RSB0
B7	IO12RSB0
B8	NC
B9	NC
B10	IO17RSB0
B11	NC
B12	NC
B13	IO36RSB0
B14	NC
B15	NC
B16	IO47RSB0
B17	IO49RSB0
B18	NC

TABLE 4-27: FG484 PIN DETAILS

FG484	
Pin Number	**AGL600 Function**
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	NC
C8	VCC
C9	VCC
C10	NC
C11	NC
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC
C21	NC
C22	VCCIB1
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO11RSB0
D9	IO16RSB0
D10	IO18RSB0
D11	IO28RSB0
D12	IO34RSB0
D13	IO37RSB0
D14	IO41RSB0
D15	IO43RSB0
D16	GBB1/IO57RSB0

TABLE 4-27: FG484 PIN DETAILS

FG484	
Pin Number	**AGL600 Function**
D17	GBA0/IO58RSB0
D18	GBA1/IO59RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO173PDB3
E5	GAA2/IO174PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO13RSB0
E9	IO14RSB0
E10	IO21RSB0
E11	IO27RSB0
E12	IO32RSB0
E13	IO38RSB0
E14	IO42RSB0
E15	GBC1/IO55RSB0
E16	GBB0/IO56RSB0
E17	IO52RSB0
E18	GBA2/IO60PDB1
E19	IO60NDB1
E20	GND
E21	NC
E22	NC
F1	NC
F2	NC
F3	NC
F4	IO173NDB3
F5	IO174NDB3
F6	VMV3
F7	IO07RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO20RSB0
F11	IO24RSB0
F12	IO33RSB0
F13	IO39RSB0
F14	IO44RSB0

TABLE 4-27: FG484 PIN DETAILS

FG484	
Pin Number	**AGL600 Function**
F15	GBC0/IO54RSB0
F16	IO51RSB0
F17	VMV0
F18	IO61NPB1
F19	IO63PDB1
F20	NC
F21	NC
F22	NC
G1	IO170NDB3
G2	IO170PDB3
G3	NC
G4	IO171NDB3
G5	IO171PDB3
G6	GAC2/IO172PDB3
G7	IO06RSB0
G8	GNDQ
G9	IO10RSB0
G10	IO19RSB0
G11	IO26RSB0
G12	IO30RSB0
G13	IO40RSB0
G14	IO45RSB0
G15	GNDQ
G16	IO50RSB0
G17	GBB2/IO61PPB1
G18	IO53RSB0
G19	IO63NDB1
G20	NC
G21	NC
G22	NC
H1	NC
H2	NC
H3	VCC
H4	IO166PDB3
H5	IO167NPB3
H6	IO172NDB3
H7	IO169NDB3
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO25RSB0
H12	IO31RSB0

TABLE 4-27: FG484 PIN DETAILS

FG484	
Pin Number	**AGL600 Function**
H13	VCCIB0
H14	VCCIB0
H15	VMV1
H16	GBC2/IO62PDB1
H17	IO67PPB1
H18	IO64PPB1
H19	IO66PDB1
H20	VCC
H21	NC
H22	NC
J1	NC
J2	NC
J3	NC
J4	IO166NDB3
J5	IO168NPB3
J6	IO167PPB3
J7	IO169PDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO62NDB1
J17	IO64NPB1
J18	IO65PPB1
J19	IO66NDB1
J20	NC
J21	IO68PDB1
J22	IO68NDB1
K1	IO157PDB3
K2	IO157NDB3
K3	NC
K4	IO165NDB3
K5	IO165PDB3
K6	IO168PPB3
K7	GFC1/IO164PPB3
K8	VCCIB3
K9	VCC
K10	GND

TABLE 4-27: FG484 PIN DETAILS

FG484	
Pin Number	**AGL600 Function**
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO69PPB1
K17	IO65NPB1
K18	IO75PDB1
K19	IO75NDB1
K20	NC
K21	IO76NDB1
K22	IO76PDB1
L1	NC
L2	IO155PDB3
L3	NC
L4	GFB0/IO163NPB3
L5	GFA0/IO162NDB3
L6	GFB1/IO163PPB3
L7	VCOMPLF
L8	GFC0/IO164NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO69NPB1
L16	GCB1/IO70PPB1
L17	GCA0/IO71NPB1
L18	IO67NPB1
L19	GCB0/IO70NPB1
L20	IO77PDB1
L21	IO77NDB1
L22	IO78NPB1
M1	NC
M2	IO155NDB3
M3	IO158NPB3
M4	GFA2/IO161PPB3
M5	GFA1/IO162PDB3
M6	VCCPLF
M7	IO160NDB3
M8	GFB2/IO160PDB3

TABLE 4-27: FG484 PIN DETAILS

FG484	
Pin Number	**AGL600 Function**
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO73PPB1
M16	GCA1/IO71PPB1
M17	GCC2/IO74PPB1
M18	IO80PPB1
M19	GCA2/IO72PDB1
M20	IO79PPB1
M21	IO78PPB1
M22	NC
N1	IO154NDB3
N2	IO154PDB3
N3	NC
N4	GFC2/IO159PDB3
N5	IO161NPB3
N6	IO156PPB3
N7	IO129RSB2
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO73NPB1
N17	IO80NPB1
N18	IO74NPB1
N19	IO72NDB1
N20	NC
N21	IO79NPB1
N22	NC
P1	NC
P2	IO153PDB3
P3	IO153NDB3
P4	IO159NDB3
P5	IO156NPB3
P6	IO151PPB3

TABLE 4-27: FG484 PIN DETAILS

FG484	
Pin Number	**AGL600 Function**
P7	IO158PPB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO87NPB1
P17	IO85NDB1
P18	IO85PDB1
P19	IO84PDB1
P20	NC
P21	IO81PDB1
P22	NC
R1	NC
R2	NC
R3	VCC
R4	IO150PDB3
R5	IO151NPB3
R6	IO147NPB3
R7	GEC0/IO146NPB3
R8	VMV3
R9	VCCIB2
R10	VCCIB2
R11	IO117RSB2
R12	IO110RSB2
R13	VCCIB2
R14	VCCIB2
R15	VMV2
R16	IO94RSB2
R17	GDB1/IO87PPB1
R18	GDC1/IO86PDB1
R19	IO84NDB1
R20	VCC
R21	IO81NDB1
R22	IO82PDB1
T1	IO152PDB3
T2	IO152NDB3
T3	NC
T4	IO150NDB3

TABLE 4-27: FG484 PIN DETAILS

FG484	
Pin Number	**AGL600 Function**
T5	IO147PPB3
T6	GEC1/IO146PPB3
T7	IO140RSB2
T8	GNDQ
T9	GEA2/IO143RSB2
T10	IO126RSB2
T11	IO120RSB2
T12	IO108RSB2
T13	IO103RSB2
T14	IO99RSB2
T15	GNDQ
T16	IO92RSB2
T17	VJTAG
T18	GDC0/IO86NDB1
T19	GDA1/IO88PDB1
T20	NC
T21	IO83PDB1
T22	IO82NDB1
U1	IO149PDB3
U2	IO149NDB3
U3	NC
U4	GEB1/IO145PDB3
U5	GEB0/IO145NDB3
U6	VMV2
U7	IO138RSB2
U8	IO136RSB2
U9	IO131RSB2
U10	IO124RSB2
U11	IO119RSB2
U12	IO107RSB2
U13	IO104RSB2
U14	IO97RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO88NDB1
U20	NC
U21	IO83NDB1
U22	NC
V1	NC
V2	NC

TABLE 4-27: FG484 PIN DETAILS

FG484	
Pin Number	**AGL600 Function**
V3	GND
V4	GEA1/IO144PDB3
V5	GEA0/IO144NDB3
V6	IO139RSB2
V7	GEC2/IO141RSB2
V8	IO132RSB2
V9	IO127RSB2
V10	IO121RSB2
V11	IO114RSB2
V12	IO109RSB2
V13	IO105RSB2
V14	IO98RSB2
V15	IO96RSB2
V16	GDB2/IO90RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	NC
W1	NC
W2	IO148PDB3
W3	NC
W4	GND
W5	IO137RSB2
W6	FF/GEB2/ IO142RSB2
W7	IO134RSB2
W8	IO125RSB2
W9	IO123RSB2
W10	IO118RSB2
W11	IO115RSB2
W12	IO111RSB2
W13	IO106RSB2
W14	IO102RSB2
W15	GDC2/IO91RSB2
W16	IO93RSB2
W17	GDA2/IO89RSB2
W18	TMS
W19	GND
W20	NC
W21	NC

TABLE 4-27: FG484 PIN DETAILS

FG484	
Pin Number	**AGL600 Function**
W22	NC
Y1	VCCIB3
Y2	IO148NDB3
Y3	NC
Y4	NC
Y5	GND
Y6	NC
Y7	NC
Y8	VCC
Y9	VCC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1

TABLE 4-28: FG484 PIN DETAILS

FG484	
Pin Number	**AGL1000 Function**
A1	GND
A2	GND
A3	VCCIB0
A4	IO07RSB0
A5	IO09RSB0
A6	IO13RSB0
A7	IO18RSB0
A8	IO20RSB0
A9	IO26RSB0
A10	IO32RSB0
A11	IO40RSB0
A12	IO41RSB0
A13	IO53RSB0
A14	IO59RSB0
A15	IO64RSB0
A16	IO65RSB0
A17	IO67RSB0
A18	IO69RSB0
A19	NC
A20	VCCIB0
A21	GND
A22	GND
AA1	GND
AA2	VCCIB3
AA3	NC
AA4	IO181RSB2
AA5	IO178RSB2
AA6	IO175RSB2
AA7	IO169RSB2
AA8	IO166RSB2
AA9	IO160RSB2
AA10	IO152RSB2
AA11	IO146RSB2
AA12	IO139RSB2
AA13	IO133RSB2
AA14	NC
AA15	NC
AA16	IO122RSB2
AA17	IO119RSB2
AA18	IO117RSB2
AA19	NC
AA20	NC

TABLE 4-28: FG484 PIN DETAILS

FG484	
Pin Number	**AGL1000 Function**
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	IO180RSB2
AB5	IO176RSB2
AB6	IO173RSB2
AB7	IO167RSB2
AB8	IO162RSB2
AB9	IO156RSB2
AB10	IO150RSB2
AB11	IO145RSB2
AB12	IO144RSB2
AB13	IO132RSB2
AB14	IO127RSB2
AB15	IO126RSB2
AB16	IO123RSB2
AB17	IO121RSB2
AB18	IO118RSB2
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	IO06RSB0
B5	IO08RSB0
B6	IO12RSB0
B7	IO15RSB0
B8	IO19RSB0
B9	IO24RSB0
B10	IO31RSB0
B11	IO39RSB0
B12	IO48RSB0
B13	IO54RSB0
B14	IO58RSB0
B15	IO63RSB0
B16	IO66RSB0
B17	IO68RSB0
B18	IO70RSB0

TABLE 4-28: FG484 PIN DETAILS

FG484	
Pin Number	**AGL1000 Function**
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	IO220PDB3
C3	NC
C4	NC
C5	GND
C6	IO10RSB0
C7	IO14RSB0
C8	VCC
C9	VCC
C10	IO30RSB0
C11	IO37RSB0
C12	IO43RSB0
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC
C21	NC
C22	VCCIB1
D1	IO219PDB3
D2	IO220NDB3
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO16RSB0
D9	IO22RSB0
D10	IO28RSB0
D11	IO35RSB0
D12	IO45RSB0
D13	IO50RSB0
D14	IO55RSB0
D15	IO61RSB0
D16	GBB1/IO75RSB0

TABLE 4-28: FG484 PIN DETAILS

FG484	
Pin Number	**AGL1000 Function**
D17	GBA0/IO76RSB0
D18	GBA1/IO77RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	IO219NDB3
E2	NC
E3	GND
E4	GAB2/IO224PDB3
E5	GAA2/IO225PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO17RSB0
E9	IO21RSB0
E10	IO27RSB0
E11	IO34RSB0
E12	IO44RSB0
E13	IO51RSB0
E14	IO57RSB0
E15	GBC1/IO73RSB0
E16	GBB0/IO74RSB0
E17	IO71RSB0
E18	GBA2/IO78PDB1
E19	IO81PDB1
E20	GND
E21	NC
E22	IO84PDB1
F1	NC
F2	IO215PDB3
F3	IO215NDB3
F4	IO224NDB3
F5	IO225NDB3
F6	VMV3
F7	IO11RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO25RSB0
F11	IO36RSB0
F12	IO42RSB0
F13	IO49RSB0
F14	IO56RSB0

TABLE 4-28: FG484 PIN DETAILS

FG484	
Pin Number	**AGL1000 Function**
F15	GBC0/IO72RSB0
F16	IO62RSB0
F17	VMV0
F18	IO78NDB1
F19	IO81NDB1
F20	IO82PPB1
F21	NC
F22	IO84NDB1
G1	IO214NDB3
G2	IO214PDB3
G3	NC
G4	IO222NDB3
G5	IO222PDB3
G6	GAC2/IO223PDB3
G7	IO223NDB3
G8	GNDQ
G9	IO23RSB0
G10	IO29RSB0
G11	IO33RSB0
G12	IO46RSB0
G13	IO52RSB0
G14	IO60RSB0
G15	GNDQ
G16	IO80NDB1
G17	GBB2/IO79PDB1
G18	IO79NDB1
G19	IO82NPB1
G20	IO85PDB1
G21	IO85NDB1
G22	NC
H1	NC
H2	NC
H3	VCC
H4	IO217PDB3
H5	IO218PDB3
H6	IO221NDB3
H7	IO221PDB3
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO38RSB0
H12	IO47RSB0

TABLE 4-28: FG484 PIN DETAILS

FG484	
Pin Number	**AGL1000 Function**
H13	VCCIB0
H14	VCCIB0
H15	VMV1
H16	GBC2/IO80PDB1
H17	IO83PPB1
H18	IO86PPB1
H19	IO87PDB1
H20	VCC
H21	NC
H22	NC
J1	IO212NDB3
J2	IO212PDB3
J3	NC
J4	IO217NDB3
J5	IO218NDB3
J6	IO216PDB3
J7	IO216NDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO83NPB1
J17	IO86NPB1
J18	IO90PPB1
J19	IO87NDB1
J20	NC
J21	IO89PDB1
J22	IO89NDB1
K1	IO211PDB3
K2	IO211NDB3
K3	NC
K4	IO210PPB3
K5	IO213NDB3
K6	IO213PDB3
K7	GFC1/IO209PPB3
K8	VCCIB3
K9	VCC
K10	GND

TABLE 4-28: FG484 PIN DETAILS

FG484	
Pin Number	**AGL1000 Function**
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO91PPB1
K17	IO90NPB1
K18	IO88PDB1
K19	IO88NDB1
K20	IO94NPB1
K21	IO98NDB1
K22	IO98PDB1
L1	NC
L2	IO200PDB3
L3	IO210NPB3
L4	GFB0/IO208NPB3
L5	GFA0/IO207NDB3
L6	GFB1/IO208PPB3
L7	VCOMPLF
L8	GFC0/IO209NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO91NPB1
L16	GCB1/IO92PPB1
L17	GCA0/IO93NPB1
L18	IO96NPB1
L19	GCB0/IO92NPB1
L20	IO97PDB1
L21	IO97NDB1
L22	IO99NPB1
M1	NC
M2	IO200NDB3
M3	IO206NDB3
M4	GFA2/IO206PDB3
M5	GFA1/IO207PDB3
M6	VCCPLF
M7	IO205NDB3
M8	GFB2/IO205PDB3

TABLE 4-28: FG484 PIN DETAILS

FG484	
Pin Number	**AGL1000 Function**
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO95PPB1
M16	GCA1/IO93PPB1
M17	GCC2/IO96PPB1
M18	IO100PPB1
M19	GCA2/IO94PPB1
M20	IO101PPB1
M21	IO99PPB1
M22	NC
N1	IO201NDB3
N2	IO201PDB3
N3	NC
N4	GFC2/IO204PDB3
N5	IO204NDB3
N6	IO203NDB3
N7	IO203PDB3
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO95NPB1
N17	IO100NPB1
N18	IO102NDB1
N19	IO102PDB1
N20	NC
N21	IO101NPB1
N22	IO103PDB1
P1	NC
P2	IO199PDB3
P3	IO199NDB3
P4	IO202NDB3
P5	IO202PDB3
P6	IO196PPB3

TABLE 4-28: FG484 PIN DETAILS

FG484	
Pin Number	**AGL1000 Function**
P7	IO193PPB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO112NPB1
P17	IO106NDB1
P18	IO106PDB1
P19	IO107PDB1
P20	NC
P21	IO104PDB1
P22	IO103NDB1
R1	NC
R2	IO197PPB3
R3	VCC
R4	IO197NPB3
R5	IO196NPB3
R6	IO193NPB3
R7	GEC0/IO190NPB3
R8	VMV3
R9	VCCIB2
R10	VCCIB2
R11	IO147RSB2
R12	IO136RSB2
R13	VCCIB2
R14	VCCIB2
R15	VMV2
R16	IO110NDB1
R17	GDB1/IO112PPB1
R18	GDC1/IO111PDB1
R19	IO107NDB1
R20	VCC
R21	IO104NDB1
R22	IO105PDB1
T1	IO198PDB3
T2	IO198NDB3
T3	NC
T4	IO194PPB3

TABLE 4-28: FG484 PIN DETAILS

FG484	
Pin Number	**AGL1000 Function**
T5	IO192PPB3
T6	GEC1/IO190PPB3
T7	IO192NPB3
T8	GNDQ
T9	GEA2/IO187RSB2
T10	IO161RSB2
T11	IO155RSB2
T12	IO141RSB2
T13	IO129RSB2
T14	IO124RSB2
T15	GNDQ
T16	IO110PDB1
T17	VJTAG
T18	GDC0/IO111NDB1
T19	GDA1/IO113PDB1
T20	NC
T21	IO108PDB1
T22	IO105NDB1
U1	IO195PDB3
U2	IO195NDB3
U3	IO194NPB3
U4	GEB1/IO189PDB3
U5	GEB0/IO189NDB3
U6	VMV2
U7	IO179RSB2
U8	IO171RSB2
U9	IO165RSB2
U10	IO159RSB2
U11	IO151RSB2
U12	IO137RSB2
U13	IO134RSB2
U14	IO128RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO113NDB1
U20	NC
U21	IO108NDB1
U22	IO109PDB1
V1	NC
V2	NC

TABLE 4-28: FG484 PIN DETAILS

FG484	
Pin Number	**AGL1000 Function**
V3	GND
V4	GEA1/IO188PDB3
V5	GEA0/IO188NDB3
V6	IO184RSB2
V7	GEC2/IO185RSB2
V8	IO168RSB2
V9	IO163RSB2
V10	IO157RSB2
V11	IO149RSB2
V12	IO143RSB2
V13	IO138RSB2
V14	IO131RSB2
V15	IO125RSB2
V16	GDB2/IO115RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO109NDB1
W1	NC
W2	IO191PDB3
W3	NC
W4	GND
W5	IO183RSB2
W6	FF/GEB2/ IO186RSB2
W7	IO172RSB2
W8	IO170RSB2
W9	IO164RSB2
W10	IO158RSB2
W11	IO153RSB2
W12	IO142RSB2
W13	IO135RSB2
W14	IO130RSB2
W15	GDC2/IO116RSB2
W16	IO120RSB2
W17	GDA2/IO114RSB2
W18	TMS
W19	GND
W20	NC
W21	NC

TABLE 4-28: FG484 PIN DETAILS

FG484	
Pin Number	**AGL1000 Function**
W22	NC
Y1	VCCIB3
Y2	IO191NDB3
Y3	NC
Y4	IO182RSB2
Y5	GND
Y6	IO177RSB2
Y7	IO174RSB2
Y8	VCC
Y9	VCC
Y10	IO154RSB2
Y11	IO148RSB2
Y12	IO140RSB2
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1

APPENDIX A: REVISION HISTORY

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the latest publication.

A.1 Revision A - 12/2022

The following is a summary of changes in revision A of the document:

- The document was migrated to Microchip template.
- The document number was updated from DS0095 to DS60001805A.
- Updated Table 1
- Updated Table 2

A.2 Revision 27 - 03/2016

The following is the summary of changes in the revision 27 of the document:

- Added the deleted package FG144 from AGL125 device in Table 1 (SAR 79355)

A.3 Revision 26 - 05/2019

The following is the summary of changes in the revision 26 of the document:

- Updated Table 1 and Temperature Grade Offerings notes by:
- Replacing Commercial (0°C to +70°C Ambient Temperature) with Commercial (0°C to +85°C Junction Temperature) (SAR 48352).
- Replacing Industrial (–40°C to +85°C Ambient Temperature) with Industrial (–40°C to +100°C Junction Temperature) (SAR 48352).
- Ambient temperature row removed in Table 2-2 (SAR 48352).
- Updated Table 2-2 note 2 from "To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microchip recommends that the user follow best design practices using Microchip's timing and power simulation tools." to "Software Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microchip recommends using custom settings for temperature range before running timing and power analysis tools. For more information on custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help." (SAR 77087).
- Updated Table 2-2 note 9 from "VMV pins must be connected to the corresponding VCCI pins. See the "Pin Descriptions" chapter of the IGLOO FPGA Fabric User Guide for further information." to "VMV and VCCI must be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" on page 3-1 for further information." (SAR 77087)
- Added 2 mA drive strengths in tables same as 4 mA (SAR 57179).
- Added reference of Package Mechanical Drawings document in all package pin assignment notes (76777).

A.4 Revision 25 - 06/2015

The following is the summary of changes in the revision 25 of the document:

- Removed package FG144 from AGL060 device in the following tables: Table 1, I/Os Per Package1 and Temperature Grade Offerings (SAR 68517)
- Removed Package Pin Assignment table of AGL060 device from FG144.(SAR 68517)

A.5 Revision 24 - 03/2014

The following is the summary of changes in the revision 24 of the document:

- Note added for the discontinuance of QN132 package to the following tables: Table 1, I/Os Per Package1, Table 3, and Temperature Grade Offerings and Section 4.8, QN132 (SAR 55117, PDN 1306).
- Removed packages CS81 and QN132 from AGL250 device in the following tables: Table 1, I/Os Per Package1, and Temperature Grade Offerings (SAR 49472).

A.6 Revision 23 - 12/2012

The following is the summary of changes in the revision 23 of the document:

- The IGLOO Ordering Information has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43173).
- The note in Table 2-189 and Table 2-190 referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42564).
  Additionally, note regarding SSOs was added.
- Live at Power-Up (LAPU) has been replaced with 'Instant On'

A.7 Revision 22 - 09/2012

The following is the summary of changes in the revision 22 of the document:

- The "Security" section was modified to clarify that Microchip does not support read-back of programmed data.
- Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40271).

A.8 Revision 21 - 05/2012

The following is the summary of changes in the revision 21 of the document:

- Under AGL125, in the Package Pin list, CS121 was incorrectly added to the datasheet in revision 19 and has been removed (SAR 38217).
- Corrected the inadvertent error for Max Values for LVPECL VIH and revised the same to '3.6' in Table 2-151 (SAR 37685).
- Figure 2-38, and Figure 2-39, have been added (SAR 34841).
- The following sentence was removed from the VMVx description in the Section 3.0, Pin Descriptions: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38317). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement
- Pin description table for AGL125 CS121 was removed as it was incorrectly added to the datasheet in revision 19 (SAR 38217)

A.9 Revision 20 - 03/2012

The following is the summary of changes in the revision 20 of the document:

- Notes indicating that AGL015 is not recommended for new designs have been added. The Devices Not Recommended For New Designs is new (SAR 35015)
- Notes indicating that device/package support is TBD for AGL250-QN132 and AGL060-FG144 have been reinserted (SAR 33689)
- Values for the power data for PAC1, PAC2, PAC3, PAC4, PAC7, and PAC8 were revised in Table 2-19 and Table 2-21 to match the SmartPower tool in Libero software version 9.0 SP1 and Power Calculator spreadsheet v7a released on 08/10/2010 (SAR 33768).
- The reference to guidelines for global spines and VersaTile rows, given in the Section 2.3.1.4, Global Clock Contribution—PCLOCK, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *IGLOO FPGA Fabric User Guide* (SAR 34730).
- Figure 2-4, has been modified for the DIN waveform; the Rise and Fall time label has been changed to t_{DIN} (SAR 37104)
- Added missing characteristics for 3.3V LVCMOS, 3.3V LVCMOS Wide range, 1.2V LVCMOS, and 1.2V LVCMOS Wide range to the following tables:
- Table 2-38, Table 2-39, Table 2-40, Table 2-42, Table 2-43, and Table 2-44 (SARs 33854 and 36891)
- Table 2-63, Table 2-64, and Table 2-65 (SAR 33854)
- Table 2-127, Table 2-128, Table 2-129, Table 2-137, Table 2-138, and Table 2-139 (SAR 36891)
- AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match Table 2-50 (SAR 34878)
- Added values for minimum pulse width and removed the FRMAX row from Table 2-173 through Table 2-188 in the

Section 2.10.2, Global Tree Timing Characteristics. Use the software to determine the FRMAX for the device you are using (SAR 29271).

A.10 Revision 19 - 09/2011

The following is the summary of changes in the revision 19 of the document:

- CS121 was added to the product tables in the Introduction for AGL125 (SAR 22737). CS81 was added for AGL250 (SAR 22737).
- Notes indicating that device/package support is TBD for AGL250-QN132 and AGL060-FG144 have been removed (SAR 33689)
- M1AGL400 was removed from the Table 2 table. This device was discontinued in April 2009 (SAR 32450)
- Dimensions for the QN48 package were added to Table 3 (SAR 30537)
- The Y security option and Licensed DPA Logo were added to the IGLOO Ordering Information section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 32151).
- The In-System Programming (ISP) and Security section were revised to clarify that although no existing security measures can give an absolute guarantee, Microchip FPGAs implement the best security available in the industry (SAR 32865
- The following sentence was removed from the Section 1.2.8, Advanced Architecture:

  "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3V) programming of IGLOO devices via an IEEE 1532 JTAG interface" (SAR 28756).
- The Section 1.4, Specifying I/O States During Programming is new (SAR 21281)
- Values for VCCPLL at 1.2V –1.5V DC core supply voltage were revised in Table 2-2 (SAR 22356)
- The value for VPUMP operation was changed from "0 to 3.45V" to "0 to 3.6V" (SAR 25220)
- The value for VCCPLL 1.5V DC core supply voltage was changed from "1.4V to 1.6V" to "1.425V to 1.575V" (SAR 26551)
- The notes in the table were renumbered in order of their appearance in the table (SAR 21869)
- The temperature used in EQ 2 was revised from 110°C to 100°C for consistency with the limits given in Table 2-2. The resulting maximum power allowed is thus 1.28W. Formerly it was 1.71 W (SAR 26259).
- Values for CS196, CS281, and QN132 packages were added to Table 2-5 (SARs 26228, 32301)
- Table 2-6 and Table 2-7 were updated to remove the column for –20°C and shift the data over to correct columns (SAR 23041)
- The tables in the Section 2.2.1, Quiescent Supply Current were updated with revised notes on IDD (SAR 24112). Table 2-8 is new
- The formulas in the table notes for Table 2-41 were corrected (SAR 21348)
- The row for 110°C was removed from Table 2-45. The example in the associated paragraph was changed from 110°C to 100°C. Table 2-46 was revised to change 110° to 100°C. (SAR 26259).
- The notes regarding drive strength in the Section 2.4.4, Summary of I/O Timing Characteristics – Default I/O Software Settings, Table 2-63 and Table 2-138 were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is ±100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 25700).
- The following sentence was deleted from the Section 2.6.3, 2.5V LVCMOS (SAR 24916):

  “It uses a 5V–tolerant input buffer and push-pull output buffer.”
- The values for $F_{DDRIMAX}$ and F_{DDOMAX} were updated in the tables in the Section 2.8.1, Input DDR Module and Section 2.8.2, Output DDR Module (SAR 23919).
- The following notes were removed from Table 2-147 (SAR 29428):

  ±5%

  Differential input voltage = ±350 mV
- Table 2-189 and Table 2-190 were updated. A note was added to both tables indicating that when the CCC/PLL core is generated by Mircosemi core generator software, not all delay values of the specified delay increments are available (SAR 25705).
- The following figures were deleted (SAR 29991). Reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in

detail (SAR 21770).
  - Figure 2-36 • Write Access after Write onto Same Address
  - Figure 2-37 • Read Access after Write onto Same Address
  - Figure 2-38 • Write Access after Read onto Same Address
- The port names in the SRAM Figure 2-32, , SRAM Table 2-191 tables, Figure 2-40, , and the FIFO Table 2-195 were revised to ensure consistency with the software names (SARs 29991, 30510).
- The Section 3.0, Pin Descriptions chapter has been added (SAR 21642).
- Package names used in the Section 4.0, Package Pin Assignments were revised to match standards given in *Package Mechanical Drawings* (SAR 27395)
- The Section 4.2, CS81 pin table for AGL250 is new (SAR 22737)
- The CS121 pin table for AGL125 is new (SAR 22737)
- The P3 function was revised in the Table 4-5 for AGL250 (SAR 24800)
- The Table 4-15 for AGL250 was added
- The pin table for AGL060 was added in Section 4.10, FG144 (SAR 33689)

A.11 Revision 18 - 12/2009

The following is the summary of change in the revision 18 of the document:

- The version changed to v2.0 for IGLOO datasheet chapters, indicating the datasheet contains information based on final characterization. Please review the datasheet carefully as most tables were updated with new data.

A.12 Revision 17 - 09/2009

The following is the summary of changes in the revision 17 of the document:

- The Reprogrammable Flash Technology was modified to add "250 MHz (1.5V systems) and 160 MHz (1.2V systems) System Performance"
- IGLOO Ordering Information was revised to note that halogen-free packages are available with RoHS-compliant packaging
- Added Table 1-1
- The definitions of hot-swap and cold-sparing were added to the Section 1.2.14, I/Os with Advanced I/O Standards

A.13 Revision 16 - 04/2009

The following is the summary of changes in the revision 16 of the document:

- M1AGL400 is no longer offered and was removed from the Table 1 product table, IGLOO Ordering Information, and Temperature Grade Offerings
- The –F speed grade is no longer offered for IGLOO devices. The speed grade column and note regarding –F speed grade were removed from IGLOO Ordering Information. The "Speed Grade and Temperature Grade Matrix" section was removed.
- This datasheet now has fully characterized data and has moved from being Advance to a Production version. The version number changed from Advance v0.5 to v2.0.
- Please review the datasheet carefully as most tables were updated with new data
- 3.3V LVCMOS and 1.2V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3V LVCMOS and 1.2V LVCMOS data.
- I_{IL} and I_{IH} input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables.
- –F was removed from the datasheet. The speed grade is no longer supported.
- The notes in Table 2-2 were updated.
- Table 2-4 was updated
- Table 2-5 was updated
- Table 2-6 and Table 2-7 were updated
- In Table 2-191 and Table 2-193, the following specifications were removed:
  - t_{WRO}
  - t_{CCKH}

- In Table 2-192 and Table 2-194, the following specifications were removed:
  - t_{WRO}
  - t_{CCKH}

A.14 Revision 15 - 02/2009

The following is the summary of change in the revision 15 of the document:

- Added Table 4-13 pin table for the AGL060 device

A.15 Revision 14 - 02/2009

The following is the summary of changes in the revision 14 of the document:

- The Advanced I/O section was revised to include two bullets regarding wide range power supply voltage support
- 3.0V wide range was added to the list of supported voltages in the "I/Os with Advanced I/O Standards" section. The Section 1.3, Wide Range I/O Support is new

A.16 Revision 13 - 01/2009

The following is the summary of change in the revision 13 of the document:

- The Table 4-3 pin table was revised to add a note regarding pins F1 and G1

A.17 Revision 12 - 12/2008

The following is the summary of changes in the revision 12 of the document:

- QN48 and QN68 were added to the AGL030 for the following tables:
  - Table 1 Product Family Table
  - IGLOO Ordering Information
  - Temperature Grade Offerings
- QN132 is fully supported by AGL125 so footnote 3 was removed
- The Table 4-9 pin diagram and pin table are new
- The Table 4-10 pin table for AGL030 is new
- The AGL600 Function for pin K15 in the Table 4-27 was changed to VCCIB1.

A.18 Revision 11 - 10/2008

This document was updated to include AGL400 device information. The following is the summary of changes in the revision 11 of the document:

- Updated Table 1 Product Family Table
- Updated IGLOO Ordering Information
- Updated Temperature Grade Offerings
- Updated Figure 1-2,
- The tables in the Section 2.2.1, Quiescent Supply Current were updated with values for AGL400. In addition, the title was updated to include:
  (VCC = VJTAG = VPP = 0V).
- The tables in the Section 2.2.3, Power Consumption of Various Internal Resources were updated with values for AGL400.
- Added Table 2-178 is new.
- Updated the Table 4-6 table for the AGL400 device is new
- Updated the Table 4-21 table for the AGL400 device is new
- Updated the Table 4-23 table for the AGL400 device is new
- Updated the Table 4-26 table for the AGL400 device is new

A.19 Revision 10 - 08/2008

The following is the summary of changes in the revision 10 of the document:

- 3.0 V LVCMOS wide range support data was added to Table 2-2
- 3.3V LVCMOS wide range support data was added to Table 2-25 to Table 2-27
- 3.3V LVCMOS wide range support data was added to Table 2-28
- 3.3V LVCMOS wide range support text was added to Table 2-49
- Table 2-49 is new

A.20 Revision 9 - 07/2008

The following is the summary of change in the revision 9 of the document:

- As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2V/1.5V to 1.2V to 1.5V.

A.21 Revision 8 - 06/2008

The following is the summary of changes in the revision 8 of the document:

- As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2V/1.5V to 1.2V to 1.5V.
- Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2V I/O set.
- DDR Tables have two additional data points added to reflect both edges for Input DDR setup and hold time.
- The power data table has been updated to match SmartPower data rather then simulation values.
- AGL015 global clock delays have been added.
- Table 2-1 was updated to combine the VCCI and VMV parameters in one row. The word "output" from the parameter description for VCCI and VMV, and table note 3 was added.
- Table 2-2 was updated to add references to tables notes 4, 6, 7, and 8. VMV was added to the VCCI parameter row, and table note 9 was added.
- In Table 2-3, the maximum operating junction temperature was changed from 110° to 100°
- VMV was removed from Table 2-4. The table title was modified to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was revised to remove "refers only to overshoot/undershoot limits for simultaneous switching I/Os."
- The Section 2.1.2.1, PLL Behavior at Brownout Condition is new
- Figure 2-2, is new
- EQ 2 was updated. The temperature was changed to 100°C, and therefore the end result changed.
- The table notes for Table 2-9, Table 2-10, and Table 2-11 were updated to remove VMV and include PDC6 and PDC7. VCCI and VJTAG were removed from the statement about IDD in the table note for Table 2-11.
- Note 2 of Table 2-12 was updated to include VCCPLL. Note 4 was updated to include PDC6 and PDC7.
- Table 2-13, Table 2-14, Table 2-15, and Table 2-16 were updated to change PDC2 to PDC6 and PDC3 to PDC7. The table notes were updated to reflect that power was measured on VCCI.
- In Table 2-19, the description for PAC13 was changed from Static to Dynamic
- Table 2-20 and Table 2-11 were updated to add PDC6 and PDC7, and to change the definition for PDC5 to bank quiescent power. Subtitles were added to indicate type of devices and core supply voltage.
- The Section 2.3.1.2, Total Static Power Consumption—PSTAT was updated to revise the calculation of P_{STAT}, including PDC6 and PDC7
- Footnote † was updated to include information about PAC13. The PLL Contribution equation was changed from: $P_{PLL} = P_{AC13} + P_{AC14} * F_{CLKOUT}$ to $P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$.

A.22 Revision 7 - 06/2008

The following is the summary of change in the revision 7 of the document:

- The Section 4.8, QN132 package diagram was updated to include D1 to D4. In addition, note 1 was changed from top view to bottom view, and note 2 is new.

A.23 Revision 6 - 06/2008

The following is the summary of changes in the revision 6 of the document:

- This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.
- Pin numbers were added to the Section 4.7, QN68 package diagram. Note 2 was added below the diagram.

A.24 Revision 5 - 03/2008

The following is the summary of change in the revision 5 of the document:

- The Section 4.4, CS196 package and pin table was added for AGL250.

A.25 Revision 4 - 03/2008

This document was updated to include AGL015 device information. QN68 is a new package offered in the AGL015. The following is the summary of changes in the revision 4 of the document:

- The Low Power section was updated to change "1.2V and 1.5V Core Voltage" to "1.2V and 1.5V Core and I/O Voltage." The text "(from 12 µW)" was removed from "Low Power Active FPGA Operation."
- 1.2V was added to the list of core and I/O voltages in the Advanced I/O and Advanced I/O sections.
- The Embedded Memory section was updated to remove the footnote reference from the section heading and place it instead after "4,608-Bit" and "True Dual-Port SRAM (except ×18)."

A.26 Revision 3 - 02/2008

This document was updated to include AGL015 device information. QN68 is a new package offered in the AGL015. The following is the summary of changes in the revision 3 of the document:

- Updated the Features section
- Updated the IGLOO Ordering Information section
- Updated the Temperature Grade Offerings section
- Updated the Table 1 Product Family Table
- Updated the Table 3
- Updated the AGL015 and AGL030 note
- The Table 4 table was updated to include M1AGL600
- In the IGLOO Ordering Information table, the QN package measurements were updated to include both 0.4 mm and 0.5 mm.
- In the Introduction, the number of I/Os was updated from 288 to 300
- The Section 4.7, QN68 section is new

A.27 Revision 2 - 01/2008

The following is the summary of changes in the revision 1 of the document:

- The Table 4-4 package and pin table was added for AGL125.

A.28 Revision 1 - 01/2008

The following is the summary of changes in the revision 1 of the document:

- The Low Power section was updated to change the description of low power active FPGA operation to "from 12 µW" from "from 25 µW." The same update was made in the Introduction section and the Section 1.1, Flash*Freeze Technology.

A.29 Revision 0 - 01/2008

The following is the summary of change in the revision 0.5 of the document:

- This document was previously in datasheet Advance v0.7. As a result of moving to the handbook format, Actel has restarted the numbering.

A.30 Revision 0.7 - 12/2007

The following is the summary of changes in the revision 0.5 of the document:

- Table 1 • IGLOO Product Family, the "I/Os Per Package1" table, and the Temperature Grade Offerings table were updated to reflect the following: CS196 is now supported for AGL250; device/package support for QN132 is to be determined for AGL250; the CS281 package was added for AGL600 and AGL1000
- Table 2 • IGLOO FPGAs Package Sizes Dimensions is new, and package sizes were removed from the "I/Os Per Package1" table
- The "I/Os Per Package1"table was updated to reflect 77 instead of 79 single-ended I/Os for the VG100 package for AGL030
- The "Timing Model" was updated to be consistent with the revised timing numbers
- In Table 2-27 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings, TJ was changed to TA in notes 1 and 2
- All AC Loading figures for single-ended I/O standards were changed from Datapaths at 35 pF to 5 pF
- The "1.2V LVCMOS (JESD8-12A)" section is new
- This document was previously in datasheet Advance v0.7. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is Advance v0.1
- Table 2-4 • IGLOO CCC/PLL Specification and Table 2-5 • IGLOO CCC/PLL Specification were updated
- The former Table 2-16 • Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in IGLOO Devices (maximum drive strength and high slew selected) was removed
- The "During Flash*Freeze Mode" section was updated to include information about the output of the I/O to the FPGA core
- Table 2-31 • Flash*Freeze Pin Location in IGLOO Family Packages (device-independent) was updated to add UC81 and CS281. Flash*Freeze pins were assigned for CS81, CS121, and CS196
- Figure 2-40 • Flash*Freeze Mode Type 2 – Timing Diagram was updated to modify the LSICC Signal
- Information regarding calculation of the quiescent supply current was added to the "Quiescent Supply Current" section
- Table 3-8 • Quiescent Supply Current (IDD) Characteristics, IGLOO Flash*Freeze Mode† was updated
- Table 3-9 • Quiescent Supply Current (IDD) Characteristics, IGLOO Sleep Mode (VCC = 0V)† was updated
- Table 3-11 • Quiescent Supply Current (IDD), No IGLOO Flash*Freeze Mode1 was updated
- Table 3-115 • Minimum and Maximum DC Input and Output Levels was updated.
- Table 3-156 • JTAG 1532 was updated and Table 3-155 • JTAG 1532 is new
- The "121-Pin CSP" and "281-Pin CSP" packages are new
- The "81-Pin CSP" table for the AGL030 device was updated to change the G6 pin function to IO44RSB1 and the JG pin function to IO45RSB1.
- The "121-Pin CSP" table for the AGL060 device is new
- The "256-Pin FBGA" table for the AGL1000 device is new
- The "281-Pin CSP" table for the AGL 600 device is new
- The "100-Pin VQFP" table for the AGL060 device is new
- The "144-Pin FBGA" table for the AGL250 device is new
- The "144-Pin FBGA" table for the AGL1000 device is new
- The "484-Pin FBGA" table for the AGL600 device is new
- The "484-Pin FBGA" table for the AGL1000 device is new

A.31 Revision 0.6 - 11/2007

The following is the summary of changes in the revision 0.5 of the document:

- Table 1 • IGLOO Product Family, the "I/Os Per Package1" table, and the "IGLOO Ordering Information", and the Temperature Grade Offerings table were updated to add the UC81 package
- The "81-Pin µCSP" table for the AGL030 device is new
- The "81-Pin CSP" table for the AGL030 device is new

A.32 Revision 0.5 - 09/2007

The following is the summary of change in the revision 0.5 of the document:

- Table 1 • IGLOO Product Family was updated for AGL030 in the Package Pins section to change CS181 to CS81

A.33 Revision 0.4 - 09/2007

The following is the summary of changes in the revision 0.4 of the document:

- Cortex-M1 device information was added to Table 1 • IGLOO Product Family, the "I/Os Per Package1" table, "IGLOO Ordering Information", and Temperature Grade Offerings
- The number of single-ended I/Os for the CS81 package for AGL030 was updated to 66 in the "I/Os Per Package1" table
- The "Power Conservation Techniques" section was updated to recommend that unused I/O signals be left floating

A.34 Revision 0.3 - 08/2007

The following is the summary of changes in the revision 0.3 of the document:

- In Table 1 • IGLOO Product Family, the CS81 package was added for AGL030. The CS196 was replaced by the CS121 for AGL060. Table note 3 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.
- The CS81 and CS121 packages were added to the "I/Os Per Package1" table. The number of single-ended I/Os was removed for the CS196 package in AGL060. Table note 6 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.
- The CS81 and CS121 packages were added to the Temperature Grade Offerings table. The temperature grade offerings were removed for the CS196 package in AGL060. Table note 3 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.
- The CS81 and CS121 packages were added to Table 2-31 • Flash*Freeze Pin Location in IGLOO Family Packages (device-independent)

A.35 Revision 0.2

The following is the summary of changes in the revision 0.2 of the document:

- The words "ambient temperature" were added to the temperature range in the "IGLOO Ordering Information", Temperature Grade Offerings, and "Speed Grade and Temperature Grade Matrix" sections
- The TJ parameter in Table 3-2 • Recommended Operating Conditions was changed to TA, ambient temperature, and table notes 4–6 were added

THE MICROCHIP WEBSITE

Microchip provides online support via our WWW site at www.microchip.com. This website is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the website contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip website at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the website at: www.microchip.com/support

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

ISBN: 978-1-6683-1706-8

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820