SY89832U

2.5V Ultra-Precision 1:4 LVDS Fanout Buffer/ Translator with Internal Termination

Features

- Guaranteed AC Performance over Temperature and Voltage:
  - DC-to >2.0 GHz Throughput
  - <570 ps Propagation Delay (IN-to-Q)
  - <20 ps Within-Device Skew
  - <200 ps Rise/Fall Time
- Ultra-Low Jitter Design:
- 81 fs_{RMS} Phase Jitter
- Unique, Patented Input Termination and V_T Pin Accepts DC- and AC-Coupled Inputs
- High-Speed LVDS Outputs
- 2.5V Voltage Supply Operation
- Industrial Temperature Range: –40°C to +85°C
- Available in a 16-Lead 3 mm x 3 mm QFN Package

Applications

- Processor Clock Distribution
- SONET Clock Distribution
- Fibre Channel Clock Distribution
- Gigabit Ethernet Clock Distribution

General Description

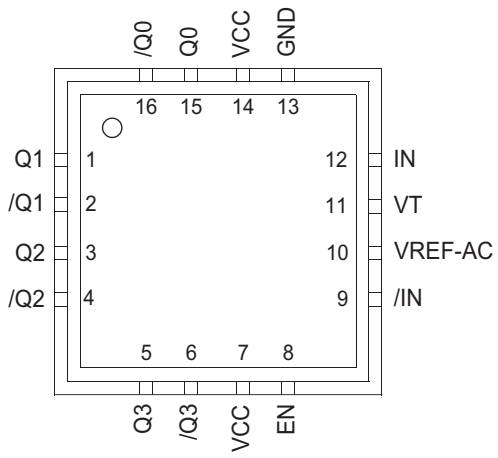
The SY89832U is a 2.5V, high-speed, 2 GHz differential, low voltage differential swing (LVDS) 1:4 fanout buffer optimized for ultra-low skew applications. Within device skew is guaranteed to be less than 20 ps over supply voltage and temperature.

The differential input buffer has a unique internal termination design that allows access to the termination network through a V_T pin. This feature allows the device to easily interface to different logic standards. A VREF–AC reference output is included for AC-coupled applications.

The SY89832U is a part of the high-speed clock synchronization family. For 3.3V applications, see SY89833L or SY89833AL.

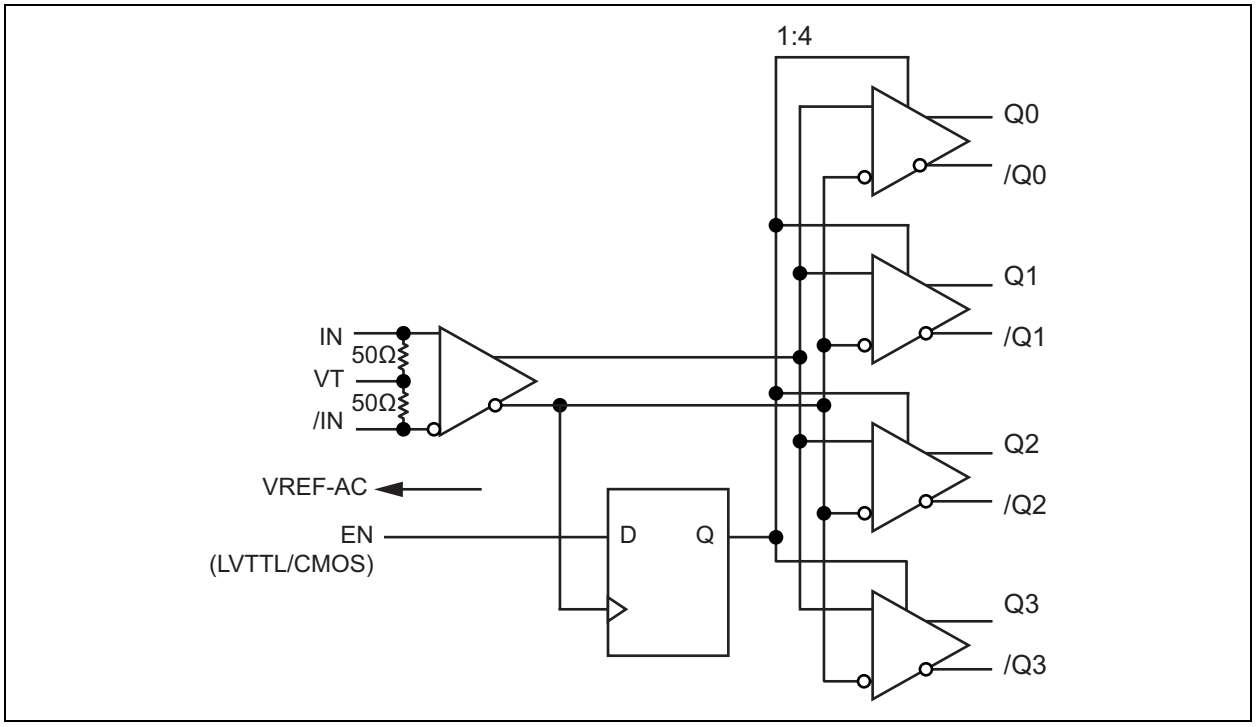
Package Type

SY89832U
16-Pin 3x3 QFN
(Top View)



United States Patent No. RE44,134

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} + 0.3V
LVDS Output Current (I_{OUT}) ..... ±10 mA
Input Current (Source or Sink Current on IN, /IN) (I_{IN}) ..... ±50 mA
Termination Current (Source or Sink Current on VT) (I_{VT}) ..... ±100 mA
V_{REF-AC} Current (Source or Sink Current on VREF-AC) ($I_{VREF-AC}$) (Note 1) ..... ±1.5 mA

Operating Ratings ††

Supply Voltage Range (V_{CC}) ..... +2.375V to +2.675V

† Notice: Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†† Notice: The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 1: Due to the limited drive capability, the VREF-AC reference should only be used for the input of the same package device (i.e., do not use for other devices).

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 2.5V ±5%; T_A = –40°C to +85°C, unless otherwise stated, (Note 1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Current	I_{CC}	—	75	100	mA	No load
Input Resistance (IN-to-VT)	R_{IN}	45	50	55	Ω	—
Differential Input Resistance (IN-to-/IN)	R_{DIFF_IN}	90	100	110	Ω	—
Input High Voltage (IN, /IN)	V_{IH}	0.1	—	V_{CC} + 0.3	V	—
Input Low Voltage (IN, /IN)	V_{IL}	–0.3	—	V_{IH} – 0.1	V	—
Input Voltage Swing	V_{IN}	0.1	—	V_{CC}	V	Note 2
Differential Input Voltage Swing	V_{DIFF_IN}	0.2	—	—	V	Note 2
Input Current (IN, /IN)	$\|I_{IN}\|$	—	—	45	mA	Note 3
Output Reference Voltage	V_{REF-AC}	V_{CC} – 1.525	V_{CC} – 1.425	V_{CC} – 1.325	V	—

Note 1: Devices are designed to meet the DC specifications shown in the above table after thermal equilibration has been established.

2: See Figure 5-1 and Figure 5-2 for V_{IN} and V_{DIFF_IN} definitions.

3: Due to the internal termination the input current depends on the applied voltages at IN, /IN, and VT inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit!

LVDS OUTPUTS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 2.5V ±5%; T_A = –40˚C to +85˚C, R_L = 100Ω across Q and /Q, unless otherwise stated. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Voltage Swing	V_{OUT}	250	325	—	mV	Note 2
Differential Voltage Output Swing	V_{DIFF_OUT}	500	650	—	mV	Note 2
Output Common Mode Voltage	V_{OCM}	1.125	—	1.275	V	Note 3
Change in Output Common Mode Voltage	ΔV_{OCM}	–50	—	50	mV	Note 3

Note 1: Devices are designed to meet the DC specifications shown in the above table after thermal equilibration has been established.

2: See Figure 5-1 and Figure 5-2 for V_{OUT} and V_{DIFF_OUT} definitions.

3: See Figure 8-2.

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 2.5V ±5%; T_A = –40˚C to +85˚C, unless otherwise stated. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V	—
Input Low Voltage	V_{IL}	0	—	0.8	V	—
Input High Current	I_{IH}	–125	—	30	µA	—
Input Low Current	I_{IL}	–300	—	—	µA	—

Note 1: Devices are designed to meet the DC specifications shown in the above table after thermal equilibration has been established.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 2.5V ±5%; T_A = –40°C to +85°C, R_L = 100Ω across Q and /Q, unless otherwise stated. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Frequency	f_{MAX}	2.0	2.5	—	GHz	V_{OUT} ≥ 200 mV
Propagation Delay In-to-Q	t_{PD}	370	470	570	ps	V_{IN} < 400 mV
		300	410	500		V_{IN} ≥ 400 mV
Within-Device Skew	t_{SKEW}	—	5	20	ps	Note 2
Part-to-Part Skew		—	—	200		Note 3
Set-Up Time EN to IN, /IN	t_S	0	—	—	ps	Note 4
Hold Time IN, /IN to EN	t_H	320	—	—	ps	Note 4
Additive Phase Jitter	t_{JITTER}	—	81	—	fs_{RMS}	622 MHz @ 2.5V, Integration range: 12 kHz to 20 MHz
		—	195	—		250 MHz @ 2.5V, Integration range: 12 kHz to 20 MHz
Output Rise/Fall Time Q (20% to 80%)	t_r/t_f	70	150	200	ps	At full output swing

Note 1: High-frequency AC parameters are guaranteed by design and characterization.

2: Within-device skew is measured between two different outputs under identical input transitions.

3: Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.

4: Set-up and Hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, Set-up and Hold times do not apply.

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	–40	—	+85	°C	—
Lead Temperature	T_J	—	+260	—	°C	Soldering, 20 sec.
Storage Temperature Range	T_A	–65	—	+150	°C	
Package Thermal Resistance (Note 1)						
Thermal Resistance, QFN-16Ld	θ_{JA}	—	60	—	°C/W	Junction-to-Ambient, Still-Air
	Ψ_{JB}	—	32	—	°C/W	Junction-to-Board

Note 1: Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential; on the PCB. θ_{JA} and Ψ_{JB} values are determined for a 4-layer board in still-air number, unless otherwise stated.

2.0 TYPICAL OPERATING CHARACTERISTICS

Note: V_{CC} = 2.5V, GND = 0V, V_{IN} = 400 mV, R_L = 100Ω across the outputs; T_A = 25°C, unless otherwise stated.

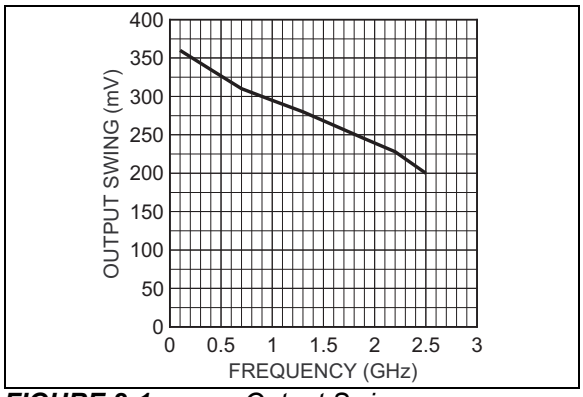


FIGURE 2-1: *Output Swing vs. Frequency.*

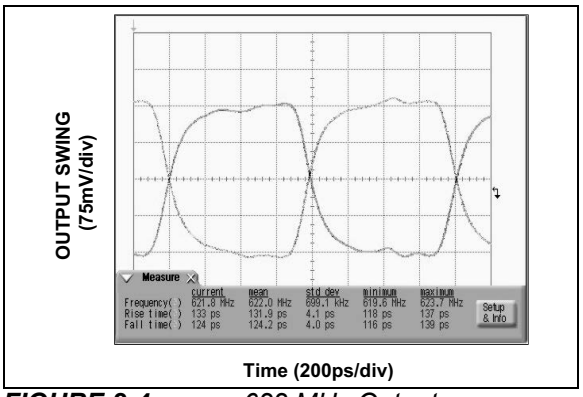


FIGURE 2-4: *622 MHz Output.*

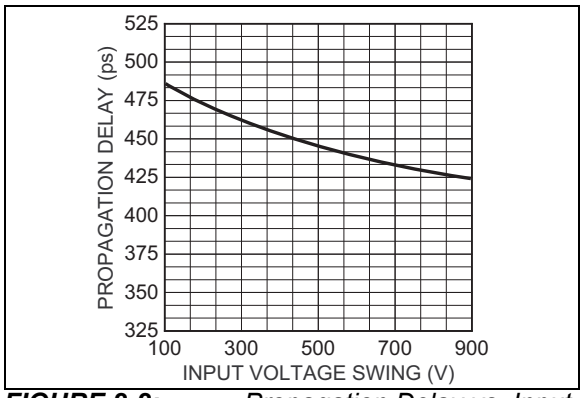


FIGURE 2-2: *Propagation Delay vs. Input Voltage Swing.*

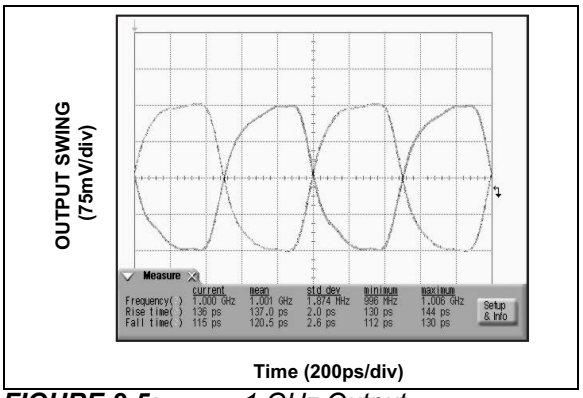


FIGURE 2-5: *1 GHz Output.*

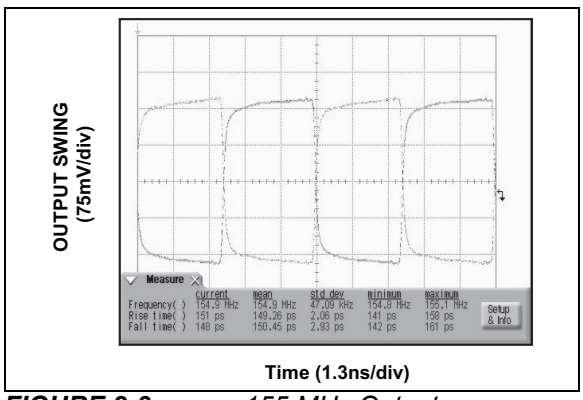


FIGURE 2-3: *155 MHz Output.*

V_{CC} = 2.5V, GND = 0, T_A = +25°C.

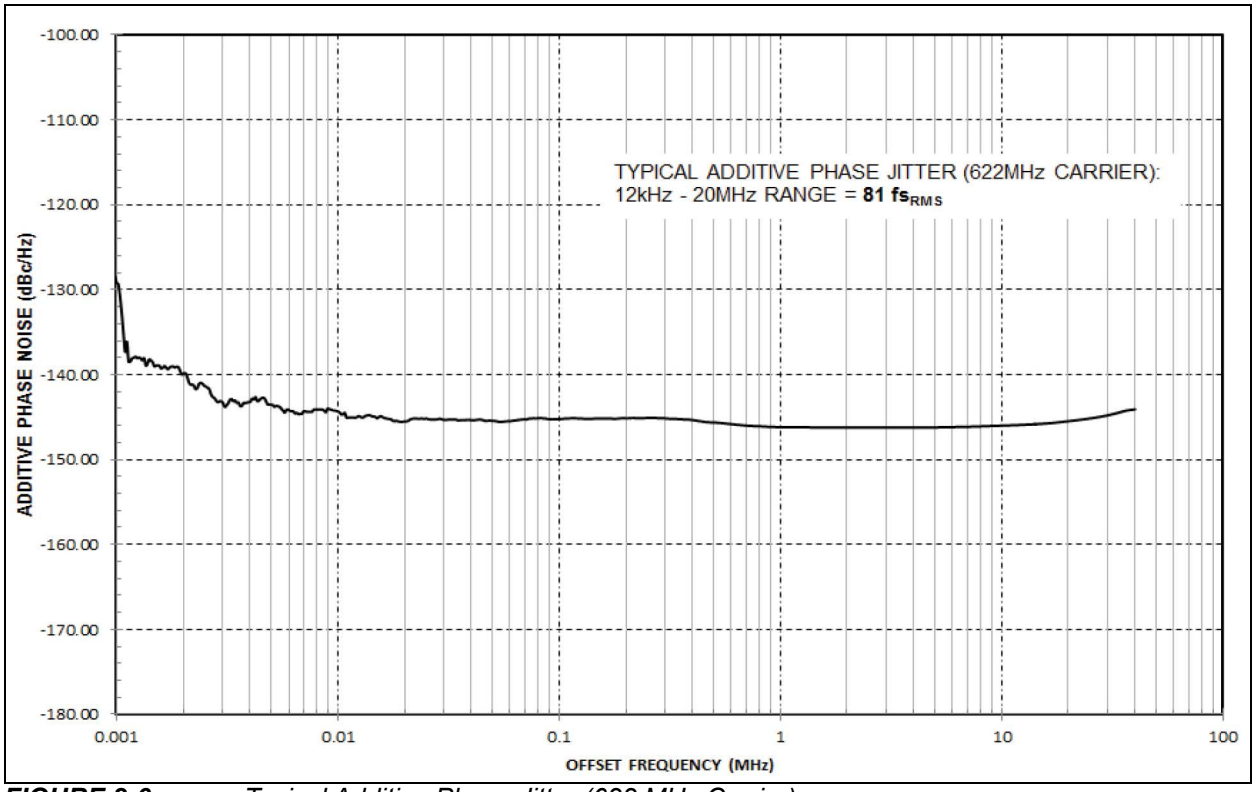


FIGURE 2-6: *Typical Additive Phase Jitter (622 MHz Carrier).*

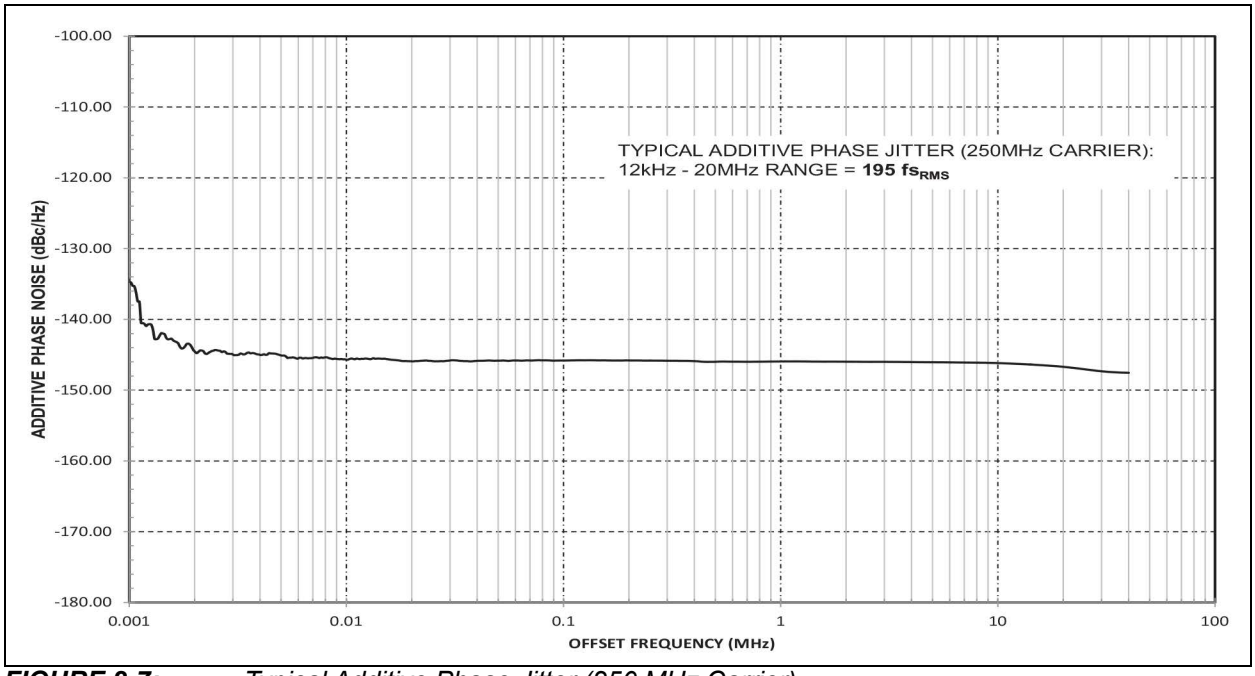


FIGURE 2-7: *Typical Additive Phase Jitter (250 MHz Carrier).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Function
15, 16 1, 2 3, 4 5, 6	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	LVDS Differential (Outputs): Normally terminated with 100Ω across the pair (Q, /Q). See LVDS Outputs section for more details.Unused outputs should be terminated with a 100Ω resistor across each pair.
8	EN	The single-ended, TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the Q outputs are in a logic LOW state. Note that this input is internally connected to a 25 kΩ pull-up resistor and will default to logic HIGH state (enabled) if left open.
9, 12	/IN, IN	Differential Input: This input is the differential signal input to the device. Input accepts AC- or DC-Coupled differential signs as small as 100 mV. Each pin internally terminates to the V_T pin through 50Ω. Note that this input will default to an intermediate state if left open. See Input Interface Applications section for more details.
10	VREF-AC	Reference Voltage: This output biases to approximately V_{CC} – 1.4V. It is used when AC coupling the input (IN, /IN). For AC-Coupled applications, connect VREF-AC to VT pin and bypass with a 0.01 µF low-ESR capacitor to VCC. See Input Interface Applications section for more details. Maximum sink/source current is ±1.5 mA. Due to the limited drive capability, the VREF-AC pin is only intended to drive the VT pin.
11	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to the VT pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See Input Interface Applications section for more details.
13	GND	Ground. GND pin and exposed pad must be connected to the most negative potential of the device ground.
7, 14	VCC	Positive Power Supply: Bypass with 0.1 µF//0.01 µF low ESR capacitors and place as close to each VCC pin as possible.

TABLE 3-2: TRUTH TABLE

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0	1

4.0 TIMING DIAGRAMS

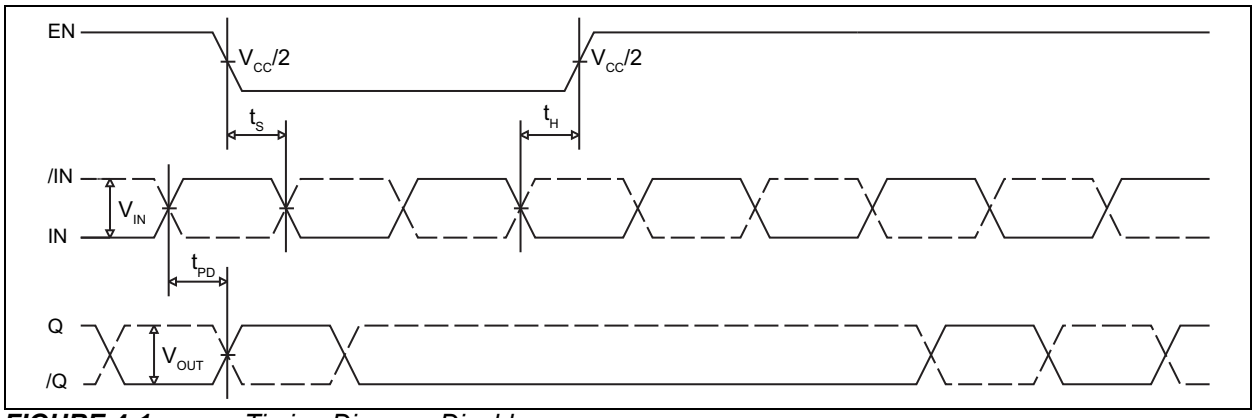


FIGURE 4-1: *Timing Diagram Disable.*

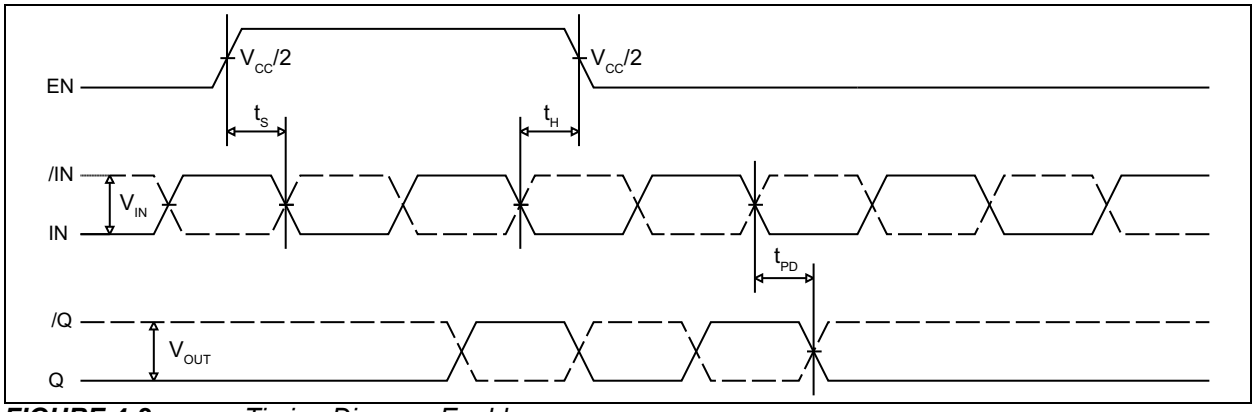


FIGURE 4-2: *Timing Diagram Enable.*

5.0 SINGLE-ENDED AND DIFFERENTIAL SWINGS

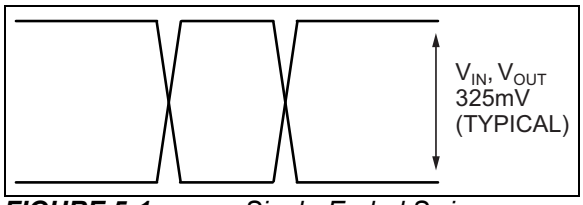


FIGURE 5-1: *Single-Ended Swing.*

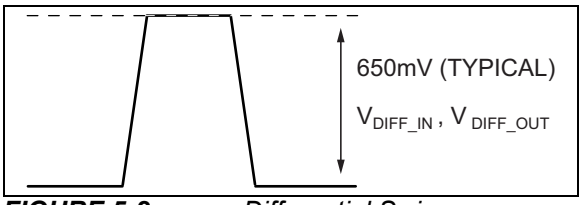


FIGURE 5-2: *Differential Swing.*

6.0 INPUT STAGE

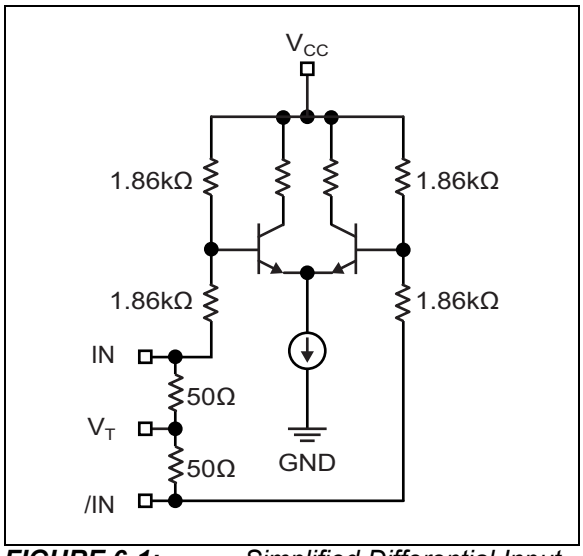


FIGURE 6-1: *Simplified Differential Input Buffer.*

7.0 INPUT INTERFACE APPLICATIONS

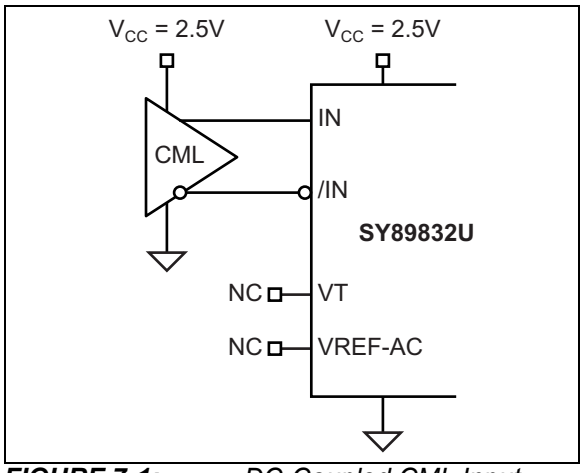


FIGURE 7-1: *DC-Coupled CML Input Interface.*

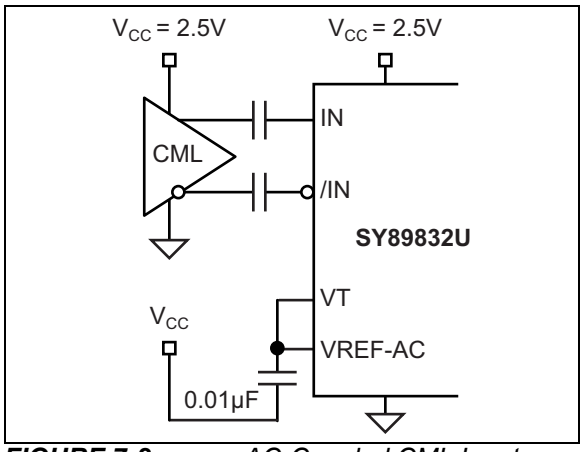


FIGURE 7-2: *AC-Coupled CML Input Interface.*

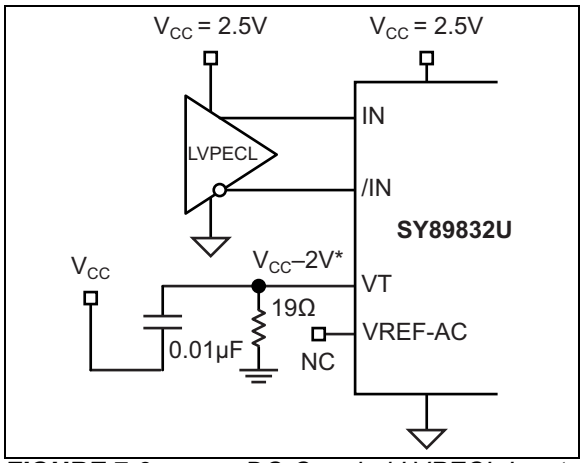


FIGURE 7-3: *DC-Coupled LVPECL Input Interface (*Bypass with 0.01 µF to GND).*

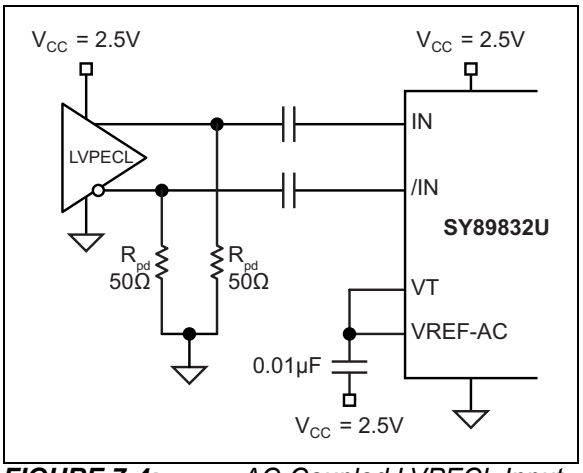


FIGURE 7-4: *AC-Coupled LVPECL Input Interface.*

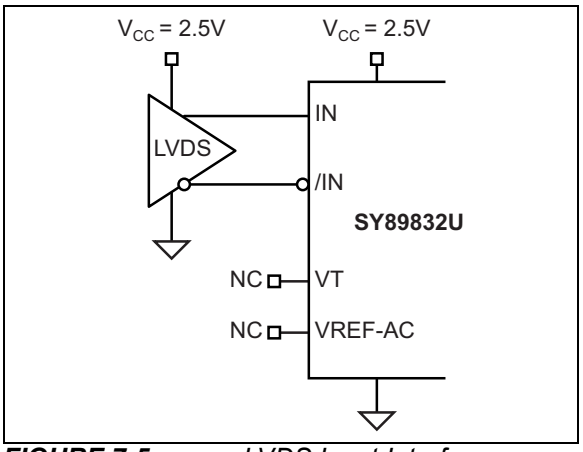


FIGURE 7-5: *LVDS Input Interface.*

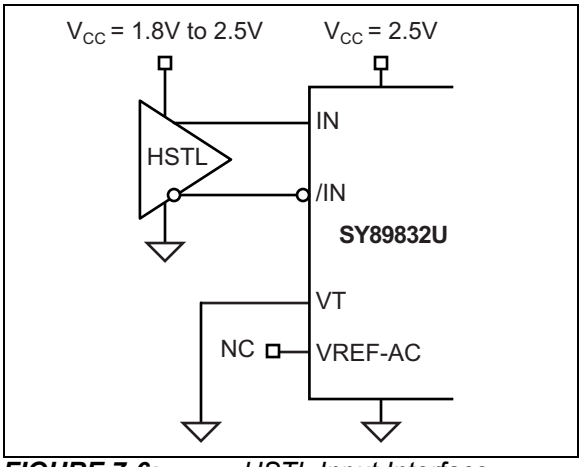


FIGURE 7-6: *HSTL Input Interface.*

8.0 LVDS OUTPUTS

LVDS specifies a small swing of 325 mV typical, on a nominal 1.2V common-mode above ground.

The common-mode voltage has tight limits to permit large variations in ground noise between an LVDS driver and receiver.

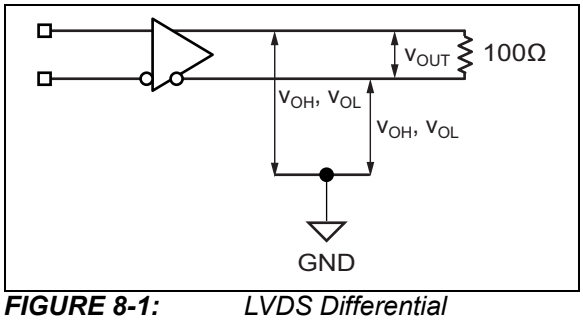


FIGURE 8-1: *LVDS Differential Measurement.*

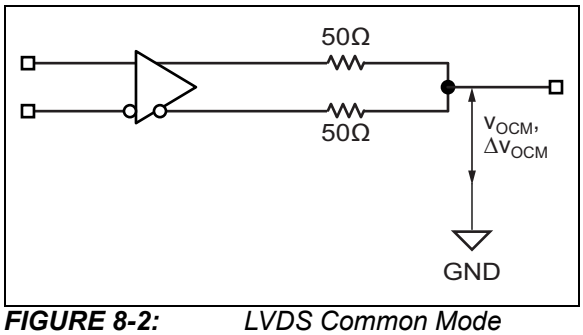
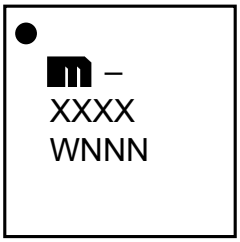


FIGURE 8-2: *LVDS Common Mode Measurement.*

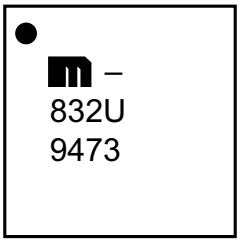
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

16-Lead QFN*



Example

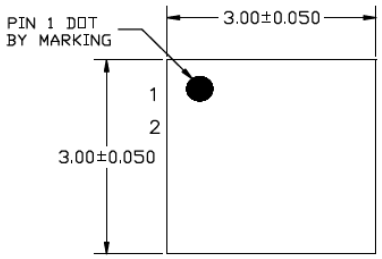


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

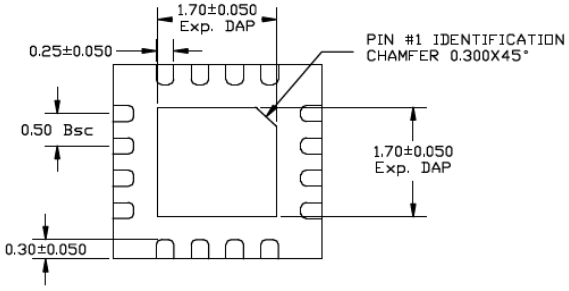
TITLE

16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

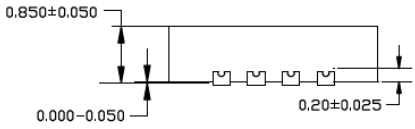
DRAWING #	QFN33-16LD-PL-3	UNIT	MM
Lead Frame	NiPdAu	Lead Finish	NiPdAu



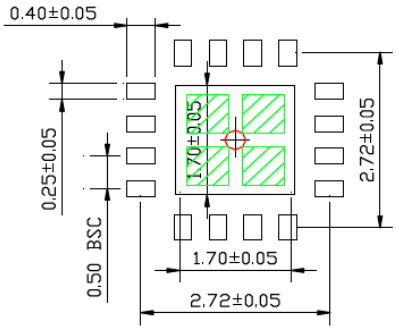
TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE: 4, 5

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60mm IN SIZE, 0.20mm SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (March 2022)

- Converted Micrel document SY89832U to Microchip data sheet template DS20006659A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Voltage Option	Package	Temperature Range	Special Processing

Device:	SY89832:		2.5V Ultra-Precision 1:4 LVDS Fanout Buffer/ Translator with Internal Termination
Voltage Option:	U	=	2.5V
Package:	M	=	16-Lead Industrial QFN
Temperature Range:	G	=	–40°C to 85°C (NiPdAu Lead Free)
Special Processing:	<blank>=		100/Tube
	TR	=	1,000/Reel

Examples:

a) SY89832UMG: 2.5V Ultra-Precision 1:4 LVDS Fanout Buffer/ Translator with Internal Termination, 2.5V, 16-Lead Industrial QFN, –40°C to 85°C (NiPdAu Lead Free), 100/Tube

b) SY89832UMG-TR: 2.5V Ultra-Precision 1:4 LVDS Fanout Buffer/ Translator with Internal Termination, 2.5V, 16-Lead Industrial QFN, –40°C to 85°C (NiPdAu Lead Free), 1,000/Reel

NOTES:

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
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