Switchtec™ PSX Gen 4 Programmable PCIe® Switch Family

PM41100, PM41084, PM41068, PM41052, PM41036, PM41028

Summary

The Switchtec PSX Gen 4 Programmable PCIe Switch Family comprises programmable and high-reliability switches that support up to 100 lanes, 52 ports, 26 virtual switch partitions, 48 Non-Transparent Bridges (NTBs), hot- and surprise-plug controllers for each port, advanced error containment, comprehensive diagnostics and debug capabilities, a wide breadth of I/O interfaces and an integrated MIPS processor.

Typical applications for the PSX family include PCIe SSD enclosures, Flash arrays, multi-host architectures, high-density servers, blade servers, pooled storage/compute and applications that require customized, high-reliability PCIe switching.

Features

High-Performance Non-Blocking Gen 4 Switches

- 100-lane, 84-lane, 68-lane, 52-lane, 36-lane and 28-lane variants
- Ports bifurcate to x1[1]/x2/x4/x8/x16 lanes
- Up to 48 NTBs assignable to any port
- Logical Non-Transparent (NT) interconnect allows for larger topologies (up to 256 masters)
- Supports 1+1 and N+1 failover mechanisms
- NT address translation using direct windows and multiple sub-windows per BAR
- Supports multicast groups per port

DMA Controller

- High-performance, ultra-low latency cut-through DMA engine
- Up to 64 DMA channels

Error Containment

- Advanced Error Reporting (AER) on all ports
- Downstream Port Containment (DPC) on all downstream ports
- Completion Timeout Synthesis (CTS) to prevent an error state in an upstream host due to incomplete non-posted transactions
- Upstream Error Containment (UEC), a programmable feature that prevents errors from propagating upstream
- Hot- and surprise-plug controllers per port
- GPIOs configurable for different cable/connector standards

Diagnostics and Debug

- Transaction Layer Packet (TLP) generator for testing and debugging of links and error handling
- Real-time eye capture
- External loopback capability
- Errors, statistics, performance and TLP latency counters

PCIe Interfaces

- Passive, managed and optical cables
- SFF-8644, SFF-8643, SFF-8639, OCuLink and other connectors
- SHPC-enabled slot and edge connectors

[1] x1 natively on four lanes

Highlights

- High-reliability PCIe: robust error containment, hot- and surprise-plug controllers per port, end-to-end data integrity protection, ECC protection on RAMs, high-quality, low-power SERDES
- PSX Software Development Kit (SDK): enables customer-differentiated solutions in areas such as error containment and surprise-plug
- Integrated enclosure management processor, I/O interfaces, and SDK for enclosure management firmware development
- Comprehensive diagnostics and debugging: PCIe generator and analyzer, per-port performance and error counters, multiple loopback modes and real-time eye capture
- Significant power, cost and board space savings with support for:
  - Up to 52 ports, 48 NTBs, and 26 virtual switch partitions
  - Flexible x1[1], x2, x4, x8, and x16 port bifurcation with no restrictions on configuring ports as either upstream or downstream, or on mapping ports to NTBs
- NVMe-MI enclosure management:
  - Integrated NVMe controller
  - In-band management supporting SES and native NVMe enclosure management stack
  - Out-of-band management supporting MCTP through I^2C
- Secure system solution with boot image authentication

Peripheral I/O Interfaces

- Up to 11 Two-Wire Interfaces (TWIs) with SMBus support
- Up to 4 SFF-8485-compliant SGPIO ports
- Up to 103 GPIO pins
- 10/100 Ethernet MAC port (MII/RMII) (PSX 100x/84x/68xG4)
- 16-bit parallel local bus interface with ECC protection
- Up to 4 UARTs
- JTAG and EJTAG interface

High-Speed I/O

- PCIe Gen 4 16 GT/s
- Supports PCIe-compliant link training and manual PHY configuration
- Manual PHY configuration for optical

Power Management

- Active State Power Management (ASPM)
- Software-controlled power management

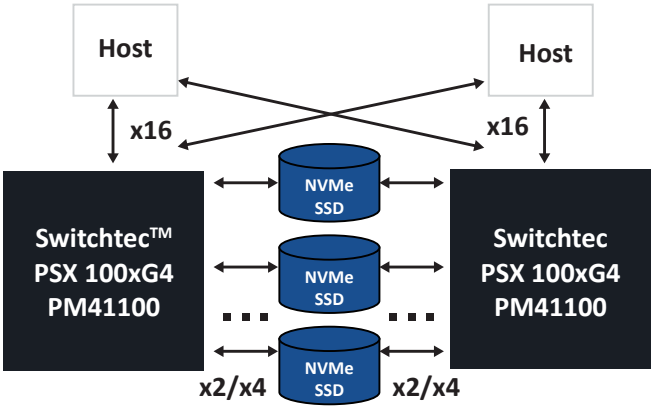
ChipLink Diagnostic Tools

- Extensive debug, diagnostics, configuration and analysis tools with an intuitive GUI
- Access to configuration data, management capabilities and signal integrity analysis tools (such as real-time eye capture)
- Connects to device over in-band PCIe or sideband signals (UART, TWI and EJTAG)

Evaluation Kit

The PM42100-KIT Switchtec Gen 4 PCIe Switch Evaluation Kit is a device evaluation environment that supports multiple interfaces.

Example Application



Ordering Information

Product	Part Numbers	Lanes	Ports/ NTBs	Partitions	Hot-plug Controllers	Package
PSX 100xG4 Gen 4 Programmable PCIe® Switch	PM41100B1-FEI	100	52/48	26	52	40 mm × 40 mm
PSX 84xG4 Gen 4 Programmable PCIe Switch	PM41084B1-FEI	84	44/42	22	44	40 mm × 40 mm
PSX 68xG4 Gen 4 Programmable PCIe Switch	PM41068B1-FEI	68	36/34	18	36	40 mm × 40 mm
PSX 52xG4 Gen 4 Programmable PCIe Switch	PM41052B1-F3EI	52	28/26	14	28	29 mm × 29 mm
PSX 36xG4 Gen 4 Programmable PCIe Switch	PM41036B1-F3EI	36	20/18	10	20	29 mm × 29 mm
PSX 28xG4 Gen 4 Programmable PCIe Switch	PM41028B1-F3EI	28	16/14	8	16	29 mm × 29 mm
PSX 52xG4 Gen 4 Programmable PCIe Switch, Automotive Qualified	PM44052B1-FEIP	52	28/26	14	28	29 mm x 29 mm
PSX 36xG4 Gen 4 Programmable PCIe Switch, Automotive Qualified	PM44036B1-FEIP	36	20/18	10	20	29 mm x 29 mm
PSX 28xG4 Gen 4 Programmable PCIe Switch, Automotive Qualified	PM44028B1-FEIP	28	16/14	8	16	29 mm x 29 mm

[1] x1 natively on four lanes