

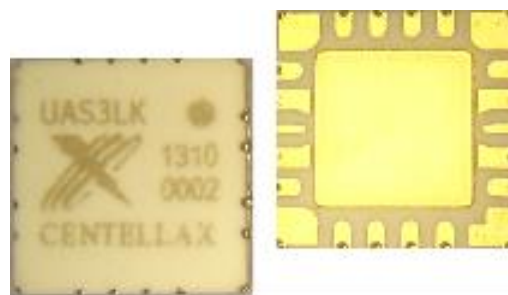
32Gb/s Broadband 3V Driver Amplifier

Features

- 3V Output
- 20 dB gain (adjustable)
- Hermetic* SMT Package
7X7x1.8mm
- Minimal external passives**
- ECCN 5A991b

Application

The UAS3LK is intended for test and measurement applications using simple NRZ or complex modulation schemes. As a general purpose gain block with flat, broadband gain, the UAS3LK is also ideal for commercial microwave radio and military electronic warfare systems.



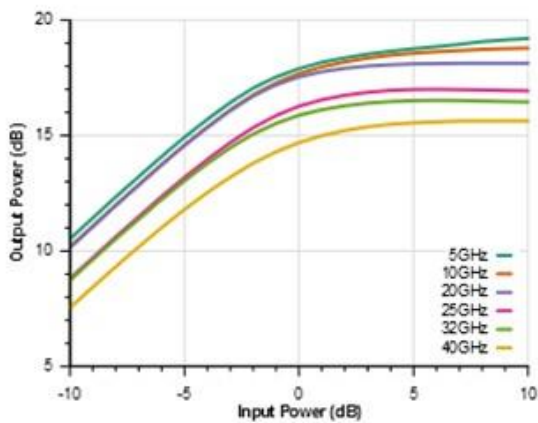
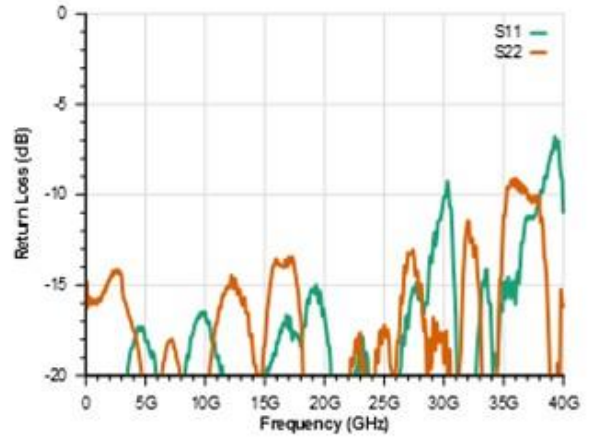
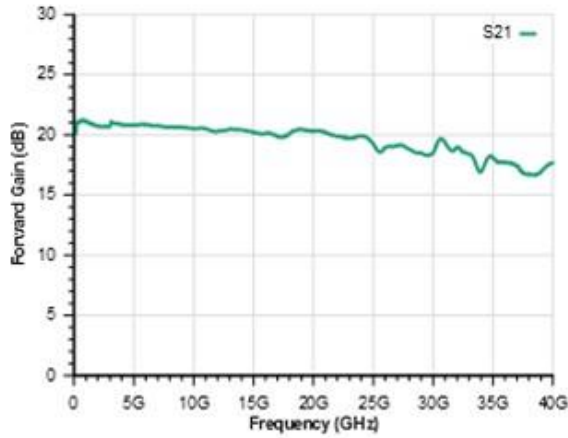
Description

The UAS3LK is a small, single channel, two stage, high-performance broadband 32 Gb/s amplifier with low jitter, 3V amplitude and 20dB gain. Integrated bias-Ts decouple high frequency signals down to 10MHz; external inductors can be used to extend operation to lower frequencies. The amplifier stages are fabricated in a production 0.15um GaAs pHEMT process. The UAS3LK features adjustable gain and is housed in a hermetically sealed, ceramic package designed for surface mount application to printed circuit boards. The UAS3LK is RoHS compliant.

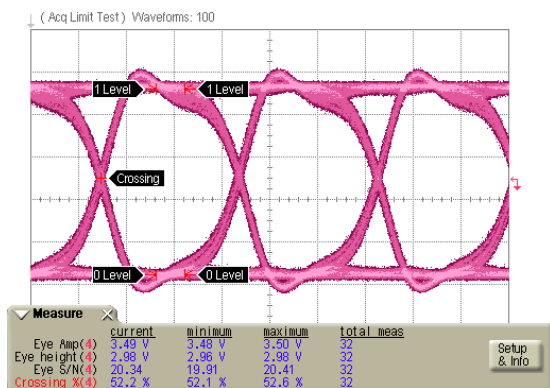
Key Characteristics: $V_{d1}=V_{d2}=5.0V \pm 5\%$, $Z_o=50\Omega$,
 V_{g1} and V_{g2} adjusted to obtain $I_{d1}=I_{d2}=90mA$ respectively with no input signal applied
 Values as measured on Microsemi P495r1 evaluation board (includes PCB loss & blocking capacitors)

Parameter	Description	Min	Typ	Max
S21 (dB)	Forward Gain			
	1MHz - 10GHz	19	21	-
	10 - 20GHz	18	20	-
	20 - 30GHz	17	19	-
S11 (dB)	Input Return Loss			
	1MHz - 10GHz	-	-15	-12
	10 - 20GHz	-	-14	-10
	20 - 30GHz	-	-10	-6
S22 (dB)	Output Return Loss			
	1MHz - 10GHz	-	-15	-12
	10 - 20GHz	-	-13	-10
	20 - 30GHz	-	-12	-8
Pout	Output Power w/ $V_{in}=200mV$			
	1MHz - 10GHz	8.5	10	-
	10 - 16GHz	9	10	-
P _{sat}	Output Power w/ $V_{in}=650mV$			
	1MHz - 10GHz	16	16.5	-
	10 - 16GHz	16	16.5	-

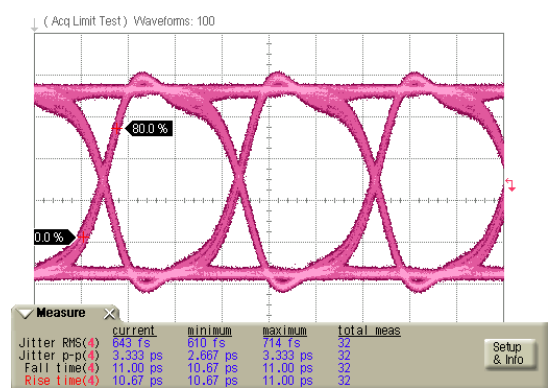
Typical Performance (data collected w/eval board)



EYES @ 23 Gb/s (400mVin)



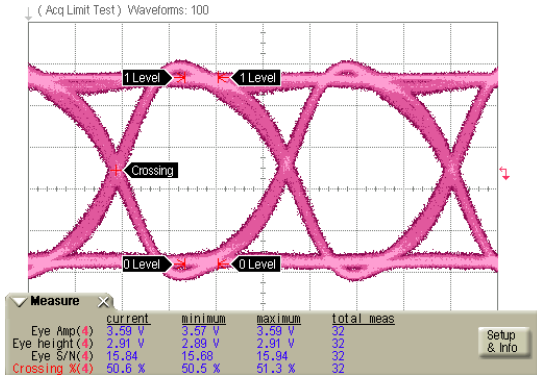
Voltage Measurements



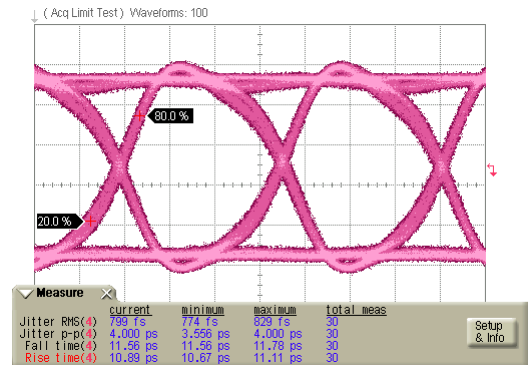
Time Measurements

Typical Performance (data collected w/eval board)

EYES @ 28 Gb/s (400mVin)

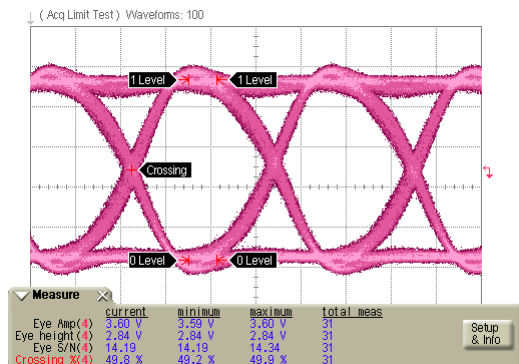


Voltage Measurements

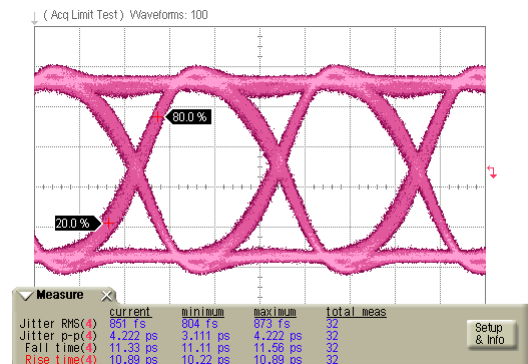


Time Measurements

EYES @ 32 Gb/s (400mVin)

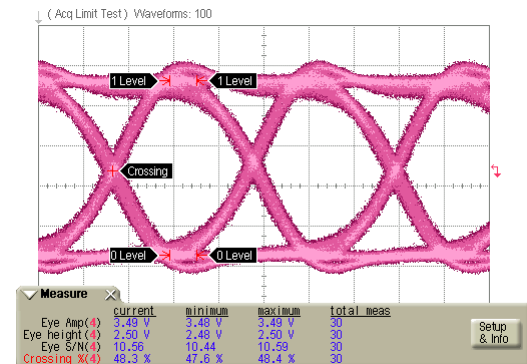


Voltage Measurements

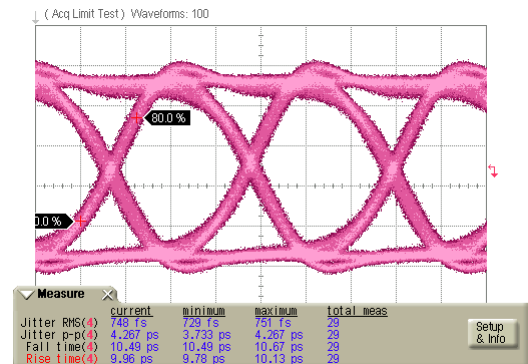


Time Measurements

EYES @ 40 Gb/s (400mVin)

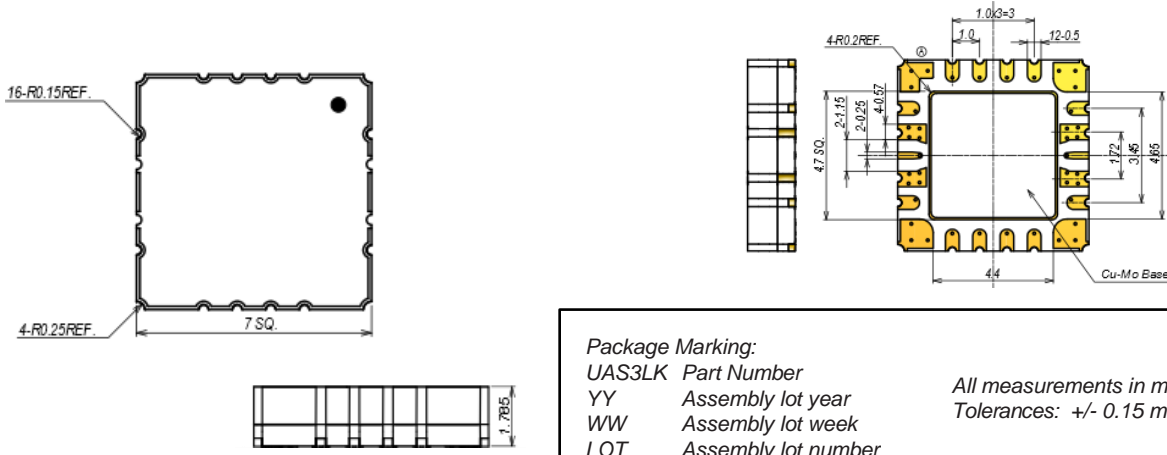


Voltage Measurements



Time Measurements

Physical Characteristics

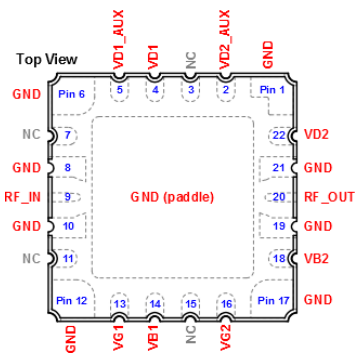


Caution, ESD Sensitive. Unpack and handle only in an ESD-safe environment

Table 1: DC & RF Pin Description

Pin #	Pin Name	Description
1,6,8,10,12,17,19,21	GND	Package Ground
2	VD2_AUX	Drain Bypass, 2nd Stage (typically leave open)
3,7,11,15	NC	No Connect
4	VD1	Drain Bias, 1st Stage
5	VD1_AUX	Drain Bypass, 1st Stage (typically leave open)
9	RF_IN	RF Input (DC coupled)
13	VG1	1st Gate Bias, 1st Stage
14	VB1	2nd Gate Bias, 1st Stage (typically leave open)
16	VG2	1st Gate Bias, 2nd Stage
18	VB2	2nd Gate Bias, 2nd Stage (typically leave open)
20	RF_OUT	RF Output (DC coupled)
22	VD2	Drain Bias, 2nd Stage
Paddle	GND	Package Ground

Pin Labeling



Functional Block Diagram

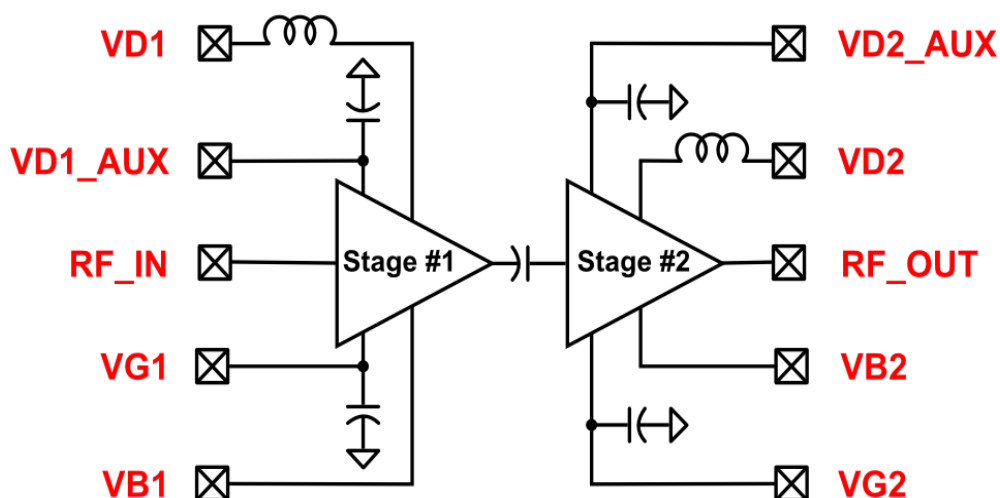


Table 2: Supplemental Specifications

Parameter	Description	Typical Operating Conditions			Absolute Max Ratings*
		Min	Typ	Max	
Vd1, Vd2	Drain Bias Voltage	+4.750 V	+5.000 V	+5.250 V	-1/+9 V
Id1, Id2	Drain Bias Current	75 mA	90 mA	150 mA	180 mA
Vg1, Vg2	1st Gate Bias Voltage (common source FET)	-0.5 V	-0.2 V	+0.2 V	-4/+0.6 V
Ig1, Ig2	1st Gate Bias Current (common source FET)	-1000 uA	-50 uA	0.0 uA	5 mA
Vb1, Vb2	2nd Gate Bias Voltage (common gate FET)	-1.0 V	Vd1/3	Vd1	-2/+9 V
Ib1, Ib2	2nd Gate Bias Current (common gate FET)	-5 mA	-	+5 mA	10 mA
Pdc	Power Dissipation**	-	0.90 W	1.58 W	-
Tcase	Base Temperature	-5 °C	-	+80 °C	-10/+100 °C
Tstore	Storage Temperature	-	-	+100 °C	-40/+125 °C
Vdc_output	DC Voltage @ RF Output	-	Vd – 4*Id	-	-1/+9 V
Idc_output	DC Current @ RF Output	-	-	150 mA	180 mA
Vdc_input	DC Voltage @ RF Input	-	-0.2	-	-4/+0.6 V
Idc_input	DC Current @ RF Input	-20 mA	-	20 mA	+/-50 mA
Lead Soldering	-	-	-	+260 °C for 5 sec	-

*Operation beyond the values listed under the Absolute Maximum Ratings may cause permanent damage to the device. Prolonged operation at conditions outside those indicated in Typical Operating Conditions may affect device reliability.

**Combinations of supply voltage, supply current, input power, and output power shall not exceed the maximum power dissipation listed above.

Information contained in this document is proprietary to Microsemi. This document may not be modified in any way without the express written consent of Microsemi. Product processing does not necessarily include testing of all parameters. Microsemi reserves the right to change the configuration and performance of the product and to discontinue product at any time.

Microsemi Corporate Headquarters

One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense and security, aerospace, and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs, and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 3,400 employees globally. Learn more at www.microsemi.com.

© 2014 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.