16-Channel Serial to Parallel Converter with High Voltage Backplane Driver and Push-Pull Outputs

Features

- HVCMOS® technology
- Output voltage up to +200V
- Shift register speed 500kHz @ V_{DD} = 2.0V
- 16 high voltage outputs
- High voltage backplane driver
- CMOS input levels

Applications

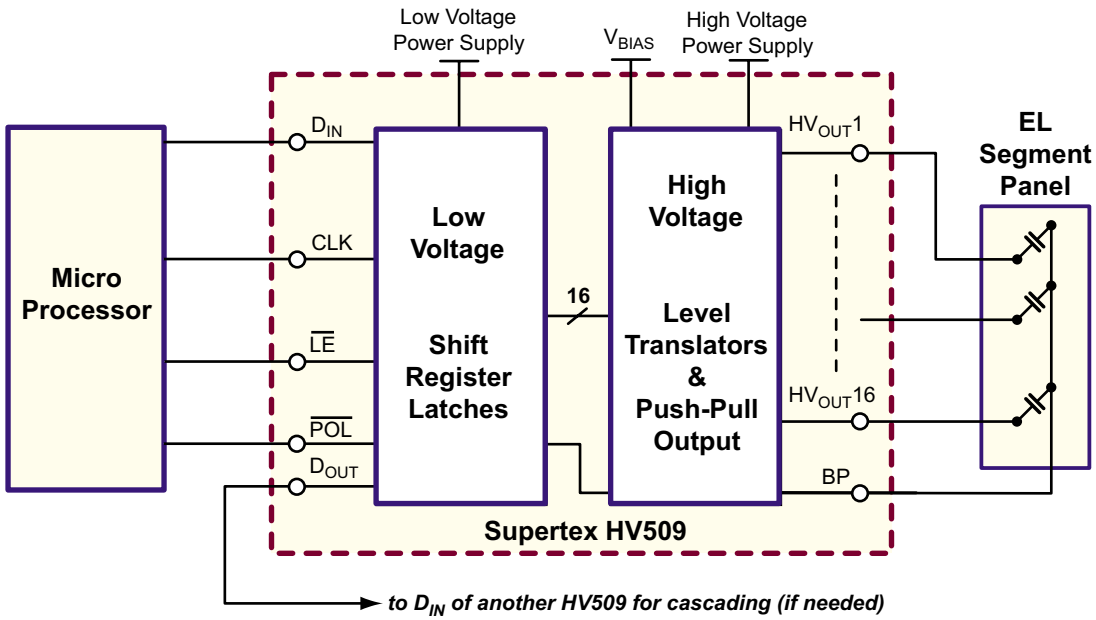
- Multiple segment EL display
- Piezoelectric transducer driver
- Braille driver

General Description

The HV509 is a 200V, 16-channel serial to parallel converter. The high voltage outputs and the backplane driver are designed to source and sink ±1.0mA.

The high voltage outputs are controlled by a 16-bit serial shift register, followed by a 16-bit latch. Data is shifted through the shift registers during the low to high clock transition. A data output buffer is provided for cascading multiple devices. Data is transferred to the 16-bit latch when a logic level low is applied to the $\overline{LE}$ input. Data is stored in the latch when $\overline{LE}$ is high. Output states are controlled by the data in the latch and by the $\overline{POL}$ pin.

Typical Application Circuit

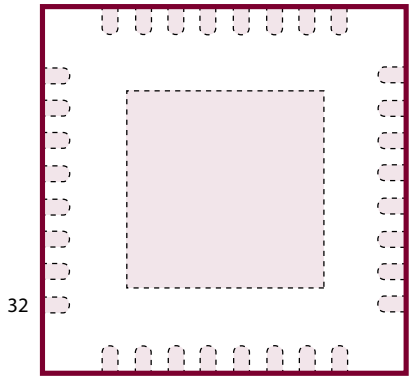


Ordering Information

Device	Package Option
	32-Lead QFN ***5.00x5.00mm body*** ***1.00mm height (max)*** ***0.50mm pitch***
HV509	HV509K6-G

-G indicates package is RoHS compliant ('Green')

Pin Configuration



32-Lead QFN
(top view)

Pads are at the bottom of the package.
Exposed heat slug is at V_{PP} potential.

Absolute Maximum Ratings

Parameter	Value
Logic supply, V_{DD}	-0.5V to 7.0V
High voltage supply, V_{PP}	215V
Translator supply voltage, V_{BIAS}	-0.5V to 7.0V
Logic input levels	-0.5V to V_{DD} + 0.5V
Operating junction temperature	-40°C to +125°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
___ = "Green" Packaging

32-Lead QFN (K6)

Operating Supply Voltages and Conditions

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Logic supply voltage	2.0	3.0	5.5	V	---
V_{BIAS}	Level translator supply voltage	2.6	-	6.6	V	---
V_{PP}	Positive high voltage supply	50	-	200	V	---
V_{IH}	High-level input voltage	$0.9V_{DD}$	-	V_{DD}	V	---
V_{IL}	Low-level input voltage	0	-	$0.1V_{DD}$	V	---
T_A	Operating temperature	0	-	+70	°C	---

Notes:

1. External ground noise reduction circuit will be provided by design upon characterization.
2. Power-up sequence should be the following*:
    1. Apply ground
    2. Apply V_{DD}
    3. Set all inputs (D_{IN}, CLK, $\overline{LE}$, $\overline{POL}$) to a known state
    4. Apply V_{BIAS}
    5. Apply V_{PP}
3. ***Power-down sequence should be the reverse of the above.***

*This power up sequence requires an external high voltage diode between VDD and VPP. Without the diode, power up VPP to a VDD level first to bias the silicon substrate. After all other signals are powered, finish raising the V_{PP} to its final level.

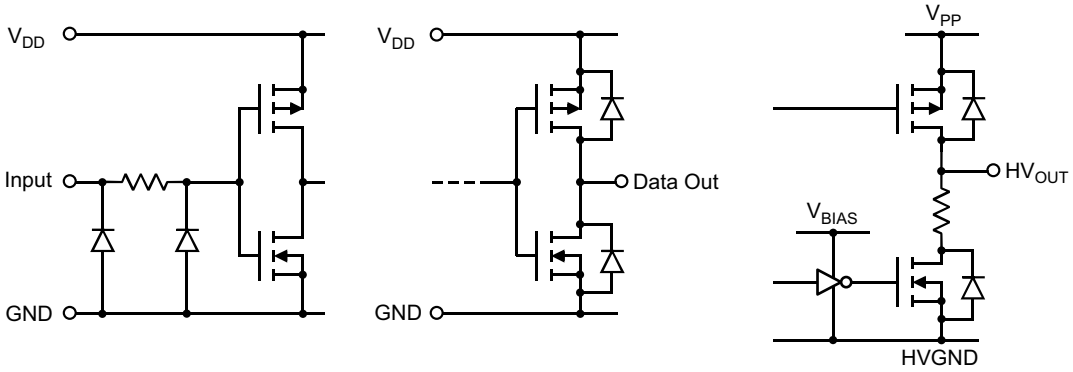
DC Electrical Characteristics *(Over operating supply voltages and temperature, unless otherwise noted)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-	-	1.0	mA	f_{CLK} = 500kHz
I_{DDQ}	Quiescent V_{DD} supply current		-	-	10	µA	All logic inputs = V_{DD} or 0V
I_{BIAS}	V_{BIAS} supply current		-	-	100	µA	All HV_{OUTS} switching at 1kHz. Peak I_{BIAS} = 200mA with all channels switching
I_{BIASQ}	Quiescent V_{BIAS} current		-	-	10	µA	No HV_{OUT} switching
I_{PPQ}	Quiescent V_{PP} supply current		-	-	100	µA	V_{PP} = 200V, outputs are static
I_{IH}	High-level logic input current		-	-	10	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current		-	-	-10	µA	V_{IL} = 0V
V_{OH}	High level output	HV_{OUT} & BP	V_{PP} - 12V	-	-	V	IHV_{OUT} = -1.0mA, V_{PP} = +200V
			V_{PP} - 12V	--	-	V	IHV_{OUT} = -1.0mA, V_{PP} = +50V
		D_{OUT}	V_{DD} - 1.0V	-	-	V	ID_{OUT} = -1.0mA
V_{OL}	Low level output	HV_{OUT} & BP	-	-	12	V	IHV_{OUT} = 1.0mA, V_{BIAS} = 5.4V, V_{PP} = +50 to +200V
		D_{OUT}	-	-	1.0	V	ID_{OUT} = 1.0mA
C_{DIN}	Logic input capacitance		-	-	10	pF	---
C_{DOUT}	Logic output capacitance		-	-	10	pF	---

AC Electrical Characteristics *(Over operating supply voltages and temperature, unless otherwise noted)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock frequency	0	-	500	kHz	---
t_C	Clock high / low pulse width	1.0	-	-	µs	---
t_{SU}	Data setup time before clock rises	50	-	-	ns	---
t_H	Data hold time after clock rises	50	-	-	ns	---
t_{CLE}	$\overline{LE}$ from CLK setup time	15	-	-	ns	---
t_{WLE}	$\overline{LE}$ pulse width	100	-	-	ns	---
t_{DD}	Clock negative edge to D_{OUT} delay	-	-	150	ns	C_{LDOUT} = 50pF, (C_{LDOUT} includes C_{DIN} and C_{DOUT})
t_{PHV}	Delay time from inputs for HV_{OUT} / BP to start rise/fall	-	-	500	ns	V_{PP} = 200V, V_{BIAS} = 5.4V
t_{OR}	HV_{OUTPUT} / BP rise time	-	-	300	µs	C_L = 1500pF, V_{PP} = 200V
t_{OF}	HV_{OUTPUT} / BP fall time	-	-	300	µs	C_L = 1500pF, V_{BIAS} = 5.4V, V_{PP} = 200V
t_{OC}	Width of $\overline{POL}$ pulses	$t_{PHV} + t_{OR}/t_{OF}$	-	-	µs	---

Input and Output Equivalent Circuits



Logic Inputs | Logic Data Output | High Voltage Outputs

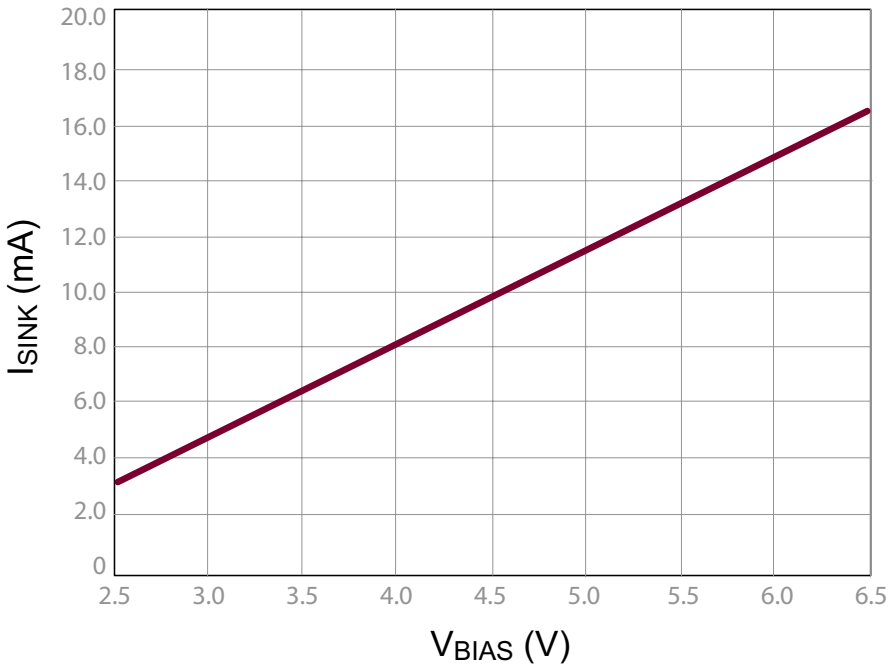
V_{BIAS} SUPPLY

The V_{BIAS} supply operates from 2.6V to 6.6V. It is the gate drive voltage for all of the output N-channel MOSFETs. This allows the output peak current sink to be set by varying the V_{BIAS} voltage. A higher V_{BIAS} voltage will increase the current sinking capability.

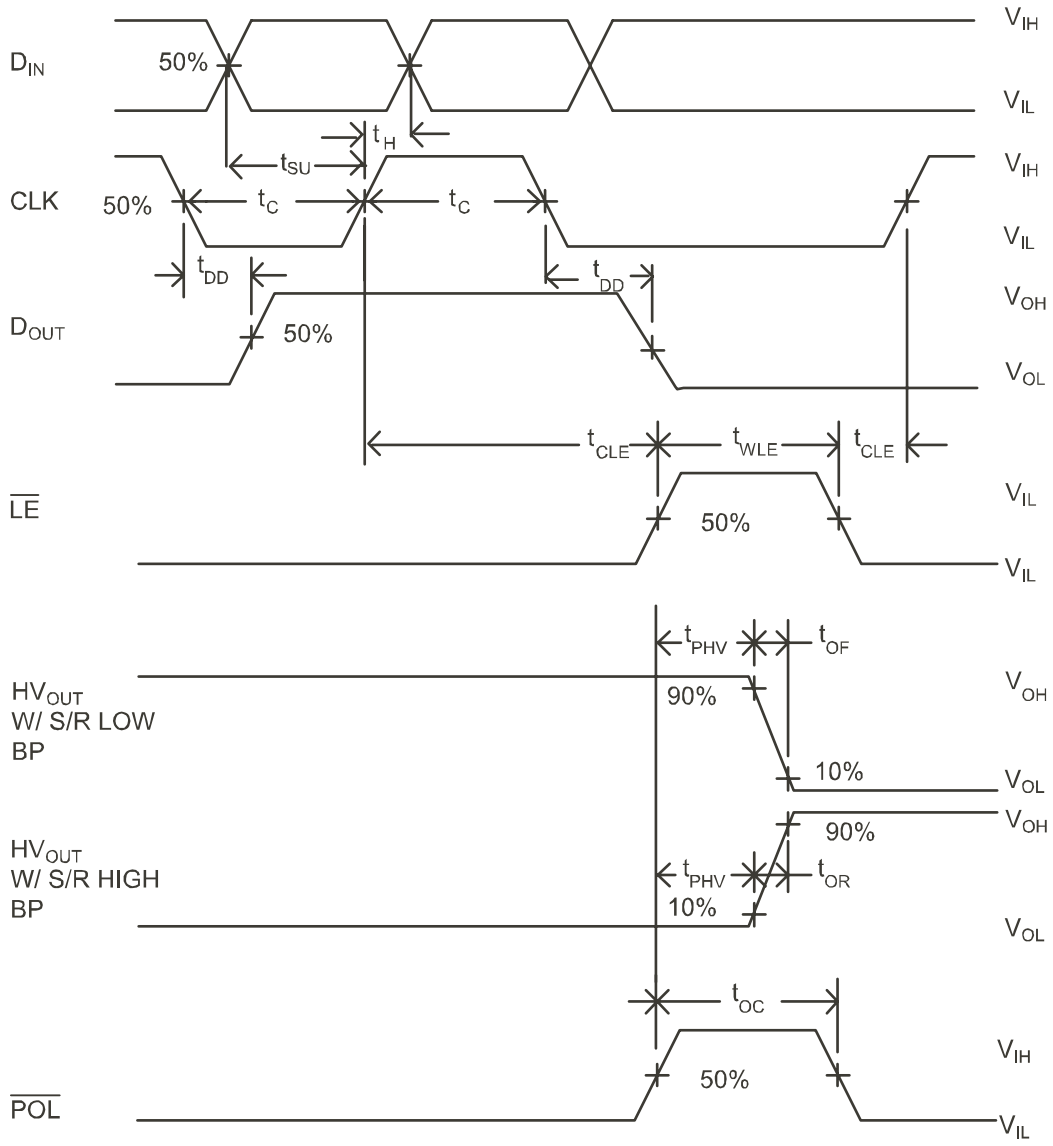
If large peak currents are not required, V_{DD} and V_{BIAS} can be connected to the same power supply, provided they are both within the operating range. The operating V_{DD} range is 2.0V to 5.5V. A plot showing the typical characteristics of I_{SINK} vs V_{BIAS} is shown below.

Typical HV_{OUT} I_{SINK} vs V_{BIAS}

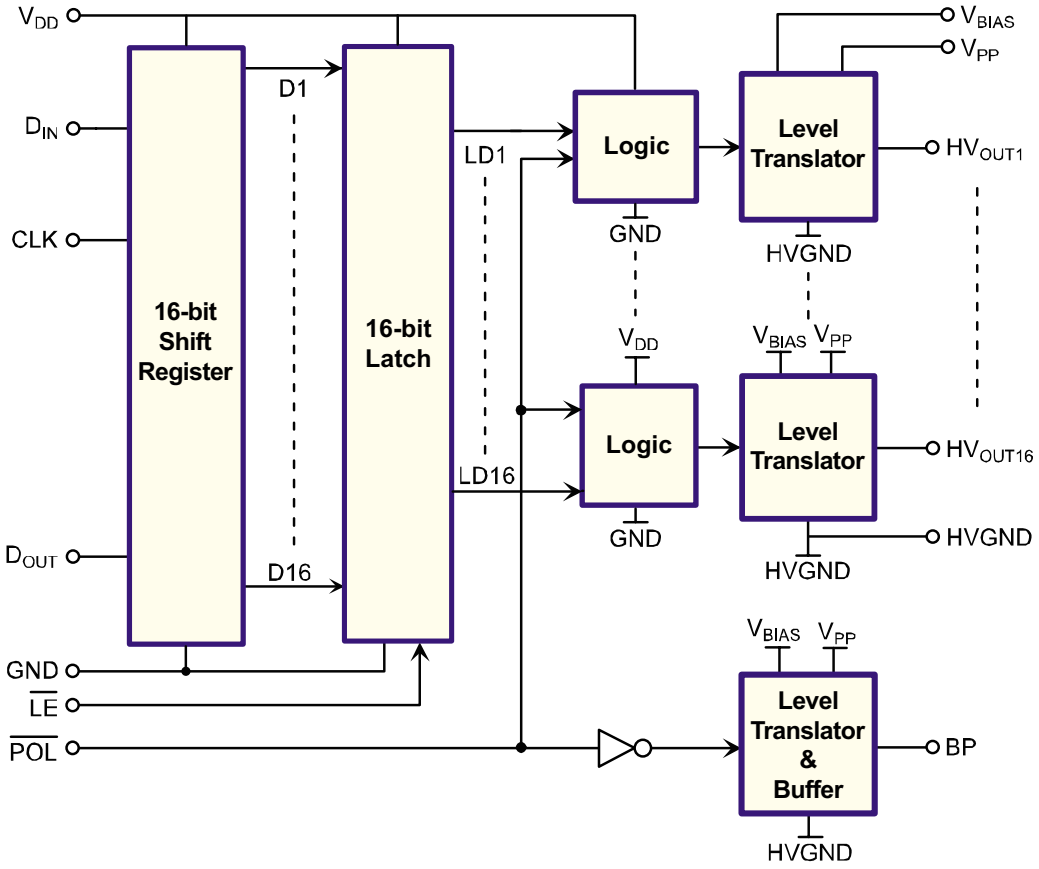
(V_{PP} = 200V, C_{LOAD} = 1nF)



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs				Outputs			
	D_{IN}	CLK	$\overline{LE}$	$\overline{POL}$	Shift Reg 1 2...16	HV Outputs 1 2...16	BP	D_{OUT}
Load S/R	H OR L	↑	H	X	H or L ●...●	● ●...●	X	●
Transfer data in latch	X	L	L	H	* *.....*	* *.....*	L	●
	X	L	L	L	* *.....*	* *.....* (b)	H	●
Store data in latches	X	X	H	H	● ●...●	● ●...●	L	●
	X	X	H	L	● ●...●	● ●...● (b)	H	●
Transparent mode	L	↑	L	H	L ●...●	L ●...●	L	●
	H	↑	L	H	H ●...●	H ●...●	L	●
Invert mode	X	X	H	L	● ●...●	● ●...● (b)	H	X
	X	X	H	H	● ●...●	● ●...●	L	X

Notes:

H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition

● = dependent on previous stage's state before the last CLK or last $\overline{LE}$ low

* = data at the last CLK ↑

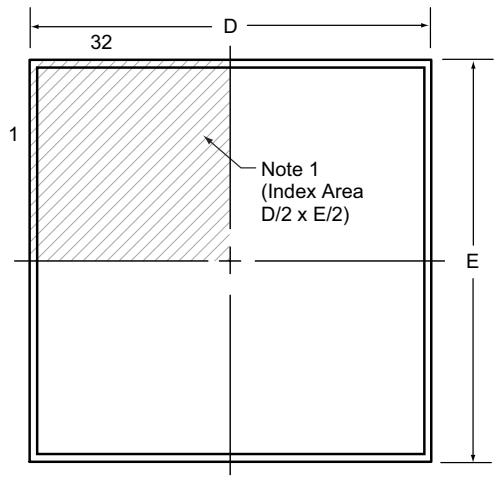
(b) = bar over all symbols

Pin Description

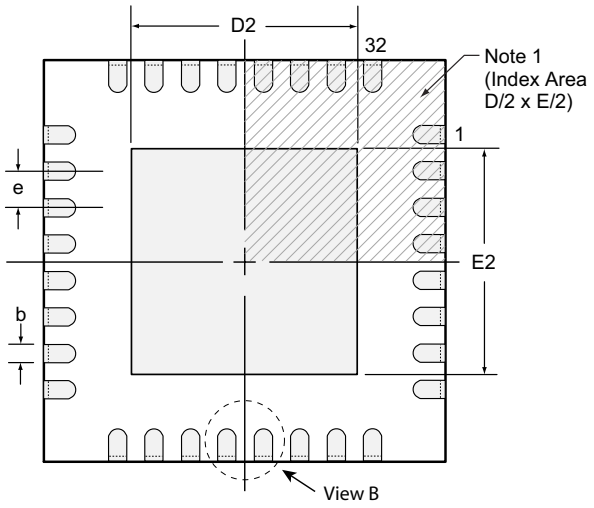
Pin #	Function	Description
1	$HV_{OUT}12$	High voltage push-pull output
2	$HV_{OUT}11$	High voltage push-pull output
3	$HV_{OUT}10$	High voltage push-pull output
4	$HV_{OUT}9$	High voltage push-pull output
5	$HV_{OUT}8$	High voltage push-pull output
6	$HV_{OUT}7$	High voltage push-pull output
7	$HV_{OUT}6$	High voltage push-pull output
8	$HV_{OUT}5$	High voltage push-pull output
9	$HV_{OUT}4$	High voltage push-pull output
10	$HV_{OUT}3$	High voltage push-pull output
11	$HV_{OUT}2$	High voltage push-pull output
12	$HV_{OUT}1$	High voltage push-pull output
13	NC	No connect
14	VPP	High voltage supply
15	GND	Logic ground
16	NC	No connect
17	DIN	Data in
18	NC	No connect
19	CLK	Clock input logic
20	VDD	Logic supply voltage
21	$\overline{POL}$	Polarity bar input logic
22	$\overline{LE}$	Latch enable bar input logic
23	NC	No connect
24	DOUT	Data out
25	NC	No connect
26	VBIAS	Level translator bias voltage
27	HVGND	High voltage ground
28	BP	High voltage backplane output
29	$HV_{OUT}16$	High voltage push-pull output
30	$HV_{OUT}15$	High voltage push-pull output
31	$HV_{OUT}14$	High voltage push-pull output
32	$HV_{OUT}13$	High voltage push-pull output

32-Lead QFN Package Outline (K6)

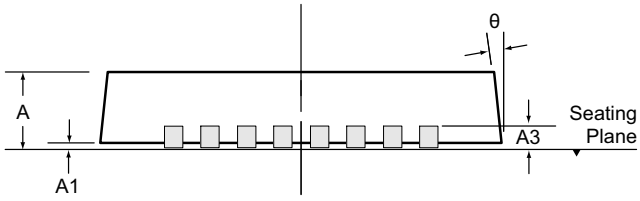
5.00x5.00mm body, 1.00mm height (max), 0.50mm pitch



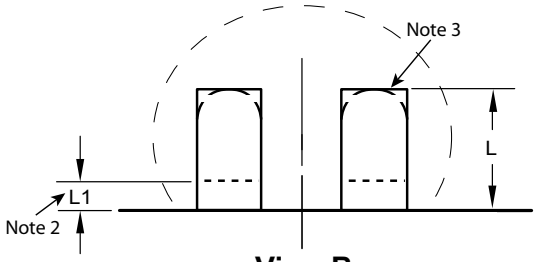
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 Identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	4.85*	1.05	4.85*	1.05	0.50 BSC	0.30†	0.00	0°
	NOM	0.90	0.02		0.25	5.00	-	5.00	-		0.40†	-	-
	MAX	1.00	0.05		0.30	5.15*	3.55†	5.15*	3.55†		0.50†	0.15	14°

JEDEC Registration MO-220, Variation VHHD-6, Issue K, June 2006.
** This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.*
† This dimension is a non-JEDEC dimension.
Drawings not to scale.
***Supertex Doc. #:** DSPD-32QFNK65X5P050, Version B090808.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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