MIC5163

Dual Regulator Controller for DDR3 GDDR3/4/5 Memory Termination

General Description

The MIC5163 is a dual regulator controller designed specifically for low voltage memory termination applications such as DDR3 and GDDR3/4/5. The MIC5163 offers a simple, low cost JEDEC compliant solution for terminating high-speed, low-voltage digital buses.

The MIC5163 controls two external N-Channel MOSFETs to form two separate regulators. It operates by switching between either the high-side MOSFET or the low-side MOSFET, depending on whether the current is being sourced to the load or being sinked by the regulator.

Designed to provide a universal solution for memory termination regardless of input voltage, output voltage, or load current; the desired MIC5163 output voltage can be externally programmed by forcing the reference voltage.

The MIC5163 operates from an input voltage as low as 0.75V up to 6V, with a second bias supply input required for operation. The MIC5163 is available in a tiny MSOP-10 package with an operating junction temperature range of –40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

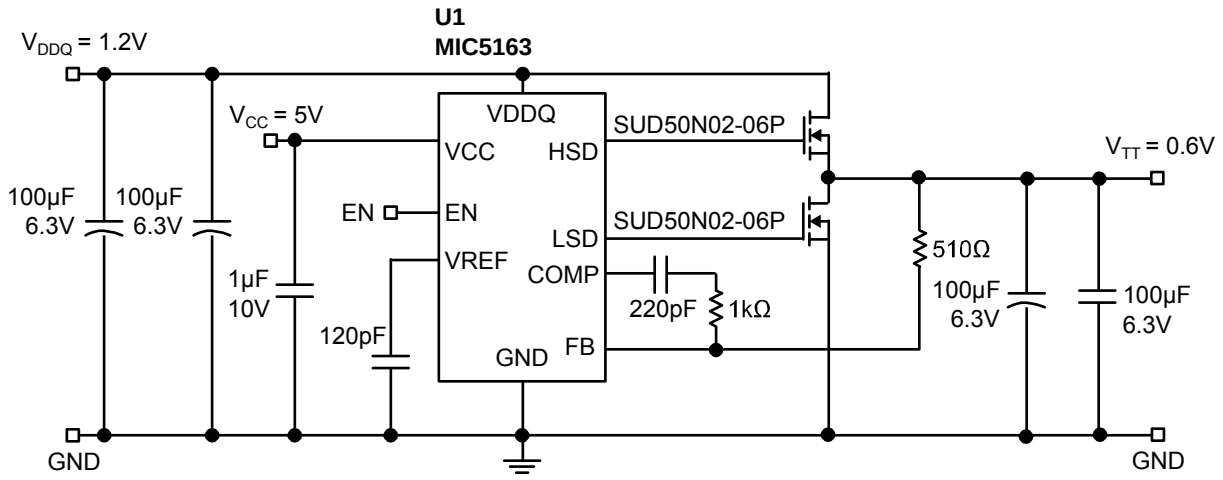
Features

- 0.75V to 6V input supply voltage
- Memory termination for: DDR3, GDDR3/4/5
- Tracking programmable output
- Logic controlled enable input
- Wide bandwidth
- Minimal external components required
- Tiny MSOP-10 package
- –40°C < T_J < +125°C

Applications

- Desktop Computers
- Servers
- Notebook computers
- Workstations

Typical Application



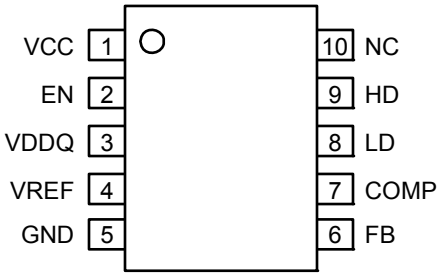
MIC5163 as a DDR3 Memory Termination Device for 3.5A application

Ordering Information

Part Number	Temperature Range	Package	Lead Finish
MIC5163YMM	–40° to +125°C	10-Pin MSOP	Pb-Free

Note: MSOP is a Green RoHs compliant package. Lead finish is NiPdAu. Mold compound is halogen free.

Pin Configuration



10-Pin MSOP (MM)

Pin Description

Pin Number	Pin Name	Pin Function
1	VCC	Bias Supply (Input): Apply a voltage between +3V and +6V to this input for internal bias to the controller
2	EN	Enable (Input): CMOS compatible input. Logic high = enable, logic low = shutdown
3	VDDQ	Input Supply Voltage
4	VREF	Reference output equal to half of VDDQ
5	GND	Ground
6	FB	Feedback input to the internal error amplifier
7	COMP	Compensation (Output): Connect a capacitor to feedback pin for compensation of the internal control loop
8	LD	Low-side drive: Connects to the Gate of the external low-side MOSFET
9	HD	High-side drive: Connects to the Gate of the external high-side MOSFET
10	NC	Not internally connected

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.3V to +7V
Supply Voltage (V_{DDQ}) ..... –0.3V to +7V
Enable Input Voltage (V_{EN}) ..... –0.3V to +7V
Lead Temperature (soldering, 10 sec.) ..... 265°C
Storage Temperature (T_S) ..... –65°C to +150°C
EDS Rating[3] ..... +2kV

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3V to +6V
Supply Voltage (V_{DDQ}) ..... +0.75V to +6V
Enable Input Voltage (V_{EN}) ..... 0V to V_{IN}
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance
MSOP (θ_{JA}) ..... 130.5°C/W
MSOP (θ_{JC}) ..... 42.6°C/W

Electrical Characteristics[4]

V_{DDQ} = 1.35V; T_A = 25°C, **bold** values indicate –40°C ≤ T_J ≤ +125°C, unless noted.

Parameter	Condition	Min	Typ	Max	Units
V_{REF} Voltage Accuracy		-1%	0.5V_{DDQ}	+1%	V
V_{TT} Voltage Accuracy (**Note 5**)	Sourcing; 100mA to 3A	-5 **-10**	0.4	+5 **+10**	mV mV
	Sinking; -100mA to -3A	-5 **-10**	0.4	+5 **+10**	mV mV
Supply Current (I_{DDQ})	V_{EN} = 1.2V (controller ON) No Load		35	70 **100**	µA µA
Supply Current (I_{CC})	No Load		10.5	20 **25**	mA mA
I_{CC} Shutdown Current (**Note 6**)	V_{EN} = 0.2V (controller OFF)		45	90	nA
Start-up Time (**Note 7**)	V_{CC} = 5V external bias; V_{EN} = V_{CC}		8	15 **30**	µs µs
Enable Input					
Enable Input Threshold	Regulator Enable	**1.2**			V
	Regulator Shutdown			**0.3**	V
Enable Hysteresis			35		mV
Enable Pin Input Current	V_{IL} < 0.2V (controller shutdown)		0.011		µA
	V_{IH} > 1.2V (controller enable)		5.75		µA
Driver					
High Side Gate Drive Voltage	High Side MOSFET Fully ON	**4.8**	4.97		V
	High Side MOSFET Fully OFF		0.03	**0.2**	V
Low Side Gate Drive Voltage	Low Side MOSFET Fully ON	**4.8**	4.97		V
	Low Side MOSFET Fully OFF		0.03	**0.2**	

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
4. Specification for packaged product only.
5. The V_{TT} voltage accuracy is measured as a delta voltage from the reference output (V_{TT} - V_{REF}).
6. Shutdown current is measured only on the V_{CC} pin. The V_{DDQ} pin will always draw a minimum amount of current when voltage is applied.

7. Start-up time is defined as the amount of time from EN = V_{CC} to HSD = 90% of V_{CC}

Test Circuit

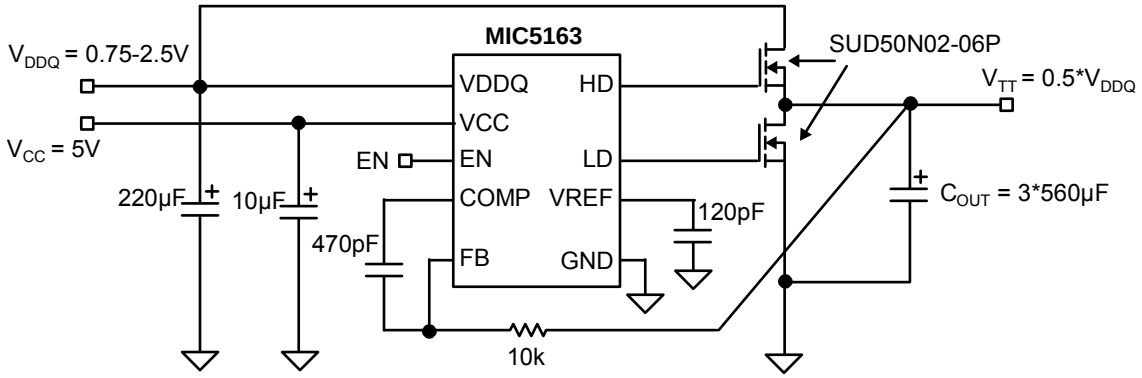
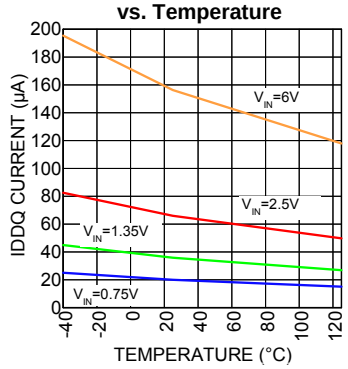


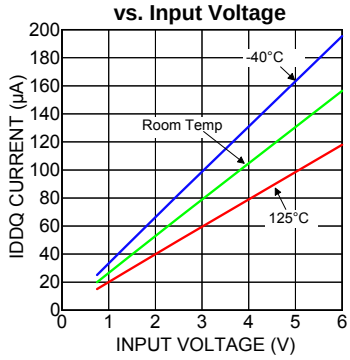
Figure 1. Test Circuit

Typical Characteristics

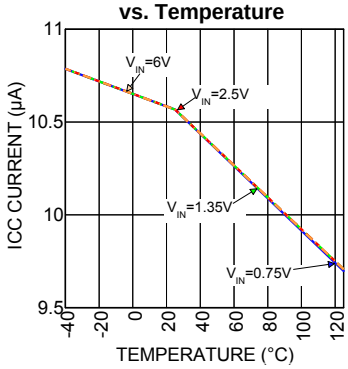
IDDQ Current vs. Temperature



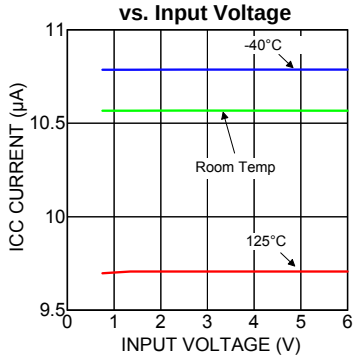
IDDQ Current vs. Input Voltage



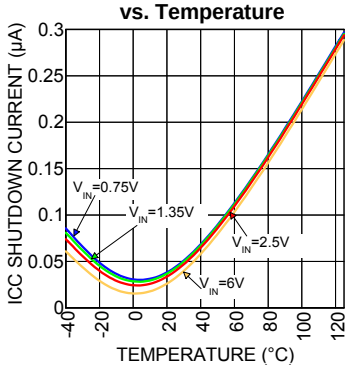
ICC Current vs. Temperature



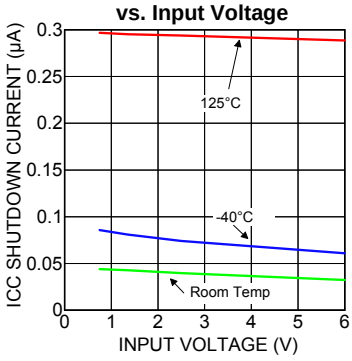
ICC Current vs. Input Voltage



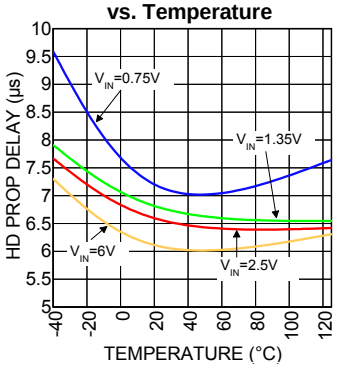
ICC Shutdown Current vs. Temperature



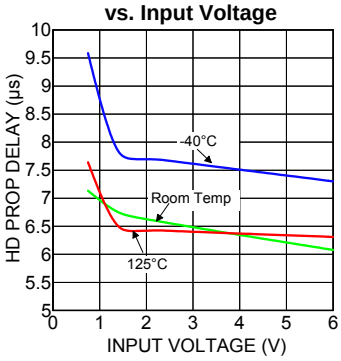
ICC Shutdown Current vs. Input Voltage



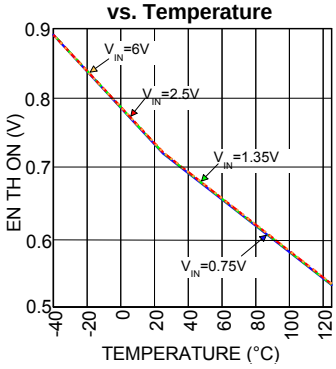
HD Prop Delay vs. Temperature



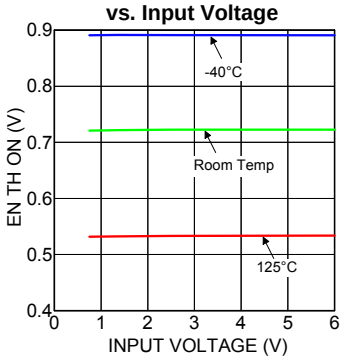
HD Prop Delay vs. Input Voltage



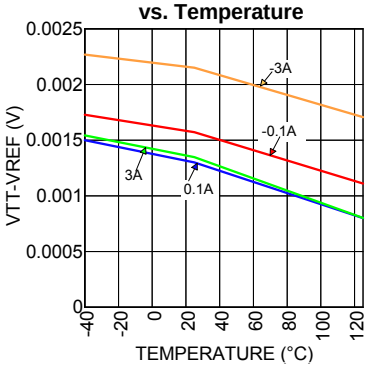
EN TH ON vs. Temperature



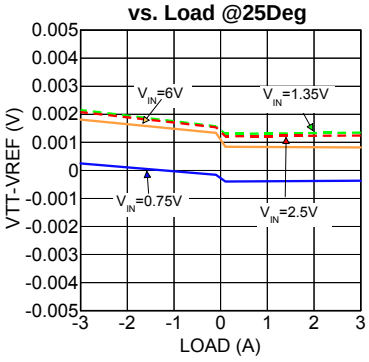
EN TH ON vs. Input Voltage



VTT-VREF vs. Temperature

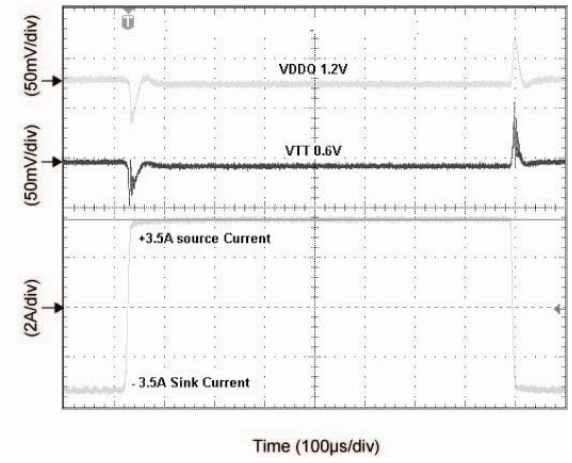


VTT-VREF vs. Load @25Deg

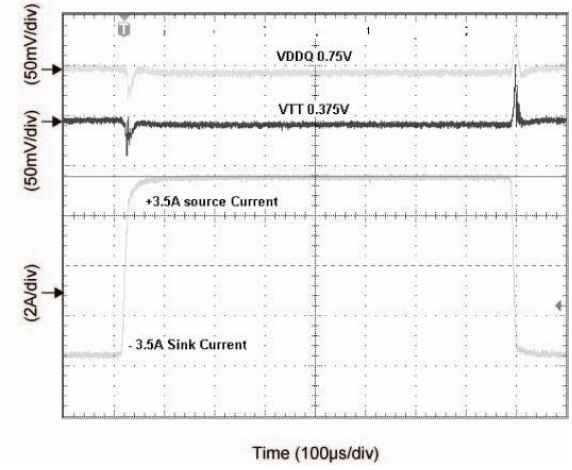


Functional Characteristics

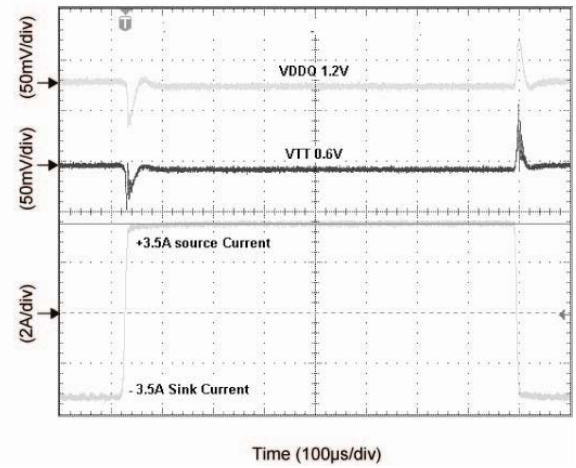
VTT = 0.6V – Load Transient (±3.5A)



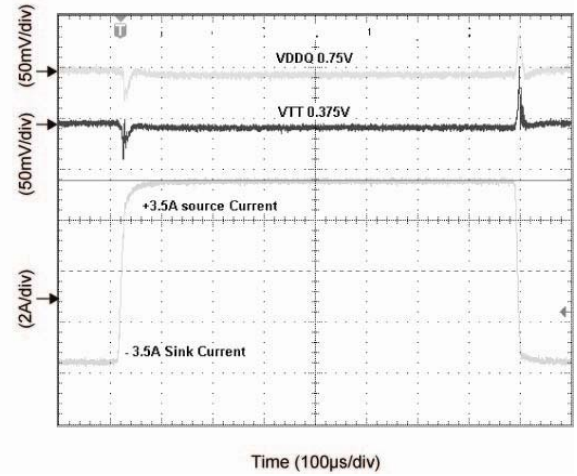
VTT = 0.375V – Load Transient (±3.5A)



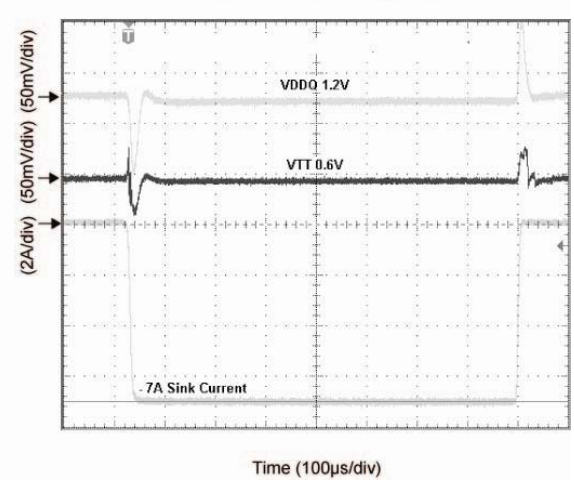
Load Transient (±3.5A)



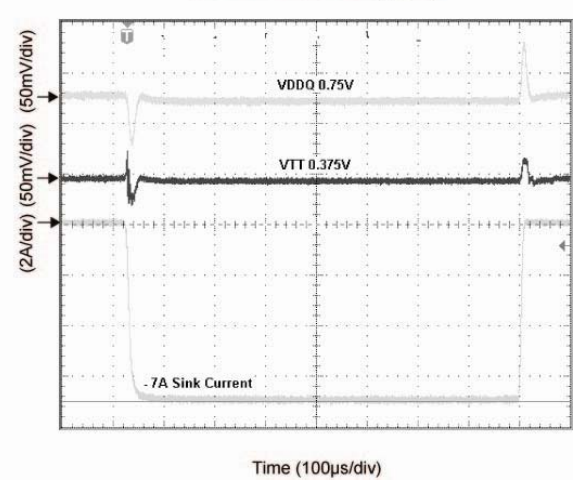
Load Transient (±3.5A)



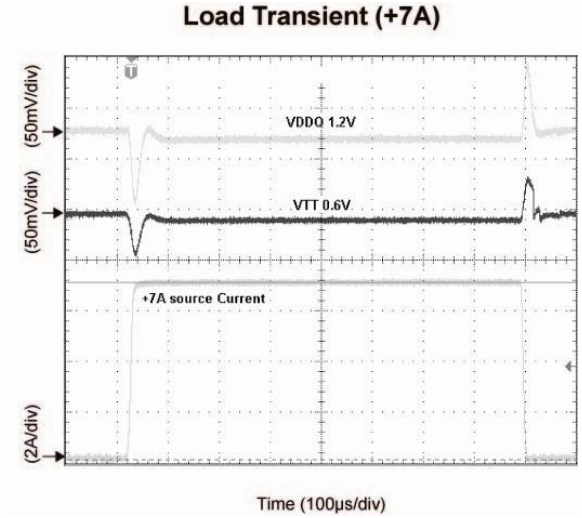
Load Transient (-7A)

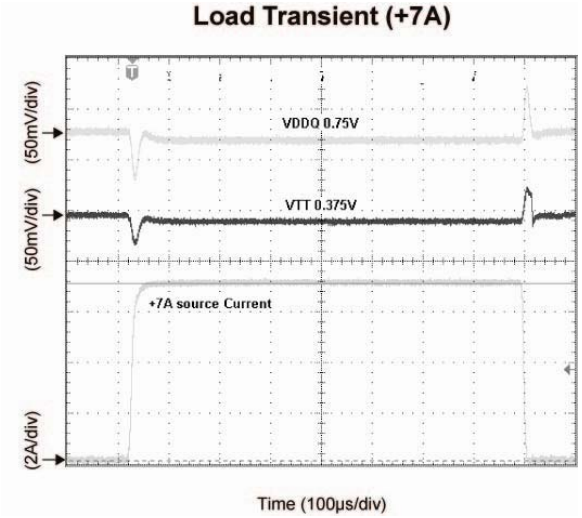


Load Transient (-7A)



Functional Characteristics (continued)





Functional Diagram

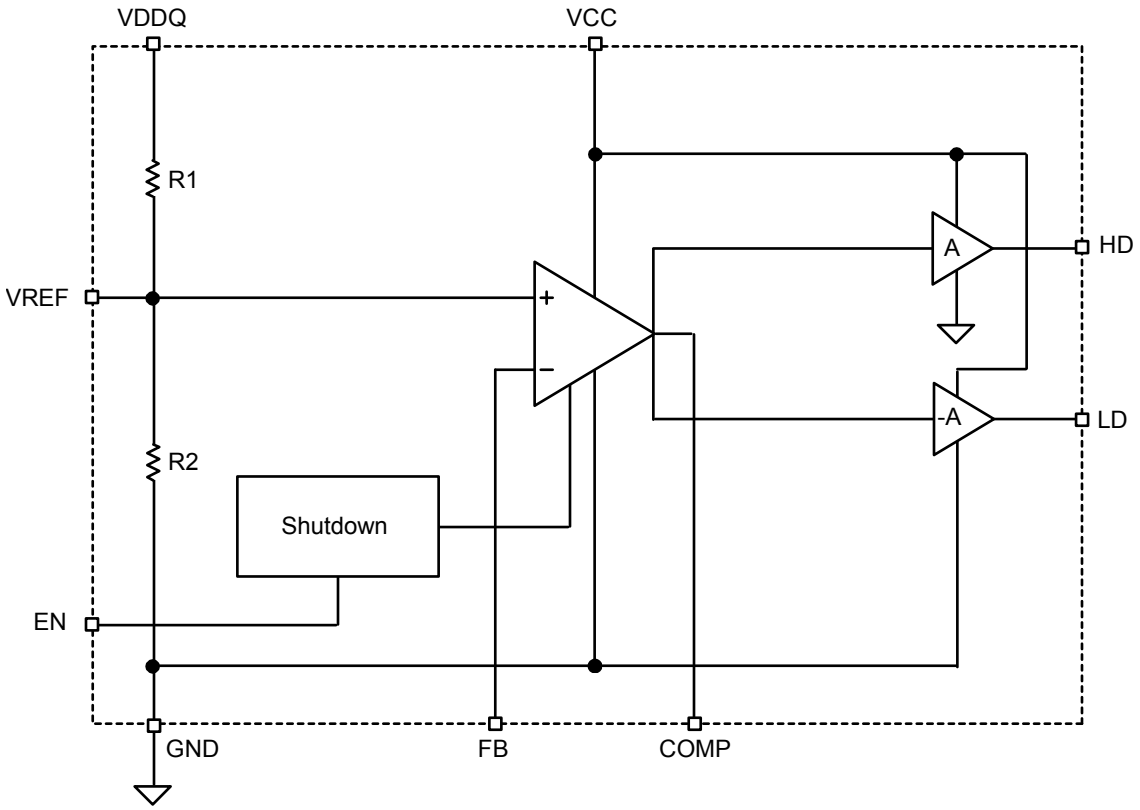


Figure 2. MIC5163 Block Diagram

Functional Description

The MIC5163 is a high performance linear controller, utilizing scalable N-Channel MOSFETs to provide JEDEC compliant bus termination. Termination is achieved by dividing down the V_{DDQ} voltage by a half, providing the reference (V_{REF}) voltage. The MIC5163 controls two external N-Channel MOSFETs to form two separate regulators. It operates by switching between either the high-side MOSFET or the low-side MOSFET, depending on whether the current is being sourced to the load or being sinked by the regulator.

V_{DDQ}

The V_{DDQ} pin on the MIC5163 provides the source current through the high side N-Channel and the reference voltage to the device. The MIC5163 can operate at V_{DDQ} input voltages as low as 0.75V. A bypass capacitance will increase performance by improving the source impedance at higher frequencies.

V_{TT}

V_{TT} is the actual termination point. V_{TT} is regulated to V_{REF}. Due to high speed signaling, the load current seen by V_{TT} is constantly changing. To maintain adequate large signal transient response, Oscons and ceramics are recommended on V_{TT}. The Oscon capacitors provide bulk charge storage while the smaller ceramic capacitors provide current during the fast edges of the bus transition.

V_{REF}

Two resistors dividing down the V_{DDQ} voltage provide V_{REF}. The resistors are valued at around 17kΩ. A minimum capacitor value of 120pF from V_{REF} to ground is mandatory.

V_{CC}

V_{CC} supplies the internal circuitry of the MIC5163 and provides the drive voltage to enhance the external N-Channel MOSFETs. A small 1µF capacitor is recommended for bypassing the V_{CC} pin.

Feedback and Compensation

The feedback provides the path for the error amplifier to regulate the V_{TT}. An external resistor must be placed between the feedback and V_{TT}. Feedback resistor values should not exceed 10kΩ and compensation capacitors should not be less than 40pF.

Enable

The MIC5163 features an active high enable input. In the off mode state, leakage currents are reduced to microamperes. The enable input has thresholds compatible with TTL/CMOS for simple logic interfacing. The enable pin can be tied directly to V_{DDQ} or V_{CC} for functionality.

Application Information

Synchronous Dynamic Random Access Memory (SDRAM) has continually evolved over the years to keep up with ever-increasing computing needs. The latest addition to SDRAM technology is DDR3 SDRAM. DDR3 SDRAM is the third generation of the DDR SDRAM family and offers improved power savings, higher data bandwidth and enhanced signal quality with multiple on-die termination (ODT) selection. In DDR3 SDRAM the values of the ODT are based on the value of an external resistor. In addition to using this external resistor for setting the ODT value, it is also used for calibrating the ODT value so that it maintains its resistance value to within a 10% tolerance.

To improve signal integrity and support higher frequency operations, the JEDEC committee defined a fly-by termination scheme used with the clocks, the command bus and address bus signals. The fly-by topology reduces simultaneous switching noise (SSN) by deliberately causing flight-time skew between the data and strobes at every DRAM as the clock, address and command signals traverse the DIMM.

The DDR3 SDRAM uses a programmable impedance output buffer. Currently, there are two drive strength settings, 34Ω and 40Ω. The 40Ω drive strength setting is currently a reserved specification defined by JEDEC, but available on the DDR3 SDRAM.

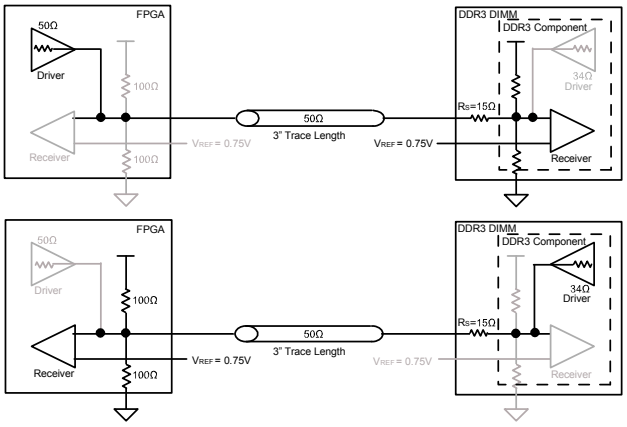


Figure 3. Dynamic OCT between Stratix III/IV FPGA Devices

The MIC5163 is a high performance linear controller that utilizes scalable N-Channel MOSFETs to provide JEDEC compliant bus termination. Termination is achieved by dividing down the V_{DDQ} voltage by half to provide the reference (V_{REF}) voltage. An internal error amplifier compares the termination voltage (V_{TT}) and V_{REF}, controlling two external N-Channel MOSFETs to sink and/or source current to maintain a termination voltage (V_{TT}) equal to V_{REF}. The N-Channels receive their enhancement voltage from a separate V_{CC} pin on the device. Although the general discussion is focused on DDR3, the MIC5163 is also capable of providing bus terminations for DDR, DDR2 and GDDR3/4/5.

V_{DDQ}

The V_{DDQ} pin on the MIC5163 provides the source current through the high side N-Channel and the reference voltage to the device. The MIC5163 can operate at V_{DDQ} voltages as low as 0.75V. Due to the possibility of large transient currents being sourced from this line, significant bypass capacitance will increase performance by improving the source impedance at higher frequencies. Since the reference is simply $V_{DDQ}/2$, perturbations on the V_{DDQ} will also appear at half the amplitude on the reference. For this reason, low ESR capacitors such as ceramics or Oscons are recommended on V_{DDQ}.

V_{TT}

V_{TT} is the actual termination point. V_{TT} is regulated to V_{REF}. Due to high speed signaling, the load current seen by V_{TT} is constantly changing. To maintain adequate large signal transient response, Oscons and ceramics are recommended on V_{TT}. The proper combination and placement of the Oscon and ceramic capacitors is important to reduce both ESR and ESL such that high-current high-speed transients do not exceed the dynamic voltage tolerance requirement of V_{TT}. The Oscon capacitors provide bulk charge storage while the smaller ceramic capacitors provide current during the fast edges of the bus transition. Using several smaller ceramic capacitors distributed near the termination resistors is typically important to reduce the effects of PCB trace inductance.

V_{REF}

Two resistors dividing down the V_{DDQ} voltage provide V_{REF} (Figure 5). The resistors are valued at around 17kΩ. A minimum capacitor value of 120pF from V_{REF} to ground is required to remove high frequency signals reflected from the source. Large capacitance values (>1500pF) should be avoided. Values greater than 1500pF slow down V_{REF} and detract from the reference voltage's ability to track V_{DDQ} during high speed load transients.

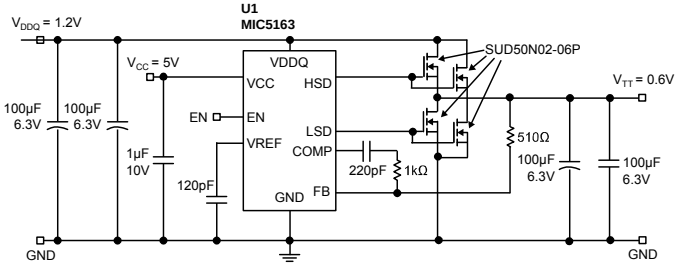


Figure 4. MIC5163 as a DDR3 Memory Termination Device for 7A Application

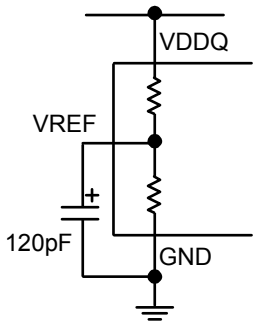


Figure 5. V_{DDQ} Divided Down to Provide V_{REF}

V_{REF} can also be manipulated for different applications. A separate voltage source can be used to externally set the reference point, bypassing the divider network. Also, external resistors can be added from V_{REF}-to-ground or V_{REF}-to-V_{DDQ} to shift the reference point up or down.

V_{CC}

V_{CC} supplies the internal circuitry of the MIC5163 and provides the drive voltage to enhance the external N-Channel MOSFETs. A small 1µF capacitor is recommended for bypassing the V_{CC} pin. The minimum V_{CC} voltage should be a gate-source voltage above V_{TT} without exceeding 6V. For example, on an DDR3 compliant terminator, V_{DDQ} equals 1.5V and V_{TT} equals 0.75V. If the N-Channel MOSFET selected requires a gate source voltage of 2.5V, V_{CC} should be a minimum of 3.25V

Feedback and Compensation

The feedback provides the path for the error amplifier to regulate V_{TT}. An external resistor must be placed between the feedback and V_{TT}. This allows the error amplifier to be correctly externally compensated. For most applications, a 510Ω resistor is recommended. The COMP pin on the MIC5163 is the output of the internal error amplifier. By placing a capacitor and resistor between the COMP pin and the feedback pin, this coupled with the feedback resistor, places an external pole and zero on the error amplifier. With a 510Ω feedback resistor, a minimum 220pF capacitor is recommended for a 3.5A peak termination circuit. An increase in the load will require additional N-Channel MOSFETs and/or increase in output capacitance may require feedback and/or compensation capacitor values to be changed to maintain stability. Feedback resistor values should not exceed 10kΩ and compensation capacitors should not be less than 40pF.

Enable

The MIC5163 features an active high enable input. In the off mode state, leakage currents are reduced to microamperes. The enable input has thresholds compatible with TTL/CMOS for simple logic interfacing. The enable pin can be tied directly to V_{DDQ} or V_{CC} for functionality. Do not float the enable pin. Floating this pin causes the enable to be in an indeterminate state.

Input Capacitance

Although the MIC5163 does not require an input capacitor for stability, using one greatly improves device performance. Due to the high-speed nature of the MIC5163, low ESR capacitors such as Oscon and ceramics are recommended for bypassing the input. The recommended value of capacitance will depend greatly on the proximity to the bulk capacitance. Although a 10µF ceramic capacitor will suffice for most applications, input capacitance may need to be increased in cases where the termination circuit is greater than 1-inch away from the bulk capacitance.

Output Capacitance

Large, low ESR capacitors are recommended for the output (V_{TT}) of the MIC5163. Although low ESR capacitors are not required for stability, they are recommended to reduce the effects of high-speed current transients on V_{TT}. The change in voltage during the transient condition will be the effect of the peak current multiplied by the output capacitor's ESR. For that reason, Oscon type capacitors and ceramic are excellent choices for this application. Oscon capacitors have extremely low ESR and a large capacitance-to-size ratio. Ceramic capacitors are also well suited to termination due to their low ESR. These capacitors should have a dielectric rating of X5R or X7R. Y5V and Z5U type capacitors are not recommended, due to their poor performance at high frequencies and over temperature. The minimum recommended capacitance for a 3.5A peak circuit is 100µF. Output capacitance can be increased to achieve greater transient performance.

MOSFET Selection

The MIC5163 utilizes external N-Channel MOSFETs to sink and source current. MOSFET selection will settle to two main categories: size and gate threshold (V_{GS}).

MOSFET Power Requirements

One of the most important factors is to determine the amount of power the MOSFET is going to be required to dissipate. Power dissipation in a DDR3 circuit will be identical for both the high side and low side MOSFETs. Since the supply voltage is divided by half to supply V_{TT}, both MOSFETs have the same voltage dropped across them. They are also required to be able to sink and source the same amount of current (for either all 0s or all 1s). This equates to each side being able to dissipate the same amount of power. Power dissipation calculation for the high-side MOSFET is as follows:

$$P_D = (V_{DDQ} - V_{TT}) \times I_SOURCE$$

Where I_source is the average source current. Power dissipation for the low-side MOSFET is as follows:

$$P_D = V_{TT} \times I_SINK$$

Where I_sink is the average sink current.

In a typical 3.5A peak DDR3 circuit, power considerations for MOSFET selection would occur as follows.

$$P_D = (V_{DDQ} - V_{TT}) \times I_SOURCE$$

$$P_D = (1.5V - 0.75V) \times 1.75A$$

$$P_D = 1.3125\ W$$

This typical DDR3 application would require both high-side and low-side N-Channel MOSFETs to be able to handle 1.3125 Watts each. In applications where there is excessive power dissipation, multiple N-Channel MOSFETs may be placed in parallel. These MOSFETs will share current, distributing power dissipation across each device.

The maximum MOSFET die (junction) temperature limits maximum power dissipation. The ability of the device to dissipate heat away from the junction is specified by the junction-to-ambient (θ_{JA}) thermal resistance. This is the sum of junction-to-case (θ_{JC}) thermal resistance, case-to-sink (θ_{CS}) thermal resistance and sink-to-ambient (θ_{SA}) thermal resistance;

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

In our example of a 3.5A peak DDR3 termination circuit, we have selected a D-pack N-Channel MOSFET that has a maximum junction temperature of 150°C. The device has a junction-to-case thermal resistance of 1.5°C/W. Our application has a maximum ambient temperature of 60°C. The required junction-to-ambient thermal resistance can be calculated as follows:

$$\theta_{JA} = \frac{T_J - T_A}{P_D}$$

Where T_J is the maximum junction temperature, T_A is the maximum ambient temperature and P_D is the power dissipation.

In our example:

$$\theta_{JA} = \frac{T_J - T_A}{P_D}$$

$$\theta_{JA} = \frac{150°C - 60°C}{1.3125W}$$

$$\theta_{JA} = 68.57\frac{°C}{W}$$

This shows that our total thermal resistance must be better than 68.57°C/W. Since the total thermal resistance is a combination of all the individual thermal resistances, the amount of heat sink required can be calculated as follows:

$$\theta_{SA} = \theta_{JA} - (\theta_{JC} + \theta_{CS})$$

In our example:

$$\theta_{SA} = \theta_{JA} - (\theta_{JC} + \theta_{CS})$$

$$\theta_{SA} = 68.57\frac{°C}{W} - \left(1.5\frac{°C}{W} + 0.5\frac{°C}{W}\right)$$

$$\theta_{SA} = 66.57\frac{°C}{W}$$

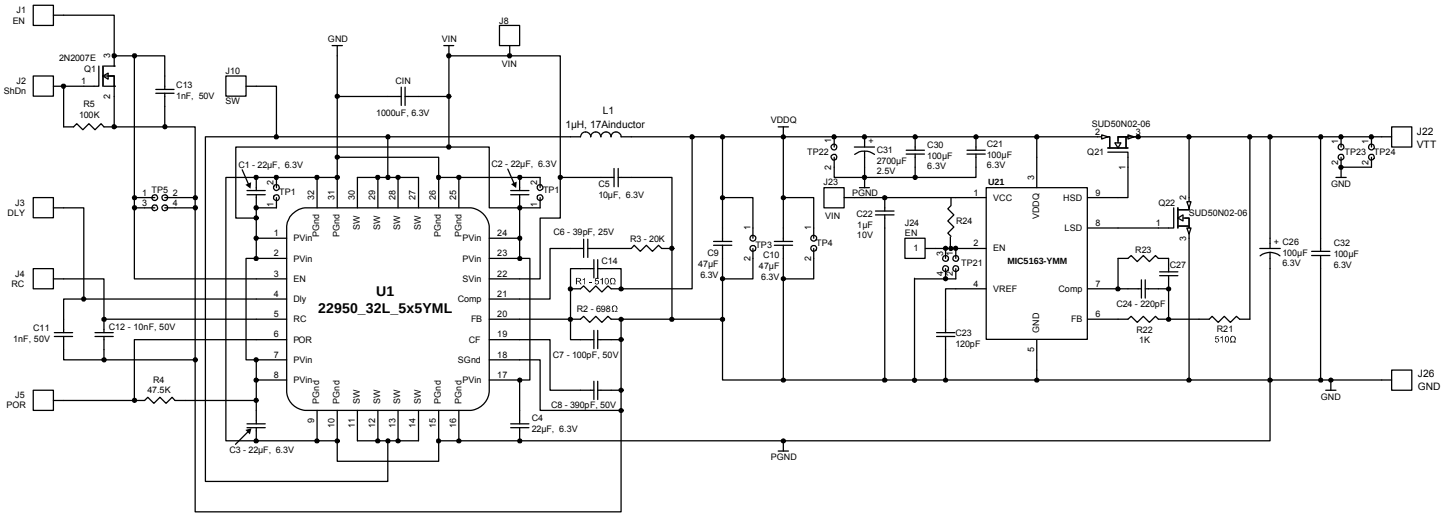
In most cases, case-to-sink thermal resistance can be assumed to be about 0.5°C/W.

The DDR3 termination circuit for our example, using 2 D-pack N-Channel MOSFETs (one high side and one on the low side) will require at least a 43°C/W heat sink per MOSFET. This may be accomplished with an external heat sink or even just the copper area that the MOSFET is soldered to. In some cases, airflow may also be required to reduce thermal resistance.

MOSFET Gate Threshold

N-Channel MOSFETs require an enhancement voltage greater than its source voltage. Typical N-Channel MOSFETs have a gate-source threshold (V_{GS}) of 1.8V and higher. Since the source of the high side N-Channel is connected to V_{TT}, the MIC5163 V_{CC} pin requires a voltage equal to or greater than the V_{GS} voltage. For example, our DDR3 termination circuit has a V_{TT} voltage of 0.75V. For an N-Channel that has a V_{GS} rating of 2.5V, the V_{CC} voltage can be as low as 3.25V. With an N-Channel that has a 4.5V V_{GS}, the minimum V_{CC} required is 5.25V. Although these N-Channels are driven below their full enhancement threshold, it is recommended that the V_{CC} voltage has enough margin to be able to fully enhance the MOSFETs for large signal transient response. In addition, low gate thresholds MOSFETs are recommended to reduce the V_{CC} requirements.

Design Example



MIC5163 As a DDR3 Memory Termination Device for 3.5A Application

Bill of Materials

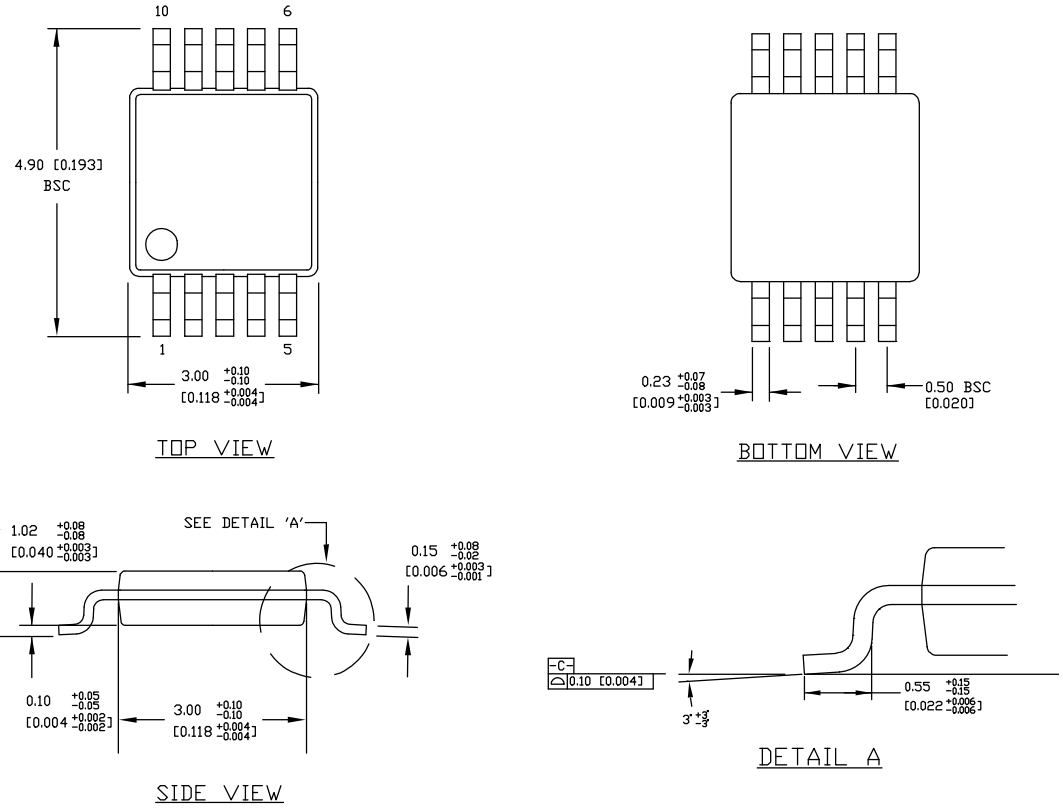
Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C3, C4	GRM21BR60J226ME39L	Murata[1]	22µF, 6.3V, X5R, 0805	4
	C2012X5R0J226K	TDK[2]		or
	08056D226MAT2A	AVX[3]		or
C5	GRM188R60J106ME47D	Murata[1]	10 µF, 6.3V, X5R, 0603	1
	C1608X5R0J106K	TDK[2]		or
	06036D106MAT2A	AVX[3]		or
C6	VJ0603Y390KXXMB	Vishay Vitramon[4]	39pF, 25V, X7R, 0603	1
	C1608C0G1H390J	TDK[2]		or
C7	VJ0603Y101KXAAT	Vishay Vitramon[4]	100pF, 50V, 0603 ceramic cap	1
C8	VJ0603Y391KXAAT	Vishay Vitramon[4]	390pF, 50V, 0603 ceramic cap	1
C9, C10	GRM31CR60J476ME19L	Murata[1]	47 µF,6.3V, 1206	2
	C3216X5R0J476M	TDK[2]		or
	12066D476MAT2A	AVX[3]		or
C11, C13	VJ0603Y102KXXMB	Vishay Vitramon[4]	1nf, 50V, 0603 ceramic cap	2
C12	VJ0603Y103KXXMB	Vishay Vitramon[4]	10nf, 50V, 0603 ceramic cap	1
C22	0603ZD105KAT2A	AVX[3]	1µF, 10V 0603 ceramic cap	1
	GRM188R61A105K	Murata[1]		or
C23	VJ0603A121KXXAT	Vishay[4]	120pF, 25V, 0603 ceramic cap	1
	06033A121JAT2A	AVX[3]		or
C24	VJ0603A221KXXAT	Vishay[4]	220pF, 25V, 0603 ceramic cap	1
	06033C221JAT2A	AVX[3]		or
C26	NOSD107M006R0080	AVX[3]	100µF, 6.3V, 7374 Tent	1
C27			N.U. 0603 ceramic cap	

Item	Part Number	Manufacturer	Description	Qty.
C30, C32, C21	18126D107MAT	AVX[3]	100µF, 6.3V, 1812 ceramic cap	3
C31	2SEPC2700M	Sanyo[5]	2700µF, 2.5V Oscon Cap	1
CIN	597D108X06R3R2T	Vishay[4]	1000µF, 6.3V, R-case	1
L1	CEP125HNP-1R0-MC	Sumida[6]	1µH, 17A inductor	1
Q1	2N7002E(SOT-23)	Vishay[4]	Signal MOSFET-SOT-236	1
Q21, Q22	SUD50N02-06P	Vishay[4]	Low VGS(th) N-Channel 20-V (D-S)	2
R1	CRCW06031101FRT1	Vishay Dale[4]	510Ω (0603 size), 1%	1
R2	CRCW06036980FRT1	Vishay Dale[4]	698Ω (0603 size), 1%	1
R3	CRCW06032002FRT1	Vishay Dale[4]	20K, (0603 size), 1%	1
R4	CRCW06034752FRT1	Vishay Dale[4]	47.5K, (0603 size), 1%	1
R5	CRCW06031003FRT1	Vishay Dale[4]	100K (0603 size), 1%	1
R21	CRCW0805510RFKTA	Vishay Dale[4]	510Ω (0805 size), 1%	1
R22, R24	CRCW06031K00FKTA	Vishay Dale[4]	1K (0603 size), 1%	1
R23			NU 0603	
U1	**MIC22950YML**	**Micrel[7]**	**Buck Regulator**	**1**
U21	**MIC5163YMM**	**Micrel[7]**	**Dual Regulator Controller for DDR3**	**1**

Notes:

1. Murata: www.murata.com.
2. TDK: www.tdk.com.
3. AVX: www.avx.com.
4. Vishay: www.vishay.com.
5. Sanyo: www.sanyo.com
6. Sumida: www.sumida.com
7. **Micrel, Inc**.: www.micrel.com.

Package Information



NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

10-Pin MSOP (MM)

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