ATA8350

Impulse-Radio Ultra-Wideband (IR-UWB) Transceiver Datasheet

Features

- Supports Frequency Ranges in the 6.2 GHz to 7.8 GHz Ultra-Wideband (UWB)
- Uses 3db™ Low-Power Secure Ranging Technology
- Spectrum of Transmission Is Compliant to UWB Regulations of ETSI (EN 302 065-3 V2.1.0) and FCC (Title 47, Part 15)
- UWB Data Communication at 246 Kbps
- Time-of-Flight Distance Measurement with ±15 cm Resolution
- Distance Measurement Method is Secured against Multiple-Attack Scenarios, for example: Cicada Attack, Early Detect/Late Commit, Preamble Injection
- Fast SPI Interface (20 Mbps) for Data Communication and Configuration
- IC Core Voltage 1.25V, I/O Voltage 2.0V to 3.5V
- Low RX and TX Peak Power allows Coin Cell Battery Applications
- Package Details:
    - 33 pins, Thin Profile Fine Pitch Ball Grid Array (TFBGA)
    - Size: 4.5 mm x 4.5 mm
    - Ball pitch: 0.65 mm
    - Ball diameter: 0.4 mm
- Temperature Range: -40°C to +105°C

Performance

- Typical UWB Center Frequencies:
    - Channel A: 6520 MHz
    - Channel B: 7040 MHz
    - Channel C: 7560 MHz
- Typical Link Budget at Ranging Error Rate (RER) = 10%: 88 dB
- Maximum Mean TX Power: -7 dBm
- Typical Power Consumption:
    - RX Average: 39 mA
    - TX Average (Max Output Power): 20 mA
    - READY Mode: 150 µA (including XTAL)
    - OFF Mode: 25 nA (only V_{DD_IO} applied)

General Description

The ATA8350 device is a highly integrated, low-power IR-UWB transceiver, with an integrated security layer for secure distance bounding and data communication between two devices.

Figure 1. ATA8350 Block Diagram
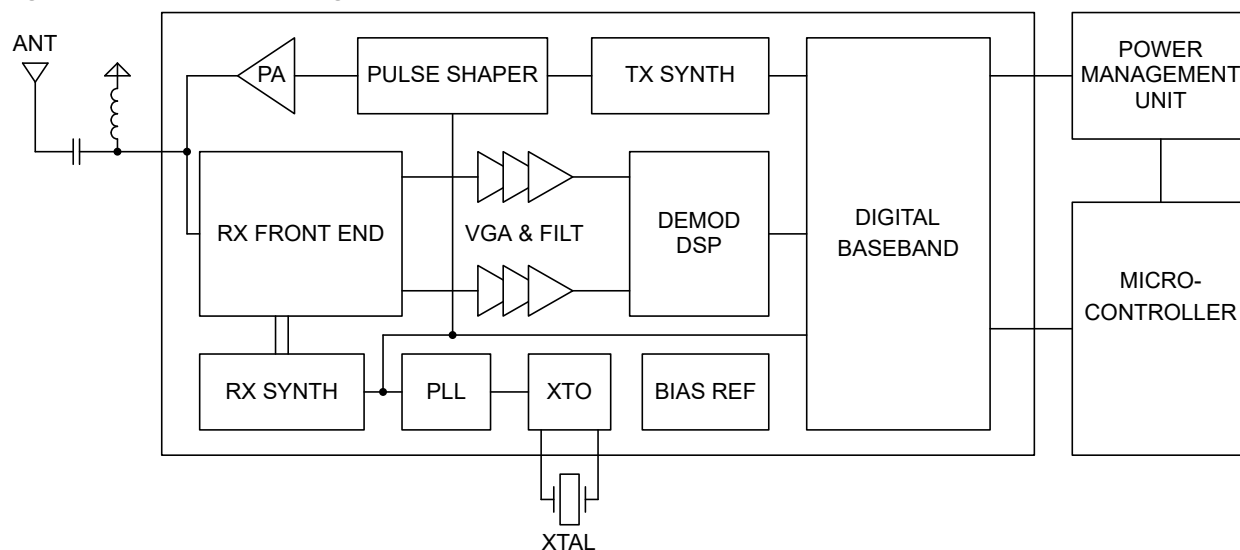
The ATA8350 fully-digital transmitting circuitry ensures maximum flexibility in the generation of UWB pulse signals. The transmitter is able to accurately generate pulse durations ranging from less than 1 ns to more than 10 ns, with a controlled envelope shape and with a carrier frequency from around 6.2 GHz to 7.8 GHz.

Transmitted output power can be programmed up to -7 dBm ensuring that all applications meet ETSI and FCC regulations.

The ATA8350 receiver distinguishes itself by a high-gain and low-power wideband analog radio frequency front end and a high-speed and low-power digital baseband processor.

The receive path consists of a frequency-down conversion circuit comprising low-noise amplifiers (LNA) and mixers, a digitally-controlled variable gain amplifier (VGA) with a digital automatic gain control (AGC), an Analog-to-Digital conversion and a digital baseband signal processing unit for highly stable sub-nanosecond time of arrival estimation (ToA).

The system includes a formally proven purpose-built media access control (MAC) layer for secure distance bounding and data communication for proximity-based access control. The layer can be configured to ensure different degrees of security while providing a sufficient amount of distance measurements to be run in a single secure access control session. This improves distance measurement accuracy by means of averaging over them.

The secure distance-bounding layer was designed to counter both application and physical-layer distance modification attacks. It can operate with any microcontroller that is able to provide cryptographically secure random number generation and authentication routines.

Table of Contents

1. Quick References

1.1 Reference Documentation

For further details, refer to the following:

- *ATA8350 Impulse-Radio Ultra-Wideband (IR-UWB)Transceiver User's Guide*
- *ATA8350 Module Application Note*

1.2 Acronyms and Abbreviations

Table 1-1. Acronyms and Abbreviations

Acronyms/ Abbreviations	Description
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
ANT	Antenna
ATB	Analog Test Bus
BFSK	Binary Frequency Shift Keying
Ch	Channel
CLK	Clock
CTRL	Control
CW	Continuous Wave
DC	Direct Current
DSP	Digital Signal Processing
ESD	Electrostatic Discharge
FE	Front-end
FLL	Frequency Locked Loop
FSK	Frequency Shift Keying
GND	Ground
GPO	General Purpose Output
IC	Integrated Circuit
ID	Identifier
IO, I/O	Input Output
IR	Impulse Radio
IRQ	Interrupt Request
LF	Low Frequency
LNA	Low-Noise Amplifier
LO	Local Oscillator

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Acronyms/ Abbreviations	**Description**
LUT	Look-up Table
MAC	Media Access Control
PA	Power Amplifier
PLL	Phase Locked Loop
PR	Prover
PSD	Power Spectral Density
RAM	Random Access Memory
RER	Ranging Error Rate
RF	Radio Frequency
RX	Receive/Reception
SPI	Serial Peripheral Interface
SRF	Self Resonant Frequency
SSID	Secure Session Identifier
T_AMB	Ambient Temperature
TA	Turnaround
TFBGA	Thin Profile Fine Pitch Ball Grid Array
ToA	Time of Arrival
TX	Transmit/Transmission
UWB	Ultra-Wideband
VGA	Variable Gain Amplifier
VR	Verifier
XTAL	Crystal
XTO	Crystal Oscillator

2. Application Diagram

Figure 2-1 shows a typical application diagram of the ATA8350. The IO voltage between 2.0V and 3.5V may be provided by a standard lithium battery (example: CR2032). The core voltage of 1.25V is generated by a DC/DC converter for optimized overall power consumption.

The ATA8350 is controlled by a host microcontroller via the SPI interface. If required, the host can derive a high precision clock from the 48 MHz crystal of the ATA8350.

Two external components are required for 50Ω antenna matching at the RFIO pin:

- High-Q wounded coil inductor with SRF > 12 GHz (recommended size 0402)
- High-Q capacitor (recommended size 0201)

The reference board gives an example for implementation including the component values to achieve the required matching (refer to the *ATA8350 Module Application Note*).

Figure 2-1. Application Diagram
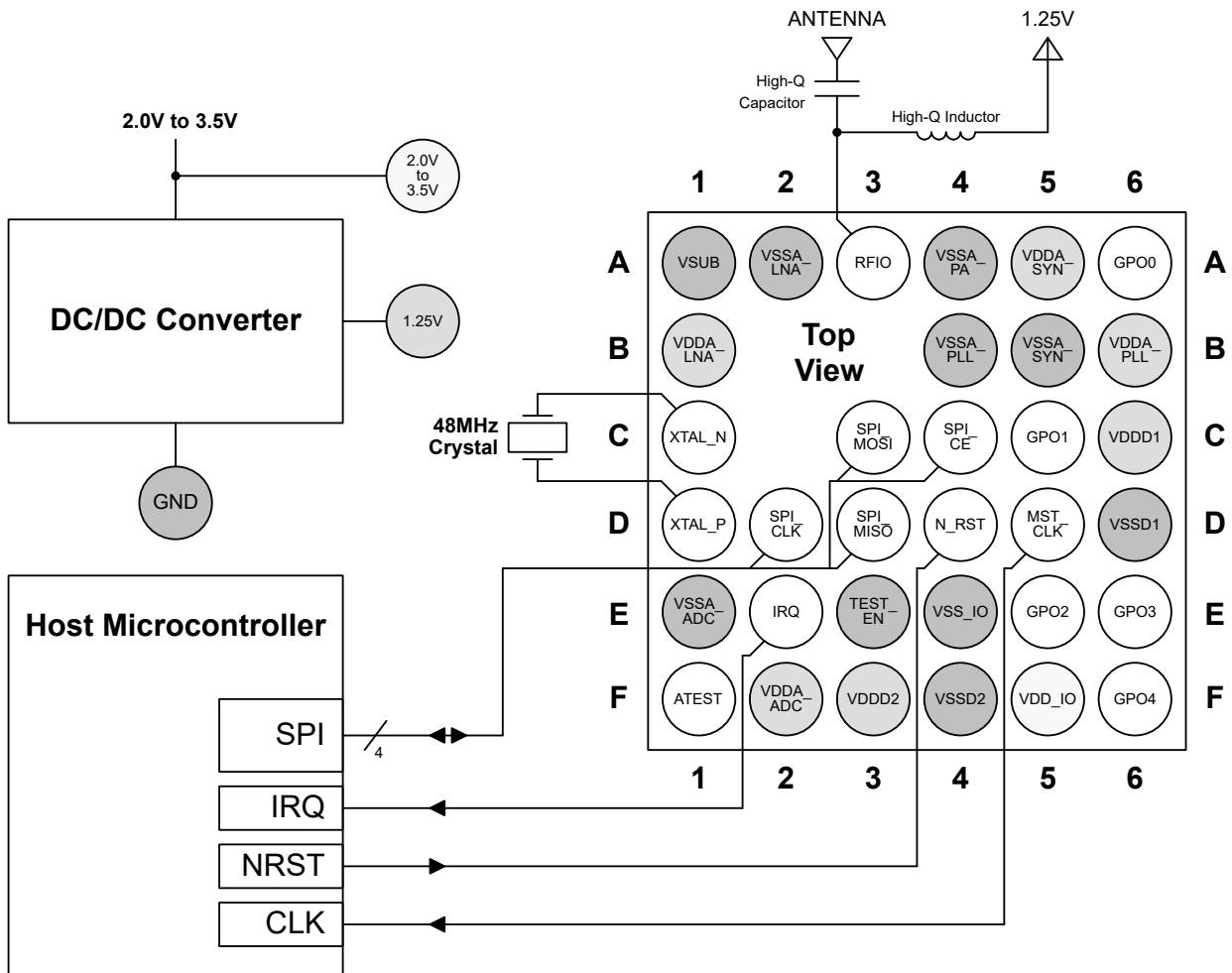
3.   Electrical Characteristics

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 3-1. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Comments
Storage Temperature	T_{STG}	-55	+125	°C	—
Ambient Temperature	T_{AMB}	-40	+105[1]	°C	Operating range
Humidity	—	—	—	—	Fully qualified according to JEDEC JESD22-A110. If the application is exposed to high humidity and the device is permanently powered, it is recommended to apply additional humidity protection
ESD HBM All Pins	HBM	-4	+4	kV	Human Body Model
ESD FCDM All Pins	FCDM	-500	+500	V	Field Induced Charged Device Model
ESD FCDM Corner Pins	FCDM_CORNER	-750	+750	V	Field Induced Charged Device Model
RFIO Pin Maximum Input Power	P_{RFIO_MAX}	—	+15	dBm	CW mode

Note:
1.   Performance degradation is possible between +85°C and +105°C.

All subsequent parameters are based on recommended settings according to 7. Recommended Register Settings. These parameters are valid for T_{AMB} = -40°C to +105°C and V_{DDA} = V_{DDD} = 1.2V to 1.3V over all process tolerances unless otherwise specified. Typical values are given at V_{DDA} = V_{DDD} = 1.25V, T_{AMB} = 25°C and for a typical process unless otherwise specified.

Table 3-2. Supply Voltages and Current Consumption

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Comments
1.00	Analog Supply Voltage	V_{DDA}	1.20	1.25	1.30	V	—
1.10	Digital Core Supply Voltage	V_{DDD}	1.20	1.25	1.30	V	—
1.20	Digital IO Supply Voltage	V_{DD_IO}	2.00	3.30	3.50	V	Functionality guaranteed within specified V_{DDD}
1.30	IO Supply Domain Leakage Current (OFF Mode)[1]	$I_{VDD\_IO\_OFF}$	—	0.025	0.5	µA	V_{DD_IO} = 3.5V V_{DDA} = V_{DDD} = V_{SS}
1.40	Core Domain Leakage Current (IDLE/ READY Mode)	I_{LEAK_IDLE}	—	40	1200	µA	V_{DD_IO} = 3.5V V_{DDA} = V_{DDD} = 1.25V XTAL off
1.50	IDLE Mode Current Consumption	I_{VDD_IDLE}	—	150	1500	µA	XTAL active, sum of all voltage domains
1.60	TX Average Current Consumption	I_{VDD_TX}	—	20	25	mA	Transmitter continuously ON, max TX power setting, core domain
1.65	RX Current Search Mode	$I_{VDD\_RX\_SRCH}$	—	39	50	mA	Receiver searching for a signal and preamble, core domain
1.70	RX Current Locked Mode	$I_{VDD\_RX\_LCK}$	—	34	45	mA	Receiver has locked on signal, core domain

Note:
1.   Characterized on samples

Table 3-3. Crystal Oscillator and Clock

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Comments
2.00	Crystal Frequency	F_{XTAL}	—	48	—	MHz	—
2.10	Crystal Parameter Requirements	ESR_{XTAL48}	—	—	60	Ω	Equivalent series resistance
2.20	(48 MHz)	CL_{XTAL48}	5	6	7	pF	Nominal load capacitance
2.30		$C0_{XTAL48}$	—	—	2	pF	Shunt capacitance
2.40		OSF_{XTAL48}	10	—	—	—	Oscillation safety factor, C0_IN < 1pF, at 25degC
2.90	Crystal Frequency Tolerance Requirements (to achieve specified sensitivity and security)	DF_{XTAL_INIT}	-2	—	+2	ppm	Initially at +25°C (after on-chip trimming)
3.00		DF_{XTAL_TEMP}	-16	—	+16	ppm	Over temperature range
3.10		DF_{XTAL_AGING}	-5	—	+5	ppm	Aging after 10 years
3.30	On-Chip C_L Trim	CL_{TRIM_RANGE}	-15%	7.63	+15%	pF	Trimming via internal 8-bit capacitor array
3.40		CL_{TRIM_STEP}	-15%	41	+15%	fF	Differential, average step size over range
3.60	Digital Clock Output	F_{MCLK}	4	—	8	MHz	Derived from XTAL. Possible configurations: 4 MHz and 8 MHz
3.80	Digital Clock Output Duty Cycle	DC_{MCLK}	33	50	66	%	—
3.90	XTO Settling Time	T_{XTAL}	—	—	2	ms	—
4.00	External Clock Input	V_{IN_XTAL}	0.8	—	1.32	V	Single-ended square wave input on xtal_p, xtal_n grounded
4.10		PN_{IN_XTAL}	—	-138	-135	dBc/Hz	Phase noise at 1 MHz
4.20		DC_{IN_XTAL}	40	50	60	%	Duty cycle

Table 3-4. Transmitter

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Comments
5.00	TX Frequency Operating Range	BW_{TX}	6.2	—	7.8	GHz	—
5.10	Pulse Peak Voltage[1]	V_{TX_PEAK}	1.5	1.8	2.1	Vpp	At maximum TX power setting
5.20	Average TX RF Power	P_{TX_AVG}	-9.5	-7	-2	dBm	Continuous, modulated transmission at maximum TX power setting
5.30	Peak TX Power	P_{TX_PEAK}	6.5	9	14	dBm	Maximum TX power setting
5.40	TX Output Power Step	DP_{TX}	—	1.2	—	dB	Average step size (13 steps)
5.50	Pulse Bandwidth	BW_{PULSE}	200	270	350	MHz	-10 dB bandwidth, related to configured pulse shape
5.60	Composite Bandwidth	BW_{COMP}	450	540	650	MHz	-10 dB bandwidth of FSK modulated signal
5.70	UWB Pulse Rate	PR	—	3.938	—	Mpulse/s	Instantaneous pulse rate
5.90	Modulation Offset	F_DEV	—	135	—	MHz	FSK deviation (+/-) from RF center frequency
6.00	RF Frequency Accuracy	RF	—	—	1	%	—
6.10	Recommended Frequency Channel A	F_{CHA}	—	6520	—	MHz	Center frequency Ch A
6.11	Recommended Frequency Channel B	F_{CHB}	—	7040	—	MHz	Center frequency Ch B
6.12	Recommended Frequency Channel C	F_{CHC}	—	7560	—	MHz	Center frequency Ch C
6.20	Out of band Signal Level[1]	L_{OOB_UWB}	—	—	-28	dB	Below 6 GHz and above 8.5 GHz, according to frequency plan in parameter 6.10, related to peak PSD, excluding harmonics.
6.30	2nd Harmonic Suppression[1]	$SUPP_2$	—	-24	—	dB	Continuous mode, related to peak PSD

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No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Comments
6.40	3rd Harmonic Suppression[1]	$SUPP_3$	—	-25	—	dB	Continuous mode, related to peak PSD

Note:
1. Characterized on samples

Table 3-5. Receiver

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Comments
7.00	Rx Frequency Operating Range	BW_{RX}	6.2	—	7.8	GHz	—
7.10	RF Input Reflection Coefficient	S_11	—	—	-8	dB	50 Ohm matching requirement
7.20	Maximum Usable Average Input Power	P_{RX_MAX}	—	-10	—	dBm	For valid ranging measurement
7.50	Rx Sensitivity Channel A and Channel B, T_AMB < 85°C[1]	$SENS_{CHAB\_85}$	—	-95	-91.5	dBm	BER 0.1%, TX from signal generator, conducted measurement on reference board, related to average RF power
7.51	Rx Sensitivity Channel A and Channel B T_AMB < 105°C[1]	$SENS_{CHAB\_105}$	—	—	-89	dBm	BER 0.1%, TX from signal generator, conducted measurement on reference board, related to average RF power
7.55	Rx Sensitivity Channel C, T_AMB < 85°C[1]	$SENS_{CHC\_85}$	—	-94	-90	dBm	BER 0.1%, TX from signal generator, conducted measurement on reference board, related to average RF power
7.56	Rx Sensitivity Channel C a, T_AMB < 105°C[1]	$SENS_{CHC\_105}$	—	—	-87	dBm	BER 0.1%, TX from signal generator, conducted measurement on reference board, related to average RF power

Note:
1. Characterized on samples

Table 3-6. Communication System

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Comments
8.00	Data Rate	SYS_{DR}	—	246	—	kB/s	—
8.20	Link Budget[1]	LB	—	88	—	dB	10% Ranging Error Rate on reference boards, conducted mode, signal generated by another ATA8350 with max output power
8.55	ADC Sampling Rate	F_{ADC}	—	1008	—	MHz	—
8.60	ToA Time Resolution	TOA_{RES}	—	992	—	ps	Related to ADC sampling rate
8.70	ToA Precision without Offset Correction	$TOA\_PREC_{WO\_OC}$	-1	—	1	ADC samples	3-sigma value for single ranging measurement. Accuracy depends on crystal offset between Verifier and Prover
8.80	ToA Precision With Offset Correction	$TOA\_PREC_{WI\_OC}$	-3	—	3	ADC samples	3-sigma value for single ranging measurement. Full accuracy, crystal offset between Verifier and Prover is corrected
8.90	SPI Speed	DR_{SPI}	—	—	20	Mbps	—

Note:
1. Characterized on samples

Table 3-7. Digital I/O Pin Characteristics

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Comments
9.00	Input low voltage	V_{IL}	-0.2	—	$0.3*V_{DD\_IO}$	V	SPI_MOSI, SPI_CE, SPI_CLK, N_RST, TEST_EN
9.10	Input high voltage	V_{IH}	$0.7*V_{DD\_IO}$	—	$V_{DD\_IO}+0.2$	V	SPI_MOSI, SPI_CE, SPI_CLK, N_RST, TEST_EN

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No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Comments
9.20	Input low level leakage current per pin	I_{IL}	—	—	10	uA	SPI_MOSI, SPI_CE, SPI_CLK, N_RST, TEST_EN, pull-down disabled, current flowing into pin
9.30	Input high level leakage current per pin	I_{IH}	—	—	10	uA	SPI_MOSI, SPI_CE, SPI_CLK, N_RST, pull-down disabled, current flowing out of pin
9.40	Output low voltage	V_{OL}	—	—	0.4	V	SPI_MISO, MST_CLK, IRQ, GPO[4:0], I_{OL} = 2mA
9.50	Output high voltage	V_{OH}	V_{DD_IO}-0.5	—	—	V	SPI_MISO, MST_CLK, IRQ, GPO[4:0], I_{OH} = -2mA
9.60	Internal pull-down resistor	R_{PD}	25	40	80	kOhm	SPI_MOSI, SPI_CE, SPI_CLK, N_RST, TEST_EN
Timing characteristics of the SPI interface can be found in the ATA8350 user guide.							

4. Pin Description

4.1 Pin Diagram and Pin Functions

Figure 4-1. Pin Diagram TFBGA33
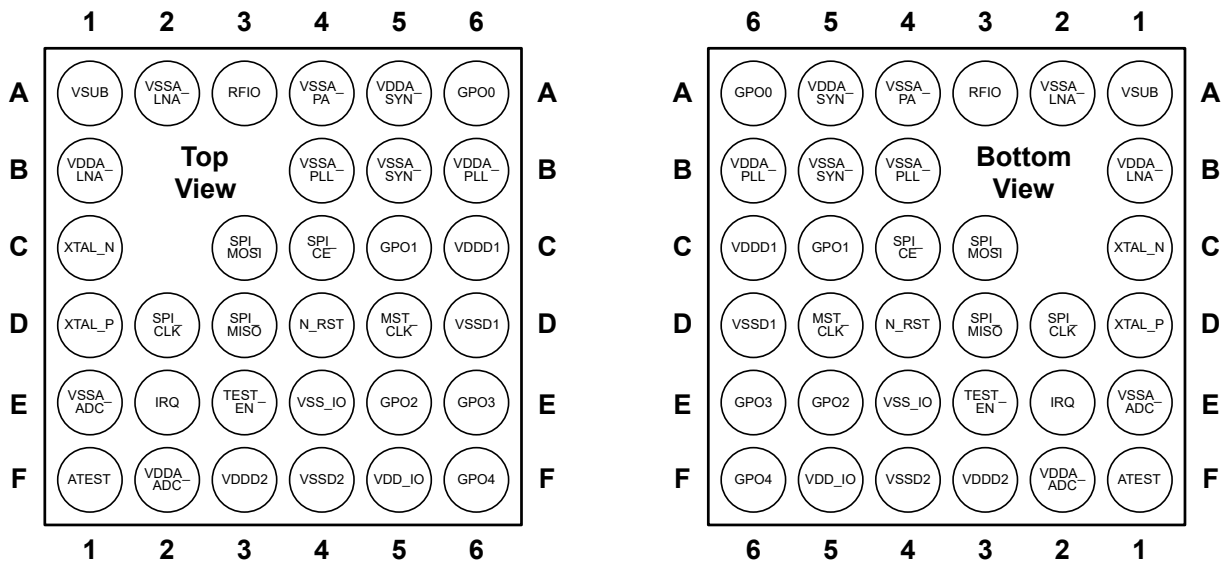
Pin Number	Pin Name	Type	Function	Voltage Domain
A1	VSUB	Analog	GND	VBAT 3.3V
A2	VSSA_LNA	Analog	GND	VCore 1.25V
A3	RFIO	Analog	RF Antenna Pin	VCore 1.25V
A4	VSSA_PA	Analog	GND	VCore 1.25V
A5	VDDA_SYN	Analog	Core Supply 1.25V	VCore 1.25V
A6	GPO0	Digital	General Purpose Output 0 (Debug / Test)	VBAT 3.3V
B1	VDDA_LNA	Analog	Core Supply 1.25V	VCore 1.25V
B4	VSSA_PLL	Analog	GND	VCore 1.25V
B5	VSSA_SYN	Analog	GND	VCore 1.25V
B6	VDDA_PLL	Analog	Core Supply 1.25V	VCore 1.25V
C1	XTAL_N	Analog	48 MHz Crystal Oscillator Negative Port, Gate Contact	—
C3	SPI_MOSI	Digital	SPI Master Out Slave In	VBAT 3.3V
C4	SPI_CE	Digital	SPI Chip Select (Active High)	VBAT 3.3V
C5	GPO1	Digital	General Purpose Output 1 (Debug / Test)	VBAT 3.3V
C6	VDDD1	Digital	Core Supply 1.25V	VCore 1.25V
D1	XTAL_P	Analog	48 MHz Crystal Oscillator Positive Port, Drain Contact	—
D2	SPI_CLK	Digital	SPI Clock Input	VBAT 3.3V
D3	SPI_MISO	Digital	SPI Master In Slave Out	VBAT 3.3V

Pin Number	Pin Name	Type	Function	Voltage Domain
..........continued				
D4	N_RST	Digital	Chip Reset (Active Low)	VBAT 3.3V
D5	MST_CLK	Digital	Master Clock Output (4 MHz)	VBAT 3.3V
D6	VSSD1	Digital	GND	VCore 1.25V
E1	VSSA_ADC	Analog	GND	VCore 1.25V
E2	IRQ	Digital	Interrupt Request Output	VBAT 3.3V
E3	TEST_EN	Digital	Test Mode Enable (Active High) - Connect to GND in Application	VBAT 3.3V
E4	VSS_IO	Digital	GND	VBAT 3.3V
E5	GPO2	Digital	General Purpose Output 2 (Debug / Test)	VBAT 3.3V
E6	GPO3	Digital	General Purpose Output 3 (Debug / Test)	VBAT 3.3V
F1	ATEST	Analog	Analog Test - Open in Application	VCore 1.25V
F2	VDDA_ADC	Analog	Core Supply 1.25V	VCore 1.25V
F3	VDDD2	Digital	Core Supply 1.25V	VCore 1.25V
F4	VSSD2	Digital	GND	VCore 1.25V
F5	VDD_IO	Digital	I/O Power Supply 3.3V	VBAT 3.3V
F6	GPO4	Digital	General Purpose Output 4 (Debug / Test)	VBAT 3.3V

4.2 Digital Pin States

The state of the digital output pins depends on the supply voltages and the state of the control signals SPI_CE and N_RST. Table 4-1 and Table 4-2 give an overview on the corresponding states.

Table 4-1. Pin States when V_{DD_IO} = 3.3V and V_{DD_CORE} = 0V

N_RST	SPI_CE	GPO[4..0]	SPI_MISO	IRQ	MST_CLK
INPUT		OUTPUT			
X	X	Z	Z	Z	Z

Table 4-2. Pin States when V_{DD_IO} = 3.3V and V_{DD_CORE} = 1.25V

N_RST	SPI_CE	GPO[4..0]	SPI_MISO	IRQ	MST_CLK
INPUT		OUTPUT			
L	X	L	Z	L	L
H	L	X	Z	X	X
H	H	X	X	X	X

with

- Z = High Impedance state
- X = Undefined state
- L = Low state
- H = High state

5.   Functional Description

5.1   Power Supply

The ATA8350 is supplied by two separate voltages:

- V_{DD_CORE} = 1.25V for the main core circuitry (comprising V_{DDA} and V_{DDD})
- V_{DD_IO} = 2.0V to 3.5V for I/Os

The subsequent procedure is followed when applying or removing the supply voltage.

- **POWER-ON sequence**: V_{DD_IO} must be applied first. V_{DD_CORE} can be applied once V_{DD_IO} is reached. If V_{DD_CORE} is powered-up before V_{DD_IO}, the I/O ring could be set to an unknown state, resulting in high I/O currents in the crowbar circuit. When V_{DD_CORE} is stable, the N_RST pin can be set to 1.
- **POWER-DOWN sequence**: Before the IC is powered-down, all internal blocks must be disabled and the signals that are controlled by the microcontroller must be reset (SPI lines and N_RST). After a delay of 100 μs the N_RST signal (if enabled) and V_{DD_CORE} can be set to ground. Once the core supply reaches 0V, V_{DD_IO} can be switched off.

5.2   SPI Interface

The ATA8350 device must be controlled by an external microcontroller using the following interface:

1.   An active-low N_RST input pin to reset the device
2.   An SPI communication link (SPI_MISO, SPI_MOSI, SPI_CLK and SPI_CE) with a baud rate up to 20 Mbps
3.   An IRQ output pin to trigger an event processed by the external host controller.

All other I/O signals are not required for device control.

The SPI telegrams have the following general bit and byte structure:

Access	Address					Data	Data	Data	Data	…	Data	Data
0: Write 1: Read	a4	a3	a2	a1	a0	—	—	—	—	…	—	—
Byte 1							Byte 2	Byte 3	…	Byte N-1	Byte N

The upper six bits of the first byte define the type of operation (read/write) and a 5-bit register address. The remaining two bits and the following data bytes are assigned to parameters within the corresponding register.

SPI operation is possible as soon as V_{DD_IO} and V_{DD_CORE} are stable. An internal clock is not required; the SPI is completely run by SPI_CLK.

5.3   Operating Modes

5.3.1   Operating Modes Overview

This section gives an overview of the operating modes that are implemented in the ATA8350. Figure 5-1 shows the available modes and the transitions between the modes.

Figure 5-1. Operating Modes Overview
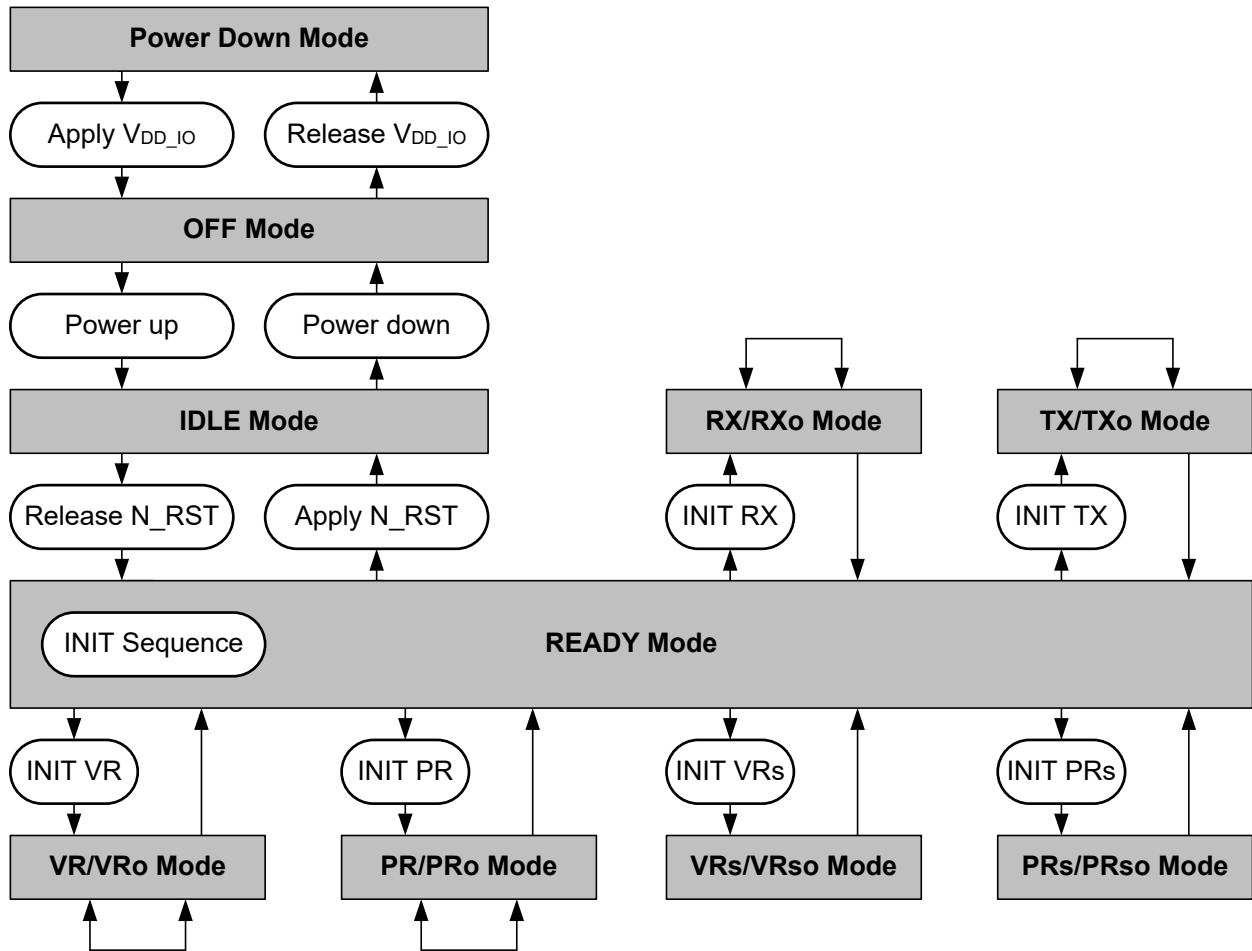
5.3.2 POWER-DOWN Mode

In Power-Down mode, no supply voltage is applied to the device, i.e., both, V_{DD_IO} and V_{DD_CORE} are switched off.

5.3.3 OFF Mode

The device is in OFF mode when V_{DD_IO} is applied but V_{DD_CORE} is connected to ground. The OFF mode is useful when the chip is inactive but the GPIO pins are required to be in a high-Z state; for example, for multi-slave SPI operation. Power consumption is reduced to the minimum.

5.3.4 IDLE Mode

In IDLE mode, both supply voltages are applied to the device. A predefined sequence must be followed to securely power-up the system.

In IDLE mode, the N_RST pin can be raised at any time to proceed to READY mode.

5.3.5 READY mode

The READY mode is entered when the chip is powered-up and the N_RST signal is raised. Initially, the system provides only access to the SPI interface. All other blocks are switched off.

Before using any of the receive or transmit modes, the INIT sequence has to be executed, which switches on and calibrates the crystal oscillator, the PLL and the FLLs.

5.3.6 Receive Mode RX

In RX mode, the device can receive data from another device programmed in TX mode.

To enter the RX mode, the device has to be configured accordingly by a sequence of SPI commands. Once programmed, the chip starts listening for a configured number of packets from a transmitting device. The information regarding the received packets is stored in the data part of the RAM.

The IC automatically switches back to READY mode when the expected number of packets are received.

5.3.7 Transmit Mode TX

In TX mode, the device can transmit data to another device programmed in RX mode.

To enter the TX mode, the device has to be configured accordingly by a sequence of SPI commands, and the TX data must be written to the data section of the RAM. Once programmed, the chip starts transmitting the configured number of packets. The IC automatically switches back to READY mode after the data are sent.

5.3.8 Distance-Bounding Modes

In the distance-bounding modes, two devices are automatically exchanging data telegrams to determine the minimum distance between them by a time-of-flight measurement. One device, the verifier, initiates the measurement and the second device, the prover, responds to this data telegram.

The distance-bounding measurement can be performed in two modes:
- Normal mode VR / PR
- Secure mode VRs / PRs

The Secure mode offers additional security by applying a pseudo-random scrambling scheme on the data symbols of each bit.

5.3.9 Modes with Frequency Offset Compensation

The device offers special modes with frequency offset compensation for the RX, TX and all distance-bounding modes. These modes are marked with a small "o": RXo, TXo, VRo, PRo, VRso and PRso mode.

Data packets in the "o"-modes contain a postamble that allows an automatic offset calculation between the frequency of the quartz oscillators in the transmitting and receiving device. Frequency offset compensation is required to gain an accurate absolute distance result between the devices. Averaging between multiple measurements is recommended to increase overall accuracy.

6. Packet, Challenge and Response Structure

All the communication packets exchanged between transmitting and receiving devices contain a preamble and a synchronization word field. The preamble is needed to achieve pulse-synchronization between the communicating devices and to calculate the time of arrival with high precision. The synchronization word is needed to achieve packet-synchronization between the communicating devices. Only upon successful packet-synchronization is it possible to correctly decode the data contained in a packet.

In the modes that provide frequency offset compensation, an additional postamble is attached to the packet.

Figure 6-1 shows the packet structure for the standard data transmission between two devices.

Figure 6-1. Data Packet Structure

Preamble	**Sync**	**Data Payload**	**Postamble**
(224 Pulses)	(127 Ps)	(#bits*16 Pulses)	(160 Pulses)

Figure 6-2 shows the structure of a typical packet that is exchanged by two devices in a distance-bounding mode. The preamble and sync word are identical to a standard data packet. Afterward, an identifier (SSID) and the random data (RNR) are exchanged, followed by an optional postamble for frequency offset compensation and the fixed turnaround time to switch the transmitter and receiver roles.

Figure 6-2. Distance-Bounding Packet Structure

Preamble	**Sync**	**SSID**	**RNR**	**Postamble**	**T A**
(224 Pulses)	(127 Ps)	(512 Pulses)	(512/768/1024 Pulses)	(160 Pulses)	

7. Recommended Register Settings

The following table describes the recommended register settings for a typical application. They differ from the default settings after reset and must be written to the device via SPI.

Table 7-1. Recommended and Default Register Settings

Register	Recommended Settings	Default Settings
A0 - Bias	0x01 0xDC 0x26 0x2A 0x1B	0x02 0x1C 0x1E 0x2A 0x1B
A1 - Bias2	0x07 0x2A 0x22 0x22 0x00	0x07 0x15 0x99 0x9A 0x20
A2 - Enable	NA	0x0A 0x00 0x00 0x00 0x00 0x00
A3 - Crystal	0x0C 0x03 0xE0 0x18 0x68 0x20	0x0C 0x03 0x28 0x18 0x68 0x00
A4 - PLL	0x10 0x2C 0xFC 0x40 0x18 0x32	0x12 0x30 0xFC 0x40 0x18 0x22
A5 - FLL RX Write	Ch A: 0x14 0xDF 0x15 0xDC 0x40 Ch B: 0x15 0x00 0x15 0xDC 0x40 Ch C: 0x15 0x21 0x15 x0DC 0x40	0x14 0xDE 0x21 0xEF 0x30
A6 - FLL RX Read	NA	NA
A7 - RX FE	NA	0x1E 0x60
A8 - VGA	NA	0x21 0x9B 0xC0
A9 - AGC	0x25 0x3E 0x15 0x40 0x05 0x40	0x26 0x01 0x06 0x08 0x02 0xC0
A10 - ADC	NA	0x28 0x80 0x00
A11 - Demod	0x2F 0x3B 0x80	0x2C 0x4C 0x88
A12 - FLL TX Write	Ch A: 0x30 0x68 0x11 0x17 0x9B 0x08 0xCA Ch B: 0x30 0x70 0x51 0x17 0x9B 0x08 0xCA Ch C: 0x30 0x78 0x91 0x17 0x9B 0x08 0xCA	0x 32 0x67 0x91 0x17 0x9B 0xC8 0xCA
A13 - BFSK	NA	0x36 0x44 0x44
A14 - TX PA	0x3B 0xF1	0x3B 0xD1
A15 - Pulse Shape	NA	0x3E 0xE5 0xDD 0x50 0xC8
A16 - Pulse Shape2	NA	0x42 0xE5 0xDD 0x50 0xC8
A17 - FLL TX Read	NA	NA
A18 - Data	NA	NA
A19 - Digital	0x4F 0x28 0x1F 0xC0 0xE8	0x4F 0x08 0x01 0xC0 0x00
A20 - ID	NA	NA
A21 - GPO	NA	0x56 0x00 0x02 0x80 0x00 0x04 0x00
A22 - Version	NA	0xD8 0x10
A23 - IRQ	NA	0x5F 0x80

Register	Recommended Settings	Default Settings
..........continued		
A24 - AGC LUT	0x79, 0x5E, 0x67, 0x9D, 0xE8, 0x7A, 0x5E, 0xA7, 0xAC, 0xEB, 0x3B, 0x0E, 0xD3, 0x30, 0xCD, 0x33, 0x84, 0xE1, 0x3C, 0x50, 0x04, 0x01, 0x10, 0x48, 0x13, 0x05, 0x01, 0x50, 0x58, 0x17, 0x06, 0x01, 0x90, 0x68, 0x1B, 0x07, 0x01, 0xD0, 0x78, 0x1F	0x78, 0x1E, 0x17, 0x89, 0xE3, 0x79, 0x1E, 0x57, 0x99, 0xE7, 0x7A, 0x1E, 0x95, 0x9D, 0x68, 0x5A, 0x56, 0xA5, 0xAC, 0x69, 0x1A, 0x86, 0xB1, 0xB0, 0x6D, 0x12, 0xC4, 0xC1, 0x34, 0x4E, 0x13, 0xC5, 0x01, 0x44, 0x52, 0x14, 0xC5, 0x41, 0x54, 0x56
A25 - ATB	NA	0x64 0x00 0x00
A26 - PAD	NA	0x68 0x00 0x00 0x00 0xFC 0x7F 0xC0
A27 - Secure Mode	NA	ID=0: 0x6C, 0x2F, 0x00, 0x10, 0x83, 0x10, 0x51, 0x87, 0x20, 0x92, 0x8B, 0x30, 0xD3, 0x8F, 0x41, 0x14, 0x93, 0x51, 0x55, 0x97, 0x61, 0x96, 0x9B, 0x71, 0xD7, 0x9F, 0x82, 0x18, 0xA3, 0x92, 0x59, 0xA7, 0xA2, 0x9A, 0xAB, 0xB2, 0xDB, 0xAF, 0xC3, 0x1C, 0xB3, 0xD3, 0x5D, 0xB7, 0xE3, 0x9E, 0xBB, 0xF3, 0xDF, 0xBF ID=1: 0x6D, 0x13, 0x2F, 0x6A, 0x51, 0x42, 0x14, 0x5E, 0x5E, 0x38, 0x75, 0x6B, 0xAE, 0x95, 0x7B, 0x2E, 0xA3, 0x54, 0xDC, 0x73, 0xE3, 0x0B
A28 - FLL CAL	NA	0x70 0x77
NA: Not applicable, e.g., for status registers or if recommended settings are identical to default settings		

8. Asset Localization Application

The asset localization application uses the ATA8350 device. The coordinator starts a distance measurement by triggering an LF signal or a UHF communication. See the following figure for an asset localization application example. It can also support more than one anchor node, if needed.

Figure 8-1. Asset Localisation Application
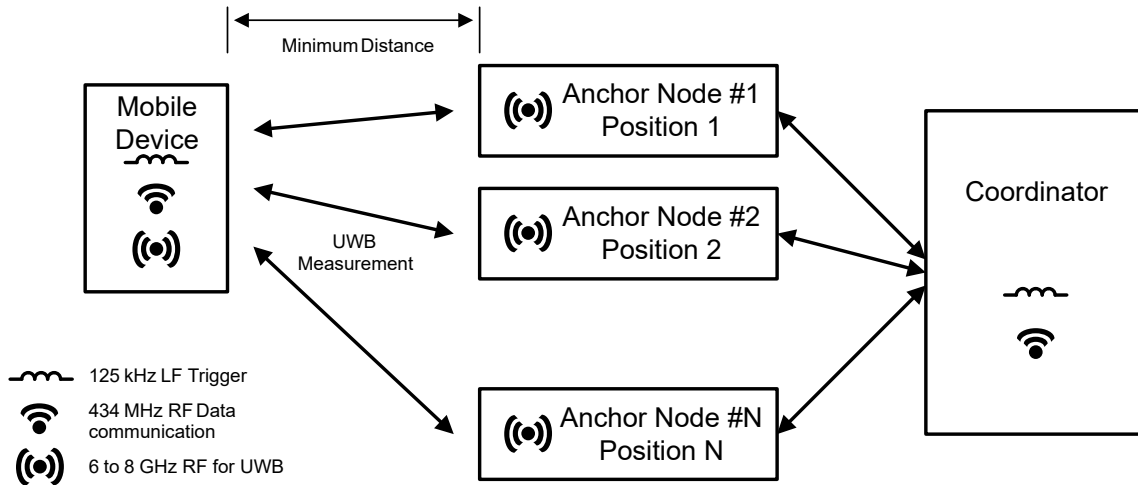
9. Ordering Information

Extended Type Number	Package	Remarks
ATA8350-7MQW	TFBGA	33-Ball Thin Fine Pitch Ball Grid Array (4YB) – 4.5 x 4.5 mm Body

10. Package Drawing

This section details the package marking information and package outline drawings.

10.1 Package Marking Information

The following figure shows the package marking information of the ATA8350.

Figure 10-1. 33-Lead TFBGA (4.5 x 4.5x 1.1 mm)

Legend:

- YY: Year code (the last two digits of the calendar year)
- WW: Week code (for example, the week of January 1 is week '01')
- NNN: Alphanumeric traceability code

10.2 Package Outline Drawing

Note: For the most current package drawings, see the Microchip Packaging Specifications located at www.microchip.com/packaging.

TOP VIEW

BOTTOM VIEW

SIDE VIEW

SEATING PLANE
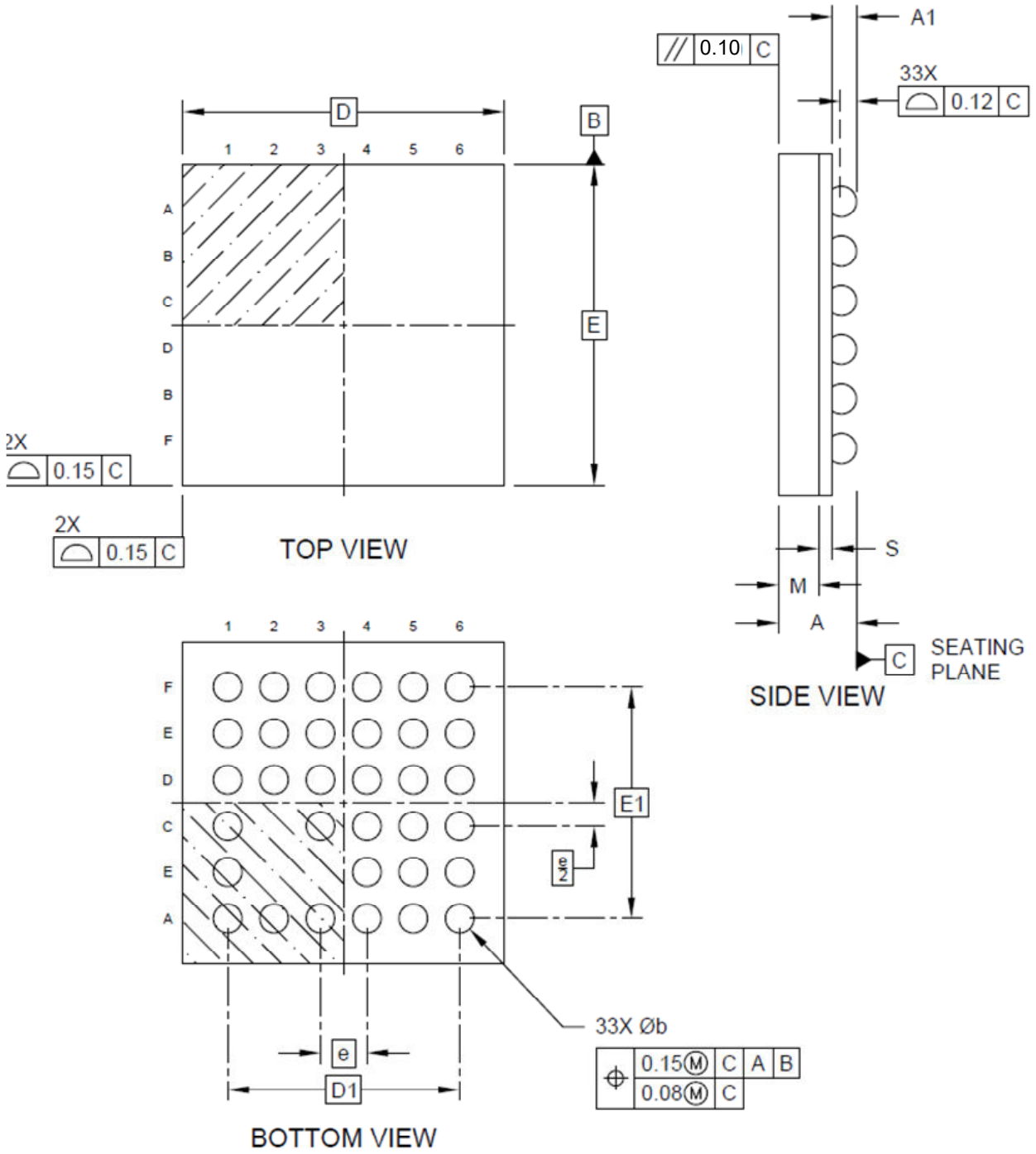
Microchip Technology Drawing C04-21460 Rev A Sheet 1 of 2
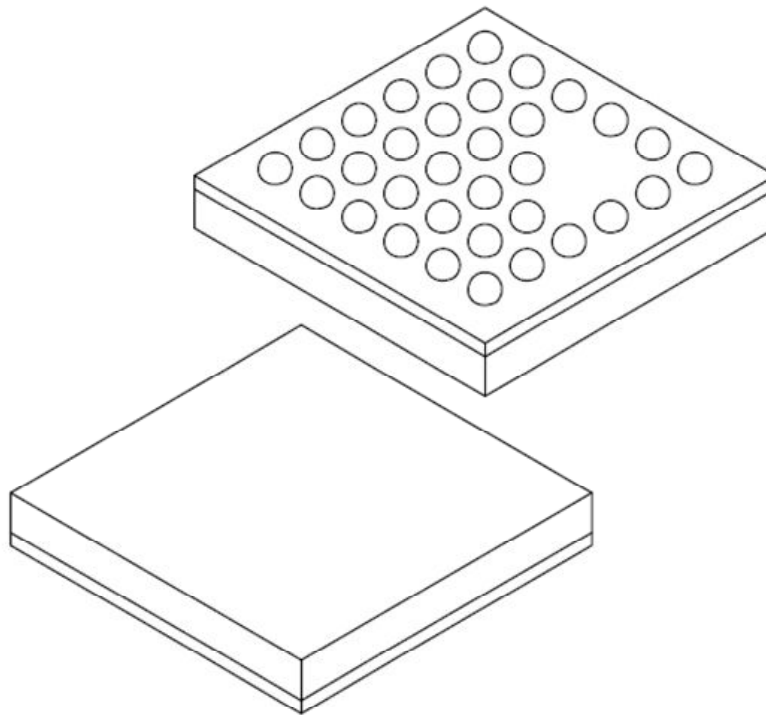
	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		33	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Standoff	A1	0.27	-	0.37
Mold Capl Thickness	M		0.530 REF	
Substrate Thickness	S		0.176 REF	
Overall Length	D		4.50 BSC	
Overall Terminal Pitch	D1		3.25 BSC	
Overall Width	E		4.50 BSC	
Overall Terminal Pitch	E1		3.25 BSC	
Ball Diameter	b	0.37	-	0.47

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

33-Ball Thin Fine Pitch Ball Grid Array (4YB) - 4.5x4.5 mm Body [TFBGA]
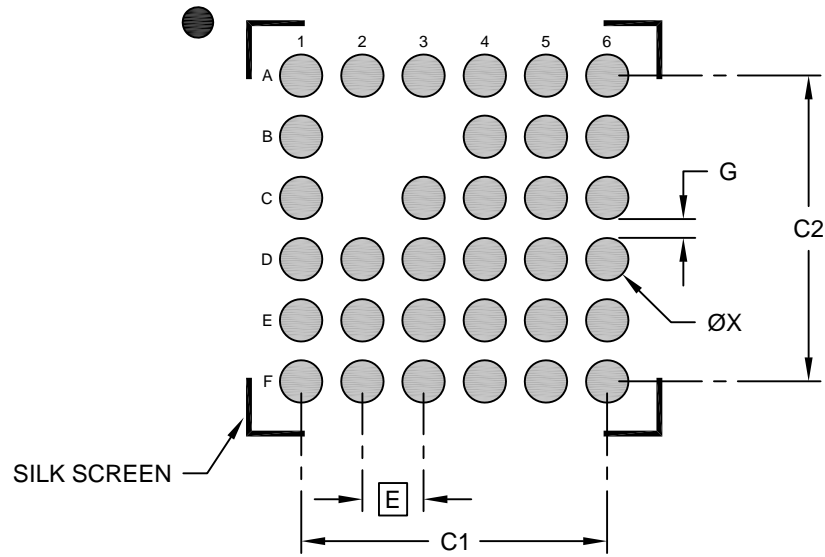
RECOMMENDED LAND PATTERN

	Units		MILLIMETERS		
	Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC		
Contact Pad Spacing	C1			3.30	
Contact Pad Spacing	C2			3.30	
Contact Pad Diameter (X33)	X		0.25	0.30	0.35
Contact Pad to Contact Pad	G		0.30		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
     BSC: Basic Dimension. Theoretically exact value shown without tolerances.

11. Document Revision History

Revision	Date	Section	Description
A	02/2021	Document	Initial Revision

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