MICROCHIP

ATA8352

ATA8352 Impulse-Radio Ultra-Wideband (IR-UWB) Transceiver Data Sheet

Features

- Supports Frequency Ranges in the 6.2 GHz to 8.3 GHz Ultra-Wideband (UWB)
- Uses 3db™ Low-Power Secure Ranging Technology
- Spectrum of Transmission Is Compliant to UWB Regulations of ETSI (EN 302 065-3 V2.1.0) and FCC (Title 47, Part 15)
- UWB Data Communication up to 1 Mbps
- Single Distance Measurement with 4 cm Resolution
- Distance Measurement Method Is Secured against Multiple-Attack Scenarios, For Example, Cicada Attack, Early Detect/Late Commit, Preamble Injection
- Supports Time-Difference-of-Arrival (TDoA) applications with timestamp capturing during TX and RX
- Tailored for industrial and home appliance applications for localization and secure distance bounding
- Fast SPI Interface (24 MHz) for Communication between the ATA8352 and a Host Microcontroller
- RX and TX Peak Power Allows Coin Cell Battery Applications with an External DC-DC Converter
- Operating Conditions:
  - IC core voltage is 1.25V
  - I/O voltage range is 2.0V to 3.5V
  - Temperature range is -40°C to +105°C
- Package Details:
  - 33 pins, Thin Profile Fine Pitch Ball Grid Array (TFBGA)
  - Size: 4.5 mm x 4.5 mm
  - Ball pitch: 0.65 mm
  - Ball diameter: 0.4 mm

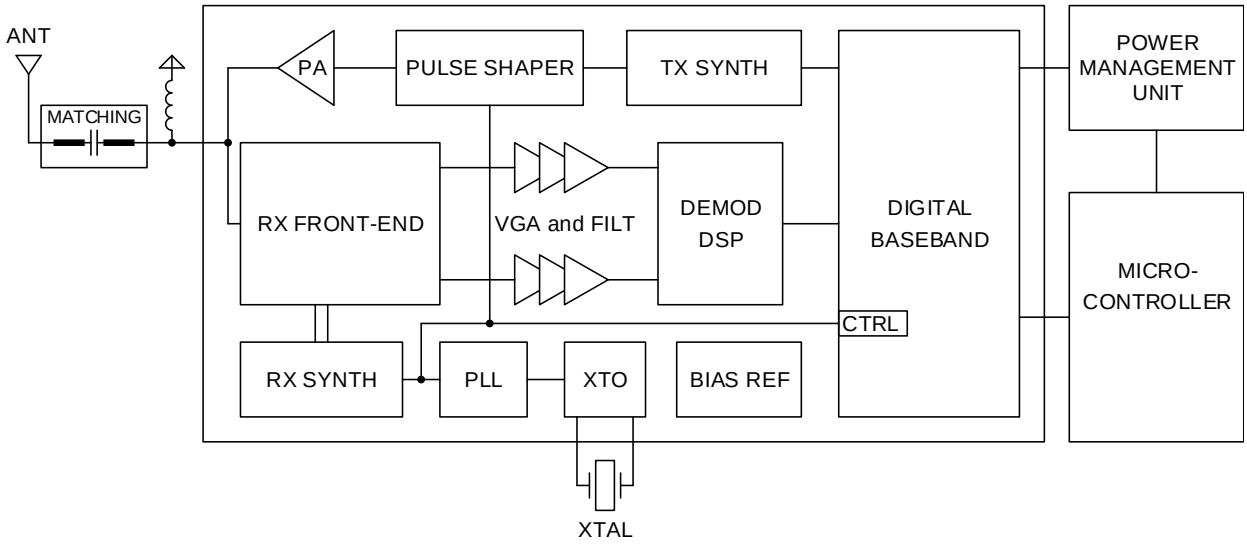
Performance

- Typical UWB Center Frequencies:
  - Channel A: 6520 MHz
  - Channel B: 7040 MHz
  - Channel C: 7560 MHz
  - Channel D: 7987 MHz
- Typical Link Budget at Ranging Error Rate (RER) = 1%: 90.5 dB
- Typical Pulsed Peak TX Output Power: up to 11.5 dBm
- Typical Power Consumption:
  - RX average: 30 mA (after sync word detection)
  - TX average (max. output power): 15 mA
  - READY mode: 250 µA (including crystal)
  - OFF mode: 25 nA (only V_{DD_IO} applied)

Description

The ATA8352 device is a highly integrated, low-power IR-UWB transceiver with an integrated security layer for secure distance bounding and data communication between two devices.

Figure 1. ATA8352 Block Diagram



The ATA8352 transceiver includes fully-digital transmitting circuitry to provide maximum flexibility in the generation of UWB pulse signals. The transmitter can accurately generate pulse durations ranging from less than 1 ns to more than 10 ns, with a controlled envelope shape and a carrier frequency from around 6.2 GHz to 8.3 GHz. The transmitter output power can be fine-tuned to ensure that all applications meet ETSI and FCC regulations.

The ATA8352 receiver is characterized by a high-gain and low-power wideband analog radio frequency front-end and a high-speed and low-power digital baseband processor.

The receive path consists of a frequency-down conversion circuit comprising Low-noise Amplifiers (LNA) and mixers, a digitally-controlled Variable Gain Amplifier (VGA) with a digital Automatic Gain Control (AGC), an Analog-to-Digital conversion and a digital baseband signal processing unit for the highly stable sub-nanosecond Time of Arrival (ToA) estimation.

The system includes a formally proven purpose-built Media Access Control (MAC) layer for secure distance bounding and data communication for proximity-based access control. The user can configure the layer to ensure security while providing a sufficient amount of distance measurements to run in a single secure access control session. This improves distance measurement accuracy through averaging.

The secure distance bounding layer design helps to block both application and physical-layer distance modification attacks. It can operate with any microcontroller that can generate cryptographically secure random numbers and perform authentication routines.

Table of Contents

1. Quick References

1.1 Reference Documentation

For further details, refer to the following:

- *ATA8352 Impulse-Radio Ultra-Wideband (IR-UWB)Transceiver User's Guide*
- *ATA8352 Module Application Note*

1.2 Acronyms and Abbreviations

Table 1-1. Acronyms and Abbreviations

Acronyms	Abbreviations
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
ANT	Antenna
ATB	Analog Test Bus
BCM	Body Control Module
BFSK	Binary Frequency Shift Keying
Ch	Channel
CLK	Clock
CTRL	Control
CW	Continuous Wave
DC	Direct Current
DSP	Digital Signal Processing
ESD	Electrostatic Discharge
FE	Front-end
FLL	Frequency Locked Loop
FSK	Frequency Shift Keying
GND	Ground
GPO	General Purpose Output
IC	Integrated Circuit
ID	Identifier
IMMO	Immobilizer
IO, I/O	Input Output
IR	Impulse Radio
IRQ	Interrupt Request
LF	Low Frequency
LNA	Low-Noise Amplifier

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Acronyms	Abbreviations
LO	Local Oscillator
LUT	Look-up Table
MAC	Media Access Control
PA	Power Amplifier
PLL	Phase Locked Loop
PR	Prover
PSD	Power Spectral Density
RAM	Random Access Memory
RER	Ranging Error Rate
RF	Radio Frequency
RX	Receive/Reception
SPI	Serial Peripheral Interface
SRF	Self Resonant Frequency
SSID	Secure Session Identifier
T_AMB	Ambient Temperature
TA	Turnaround
TFBGA	Thin Profile Fine Pitch Ball Grid Array
ToA	Time of Arrival
TDoA	Time Difference-of-Arrival
TX	Transmit/Transmission
UWB	Ultra-Wideband
VGA	Variable Gain Amplifier
VR	Verifier
XTAL	Crystal
XTO	Crystal Oscillator

2. Ordering Information

Extended Type Number	Package	Remarks
ATA8352-7MQW	TFBGA	33-Ball Thin Fine Pitch Ball Grid Array (4YB) – 4.5x4.5 mm Body

3. Functional Overview

3.1 Pin Diagram and Pin Functions

Figure 3-1. Pin Diagram TFBGA33

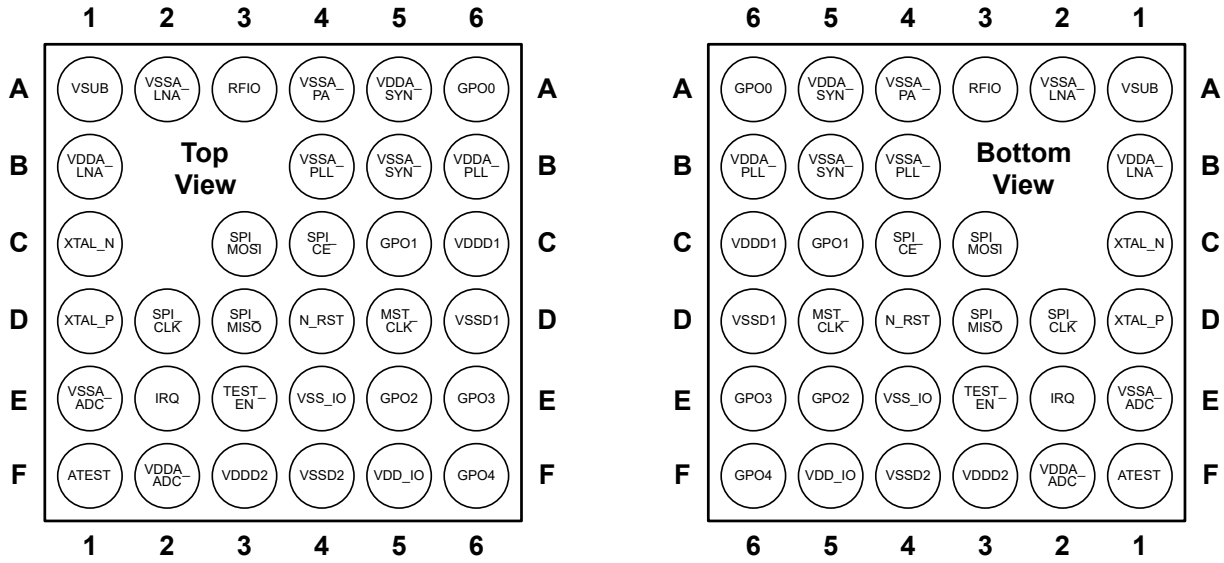

Table 3-1. Pin Description

Pin Number	Pin Name	Type	Function	Voltage Domain
A1	VSUB	Analog	GND	VBAT 3.3V
A2	VSSA_LNA	Analog	GND	VCore 1.25V
A3	RFIO	Analog	RF Antenna Pin	VCore 1.25V
A4	VSSA_PA	Analog	GND	VCore 1.25V
A5	VDDA_SYN	Analog	Core Supply 1.25V	VCore 1.25V
A6	GPO0 (1)	Digital	General Purpose Output 0 (Debug/Test)	VBAT 3.3V
B1	VDDA_LNA	Analog	Core Supply 1.25V	VCore 1.25V
B4	VSSA_PLL	Analog	GND	VCore 1.25V
B5	VSSA_SYN	Analog	GND	VCore 1.25V
B6	VDDA_PLL	Analog	Core Supply 1.25V	VCore 1.25V
C1	XTAL_N	Analog	48 MHz Crystal Oscillator Negative Port, Gate Contact	—
C3	SPI_MOSI	Digital	SPI Master Out Slave In	VBAT 3.3V
C4	SPI_CE	Digital	SPI Chip Select (Active-high)	VBAT 3.3V
C5	GPO1(1)	Digital	General Purpose Output 1 (Debug/Test)	VBAT 3.3V
C6	VDDD1	Digital	Core Supply 1.25V	VCore 1.25V
D1	XTAL_P	Analog	48 MHz Crystal Oscillator Positive Port, Drain Contact	—
D2	SPI_CLK	Digital	SPI Clock Input	VBAT 3.3V

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Pin Number	**Pin Name**	**Type**	**Function**	**Voltage Domain**
D3	SPI_MISO	Digital	SPI Master In Slave Out	VBAT 3.3V
D4	N_RST	Digital	Chip Reset (Active-low)	VBAT 3.3V
D5	MST_CLK	Digital	Master Clock Output (default 4 MHz)	VBAT 3.3V
D6	VSSD1	Digital	GND	VCore 1.25V
E1	VSSA_ADC	Analog	GND	VCore 1.25V
E2	IRQ	Digital	Interrupt Request Output	VBAT 3.3V
E3	TEST_EN(2)	Digital	Test Mode Enable (Active-high) - Connect to GND in Application	VBAT 3.3V
E4	VSS_IO	Digital	GND	VBAT 3.3V
E5	GPO2(1)	Digital	General Purpose Output 2 (Debug/Test)	VBAT 3.3V
E6	GPO3(1)	Digital	General Purpose Output 3 (Debug/Test)	VBAT 3.3V
F1	ATEST	Analog	Analog Test - Open in Application	VCore 1.25V
F2	VDDA_ADC	Analog	Core Supply 1.25V	VCore 1.25V
F3	VDDD2	Digital	Core Supply 1.25V	VCore 1.25V
F4	VSSD2	Digital	GND	VCore 1.25V
F5	VDD_IO	Digital	I/O Power Supply 3.3V	VBAT 3.3V
F6	GPO4(1)	Digital	General Purpose Output 4 (Debug/Test)	VBAT 3.3V

Notes:

1. The pins GPO0 to GPO4 are used for testing and debug purposes only and are not intended for general use in an application.
2. The pin TEST_EN (E3) is used only for device testing and must be connected to GND for a communication or distance bounding application.

3.2 Digital Pin States

The state of the digital output pins depends on the supply voltages and the state of the control signals SPI_CE and N_RST. Table 3-2 and Table 3-3 give an overview on the corresponding states.

Table 3-2. Pin States when V_{DD_IO} = 3.3V and V_{DD_CORE} = 0V

Operating Mode	N_RST	SPI_CE	GPO [4:0]	SPI_MISO	IRQ	MST_CLK
	Input		Output			
OFF	X	X	Z	Z	Z	Z

Table 3-3. Pin States when V_{DD_IO} = 3.3V and V_{DD_CORE} = 1.25V

Operating Mode	N_RST	SPI_CE	SPI_MOSI	SPI_CLK	GPO[4:0]	SPI_MISO	IRQ	MST_CLK
	Input				Output			
IDLE	L	L	[1]	[1]	L	Z	L	L
	L	H	[1]	[1]	L	L	L	L
READY or Communication	H	L	[1]	[1]	X	Z	X	X
	H	H	[1]	[1]	X	L	X	X

with

- Z = High Impedance state
- X = Undefined state
- L = Low state
- H = High state

Note:

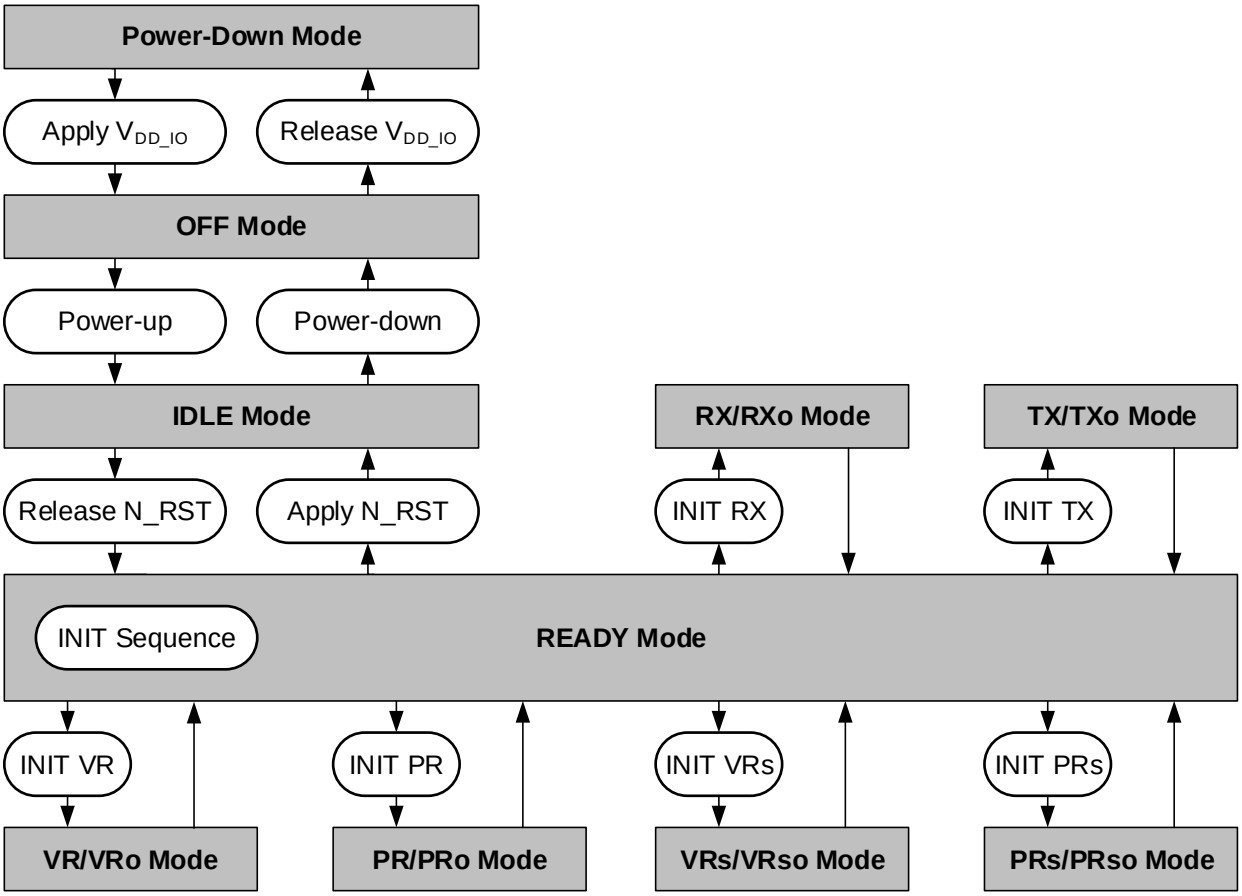
1. Input stage with pull-down (~20 kΩ), that is 'L' stage if Open.

4. Functional Description

4.1 Operating Modes

This section gives an overview of the operating modes, which are implemented in the ATA8352. Figure 4-1 shows the available modes and the transitions between the modes.

Figure 4-1. Operating Modes Overview



4.1.1 Power-Down Mode

In Power-Down mode, no supply voltage is applied to the device; in other words, both, V_{DD_IO} and V_{DD_CORE} are switched off.

4.1.2 OFF Mode

The device is in OFF mode when V_{DD_IO} is applied but V_{DD_CORE} is connected to ground. The OFF mode is useful when the chip is inactive but the GPIO pins are required to be in a high-Z state; for example, for multi-slave SPI operation. Power consumption is reduced to the minimum.

4.1.3 IDLE Mode

In IDLE mode, both supply voltages are applied to the device. A predefined sequence must be followed to securely power up the system.

In IDLE mode, the N_RST pin can be raised at any time to proceed to READY mode.

4.1.4 READY mode

The READY mode is entered when the chip is powered up and the N_RST signal is raised. Initially, the system provides only access to the SPI interface. All other blocks are switched off.

Before using any of the receive or transmit modes, the INIT sequence must be executed, which switches on and calibrates the crystal oscillator, the PLL and the FLLs.

4.1.5 Receive Mode RX

In the RX mode, the device can receive data from another device that is programmed in the TX mode.

To enter the RX mode, the device must be configured accordingly by a sequence of SPI commands. Once programmed, the chip starts listening for a configured number of packets from a transmitting device. The information regarding the received packets is stored in the data part of the RAM.

The IC automatically switches back to the READY mode when the expected number of packets is received.

4.1.6 Transmit Mode TX

In the TX mode, the device can transmit data to another device that is programmed in the RX mode.

To enter the TX mode, the device must be configured accordingly by a sequence of SPI commands and the TX data must be written to the data section of the RAM. Once programmed, the chip starts transmitting the configured number of packets. The IC automatically switches back to the READY mode after the data have been sent.

4.1.7 Distance Bounding Modes

In the Distance Bounding modes, two devices (verifier and prover) are automatically exchanging data telegrams to determine the minimum distance between them by a time-of-flight measurement. The verifier initiates the measurement, and the prover responds to this data telegram.

The distance bounding measurement can be performed in two modes:

- Normal mode VR/PR
- Secure mode VRs/PRs

The Secure mode offers additional security by applying a pseudo-random scrambling scheme to each bit's data symbols.

4.1.8 Modes with Frequency Offset Compensation

The device offers special modes with frequency offset compensation for the RX, TX and all distance bounding modes. These modes are:

- RXo
- TXo
- VRo
- PRo
- VRso
- PRso

In these modes, data packets contain a postamble that allows an automatic offset calculation between the quartz oscillators' frequency in the transmitting and receiving device. Frequency offset compensation is required to gain an accurate absolute distance result between the devices. Averaging between multiple measurements is recommended to increase overall accuracy.

4.2 Recommended Register Settings

The following table provides the recommended and the default settings for a typical application. The default settings reflect the configuration of the system after a reset. The recommended settings can be written to the device via SPI. The major differences to the default settings are:

- Increased pulse bandwidth of 360 MHz
- Reduced pre-amble and post-amble lengths
- Eight symbols per bit
- No SSID transmission

The short telegram length combined with a higher pulse bandwidth allows for an increased transmit power and, therefore, higher link budget.

Table 4-1. Recommended and Default Register Settings

Register	Recommended Settings	Default Settings
A0 – Bias	0x01 0xDC 0x26 0x2A 0x00	0x01 0xDF 0x26 0x2A 0x00
A1 – Bias2	Ch A: 0x07 0x2A 0x22 0x20 0x20 Ch B, C, D: 0x07 0x2A 0x22 0x20 0x00	0x07 0x2A 0x22 0x20 0x00
A2 – Enable	0x0A 0x00 0x00 0x00 0x00	0x0A 0x00 0x00 0x00 0x00
A3 – Crystal	0x0C 0x03 0xB0 0x78 0x78 0x20	0x0C 0x03 0x28 0x18 0x68 0x00
A4 – PLL	Ch A, B, C: 0x12 0x30 0xFC 0x40 0x18 0x22 0x80 Ch D: 0x12 0x31 0x08 0x40 0x18 0x22 0x80	0x12 0x30 0xFC 0x40 0x18 0x22 0x80
A5 – FLL RX Write	Ch A: 0x14, 0xDE, 0x95, 0xDF, 0x76, 0xC8 Ch B: 0x14, 0xFF, 0x95, 0xDF, 0x76, 0xC8 Ch C: 0x15, 0x1F, 0x15, 0xDF, 0x76, 0xC8 Ch D: 0x15, 0x25, 0x15, 0xDF, 0x76, 0xC8	0x14 0xDD 0x55 0xE3 0x36 0xC8
A6 – FLL RX Read	NA	NA
A7 – RX FE	0x1E 0x40	0x1E 0x60
A8 – VGA	0x21 0xDF 0xC0	0x21 0x9B 0xC0
A9.0 – AGC Preamble	0x24 0xC8 0x83 0x4D 0x53 0x30	0x24 0xCF 0x85 0x50 0x01 0x50
A9.1 – AGC Postamble	0x25 0xC8 0x83 0x4D 0x53 0x30	0x25 0xCF 0x85 0x50 0x01 0x50
A10 – ADC	0x28 0x80 0x00	0x28 0x80 0x00
A11 – Demod	0x2E 0x19 0x80	0x2E 0x19 0x80

.....continued

Register	Recommended Settings	Default Settings
A12 – FLL TX Write	Ch A: 0x32, 0x67, 0xD1, 0x17, 0xBB, 0xC8, 0xE8 Ch B: 0x32, 0x6F, 0xF1, 0x17, 0xBB, 0xC8, 0xEA Ch C: 0x32, 0x78, 0x31, 0x17, 0xBB, 0xC8, 0xEC Ch D: 0x32, 0x79, 0x31, 0x17, 0xBB, 0xC8, 0xEE	0x32 0x67 0x11 0x17 0x9B 0xC8 0xCA
A13 – BFSK	0x36 0x4C 0x4C 0x3C 0x80	0x36 0x44 0x44 0x3C 0x80
A14 – TX PA	0x3B 0xC1 0xFF 0xF8 0x88 0x80	0x3B 0xC9 0xFF 0xF8 0x88 0x8E
A15 – Pulse Shape	0x3E 0x5D 0x95 0x0C 0x48	0x3E 0xE5 0xDD 0x50 0xC8
A16 – Pulse Shape2	0x42 0x5D 0x95 0x0C 0x48	0x42 0xE5 0xDD 0x50 0xC8
A17 – FLL TX Read	NA	NA
A18 – Data	NA	NA
A19 – Digital	0x4F 0x1C 0x03 0x00	0x4F 0x1C 0x02 0x80
A20 – ID	NA	NA
A21 – GPO	0x56 0x00 0x02 0x80 0x04	0x56 0x00 0x02 0x80 0x04
A22 – Version	0xD8 0x1C	0xD8 0x1C
A23 – IRQ	0x5F 0x80	0x5F 0x80
A24.0 – Mode	0x60 0x53 0x0C 0x90	0x60 0x5A 0x00 0x10
A24.3 – AGC LUT	0x63 0xBC 0x17 0x86 0xF1 0x5E 0x3B 0xCB 0x39 0x27 0x34 0xE8 0x8C 0xF1 0xA6 0x35 0xC2 0xA8 0x59 0x0B 0xA0 0x6C 0x0E 0x81 0xF0 0x42 0x08 0xC1 0x28 0x27 0x05 0x20 0xAC 0x16 0x82 0xF0 0x62 0x0C 0xC1 0xA8 0x37 0x07 0x20 0xEC 0x1F	0x63 0xBC 0xB7 0x9A 0xF3 0xDE 0x8B 0xD3 0x7A 0xAF 0x5C 0xEB 0x9D 0x93 0xB6 0x66 0x4C 0xD9 0x9D 0x13 0xA2 0x7C 0x50 0x82 0x10 0x46 0x09 0x41 0x38 0x29 0x05 0x60 0xB4 0x17 0x83 0x10 0x66 0x0D 0x41 0xB8 0x39 0x07 0x60 0xF4 0x1F
A25 – ATB	0x64 0x00 0x00	0x64 0x00 0x00
A26 – PAD	0x68 0x00 0x00 0x00 0xFC 0x7F 0xC0	0x68 0x00 0x00 0x00 0xFC 0x7F 0xC0

.....continued

Register	Recommended Settings	Default Settings
A27 – Secure Mode	NA	ID = 0: 0x6C, 0x2F, 0x00, 0x10, 0x83, 0x10, 0x51, 0x87, 0x20, 0x92, 0x8B, 0x30, 0xD3, 0x8F, 0x41, 0x14, 0x93, 0x51, 0x55, 0x97, 0x61, 0x96, 0x9B, 0x71, 0xD7, 0x9F, 0x82, 0x18, 0xA3, 0x92, 0x59, 0xA7, 0xA2, 0x9A, 0xAB, 0xB2, 0xDB, 0xAF, 0xC3, 0x1C, 0xB3, 0xD3, 0x5D, 0xB7, 0xE3, 0x9E, 0xBB, 0xF3, 0xDF, 0xBF ID = 1: 0x6D, 0x13, 0x2F, 0x6A, 0x51, 0x42, 0x14, 0x5E, 0x5E, 0x38, 0x75, 0x6B, 0xAE, 0x95, 0x7B, 0x2E, 0xA3, 0x54, 0xDC, 0x73, 0xE3, 0x0B
A28 – FLL CAL	0x70 0x77	0x70 0x77
A29 – TDoA	0x74 0x00 0x00 0x00 0x00 0x00 0x00	0x74 0x00 0x00 0x00 0x00 0x00 0x00

- NA = Not applicable; for example, for status registers or if the recommended settings are identical to the default settings.

4.3 Packet, Challenge and Response Structure

All the communication packets exchanged between transmitting and receiving devices contain a preamble and a synchronization word field. The preamble is needed to achieve pulse-synchronization between the communicating devices and to calculate the time of arrival with high precision. The synchronization word is required to achieve packet-synchronization between the communicating devices. Only upon successful packet-synchronization is it possible to correctly decode the data contained in a packet.

In these modes, an additional postamble can be attached to the packet.

Figure 4-2 shows the packet structure for the standard data transmission between two devices with default settings.

Figure 4-2. Data Packet Structure

Figure 4-3 shows the structure of a typical packet that is exchanged by two devices in a Distance Bounding mode with the default settings. The preamble and sync word are identical to a standard data packet. Afterward, an optional identifier (SSID) and the random data (RNR) are exchanged, followed by an optional postamble for the frequency offset compensation and the fixed turnaround time (TA) to switch the transmitter and receiver roles.

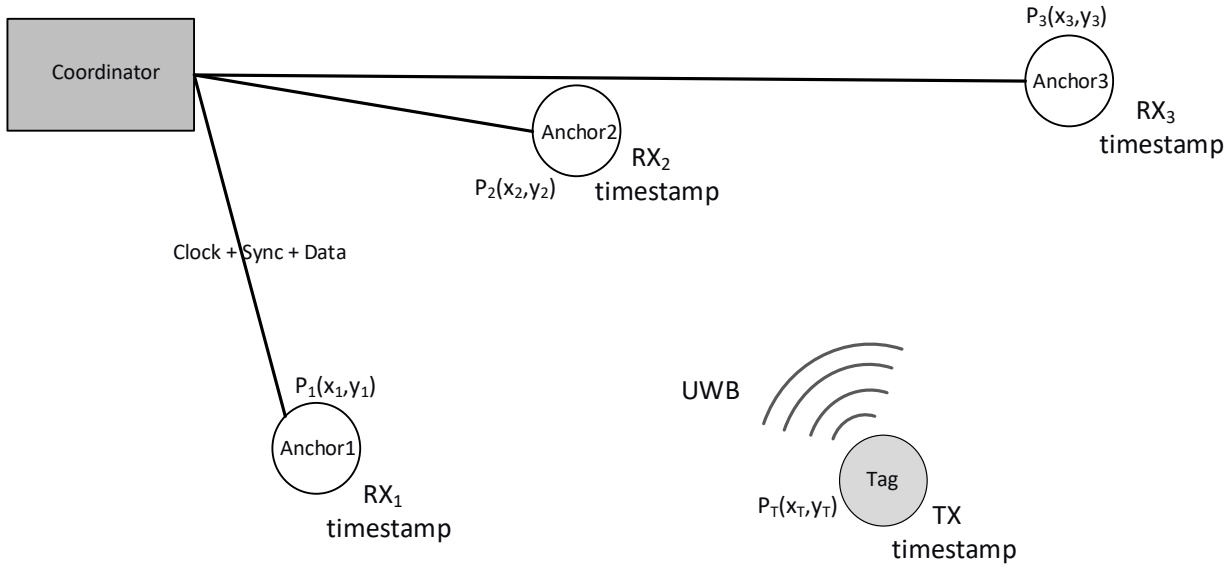
Figure 4-3. Distance Bounding Packet Structure

4.4 UWB Application Areas

The ATA8352 can be used for secure distance bounding applications in industrial environments for example to control machine access and handling and for Real-Time-Location-Services (RTLS) to determine and track the

position of mobile machines, devices and goods. It is also suitable for secure home access applications. The following figure highlights one of these application areas.

Figure 4-4. Real Time Location Service using UWB



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4.5 SPI Interface

The ATA8352 device must be controlled by an external microcontroller using the following interface:

1. An active-low N_RST input pin to reset the device
2. An SPI communication link (SPI_MISO, SPI_MOSI, SPI_CLK and SPI_CE) with a baud rate up to 24 Mbps
3. An IRQ output pin to trigger an event processed by the external host controller

All other I/O signals are not required for device control.

The SPI telegrams have the following general bit and byte structure:

Access	Address					Data	Data	Data	Data	…	Data	Data
0: Write 1: Read	a4	a3	a2	a1	a0	—	—	—	—	…	—	—
Byte 1								Byte 2	Byte 3	…	Byte N-1	Byte N

The upper six bits of the first byte define the type of operation (read/write) and a 5-bit register address. The remaining two bits and the following data bytes are assigned to parameters within the corresponding register.

SPI operation is possible as soon as V_{DD_IO} and V_{DD_CORE} are stable. An internal clock is not required; the SPI is completely run by SPI_CLK.

4.6 Power Supply

The ATA8352 is supplied by two separate voltages:

- V_{DD_CORE} = 1.25V for the main core circuitry (comprising V_{DDA} and V_{DDD})
- V_{DD_IO} = 2.0V to 3.5V for I/Os

The subsequent procedure must be followed when applying or removing the supply voltage.

- **Power-up sequence**: V_{DD_IO} must be applied first. V_{DD_CORE} can be applied once V_{DD_IO} is reached. If V_{DD_CORE} is powered-up before V_{DD_IO}, the I/O ring could be set to an unknown state, resulting in high I/O currents in the crowbar circuit. When V_{DD_CORE} is stable, the N_RST pin can be set to 1 after a delay of 100 µs.
- **Power-down sequence**: Before the IC is powered-down, all the internal blocks must be disabled and the signals, which are controlled by the microcontroller, must be Reset (SPI lines and N_RST). After a delay of 100 µs, the N_RST signal (if enabled) and V_{DD_CORE} can be set to ground. Once the core supply has reached 0V, V_{DD_IO} can be switched off.

V_{DD_CORE} Brownout

The user must ensure that V_{DD_CORE} does not drop below 1.0V during operation. Even if the voltage recovers, the system might not work within specifications afterward and might require a complete System Reset. External voltage supervision and brownout detection are recommended.

5. Electrical Specifications

Table 5-1. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Comments
Storage Temperature	T_{STG}	-55	+125	°C	—
Ambient Temperature	T_{AMB}	-40	+105	°C	Operating range
Humidity	—	—	—	—	Fully qualified according to JEDEC JESD22-A110. If the application is exposed to high humidity and the device is permanently powered, it is recommended to apply additional humidity protection.
ESD HBM All Pins	HBM	-4	+4	kV	Human Body Model
ESD CDM All Pins	CDM	-750	+750	V	Charged Device Model
RFIO Pin Maximum Input Power	P_{RFIO_MAX}	—	+15	dBm	CW mode

⚠ CAUTION Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All subsequent parameters are based on default register settings unless otherwise specified. These parameters are valid for T_{AMB} = -40°C to +105°C and V_{DDA} = V_{DDD} = 1.2V to 1.3V over all process tolerances unless otherwise specified. Typical values are given at V_{DDA} = V_{DDD} = 1.25V, T_{AMB} = 25°C and for a typical process unless otherwise specified.

Table 5-2. Supply Voltages and Current Consumption

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Comments
1.00	Analog Supply Voltage	V_{DDA}	1.20	1.25	1.30	V	—
1.10	Digital Core Supply Voltage	V_{DDD}	1.20	1.25	1.30	V	—
1.20	Digital IO Supply Voltage	V_{DD_IO}	2.00	3.30	3.50	V	Functionality guaranteed within specified V_{DDD}
1.30	IO Supply Domain Leakage Current (OFF Mode)[1]	$I_{VDD\_IO\_OFF}$	—	0.025	0.5	µA	V_{DD_IO} = 3.5V V_{DDA} = V_{DDD} = V_{SS}
1.40	Core Domain Leakage Current (IDLE/ READY Mode)	I_{LEAK_IDLE}	—	60	1900	µA	V_{DD_IO} = 3.3V V_{DDA} = V_{DDD} = 1.25V XTAL off
1.50	IDLE Mode Current Consumption	I_{VDD_IDLE}	—	250	2200	µA	XTAL active, sum of all voltage domains
1.60	TX Average Current Consumption	I_{VDD_TX}	—	15	23	mA	Transmitter continuously ON, max TX power setting, core domain
1.65	RX Current Search Mode	$I_{VDD\_RX\_SRCH}$	—	65	90	mA	Receiver searching for a signal and preamble, core domain
1.70	RX Current Locked Mode[1]	$I_{VDD\_RX\_LCK}$	—	30	45	mA	Receiver has locked on signal, core domain

Note:

1. Characterized on samples.

Table 5-3. Crystal Oscillator and Clock

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Comments
2.00	Crystal Frequency	F_{XTAL}	—	48	—	MHz	—
2.10	Crystal Parameter Requirements (48 MHz)	ESR_{XTAL48}	—	—	60	Ω	Equivalent series resistance
2.20		CL_{XTAL48}	—	6	—	pF	Nominal load capacitance
2.30		$C0_{XTAL48}$	—	—	2	pF	Shunt capacitance
2.40		OSF_{XTAL48}	10	—	—	—	Oscillation safety factor, $C0_{XTAL48}$ < 1pF, at 25degC
2.90	Crystal Frequency Tolerance Requirements	DF_{XTAL_INIT}	-20	—	+20	ppm	Frequency tolerance at +25°C
3.00		DF_{XTAL_TEMP}	-16	—	+16	ppm	Frequency tolerance over temperature range
3.10		DF_{XTAL_AGING}	-5	—	+5	ppm	Aging after 10 years
3.30	On-Chip C_L Trim	CL_{TRIM_RANGE}	6.5	7.63	8.8	pF	Trimming via internal 8-bit capacitor array
3.60	Digital Clock Output	F_{MCLK}	4	—	16	MHz	Derived from XTAL. Possible configurations: 4 MHz, 8 MHz, 16 MHz
3.80	Digital Clock Output Duty Cycle	DC_{MCLK}	33	50	66	%	—
3.90	XTO Settling Time	T_{XTAL}	—	—	2	ms	—
4.00	External 48 MHz Clock Input Requirements	V_{IN_XTAL}	0.8	—	1.2	V	Single-ended square wave swing, input on xtal_p, xtal_n connected to ground
4.10		PN_{IN_XTAL}	—	-138	-135	dBc/Hz	Phase noise at 1 MHz
4.20		DC_{IN_XTAL}	40	50	60	%	Duty cycle

Table 5-4. Transmitter

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Comments
5.00	TX Frequency Operating Range	BW_{TX}	6.2	—	8.3	GHz	Bandwidth: -10dB
5.20	Average TX RF Power Channels A, B, C[1]	$P_{TX\_AVG\_ABC}$	-9	-6	-4.5	dBm	Continuous, modulated transmission at maximum TX power setting.
5.21	Average TX RF Power Channel D[1]	$P_{TX\_AVG\_D}$	-10.5	-7.5	-5.5	dBm	Continuous, modulated transmission at maximum TX power setting.
5.30	Peak TX Power	P_{TX_PEAK}	7	11.5	15.5	dBm	Maximum TX power setting
5.40	TX Output Power Step[1]	DP_{TX}	0	0.15	0.35	dB	Fine power steps
5.50	Pulse Bandwidth Default[1]	BW_{PULSE_290}	—	290	—	MHz	-10dB bandwidth of single pulse, default settings
5.51	Pulse Bandwidth Recommended[1]	BW_{PULSE_360}	—	360	—	MHz	-10dB bandwidth of single pulse, recommended settings
5.55	Pulse Bandwidth Range	BW_{PULSE_RANGE}	200	—	500	MHz	-10dB bandwidth, design parameter, related to configured pulse shape.

.....continued

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Comments
5.60	Composite Bandwidth Default[1]	BW_{COMP_290}	—	560	—	MHz	-10dB bandwidth of modulated signal, related to configured pulse shape and FSK deviation, default settings
5.61	Composite Bandwidth Recommended[1]	BW_{COMP_360}	—	640	—	MHz	-10dB bandwidth of modulated signal, related to configured pulse shape and FSK deviation, recommended settings
5.70	Pulse Rate Channel A, B, C	PR_{ABC}	—	3.9375	—	Mpulse/s	Instantaneous pulse rate. Design parameter
5.71	Pulse Rate Channel D	PR_{D}	—	4.125	—	Mpulse/s	Instantaneous pulse rate, recommeded settings. Design parameter.
5.90	BFSK Deviation Default	F_{DEV_290}	—	135	—	MHz	FSK deviation (+/-) from RF center frequency, default settings. Design parameter.
5.91	BFSK Deviation Recommended	F_{DEV_360}	—	145	—	MHz	FSK deviation (+/-) from RF center frequency, recommended settings. Design parameter.
6.00	RF Frequency Accuracy	RF	—	—	1	%	—
6.10	Recommended Frequency Channel A	F_{CHA}	—	6520	—	MHz	Center frequency Ch A
6.11	Recommended Frequency Channel B	F_{CHB}	—	7040	—	MHz	Center frequency Ch B
6.12	Recommended Frequency Channel C	F_{CHC}	—	7560	—	MHz	Center frequency Ch C
6.13	Recommended Frequency Channel D	F_{CHD}	—	7987	—	MHz	Center frequency Ch D
6.20	Out of Band Signal Level[1]	L_{OOB_UWB}	—	—	-30	dB	Below 6GHz and above 8.5GHz, according to frequency plan in parameters 6.10 to 6.13, related to peak PSD, excluding LO harmonics.
6.30	2nd Harmonic Suppression Channel A, B and C[1]	$SUPP_{2ABC}$	—	-27	—	dB	Continuous mode, related to peak PSD
6.33	2nd Harmonic Suppression Channel D[1]	$SUPP_{2D}$	—	-21	—	dB	Continuous mode, related to peak PSD
6.40	3rd Harmonic Suppression Channel A[1]	$SUPP_{3A}$	—	-29	—	dB	Continuous mode, related to peak PSD
6.41	3rd Harmonic Suppression Channel B[1]	$SUPP_{3B}$	—	-25	—	dB	Continuous mode, related to peak PSD
6.42	3rd Harmonic Suppression Channel C[1]	$SUPP_{3C}$	—	-22	—	dB	Continuous mode, related to peak PSD
6.43	3rd Harmonic Suppression Channel D[1]	$SUPP_{3D}$	—	-27	—	dB	Continuous mode, related to peak PSD

Note:

1. Characterized on samples.

Table 5-5. Receiver

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Comments
7.00	Rx Frequency Operating Range	BW_{RX}	6.2	—	8.3	GHz	—
7.10	RF Matching[1]	S_11	—	-7	—	dB	S11 absolute value, referred to 50Ω matching on reference board with High-Q capacitor, High-Q inductor and microstrip/co-planar lines. Typical process, room temperature.
7.20	Maximum Usable Average Input Power[1]	P_{RX_MAX}	—	-10	—	dBm	For valid ranging measurement
7.50	Rx Sensitivity T_AMB < 85°C[1]	$SENS_{85}$	—	-96.5	-95	dBm	TX from signal generator, conducted measurement on reference board, related to average power, ranging measurement with payload of 32 bits, 0 errors allowed, packet error rate = 1%.
7.51	Rx Sensitivity T_AMB < 105°C[1]	$SENS_{105}$	—	—	-92	dBm	TX from signal generator, conducted measurement on reference board, related to average power, ranging measurement with payload of 32 bits, 0 errors allowed, packet error rate = 1%.

Note:

1. Characterized on samples.

Table 5-6. Communication System

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Comments
8.00	Data Rate Range	SYS_{DR}	246	492	1000	kB/s	Clock divider scheme according to default settings, configurable number of pulses per bit in payload
8.01	Data Rate Channel A, B, C	SYS_{DR_ABC}	—	492	—	kB/s	Default and recommended settings, payload configuration: 8 pulses per bit, design parameter
8.02	Data Rate Channel D	SYS_{DR_D}	—	515	—	kB/s	Recommended settings for channel D, payload configuration: 8 pulses per bit, design parameter
8.20	Link Budget[1]	LB	—	90.5	—	dB	Measured on reference boards, recommended settings, 10% ranging error rate, max 3 errors in payload, output PSD -41.3 dBm/MHz
8.55	ADC Sampling Rate Channels A, B, C	F_{ADC_ABC}	—	1008	—	MHz	Design parameter
8.56	ADC Sampling Rate Channel D	F_{ADC_D}	—	1056	—	MHz	Recommended settings for channel D. Design parameter.
8.60	Time-of-Arrival Time Resolution Channels A, B, C	TOA_{RES_ABC}	—	124	—	ps	Related to ADC sampling rate. Design parameter.
8.61	Time-of-Arrival Time Resolution Channel D	TOA_{RES_D}	—	118	—	ps	Related to ADC sampling rate, channel D recommended settings. Design parameter.
8.90	SPI Speed	DR_{SPI}	—	—	24	Mbps	—

Note:

1. Characterized on samples.

Table 5-7. Digital I/O Pin Characteristics

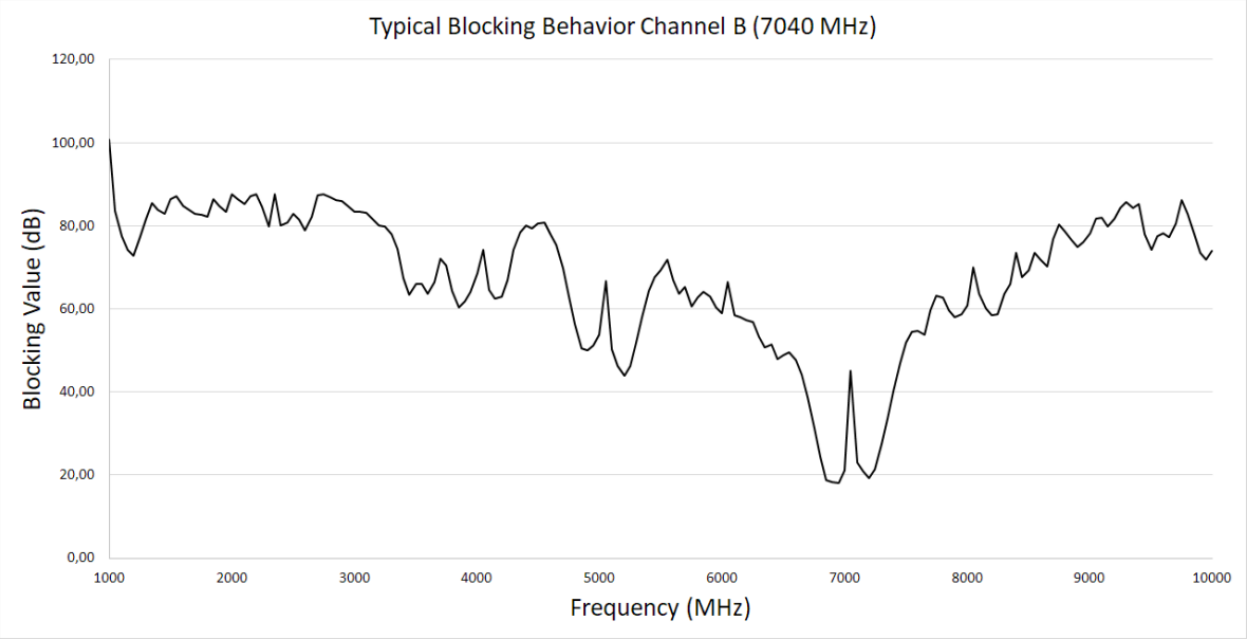
No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Comments
9.00	Input low voltage	V_{IL}	-0.2	—	0.3*V_{DD_IO}	V	SPI_MOSI, SPI_CE, SPI_CLK, N_RST, TEST_EN
9.10	Input high voltage	V_{IH}	0.7*V_{DD_IO}	—	V_{DD_IO} +0.2	V	SPI_MOSI, SPI_CE, SPI_CLK, N_RST, TEST_EN
9.20	Input low level leakage current per pin	I_{IL}	—	—	10	uA	SPI_MOSI, SPI_CE, SPI_CLK, N_RST, TEST_EN, pull-down disabled, current flowing into pin
9.30	Input high level leakage current per pin	I_{IH}	—	—	10	uA	SPI_MOSI, SPI_CE, SPI_CLK, N_RST, pull-down disabled, current flowing out of pin
9.40	Output low voltage	V_{OL}	—	—	0.4	V	SPI_MISO, MST_CLK, IRQ, GPO[4:0], I_{OL}=2mA
9.50	Output high voltage	V_{OH}	V_{DD_IO}-0.5	—	—	V	SPI_MISO, MST_CLK, IRQ, GPO[4:0], I_{OH}=-2mA
9.60	Internal pull-down resistor	R_{PD}	25	40	80	kΩ	SPI_MOSI, SPI_CE, SPI_CLK, N_RST, TEST_EN

Note: The timing characteristics of the SPI interface can be found in the *ATA8352 user guide*.

Blocking

The following figure shows the typical blocking behavior of the ATA8352 for channel B.

Figure 5-1. Blocking Behavior



6. Reference Circuit

The following figure illustrates a typical reference circuit diagram of the ATA8352. The IO voltage between 2.0V and 3.5V may be provided by a standard lithium battery (example: CR2032). The core voltage of 1.25V is generated by a DC/DC converter for optimized overall power consumption.

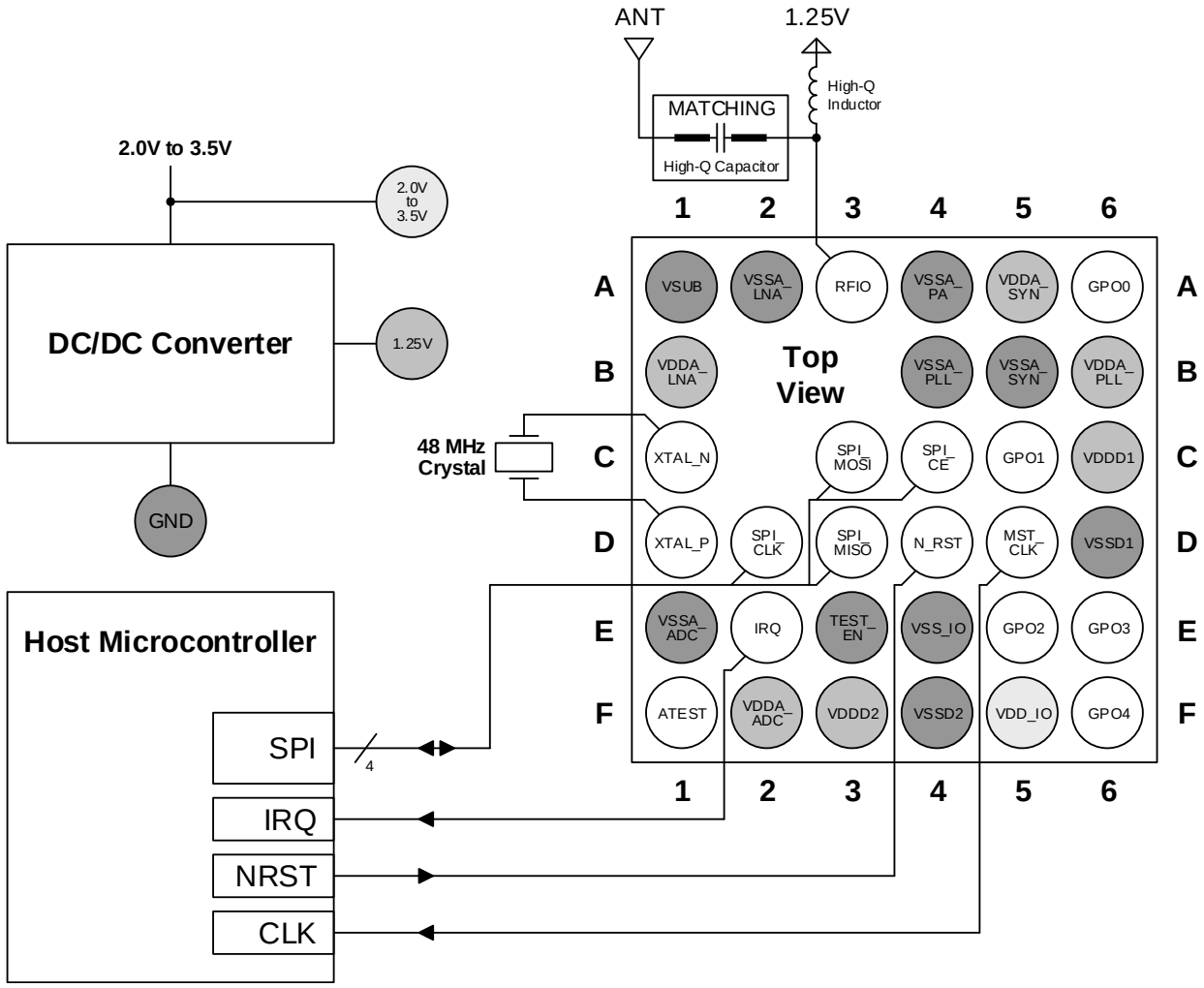
The ATA8352 is controlled by a host microcontroller via the SPI interface. If required, the host can derive a high precision clock from the 48 MHz crystal of the ATA8352.

The RFIO pin of the device has an impedance of 30Ω. The application of this pin when matching to a 50Ω antenna requires the following components:

- High-Q wounded coil inductor with a Self-resonant Frequency (SRF) > 12 GHz (recommended size 0402).
- 30Ω to 50Ω matching network including a High-Q capacitor (recommended size 0201). It is recommended to use microstrip and co-planar lines to achieve the required matching.

The Microchip reference design gives an example implementation including the component values to achieve the required matching.

Figure 6-1. Reference Circuit Diagram



7. Package Information

This section details the package marking information and package outline drawings.

7.1 Package Marking Information

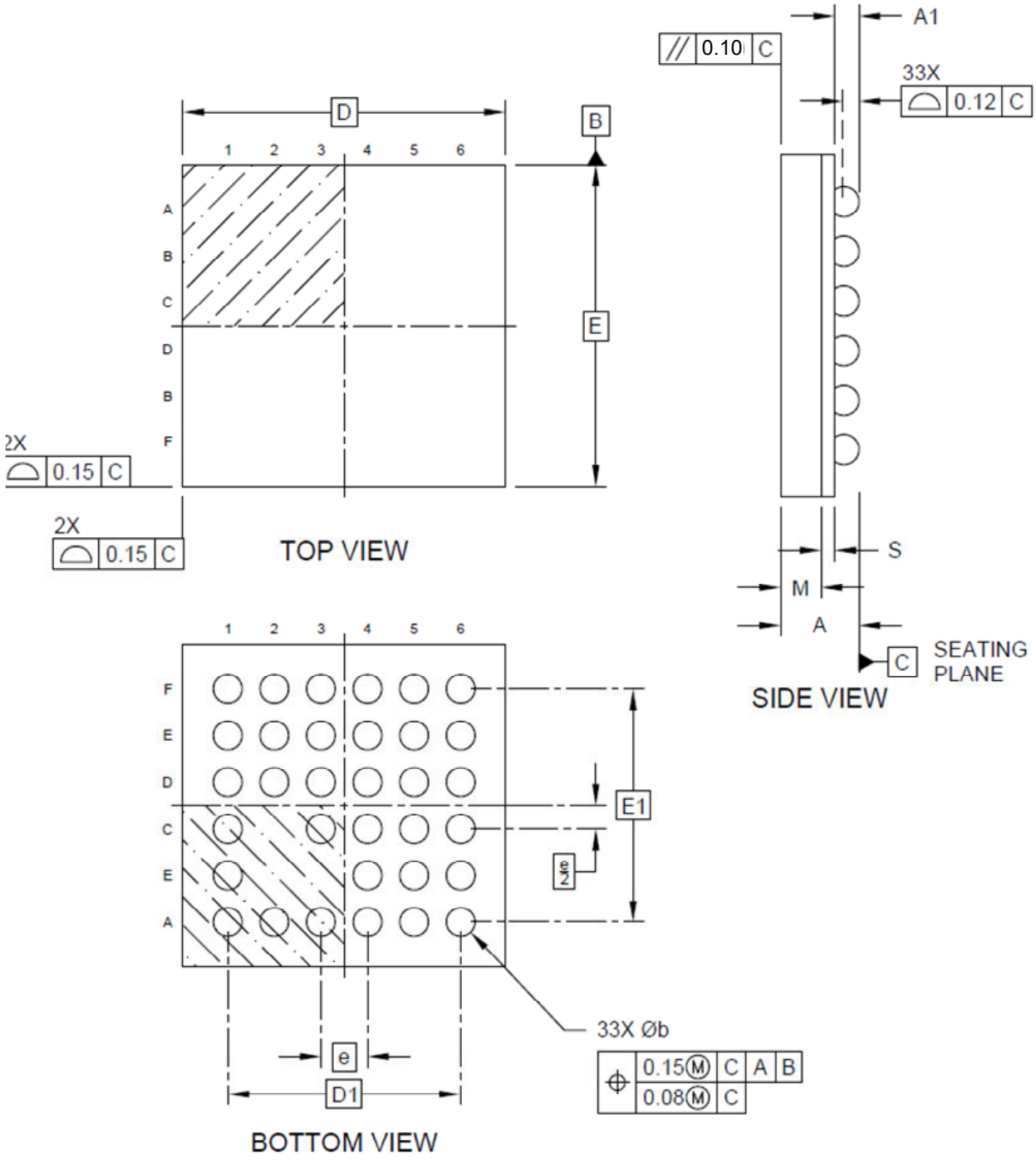
The following figure shows the package marking information of the ATA8352.

Figure 7-1. 33-Lead TFBGA (4.5x4.5x1.1mm)

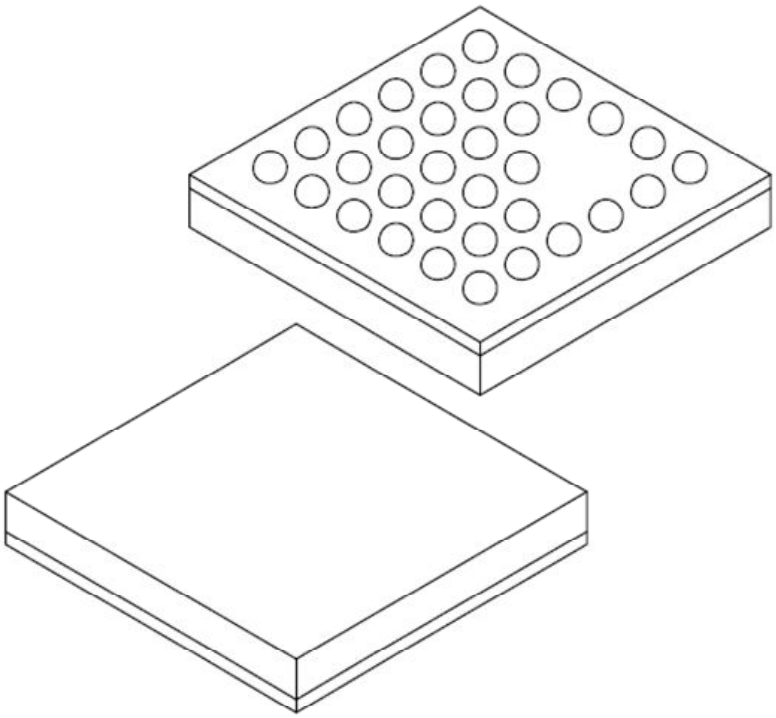
Legend:

- YY: Year code (the last two digits of the calendar year)
- WW: Week code (for example, the week of January 1 is week ‘01’)
- NNN: Alphanumeric traceability code

7.2 Package Outline Drawing



Microchip Technology Drawing C04-21460 Rev A Sheet 1 of 2



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		33	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Standoff	A1	0.27	-	0.37
Mold Capl Thickness	M		0.530 REF	
Substrate Thickness	S		0.176 REF	
Overall Length	D		4.50 BSC	
Overall Terminal Pitch	D1		3.25 BSC	
Overall Width	E		4.50 BSC	
Overall Terminal Pitch	E1		3.25 BSC	
Ball Diameter	b	0.37	-	0.47

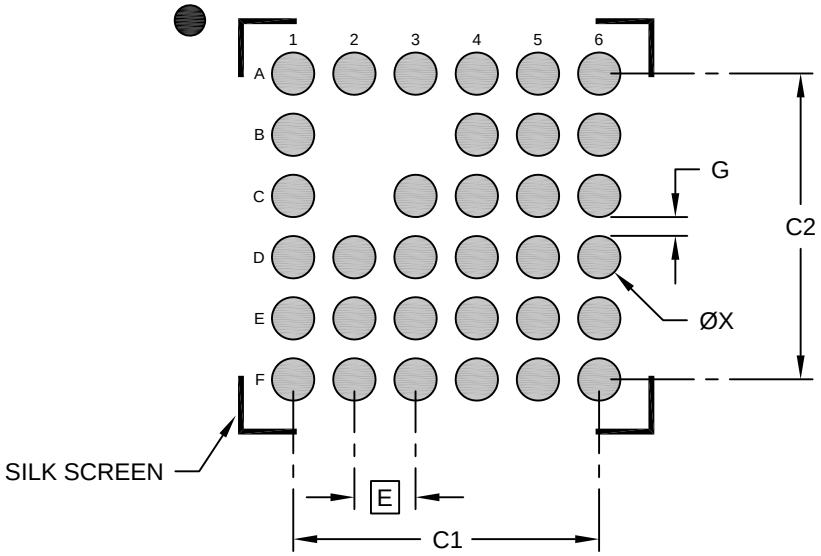
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

33-Ball Thin Fine Pitch Ball Grid Array (4YB) - 4.5x4.5 mm Body [TFBGA]



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		3.30	
Contact Pad Spacing	C2		3.30	
Contact Pad Diameter (X33)	X	0.25	0.30	0.35
Contact Pad to Contact Pad	G	0.30		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

8. Document Revision History

Revision	Date	Section	Description
A	02/2021	Document	Initial Revision

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