ZL30150
Two Channel Clock Translator / NCO
Data Sheet

March 2015

Features

- Generates any Telecom or SyncE frequency independent of the input frequency rate
- Two general purpose synthesizers generate a wide range of digital bus clocks
- Programmable digital PLLs synchronizes to any Telecom (N * 8 kHz) or any Synchronized Ethernet (SyncE) frequencies.
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Digital PLLs filter jitter from 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz
- Four programmable Numerically Controlled Oscillators (NCOs) available where two NCOs can be used at the time
- Automatic hitless reference switching and digital holdover on reference fail
- Four reference inputs configurable as single ended or differential
- Eight LVPECL outputs and four LVCMOS outputs
- Eight outputs configurable as LVCMOS or LVDS/LVPECL/HCSL
- Operates from a single crystal resonator or clock oscillator
- Customer defined default device configuration, including input/output frequencies, is available via OTP(One Time Programmable) memory
- Dynamically configurable via SPI/I2C interface and volatile configuration registers

Ordering Information		
ZL30150GGG2	100 Pin LBGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

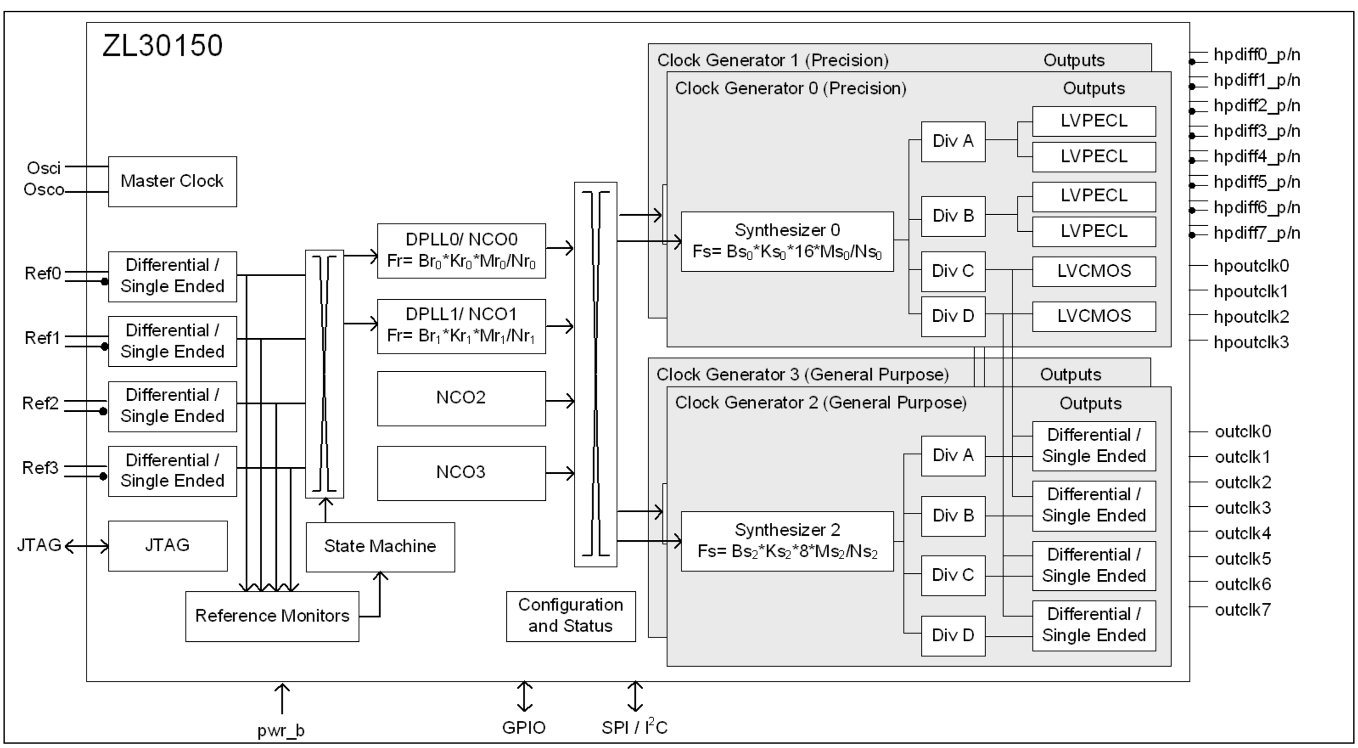

Figure 1 - Functional Block Diagram

Applications

- 10 Gigabit line cards
- Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W, XAUI Clocks
- SONET/SDH

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Change Summary

Below are the changes from the June 2012 issue to the March 2015 issue

Page	Item	Change
1	Added Features bullet	Included availability of customer defined default configurations
1	Ordering Information	Removed ZL30150GGG (leaded version) for the ordering information
14, 30, 30	Updated section 4.0, 5.0 and added 5.1	Updated to included the availability of Custom OTP configuration
170	13.0, “Package Markings“	Added section 13.0 for package markings

Below are the changes from the February 2012 issue to the June 2012 issue

Page	Item	Change
162	Input to Output alignment	Added min/max values for t_{HP_REFD}
163	Output to Output Alignment	Added min/max values for $t_{OUT2OUTD}$
52 and 141	Register 0xC6 - Chip_Revision	Updated chip_revision register 0xC6 = 0x03

1.0 Pin Diagram

	1	2	3	4	5	6	7	8	9	10
A	hpdiff3_p	avss	filter1	avss	osco	osci	avss	filter2	avss	hpdiff7_p
B	hpdiff3_n	avss	filter1_ref	avdd	vcore	vcore	pwr_b	filter2_ref	avss	hpdiff7_n
C	hpdiff2_p	hpdiff2_n	avss	gpio5	at	vss	gpio0	avss	hpdiff6_n	hpdiff6_p
D	hpdiff1_p	hpdiff1_n	avdd	test_en	vcore	vdd_io	gpio11	avdd	hpdiff5_n	hpdiff5_p
E	hpdiff0_p	hpdiff0_n	avdd	gpio7	vss	vss	gpio8	avdd	hpdiff4_n	hpdiff4_p
F	gpio6	avdd	gpio4	so_asel1	vss	vss	gpio1	gpio3	avdd	sck_scl
G	hpoutclk1	hpoutclk0	gpio9	si_sda	vcore	vcore	gpio2	cs_b_asel0	hpoutclk2	hpoutclk3
H	b1vdd_io	avss	avss	tck	vcore	vcore	gpio10	avss	avss	b2vdd_io
J	outclk0	outclk1	tdo	ref0_p	ref1_p	ref2_n	ref3_n	tms	outclk7	outclk6
K	outclk2	outclk3	trst_b	ref0_n	ref1_n	ref2_p	ref3_p	tdi	outclk4	outclk5

1 - A1 corner is identified by metallized markings.

Figure 2 - Package Description

2.0 Pin Description

All device inputs and output are LVCMOS unless it was specifically stated to be differential.

Ball #	Name	I/O	Description
Input Reference			
J4 K4 J5 K5 K6 J6 K7 J7	ref0_p ref0_n ref1_p ref1_n ref2_p ref2_n ref3_p ref3_n	I	**Input Reference 0, 1, 2 and 3.** Input reference sources used for synchronization. The positive and negative pair of these inputs accepts a differential input signal. The refx_p input terminal accept a CMOS input reference. These inputs could be used as a device external feedback input. Maximum frequency limit on single ended inputs is 177.5 MHz, and 750 MHz on differential inputs.
Output Clocks			
J1 J2 K1 K2 K9 K10 J10 J9	outclk0 outclk1 outclk2 outclk3 outclk4 outclk5 outclk6 outclk7	O	**Output Clock 0 to 7.** Configurable output clocks. These can be configured as single ended or differential (0&1, 2&3, 4&5, 6&7) Maximum frequency limit on single ended LVCMOS outputs is 160 MHz, and 350 MHz on differential outputs.
G2 G1 G9 G10	hpoutclk0 hpoutclk1 hpoutclk2 hpoutclk3	O	**High Performance Output Clock 0 to 3.** This output can be configured to provide any one of the single ended high performance clock outputs. Maximum frequency limit on single ended LVCMOS outputs is 177.5 MHz
E1 E2 D1 D2 C1 C2 A1 B1 E10 E9 D10 D9 C10 C9 A10 B10	hpdiff0_p hpdiff0_n hpdiff1_p hpdiff1_n hpdiff2_p hpdiff2_n hpdiff3_p hpdif3_n hpdiff4_p hpdiff4_n hpdiff5_p hpdiff5_n hpdiff6_p hpdiff6_n hpdiff7_p hpdif7_n	O	**High Performance Differential Output Clock 0 to 7 (LVPECL).** This output can be configured to provide any one of the available high performance differential output clocks. Maximum frequency limit on differential outputs is 750 MHz
Control and Status			

Table 1 - Pin Description

Ball #	Name	I/O	Description
B7	pwr_b	I	**Power-on Reset.** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. The pwr_b pin should be held low for 2ms. This pin is internally pulled-up to V_{DD}. **User can access device registers either 55 ms after pwr_b goes high, or after bit 7 in register at address 0x00 goes high which can be determined by polling the register at address 0x00.**
C7 F7 G7 F8 F3 C4 F1 E4 E7 G3 H7 D7	gpio0 gpio1 gpio2 gpio3 gpio4 gpio5 gpio6 gpio7 gpio8 gpio9 gpio10 gpio11	I/O	**General Purpose Input and Output pins.** These are general purpose pins managed by the internal processor based on device configuration. Recommended usage of GPIO include: • DPLL lock indicators • DPLL holdover indicators • Reference fail indicators • Reference select control or monitor • Differential output clock enable (per output or as a bank of 2 or 4 outputs) • High performance LVCMOS outputs enable • Host Interrupt Output: flags changes of device status prompting the processor to read the enabled interrupt service registers (ISR). Pins 5:0 are internally pulled down to GND and pins 11:6 are internally pulled up to V_{DD}. If not used GPIO can be kept unconnected. **After power on reset, device GPIO[0,1,3,4,5] configure some of device basic functions, GPIO[3] set I2C or SPI control mode, GPIO[1,0] set master clock rate selection. The GPIO[0,1,3] pins must be either pulled low or high with an external 1 KΩ resistor as needed for their assigned functions at reset; or they must be driven low or high for 55 ms after reset, and released and used for normal GPIO functions.** **The GPIO[4,5] pins must be either pulled low with external 1 KΩ resistors; or they must be driven low for 55 ms after reset, and then released and used for normal GPIO functions.**
Host Interface			
F10	sck_scl	I/O	**Clock for Serial Interface.** Provides clock for serial micro-port interface. This pin is also the serial clock line (SCL) when the host interface is configured for I2C mode. As an input this pin is internally pulled up to V_{DD}.
G4	si_sda	I/O	**Serial Interface Input.** Serial interface input stream. The serial data stream holds the access command, the address and the write data bits. This pin is also the serial data line (SDA) when host interface is configured for I2C mode. This pin is internally pulled up to V_{DD}.
F4	so_asel1	I/O	**Serial Interface Output.** Serial interface output stream. As an output the serial stream holds the read data bits. This pin is also the I2C address select when host interface is configured for I2C mode.

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
G8	cs_b_asel0	I	**Chip Select for Serial Interface.** Serial interface chip select, this is an active low signal. This pin is also the I2C address select when host interface is configured for I2C mode.This pin is internally pulled up to V_{DD}.
APLL Loop Filter			
A3	filter1	A	**External Analog PLL1 Loop Filter terminal.**
B3	filter1_ref	A	**Analog PLL1 External Loop Filter Reference.**
A8	filter2	A	**External Analog PLL2 Loop Filter terminal.**
B8	filter2_ref	A	**Analog PLL2 External Loop Filter Reference.**
JTAG (IEEE 1149.1) and Test			
D4	test_en	I	**Test Mode Enable.** A logic high at this pin enables device test modes. This pin is internally pulled down to GND. Connect this pin to GND.
C5	at	A-I/O	**Analog PLL Test.** Test pin for analog PLL. Leave unconnected.
J3	tdo	O	**Test Serial Data Out.** JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
K8	tdi	I	**Test Serial Data In.** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
K3	trst_b	I	**Test Reset.** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to VDD. If this pin is not used then it should be connected to GND.
H4	tck	I	**Test Clock.** Provides the clock to the JTAG test logic. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be connected to GND.
J8	tms	I	**Test Mode Select.** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
Master Clock			
A5	osco	A-O	**Oscillator Master Clock.** For crystal operation, a crystal is connected from this pin to osci. Not suitable for driving other devices. For clock oscillator operation, this pin is left unconnected.
A6	osci	I	**Oscillator Master Clock.** For crystal operation, a crystal is connected from this pin to osco. For clock oscillator operation, this pin is connected to a clock source.
Power and Ground			
D6	$V_{DD\text{-}IO}$		**Positive Supply Voltage IO.** $+3.3V_{DC}$ nominal.
H1	$B1V_{DD\text{-}IO}$		**Bank 1 Positive Supply Voltage IO.** Output group specific $+3.3/2.5/1.8/1.5V_{DC}$ nominal.

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
H10	$B2V_{DD-IO}$		**Bank 2 Positive Supply Voltage IO.** Output group specific $+3.3/2.5/1.8/1.5V_{DC}$ nominal.
B5 B6 D5 G5 G6 H5 H6	V_{CORE}		**Positive Supply Voltage.** $+1.8V_{DC}$ nominal. These pins should not be connected together on the board. Please refer to ZLAN-269 for recommendations
B4 D3 D8 E3 E8 F2 F9	AV_{DD}		**Positive Analog Supply Voltage.** $+3.3V_{DC}$ nominal.
C6 E5 E6 F5 F6	V_{SS}		**Ground.** 0 Volts.
A2 A4 A7 A9 B2 B9 C3 C8 H2 H3 H8 H9	AV_{SS}		**Analog Ground.** 0 Volts.

Table 1 - Pin Description (continued)

3.0 Application Example

Synchronous Optical Ethernet ports supporting 10GBASE-W/10GBASE-R often require multiple frequency translation paths to synchronize the optical port with the system backplane; and to translate the receive line clock rate to the system backplane clock rate for use in system synchronization. Figure 3 illustrates how a single ZL30150 efficiently handles all synchronization and clock rate translations required for a synchronous 10GBASE-W/10GBASE-R port.

ZL30150 in Figure 3 is configured with one DPLL that selects between two 19.44 MHz backplane clocks; both backplane clocks can be monitored for impairments and the automatic reference switching state machine can switch from a failed reference to a good reference without causing bit errors in the transmission channel. DPLL 0 uses one precision clock generator to generate two copies of a low jitter 156.25 MHz clock to time the XAUI bus and the other precision clock generator to generate a synchronous low jitter clock at either 156.25 MHz or 155.52 MHz depending on whether a 10 GBASE-R or 10 GBASE-W port is implemented.

DPLL1 uses one of the general purpose clock generators to generate two copies of a 19.44MHz clock synchronized to the receive line clock; the receive line clock rate will be either 161.13 MHz or 155.52 MHz depending on if a 10GBASE-R or 10GBASE-W port is implemented. The clock rate translation from 161.13 MHz to 19.44 MHz involves a double translation which is accomplished via the two stage PLL architecture of the ZL30150.

Synthesizer 3 is used in free run mode where it can generate any free-run frequency from 1 Hz to 350 MHz. I Figure 3 it is used to generate common clock frequency (33.33 MHz, 66.66 MHz or 100 MHz) for micro-processor.

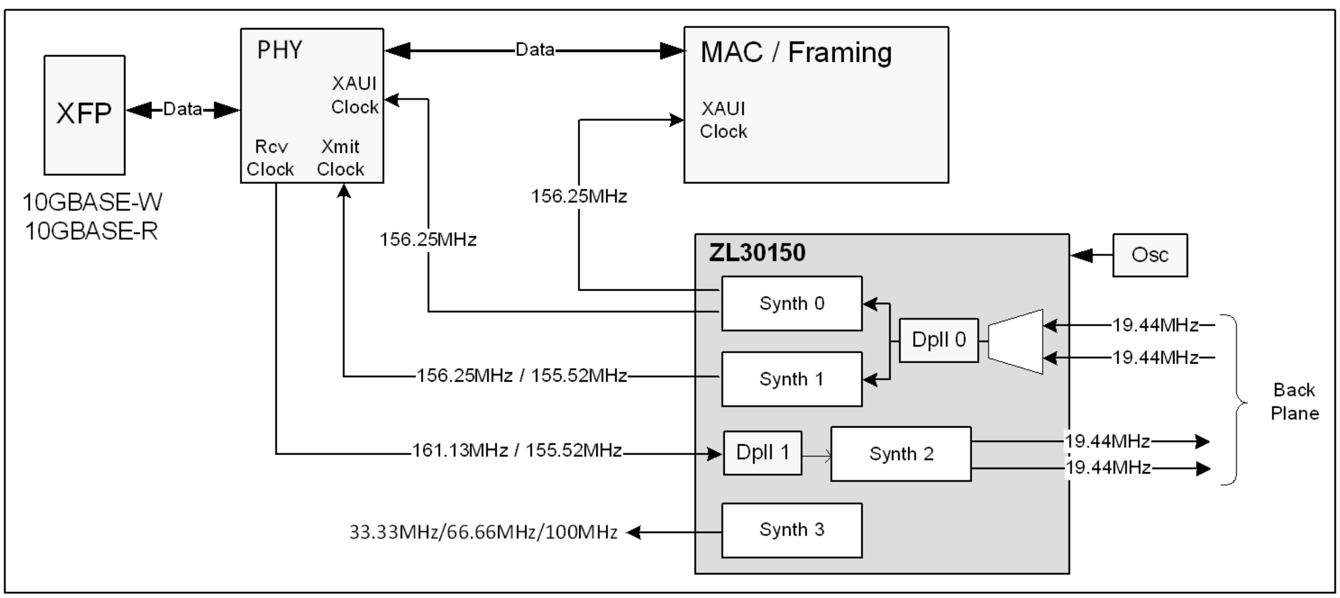

Figure 3 - Application Diagram: Frequency Translation for 10GBASE-W / 10GBASE-R Synchronous Ethernet

4.0 Functional Description

The functional block diagram of the device is shown in Figure 1. The ZL30150 is a Two channel clock translator/NCO that can be configured by any of the following methods; power-up with its default configuration; power-up with a custom OTP (One Time Programmable) configuration; after power-up it can be dynamically configured via the SPI/I2C port. Configurations set via the SPI/I2C are volatile and will need to be rewritten if the device is reset or powered-down. The SPI/I2C port is also used to access the status registers. The ZL30150's detailed operation is described in the following sections.

4.1 Input Sources

The device has 5 input sources: 4 input references (single ended or differential) and one oscillator clock source (oscillator or xtal).

The device master clock frequency is configured on reset via external voltage levels on GPIO[1:0] pins. The recommended frequency of the master clock is 24.576 MHz.

The device synchronizes (locks) to any input reference which is a 8 kHz multiple, or it synchronizes (locks) to any input reference which is an (M/N x 8 kHz) multiple (FEC rate converted) where M and N are 16 bits wide.

The device input reference frequency is programmed during initialization, change of input reference frequency can be supported if DPLL was forced in to Holdover mode before a frequency change.

The device accepts an input reference with maximum frequency of 177.5 MHz through single ended LVCMOS input (or 750 MHz frequency through differential inputs) and a minimum frequency of 8 kHz. The device synchronizes (locks) to any Telecom or SyncE input reference.

If the frequency of an input reference exceeds 400 MHz, the reference will need to be divided by 2 before being fed to DPLL. Division by 2 can be set by programming ref_config register at address 0x0A.

4.2 Input Reference Monitoring

The input references are monitored by reference monitor schemes, independent for each reference. They indicate abnormal behavior of the reference signal, for example; drift from its nominal frequency or excessive jitter.

- **Loss of Signal Monitor (LOS)**: LOS is an external signal, fed to one of ZL30150 GPIO pins. LOS is typically generated by a PHY device whose recovered clock is fed to one of ZL30150 reference inputs. PHY device will generate LOS signal when it cannot reliably extract the clock from the line. User can set one of GPIO pins as LOS input by programming corresponding GPIO register.
- **Coarse Frequency Monitor (CFM)**: This circuit monitors the reference over a short time interval. It detects large frequency irregularities (larger or equal than 0.1%).
- **Single Cycle Monitor (SCM)**: This detector checks the period of a single clock cycle to detect large phase hits or the complete loss of the clock.
- **Guard Soak Timer (GST):** Timer associated with the CFM and SCM modules to disqualify the reference input signal (see Table 2)

The monitor failure indicators are flagged in the status registers and have associated mask bits, as follows:

- Reference Fail Mask: Ref0FailMask<3:0>, Ref1FailMask<3:0>, Ref2FailMask<3:0>, Ref3FailMask<3:0>: these mask bits masks the failure indicator on corresponding fail pins/bits.
- Reference Switching Mask for the current active (locked to) reference: RefSwMask<3:0> these mask bits masks the failure indicators that are used in the automatic reference switching state machine independently for each supported DPLL.
- Holdover Mask for the current active (locked to) reference: HOMask<3:0>, these mask bits masks the failure indicators that are used to go into auto-holdover independently for each supported DPLL.

- MSB bit for CFM and LSB bit for GST

The single cycle and coarse monitor failure flags feed a timer (Guard Soak Timer) that disqualifies the reference input signal when the failures are present for more than the period of time defined in Table 2.

Guard Soak Timer Control bits in control register	Time to disqualify a reference	Notes
00	minimum delay possible	
01	10 ms	
10	50 ms	default value
11	2.5 s	

Table 2 - Guard Soak Time To Disqualify a Reference

The Guard Soak Timer that is used for the CFM and SCM modules has a built-in decay time hysteresis according to Table 3 (Timer to Qualify a reference) to prevent flickering of status bits at the threshold boundaries.

The Timer to Qualify a reference is a multiple of the Guard Soak Timer. Table 3 shows the multiplication factor to multiply the Guard Soak Timer to calculate the time to qualify a reference.

Control bits to control the Timer to qualify a reference	Multiples of the Guard Soak Time to qualify a reference	Notes
00	2	
01	4	Default value
10	16	
11	32	

Table 3 - Guard Soak Time To Qualify a Reference

When a GPIO pin is used as a reference fail indicator, it indicates a valid reference if:

- The SCM does not detect phase hits, nor complete loss of clock or Ref<i>FailMask<0> is at logic “0”
- The CFM does not detect phase irregularity or Ref<i>FailMask<1> is at logic “0”
- The Guard Soak Time is triggered or Ref<i>FailMask<2> is at logic “0”

4.3 Digital Phase Locked Loop (DPLL)

The device supports two independent digital PLL modules. Initial default configuration defines two active DPLLs.

4.3.1 DPLL General Characteristics

Pull-in Hold-in range

The DPLL supports pull-in/hold-in of +/-52 ppm, +/-130 ppm, +/-400 ppm or +/-3900 ppm.

DPLL bandwidth (jitter/wander transfer)

The DPLL supports the following first order filtering cut-off frequencies:14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz and 896 Hz. DPLL bandwidth is determined during the initialization. Dynamic change of DPLL bandwidth is supported. When changing the bandwidth dynamically, it is recommended to put DPLL to the Holdover mode first and then to change the bandwidth. After the bandwidth has been changed, the DPLL should be set to the Normal mode.

The DPLL locks to an input reference and provides stable low jitter output clock if the selected loop bandwidth is less than 1/30th the input reference frequency. As an example, a 19.44 MHz reference could deploy a bandwidth up to 896 Hz and for 8 kHz reference we recommend a maximum loop bandwidth of 56 Hz.

Jitter/Wander Generation

Jitter and wander generation performances are provided in section 10.0, “Performance Characterization“.

Phase Transients

On reference switch with phase tracking active (i.e., TIE clear active or glitch-less reference switching), the DPLL transitions the phase of the output smoothly, limited by the selected loop bandwidth and by the selected phase slope limit.

The Microsemi device offers the following phase slope limiting options: 61 usec/sec, 7.5 usec/sec, 0.885 usec/sec or unlimited.

Holdover Stability

DPLL initial holdover accuracy is better than 50 ppb.

Input Tolerance Criteria

Input tolerance indicates that the device tolerates certain jitter, wander and phase transients at its input reference while maintaining outputs within an expected performance and without experiencing any alarms, reference switching or holdover conditions. Input tolerance is associated with input reference source characteristics and the standards associated with input reference type.

DPLL Monitoring

The DPLL provides lock and holdover indicators using the default lock indicator conditions.

The lock time is dependent on employed loop bandwidth. The device has a lock time of less than 1 sec for all available DPLL loop bandwidth selections.

4.3.2 DPLL States

The device DPLL(s) supports three DPLL states: Free-run, Normal (Locked) and Holdover. The Holdover and Free-run states are used to cope with reference impairments.

Each of these modes have a corresponding state in the internal State Machine described as follows:

Freerun State: the Freerun state is entered when synchronization to the reference is not required or is not possible. Typically this occurs immediately following system power-up. In the Freerun State, the device provides timing and synchronization signals which are based on the master clock frequency (supplied to osci pin) only, and are not synchronized to the reference input signals. The freerun accuracy of the output clock is equal to the accuracy of the master clock (osci). So if a ±20 ppm freerun output clock is required, the master clock must also be ±20 ppm.

Holdover State: the Holdover State is typically entered when input reference is temporarily disrupted. In the Holdover State, the device provides output clocks which are not locked to an external reference signal, but are based on storage techniques. The storage value is determined while the device is in Normal Mode and locked to an external reference signal. Initial holdover accuracy is a function of DPLL while holdover drift is reliant on the drift of the master clock (osci).

Normal State: the Normal State is entered when a valid reference clock is available for synchronization. In the Normal State the device provides output clocks which are synchronized to one of the available 4 input references. From a reset condition - if a valid input reference is available - the device takes less than a second (lock time) to output signals which are synchronized (phase and frequency locked) to the reference input.

4.3.3 DPLL Rate Conversion Function and FEC Support

The DPLL supports rate conversion with a 16 bit forward divider and a 16 bit feedback divider.

The DPLL provides up scaling and down scaling functions.

The DPLL has the ability to switch from normal rate (before FEC is negotiated) to FEC rate and vice versa.

The DPLL supports simple rate conversion (i.e., take in 19.44 MHz and create 255/238 FEC SONET clock of 666.51 MHz), and supports double rate conversion (i.e., take in 19.44 MHz, create FEC 10 GbE clock of 644.5313, which is 66/64 rate converted 625 MHz, or create 690.5692 which is 255/238X66/64 rate converted 625 MHz)

The following is just an example of the frequencies that can be supported (many more frequencies can be supported):

- **GbE:**
  - 25 MHz
  - 125 MHz
- **XAUI (chip to chip interface, which is a common chassis to chassis interface)**:
  - 156.25 MHz or x2 or x4 version
- **OC-192/STM-64:**
  - 155.52 MHz or x2 or x4 version
  - 155.52 MHz x 255/237 (standard EFEC for long reach) or x2 or x4 version
  - 155.52 MHz x 255/238 (standard GFEC for long reach) or x2 or x4 version
- **10 GbE:**
  - 156.25 MHz which is 125 MHz x 10/8 or x2 or x4 version
  - 155.52 MHz x 66/64 or x2 or x4 version
  - Long reach 10 GE might require the following frequencies with simple rate conversion: (156.25 MHz x 255/237) and (156.25 MHz x 255/238).
  - The following frequencies with double rate conversion: (155.52 MHz x 66/64 x 255/237) or (155.52 MHz x 66/64 x 255/238) and (156.25 MHz x 66/64 x 255/238) or (156.25 MHz x 66/64 x 255/238). Also, user can use x2 or x4 version of the listed frequencies.

Application Note ZLAN-267 explains how to generate the most common frequencies.

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4.3.4 DPLL Input to Output and Output to Output Phase Alignment

Techniques offered for Phase Alignment

When the output clock is locked to a jitter free and wander free input clock, input to output latency is expected to have a typical error of 0 nsec.

The coarse and fine phase adjustments allow for input to output and output to output latency corrections to compensate for PCB load delay, as detailed in 4.7, “Output Drivers“.

The PLL architecture allows for implementation of an external feedback (external output clock phase sense) of the PLL path that is fed through one of the available references (REF 0, 1, 2 or 3). Such external feedback would allow for dynamic changes of PCB routing and external buffer delay caused by changes in temperature.

External feedback cannot be used if synthesizer in the feedback path is programmed such that
Bs*Ks*Ms/Ns = 65,536,000.

4.4 Frequency Synthesis Engines

The ultra low jitter frequency synthesis engine can generate output clocks which meet the jitter generation requirements detailed in section 10.0, “Performance Characterization“.

The frequency synthesis engine’s APLL requires an external RC loop filter as described in Figure 18

The frequency synthesis engines can generate any clock which is (M/N X 8 kHz) multiple (FEC rate converted clock). The M and N are 16 bits wide.

All synthesizers can be locked to either of two DPLLs and two NCOs.

4.4.1 Use of synthesis engines in NCO mode

The device has four NCOs. DPLL0 and DPLL1 can alternatively be used as NCO0 and NCO1 plus two dedicated NCOs: NCO2 and NCO3. Only two NCOs can be used at the time. For example if DPLL0 and DPLL1 are used in PLL mode NCO2 and NCO3 can be use. However, if DPLL0 and DPLL1 are both used as NCOs, NCO2 and NCO3 are not available. Two active NCOs are enabled and selected by programming registers NCO_a_adjust_en and NCO_b_adjust_en at addresses 0xEC and 0xF1. It should be noted that two active NCOs (a and b) should never be set to point to the same DPLL/NCO.

NCOs output frequencies can be tuned with uP via SPI/I2C port. Selected NCO center frequency is first set by programming B, K, M and N registers of the synthesizer fed by NCO and then NCO frequency can be fine tuned by programming fine frequency offset registers at addresses 0xED:0xF0 and 0xF2:0xF5. The fine frequency tuning can adjust output frequency up to +/-0.5% off nominal with 0.24 ppb steps.

4.5 Dividers and Skew Management

The device has 4 independent dividers associated with each frequency synthesis engine.

The divider engines associated with the high performance differential outputs generate output clocks between 1 Hz and 750 MHz with 50% duty cycle. The other divider engines generate output clocks between 1 Hz and 177.5 MHz for high performance LVCMOS outputs and 160 MHz for single ended configurable outputs with 50% duty cycle. When configurable outputs are in differential mode, the maximum frequency is 350 MHz.

The divider modules generating the single ended output clocks provides the ability to manage the phase skew of the output clock by a coarse step equal to the internal high speed clock period.

The single ended generated output clocks can be stopped either on rising or falling edge (programmed through serial interface or GPIO).

The device can be configured to adjust the phase skew of single ended clocks in steps of sub high speed synthesizer clock cycle period.

4.6 Output Multiplexer

Figure 5 shows the multiplexing configuration that is supported.

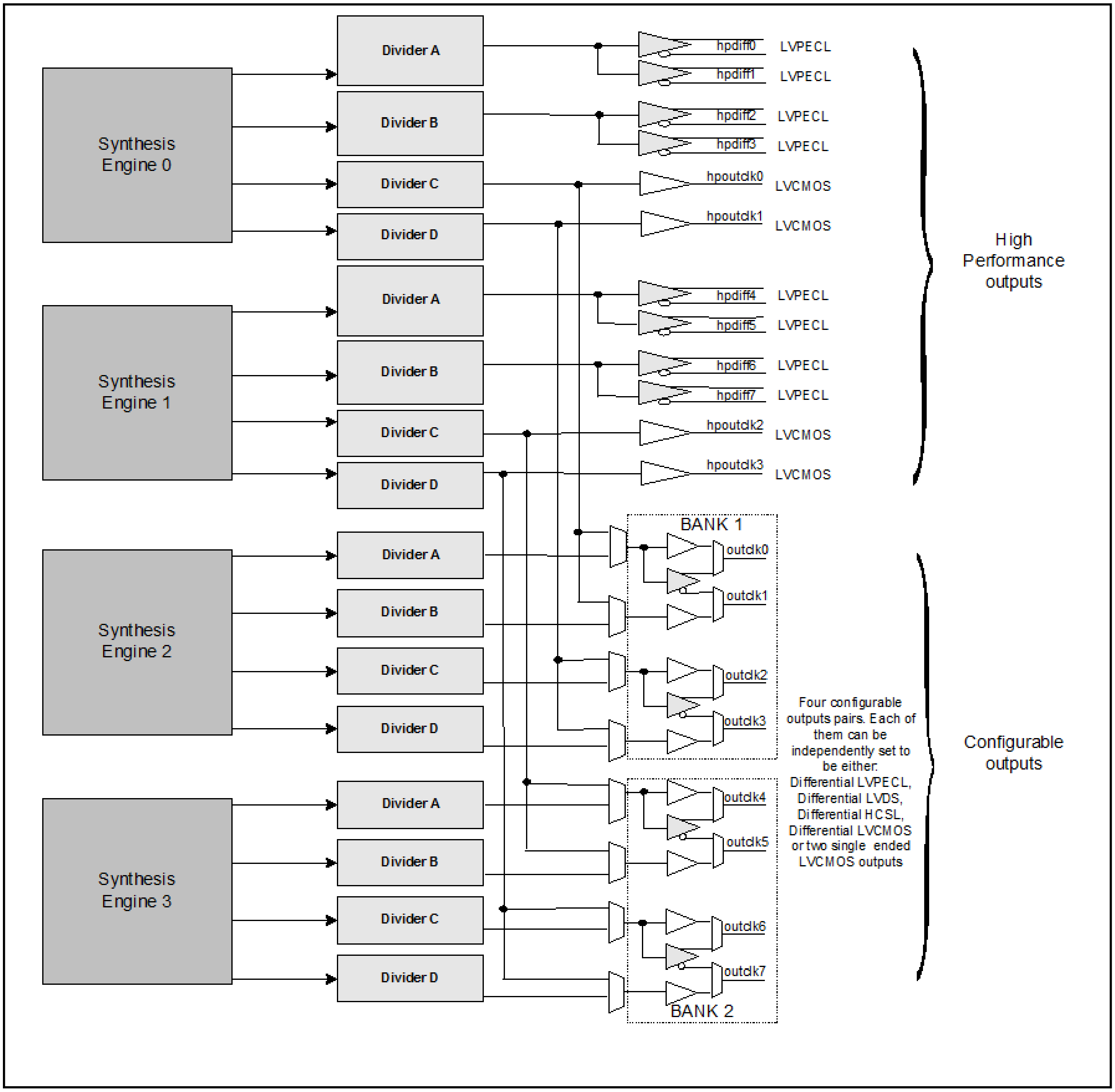


Figure 5 - Output Clocks Muxing Configuration

4.7 Output Drivers

The device has 8 high performance (HP) differential (LVPECL) outputs.

The device has 4 high performance (HP) single ended (LVCMOS) outputs.

The device also has 2 banks of configurable output drivers. Each bank can be set as a 4 single ended drivers (LVCMOS) or as a 2 differential output drivers (LVPECL, LVDS, or HCSL). Each output bank has its own power supply pins, such that each bank of 4 single ended drivers can be set to operate in 3.3 V, 2.5 V, 1.8 V or 1.5 V mode.

High Performance (HP) single ended driver (LVCMOS) supports the jitter specification detailed in section 10.0, “Performance Characterization“ and a maximum speed of 177.5 MHz.

The high performance (HP) differential driver (LVPECL) supports the jitter specification detailed in section 10.0, “Performance Characterization“ and a maximum speed of 750 MHz.

LVPECL outputs should be terminated as shown in Figure 6. Terminating resistors provide 50 Ω equivalent Thevenin termination as well as biasing for the output LVPECL driver. Terminating resistors should be placed as close as possible to input pins of the LVPECL receiver. If the LVPECL receiver has internal biasing then AC coupling capacitors should be added.

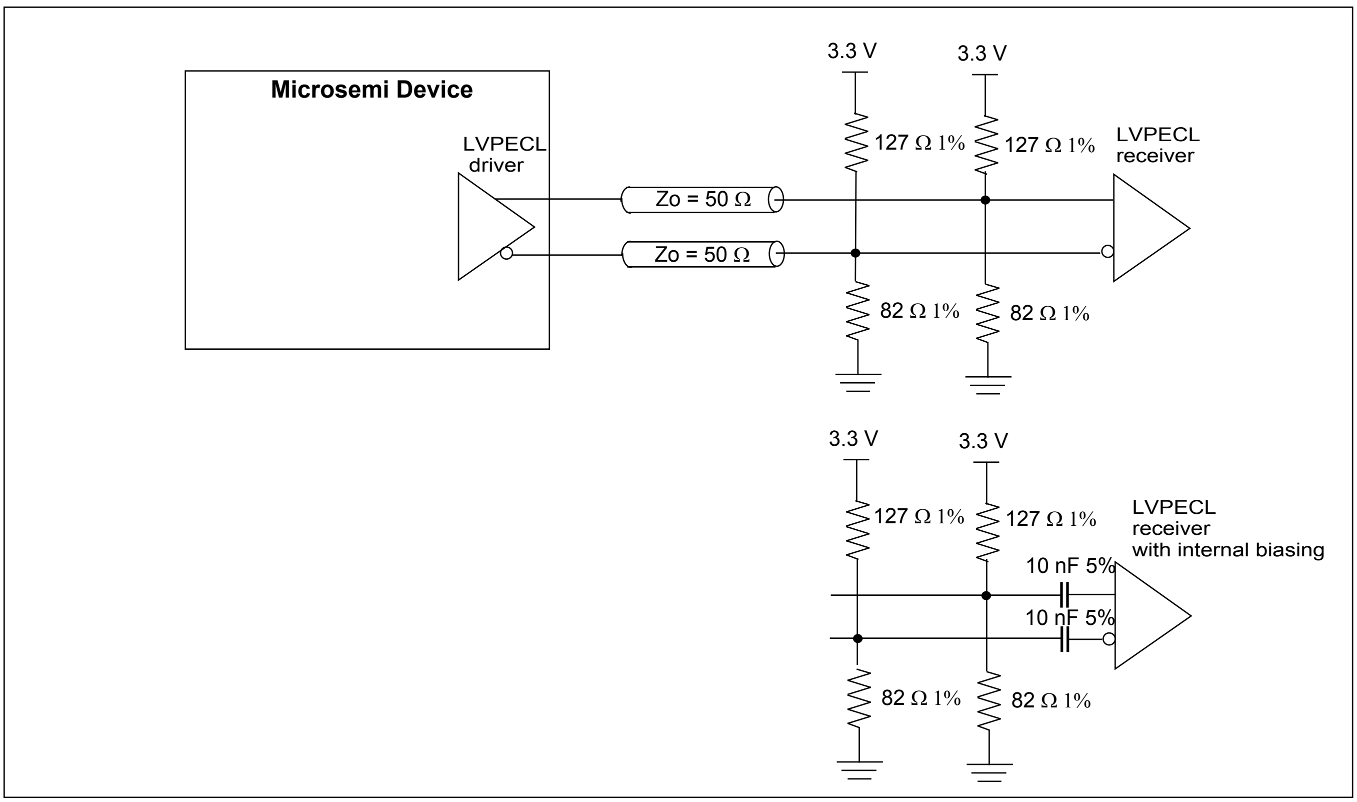


Figure 6 - Terminating LVPECL Outputs

If the transmission line is required to be AC coupled then the termination shown in Figure 7 should be implemented. 200 Ω resistors are used to provide DC biasing for LVPECL driver. Both AC coupling capacitor and biasing resistors should be placed as close as possible to output pins.

Thevenin termination (127 Ω and 82 Ω resistor) provide 50 Ω termination as well as biasing of the input LVPECL receiver. If the LVPECL receiver has internal DC biasing then the line should be terminated with 100 Ω termination resistor between positive and negative input. In both cases termination resistors should be places as close as possible to the LVPECL receiver pins. Some LVPECL receivers have internal biasing and termination. In this case no external termination should be present.

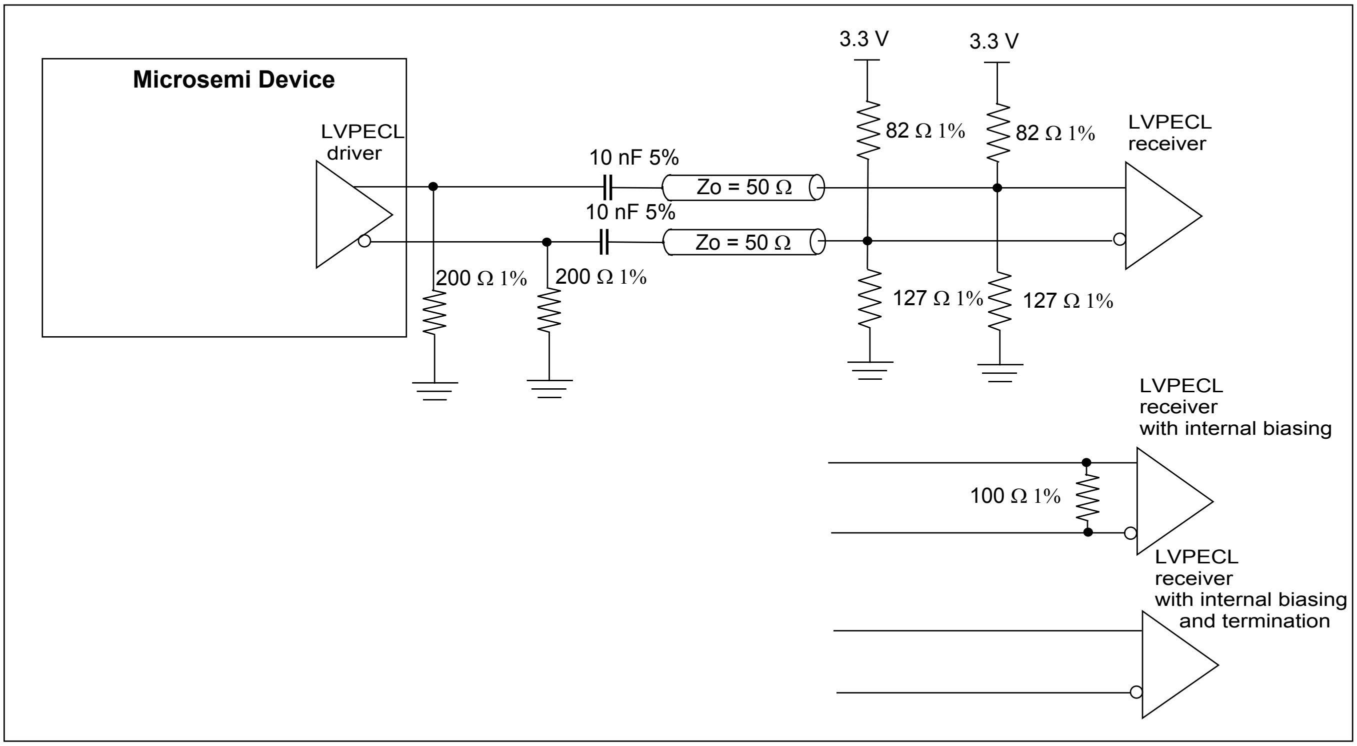


Figure 7 - Terminating AC Coupled LVPECL Outputs

High performance LVCMOS outputs (hpoutclkx) should be terminated at the source with 22 Ω resistor as shown in Figure 8. The same type of termination should be used for configurable outputs when they are set to be LVCMOS.

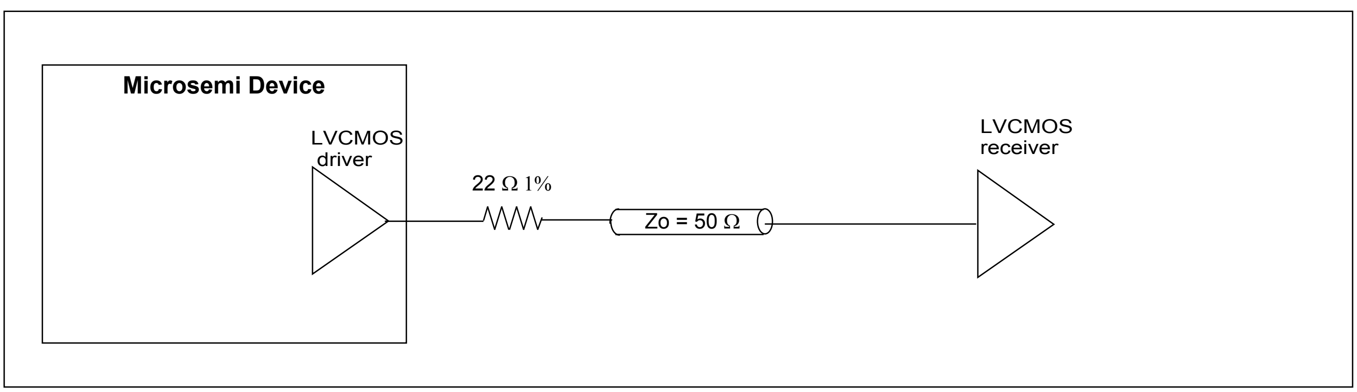


Figure 8 - Terminating LVCMOS Outputs

If the differential output drivers are programmed to be LVDS the termination in Figure 9 should be used.

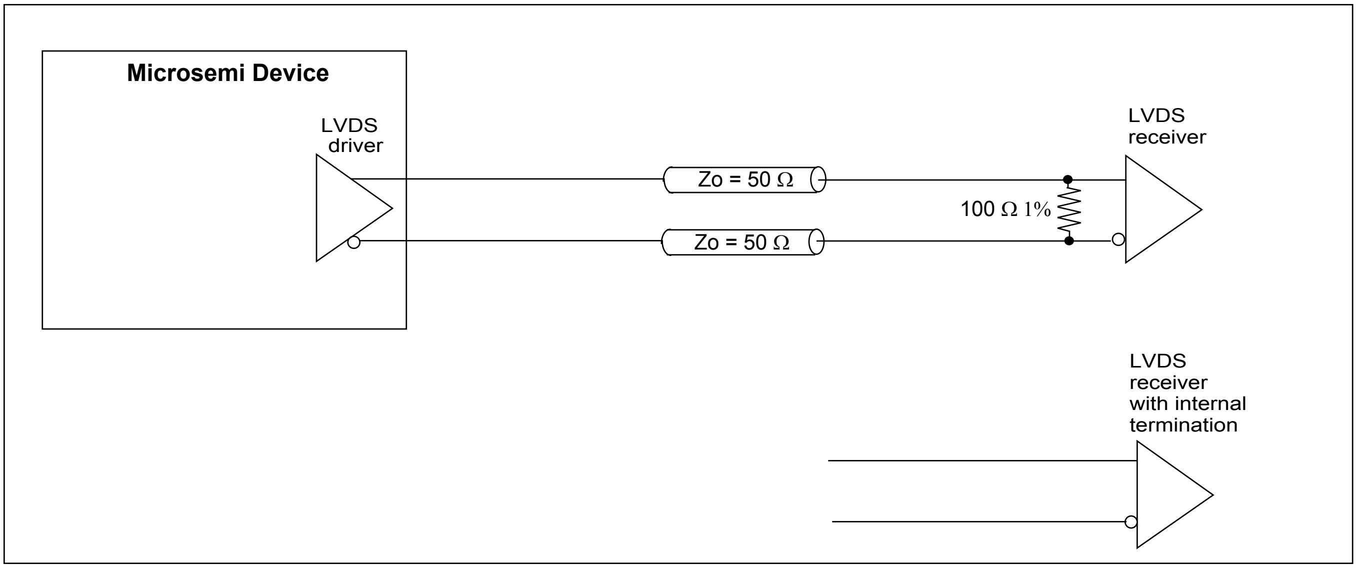


Figure 9 - Terminating LVDS Outputs

When configurable outputs are set to be HCSL, the termination shown in Figure 10 should be used.

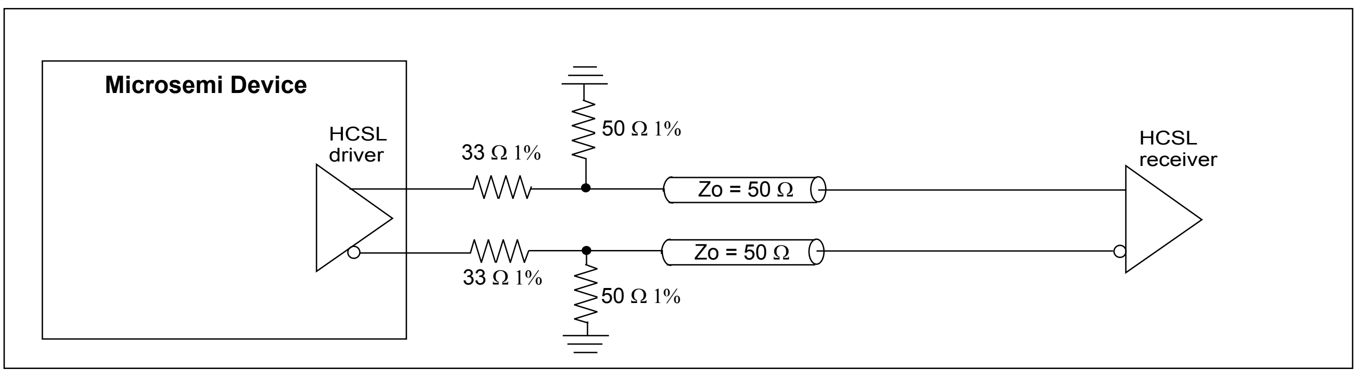


Figure 10 - Terminating HCSL Outputs

4.7.1 Configurable Single Ended Driver - Slew Rate Control

Slew rate of configurable single ended drivers can be programmed to be either fast or medium.

Fast slew rate should be used to:

- Buffer high speed single ended (CMOS) output clock (up to 160 MHz) and/or
- Buffer single ended (CMOS) output clock on a large output load (up to 30 pf)
- Provide rail to rail single ended output clock for any selection of output drive supply voltage (1.5, 1.8, 2.5, 3.3 Volt)

Medium slew rate should be used to:

- Maintain limited output clock ringing and PCB output clocks cross modulation when driving low speed output clock or when small load is present at the output

Each of the available single ended configurable outputs of the device has 2 available slew rate control limits.These limits are user selectable based on: output clock speed, expected output load or output supply voltage. Table 4 details the limits and the expected output clock slew rates.

	Slew Rate for Fast Slew		**Slew Rate for Medium Slew**	
Expected Load	10 pF	20 pF	10 pF	20 pF
Output Clock 80 MHz or less	1.62 V/ns	1.47 V/ns	0.93 V/ns	0.96 V/ns
Output Clock 160 MHz or less	1.58 V/ns	1.38 V/ns	1.09 V/ns	1.08 V/ns

Table 4 - Slew Rate Control Limits Versus Output Clock Slew Rates

4.8 Input Buffers

ZL30150 has four reference inputs ref[3:0]_p/ref[3:0]_n that can work as either single ended or differential. By default ref0 is differential and the others are single ended. This can be changed by programming ref_config register at address 0x0A.

Input frequency range for differential inputs is: 8 kHz to 750 MHz; for single ended inputs is: 8 kHz to 177.5 MHz.

Differential reference inputs need to be properly terminated and biased as shown in Figure 11 and Figure 12 for LVPECL and Figure 13 and Figure 14 for LVDS drivers. When terminating LVPECL signal, it is necessary either to adjust termination resistors for DC coupling or to AC couple the LVPECL driver because ZL30150 differential inputs have different common mode (bias) voltage than LVPECL receivers. Thevenin termination (182 Ω and 68 Ω resistors) provide 50 ohm equivalent termination as well as biasing of the input buffer for DC coupled line. For AC coupled line, Thevenin termination with 127 Ω and 82 Ω resistors should be used as shown in Figure 12. The value of the AC coupling capacitors will depend on the minimum reference clock frequency. The value of 10 nF is good for input clock frequencies above 100 MHz. For lower clock frequencies capacitor values will have to be increased.

Terminations for DC and AC coupled LVDS line are shown in Figure 13 and Figure 14 respectively. Differential input biasing is provided by LVDS driver in case of DC coupling (Figure 13), whereas for AC coupling (Figure 14) biasing is generated by 12 kΩ and 8.2 kΩ resistors. In both cases, the line is terminated with 100 Ω.resistor.

For single ended CMOS inputs, refx_n input needs to be connected to the ground as shown in Figure 15. The value of series termination resistor will depend on CMOS output driver but the most common values are 33 Ω and 22 Ω.

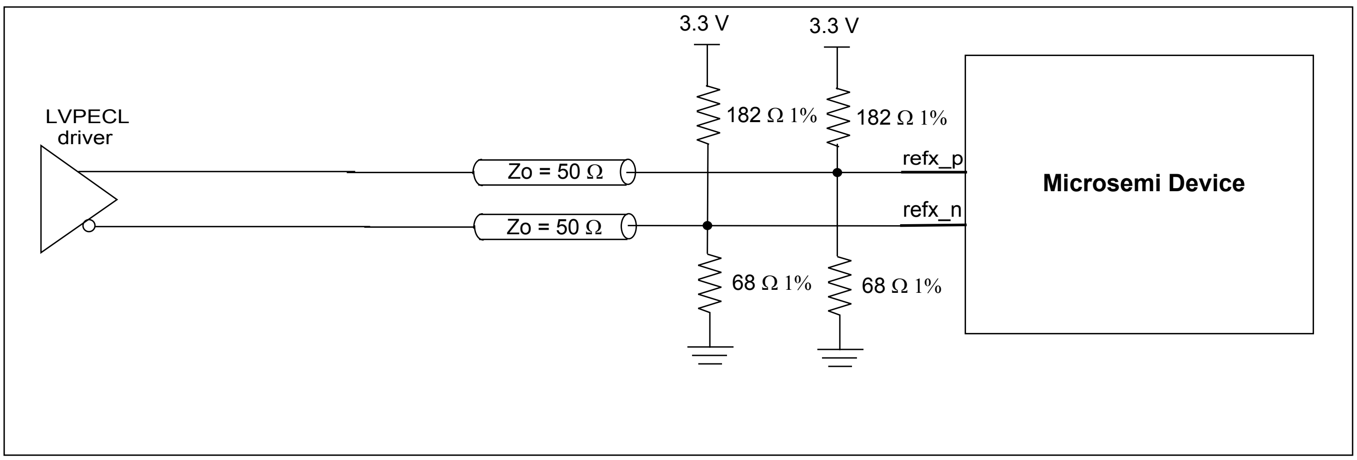


Figure 11 - Differential DC Coupled LVPECL Termination

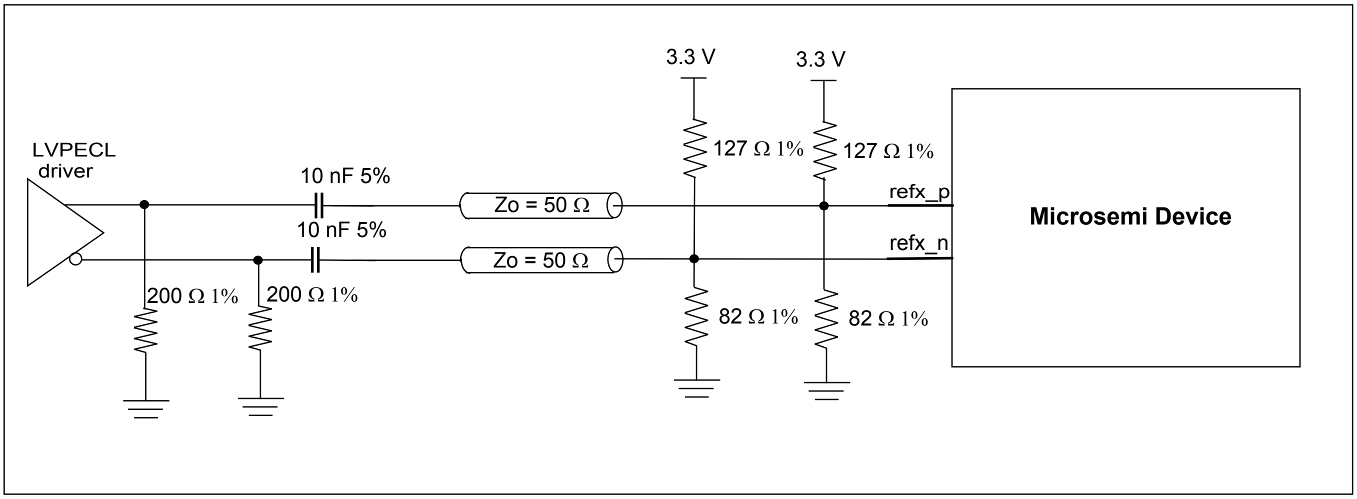


Figure 12 - Differential AC Coupled LVPECL Termination

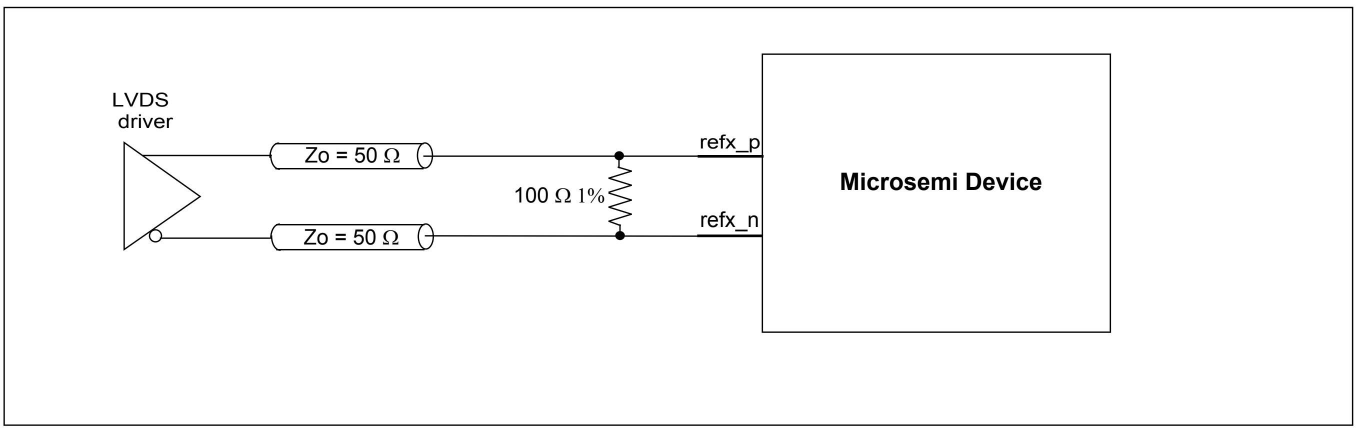


Figure 13 - Differential DC Coupled LVDS Termination

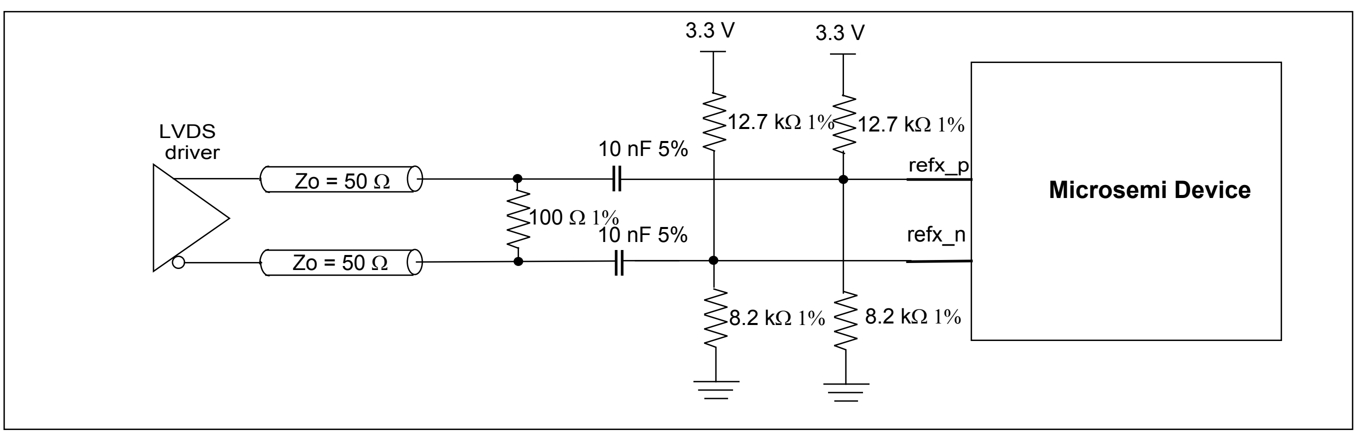


Figure 14 - Differential AC Coupled LVDS Termination

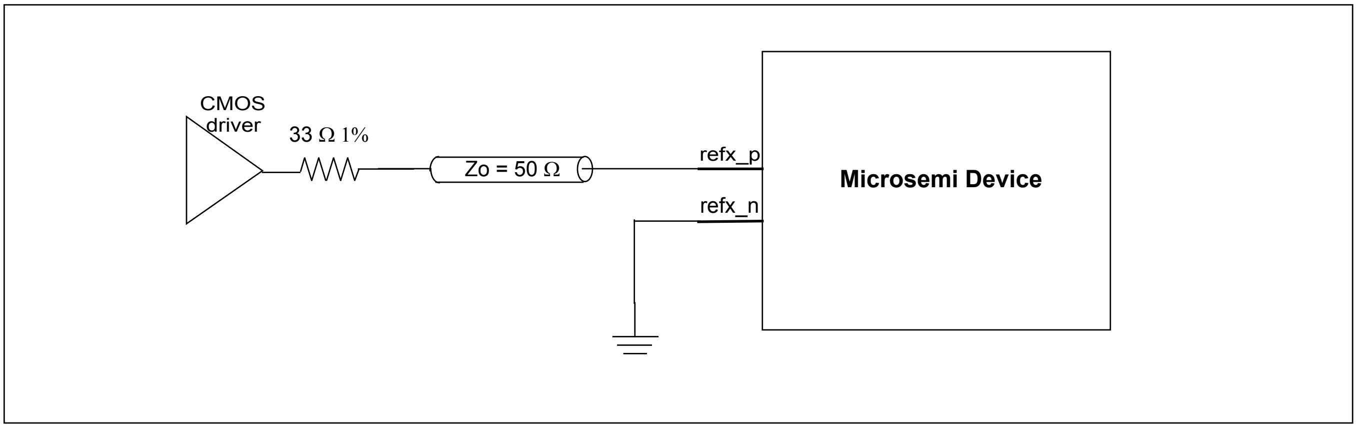


Figure 15 - Single Ended CMOS Termination

4.9 Master Clock Interface

The master oscillator determines the DPLL's free-run frequency accuracy and holdover stability. The reference monitor circuitry also uses this frequency as its point of reference (0 ppm) when making frequency measurements. The master clock interface was designed to accept either a free-running clock oscillator (XO) or a crystal (XTAL). Refer to application note ZLAN-68 for a list of recommended clock oscillators.

4.10 Clock Oscillator

When using a clock oscillator as the master timing source, connect the oscillator's output clock to the **osci** pin as shown in Figure 16. The connection to osci should be direct and not AC coupled. The **osco** pin must be left unconnected.

When using crystal resonator as the master timing source, connect crystal between **osci** and **osco** pins as shown in Figure 16. Crystal should have bias resistor of 1 MΩ and load capacitances C1 and C2. Value of load capacitances is dependent on crystal and should be as per crystal datasheet. Crystal should be a fundamental mode type -- not an overtone. See ZLAN-68 for crystal recommendation.

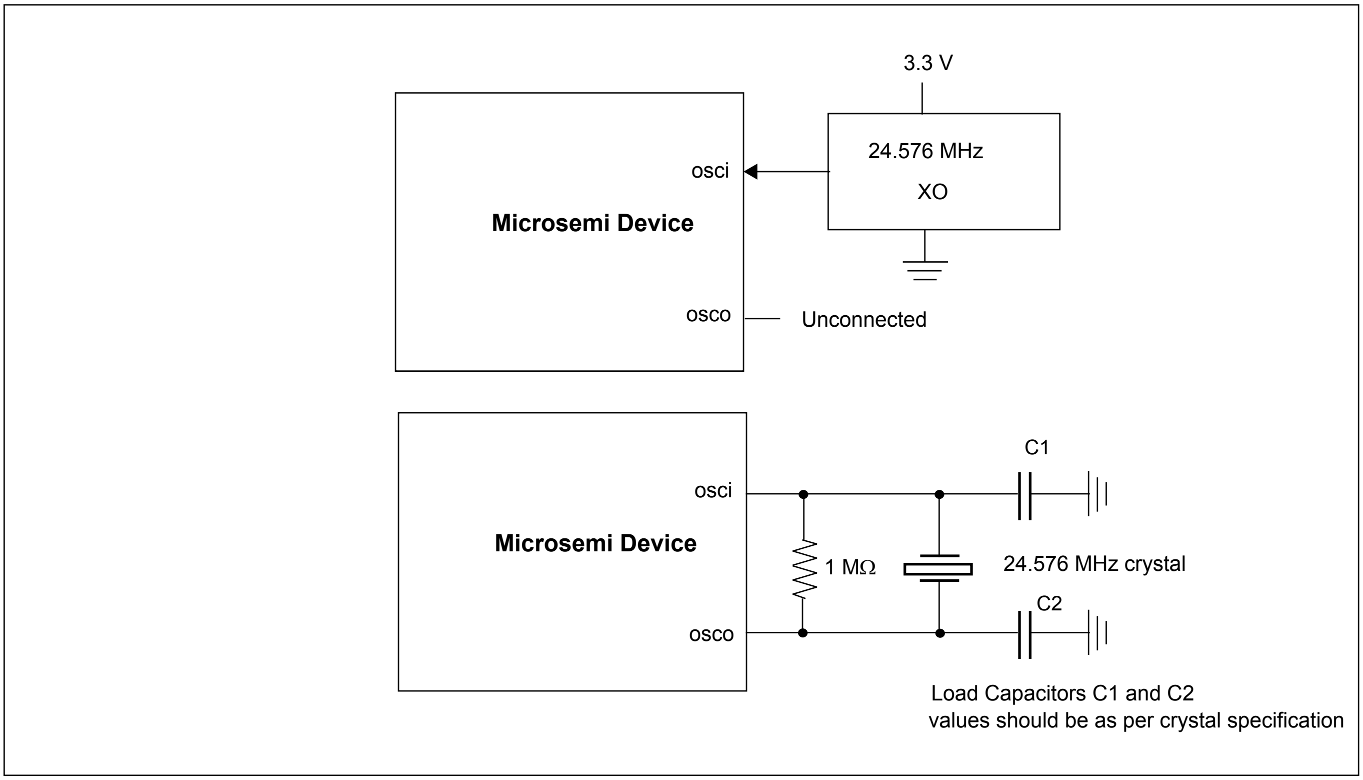


Figure 16 - Clock Oscillator Circuit

The device internal system clocks are generated off the device master clock input (Oscillator or a crystal employing an on-chip buffer/driver). The master clock selection is done at start-up using the available GPIO pins, right after pwr_b get de-asserted. The GPIO[1:0] pins need to be held high for 55 ms after the de-assertion of pwr_b, after which time they can be released and used as any other GPIO. Alternatively, these pins can be pulled high with 1 kΩ resistors.

GPIO [1:0]	Master Clock Frequency
00	reserved
01	reserved
10	reserved
11	24.576 MHz

Table 5 - Master Clock Frequency Selection

4.11 Power Up/Down Sequence

The 3.3 V supply should be powered before or simultaneously with the 1.8 V supply. The 1.8 V supply must never be greater than the 3.3 V supply by more than 0.3 V. The 1.5V/1.8V/2.5V/3.3V configurable output supply must never be greater than the 3.3V supply by more than 0.3V.

The power-down sequence is less critical, however it should be performed in the reverse order to reduce transient currents that consume power.

4.12 Power Supply Filtering

Jitter levels on the output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins. For recommended common layout practices, refer to Microsemi Application Note ZLAN-269.

4.13 Reset and Configuration Circuit

To ensure proper operation, the device must be reset by holding the pwr_b pin low for at least 2 ms after power-up when 3.3V and 1.8V supplies are stable. Following reset, the device will operate under specified default settings.

The reset pin can be controlled with on-board system reset circuitry or by using a stand-alone power-up reset circuit as shown in Figure 17. This circuit provides approximately 2 ms of reset low time. The pwr_b input has Schmidt trigger properties to prevent level bouncing.

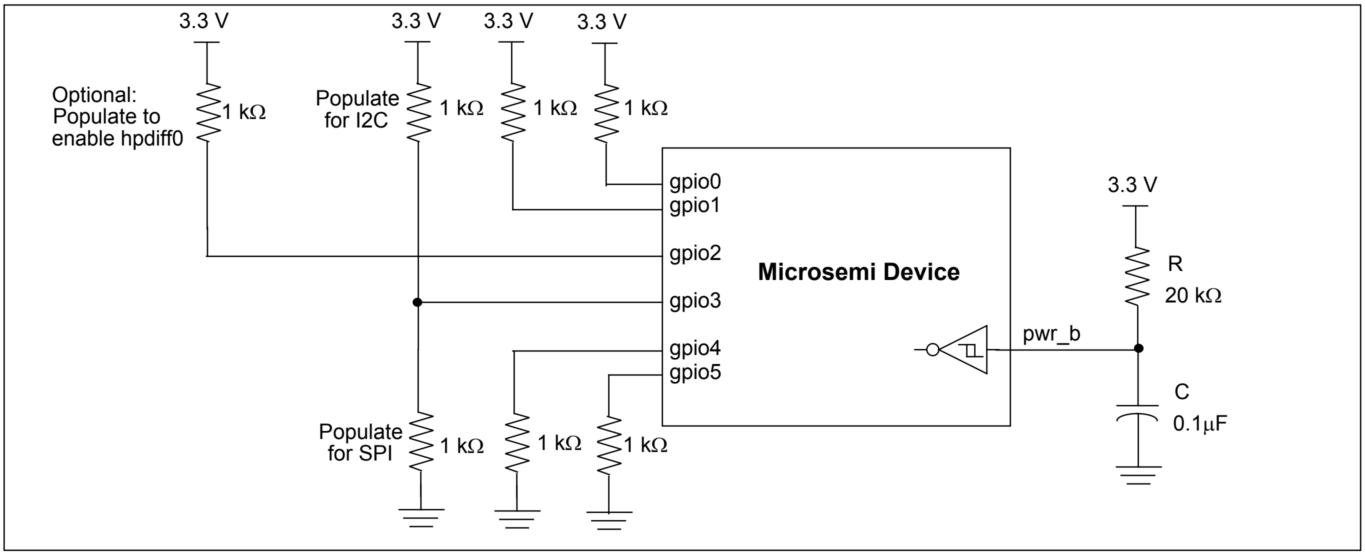


Figure 17 - Typical Power-Up Reset and Configuration Circuit

General purpose pins gpio[0,1,3,4,5] are used to configure device on the power up. They have to be pulled up/down with 1 kΩ resistors as shown in Figure 17 or they can be pulsed low/high during the pwr_b low pulse and kept at the same level for at least 55 ms after pwr_b goes high. After 55 ms they can be released and used as general purpose I/O as described in Section 6.0.

By default all outputs are disabled to allow user first to program required frequencies for different outputs and then to enable corresponding outputs. During the prototype phase, hardware designer can verity if the device is working properly even before software driver is implemented just by pulling up gpio2 pin which enables hpdiff0 output (generates 622.08 MHz by default).

4.14 Ultra Low Jitter Synthesizer Filter Components and Recommended Layout

The APLL for the ultra low jitter synthesizer in the Microsemi device uses external components to help optimize its loop bandwidth. For optimal jitter performance, the following component values are recommended:

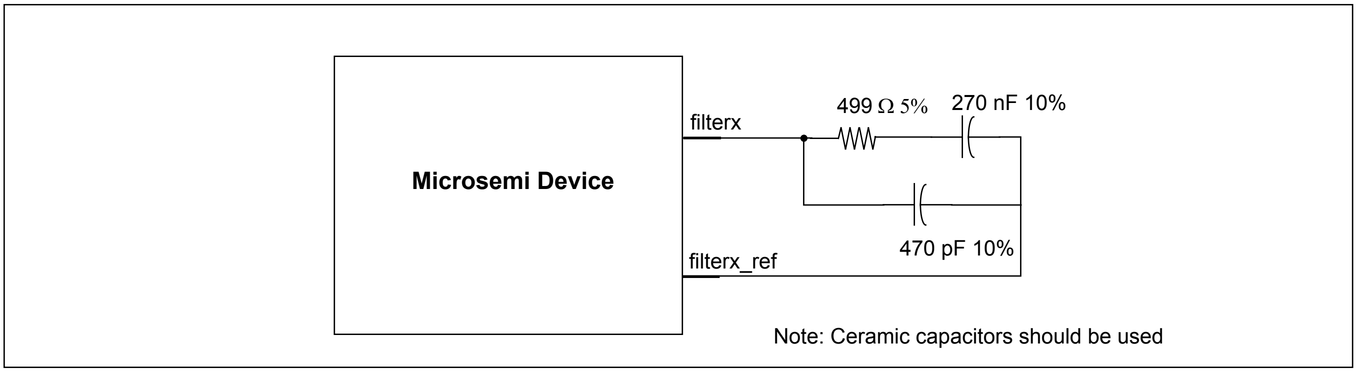


Figure 18 - APLL Filter Component Values

Recommended layout for loop filters is shown in Figure 19:

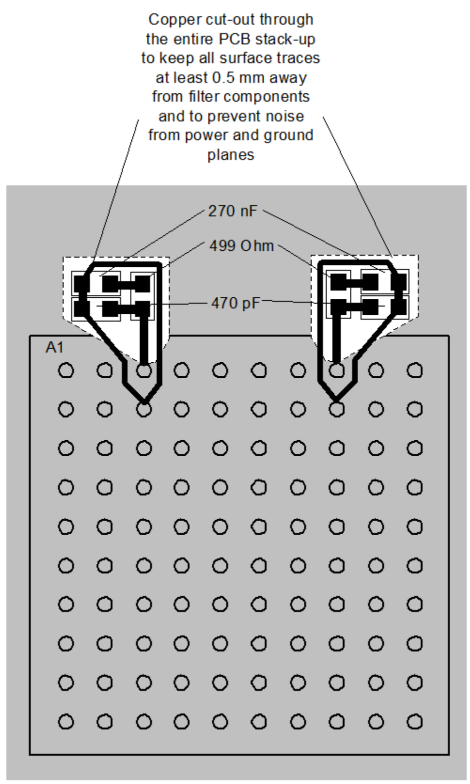


Figure 19 - Recommended Layout for Loop Filters

5.0 Configuration and Control

The ZL30150 configuration is composed of 253 x 8 bits. The configuration registers are assigned their values by any of the following three methods:

1) Default configuration
2) Custom OTP (One Time Programmable) configuration
3) SPI/I2C configuration

5.1 Custom OTP Configuration

At power-up the device sets its configuration registers to the user defined custom configuration values stored in it's OTP (One Time Programmable). Custom configurations can be generated using Microsemi's Clockcenter GUI software (ZLS30CLKCTR). For custom configured devices contact your local Microsemi Field Applications Engineer or Sales Manager.

5.2 GPIO Configuration and Programmability

The device GPIO is mapped by the SPI/I2C programmability. The following is an example of control and status signals that can be supported:

- DPLL lock indicators
- DPLL holdover indicators
- Reference 0, 1, 2, and 3 fail indicators
- Reference select control or monitor
- Differential output clock enable (per output or as a bank of 2 or 4 outputs)
- Host Interrupt Output: flags changes of device status prompting the processor to read the enabled interrupt service registers (ISR).
- Output clock stop/start

The following table defines the function of the GPIO pin when configured as a control pin. Configuring the value in bit 6:0 in GPIO configuration registers enables the stated function.

Value	Name	Description
Default		
0x00	Default	GPIO defined as an input. No function assigned.
Input References		
0x10	Ref0 external LOS signal	Ref0 external Loss Of Signal (LOS) - indicator to DPLLs that Ref0 has failed. Internally in the DPLLs this signal is used for reference monitor indicator, reference switching or holdover entering and for ISR generation.
0x14	Ref1 external LOS signal	Same description as REF0 external LOS
0x18	Ref2 external LOS signal	Same description as REF0 external LOS
0x1C	Ref3 external LOS signal	Same description as REF0 external LOS
DPLL		
0x20	DPLL0 Time Interval Error (TIE) clear enable	This signal is OR-ed with the 'DPLL0 TIE clear enable' bit of the 'DPLL control' register. Functionality of this signal is explained in the 'DPLL control' register.

Value	Name	Description
0x28	DPLL1 Time Interval Error (TIE) clear enable	Same description as DPLL0 TIE clear enable
Synthesizer Post Divider		
0x44	Stop output clock from Synthesizer0 Post Divider C bit1	This signal is OR-ed with the 'Syntheizer0 Post Divider C stop clock' bit1 in the 'Synthesizer0 and Synthesizer1 Post Dividers stop clock' register.
0x45	Stop output clock from Synthesizer0 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x46	Stop output clock from Synthesizer0 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x47	Stop output clock from Synthesizer0 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4C	Stop output clock from Synthesizer1 Post Divider C bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4D	Stop output clock from Synthesizer1 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4E	Stop output clock from Synthesizer1 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4F	Stop output clock from Synthesizer1 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x50	Stop output clock from Synthesizer2 Post Divider A bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x51	Stop output clock from Synthesizer2 Post Divider A bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x52	Stop output clock from Synthesizer2 Post Divider B bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x53	Stop output clock from Synthesizer2 Post Divider B bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x54	Stop output clock from Synthesizer2 Post Divider C bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x55	Stop output clock from Synthesizer2 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1

Value	Name	Description
0x56	Stop output clock from Synthesizer2 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x57	Stop output clock from Synthesizer2 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x58	Stop output clock from Synthesizer3 Post Divider A bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x59	Stop output clock from Synthesizer3 Post Divider A bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5A	Stop output clock from Synthesizer3 Post Divider B bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5B	Stop output clock from Synthesizer3 Post Divider B bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5C	Stop output clock from Synthesizer3 Post Divider C bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5D	Stop output clock from Synthesizer3 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5E	Stop output clock from Synthesizer3 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5F	Stop output clock from Synthesizer3 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
High Performance Differential Outputs		
0x60	Enable Differential output HPDIFF0	This signal is OR-ed with the 'Enable HPDIFF0' bit in the 'High performance differential output enable' register. Functionality of this signal is explained in hpdiff_en register.
0x62	Enable Differential output HPDIFF1	Same description as Enable Differential output HPDIFF0
0x64	Enable Differential output HPDIFF2	Same description as Enable Differential output HPDIFF0
0x66	Enable Differential output HPDIFF3	Same description as Enable Differential output HPDIFF0
0x68	Enable Differential output HPDIFF4	Same description as Enable Differential output HPDIFF0
0x6A	Enable Differential output HPDIFF5	Same description as Enable Differential output HPDIFF0

Value	Name	Description
0x6C	Enable Differential output HPDIFF6	Same description as Enable Differential output HPDIFF0
0x6E	Enable Differential output HPDIFF7	Same description as Enable Differential output HPDIFF0
High Performance CMOS Outputs		
0x70	Enable HPOUTCLK0	This signal is OR-ed with the 'Enable HPOUTCLK0' bit in the 'High performance CMOS output enable' register.
0x72	Enable HPOUTCLK1	Same description as Enable HPOUTCLK0
0x74	Enable HPOUTCLK2	Same description as Enable HPOUTCLK0
0x76	Enable HPOUTCLK3	Same description as Enable HPOUTCLK0

The following table defines the function of the GPIO pin when configured as a status pin. Configuring the value in bit 6:0 in GPIO configuration registers enables the stated function.

Value	Name	Description
Interrupt		
0x80	Interrupt output signal	This bit will be high if the interrupt has been asserted.
Input References		
0x88	Ref0 - Signal not present in last second	This bit will be high if Ref0 signal was not toggling in the last second.
0x89	Ref0 Single Cycle Measurement (SCM) failure	This bit will be set if Ref0 SCM indicator is active (see 'Ref0 SCM and CFM limits' register for SCM limits).
0x8A	Ref0 Coarse Frequency Measurement (CFM) failure	This bit will be set if Ref0 CFM indicator is active (see 'Ref0 SCM and CFM limits' register for CFM limits).
0x8B	Ref0 Guard Soak Timer (GST) indicator	Ref0 Guard Soak Timer (GST) indicator
0x8C	Ref0 failure indicator	This bit will be set if either Ref0 external LOS signal is high, or Ref0 SCM, CFM or GST indicator is high, and appropriate mask bit in the 'Ref0 and Ref1 failure mask' register is set to 1 (not masked).
0x90	Ref1 - Signal not present in last second	Same description as for Ref0
0x91	Ref1 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0x92	Ref1 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0x93	Ref1 Guard Soak Timer (GST) indicator	Same description as for Ref0
0x94	Ref1 failure indicator	Same description as for Ref0

Value	Name	Description
0x98	Ref2 - Signal not present in last second	Same description as for Ref0
0x99	Ref2 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0x9A	Ref2 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0x9B	Ref2 Guard Soak Timer (GST) indicator	Same description as for Ref0
0x9C	Ref2 failure indicator	Same description as for Ref0
0xA0	Ref3 - Signal not present in last second	Same description as for Ref0
0xA1	Ref3 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0xA2	Ref3 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0xA3	Ref3 Guard Soak Timer (GST) indicator	Same description as for Ref0
0xA4	Ref3 failure indicator	Same description as for Ref0
DPLL Filters		
0xA8	DPLL0 Normal mode indicator	This bit will be set when DPLL0 is in normal locking mode (not holdover, not freerun)
0xA9	DPLL0 holdover mode indicator	This bit will be set when DPLL0 is in holdover mode
0xAA	DPLL0 used reference bit1	This bit in combination with DPLL0 ref sel bit0 represents DPLL0 selected reference. Selection: bit1 bit0 0 0 = Ref0 0 1 = Ref1 1 0 = Ref2 1 1 = Ref3
0xAB	DPLL0 used reference bit0	See bit1 description
0xAF	DPLL0 Lock Indication 0	This bit will be set when DPLL0 phase error is less then 36us during 10s period.
0xB0	DPLL0 Lock Indication 1	This bit will be set when DPLL0 phase error is less then 1us during 1s period.
0xB1	DPLL0 Lock Indication 2	This bit will be set when DPLL0 phase error is less then 10us during 1 s period.
0xB2	DPLL0 Lock Indication 3	This bit will be set when DPLL0 phase error is less then 10us during 10s period.

Value	Name	Description
0xB8	DPLL1 Normal mode indicator	Same description as for DPLL0
0xB9	DPLL1 holdover mode indicator	Same description as for DPLL0
0xBA	DPLL1 used reference bit1	Same description as for DPLL0
0xBB	DPLL1 used reference bit0	Same description as for DPLL0
0xBF	DPLL1 Lock Indication 0	Same description as for DPLL0
0xC0	DPLL1 Lock Indication 1	Same description as for DPLL0
0xC1	DPLL1 Lock Indication 2	Same description as for DPLL0
0xC2	DPLL1 Lock Indication 3	Same description as for DPLL0

5.3 Configuration Registers

This section refers to configuration registers that are set by the user to define device operation.

5.3.1 Input Reference Configuration and Programmability

The following is the set of parameters that are configurable:

- Input reference frequency as multiple of 1 kHz, and M/N ratio of the 1 kHz multiple
- Default input reference selection
- Reference selection Priority
- Automatic or manual reference switching
- Glitch-less or hit-less reference switching
- Reference switch based on single cycle monitor or coarse frequency monitor or guard soak timer

5.3.2 DPLL Configuration and Programmability

The following is the set of parameters that are configurable:

- Number of active DPLLs
- DPLL input reference
- DPLL loop bandwidth

5.3.3 Output Multiplexer Configuration and Programmability

The following is the set of parameters that are configurable:

- Output multiplexer configuration
- Start or Stop clock.

5.3.4 Synthesis Macro Configuration and Programmability

The following is the set of parameters that are configurable:

- Synthesis Macro locked to DPLL0/NCO0, DPLL1/NCO1, NCO2, NCO3, freerun or disabled
- Synthesis Macro mode M/N ratio or 1 kHz multiple
- Synthesis Macro high speed output clock, defined as a 1 kHz multiple and 1 kHz multiple with M/N ratio

5.3.5 Output Dividers and Skew Management Configuration and Programmability

The following is the set of parameters that are configurable:

- Post divider enable/disable
- Divider ratio
- Output delay value

5.3.6 Output Drivers configuration and Programmability

The following is the set of parameters that are configurable:

- Output driver Enable/Disable
  - Output driver mode (single ended or differential)
  - Single ended driver slew rate control (slow, medium and fast)
  - Differential driver mode (LVPECL, LVDS, HCSL)

5.4 State Control and Reference Switch Modes

The device has two main control modes of operation: un-managed mode and managed mode.

In un-managed mode of operation, the DPLL state (normal, freerun and holdover) and the selected reference is automatically set by the device internal state machine. It is based on availability of a valid reference and on the reference selection priority.

In managed mode of operation, the DPLL state (normal, freerun and holdover) and the selected reference is manually set by the user.

The device allows for smooth transition from in and out of the two modes of operation. Hence if the DPLL was in managed mode and locked to ref2 reference and it was switched to un-managed mode of operation, then the state machine continues managing the device starting from being locked to the ref2 reference and it will not force reference switching to any other reference unless a change in conditions required such transition.

To facilitate monitoring and managing the device during managed mode of operation, and to facilitate monitoring the device during the un-managed mode, some control and status bits can be muxed into the GPIO pins. The following is a list for such control and monitor bits:

- DPLL state (2 control bits), Normal, holdover and freerun
- DPLL reference selection (2 control and 2 status bits)
- DPLL reference switching mode (1 control bit) (tie_clr_b) hit-less and glitch-less
- Reference monitoring (3 status bits)
- DPLL holdover indication (1 status bit)
- DPLL lock indication (1 status bit)

Each DPLL has its own independent state control and reference selection state machine.

5.4.1 Un-managed Mode

The un-managed mode combines the functionality of the normal state with automatic holdover and automatic reference switching. In this mode, transitioning from one mode to the other is controlled by the device internal state machine.

The on-chip state machine monitors the device status bits, and based on the status information the state machine makes a decision to force holdover or to perform reference switch.

In the un-managed mode of operation, the device internal state machine manages the device operating states. The reference switching state machine is based on the internal clock monitoring of each of the available input clock sources and the reference priority.

The state machine selects a reference source based on its priority value defined in a control register and the current availability of the reference. If all the references are available, the reference with the highest priority is selected; if this reference fails, the next highest priority reference is selected, and so on.

In un-managed mode, the state machine only reacts to failure indicators and performs reference switching if either one of the following conditions takes place and they are not masked with their corresponding mask bits as follows:

- LOS detected a failure and RefSwMask<0> is at logic “1”
- SCM detected a failure and RefSwMask<1> is at logic “1”
- CFM detected a failure and RefSwMask<2> is at logic “1”
- The Guard Soak Time is triggered and RefSwMask<3> is at logic “1”

The default conditions is RefSwMask<3:0> “1000”.

In un-managed mode of operation, the state machine only reacts to failure indicators and goes into auto-holdover under one of the following conditions if they are not masked with their corresponding mask bits:

- LOS detected a failure and HOMask<0> is at logic “1”
- SCM detected a failure and HOMask<1> is at logic “1”
- CFM detected a failure and HOMask<2> is at logic “1”
- The Guard Soak Time is triggered and HOMask<3> is at logic “1”
- Reference switch condition exist, and no reference is available

The default conditions is HOMask<3:0> is “0111”.

In un-managed mode of operation, the state machine automatically recovers from auto-holdover when the conditions to enter auto-holdover are not present.

In un-managed mode, the device automatically selects a valid reference input. If the current reference used for synchronization fails, the state machine switches to the other available reference. If all the available references fail, then the device enters the Holdover mode without switching to another reference. The selection is based on reference priority. Active reference is shown by reference selection status bits.

Reference Priority

Every reference has 3 bits in a control register associated with its priority value (0 to 3) to allow system designers to program the priority of the input references. The priorities are relative to each other, with lower value numbers being the higher priority. value “111" disables the ability to select the reference (i.e., mark reference: don’t use for synchronization). If two or more inputs are given the same priority number, the input is selected based on the reference naming convention (i.e., ref0 is higher priority than ref1). The default reference selection priority is based on reference number (i.e., ref0 is highest priority and ref3 is the lowest priority).

When two references have the same priority they will not revert to each other (as reference availability change), but they will revert to a reference with a higher priority when it is available.

5.4.2 Managed Mode

The managed mode combines the functionality of the Holdover, Freerun and Normal states with automatic Holdover, and manual reference switching through bits in the control registers. In this mode, transitioning from one state to the other is controlled by an external controller.

The external controller monitors the device status bits. Based on the status information, the external controller makes a decision to force holdover or to perform reference switch. In managed mode of reference selection, the active reference input is selected based on reference selection control bits. If the external controller sets the device to lock to a failed reference, the device stays in auto-holdover and only switches to that reference if it becomes valid.

The state machine only reacts to failure indicators and goes into auto-holdover under one of the following conditions if they are not masked with their corresponding mask bits:

- LOS detected a failure and HOMask<0> is at logic “1”
- SCM detected a failure and HOMask<1> is at logic “1”
- CFM detected a failure and HOMask<2> is at logic “1”
- The Guard Soak Time is triggered and HOMask<3> is at logic “1”

The default conditions HOMask<3:0> is “0111”.

The state machine automatically recovers from auto-holdover when the conditions to enter auto-holdover are not present.

Time critical state transitions for entry into auto-holdover and exit from auto-holdover are managed by the internal state machine. Such transition into and out of the auto-holdover state will not allow for change of reference, unless forced by reference selection control bits. A change on the reference select bits triggers an internal state transition into auto-holdover and then exit into Normal state and locking to the new reference.

6.0 Host Interface

A host processor controls and receives status from the Microsemi device using either a SPI or an I^2C interface. The type of interface is selected using the startup state of the GPIO pins.

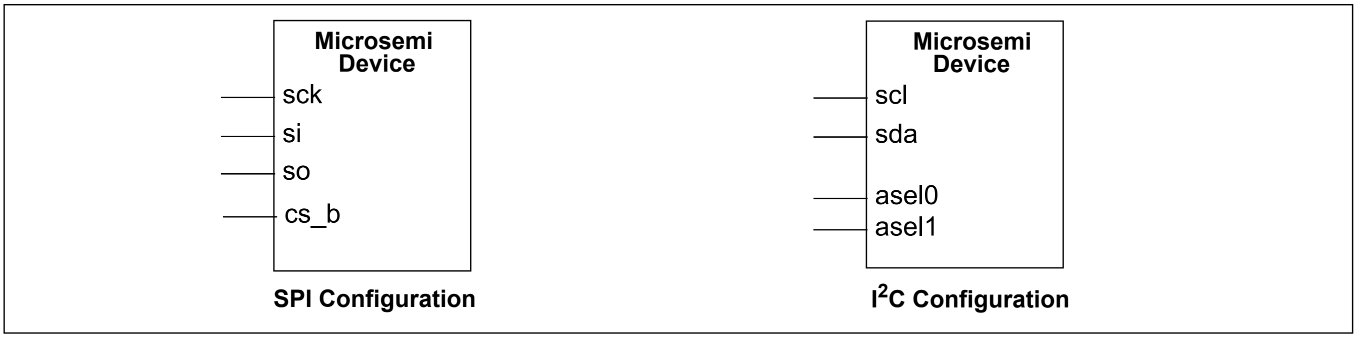


Figure 20 - Serial Interface Configuration

The selection between I2C and SPI interfaces is performed at start-up using GPIO[3] pin, right after pwr_b gets de-asserted. The GPIO pin need to be held at their appropriate value for 55 ms after the de-assertion of pwr_b, after which time they can be released and used as any other GPIO.

Both interfaces use seven bit address field and the device has eight bit address space. Hence, memory is divided in two pages. Page 0 with addresses 0x00 to 0x7E and Page 1 with addresses 0x80 to 0xFF. Writing 0x01 to Page Register at address 0x7F, toggles SPI/I2C accesses between Page 0 and Page 1.

GPIO[3]	Serial Interface
0	SPI
1	I2C

Table 6 - Serial Interface Selection

6.1 Serial Peripheral Interface

The serial peripheral interface (SPI) allows read/write access to the registers that are used to configure, read status, and allow manual control of the device.

This interface supports two modes of access: Most Significant Bit (MSB) first transmission or Least Significant Bit (LSB) first transmission. The mode is automatically selected based on the state of **sck**_scl pin when the **cs_b**_asel0 pin is active. If the **sck**_scl pin is low during **cs_b**_asel0 activation, then MSB first timing is selected. If the **sck**_scl pin is high during **cs_b**_asel0 activation, then LSB first timing is assumed.

The SPI port expects 7-bit addressing and 8-bit data transmission, and is reset when the chip select pin **cs_b**_asel0 is high. During SPI access, the **cs_b**_asel0 pin must be held low until the operation is complete. The first bit transmitted during the address phase of a transfer indicates whether a read (1) or a write (0) is being performed. Burst read/write mode is also supported by leaving the chip select signal **cs_b**_asel0 is low after a read or a write. The address will be automatically incremented after each data byte is read or written.

The serial peripheral interface supports half-duplex processor mode which means that during a write cycle to the device, output data from the **so**_asel1 pin must be ignored. Similarly, the input data on the **si**_sda pin is ignored by the device during a read cycle.

Functional waveforms for the LSB and MSB first mode, and burst mode are shown in Figure 21, Figure 22 and Figure 23. Timing characteristics are shown in Table 8, Figure 34, and Figure 35.

6.1.1 Least Significant Bit (LSB) First Transmission Mode

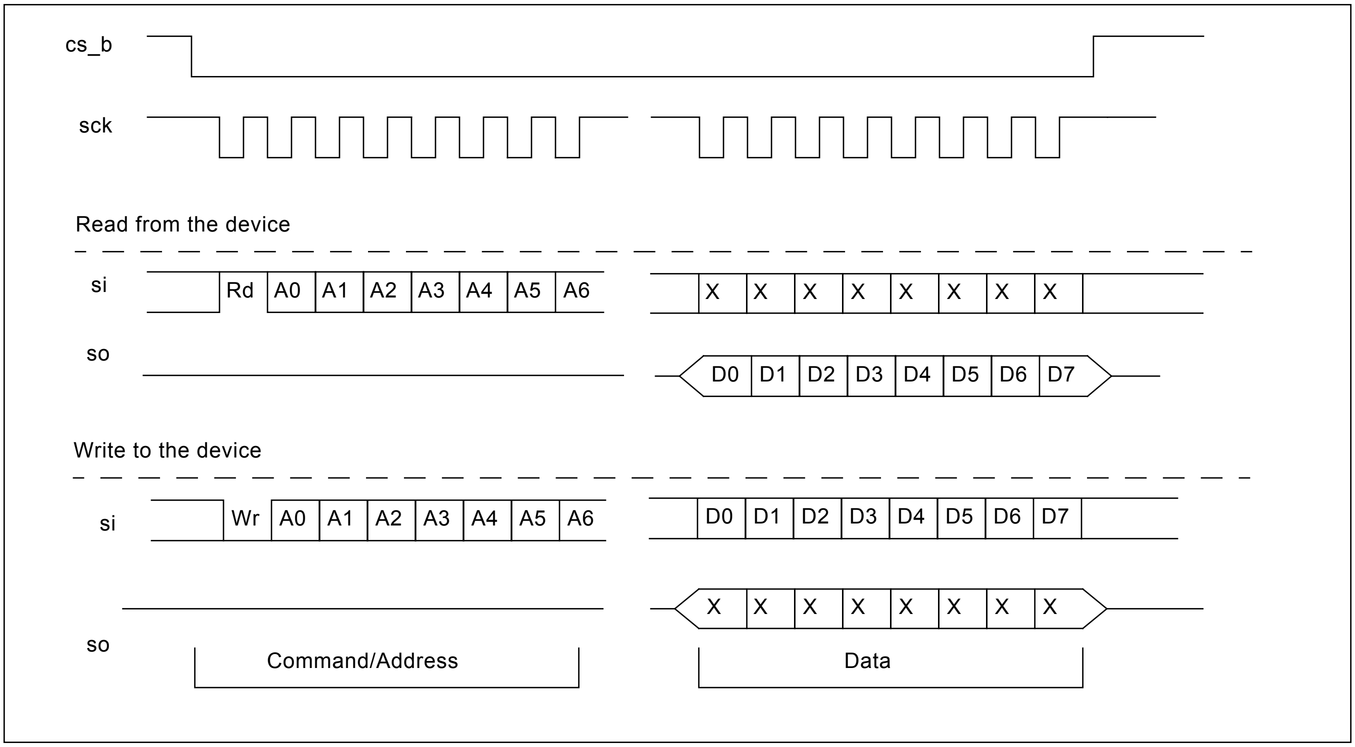


Figure 21 - Serial Peripheral Interface Functional Waveforms - LSB First Mode

6.1.2 Most Significant Bit (MSB) First Transmission Mode

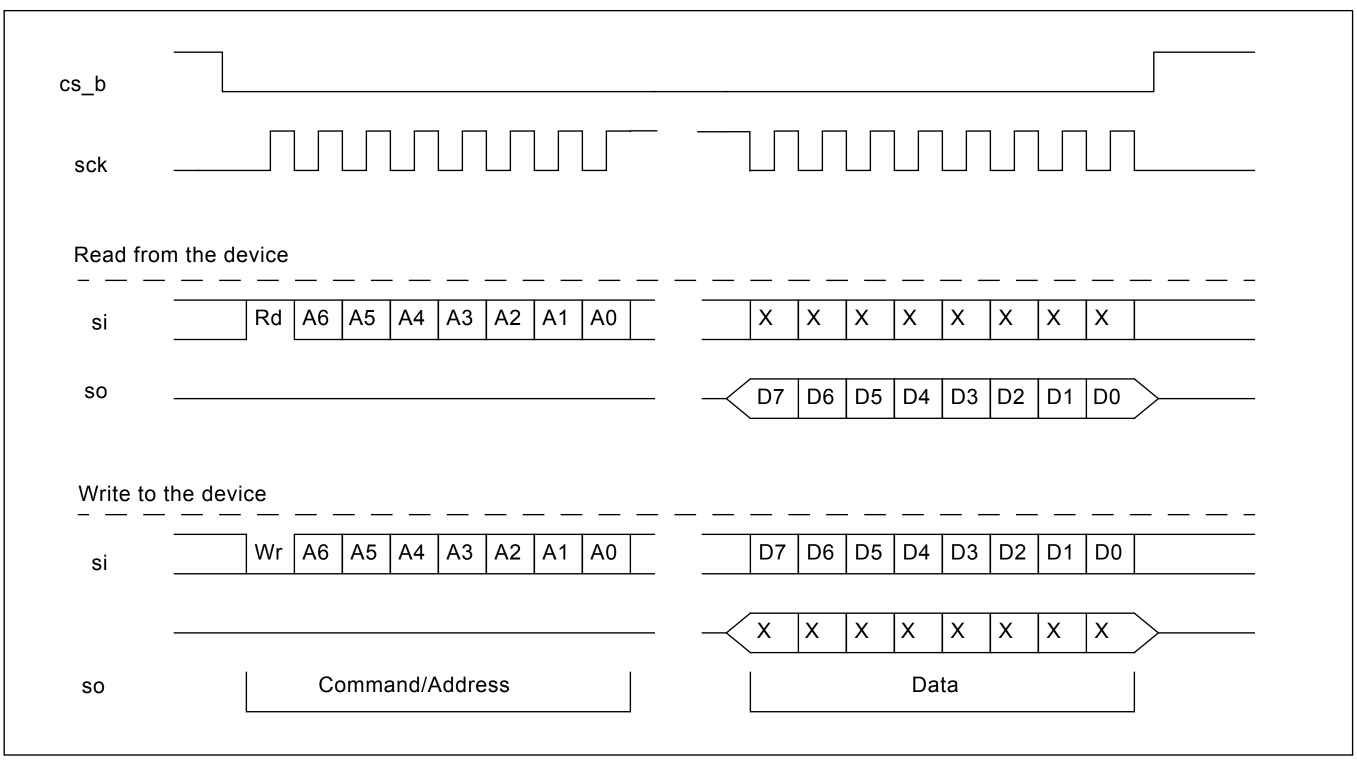


Figure 22 - Serial Peripheral Interface Functional Waveforms - MSB First Mode

6.1.3 SPI Burst Mode Operation

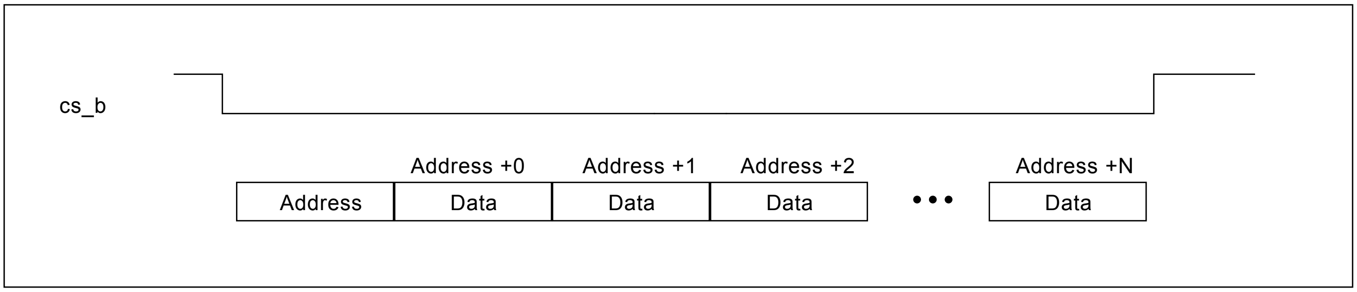


Figure 23 - Example of a Burst Mode Operation

6.1.4 I^{2}C Interface

The I^{2}C controller supports version 2.1 (January 2000) of the Philips I^{2}C bus specification. The port operates in slave mode with 7-bit addressing, and can operate in Standard (100 kbits/s) and Fast (400 kbits/s) mode. Burst mode is supported in both standard and fast modes.

Data is transferred MSB first and occurs in 1 byte blocks. As shown in Figure 24, a **write** command consists of a 7-bit device (slave) address, a 7-bit register address (0x00 - 0x7F), and 8-bits of data.

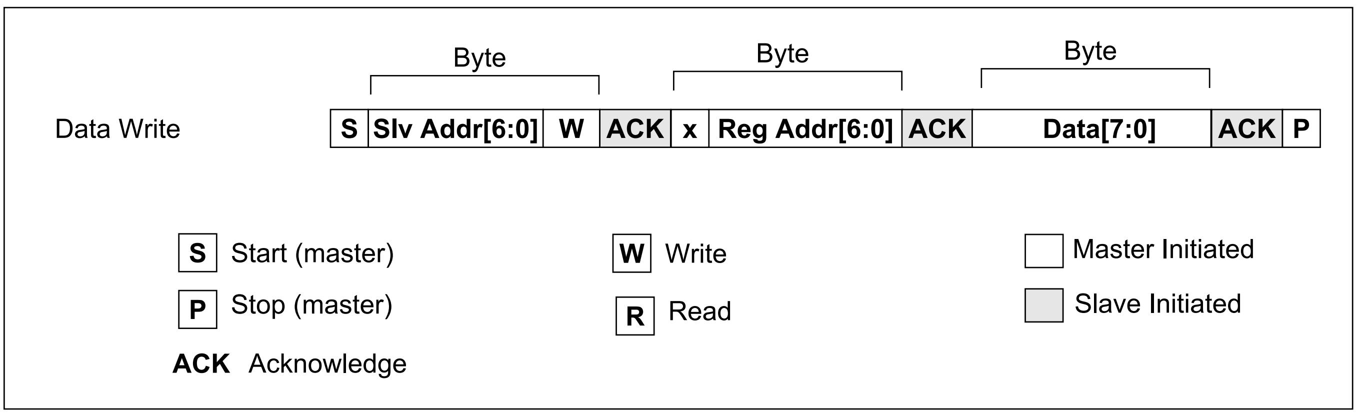


Figure 24 - I^{2}C Data Write Protocol

A **read** is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. This is shown in Figure 25.

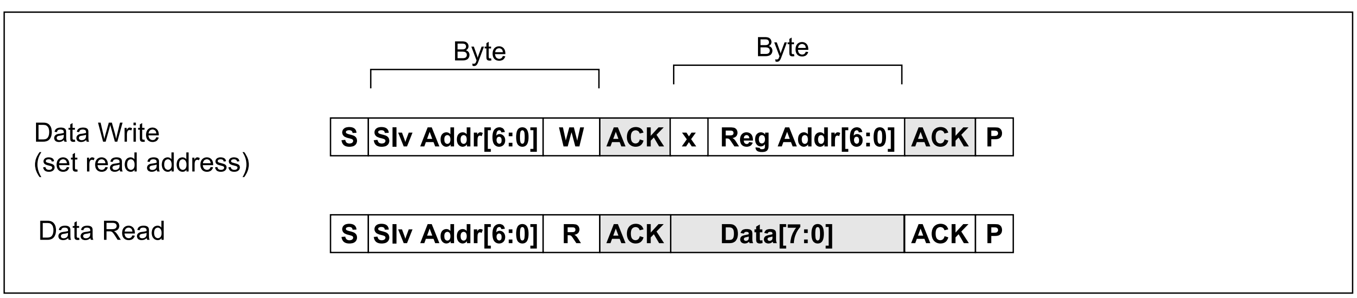


Figure 25 - I^{2}C Data Read Protocol

The **7-bit device (slave) address** contains a 5-bit fixed address plus variable bits which are set with the **asel0,** and **asel1** pins. This allows multiple ZL30150s to share the same I^2C bus. The address configuration is shown in Figure 26.

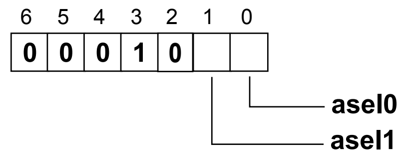


Figure 26 - I^2C 7-bit Slave Address

The device also supports burst mode which allows multiple data write or read operations with a single specified address. This is shown in Figure 27 (write) and Figure 28 (read). The first data byte is written/read from the specified address, and subsequent data bytes are written/read using an automatically increment address. The maximum auto increment address of a burst operation is 0x7F. Any operations beyond this limit will be ignored. In other words, the auto increment address does not wrap around to 0x00 after reaching 0x7F.

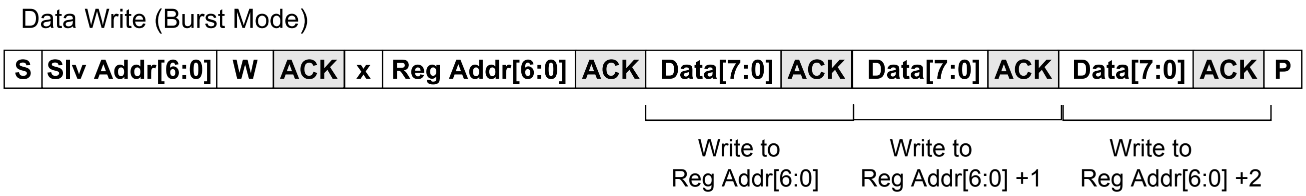


Figure 27 - I^2C Data Write Burst Mode

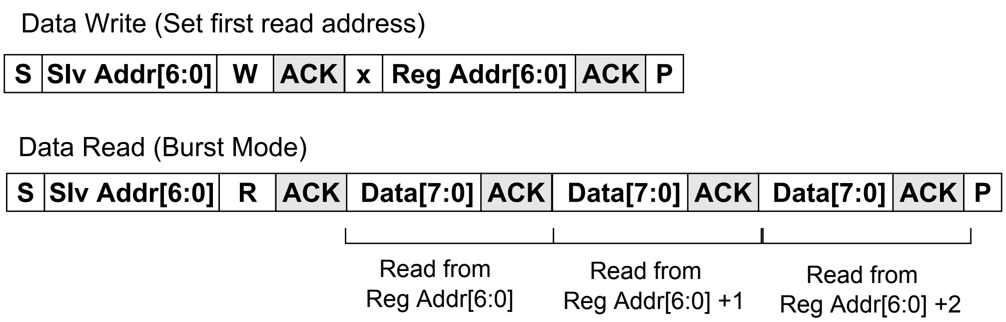


Figure 28 - I^2C Data Read Burst Mode

7.0 Register Map

The device is mainly controlled by accessing software registers through the serial interface (SPI or I^2C). The device can be configured to operate in a highly automated manner which minimizes its interaction with the system's processor, or it can operate in a manual mode where the system processor controls most of the operation of the device.

The simplest way to generate appropriate configuration for the device is to use the evaluation board GUI which can operate standalone (without the board). With GUI user can quickly set all required parameters and save the configuration to a text file.

Multi-byte Register Values

The device register map is based on 8-bit register access, so register values that require more than 8 bits must be spread out over multiple registers and accessed in 8-bit segments. When accessing multi-byte register values, it is important that the registers are accessed in the proper order—they must follow big endian addressing scheme. The 8-bit register containing the most significant byte (MSB) must be accessed first, and the register containing the least significant byte (LSB) must be accessed last. An example of a multi-byte register is shown in Figure 29. When writing a multi-byte value, the value is latched when the LSB is written.

Example:
The programmable input reference M and N 16 bit values defining the M/N ratio is programmed using a 32-bit value which is spread over four 8-bit registers. The MSB is contained in address 0x14 and the LSB in 0x17. When reading or writing this multi-byte value, the MSB must be accessed first, followed by the middle bytes, and the LSB last.

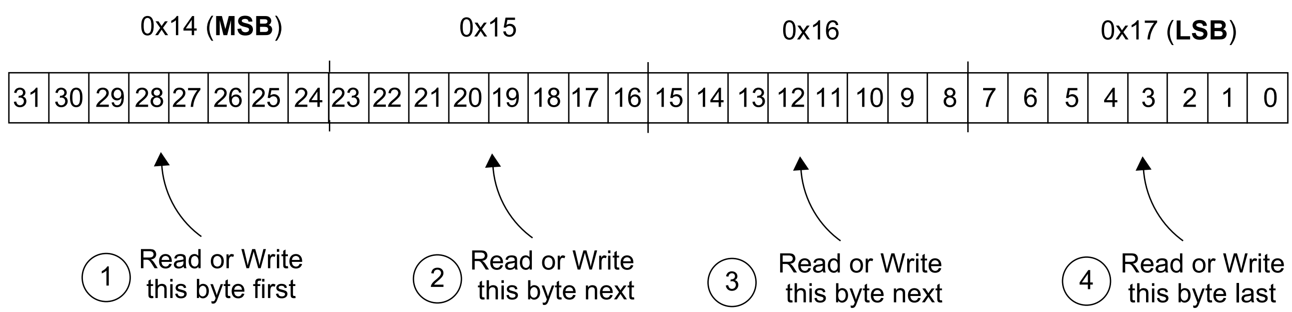


Figure 29 - Accessing Multi-byte Register Values

To assist in device setup, a configuration GUI is provided. The configuration GUI can directly configure the device evaluation board, but it also functions as a tool to provide details on how to configure different device registers.

Writing to registers

Writes to registers should follow following procedure:

-write 0x01 to Sticky R Lock Register at address 0x0D

- write to one or multiple register(s)

-write 0x00 to Sticky R Lock Register at address 0x0D

When changing the dplln_mode bits[1:0] in the dplln_mode_refsel registers (0x33,0x38) from ’11’ (automatic mode) to ’10’ (forced reference lock mode), the following procedure should be followed:

-write 0x01 to Sticky_R_Lock Register at address 0x0D

-write to one or more ZL30150 control register(s)*

-wait 12ms

-write 0x00 to Sticky_R_Lock Register at address 0x0D

* includes changing the dplln_mode bits[1:0] (from '11' to '10') in one or more of the DPLLn_mode_refsel registers.

Reading from Sticky Read (StickyR) Registers

Access to some status registers is defined as Sticky Read (StickyR). Procedure for accessing these registers is:

-clear status register(s) by writing 0x00 to it (please follow Writing to registers procedure shown above)

-wait for 12 ms

-read the status register(s)

Time between two write accesses to the same register

- For each of the following four frequency adjustment registers, page_register, and Sticky R Lock Register there is no waiting time required between two write accesses to the same register.

  "NCO_a_adjust_en" at address 0xEC

  "NCO_a_freq_adjustment" at addresses 0xED: 0xF0

  "NCO_b_adjust_en" at address 0xF1

  "NCO_b_freq_adjustment" at addresses 0xF2: 0xF5

  "page_register" at address 0x7F

  "Sticky R Lock Register" at address 0x0D

- For the other registers, user should wait at least 12 ms between two write accesses to the same register, and all of these registers can be updated together every 12 ms.

The following table provides a summary of the registers available for status updates and configuration of the device. Devices with a custom OTP configuration will power-up with the custom configuration values instead of the default values.

Register _Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
Miscellaneous Registers				
0x00	id_reg	0x0D	Chip ID and version identification. User should not write to this register. If this register is written to, the default value will be temporarily overwritten until the next reset. The temporary change of the default value will not affect the performance of the device.	R/W
Interrupts and Reference Monitor				
0x02	ref_fail_isr_status	0x00	Reference failure status register	StickyR
0x03	dpll_isr_status	0x00	DPLL status register for DPLL 0 and 1	StickyR
0x04	ref_fail_isr_mask	0x00	Reference failure interrupt service register mask	R/W
0x05	dpll_isr_mask	0x00	DPLL interrupt service register mask	R/W
0x06	ref_mon_fail_3_2	0x00	Ref3 and Ref2 failure indications	StickyR
0x07	ref_mon_fail_1_0	0x00	Ref1 and Ref0 failure indications	StickyR
0x08	ref_mon_fail_mask_3_2	0x66	Control register to mask each failure indicator for Ref3 and Ref2	R/W
0x09	ref_mon_fail_mask_1_0	0x66	Control register to mask each failure indicator for Ref1 and Ref0	R/W
0x0A	ref_config	0x10	Configures input references to be differential or single-ended	R/W
0x0B	gst_disqualif_time	0xAA	Control register for the guard soak timer disqualification time for the references	R/W
0x0C	gst_qualif_time	0x55	Control register for the guard soak timer qualification time for the references	R/W
0x0D	sticky_r_lock	0x00	Used to lock StickyR Status Registers from being updated by internal device logic	R/W
Input Frequency Configuration				
0x10:0x11	ref0_base_freq	0x9C40	Ref0 base frequency in Hz (16 bits, unsigned integer)	R/W

Table 7 - Register Map

Register _Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x12: 0x13	ref0_freq_multiple	0x0F30	Ref0 frequency as a multiple of the base frequency (16 bits, unsigned integer)	R/W
0x14:0x17	ref0_ratio_M_N	0x00010 001	Ref0 Mr and Nr values, used for multiplication ratio Mr/Nr (2 x 16 bits unsigned integers)	R/W
0x18:0x19	ref1_base_freq	0x9C40	Ref1 base frequency in Hz (16 bits, unsigned integer)	R/W
0x1A: 0x1B	ref1_freq_multiple	0x01E6	Ref1 frequency as a multiple of the base frequency (16 bits, unsigned integer)	R/W
0x1C:0x1F	ref1_ratio_M_N	0x00010 001	Ref1 Mr and Nr values, used for multiplication ratio Mr/Nr (2 x 16 bits unsigned integers)	R/W
0x20:0x21	ref2_base_freq	0x9C40	Ref2 base frequency in Hz (16 bits, unsigned integer)	R/W
0x22: 0x23	ref2_freq_multiple	0x01E6	Ref3 frequency as a multiple of the base frequency (16 bits, unsigned integer)	R/W
0x24:0x27	ref2_ratio_M_N	0x00010 001	Ref2 Mr and Nr values, used for multiplication ratio Mr/Nr (2 x 16 bits unsigned integers)	R/W
0x28:0x29	ref3_base_freq	0x9C40	Ref3 base frequency in Hz (16 bits, unsigned integer)	R/W
0x2A: 0x2B	ref3_freq_multiple	0x01E6	Ref3 frequency as a multiple of the base frequency (16 bits, unsigned integer)	R/W
0x2C:0x2F	ref3_ratio_M_N	0x00010 001	Ref3 Mr and Nr values, used for multiplication ratio Mr/Nr (2 x 16 bits unsigned integers)	R/W
DPLL Configuration, State Machine Control and Monitor				
0x30	dpll0_ctrl	0x0C	DPLL0 control register	R/W
0x31	dpll0_ref_priority3_2	0x32	DPLL0 reference 3 and 2 selection priority	R/W
0x32	dpll0_ref_priority1_0	0x10	DPLL0 reference 2 and 1 selection priority	R/W
0x33	dpll0_mode_refsel	0x0F	DPLL0 reference selection control or reference selection status	R/W

Table 7 - Register Map (continued)

Register _Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x34	dpll0_ref_fail_mask	0x87	Control register to mask each failure indicator (SCM, CFM, PFM and GST) used for automatic reference switching and automatic holdover	R/W
0x35	dpll1_ctrl	0x0C	DPLL1 control register	R/W
0x36	dpll1_ref_priority3_2	0x32	DPLL1 reference 3 and 2 selection priority	R/W
0x37	dpll1_ref_priority1_0	0x10	DPLL1 reference 2 and 1 selection priority	R/W
0x38	dpll1_mode_refsel	0x0F	DPLL1 reference selection or reference selection status	R/W
0x39	dpll1_ref_fail_mask	0x87	Control register to mask each failure indicator (SCM, CFM, PFM and GST) used for automatic reference switching and automatic holdover	R/W
0x3B	dpll0_pull_in_sel	0x07	DPLL0 Pull in range select	R/W
0x3D	dpll1_pull_in_sel	0x07	DPLL1 Pull in range select	R/W
0x44	dpll_hold_lock_fail	0x00	DPLLs lock and holdover status	StickyR
0x45	ex_fb_ctrl	0x00	External feedback control	R/W
0x46	reduced_diff_out_pwr	0xFF	Enables reduced power on high performance differential outputs	R/W
Input Reference Monitoring Registers				
0x47	phase_mem_limit_ref0	0x0A	Reference 0 phase memory limit	R/W
0x48	phase_mem_limit_ref1	0x0A	Reference 1 phase memory limit	R/W
0x49	phase_mem_limit_ref2	0x0A	Reference 2 phase memory limit	R/W
0x4A	phase_mem_limit_ref3	0x0A	Reference 3 phase memory limit	R/W
0x4B	scm_cfm_limit_ref0	0x55	Reference 0 single cycle monitor (SCM) and coarse frequency monitor (CFM) limits	R/W
0x4C	scm_cfm_limit_ref1	0x55	Reference 1 single cycle monitor (SCM) and coarse frequency monitor (CFM) limits	R/W
0x4D	scm_cfm_limit_ref2	0x55	Reference 2 single cycle monitor (SCM) and coarse frequency monitor (CFM) limits	R/W
0x4E	scm_cfm_limit_ref3	0x55	Reference 3 single cycle monitor (SCM) and coarse frequency monitor (CFM) limits	R/W
0x4F	dpll_config	0xF2	Selects which DPLLs are active	R/W

Table 7 - Register Map (continued)

Register _Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
Output Synthesizer Configuration Registers				
0x50:0x51	synth0_base_freq	0x9C40	Synthesizer 0 base frequency	R/W
0x52:0x53	synth0_freq_multiple	0x0798	Synthesizer 0 base frequency multiplication number	R/W
0x54:0x57	synth0_ratio_M_N	0x00010 001	Specifies numerator Ms and denominator Ns for synthesizer 0 multiplication ratio Ms/Ns	R/W
0x58:0x59	synth1_base_freq	0x61A8	Synthesizer 1 base frequency	R/W
0x5A:0x5B	synth1_freq_multiple	0x0C35	Synthesizer 1 base frequency multiplication number	R/W
0x5C:0x5F	synth1_ratio_M_N	0x00010 001	Specifies numerator Ms and denominator Ns for synthesizer 1 multiplication ratio Ms/Ns	R/W
0x60:0x61	synth2_base_freq	0x9C40	Synthesizer 2 base frequency	R/W
0x62:0x63	synth2_freq_multiple	0x0798	Synthesizer 2 base frequency multiplication number	R/W
0x64:0x67	synth2_ratio_M_N	0x00010 001	Specifies numerator Ms and denominator Ns for synthesizer 2 multiplication ratio Ms/Ns	R/W
0x68:0x69	synth3_base_freq	0x9C40	Synthesizer 3 base frequency	R/W
0x6A:0x6B	synth3_freq_multiple	0x0798	Synthesizer 3 base frequency multiplication number	R/W
0x6C:0x6F	synth3_ratio_M_N	0x00010 001	Specifies numerator Ms and denominator Ns for synthesizer 3 multiplication ratio Ms/Ns	R/W
0x70	output_synth_drive_pll	0x44	Selects which DPLL drives which synthesizer	R/W
0x71	output_synthesizer_en	0x03	Output synthesizer enable	R/W
0x72	dpll_lock_selection	0x00	DPLL lock selection	R/W
0x73:0x76	central_freq_offset	0x046A AAAB	Central frequency offset to compensate for oscillator inaccuracy	R/W
0x77	synth_1_0_filter_sel	0x00	Synthesizer 1 and 0 selection between internal and external filter	R/W
0x78	synth0_fine_phase_shift	0x00	Synthesizer 0 fine phase shift	R/W
0x79	synth1_fine_phase_shift	0x00	Synthesizer 1 fine phase shift	R/W

Table 7 - Register Map (continued)

Register _Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x7A	synth2_fine_phase_shift	0x00	Synthesizer 2 fine phase shift	R/W
0x7B	synth3_fine_phase_shift	0x00	Synthesizer 3 fine phase shift	R/W
0x7F	page_register	0x00	Selects between pages 0 and 1	R/W
0x80:0x82	synth0_post_div_A	0x000002	Synthesizer 0 post divider A	R/W
0x83:0x85	synth0_post_div_B	0x000002	Synthesizer 0 post divider B	R/W
0x86:0x88	synth0_post_div_C	0x000040	Synthesizer 0 post divider C	R/W
0x89:0x8B	synth0_post_div_D	0x000040	Synthesizer 0 post divider D	R/W
0x8C,0x8E	synth1_post_div_A	0x000002	Synthesizer 1 post divider A	R/W
0x8F,0x91	synth1_post_div_B	0x000002	Synthesizer 1 post divider B	R/W
0x92,0x94	synth1_post_div_C	0x000032	Synthesizer 1 post divider C	R/W
0x95,0x97	synth1_post_div_D	0x000032	Synthesizer 1 post divider D	R/W
0x98,0x9A	synth2_post_div_A	0x000000	Synthesizer 2 post divider A	R/W
0x9B,0x9D	synth2_post_div_B	0x000000	Synthesizer 2 post divider B	R/W
0x9E,0xA0	synth2_post_div_C	0x000000	Synthesizer 2 post divider C	R/W
0xA1,0xA3	synth2_post_div_D	0x000000	Synthesizer 2 post divider D	R/W
0xA4,0xA6	synth3_post_div_A	0x000000	Synthesizer 3 post divider A	R/W
0xA7,0xA9	synth3_post_div_B	0x000000	Synthesizer 3 post divider B	R/W
0xAA,0xAC	synth3_post_div_C	0x000000	Synthesizer 3 post divider C	R/W

Table 7 - Register Map (continued)

Register _Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0xAD,0xAF	synth3_post_div_D	0x000000	Synthesizer 3 post divider D	R/W
Output Reference Selection and Output Driver Control				
0xB0	hp_diff_en	0x00	High Performance differential output enable	R/W
0xB1	hp_cmos_en	0x00	Enables High Performance CMOS outputs hpoutclk[3:0]	R/W
0xB2	config_output_mode_7_4	0x00	Enables and controls configurable outputs outclk[7:4]	R/W
0xB3	config_output__mode_3_0	0x00	Enables and controls configurable outputs outclk[3:0]	R/W
0xB4	config_output_mux_7_4	0x00	Multiplexer selection for configurable outputs outclk[7:4]	R/W
0xB5	config_output_mux_3_0	0x00	Multiplexer selection for configurable outputs outclk[3:0]	R/W
0xB6	synth3_stop_clk	0x00	Stops output clocks for post dividers of Synthesis Engine 3 at either high or low logical level	R/W
0xB7	synth2_stop_clk	0x00	Stops output clocks for post dividers of Synthesis Engine 2 at either high or low logical level	R/W
0xB8	synth1_0_stop_clk	0x00	Stops output clocks for post dividers C and D of Synthesis Engine 0 and 1 at either high or low logical level	R/W
0xB9	syn_fail_flag_status	0x00	Indicates Synthesizers loss of lock	StickyR
0xBA	clear_sync_fail_flag	0x00	Clears Synthesizers fail flag in register 0xB9	R/W
0xBF:0xC0	phase_shift_s0_postdiv_C	0x0000	hpoutclk or configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 0, Post Divider C.	R/W
0xC1:0xC2	phase_shift_s0_postdiv_D	0x0000	hpoutclk or configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 0, Post Divider D.	R/W
0XC3	xo_or_crystal_sel	0x00	Disables OSCo driver.	R/W

Table 7 - Register Map (continued)

Register _Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0xC6	chip_revision	0x03	Chip revision number	R/W
0xC7:0xC8	phase_shift_s1_postdiv_C	0x0000	hpoutclk or configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 1, Post Divider C.	R/W
0xC9:0xCA	phase_shift_s1_postdiv_D	0x0000	hpoutclk or configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 1, Post Divider D.	R/W
0xCB:0xCC	phase_shift_s2_postdiv_A	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 2, Post Divider A.	R/W
0xCD:0xCE	phase_shift_s2_postdiv_B	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 2, Post Divider B.	R/W
0xCF:0xD0	phase_shift_s2_postdiv_C	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 2, Post Divider C.	R/W
0xD1:0xD2	phase_shift_s2_postdiv_D	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 2, Post Divider D.	R/W
0xD3:0xD4	phase_shift_s3_postdiv_A	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 3, Post Divider A.	R/W
0xD5:0xD6	phase_shift_s3_postdiv_B	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 3, Post Divider B.	R/W

Table 7 - Register Map (continued)

Register _Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0xD7:0xD8	phase_shift_s3_postdiv_C	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 3, Post Divider C.	R/W
0xD9:0xDA	phase_shift_s3_postdiv_D	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 3, Post Divider D.	R/W
0xDB	config_output_voltage	0x0F	Configurable output voltage level selection	R/W
0xDC	config_output_slew_rate	0x00	Configurable output slew rate control	R/W
0xE0	gpio_function_pin0	0x00	GPIO0 control or status select	R/W
0xE1	gpio_function_pin1	0x00	GPIO1 control or status select	R/W
0xE2	gpio_function_pin2	0x60	GPIO2 control or status select	R/W
0xE3	gpio_function_pin3	0x00	GPIO3control or status select	R/W
0xE4	gpio_function_pin4	0x00	GPIO4 control or status select	R/W
0xE5	gpio_function_pin5	0x00	GPIO5 control or status select	R/W
0xE6	gpio_function_pin6	0x00	GPIO6 control or status select	R/W
0xE7	gpio_function_pin7	0x00	GPIO7 control or status select	R/W
0xE8	gpio_function_pin8	0x00	GPIO8 control or status select	R/W
0xE9	gpio_function_pin9	0x00	GPIO9 control or status select	R/W
0xEA	gpio_function_pin10	0x00	GPIO10 control or status select	R/W
0xEB	gpio_function_pin11	0x00	GPIO11 control or status select	R/W
0xEC	NCO_a_adjust_en	0x00	Enables NCO a offset adjustment	R/W
0xED:0xF0	NCO_a_freq_offset	0x00000 000	NCO a frequency offset adjustment where n is selected in register 0xEC	R/W
0xF1	NCO_b_adjust_en	0x00	Enables NCO b offset adjustment	R/W
0xF2:0xF5	NCO_b_freq_offset	0x00000 000	NCO b frequency offset adjustment where n is selected in register 0xF1	R/W

Table 7 - Register Map (continued)

8.0 Detailed Register Map

Register_Address: **0x00** Register Name: **id_reg** Default Value: **0x0D** Type: R/W		
Bit Field	**Function Name**	**Description**
4:0	chip_id	Chip Identification = 0b01101
6:5	chip_revision	Chip revision number = 0b00 (full chip revision = chip_revision bits in register 0xC6 and chip_revision bits[6:5] in register 0x00)
7	ready_indication	After reset this bit will be undefined for up to 45 ms. After 45 ms this bit will go low indicating that the device is finalizing self-initialization. Finally, this bit will go high indicating that the device is ready to be programmed by the user. It can take up to 55 ms for this bit to go high after the reset.

Register_Address: **0x02** Register Name: **ref_fail_isr_status** Default Value: **0x00** Type: StickyR		
Bit Field	**Function Name**	**Description**
0	ref0_fail	This bit is set to 1 when ref0 has a failure. The device will set this bit to high when ref0_fail_mask bit of the ref_fail_isr_mask register at address 0x04 is high and conditions for ref0 failure are satisfied. When this bit is set to high, it also sets IRQ line to high.
1	ref1_fail	Same description as for ref0
2	ref2_fail	Same description as for ref0
3	ref3_fail	Same description as for ref0
7:4	reserved	Leave as default

Register_Address: **0x03** Register Name: **dpll_isr_status** Default Value: **0x00** Type: StickyR		
Bit Field	**Function Name**	**Description**
0	dpll0_holdover	The device will set this bit to high when dpll0_holdover_mask bit of the dpll_interrupt_mask register at address 0x05 is high and DPLL0 went into holdover mode. When this bit is set to high, it also sets IRQ line to high.
1	dpll0_loss_of_lock	The device will set this bit to high when 'dpll0_loss_of_lock_mask bit of the dpll_interrupt_mask register at address 0x05 is high and DPLL0 has lost lock. When this bit is set to high, it also sets IRQ line to high.
2	dpll1_holdover	Same description as above but for dpll1
3	dpll1_loss _of_lock	Same description as above but for dpll1
7:4	reserved	Leave as default

Register_Address: **0x04** Register Name: **ref_fail_isr_mask** Default Value: **0x00** Type: R/W		
Bit Field	**Function Name**	**Description**
0	ref0_fail_isr_mask	Reference 0 failure interrupt generation mask. When set to zero disables interrupt generation and appearance in the Reference Status ISR register.
1	ref1_fail_isr_mask	Same description as above but for ref1.
2	ref2_fail_isr_mask	Same description as above but for ref2.
3	ref3_fail_isr_mask	Same description as above but for ref3.
7:4	reserved	Leave as default

Register_Address: **0x05** Register Name: **dpll_isr_mask** Default Value: **0x00** Type: R/W		
Bit Field	**Function Name**	**Description**
0	dpll0_holdover_mask	DPLL0 holdover indication mask. When set to zero disables interrupt generation and appearance in the DPLL Status ISR register.
1	dpll0_loss_of_lock_mask	DPLL0 loss of lock indication mask. When set to zero disables interrupt generation and appearance in the DPLL Status ISR register.
2	dpll1_holdover_mask	Same description as above but for dpll1.
3	dpll1_loss_of_lock_mask	Same description as above but for dpll1.
7:4	reserved	Leave as default.

Register_Address: **0x06** Register Name: **ref_mon_fail_3_2** Default Value: **0x00** Type:StickyR		
Bit Field	**Function Name**	**Description**
0	ref2_fail_los	Reference 2 Loss Of Signal (LOS) indicator. The device will set this bit to high when external Ref 2 LOS signal (typically from PHY device), applied to selected GPIO, goes high. The Ref2 LOS signal indicator can be associated with any of available GPIOs pins through the 'GPIO function' registers. **Note:** this bit is not maskable.
1	ref2_fail_scm	Reference 2 Single Cycle Monitor (SCM) indicator. This bit is set high whenever Single Cycle Failure on Reference 2 occurs. **Note:** this bit is not maskable.
2	ref2_fail_cfm	Reference 2 coarse frequency monitoring (SCM) indicator. This bit is set high whenever coarse frequency monitoring failure on Reference 2 occurs. **Note:** this bit is not maskable.
3	ref2_fail_gst	Guard Soak Timer (GST) failure indicator on Reference 2. This bit is set high whenever Reference 2 guard soak timer expires. **Note:** this bit is not maskable.
4	ref3_fail_los	Same description as above but for ref3.
5	ref3_fail_scm	Same description as above but for ref3.
6	ref3_fail_cfm	Same description as above but for ref3.

Register_Address: **0x06** Register Name: **ref_mon_fail_3_2** Default Value: **0x00** Type:StickyR		
Bit Field	**Function Name**	**Description**
7	ref3_fail_gst	Same description as above but for ref3.

Register_Address: **0x07** Register Name: **ref_mon_fail_1_0** Default Value: **0x00** Type: SticlyR		
Bit Field	**Function Name**	**Description**
0	ref0_fail_los	Reference 0 Loss Of Signal (LOS) indicator. The device will set this bit to high when external Ref 0 LOS signal (typically from PHY device), applied to selected GPIO, goes high. The Ref0 LOS signal indicator can be associated with any of available GPIOs pins through the 'GPIO function' registers. **Note:** this bit is not maskable.
1	ref0_fail_scm	Reference 0 Single Cycle Monitor (SCM) indicator. This bit is set high whenever Single Cycle Failure on Reference 0 occurs. **Note:** this bit is not maskable.
2	ref0_fail_cfm	Reference 0 coarse frequency monitoring (CFM) indicator. This bit is set high whenever coarse frequency monitoring failure on Reference 0 occurs. **Note:** this bit is not maskable.
3	ref0_fail_gst	Guard Soak Timer (GST) failure indicator on Reference 0. This bit is set high whenever Reference 0 guard soak timer expires. **Note:** this bit is not maskable.
4	ref1_fail_los	Same description as above but for ref1.
5	ref1_fail_scm	Same description as above but for ref1.
6	ref1_fail_cfm	Same description as above but for ref1.
7	ref1_fail_gst	Same description as above but for ref1.

Register_Address: **0x08** Register Name: **ref_mon_fail_mask_3_2** Default Value: **0x66** Type: R/W		
Bit Field	**Function Name**	**Description**
3:0	ref2_fail_mask	Masks failure indicators (LOS,SCM, CFM, and GST) for reference 2. bit 0: LOS (Loss of Clock) bit 1: SCM (Single Cycle Monitor) bit 2: CFM (Coarse Frequency Monitor) bit 3: GST (Guard Soak Timer) 0: failure bit is masked (disabled) 1: failure bit is un-masked (enabled) **Note**: When set low these bits will mask corresponding Reference 2 failure indicators in Reference Failure Interrupt Status Register at address 0x02. They will not affect bits in Reference Monitoring Failure Mask Register at address 0x06 because bits in Reference Monitoring Failure Mask Register are not maskable.
7:4	ref3_fail_mask	Same description as above but for ref3

Register_Address: **0x09** Register Name: **ref_mon_fail_mask_1_0** Default Value: **0x66** Type: R/W		
Bit Field	**Function Name**	**Description**
3:0	ref0_fail_mask	Masks failure indicators (LOS,SCM, CFM, and GST) for reference 0. bit 0: LOS (Loss of Clock) bit 1: SCM (Single Cycle Monitor) bit 2: CFM (Coarse Frequency Monitor) bit 3: GST (Guard Soak Timer) 0: failure bit is masked (disabled) 1: failure bit is un-masked (enabled) **Note**: When set low these bits will mask corresponding Reference 0 failure indicators in Reference Failure Interrupt Status Register at address 0x02. They will not affect bits in Reference Monitoring Failure Mask Register at address 0x07 because bits in Reference Monitoring Failure Mask Register are not maskable.
7:4	ref1_fail_mask	Same description as above but for ref1.

Register_Address: **0x0A** Register Name: **ref_config** Default Value: **0x10** Type: R/W		
Bit Field	**Function Name**	**Description**
0	ref0_pre-divider_enable	When set high, the Reference 0 input clock will be divided by 2 prior to being fed to DPLL. All registers, which require frequency of the Reference 0 will have to be programmed with half of Reference 0 frequency. When set low, the Reference 0 is fed directly to DPLL.
1	ref1_pre-divider_enable	Same description as above but for ref1
2	ref2_pre-divider_enable	Same description as above but for ref2
3	ref3_pre-divider_enable	Same description as above but for ref3
4	ref0_diff_input_enable	When set high, the device expects differential clock at Ref 0 input pins (Ref0_P and Ref0_N). When set low, the device expects single-ended clock at Ref0_P input pin, and Ref0_N input should be connected to ground.
5	ref1_diff_input_enable	Same description as above but for ref1
6	ref2_diff_input_enable	Same description as above but for ref2
7	ref3_diff_input_enable	Same description as above but for ref3

Register_Address: **0x0B** Register Name: **gst_disqualif_time** Default Value: **0xAA** Type: R/W		
Bit Field	**Function Name**	**Description**
1:0	ref0_gst_disqualif_timer	Selects time to disqualify input reference after detection of either the Ref 0 CFM or Ref 0 SCM indicators. 00: minimum delay 01: 10 ms 10: 50 ms (default) 11: 2.5 s
3:2	ref1_gst_disqualif_timer	Same description as above but for ref1
5:4	ref2_gst_disqualif_timer	Same description as above but for ref2

Register_Address: **0x0B** Register Name: **gst_disqualif_time** Default Value: **0xAA** Type: R/W		
Bit Field	**Function Name**	**Description**
7:6	ref3_gst_disqualif_timer	Same description as above but for ref3

Register_Address: **0x0C** Register Name: **gst_qualif_time** Default Value: **0x55** Type: R/W		
Bit Field	**Function Name**	**Description**
1:0	ref0_gst_qualif_timer	Selects time to qualify input reference after deassertion of both the Ref 0 CFM and Ref 0 SCM indicators. 00: 2 x selected Ref0 GST disqualify time 01: 4 x selected Ref0 GST disqualify time (default) 10: 6 x selected Ref0 GST disqualify time 11: 8 x selected Ref0 GST disqualify time
3:2	ref1_gst_qualif_timer	Same description as above but for ref1
5:4	ref2_gst_qualif_timer	Same description as above but for ref2
7:6	ref3_gst_qualif_timer	Same description as above but for ref3

Register_Address: **0x0D** Register Name: **sticky_r_lock** Default Value: **0x00** Type: R/W		
Bit Field	**Function Name**	**Description**
7:0	sticky_r_lock	This register is used when accessing StickyR status registers. Writing 0x01 to this register locks the status register from being updated by internal logic. Writing 0x00 to this register enables internal updates of StickyR status registers Please refer to **Reading from Sticky Read (StickyR) registers** and **Writing to registers** procedure at the beginning of 7.0, “Register Map“ section.

Register_Address: **0x10:0x11** Register Name: **ref0_base_freq** Default Value: **0x9C40** Type: R/W		
Bit Field	**Function Name**	**Description**
15:0	ref0_base_freq	Unsigned binary value of these bits represents Ref0 base frequency Br in Hz. The Br has to be set to one of the following three values (otherwise 0x1F40 will be used instead): 0x1F40 for 8 kHz, 0x3E80 for 16 kHz, 0x61A8 for 25 kHz 0x9C40 for 40kHz **Note:** in order to write 16 bit value to this register (and any other register that is bigger than 8 bits), the most significant byte has to be written to the lower address and least significant byte has to be written to the higher address. Hence, memory mapping follows big endian.

Register_Address: **0x12:0x13** Register Name: **ref0_freq_multiple** Default Value: **0x0F30** Type: R/W		
Bit Field	**Function Name**	**Description**
15:0	ref0_freq_multiple	Unsigned binary value of these bits represents Ref0 base frequency multiplication number. 'Base frequency' number Br multiplied by the 'Base frequency multiple' number Kr has to equal the reference frequency in Hz. Examples of some references frequencies and appropriate values that can be programmed for Br and Kr to match that reference frequency: Reference frequency / Base frequency Br / Base frequency multiple Kr 2.048 MHz / 8 kHz (0x1F40) / 256 (0x0100) 1.544 MHz / 8 kHz (0x1F40) / 193 (0x00C1) 19.44 MHz / 8 kHz (0x1F40) / 2430 (0x097E) 622.08 MHz / 16 kHz (0x3E80) / 38880 (0x97E0) 156.25 MHz / 25 kHz (0x61A8) / 6250 (0x186A) 25 MHz / 25 kHz (0x61A8) / 1000 (0x03E8)

Register_Address: **0x14:0x17** Register Name: **ref0_ratio_M_N** Default Value: **0x00010001** Type: R/W		
Bit Field	**Function Name**	**Description**
15:0	ref0_FEC_denom_Nr	Unsigned binary value of Mr bits, in combination with unsigned binary value of Nr bits represents Ref0 FEC multiplication ratio. For FEC reference frequencies, the 'Base frequency' number Br multiplied by the 'Base frequency multiple' number Kr, multiplied by Mr and divided by Nr has to equal the reference frequency in Hz; Ref_freq [Hz] = Br x Kr x Mr / Nr Mr and Nr are limited to: 1) Mr = 66 and Nr = 64. These values for Mr and Nr are allowed only when Br and Kr are programmed to Br = 25000 and Kr = 6250. 2) Mr = 1 and Nr = 1 for all other cases (default values)
31:16	ref0_FEC_numer_Mr	

Register_Address: **0x18:0x19** Register Name: **ref1_base_freq** Default Value: **0x9C40** Type: R/W		
Bit Field	**Function Name**	**Description**
15:0	ref1_base_freq	Unsigned binary value of these bits represents Ref1 base frequency Br in Hz. The Br has to be set to one of the following three values (otherwise 0x1F40 will be used instead): 0x1F40 for 8 kHz, 0x3E80 for 16 kHz, 0x61A8 for 25 kHz 0x9C40 for 40kHz **Note:** in order to write 16 bit value to this register (and any other register that is bigger than 8 bits), the most significant byte has to be written to the lower address and least significant byte has to be written to the higher address. Hence, memory mapping follows big endian.

Register_Address: **0x1A:0x1B** Register Name: **ref1_freq_multiple** Default Value: **0x01E6** Type: R/W		
Bit Field	**Function Name**	**Description**
15:0	ref1_freq_multiple	Unsigned binary value of these bits represents Ref1 base frequency multiplication number. 'Base frequency' number Br multiplied by the 'Base frequency multiple' number Kr has to equal the reference frequency in Hz. Examples of some references frequencies and appropriate values that can be programmed for Br and Kr to match that reference frequency: Reference frequency Base frequency Br Base frequency multiple Kr 2.048 MHz 8 kHz (0x1F40) 256 (0x0100) 1.544 MHz 8 kHz (0x1F40) 193 (0x00C1) 19.44 MHz 8 kHz (0x1F40) 2430 (0x097E) 622.08 MHz 16 kHz (0x3E80) 38880 (0x97E0) 156.25 MHz 25 kHz (0x61A8) 6250 (0x186A) 25 MHz 25 kHz (0x61A8) 1000 (0x03E8)

Register_Address: **0x1C:0x1F** Register Name: **ref1_ratio_M_N** Default Value: **0x00010001** Type: R/W		
Bit Field	**Function Name**	**Description**
15:0	ref1_FEC_denom_Nr	Unsigned binary value of Mr bits, in combination with unsigned binary value of Nr bits represents Ref0 FEC multiplication ratio. For FEC reference frequencies, the 'Base frequency' number Br multiplied by the 'Base frequency multiple' number Kr, multiplied by Mr and divided by Nr has to equal the reference frequency in Hz; Ref_freq [Hz] = Br x Kr x Mr / Nr Mr and Nr are limited to: 1) Mr = 66 and Nr = 64. These values for Mr and Nr are allowed only when Br and Kr are programmed to Br = 25000 and Kr = 6250. 2) Mr = 1 and Nr = 1 for all other cases (default values)
31:16	ref1_FEC_numer_Mr	

Register_Address: **0x20:0x21** Register Name: **ref2_base_freq** Default Value: **0x9C40** Type: R/W		
Bit Field	**Function Name**	**Description**
15:0	ref2_base_freq	Unsigned binary value of these bits represents Ref2 base frequency Br in Hz. The Br has to be set to one of the following three values (otherwise 0x1F40 will be used instead): 0x1F40 for 8 kHz, 0x3E80 for 16 kHz, 0x61A8 for 25 kHz 0x9C40 for 40kHz **Note:** in order to write 16 bit value to this register (and any other register that is bigger than 8 bits), the most significant byte has to be written to the lower address and least significant byte has to be written to the higher address. Hence, memory mapping follows big endian.

Register_Address: **0x22:0x23** Register Name: **ref2_freq_multiple** Default Value: **0x01E6** Type: R/W		
Bit Field	**Function Name**	**Description**
15:0	ref2_freq_multiple	Unsigned binary value of these bits represents Ref2 base frequency multiplication number. 'Base frequency' number Br multiplied by the 'Base frequency multiple' number Kr has to equal the reference frequency in Hz. Examples of some references frequencies and appropriate values that can be programmed for Br and Kr to match that reference frequency: Reference frequency / Base frequency Br / Base frequency multiple Kr 2.048 MHz / 8 kHz (0x1F40) / 256 (0x0100) 1.544 MHz / 8 kHz (0x1F40) / 193 (0x00C1) 19.44 MHz / 8 kHz (0x1F40) / 2430 (0x097E) 622.08 MHz / 16 kHz (0x3E80) / 38880 (0x97E0) 156.25 MHz / 25 kHz (0x61A8) / 6250 (0x186A) 25 MHz / 25 kHz (0x61A8) / 1000 (0x03E8)

Register_Address: **0x24:0x27** Register Name: **ref2_ratio_M_N** Default Value: **0x00010001** Type: R/W		
Bit Field	**Function Name**	**Description**
15:0	ref2_FEC_denom_Nr	Unsigned binary value of Mr bits, in combination with unsigned binary value of Nr bits represents Ref2 FEC multiplication ratio. For FEC reference frequencies, the 'Base frequency' number Br multiplied by the 'Base frequency multiple' number Kr, multiplied by Mr and divided by Nr has to equal the reference frequency in Hz; Ref_freq [Hz] = Br x Kr x Mr / Nr Mr and Nr are limited to: 1) Mr = 66 and Nr = 64. These values for Mr and Nr are allowed only when Br and Kr are programmed to Br = 25000 and Kr = 6250. 2) Mr = 1 and Nr = 1 for all other cases (default values)
31:16	ref2_FEC_numer_Mr	

Register_Address: **0x28:0x29** Register Name: **ref3_base_freq** Default Value: **0x9C40** Type: R/W		
Bit Field	**Function Name**	**Description**
15:0	ref3_base_freq	Unsigned binary value of these bits represents Ref3 base frequency Br in Hz. The Br has to be set to one of the following three values (otherwise 0x1F40 will be used instead): 0x1F40 for 8 kHz, 0x3E80 for 16 kHz, 0x61A8 for 25 kHz 0x9C40 for 40kHz **Note:** in order to write 16 bit value to this register (and any other register that is bigger than 8 bits), the most significant byte has to be written to the lower address and least significant byte has to be written to the higher address. Hence, memory mapping follows big endian.

Register_Address: **0x2A:0x2B** Register Name: **ref3_freq_multiple** Default Value: **0x01E6** Type: R/W		
Bit Field	**Function Name**	**Description**
15:0	ref3_freq_multiple	Unsigned binary value of these bits represents Ref3 base frequency multiplication number. 'Base frequency' number Br multiplied by the 'Base frequency multiple' number Kr has to equal the reference frequency in Hz. Examples of some references frequencies and appropriate values that can be programmed for Br and Kr to match that reference frequency: Reference frequency Base frequency Br Base frequency multiple Kr 2.048 MHz 8 kHz (0x1F40) 256 (0x0100) 1.544 MHz 8 kHz (0x1F40) 193 (0x00C1) 19.44 MHz 8 kHz (0x1F40) 2430 (0x097E) 622.08 MHz 16 kHz (0x3E80) 38880 (0x97E0) 156.25 MHz 25 kHz (0x61A8) 6250 (0x186A) 25 MHz 25 kHz (0x61A8) 1000 (0x03E8)

Register_Address: **0x2C:0x2F** Register Name: **ref3_ratio_M_N** Default Value: **0x00010001** Type: R/W		
Bit Field	**Function Name**	**Description**
15:0	ref3_FEC_denom_Nr	Unsigned binary value of Mr bits, in combination with unsigned binary value of Nr bits represents Ref3 FEC multiplication ratio. For FEC reference frequencies, the 'Base frequency' number Br multiplied by the 'Base frequency multiple' number Kr, multiplied by Mr and divided by Nr has to equal the reference frequency in Hz; Ref_freq [Hz] = Br x Kr x Mr / Nr Mr and Nr are limited to: 1) Mr = 66 and Nr = 64. These values for Mr and Nr are allowed only when Br and Kr are programmed to Br = 25000 and Kr = 6250. 2) Mr = 1 and Nr = 1 for all other cases (default values)
31:16	ref3_FEC_numer_Mr	

Register_Address: **0x30** Register Name: **dpll0_ctrl** Default Value: **0x0C** Type: R/W		
Bit Field	**Function Name**	**Description**
1:0	reserved	Leave as default
3:2	dpll0_phase_slope_limit	Selects phase slope limit for DPLL0 00: 61 usec/sec 01: 7.5 usec/sec 10: 0.885 usec/sec 11: unlimited
4	dpll0_tie_clear_enable	Set high to align phase of the DPLL0 output clock with the phase of input reference. This bit should be held low if hitless reference switching is required.
7:5	dpll0_loop_bandwidth	Selects loop bandwidth of DPLL0: 000: 14 Hz 001: 28 Hz 010: 56 Hz 011: 112 Hz 100: 224 Hz 101: 448 Hz 110: 896 Hz 111: reserved

Register_Address: **0x31** Register Name: **dpll0_ref_priority3_2** Default Value: **0x32** Type: R/W		
Bit Field	**Function Name**	**Description**
2:0	dpll0_ref2_priority	Selects Ref2 priority when DPLL0 operates in automatic reference switching mode: 000: ref2 has highest priority 001: ref2 has 2nd highest priority 010: ref2 has 3rd highest priority 011: ref2 has 4th highest priority 100: ref2 has 5th highest priority 101: ref2 has 6th highest priority 110: ref2 has 7th highest priority 111: ref2 is disabled **Note:** When references are programmed to have different priority number, DPLL will perform 'REVERTIVE' switching between them. This means that the DPLL will always switch to the highest priority reference (reference with lowest priority number) whenever that reference becomes available (doesn't fail). When references are programmed to have the same priority number, DPLL will perform 'NON-REVERTIVE' switching between them. This means that the DPLL will not perform switch to another reference with the same priority when that reference becomes available. Combinations of same and different priority numbers can be used, such that DPLL performs revertive switching between different priority references, but non-revertive switching among references with the same priority.
3	reserved	Leave as default
6:4	dpll0_ref3_priority	Description same as above but for dpll0_ref3_priority
7	reserved	Leave as default

Register_Address: **0x32** Register Name: **dpll0_ref_priority1_0** Default Value: **0x10** Type: R/W		
Bit Field	**Function Name**	**Description**
2:0	dpll0_ref0_priority	Selects Ref0 priority when DPLL0 operates in automatic reference switching mode: 000: ref0 has highest priority 001: ref0 has 2nd highest priority 010: ref0 has 3rd highest priority 011: ref0 has 4th highest priority 100: ref0 has 5th highest priority 101: ref0 has 6th highest priority 110: ref0 has 7th highest priority 111: ref0 is disabled **Note:** When references are programmed to have different priority number, DPLL will perform 'REVERTIVE' switching between them. This means that the DPLL will always switch to the highest priority reference (reference with lowest priority number) whenever that reference becomes available (doesn't fail). When references are programmed to have the same priority number, DPLL will perform 'NON-REVERTIVE' switching between them. This means that the DPLL will not perform switch to another reference with the same priority when that reference becomes available. Combinations of same and different priority numbers can be used, such that DPLL performs revertive switching between different priority references, but non-revertive switching among references with the same priority.
3	reserved	Leave as default
6:4	dpll0_ref1_priority	Description same as above but for dpll0_ref1_priority
7	reserved	Leave as default

Register_Address: **0x33** Register Name: **dpll0_mode_refsel** Default Value: **0x0F** Type: R/W		
Bit Field	**Function Name**	**Description**
1:0	dpll0_mode	Selects DPLL0 mode of operation. 00: freerun mode 01: forced holdover mode 10: forced reference lock mode 11: automatic mode In 'automatic mode', reference selection is based on reference availability and reference priority selection. In this mode, DPLL0 will go to holdover only if none of 4 references is available. In 'forced reference lock mode', the DPLL0 has to lock to programmed reference (selected by the 'Reference selection or selected reference status' bits of this register. If the selected reference is not available, the DPLL0 will go to holdover mode and will not switch to another reference, regardless if some other references might be available. When the 'forced holdover mode' is programmed, all references are ignored and DPLL0 has to go to holdover (based on last selected reference). When the 'freerun mode' is selected, the DPLL has to generate all its output clocks based only on the oscillator OSCI input.
4:2	reserved	Leave as default
5	dpll0_ext_fb_enable	When this bit is set to 1, DPLL0 will use the external feedback phase to compensate for the delay on all related output clocks (all output clocks coming from all synthesizers that are associated with the DPLL0). When this bit is 0, DPLL0 will ignore external feedback. **Note:** There is only one external feedback available, so the external feedback phase will be used if this bit is set, regardless whether DPLL0 is used to create the external feedback phase or one of other DPLLs
7:6	dpll0_refsel_refstatus	When the 'DPLL0 mode' bits of this register are set to 11 (automatic mode), these bits are status bits and they represent selected reference status, i.e. 00 = Ref0 is selected as reference for DPLL0 and so on. When the 'DPLL0 mode' bits of this register are set to 10 (forced reference mode), these bits are control bits and they select which reference is DPLL0 forced to select as follows: 00: ref0 01: ref1 10: ref2 11: ref3 When forced reference fails, the DPLL will go to holdover mode When the 'DPLL0 mode' bits of this register are set to 00 or 01 (freerun or holdover mode), these bits are ignored.

Register_Address: **0x34** Register Name: **dpll0_ref_fail_mask** Default Value: **0x87** Type: R/W		
Bit Field	**Function Name**	**Description**
3:0	dpll0_holdover_mask	When set low these bits prevent DPLL0 from going to holdover mode when corresponding reference failure mechanism occur. xxx0: mask holdover on LOS xx0x: mask holdover on SCM x0xx: mask holdover on CFM 0xxx: mask holdover on GST **Note:** GST bit should never be programmed to 1 if neither CFM nor SCM bits are programmed to 1 (e.g. bits 3:1 should never be programmed to '100').
7:4	dpll0_refswitch_fail_mask	When set low these bits prevent reference switching to be performed when corresponding reference failure occurs. xxx0: mask reference switch on LOS xx0x: mask reference switch on SCM x0xx: mask reference switch on CFM 0xxx: mask reference switch on GST

Register_Address: **0x35** Register Name: **dpll1_ctrl** Default Value: **0x0C** Type: R/W		
Bit Field	**Function Name**	**Description**
1:0	reserved	Leave as default
3:2	dpll1_phase_slope_limit	Selects phase slope limit for DPLL1 00: 61 usec/sec 01: 7.5 usec/sec 10: 0.885 usec/sec 11: unlimited
4	dpll1_tie_clear_enable	Set high to align phase of the DPLL1 output clock with the phase of input reference. This bit should be held low if hitless reference switching is required.
7:5	dpll1_loop_bandwidth	Selects loop bandwidth of DPLL1: 000: 14 Hz 001: 28 Hz 010: 56 Hz 011: 112 Hz 100: 224 Hz 101: 448 Hz 110: 896 Hz 111: reserved

Register_Address: **0x36** Register Name: **dpll1_ref_priority3_2** Default Value: **0x32** Type: R/W		
Bit Field	**Function Name**	**Description**
2:0	dpll1_ref2_priority	Selects Ref2 priority when DPLL1 operates in automatic reference switching mode: 000: ref2 has highest priority 001: ref2 has 2nd highest priority 010: ref2 has 3rd highest priority 011: ref2 has 4th highest priority 100: ref2 has 5th highest priority 101: ref2 has 6th highest priority 110: ref2 has 7th highest priority 111: ref2 is disabled **Note:** When references are programmed to have different priority number, DPLL will perform 'REVERTIVE' switching between them. This means that the DPLL will always switch to the highest priority reference (reference with lowest priority number) whenever that reference becomes available (doesn't fail). When references are programmed to have the same priority number, DPLL will perform 'NON-REVERTIVE' switching between them. This means that the DPLL will not perform switch to another reference with the same priority when that reference becomes available. Combinations of same and different priority numbers can be used, such that DPLL performs revertive switching between different priority references, but non-revertive switching among references with the same priority.
3	reserved	Leave as default
6:4	dpll1_ref3_priority	Description same as above but for dpll1_ref3_priority
7	reserved	Leave as default

Register_Address: **0x37** Register Name: **dpll1_ref_priority1_0** Default Value: **0x10** Type: R/W		
Bit Field	**Function Name**	**Description**
2:0	dpll1_ref0_priority	Selects Ref0 priority when DPLL1 operates in automatic reference switching mode: 000: ref0 has highest priority 001: ref0 has 2nd highest priority 010: ref0 has 3rd highest priority 011: ref0 has 4th highest priority 100: ref0 has 5th highest priority 101: ref0 has 6th highest priority 110: ref0 has 7th highest priority 111: ref0 is disabled **Note:** When references are programmed to have different priority number, DPLL will perform 'REVERTIVE' switching between them. This means that the DPLL will always switch to the highest priority reference (reference with lowest priority number) whenever that reference becomes available (doesn't fail). When references are programmed to have the same priority number, DPLL will perform 'NON-REVERTIVE' switching between them. This means that the DPLL will not perform switch to another reference with the same priority when that reference becomes available. Combinations of same and different priority numbers can be used, such that DPLL performs revertive switching between different priority references, but non-revertive switching among references with the same priority.
3	reserved	Leave as default
6:4	dpll1_ref1_priority	Description same as above but for dpll1_ref1_priority
7	reserved	Leave as default

Register_Address: **0x38** Register Name: **dpll1_mode_refsel** Default Value: **0x0F** Type: R/W		
Bit Field	**Function Name**	**Description**
1:0	dpll1_mode	Selects DPLL1 mode of operation. 00: freerun mode 01: forced holdover mode 10: forced reference lock mode 11: automatic mode In 'automatic mode', reference selection is based on reference availability and reference priority selection. In this mode, DPLL1 will go to holdover only if none of 4 references is available. In 'forced reference lock mode', the DPLL1 has to lock to programmed reference (selected by the 'Reference selection or selected reference status' bits of this register. If the selected reference is not available, the DPLL1 will go to holdover mode and will not switch to another reference, regardless if some other references might be available. When the 'forced holdover mode' is programmed, all references are ignored and DPLL1 has to go to holdover (based on last selected reference). When the 'freerun mode' is selected, the DPLL has to generate all its output clocks based only on the oscillator OSCI input.
4:2	reserved	Leave as default
5	dpll1_ext_fb_enable	When this bit is set to 1, DPLL1 will use the external feedback phase to compensate for the delay on all related output clocks (all output clocks coming from all synthesizers that are associated with the DPLL1). When this bit is 0, DPLL1 will ignore external feedback. **Note:** There is only one external feedback available, so the external feedback phase will be used if this bit is set, regardless whether DPLL1 is used to create the external feedback phase or one of other DPLLs
7:6	dpll1_refsel_refstatus	When the 'DPLL1 mode' bits of this register are set to 11 (automatic mode), these bits are status bits and they represent selected reference status, i.e. 00 = Ref0 is selected as reference for DPLL1 and so on. When the 'DPLL1 mode' bits of this register are set to 10 (forced reference mode), these bits are control bits and they select which reference is DPLL1 forced to select as follows: 00: ref0 01: ref1 10: ref2 11: ref3 When forced reference fails, the DPLL will go to holdover mode. When the 'DPLL1 mode' bits of this register are set to 00 or 01 (freerun or holdover mode), these bits are ignored.

Register_Address: **0x39** Register Name: **dpll1_ref_fail_mask** Default Value: **0x87** Type: R/W		
Bit Field	**Function Name**	**Description**
3:0	dpll1_holdover_mask	When set low these bits prevent DPLL1 from going to holdover mode when corresponding reference failure mechanism occur. xxx0: mask holdover on LOS xx0x: mask holdover on SCM x0xx: mask holdover on CFM 0xxx: mask holdover on GST **Note:** GST bit should never be programmed to 1 if neither CFM nor SCM bits are programmed to 1 (e.g. bits 3:1 should never be programmed to '100').
7:4	dpll1_refswitch_fail_mask	When set low these bits prevent reference switching to be performed when corresponding reference failure occurs. xxx0: mask reference switch on LOS xx0x: mask reference switch on SCM x0xx: mask reference switch on CFM 0xxx: mask reference switch on GST

Register_Address: **0x3B** Register Name: **dpll0_pull_in_sel** Default Value: **0x07** Type: R/W		
Bit Field	**Function Name**	**Description**
2:0	dpll0_pull_in_hold_in	Selects pull-in and hold-in range for DPLL0. 000: +/- 12 ppm 001: +/- 52 ppm 010: +/- 82 ppm 011: +/- 130 ppm 100: +/- 400 ppm 101: reserved 110: reserved 111: unlimited
7:3	Reserved	Leave as default

Register_Address: **0x3D** Register Name: **dpll1_pull_in_sel** Default Value: **0x07** Type: R/W		
Bit Field	**Function Name**	**Description**
2:0	dpll1_pull_in_hold_in	Selects pull-in and hold-in range for DPLL1. 000: +/- 12 ppm 001: +/- 52 ppm 010: +/- 82 ppm 011: +/- 130 ppm 100: +/- 400 ppm 101: reserved 110: reserved 111: unlimited
7:3	Reserved	Leave as default

Register_Address: **0x44** Register Name: **dpll_hold_lock_fail** Default Value: **0x00** Type:**Sticky R**		
Bit Field	**Function Name**	**Description**
0	dpll0_holdover_status	The device will set this bit high when DPLL0 is in holdover mode. **Note:** This bit is not maskable.
1	dpll0_lock_status	The device will set this bit high when DPLL0 is locked to an input reference. **Note:** This bit is not maskable.
2	dpll1_holdover_status	Same description as above but for dpll1_holdover_status
3	dpll1_lock_status	Same description as above but for dpll1_lock_status
7:4	reserved	Leave as default

Register_Address: **0x45** Register Name: **ext_fb_ctrl** Default Value: **0x00** Type: R/W		
Bit Field	**Function Name**	**Description**
0	ext_fb_dpll_select	0: external feedback phase represents difference in phase between DPLL0 selected active reference and selected feedback source 1: external feedback phase represents difference in phase between DPLL1 selected active reference and selected feedback source **Note 1:** If external feedback is enabled for particular PLL ('external feedback enable' bit of the 'dpllx_mode_refsel' register is set), resulting DPLL output phase will be compensated for the external feedback phase, regardless which DPLL is used for the external feedback phase calculation. **Note 2:** In order to have proper behavior with external feedback, it is required that main reference and the external feedback source are frequency locked (they do not have to have the same frequency).
1	reserved	Leave as default
3:2	ext_fb_ref_select	00: ref0 is selected as external feedback source 01: ref1 is selected as external feedback source 10: ref2 is selected as external feedback source 11: ref3 is selected as external feedback source
6:4	reserved	Leave as default
7	ext_fb_enable	When set high, this bit enables external feedback

Register_Address: **0x46** Register Name: **reduced_diff_out_pw** Default Value: **0xFF** Type: R/W		
Bit Field	**Function Name**	**Description**
0	hpout0_reduced_pwr	When this bit is set to high, it will enable reduced power mode for HPDIFF0_P and HPDIFF0_N outputs. When low, the outputs are in full power mode
1	hpout1_reduced_pwr	Same description as above but for HPDIFF1 output.
2	hpout2_reduced_pwr	Same description as above but for HPDIFF2 output.
3	hpout3_reduced_pwr	Same description as above but for HPDIFF3 output.
4	hpout4_reduced_pwr	Same description as above but for HPDIFF4 output.
5	hpout5_reduced_pwr	Same description as above but for HPDIFF5 output.
6	hpout6_reduced_pwr	Same description as above but for HPDIFF6 output.
7	hpout7_reduced_pwr	Same description as above but for HPDIFF7 output.

Register_Address: **0x47** Register Name: **phasememlimit_ref0** Default Value: **0x0A** Type: R/W		
Bit Field	**Function Name**	**Description**
7:0	ref0_phasemem_limit	Unsigned binary value of these bits are used to calculate Ref0 phase memory limit. Value that needs to be written to this register is calculated as: Value = round(32 * log(PhaseMemLimit * 10^5)) Phase memory limit should be at least one half period of the clock fed the Ref0. Typical phase memory limits are: Phase memory limit Value Input reference frequency 10 us 0x00 higher than 200 kHz 100 us 0x20 8 kHz 1 ms 0x40 1 kHz

Register_Address: **0x48** Register Name: **phasememlimit_ref1** Default Value: **0x0A** Type: R/W		
Bit Field	**Function Name**	**Description**
7:0	ref1_phasemem_limit	Unsigned binary value of these bits are used to calculate Ref1 phase memory limit. Value that needs to be written to this register is calculated as: Value = round(32 * log(PhaseMemLimit * 10^5)) Phase memory limit should be at least one half period of the clock fed the Ref1. Typical phase memory limits are: Phase memory limit Value Input reference frequency 10 us 0x00 higher than 200 kHz 100 us 0x20 8 kHz 1 ms 0x40 1 kHz

Register_Address: **0x49** Register Name: **phasememlimit_ref2** Default Value: **0x0A** Type: R/W		
Bit Field	**Function Name**	**Description**
7:0	ref2_phasemem_limit	Unsigned binary value of these bits are used to calculate Ref2 phase memory limit. Value that needs to be written to this register is calculated as: Value = round(32 * log(PhaseMemLimit * 10^5)) Phase memory limit should be at least one half period of the clock fed the Ref2. Typical phase memory limits are: Phase memory limit Value Input reference frequency 10 us 0x00 higher than 200 kHz 100 us 0x20 8 kHz 1 ms 0x40 1 kHz

Register_Address: **0x4A** Register Name: **phasememlimit_ref3** Default Value: **0x0A** Type: R/W		
Bit Field	**Function Name**	**Description**
7:0	ref3_phasemem_limit	Unsigned binary value of these bits are used to calculate Ref3 phase memory limit. Value that needs to be written to this register is calculated as: Value = round(32 * log(PhaseMemLimit * 10^5)) Phase memory limit should be at least one half period of the clock fed the Ref3. Typical phase memory limits are: Phase memory limit Value Input reference frequency 10 us 0x00 higher than 200 kHz 100 us 0x20 8 kHz 1 ms 0x40 1 kHz

Register_Address: **0x4B** Register Name: **scm_cfm_limit_ref0** Default Value: **0x55** Type: R/W		
Bit Field	**Function Name**	**Description**
2:0	ref0_cfm_limit	These bits represent Ref0 Coarse Frequency Monitor (CFM) limit selection. When Ref0 fails criteria specified by these bits, the CFM failure indicator will go high (can be read in the 'Ref0 and Ref1 failure indicators' register). Selection: 000 = +/- 0.1% (in Ref0 frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50%
3	reserved	Leave as default.

Register_Address: **0x4B** Register Name: **scm_cfm_limit_ref0** Default Value: **0x55** Type: R/W		
Bit Field	**Function Name**	**Description**
6:4	ref0_scm_limit	These bits represent Ref0 Single Cycle Monitor (SCM) limit selection. When Ref0 fails criteria specified by these bits, the SCM failure indicator will go high. Selection: 000 = +/- 0.1% (in Ref0 frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50% Note that Ref0 clock is sampled by 800 MHz clock, so the measurement granularity is 1.25 ns. This imposes limitation to SCM limits that can be programmed depending on Ref0 clock frequencies: +/- 0.1% : can be programmed for frequencies below 800 kHz +/- 0.5% : below 4 MHz +/- 1% : below 8 MHz +/- 2% : below 16 MHz +/- 5% : below 40 MHz +/- 10% : below 80 MHz +/- 20% : below 160 MHz +/- 50% : below 400 MHz **Note:** SCM indicator should not be used (should be masked) for input references frequencies above 400 MHz.
7	reserved	Leave as default.

Register_Address: **0x4C** Register Name: **scm_cfm_limit_ref1** Default Value: **0x55** Type: R/W		
Bit Field	**Function Name**	**Description**
2:0	ref1_cfm_limit	These bits represent Ref1 Coarse Frequency Monitor (CFM) limit selection. When Ref1 fails criteria specified by these bits, the CFM failure indicator will go high. Selection: 000 = +/- 0.1% (in Ref1 frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50%
3	reserved	Leave as default
6:4	ref1_scm_limit	These bits represent Ref1 Single Cycle Monitor (SCM) limit selection. When Ref1 fails criteria specified by these bits, the SCM failure indicator will go high. Selection: 000 = +/- 0.1% (in Ref1 frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50% Note that Ref1 clock is sampled by 800 MHz clock, so the measurement granularity is 1.25 ns. This imposes limitation to SCM limits that can be programmed depending on Ref1 clock frequencies: +/- 0.1% : can be programmed for frequencies below 800 kHz +/- 0.5% : below 4 MHz +/- 1% : below 8 MHz +/- 2% : below 16 MHz +/- 5% : below 40 MHz +/- 10% : below 80 MHz +/- 20% : below 160 MHz +/- 50% : below 400 MHz **Note:** SCM indicator should not be used (should be masked) for input references frequencies above 400 MHz.

Register_Address: **0x4C** Register Name: **scm_cfm_limit_ref1** Default Value: **0x55** Type: R/W		
Bit Field	**Function Name**	**Description**
7	reserved	Leave as default.

Register_Address: **0x4D** Register Name: **scm_cfm_limit_ref2** Default Value: **0x55** Type: R/W		
Bit Field	**Function Name**	**Description**
2:0	ref2_cfm_limit	These bits represent Ref2 Coarse Frequency Monitor (CFM) limit selection. When Ref2 fails criteria specified by these bits, the CFM failure indicator will go high. Selection: 000 = +/- 0.1% (in Ref2 frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50%
3	reserved	default

Register_Address: **0x4D** Register Name: **scm_cfm_limit_ref2** Default Value: **0x55** Type: R/W		
Bit Field	**Function Name**	**Description**
6:4	ref2_scm_limit	These bits represent Ref2 Single Cycle Monitor (SCM) limit selection. When Ref2 fails criteria specified by these bits, the SCM failure indicator will go high. Selection: 000 = +/- 0.1% (in Ref2 frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50% Note that Ref2 clock is sampled by 800 MHz clock, so the measurement granularity is 1.25 ns. This imposes limitation to SCM limits that can be programmed depending on Ref2 clock frequencies: +/- 0.1% : can be programmed for frequencies below 800 kHz +/- 0.5% : below 4 MHz +/- 1% : below 8 MHz +/- 2% : below 16 MHz +/- 5% : below 40 MHz +/- 10% : below 80 MHz +/- 20% : below 160 MHz +/- 50% : below 400 MHz **Note:** SCM indicator should not be used (should be masked) for input references frequencies above 400 MHz.
7	reserved	Leave as default

Register_Address: **0x4E** Register Name: **scm_cfm_limit_ref3** Default Value: **0x55** Type: R/W		
Bit Field	**Function Name**	**Description**
2:0	ref3_cfm_limit	These bits represent Ref3 Coarse Frequency Monitor (CFM) limit selection. When Ref3 fails criteria specified by these bits, the CFM failure indicator will go high. Selection: 000 = +/- 0.1% (in Ref3 frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50%
3	reserved	default
6:4	ref3_scm_limit	These bits represent Ref3 Single Cycle Monitor (SCM) limit selection. When Ref3 fails criteria specified by these bits, the SCM failure indicator will go high. Selection: 000 = +/- 0.1% (in Ref3 frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50% Note that Ref3 clock is sampled by 800 MHz clock, so the measurement granularity is 1.25 ns. This imposes limitation to SCM limits that can be programmed depending on Ref3 clock frequencies: +/- 0.1% : can be programmed for frequencies below 800 kHz +/- 0.5% : below 4 MHz +/- 1% : below 8 MHz +/- 2% : below 16 MHz +/- 5% : below 40 MHz +/- 10% : below 80 MHz +/- 20% : below 160 MHz +/- 50% : below 400 MHz **Note:** SCM indicator should not be used (should be masked) for input references frequencies above 400 MHz.

Register_Address: **0x4E** Register Name: **scm_cfm_limit_ref3** Default Value: **0x55** Type: R/W		
Bit Field	**Function Name**	**Description**
7	default	Leave as default.

Register_Address: **0x4F** Register Name: **dpll_config** Default Value: **0xF2** Type:**R/W**		
Bit Field	**Function Name**	**Description**
1:0	dpll_config	Select which DPLLs are active 00: none 01: DPLL0 active 10: DPLL0 and DPLL1 11: reserved
3:2	reserved	Leave as default.
7:4	phase_acquisiton_enable	When set high enables corresponding phase acquisition module. When set low powers down corresponding module. xxx1: enables phase acquisition module 0 xx1x: enables phase acquisition module 1 x1xx: enables phase acquisition module 2 1xxx: enables phase acquisition module 3

Register_Address: **0x50:0x51** Register Name: **synth0_base_freq** Default Value: **0x9C40** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	synth0_base_freq_Bs	Unsigned binary value of these bits represents Synthesizer base frequency Bs in Hz. Examples of values fro Bs that can be programmed: 0x1F40 for 8 kHz, 0x61A8 for 25 kHz, 0x9C40 for 40 kHz. **Note 1**: Bs has to be directly divisible from 1600000000, i.e. mod (1600000000, Bs) has to be 0 **Note 2:** Bs has to be chosen such that programmed output frequency is either 8k or 25k multiple (except for allowed case of Ms/Ns = 66/64 when Br = 25000 and Kr = 3125). So, either 8000 or 25000 has to be directly divisible from Bs x Ks / P, i.e. mod (Bs x Ks / P, 8000) or mod (Bs x Ks / P, 25000) has to be 0, where P is chosen postdivider ratio.

Register_Address: **0x52:0x53** Register Name: **synth0_freq_multiple** Default Value: **0x0798** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	synth0_base_freq_mult_Ks	Unsigned binary value of these bits represents Synthesizer base frequency multiplication number. The 'Base frequency' number Bs multiplied by the 'Base frequency multiple' number Ks, and multiplied by 16 equals the synthesizer frequency in Hz. Synthesizer frequency Base frequency Bs Base frequency multiple Ks 1.048576 GHz 8 kHz (0x1F40) 8192 (0x2000) 1.25 GHz 25 kHz (0x61A8) 3125 (0x0C35) **Note:** Ks has to be chosen such that programmed output frequency is either 8k or 25k multiple (except for allowed case of Ms/Ns = 66/64 when Br = 25000 and Kr = 3125). So, either 8000 or 25000 has to be directly divisible from Bs x Ks / P, i.e. mod (Bs x Ks / P, 8000) or mod (Bs x Ks / P, 25000) has to be 0, where P is chosen postdivider ratio.

Register_Address: **0x54:0x57** Register Name: **synth0_ratio_M_N** Default Value: **0x00010001** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	synth0_ratio_denom_Ns	Unsigned binary value of Ms bits, in combination with unsigned binary value of Ns bits represents Synthesizer FEC multiplication ratio. Synthesizer FEC frequencies are calculated using the following formula: Synth_freq [Hz] = Bs x Ks x 16 x Ms / Ns Ms and Ns are limited to: 1) Ms = 66 and Ns = 64. These values for Ms and Ns are allowed only when Bs and Ks are programmed to Br = 25000 and Kr = 3125. 2) Ms = 1 and Ns = 1 for all other cases (default values)
31:16	synth0_ratio_numer_Ms	

Register_Address: **0x58:0x59** Register Name: **synth1_base_freq** Default Value: **0x61A8** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	synth1_base_freq_Bs	Unsigned binary value of these bits represents Synthesizer base frequency Bs in Hz. Examples of values fro Bs that can be programmed: 0x1F40 for 8 kHz, 0x61A8 for 25 kHz, 0x9C40 for 40 kHz. **Note 1**: Bs has to be directly divisible from 1600000000, i.e. mod (1600000000, Bs) has to be 0 **Note 2:** Bs has to be chosen such that programmed output frequency is either 8k or 25k multiple (except for allowed case of Ms/Ns = 66/64 when Br = 25000 and Kr = 3125). So, either 8000 or 25000 has to be directly divisible from Bs x Ks / P, i.e. mod (Bs x Ks / P, 8000) or mod (Bs x Ks / P, 25000) has to be 0, where P is chosen postdivider ratio.

Register_Address: **0x5A:0x5B** Register Name: **synth1_freq_multiple** Default Value: **0x0C35** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	synth1_base_freq_mult_Ks	Unsigned binary value of these bits represents Synthesizer base frequency multiplication number. The 'Base frequency' number Bs multiplied by the 'Base frequency multiple' number Ks, and multiplied by 16 equals the synthesizer frequency in Hz. Synthesizer frequency Base frequency Bs Base frequency multiple Ks 1.048576 GHz 8 kHz (0x1F40) 8192 (0x2000) 1.25 GHz 25 kHz (0x61A8) 3125 (0x0C35) **Note:** Ks has to be chosen such that programmed output frequency is either 8k or 25k multiple (except for allowed case of Ms/Ns = 66/64 when Br = 25000 and Kr = 3125). So, either 8000 or 25000 has to be directly divisible from Bs x Ks / P, i.e. mod (Bs x Ks / P, 8000) or mod (Bs x Ks / P, 25000) has to be 0, where P is chosen postdivider ratio.

Register_Address: **0x5C:0x5F** Register Name: **synth1_ratio_M_N** Default Value: **0x00010001** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	synth1_ratio_denom_Ns	Unsigned binary value of Ms bits, in combination with unsigned binary value of Ns bits represents Synthesizer FEC multiplication ratio. Synthesizer FEC frequencies are calculated using the following formula: Synth_freq [Hz] = Bs x Ks x 16 x Ms / Ns Ms and Ns are limited to: 1) Ms = 66 and Ns = 64. These values for Ms and Ns are allowed only when Bs and Ks are programmed to Br = 25000 and Kr = 3125. 2) Ms = 1 and Ns = 1 for all other cases (default values)
31:16	synth1_ratio_numer_Ms	

<table>
<tr><td colspan="3">Register_Address: 0x60:0x61
Register Name: synth2_base_freq
Default Value: 0x9C40
Type:R/W</td></tr>
<tr><th>Bit Field</th><th>Function Name</th><th>Description</th></tr>
<tr><td>15:0</td><td>synth2_base_freq_Bs</td><td>Unsigned binary value of these bits represents Synthesizer base frequency Bs in Hz. Examples of values fro Bs that can be programmed:

0x1F40 for 8 kHz,
0x61A8 for 25 kHz,
0x9C40 for 40 kHz.

Note 1: Bs has to be directly divisible from 1600000000, i.e. mod (1600000000, Bs) has to be 0

Note 2: Bs has to be chosen such that programmed output frequency is either 8k or 25k multiple (except for allowed case of Ms/Ns = 66/64 when Br = 25000 and Kr = 3125). So, either 8000 or 25000 has to be directly divisible from Bs x Ks / P, i.e. mod (Bs x Ks / P, 8000) or mod (Bs x Ks / P, 25000) has to be 0, where P is chosen postdivider ratio.</td></tr>
</table>

<table>
<tr><td colspan="3">Register_Address: 0x62:0x63
Register Name: synth2_freq_multiple
Default Value: 0x0798
Type:R/W</td></tr>
<tr><th>Bit Field</th><th>Function Name</th><th>Description</th></tr>
<tr><td>15:0</td><td>synth2_base_freq_mult_Ks</td><td>Unsigned binary value of these bits represents Synthesizer base frequency multiplication number.

The 'Base frequency' number Bs multiplied by the 'Base frequency multiple' number Ks, and multiplied by 16 equals the synthesizer frequency in Hz.

Synthesizer frequency   Base frequency Bs   Base frequency multiple Ks
1.048576 GHz   8 kHz (0x1F40)   8192 (0x2000)
1.25 GHz   25 kHz (0x61A8)   3125 (0x0C35)

Note: Ks has to be chosen such that programmed output frequency is either 8k or 25k multiple (except for allowed case of Ms/Ns = 66/64 when Br = 25000 and Kr = 3125). So, either 8000 or 25000 has to be directly divisible from Bs x Ks / P, i.e. mod (Bs x Ks / P, 8000) or mod (Bs x Ks / P, 25000) has to be 0, where P is chosen postdivider ratio.</td></tr>
</table>

<table>
<tr><td colspan="3">Register_Address: 0x64:0x67
Register Name: synth2_fec_ratio_M_N
Default Value: 0x00010001
Type:R/W</td></tr>
<tr><th>Bit Field</th><th>Function Name</th><th>Description</th></tr>
<tr><td>15:0</td><td>synth2_fec_ratio_denom_Ns</td><td rowspan="2">Unsigned binary value of Ms bits, in combination with unsigned binary value of Ns bits represents Synthesizer FEC multiplication ratio. Synthesizer FEC frequencies are calculated using the following formula:

Synth_freq [Hz] = Bs x Ks x 16 x Ms / Ns

Ms and Ns are limited to:
1) Ms = 66 and Ns = 64. These values for Ms and Ns are allowed only when Bs and Ks are programmed to Br = 25000 and Kr = 3125.
2) Ms = 1 and Ns = 1 for all other cases (default values)</td></tr>
<tr><td>31:16</td><td>synth2_fec_ratio_numer_Ms</td></tr>
</table>

<table>
<tr><td colspan="3">Register_Address: 0x68:0x69
Register Name: synth3_base_freq
Default Value: 0x9C40
Type:R/W</td></tr>
<tr><th>Bit Field</th><th>Function Name</th><th>Description</th></tr>
<tr><td>15:0</td><td>synth3_base_freq_Bs</td><td>Unsigned binary value of these bits represents Synthesizer base frequency Bs in Hz. Examples of values fro Bs that can be programmed:

0x1F40 for 8 kHz,
0x61A8 for 25k Hz,
0x9C40 for 40 kHz.

Note 1: Bs has to be directly divisible from 1600000000, i.e. mod (1600000000, Bs) has to be 0

Note 2: Bs has to be chosen such that programmed output frequency is either 8k or 25k multiple (except for allowed case of Ms/Ns = 66/64 when Br = 25000 and Kr = 3125). So, either 8000 or 25000 has to be directly divisible from Bs x Ks / P, i.e. mod (Bs x Ks / P, 8000) or mod (Bs x Ks / P, 25000) has to be 0, where P is chosen postdivider ratio.</td></tr>
</table>

Register_Address: **0x6A:0x6B**
Register Name: **synth3_freq_multiple**
Default Value: **0x0798**
Type:**R/W**

Bit Field	Function Name	Description
15:0	synth3_base_freq_mult_Ks	Unsigned binary value of these bits represents Synthesizer base frequency multiplication number. The 'Base frequency' number Bs multiplied by the 'Base frequency multiple' number Ks, and multiplied by 16 equals the synthesizer frequency in Hz. Synthesizer frequency / Base frequency Bs / Base frequency multiple Ks 1.048576 GHz / 8 kHz (0x1F40) / 8192 (0x2000) 1.25 GHz / 25 kHz (0x61A8) / 3125 (0x0C35) **Note:** Ks has to be chosen such that programmed output frequency is either 8k or 25k multiple (except for allowed case of Ms/Ns = 66/64 when Br = 25000 and Kr = 3125). So, either 8000 or 25000 has to be directly divisible from Bs x Ks / P, i.e. mod (Bs x Ks / P, 8000) or mod (Bs x Ks / P, 25000) has to be 0, where P is chosen postdivider ratio.

Register_Address: **0x6C:0x6F**
Register Name: **synth3_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

<table>
<tr><th>Bit Field</th><th>Function Name</th><th>Description</th></tr>
<tr><td>15:0</td><td>synth3_fec_ratio_denom_Ns</td><td rowspan="2">Unsigned binary value of Ms bits, in combination with unsigned binary value of Ns bits represents Synthesizer FEC multiplication ratio. Synthesizer FEC frequencies are calculated using the following formula:

Synth_freq [Hz] = Bs x Ks x 16 x Ms / Ns

Ms and Ns are limited to:
1) Ms = 66 and Ns = 64. These values for Ms and Ns are allowed only when Bs and Ks are programmed to Br = 25000 and Kr = 3125.
2) Ms = 1 and Ns = 1 for all other cases (default values)</td></tr>
<tr><td>31:16</td><td>synth3_fec_ratio_numer_Ms</td></tr>
</table>

Register_Address: **0x70** Register Name: **output_synth_drive_pll** Default Value: **0x44** Type:**R/W**		
Bit Field	**Function Name**	**Description**
1:0	dpll_nco_for_synth0	Selects which DPLL will drive Synthesizer 0. 00: DPLL0/NCO0 01: DPLL1/NCO1 10: NCO2 11: NCO3
3:2	dpll_nco_for_synth1	Same as above but for Synthesizer 1
5:4	dpll_nco_for_synth2	Same as above but for Synthesizer 2
7:6	dpll_nco_for_synth3	Same as above but for Synthesizer 3

Register_Address: **0x71** Register Name: **output_synth_en** Default Value: **0x03** Type:**R/W**		
Bit Field	**Function Name**	**Description**
3:0	synth_en	Enables output of Synthesizers 0 to 3 xxx1: enables synth0 output xx1x: enables synth1 output x1xx: enables synth2 output 1xxx: enables synth3 output
7:4	reserved	Leave as default

Register_Address: **0x72** Register Name: **dpll_lock_selection** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
1:0	dpll0_lock_selection	Selects DPLL0 lock indicator status condition (appearing in the 'DPLL lock fail' register). 00: phase error is smaller than 36 us during 10 s 01: phase error is smaller than 1 us during 1 s 10: phase error is smaller than 10 us during 1 s 11: phase error is smaller than 10 us during 10 s
3:2	dpll1_lock_selection	Same as above but for dpll1
7:4	reserved	Leave as default

Register_Address: **0x73:0x76** Register Name: **central_freq_offset** Default Value: **0x046AAAAB** Type:**R/W**		
Bit Field	**Function Name**	**Description**
31:0	central_freq_offset	2's complement binary value of these bits represent central frequency offset for the device. This value should be used to compensate for oscillator inaccuracy, or make the device look like Numerically Controlled Oscillator (NCO). This register controls central frequency of all 4 Synthesizers. Expressed in steps of +/- 2^-32 of nominal setting. When oscillator inaccuracy is known: inacc_osc = (f_osc - f_nom)/f_nom (usually specified in ppm), value to be programmed in this register is calculated as per the following formula: X = (1/(1 + inacc_osc) - 1)*2^32, when f_osc < f_nom X = (1/(1 + inacc_osc))*2^32, when f_osc > f_nom, where inacc_osc - represents oscillator frequency inaccuracy, f_osc - represents oscillator frequency, and f_nom - represents oscillator nominal frequency (i.e., 25 MHz) Generally, when the oscillator frequency is lower than the nominal, frequency offset has to be programmed to compensate it in opposite direction, i.e. frequency offset has to be positive, and vice versa. Example 1): if oscillator inaccuracy is -2% (f_osc = 24.5 MHz; inacc_osc = (f_osc - 25 MHz)/25MHz = -0.02), X= (1/(1+(-0.02)) - 1)*2^32 = (1/0.98 - 1)*2^32 = 87652394 = 0x0539782A Example 2): if oscillator inaccuracy is +2% (f_osc = 25.5 MHz; inacc_osc = (f_osc - 25 MHz)/25MHz = 0.02), X= (1/(1+ 0.02))*2^32 = (1/1.02)*2^32 = 4210752251 = 0xFAFAFAFB When NCO behavior is desired, the output frequency should be calculated as per formula: fout = (1 + X/2^32)*finit where X -represent 2's complement number specified in this register finit - initial frequency set by Bs, Ks, Ms, Ns and postdivider number for particular VCO fout - output frequency **Note 1:** Nominal frequency for central frequency offset calculation is 25 MHz although master clock frequency is required to be 24.576 MHz. Because of this default value in this register is 0x046AAAAB. **Note 2:** Central Frequency Offset should not exceed +/-5% off nominal.

Register_Address: **0x77** Register Name: **synth1_0_filter_sel** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
0	synth0_filter_select	Selects filter used by Synthesizer 0 0: external filter 1: internal filter
1	synth1_filter_select	Selects filter used by Synthesizer 1 0: external filter 1: internal filter
7:2	reserved	reserved

Register_Address: **0x78** Register Name: **synth0_fine_phase_shift** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:0	syn0_fine_phase_shift	Unsigned binary value of these bits represent Synth0 fine phase shift (advancement) in steps of Synth0_period / 256. **Note 1:** This register controls fine phase shift for all clocks coming out of the Synthesizer 0 (including all four postdividers)

Register_Address: **0x79** Register Name: **synth1_fine_phase_shift** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:0	syn1_fine_phase_shift	Unsigned binary value of these bits represent Synth1 fine phase shift (advancement) in steps of Synth1_period / 256. **Note 1:** This register controls fine phase shift for all clocks coming out of the Synthesizer 1 (including all four postdividers)

Register_Address: **0x7A** Register Name: **synth2_fine_phase_shift** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:0	syn2_fine_phase_shift	Unsigned binary value of these bits represent Synth0 fine phase shift (advancement) in steps of Synth2_period / 256. **Note 1:** This register controls fine phase shift for all clocks coming out of the Synthesizer 2 (including all four postdividers)

Register_Address: **0x7B** Register Name: **synth3_fine_phase_shift** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:0	syn3_fine_phase_shift	Unsigned binary value of these bits represent Synth3 fine phase shift (advancement) in steps of Synth3_period / 256. **Note 1:** This register controls fine phase shift for all clocks coming out of the Synthesizer 3 (including all four postdividers)

Register_Address: **0x7F** Register Name: **page_register** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
0	page_select	This register is used to toggle memory access between page 0 (addresses 0x00 to 0x7E) and page 1 (addresses 0x80 to 0xFF). This is required because SPI and I2C ports have only seven address bits and the device memory space is eight bit wide. 0: selects addresses 0x00 to 0x7E 1: selects addresses 0x80 to 0xFB
7:1	reserved	reserved

Page_Address: **0x80:0x82** Register Name: **synth0_post_div_A** Default Value: **0x000002** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	frm_pulse_rate_or_div	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] are equal to’1111’ and bits[17:16] are different from ’00’ these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] are equal to ’1111’ and bits[17:16] are equal to ’00’ these bits selects division factor of the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer 0 base frequency divided by the value stored in these bits. Whenever bits[23:20] are different from ’1111’ the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer 0 output frequency divided by the value stored in bits[23:0].

Page_Address: **0x80:0x82** Register Name: **synth0_post_div_A** Default Value: **0x000002** Type:**R/W**		
Bit Field	**Function Name**	**Description**
17:16	frm_pulse_source_or_div	Function of these bits depends on value in bits[23:20]. Whenever these bits are different from ’00’ and bits[23:20] are equal to ’1111’ these bits select related clock (postdivider) within the same Synthesizer 0 (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 00 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111. 00: low frequency clock 01: clock 1 (Synth 0 postdivider B) 10: clock 2 (Synth 0 postdivider C) 11: clock 3 (Synth 0 postdivider D)
18	frm_pulse_polrty_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
19	frm_pulse_type_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1kHz or higher) 1111 and bits[17:16] == 00 : output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer0 base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 00 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from ’1111’ then the output is clock with 50% duty cycle with frequency equal to the Synthesizer0 frequency divided by the value in bits [23:0]

Register_Address: **0x83:0x85** Register Name: **synth0_post_div_B** Default Value: **0x000002** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	frm_pulse_rate_or_div	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] are equal to'1111' and bits[17:16] are different from '01' these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] are equal to '1111' and bits[17:16] are equal to '01' these bits selects division factor of the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer 0 base frequency divided by the value stored in these bits. Whenever bits[23:20] are different from '1111' the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer 0 output frequency divided by the value stored in bits[23:0].
17:16	frm_pulse_source_or_div	Function of these bits depends on value in bits[23:20]. Whenever these bits are different from '01' and bits[23:20] are equal to '1111' these bits select related clock (postdivider) within the same Synthesizer 0 (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 01 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111. 00: clock 1 (Synth 0 postdivider A) 01: low frequency clock 10: clock 2 (Synth 0 postdivider C) 11: clock 3 (Synth 0 postdivider D)
18	frm_pulse_polrty_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to '1111' this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
19	frm_pulse_type_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to '1111' this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse

Register_Address: **0x83:0x85** Register Name: **synth0_post_div_B** Default Value: **0x000002** Type:**R/W**		
Bit Field	**Function Name**	**Description**
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1 kHz or higher) 1111 and bits[17:16] == 01 : output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer 0 base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 01 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from ’1111’ then the output is clock with 50% duty cycle with frequency equal to the Synthesizer0 frequency divided by the value in bits [23:0]

Register_Address: **0x86:0x88** Register Name: **synth0_post_div_C** Default Value: **0x000040** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	frm_pulse_rate_or_div	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] are equal to’1111’ and bits[17:16] are different from ’10’ these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] are equal to ’1111’ and bits[17:16] are equal to ’10’ these bits selects division factor of the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer 0 base frequency divided by the value stored in these bits. Whenever bits[23:20] are different from ’1111’ the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer 0 output frequency divided by the value stored in bits[23:0]. **Note:** The output clock duty-cycle may not be within specified 45% to 55% when post divider value P0C is an odd number and where frequency of the output clock is close to the maximum output frequency supported by hpoutclk. The worst case duty-cycle is 30% is when synthesizer frequency is set to 1 GHz and the P0C is set to 7. If duty-cycle of 45% to 55% is required, user can set synthesizer to run at 1GHz * 8/7 and P0C to 8 which will still generate the same frequency but within 45% to 55% duty-cycle. For odd P0C values greater than or equal to 41 (43, 45...) the duty-cycle will be within 45% to 55%. For even P0C values duty-cycle is always within 45% to 55%
17:16	frm_pulse_source_or_div	Function of these bits depends on value in bits[23:20]. Whenever these bits are different from ’10’ and bits[23:20] are equal to ’1111’ these bits select related clock (postdivider) within the same Synthesizer 0 (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 10 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111. 00: clock 1 (Synth 0 postdivider A) 01: clock 2 (Synth 0 postdivider B) 10: low frequency clock 11: clock 3 (Synth 0 postdivider D)

Register_Address: **0x86:0x88** Register Name: **synth0_post_div_C** Default Value: **0x000040** Type:**R/W**		
Bit Field	**Function Name**	**Description**
18	frm_pulse_polrty_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
19	frm_pulse_type_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1kHz or higher) 1111 and bits[17:16] == 10 : output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer 0 base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 10 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from ’1111’ then the output is clock with 50% duty cycle with frequency equal to the Synthesizer0 frequency divided by the value in bits [23:0]

Register_Address: **0x89:0x8B**
Register Name: **synth0_post_div_D**
Default Value: **0x000040**
Type:**R/W**

Bit Field	Function Name	Description
15:0	frm_pulse_rate_or_div	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] are equal to'1111' and bits[17:16] are different from '11' these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] are equal to '1111' and bits[17:16] are equal to '11' these bits selects division factor of the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer 0 base frequency divided by the value stored in these bits. Whenever bits[23:20] are different from '1111' the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer 0 output frequency divided by the value stored in bits[23:0]. **Note:** The output clock duty-cycle may not be within specified 45% to 55% when post divider value P0D is an odd number and where frequency of the output clock is close to the maximum output frequency supported by hpoutclk. The worst case duty-cycle is 30% is when synthesizer frequency is set to 1 GHz and the P0D is set to 7. If duty-cycle of 45% to 55% is required, user can set synthesizer to run at 1 GHz * 8/7 and P0D to 8 which will still generate the same frequency but within 45% to 55% duty-cycle. For odd P0D values greater than or equal to 41 (43, 45...) the duty-cycle will be within 45% to 55%. For even P0D values duty-cycle is always within 45% to 55%
17:16	frm_pulse_source_or_div	Function of these bits depends on value in bits[23:20]. Whenever these bits are different from '11' and bits[23:20] are equal to '1111' these bits select related clock (postdivider) within the same Synthesizer 0 (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 11 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111. 00: clock 1 (Synth 0 postdivider A) 01: clock 2 (Synth 0 postdivider B) 10: clock 3 (Synth 0 postdivider C) 11: low frequency clock

Register_Address: **0x89:0x8B** Register Name: **synth0_post_div_D** Default Value: **0x000040** Type:**R/W**		
Bit Field	**Function Name**	**Description**
18	frm_pulse_polrty_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
19	frm_pulse_type_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1kHz or higher) 1111 and bits[17:16] == 11 : output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer 0 base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 11 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from ’1111’ then the output is clock with 50% duty cycle with frequency equal to the Synthesizer0 frequency divided by the value in bits [23:0]

Register_Address: **0x8C:0x8E** Register Name: **synth1_post_div_A** Default Value: **0x000002** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	frm_pulse_rate_or_div	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] are equal to'1111' and bits[17:16] are different from '00' these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] are equal to '1111' and bits[17:16] are equal to '00' these bits selects division factor of the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer1 base frequency divided by the value stored in these bits. Whenever bits[23:20] are different from '1111' the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer1 output frequency divided by the value stored in bits[23:0].
17:16	frm_pulse_source_or_div	Function of these bits depends on value in bits[23:20]. Whenever these bits are different from '00' and bits[23:20] are equal to '1111' these bits select related clock (postdivider) within the same Synthesizer1 (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 00 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111. 00: low frequency clock 01: clock 1 (Synth 1 postdivider B) 10: clock 2 (Synth 1 postdivider C) 11: clock 3 (Synth 1 postdivider D)
18	frm_pulse_polrty_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to '1111' this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse

Register_Address: **0x8C:0x8E** Register Name: **synth1_post_div_A** Default Value: **0x000002** Type:**R/W**		
Bit Field	**Function Name**	**Description**
19	frm_pulse_type_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1kHz or higher) 1111 and bits[17:16] == 00 : output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer1 base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 00 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from ’1111’ then the output is clock with 50% duty cycle with frequency equal to the Synthesizer1 frequency divided by the value in bits [23:0]

<table>
<tr><td colspan="3">Register_Address: 0x8F:0x91
Register Name: synth1_post_div_B
Default Value: 0x000002
Type:R/W</td></tr>
<tr><th>Bit Field</th><th>Function Name</th><th>Description</th></tr>
<tr><td>15:0</td><td>frm_pulse_rate_or_div</td><td>Function of these bits depends on the value in bits[23:20].

Whenever bits[23:20] are equal to’1111’ and bits[17:16] are different from ’01’ these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses.

Whenever bits[23:20] are equal to ’1111’ and bits[17:16] are equal to ’01’ these bits selects division factor of the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer1 base frequency divided by the value stored in these bits.

Whenever bits[23:20] are different from ’1111’ the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer1 output frequency divided by the value stored in bits[23:0].</td></tr>
<tr><td>17:16</td><td>frm_pulse_source_or_div</td><td>Function of these bits depends on value in bits[23:20].

Whenever these bits are different from ’01’ and bits[23:20] are equal to ’1111’ these bits select related clock (postdivider) within the same Synthesizer1 (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 01 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111.

00: clock 1 (Synth 1 postdivider A)
01: low frequency clock
10: clock 2 (Synth 1 postdivider C)
11: clock 3 (Synth 1 postdivider D)</td></tr>
<tr><td>18</td><td>frm_pulse_polrty_or_div</td><td>Function of this bit depends on the value in bits[23:20].

Whenever bits[23:20] are equal to ’1111’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0])
0: positive frame pulse
1: negative frame pulse</td></tr>
<tr><td>19</td><td>frm_pulse_type_or_div</td><td>Function of this bit depends on the value in bits[23:20].

Whenever bits[23:20] are equal to ’1111’ this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0])
0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse)
1: GCI frame pulse (frame boundary defined by first edge of the frame pulse</td></tr>
</table>

Register_Address: **0x8F:0x91** Register Name: **synth1_post_div_B** Default Value: **0x000002** Type:**R/W**		
Bit Field	**Function Name**	**Description**
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1kHz or higher) 1111 and bits[17:16] == 01 : output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer1 base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 01 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from '1111' then the output is clock with 50% duty cycle with frequency equal to the Synthesizer1 frequency divided by the value in bits [23:0]

Register_Address: **0x92:0x94** Register Name: **synth1_post_div_C** Default Value: **0x000032** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	frm_pulse_rate_or_div	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] are equal to’1111’ and bits[17:16] are different from ’10’ these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] are equal to ’1111’ and bits[17:16] are equal to ’10’ these bits selects division factor of the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer1 base frequency divided by the value stored in these bits. Whenever bits[23:20] are different from ’1111’ the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer1 output frequency divided by the value stored in bits[23:0]. **Note:** The output clock duty-cycle may not be within specified 45% to 55% when post divider value P1C is an odd number and where frequency of the output clock is close to the maximum output frequency supported by hpoutclk. The worst case duty-cycle is 30% is when synthesizer frequency is set to 1 GHz and the P1C is set to 7. If duty-cycle of 45% to 55% is required, user can set synthesizer to run at 1 GHz * 8/7 and P1C to 8 which will still generate the same frequency but within 45% to 55% duty-cycle. For odd P1C values greater than or equal to 41 (43, 45...) the duty-cycle will be within 45% to 55%. For even P1C values duty-cycle is always within 45% to 55%
17:16	frm_pulse_source_or_div	Function of these bits depends on value in bits[23:20]. Whenever these bits are different from ’10’ and bits[23:20] are equal to ’1111’ these bits select related clock (postdivider) within the same Synthesizer1 (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 10 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111. 00: clock 1 (Synth 1 postdivider A) 01: clock 2 (Synth 1 postdivider B) 10: low frequency clock 11: clock 3 (Synth 1 postdivider D)

Register_Address: **0x92:0x94** Register Name: **synth1_post_div_C** Default Value: **0x000032** Type:**R/W**		
Bit Field	**Function Name**	**Description**
18	frm_pulse_polrty_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
19	frm_pulse_type_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1kHz or higher) 1111 and bits[17:16] == 10 : output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer1 base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 10 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from ’1111’ then the output is clock with 50% duty cycle with frequency equal to the Synthesizer1 frequency divided by the value in bits [23:0]

Register_Address: **0x95:0x97** Register Name: **synth1_post_div_D** Default Value: **0x000032** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	frm_pulse_rate_or_div	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] are equal to'1111' and bits[17:16] are different from '11' these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] are equal to '1111' and bits[17:16] are equal to '11' these bits selects division factor of the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer1 base frequency divided by the value stored in these bits. Whenever bits[23:20] are different from '1111' the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer1 output frequency divided by the value stored in bits[23:0]. **Note:** The output clock duty-cycle may not be within specified 45% to 55% when post divider value P1D is an odd number and where frequency of the output clock is close to the maximum output frequency supported by hpoutclk. The worst case duty-cycle is 30% is when synthesizer frequency is set to 1 GHz and the P1D is set to 7. If duty-cycle of 45% to 55% is required, user can set synthesizer to run at 1 GHz * 8/7 and P1D to 8 which will still generate the same frequency but within 45% to 55% duty-cycle. For odd P1D values greater than or equal to 41 (43, 45...) the duty-cycle will be within 45% to 55%. For even P1D values duty-cycle is always within 45% to 55%.
17:16	frm_pulse_source_or_div	Function of these bits depends on value in bits[23:20]. Whenever these bits are different from '11' and bits[23:20] are equal to '1111' these bits select related clock (postdivider) within the same Synthesizer 0 (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 11 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111. 00: clock 1 (Synth 1 postdivider A) 01: clock 2 (Synth 1 postdivider B) 10: clock 3 (Synth 1 postdivider C) 11: low frequency clock

Register_Address: **0x95:0x97** Register Name: **synth1_post_div_D** Default Value: **0x000032** Type:**R/W**		
Bit Field	**Function Name**	**Description**
18	frm_pulse_polrty_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
19	frm_pulse_type_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1kHz or higher) 1111 and bits[17:16] == 11 : output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer1 base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 11 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from ’1111’ then the output is clock with 50% duty cycle with frequency equal to the Synthesizer1 frequency divided by the value in bits [23:0]

Register_Address: **0x98:0x9A** Register Name: **synth2_post_div_A** Default Value: **0x000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	frm_pulse_rate_or_div	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] are equal to’1111’ and bits[17:16] are different from ’00’ these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] are equal to ’1111’ and bits[17:16] are equal to ’00’ these bits selects division factor of the low frequency output clock. The output is low frequency is equal to Synthesizer 2 base frequency divided by the value stored in these bits. Whenever bits[23:20] are different from ’1111’ the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer 2 output frequency divided by the value stored in bits[23:0].
17:16	frm_pulse_source_or_div	Function of these bits depends on value in bits[23:20]. Whenever these bits are different from ’00’ and bits[23:20] are equal to ’1111’ these bits select related clock (postdivider) within the same Synthesizer 2 (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 00 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111. 00: low frequency clock 01: clock 1 (Synth 2 postdivider B) 10: clock 2 (Synth 2 postdivider C) 11: clock 3 (Synth 2 postdivider D)
18	frm_pulse_polrty_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
19	frm_pulse_type_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse

Register_Address: **0x98:0x9A** Register Name: **synth2_post_div_A** Default Value: **0x000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1kHz or higher) 1111 and bits[17:16] == 00 : output is low frequency clock with 50% duty cycle with frequency equal to Synthesizer 2 base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 00 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from ’1111’ then the output is clock with 50% duty cycle with frequency equal to the Synthesizer 2 frequency divided by the value in bits [23:0]

Register_Address: **0x9B:0x9D** Register Name: **synth2_post_div_B** Default Value: **0x000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	frm_pulse_rate_or_div	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] are equal to’1111’ and bits[17:16] are different from ’01’ these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] are equal to ’1111’ and bits[17:16] are equal to ’01’ these bits selects division factor of the low frequency output clock. The output is low frequency is equal to Synthesizer 2 base frequency divided by the value stored in these bits. Whenever bits[23:20] are different from ’1111’ the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer 2 output frequency divided by the value stored in bits[23:0].

Register_Address: **0x9B:0x9D** Register Name: **synth2_post_div_B** Default Value: **0x000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
17:16	frm_pulse_source_or_div	Function of these bits depends on value in bits[23:20]. Whenever these bits are different from ’01’ and bits[23:20] are equal to ’1111’ these bits select related clock (postdivider) within the same Synthesizer 2 (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 01 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111. 00: clock 1 (Synth 2 postdivider A) 01: low frequency clock 10: clock 2 (Synth 2 postdivider C) 11: clock 3 (Synth 2 postdivider D)
18	frm_pulse_polrty_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
19	frm_pulse_type_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1kHz or higher) 1111 and bits[17:16] == 01 : output is low frequency clock with 50% duty cycle with frequency equal to Synthesizer 2 base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 01 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from ’1111’ then the output is clock with 50% duty cycle with frequency equal to the Synthesizer 2 frequency divided by the value in bits [23:0]

Register_Address: **0x9E:0xA0** Register Name: **synth2_post_div_C** Default Value: **0x000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	frm_pulse_rate_or_div	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] are equal to'1111' and bits[17:16] are different from '10' these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] are equal to '1111' and bits[17:16] are equal to '10' these bits selects division factor of the low frequency output clock. The output is low frequency is equal to Synthesizer 2 base frequency divided by the value stored in these bits. Whenever bits[23:20] are different from '1111' the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer 2 output frequency divided by the value stored in bits[23:0].
17:16	frm_pulse_source_or_div	Function of these bits depends on value in bits[23:20]. Whenever these bits are different from '10' and bits[23:20] are equal to '1111' these bits select related clock (postdivider) within the same Synthesizer 2 (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 10 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111. 00: clock 1 (Synth 2 postdivider A) 01: clock 2 (Synth 2 postdivider B) 10: low frequency clock 11: clock 3 (Synth 2 postdivider D)
18	frm_pulse_polrty_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to '1111' this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
19	frm_pulse_type_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to '1111' this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse

Register_Address: **0x9E:0xA0** Register Name: **synth2_post_div_C** Default Value: **0x000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1kHz or higher) 1111 and bits[17:16] == 10 : output is low frequency clock with 50% duty cycle with frequency equal to Synthesizer 2 base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 10 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from '1111' then the output is clock with 50% duty cycle with frequency equal to the Synthesizer 2 frequency divided by the value in bits [23:0]

Register_Address: **0xA1:0xA3** Register Name: **synth2_post_div_D** Default Value: **0x000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	frm_pulse_rate_or_div	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] are equal to'1111' and bits[17:16] are different from '11' these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] are equal to '1111' and bits[17:16] are equal to '11' these bits selects division factor of the low frequency output clock. The output is low frequency is equal to Synthesizer 2 base frequency divided by the value stored in these bits. Whenever bits[23:20] are different from '1111' the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer 2 output frequency divided by the value stored in bits[23:0].

Register_Address: **0xA1:0xA3** Register Name: **synth2_post_div_D** Default Value: **0x000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
17:16	frm_pulse_source_or_div	Function of these bits depends on value in bits[23:20]. Whenever these bits are different from ’11’ and bits[23:20] are equal to ’1111’ these bits select related clock (postdivider) within the same Synthesizer 2 (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 11 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111. 00: clock 1 (Synth 2 postdivider A) 01: clock 2 (Synth 2 postdivider B) 10: clock 3 (Synth 2 postdivider C) 11: low frequency clock
18	frm_pulse_polrty_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
19	frm_pulse_type_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1kHz or higher) 1111 and bits[17:16] == 11 : output is low frequency clock with 50% duty cycle with frequency equal to Synthesizer 2 base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 11 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from ’1111’ then the output is clock with 50% duty cycle with frequency equal to the Synthesizer 2 frequency divided by the value in bits [23:0]

Register_Address: **0xA4:0xA6** Register Name: **synth3_post_div_A** Default Value: **0x000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	frm_pulse_rate_or_div	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] are equal to'1111' and bits[17:16] are different from '00' these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] are equal to '1111' and bits[17:16] are equal to '00' these bits selects division factor of the low frequency output clock. The output is low frequency is equal to Synthesizer 3 base frequency divided by the value stored in these bits. Whenever bits[23:20] are different from '1111' the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer 3 output frequency divided by the value stored in bits[23:0].
17:16	frm_pulse_source_or_div	Function of these bits depends on value in bits[23:20]. Whenever these bits are different from '00' and bits[23:20] are equal to '1111' these bits select related clock (postdivider) within the same Synthesizer 3 (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 00 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111. 00: low frequency clock 01: clock 1 (Synth 3 postdivider B) 10: clock 2 (Synth 3 postdivider C) 11: clock 3 (Synth 3 postdivider D)
18	frm_pulse_polrty_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to '1111' this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
19	frm_pulse_type_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to '1111' this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse

Register_Address: **0xA4:0xA6** Register Name: **synth3_post_div_A** Default Value: **0x000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1kHz or higher) 1111 and bits[17:16] == 00 : output is low frequency clock with 50% duty cycle with frequency equal to Synthesizer 3 base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 00 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from ’1111’ then the output is clock with 50% duty cycle with frequency equal to the Synthesizer 3 frequency divided by the value in bits [23:0]

Register_Address: **0xA7:0xA9** Register Name: **synth3_post_div_B** Default Value: **0x000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	frm_pulse_rate_or_div	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] are equal to’1111’ and bits[17:16] are different from ’01’ these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] are equal to ’1111’ and bits[17:16] are equal to ’01’ these bits selects division factor of the low frequency output clock. The output is low frequency is equal to Synthesizer 3 base frequency divided by the value stored in these bits. Whenever bits[23:20] are different from ’1111’ the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer 3 output frequency divided by the value stored in bits[23:0].

Register_Address: **0xA7:0xA9** Register Name: **synth3_post_div_B** Default Value: **0x000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
17:16	frm_pulse_source_or_div	Function of these bits depends on value in bits[23:20]. Whenever these bits are different from ’01’ and bits[23:20] are equal to ’1111’ these bits select related clock (postdivider) within the same Synthesizer 3 (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 01 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111. 00: clock 1 (Synth 3 postdivider A) 01: low frequency clock 10: clock 2 (Synth 3 postdivider C) 11: clock 3 (Synth 3 postdivider D)
18	frm_pulse_polrty_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
19	frm_pulse_type_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1kHz or higher) 1111 and bits[17:16] == 01 : output is low frequency clock with 50% duty cycle with frequency equal to Synthesizer 3 base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 01 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from ’1111’ then the output is clock with 50% duty cycle with frequency equal to the Synthesizer 3 frequency divided by the value in bits [23:0]

Register_Address: **0xAA:0xAC** Register Name: **synth3_post_div_C** Default Value: **0x000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	frm_pulse_rate_or_div	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] are equal to'1111' and bits[17:16] are different from '10' these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] are equal to '1111' and bits[17:16] are equal to '10' these bits selects division factor of the low frequency output clock. The output is low frequency is equal to Synthesizer 3 base frequency divided by the value stored in these bits. Whenever bits[23:20] are different from '1111' the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer 3 output frequency divided by the value stored in bits[23:0].
17:16	frm_pulse_source_or_div	Function of these bits depends on value in bits[23:20]. Whenever these bits are different from '10' and bits[23:20] are equal to '1111' these bits select related clock (postdivider) within the same Synthesizer 3 (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 10 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111. 00: clock 1 (Synth 3 postdivider A) 01: clock 2 (Synth 3 postdivider B) 10: low frequency clock 11: clock 3 (Synth 3 postdivider D)
18	frm_pulse_polrty_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to '1111' this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
19	frm_pulse_type_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to '1111' this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse

Register_Address: **0xAA:0xAC** Register Name: **synth3_post_div_C** Default Value: **0x000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1kHz or higher) 1111 and bits[17:16] == 10 : output is low frequency clock with 50% duty cycle with frequency equal to Synthesizer 3 base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 10 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from ’1111’ then the output is clock with 50% duty cycle with frequency equal to the Synthesizer 3 frequency divided by the value in bits [23:0]

Register_Address: **0xAD:0xAF** Register Name: **synth3_post_div_D** Default Value: **0x000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	frm_pulse_rate_or_div	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] are equal to’1111’ and bits[17:16] are different from ’11’ these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] are equal to ’1111’ and bits[17:16] are equal to ’11’ these bits selects division factor of the low frequency output clock. The output is low frequency is equal to Synthesizer 3 base frequency divided by the value stored in these bits. Whenever bits[23:20] are different from ’1111’ the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer 3 output frequency divided by the value stored in bits[23:0].

Register_Address: **0xAD:0xAF** Register Name: **synth3_post_div_D** Default Value: **0x000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
17:16	frm_pulse_source_or_div	Function of these bits depends on value in bits[23:20]. Whenever these bits are different from ’11’ and bits[23:20] are equal to ’1111’ these bits select related clock (postdivider) within the same Synthesizer 0 (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 11 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111. 00: clock 1 (Synth 3 postdivider A) 01: clock 2 (Synth 3 postdivider B) 10: clock 3 (Synth 3 postdivider C) 11: low frequency clock
18	frm_pulse_polrty_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
19	frm_pulse_type_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1kHz or higher) 1111 and bits[17:16] == 11 : output is low frequency clock with 50% duty cycle with frequency equal to Synthesizer 3 base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 11 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from ’1111’ then the output is clock with 50% duty cycle with frequency equal to the Synthesizer 3 frequency divided by the value in bits [23:0]

Register_Address: **0xB0** Register Name: **hp_diff_en** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:0	hp_diff_en	Set high to enable corresponding high performance differential output. Set low to tristate the corresponding output. xxxxxxx1: enables hpdiff0_p/n xxxxxx1x: enables hpdiff1_p/n xxxxx1xx: enables hpdiff2_p/n xxxx1xxx: enables hpdiff3_p/n xxx1xxxx: enables hpdiff4_p/n xx1xxxxx: enables hpdiff5_p/n x1xxxxxx: enables hpdiff6_p/n 1xxxxxxx: enables hpdiff7_p/n

Register_Address: **0xB1** Register Name: **hp_cmos_en** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
3:0	hp_cmos_en	Set high to enable corresponding high performance output. Set low to tristate the corresponding output. xxx1: enables hpout0 xx1x: enables hpout1 x1xx: enables hpout2 1xxx: enables hpout3
7:4	reserved	Leave as default.

Register_Address: **0xB2** Register Name: **config_output_mode_7_4** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
2:0	config_output_mode_5_4	These bits are used to enable outputs, and to select the mode of operation for configurable outputs 4 and 5 000: disable outputs 001: enable outclk4 in CMOS mode 010: enable outclk5 in CMOS mode 011: enable outclk4 and outclk5 in CMOS mode 100: enable outclk4 and outclk5 in complementary CMOS mode (outclk5 is inverted outclk4) 101: enable HCSL differential outputs 110: enable LVDS differential outputs 111: enable PECL differential outputs
3	reserved	Leave as default.
6:4	config_output_mode_7_6	Same description as above but for config_output_mode_7_6
7	reserved	Leave as default.

Register_Address: **0xB3** Register Name: **config_output_mode_3_0** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
2:0	config_output_mode_1_0	These bits are used to enable outputs, and to select the mode of operation for configurable outputs 0 and 1 000: disable outputs 001: enable outclk0 in CMOS mode 010: enable outclk1 in CMOS mode 011: enable outclk0 and outclk1 in CMOS mode 100: enable outclk0 and outclk1 in complementary CMOS mode (outclk1 is inverted outclk0) 101: enable HCSL differential outputs 110: enable LVDS differential outputs 111: enable PECL differential outputs
3	reserved	Leave as default.
6:4	config_output_mode_3_2	Same description as above but for config_output_mode_3_2

Register_Address: **0xB3** Register Name: **config_output_mode_3_0** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7	reserved	Leave as default.

Register_Address: **0xB4** Register Name: **config_output_mux_7_4** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
1:0	config_mux_output_4	These bits determine which clock will be selected to appear on outclk4 output in both, single ended and differential mode. 00: S3_A (Synthesis Engine 3, Divider A) 01: S1_C 10 and 11: reserved **Note:** Synthesizer 3 has to be enabled in register at address 0x71 whenever clock from high performance synthesizer 1 (S1) is selected to appear on the outclk in differential mode (LVPECL, LVDS, HCSL). This is not required when outclk is set to LVCMOS mode.
3:2	config_mux_output_5	These bits determine which clock will be selected to appear on outclk5 output when in single ended mode is selected by the 'Configurable output enable and control' register. When differential mode is selected for outclk4 and outclk5, these bits are ignored and outclk5 will have inverted version of outclk4 output clock. 00: S3_C (Synthesis Engine 3, Divider C) 01: S1_D 10 and 11: reserved **Note:** Synthesizer 3 has to be enabled in register at address 0x71 whenever clock from high performance synthesizer 1 (S1) is selected to appear on the outclk in differential mode (LVPECL, LVDS, HCSL). This is not required when outclk is set to LVCMOS mode.

Register_Address: **0xB4** Register Name: **config_output_mux_7_4** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
5:4	config_mux_output_6	These bits determine which clock will be selected to appear on outclk6 output in both, single ended and differential mode. 00: S3_A (Synthesis Engine 3, Divider A) 01: S1_C 10 and 11: reserved **Note:** Synthesizer 3 has to be enabled in register at address 0x71 whenever clock from high performance synthesizer 1 (S1) is selected to appear on the outclk in differential mode (LVPECL, LVDS, HCSL). This is not required when outclk is set to LVCMOS mode.
7:6	config_mux_output_7	these bits determine which clock will be selected to appear on outclk7 output when in single ended mode is selected by the 'Configurable output enable and control' register. When differential mode is selected for outclk6 and outclk7, these bits are ignored and outclk7 will have inverted version of outclk6 output clock. 00: S3_D (Synthesis Engine 3, Divider D) 01: S1_D 10 and 11: reserved **Note:** Synthesizer 3 has to be enabled in register at address 0x71 whenever clock from high performance synthesizer 1 (S1) is selected to appear on the outclk in differential mode (LVPECL, LVDS, HCSL). This is not required when outclk is set to LVCMOS mode.

Register_Address: **0xB5** Register Name: **config_output_mux_3_0** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
1:0	config_mux_output_0	These bits determine which clock will be selected to appear on outclk0 output in both, single ended and differential mode. 00: S2_A (Synthesis Engine 2, Divider A) 01: S0_C 10 and 11: reserved **Note:** Synthesizer 2 has to be enabled in register at address 0x71 whenever clock from high performance synthesizer 0 (S0) is selected to appear on the outclk in differential mode (LVPECL, LVDS, HCSL). This is not required when outclk is set to LVCMOS mode.
3:2	config_mux_output_1	These bits determine which clock will be selected to appear on outclk1 output when in single ended mode is selected by the 'Configurable output enable and control' register. When differential mode is selected for outclk0 and outclk1, these bits are ignored and outclk1 will have inverted version of outclk0 output clock. 00: S2_B (Synthesis Engine 2, Divider B) 01: S0_C 10 and 11: reserved **Note:** Synthesizer 2 has to be enabled in register at address 0x71 whenever clock from high performance synthesizer 0 (S0) is selected to appear on the outclk in differential mode (LVPECL, LVDS, HCSL). This is not required when outclk is set to LVCMOS mode.
5:4	config_mux_output_2	These bits determine which clock will be selected to appear on outclk2 output in both, single ended and differential mode. 00: S2_C (Synthesis Engine 2, Divider C) 01: S0_D 10 and 11: reserved **Note:** Synthesizer 2 has to be enabled in register at address 0x71 whenever clock from high performance synthesizer 0 (S0) is selected to appear on the outclk in differential mode (LVPECL, LVDS, HCSL). This is not required when outclk is set to LVCMOS mode.

Register_Address: **0xB5** Register Name: **config_output_mux_3_0** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:6	config_mux_output_3	These bits determine which clock will be selected to appear on outclk3 output when in single ended mode is selected by the 'Configurable output enable and control' register. When differential mode is selected for outclk2 and outclk3, these bits are ignored and outclk3 will have inverted version of outclk2 output clock. 00: S2_D (Synthesis Engine 2, Divider D) 01: S0_D 10 and 11: reserved **Note:** Synthesizer 2 has to be enabled in register at address 0x71 whenever clock from high performance synthesizer 0 (S0) is selected to appear on the outclk in differential mode (LVPECL, LVDS, HCSL). This is not required when outclk is set to LVCMOS mode.

Register_Address: **0xB6** Register Name: **synth3_stop_clock** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
1:0	synth3_post_div_A_stop	Appropriate setting of these bits will cause Synthesizer3 Post Divider A to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop outclk4 at falling edge (output stays low) 11: stop outclk4 at rising edge (output stays high). **Note:** This setting assumes that user has selected Synthesizer3 Post Divider A as the source for outclk4.

Register_Address: **0xB6** Register Name: **synth3_stop_clock** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
3:2	synth3_post_div_B_stop	Appropriate setting of these bits will cause Synthesizer3 Post Divider B to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop outclk5 at falling edge (output stays low) 11: stop outclk5 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer3 Post Divider B as the source for outclk5.
5:4	synth3_post_div_C_stop	Appropriate setting of these bits will cause Synthesizer3 Post Divider C to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop outclk6 at falling edge (output stays low) 11: stop outclk6 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer3 Post Divider C as the source for outclk6.
7:6	synth3_post_div_D_stop	Appropriate setting of these bits will cause Synthesizer3 Post Divider D to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop outclk7 at falling edge (output stays low) 11: stop outclk7 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer3 Post Divider D as the source for outclk7.

Register_Address: **0xB7** Register Name: **synth2_stop_clock** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
1:0	synth2_post_div_A_stop	Appropriate setting of these bits will cause Synthesizer2 Post Divider A to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop outclk0 at falling edge (output stays low) 11: stop outclk0 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer2 Post Divider A as the source for outclk0.
3:2	synth2_post_div_B_stop	Appropriate setting of these bits will cause Synthesizer2 Post Divider B to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop outclk1 at falling edge (output stays low) 11: stop outclk1 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer2 Post Divider B as the source for outclk1.
5:4	synth2_post_div_C_stop	Appropriate setting of these bits will cause Synthesizer2 Post Divider C to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop outclk2 at falling edge (output stays low) 11: stop outclk2 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer2 Post Divider C as the source for outclk2.
7:6	synth2_post_div_D_stop	Appropriate setting of these bits will cause Synthesizer2 Post Divider D to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop outclk3 at falling edge (output stays low) 11: stop outclk3 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer2 Post Divider D as the source for outclk3.

Register_Address: **0xB8** Register Name: **synth1_0_stop_clock** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
1:0	synth0_post_div_C_stop	Appropriate setting of these bits will cause Synthesizer0 Post Divider C to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop hpoutclk0 at falling edge (output stays low) 11: stop hpoutclk0 at rising edge (output stays high) **Note:** Polarity will be reversed is this clock is selected by register 0xB5 to appear on configurable outputs.
3:2	synth0_post_div_D_stop	Appropriate setting of these bits will cause Synthesizer0 Post Divider D to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop hpoutclk1 at falling edge (output stays low) 11: stop hpoutclk1 at rising edge (output stays high) **Note:** Polarity will be reversed is this clock is selected by register 0xB5 to appear on configurable outputs.
5:4	synth1_post_div_C_stop	Appropriate setting of these bits will cause Synthesizer1 Post Divider C to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop hpoutclk2 at falling edge (output stays low) 11: stop hpoutclk2 at rising edge (output stays high) **Note:** Polarity will be reversed is this clock is selected by register 0xB4 to appear on configurable outputs.
7:6	synth1_post_div_D_stop	Appropriate setting of these bits will cause Synthesizer1 Post Divider D to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop hpoutclk3 at falling edge (output stays low) 11: stop hpoutclk3 at rising edge (output stays high) **Note:** Polarity will be reversed is this clock is selected by register 0xB4 to appear on configurable outputs.

Register_Address: **0xB9** Register Name:**sync_fail_flag_status** Default Value: **0x00** Type:**StickyR**		
Bit Field	**Function Name**	**Description**
0	Synth0_syncFail_flag	When high, this bit indicates that Synthesizer 0 has lost lock. If this status bit appears set after clearing Synth0_ClearSyncFail_flag (register at address 0xBA), it is indication that Synthesizer 0 has lost lock, therefore generating wrong output frequency. **Note:** This bit will be set upon power up or device reset.
1	Synth1_syncFail_flag	Same description as above but for Synth1
2	Synth2_syncFail_flag	Same description as above but for Synth2
3	Synth3_syncFail_flag	Same description as above but for Synth3
7:4	reserved	Leave as default.

Register_Address: **0xBA** Register Name:**clear_sync_fail_flag** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
0	Synth0_clearSyncFail_flag	When high, this bit clears sticky Synth0_syncFail_flag. **Note:** after clearing Synth0_syncFail_flag, this bit must be set low for normal device operation
1	Synth1_clearSyncFail_flag	Same description as above but for Synth1
2	Synth2_clearSyncFail_flag	Same description as above but for Synth2
3	Synth3_clearSyncFail_flag	Same description as above but for Synth3
7:4	reserved	Leave as default.

Register_Address: **0xBF:0xC0** Register Name:**phase_shift_s0_postdiv_c** Default Value: **0x0000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
12:0	phase_shift_s0_postdiv_c	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer0 frequency for all clocks coming from Synthesizer0 Post Divider C (0:no shift, -1: delay output clock for 1 period, 1: advance output clock for 1 period, and so on)
15:13	quad_shift_s0_postdiv_c	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer0 Post Divider C. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xC1:0xC2** Register Name:**phase_shift_s0_postdiv_d** Default Value: **0x0000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
12:0	phase_shift_s0_postdiv_d	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer0 frequency for all clocks coming from Synthesizer0 Post Divider D (0: no shift, -1: delay output clock for 1 period, 1: advance output clock for 1 period, and so on)

Register_Address: **0xC1:0xC2** Register Name:**phase_shift_s0_postdiv_d** Default Value: **0x0000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:13	quad_shift_s0_postdiv_d	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer0 Post Divider D. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xC3** Register Name:**xo_or_crystal_sel** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
0	xo_or_crystal_sel	0: enables OSCo driver 1: disables OSCo driver Set to 1 when xo is used as master clock. Set to 0 when crystal is used as master clock.
7:1	Reserved	Leave as default

Register_Address: **0xC6** Register Name:**chip_revison** Default Value: **0x03** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:0	chip_revision	Chip_revision = 0b00000011 (full chip revision = chip_revision bits in register 0xC6 and chip_revision bits[6:5] in register 0x00)

Register_Address: **0xC7:0xC8** Register Name:**phase_shift_s1_postdiv_c** Default Value: **0x0000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
12:0	phase_shift_s1_postdiv_c	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer1 frequency for all clocks coming from Synthesizer1 Post Divider C (0: no shift, -1: delay output clock for 1 period, 1: advance output clock for 1 period, and so on)
15:13	quad_shift_s1_postdiv_c	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer1 Post Divider C. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xC9:0xCA**
Register Name:**phase_shift_s1_postdiv_d**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	phase_shift_s1_postdiv_d	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer1 frequency for all clocks coming from Synthesizer1 Post Divider D (0: no shift, -1: delay output clock for 1 period, 1: advance output clock for 1 period, and so on)
15:13	quad_shift_s1_postdiv_d	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer1 Post Divider D. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xCB:0xCC**
Register Name:**phase_shift_s2_postdiv_a**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	phase_shift_s2_postdiv_a	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer2 frequency for all clocks coming from Synthesizer2 Post Divider A (0: no shift, -1: delay output clock for 1 period, 1: advance output clock for 1 period, and so on)
15:13	quad_shift_s2_postdiv_a	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer2 Post Divider A. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xCD:0xCE** Register Name:**phase_shift_s2_postdiv_b** Default Value: **0x0000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
12:0	phase_shift_s2_postdiv_b	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer2 frequency for all clocks coming from Synthesizer2 Post Divider B (0: no shift, -1: delay output clock for 1 period, 1: advance output clock for 1 period, and so on)
15:13	quad_shift_s2_postdiv_b	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer2 Post Divider B. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xCF:0xD0** Register Name:**phase_shift_s2_postdiv_c** Default Value: **0x0000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
12:0	phase_shift_s2_postdiv_c	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer2 frequency for all clocks coming from Synthesizer2 Post Divider C (0: no shift, -1: delay output clock for 1 period, 1: advance output clock for 1 period, and so on)

Register_Address: **0xCF:0xD0** Register Name:**phase_shift_s2_postdiv_c** Default Value: **0x0000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:13	quad_shift_s2_postdiv_c	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer2 Post Divider C. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xD1:0xD2** Register Name:**phase_shift_s2_postdiv_d** Default Value: **0x0000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
12:0	phase_shift_s2_postdiv_d	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer2 frequency for all clocks coming from Synthesizer2 Post Divider D (0: no shift, -1: delay output clock for 1 period, 1: advance output clock for 1 period, and so on)
15:13	quad_shift_s2_postdiv_d	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer2 Post Divider D. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xD3:0xD4** Register Name:**phase_shift_s3_postdiv_a** Default Value: **0x0000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
12:0	phase_shift_s3_postdiv_a	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer3 frequency for all clocks coming from Synthesizer3 Post Divider A (0: no shift, -1: delay output clock for 1 period, 1: advance output clock for 1 period, and so on)
15:13	quad_shift_s3_postdiv_a	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer3 Post Divider A. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xD5:0xD6** Register Name:**phase_shift_s3_postdiv_b** Default Value: **0x0000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
12:0	phase_shift_s3_postdiv_b	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer3 frequency for all clocks coming from Synthesizer3 Post Divider B (0: no shift, -1: delay output clock for 1 period, 1: advance output clock for 1 period, and so on)
15:13	quad_shift_s3_postdiv_b	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer3 Post Divider B. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xD7:0xD8** Register Name:**phase_shift_s3_postdiv_c** Default Value: **0x0000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
12:0	phase_shift_s3_postdiv_c	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer3 frequency for all clocks coming from Synthesizer3 Post Divider C (0: no shift, -1: delay output clock for 1 period, 1: advance output clock for 1 period, and so on)
15:13	quad_shift_s3_postdiv_c	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer3 Post Divider C. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xD9:0xDA** Register Name:**phase_shift_s3_postdiv_d** Default Value: **0x0000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
12:0	phase_shift_s3_postdiv_d	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer3 frequency for all clocks coming from Synthesizer3 Post Divider D (0: no shift, -1: delay output clock for 1 period, 1: advance output clock for 1 period, and so on)
15:13	quad_shift_s3_postdiv_d	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer3 Post Divider D. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xDB** Register Name:**config_output_voltage** Default Value: **0x0F** Type:**R/W**		
Bit Field	**Function Name**	**Description**
1:0	bank1_output_voltage	Based on provided voltage level to the configurable outputs bank 1 (outputs outclk3, outclk2, outclk1 and outclk0), customer must configure these bits to represent that voltage. 00: 1.5 V 01: 1.8 V 10: 2.5 V 11: 3.3 V These values are used for appropriate configurable outputs slew rate calculation
3:2	bank2_output_voltage	Based on provided voltage level to the configurable outputs bank 2 (outputs outclk7, outclk6, outclk5 and outclk4), customer must configure these bits to represent that voltage. 00: 1.5 V 01: 1.8 V 10: 2.5 V 11: 3.3 V These values are used for appropriate configurable outputs slew rate calculation
7:4	reserved	reserved

Register_Address: **0xDC** Register Name:**config_output_slew_rate** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
0	slew_rate_outclk_1_0	Slew rate for outclk1 and outclk0. 0: medium 1: fast
1	slew_rate_outclk_3_2	Same description as above but for slew_rate_outclk_3_2
2	slew_rate_outclk_5_4	Same description as above but for slew_rate_outclk_5_4
3	slew_rate_outclk_7_6	Same description as above but for slew_rate_outclk_7_6
7:4	reserved	Leave as default.

Register_Address: **0xE0** Register Name:**gpio_function_pin0** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin0_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO0 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO pin unused.
7	gpio_pin0_con_or_stat_sel	Selects whether GPIO0 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE1** Register Name:**gpio_function_pin1** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin1_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO1 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO pin unused.
7	gpio_pin1_con_or_stat_sel	Selects whether GPIO1 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE2** Register Name:**gpio_function_pin2** Default Value: **0x60** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin2_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO2 control or status select' bit. The control and status table consist of 128 bits each. Default: hpdiff0 enable.
7	gpio_pin2_con_or_stat_sel	Selects whether GPIO2 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE3** Register Name:**gpio_function_pin3** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin3_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO3 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO pin unused.
7	gpio_pin3_con_or_stat_sel	Selects whether GPIO3 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE4** Register Name:**gpio_function_pin4** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin4_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO4 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO pin unused.
7	gpio_pin4_con_or_stat_sel	Selects whether GPIO4 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE5** Register Name:**gpio_function_pin5** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin5_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO5 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO pin unused..
7	gpio_pin5_con_or_stat_sel	Selects whether GPIO5 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE6** Register Name:**gpio_function_pin6** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin6_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO6 control or status select' bit. The control and status table consist of 128 bits each. Default:GPIO pin unused.

Register_Address: **0xE6** Register Name:**gpio_function_pin6** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7	gpio_pin6_con_or_stat_sel	Selects whether GPIO6 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE7** Register Name:**gpio_function_pin7** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin7_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO7 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO pin unused.
7	gpio_pin7_con_or_stat_sel	Selects whether GPIO7 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE8** Register Name:**gpio_function_pin8** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin8_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO8 control or status select' bit. The control and status table consist of 128 bits each. Deafault:GPIO pin unused.
7	gpio_pin8_con_or_stat_sel	Selects whether GPIO8 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE9** Register Name:**gpio_function_pin9** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin9_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO9 control or status select' bit. The control and status table consist of 128 bits each. Deafault:GPIO pin unused.
7	gpio_pin9_con_or_stat_sel	Selects whether GPIO9 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xEA** Register Name:**gpio_function_pin10** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin10_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO10 control or status select' bit. The control and status table consist of 128 bits each. Deafault:GPIO pin unused.
7	gpio_pin10_con_or_stat_sel	Selects whether GPIO10 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xEB** Register Name:**gpio_function_pin11** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin11_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO11 control or status select' bit. The control and status table consist of 128 bits each. Deafault:GPIO pin unused.

Register_Address: **0xEB** Register Name:**gpio_function_pin11** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7	gpio_pin11_con_or_stat_sel	Selects whether GPIO11 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xEC** Register Name:**NCO_a_adjust_en** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
0	NCO_a_adjust_en	Enables fine frequency adjustment of NCO a: 0 = disable 1 = enable **Note:** If bits 2:1 selects one of DPLLs (0 or 1) and if this bit is set high DPLL will operate in NCO mode.
2:1	NCO_a_select	Selects which NCO ("a") will be active: 00: DPLL0/NCO0 01: DPLL1/NCO1 10: NCO2 11: NCO3 **Note:** Two active NCOs (a and b) programmed in registers at addressed 0xEC and 0xF1 should never be set to point to the same DPLL/NCO.
7:3	reserved	leave as default

Register_Address: **0xED:0xF0** Register Name: **NCO_a_freq_adjustment** Default Value: **0x00000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
31:0	NCO_a_freq_adjustment	2's complement binary value of these bits represent NCO a (selected in register 0xEC) frequency offset. This register allows user to change frequecy of the NCO a in real time at the 300us rate with resolution of 0.24ppb. Expressed in steps of +/- 2^-32 of nominal setting. When NCO behaviour is desired, the output frequency should be calculated as per formula: fout = (1 + X/2^32)*finit where X -represent 2's complement number specified in this register finit - initial frequency set by Bs, Ks, Ms, Ns and postdivider number for synthesizer fed by NCO a fout - output frequency **Note 1:** NCO offset should not exceed +/-0.5% off nominal. **Note 2:** This register is ignored when the value in register 0xEC is equal to 0x00

Register_Address: **0xF1** Register Name:**NCO_b_adjust_en** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
0	NCO_b_adjust_en	Enables fine frequency adjustment of NCO b: 0 = disable 1 = enable **Note:** If bits 2:1 selects one of DPLLs (0 or 1) and if this bit is set high DPLL will operate in NCO mode.

Register_Address: **0xF1** Register Name:**NCO_b_adjust_en** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
2:1	NCO_b_select	Selects which NCO("b") will be active: 00: DPLL0 / NCO0 01: DPLL1 / NCO1 10: NCO2 11: NCO3 **Note:** Two active NCOs (a and b) programmed in registers at addressed 0xEC and 0xF1 should never be set to point to the same DPLL/NCO.
7:3	reserved	leave as default

Register_Address: **0xF2:0xF5** Register Name: **NCO_b_freq_adjustment** Default Value: **0x00000000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
31:0	NCO_b_freq_adjustment	2's complement binary value of these bits represent NCO b (selected in register 0xF1) frequency offset. This register allows user to change frequecy of the NCO b in real time with 300us rate and with resolution of 0.24 ppb. Expressed in steps of +/- 2^-32 of nominal setting. When NCO behaviour is desired, the output frequency should be calculated as per formula: fout = (1 + X/2^32)*finit where X -represent 2's complement number specified in this register finit - initial frequency set by Bs, Ks, Ms, Ns and postdivider number for synthesizer fed by NCO b fout - output frequency **Note 1:** NCO offset should not exceed +/-0.5% off nominal. **Note 2:** This register is ignored when the value in register 0xF1 is equal to 0x00

9.0 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage	V_{DD_R}	-0.5	4.6	V
2	Core supply voltage	V_{CORE_R}	-0.5	2.5	V
3	Voltage on any digital pin	V_{PIN}	-0.5	6	V
4	Voltage on osci and osco pin	V_{OSC}	-0.3	V_{DD} + 0.3	V
5	Storage temperature	T_{ST}	-55	125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated

Recommended Operating Conditions*

	Characteristics	Sym	Min.	Typ.	Max.	Units
1	Supply voltage	V_{DD-IO} AV_{DD}	3.135	3.30	3.465	V
2	Core supply voltage	V_{CORE}	1.71	1.80	1.89	V
3	Operating temperature	T_A	-40	25	85	°C
4	I/O Bank Supply Voltage	$B1V_{DD-IO}$, $B2V_{DD-IO}$	1.425 1.71 2.375 3.135	1.5 1.8 2.5 3.3	1.575 1.89 2.625 3.465	V

* Voltages are with respect to ground (GND) unless otherwise stated

DC Electrical Characteristics - Power - Core

	Characteristics	Sym	Typ.	Max.	Units	Notes
1	Core supply current (Vcore)	I_{CORE} (Vdd 3.3V)	46	48	mA	
		I_{CORE} (Vdd 1.8V)	102	109	mA	
2	Current for each HP Synthesis Engine	I_{SYN} (Vdd 3.3V)	57	73	mA	
		I_{SYN}(Vdd 1.8V)	0.2	1	mA	
3	Current for each General Purpose Synthesis Engine	I_{SYN} (Vdd 3.3V)	4	7	mA	
		I_{SYN}(Vdd 1.8V)	12	13	mA	

DC Electrical Characteristics - Power - High Performance Outputs

	Characteristics	Sym.	Typ.	Max.	Units	Notes
1	Power for each hpdiff clock driver	P_{hpdiff}(Vdd 3.3V)	85	91	mW	Including power to biasing and load resistors R_L = 50Ω
2	Power for each hpdiff clock driver minus power dissipated in the biasing and load resistors.	P_{hpdiff}(Vdd 3.3V)	36	42	mW	Without power to biasing and load resistors R_L = 50Ω
3	Power for each hpdiff clock driver (reduced power mode)	$P_{hpdifflp}$(Vdd 3.3V)	80	86	mW	Including power to biasing and load resistors R_L = 50Ω
4	Power for each hpdiff clock driver minus power dissipated in the load resistor. (reduced power mode)	$P_{hpdifflp}$(Vdd 3.3V)	31	37	mW	Without power to biasing and load resistors R_L = 50Ω
5	Power for each output divider of high performance synthesizers (enabled if one of two differential outputs assigned to it is enabled).	P_{div}(Vdd 3.3V)	17	40	mW	
6	Power for each hpoutclk clock driver	P_{hpout}(Vdd 3.3V)	17+ 7	40+36	mW	155.52 MHz output 10 pF load fixed power (due to output divider) + variable power (proportional to frequency and load)

DC Electrical Characteristics* - Power - Configurable Outputs

	Characteristics	Sym.	Typ.	Max.	Units	Notes
1	Power for each outclk clock driver in LVDS mode	$P_{Out-LVDS}$	32	35	mW	Including power to load resistor R_L = 100Ω
2	Power for each LVDS clock driver minus power dissipated in the load resistor	$P_{Out-LVDS}$	31	34	mW	Without power to load resistor R_L = 100Ω
3	Power for each outclk clock driver in LVPECL mode	$P_{Out-LVPECL}$	80	81	mW	Including power to biasing and load resistors R_L = 50Ω
4	Power for each LVPECL clock driver minus power dissipated in the biasing and load resistors	$P_{Out-LVPECL}$	38	39	mW	Without power to biasing and load resistors R_L = 50Ω
5	Power for each outclk clock driver in HCSL mode	$P_{Out-HCSL}$	62	64	mW	Including power to load resistors R_L = 33Ω + 50Ω
6	Power for each HCSL clock driver minus power dissipated in the load resistors	$P_{Out-HCSL}$	46	48	mW	Including power to load resistors R_L = 33Ω + 50Ω
7	Power for each outclk clock driver in 1.5V CMOS mode	$P_{Out-CMOS1.5}$	5.9	6.2	mW	C_L = 10pF @155.52MHz (proportional to frequency and load)
8	Power for each outclk clock driver in 1.8V CMOS mode	$P_{Out-CMOS1.8}$	9	10	mW	C_L = 10pF @155.52MHz (proportional to frequency and load)
9	Power for each outclk clock driver in 2.5V CMOS mode	$P_{Out-CMOS2.5}$	23	24	mW	C_L = 10pF @155.52MHz (proportional to frequency and load)
10	Power for each outclk clock driver in 3.3V CMOS mode	$P_{Out-CMOS3.3}$	42	44	mW	C_L = 10pF @155.52MHz (proportional to frequency and load)

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise state.

DC Electrical Characteristics - Inputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage	V_{CIH}	$0.7 \cdot V_{DD-IO}$			V	
2	CMOS low-level input voltage	V_{CIL}			$0.3 \cdot V_{DD-IO}$	V	
3	CMOS Input leakage current	I_{IL}	-10		10	µA	$V_I = V_{DD}$ or 0 V
4	Differential input common mode voltage	V_{CM}	1.1		2.0	V	
5	Differential input voltage difference	V_{ID}	0.25		1.0	V	

AC/DC Electrical Characteristics - OSCi Input

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage	V_{CIH}	2.0			V	
2	CMOS low-level input voltage	V_{CIL}			0.8	V	
3	Input leakage current	I_{IL}	-10		10	μA	$V_I = V_{DD}$ or 0 V
4	Duty Cycle		40		60	%	

DC Electrical Characteristics - High Performance Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	HPCMOS High-level output voltage	V_{OH}	$0.8 \cdot AV_{DD}$			V	I_{OH} = 2mA C_L = 5pF
2	HPCMOS Low-level output voltage	V_{OL}			$0.2 \cdot AV_{DD}$	V	I_{OL} = 2mA C_L = 5pF
3	LVPECL: High-level output voltage	V_{OH_LVPECL}	AV_{DD} - 1.12	AV_{DD} - 1.00	AV_{DD} - 0.88	V	$R_L = 50\Omega$ to AV_{DD} - 2V, C_L = 1pF
4	LVPECL: Low-level output voltage	V_{OL_LVPECL}	AV_{DD} - 1.81	AV_{DD} - 1.71	AV_{DD} - 1.55	V	$R_L = 50\Omega$ to AV_{DD} - 2V, C_L = 1pF
5	LVPECL: Differential output voltage*	V_{OD_LVPECL}	0.53	0.67	0.80	V	$R_L = 50\Omega$ to AV_{DD} - 2V, C_L = 1pF

* Output swing is guaranteed for frequency up to 720MHz, it may decrease by 50mv if the frequency is greater than 720MHz

DC Electrical Characteristics - Configurable Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	3.3 V CMOS High-level output voltage	V_{OH}	$0.8 \cdot B1V_{DD\text{-}IO}$ $0.8 \cdot B2V_{DD\text{-}IO}$			V	I_{OH} = 2mA C_L = 5pF
2	3.3 V CMOS Low-level output voltage	V_{OL}			$0.2 \cdot B1V_{DD\text{-}IO}$ $0.2 \cdot B2V_{DD\text{-}IO}$	V	I_{OL} = 2mA C_L = 5pF
3	2.5 V CMOS High-level output voltage	V_{OH}	$0.8 \cdot B1V_{DD\text{-}IO}$ $0.8 \cdot B2V_{DD\text{-}IO}$			V	I_{OH} = 2mA C_L = 5pF
4	2.5 V CMOS Low-level output voltage	V_{OL}			$0.2 \cdot B1V_{DD\text{-}IO}$ $0.2 \cdot B2V_{DD\text{-}IO}$	V	I_{OL} = 2mA C_L = 5pF

DC Electrical Characteristics - Configurable Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
5	1.8 V CMOS High-level output voltage	V_{OH}	$0.8 \cdot B1V_{DD\text{-}IO}$ $0.8 \cdot B2V_{DD\text{-}IO}$			V	I_{OH} = 2mA C_L = 5pF
6	1.8 V CMOS Low-level output voltage	V_{OL}			$0.2 \cdot B1V_{DD\text{-}IO}$ $0.2 \cdot B2V_{DD\text{-}IO}$	V	I_{OL} = 2mA C_L = 5pF
7	1.5 V CMOS High-level output voltage	V_{OH}	$0.8 \cdot B1V_{DD\text{-}IO}$ $0.8 \cdot B2V_{DD\text{-}IO}$			V	I_{OH} = 2mA C_L = 5pF
8	1.5 V CMOS Low-level output voltage	V_{OL}			$0.2 \cdot B1V_{DD\text{-}IO}$ $0.2 \cdot B2V_{DD\text{-}IO}$	V	I_{OL} = 2mA C_L = 5pF
9	LVPECL: High-level output voltage	V_{OH_LVPECL}	AV_{DD} - 1.12	AV_{DD} - 1.00	AV_{DD} - 0.88	V	R_L = 50Ω to AV_{DD} - 2V, C_L = 1pF
10	LVPECL: Low-level output voltage	V_{OL_LVPECL}	AV_{DD} - 1.81	AV_{DD} - 1.71	AV_{DD} - 1.55	V	R_L = 50Ω to AV_{DD} - 2V, C_L = 1pF
11	LVPECL: Differential output voltage	V_{OD_LVPECL}	0.48	0.64	0.80	V	R_L = 50Ω to AV_{DD} - 2V, C_L = 1pF
12	LVDS: High-level output voltage	V_{OH_LVDS}	1.18	1.30	1.47	V	R_L = 100Ω, C_L = 1pF
13	LVDS: Low-level output voltage	V_{OL_LVDS}	0.91	0.98	1.10	V	R_L = 100Ω, C_L = 1pF
14	LVDS: Differential output voltage	V_{OD_LVDS}	0.27	0.32	0.37	V	R_L = 100Ω, C_L = 1pF
15	LVDS: output offset voltage	V_{OFF_LVDS}		30		mV	R_L = 100Ω, C_L = 1pF
16	HCSL: High-level output voltage	V_{OH_HCSL}	0.6	0.7	0.9	V	R_L = 50Ω each to ground C_L = 5pF
17	HCSL: Low-level output voltage	V_{OL_HCSL}	0.00	0.01	0.03	V	R_L = 50Ω each to ground C_L = 5pF

AC Electrical Characteristics* -Output Timing Parameters Measurement Voltage Levels (see Figure 30)

	Characteristics	Sym.	CMOS	LVPECL	LVDS	Units
1	Threshold Voltage	$V_{T\text{-}CMOS}$ $V_{T\text{-}LVPECL}$ $V_{T\text{-}CML}$	$0.5V_{DD}$	V_{DD}-1.35	1.14	V
2	Rise and Fall Threshold Voltage High	V_{HM}	$0.8V_{DD}$	$0.8V_{OD\_LVPECL}$	$0.8V_{OD\_LVDS}$	V
3	Rise and Fall Threshold Voltage Low	V_{LM}	$0.2V_{DD}$	$0.2V_{OD\_LVPECL}$	$0.2V_{OD\_LVDS}$	V

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated

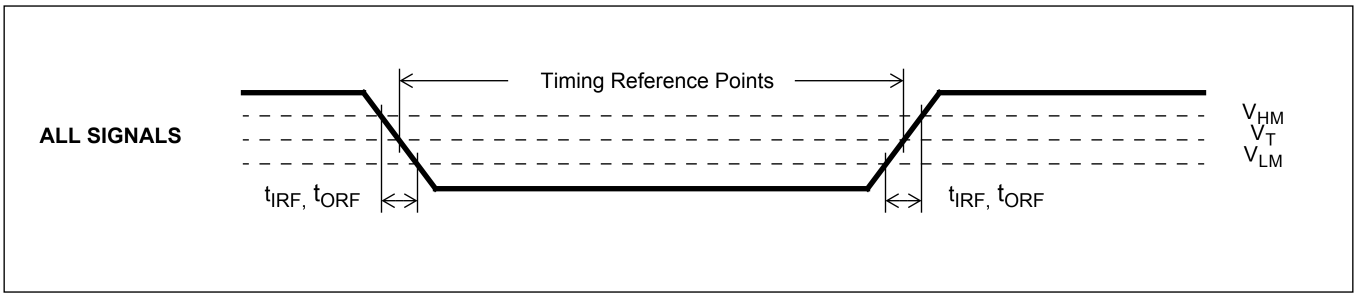


Figure 30 - Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics* - Inputs (see Figure 31).

	Characteristics	Symbol	Min.	Typ.	Max.	Units
1	Input reference Frequency (CMOS Inputs)	$1/t_{REFP}$			177.5	MHz
2	Input reference Frequency (LVPECL Inputs)	$1/t_{REFP}$			750	MHz
3	Input reference pulse width high or low	t_{REFW}	0.55			ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions

AC Electrical Characteristics* - Input To Output Timing (see Figure 31)

	Characteristics	Symbol	Min.	Typ.	Max.	Units
1	Input reference to hpoutclk0 output clock (with same frequency) delay	t_{HP_REFD}	-2	0	+2	ns
2	Input reference to outclk0 (with same frequency) delay	t_{REFD}		0		ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

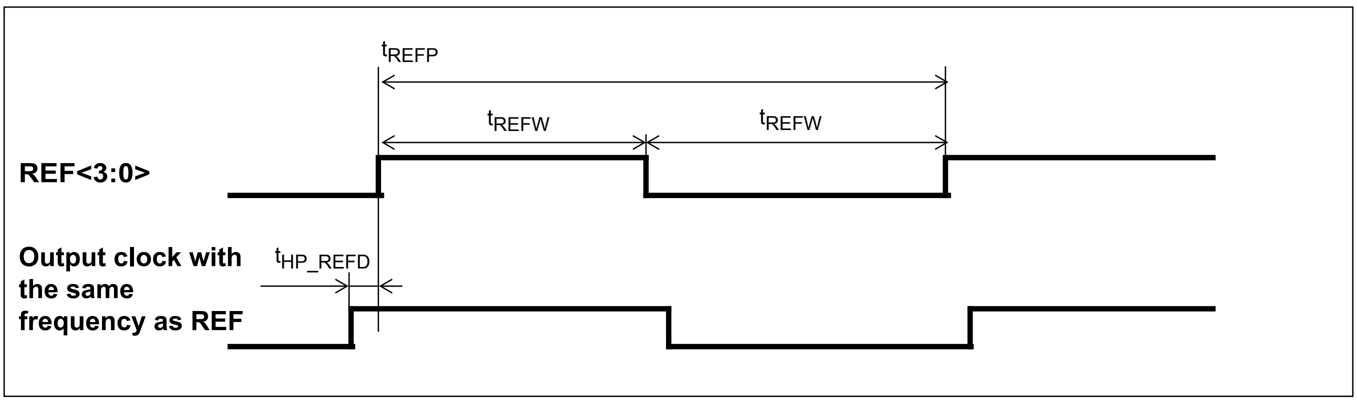


Figure 31 - Input To Output Timing for hpoutclk0

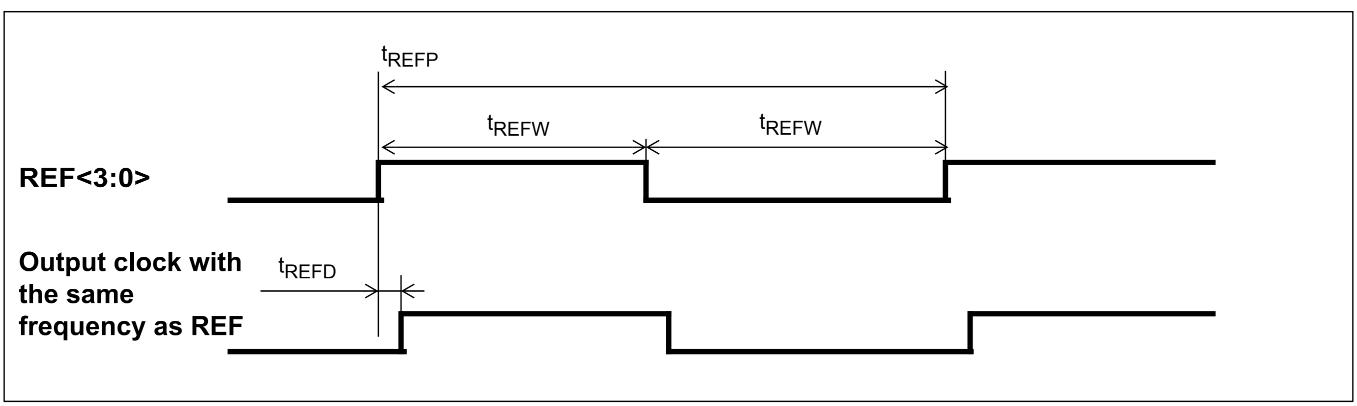


Figure 32 - Input To Output Timing To outclk0

AC Electrical Characteristics* - Outputs (see Figure 33).

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Clock skew between high performance outputs	$t_{OUT2OUTD}$	-1	0	+1	ns	
2	Clock skew between configurable outputs	$t_{OUT2OUTD}$		0		ns	
3	Output clock Duty Cycle	t_{PWH}, t_{PWL}	45%	50%	55%	Duty Cycle	
4	hpdiff (LVPECL) Output clock rise or fall time	t_r / t_f	265	370	515	ps	
5	hpoutclk (LVCMOS) clock rise and fall time	t_r / t_f	620	950	1490	ps	10pF load
6	Output Clock Frequency (hpdiff)	F_{hpdiff}			750	MHz	
7	Output Clock Frequency (hpoutclk)	F_{hpout}			177.5	MHz	
8	Output Clock Frequency (single-ended configurable outclk outputs)	F_{out}			160	MHz	
9	Output Clock Frequency (differential configurable outclk outputs)	F_{out_diff}			350	MHz	

* Supply voltage and operating temperature are as per Recommended Operating Conditions

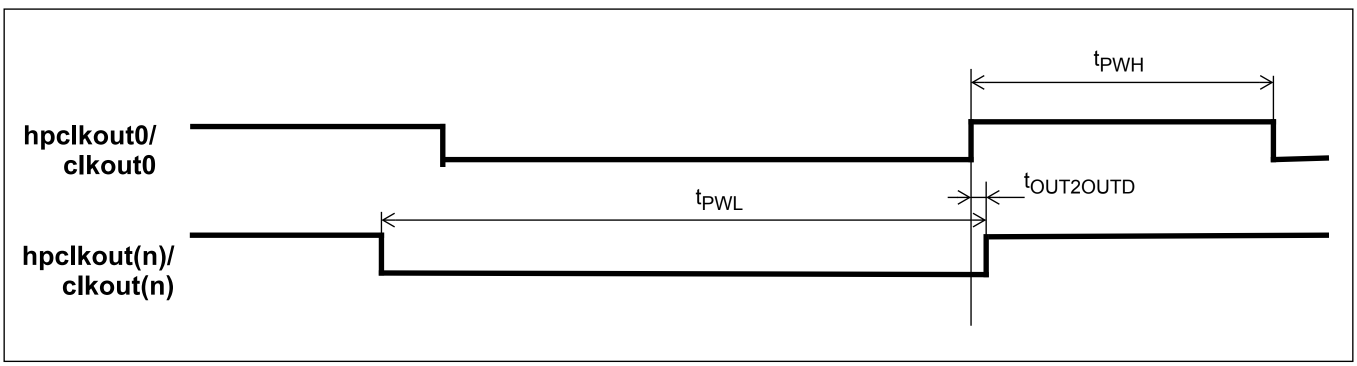


Figure 33 - Output Timing Referenced To hpclkout0/clkout0

Functional waveforms and timing characteristics for the LSB first mode are shown in Figure 34, and Figure 35 describe the MSB first mode. Table 8 shows the timing specifications.

Specification	Name	Min.	Max.	Units
sck period	tcyc	124		ns
sck pulse width low	tclkl	62		ns
sck pulse width high	tclkh	62		ns
si setup (write) from sck rising	trxs	10		ns
si hold (write) from sck rising	trxh	10		ns
so delay (read) from sck falling	txd		25	ns
cs_b setup from sck falling (LSB first)	tcssi	20		ns
cs_b setup from sck rising (MSB first)	tcssm	20		ns
cs_b hold from sck falling (MSB first)	tcshm	10		ns
cs_b hold from sck rising (LSB first)	tcshi	10		ns
cs_b to output high impedance	tohz		60	ns

Table 8 - Serial Peripheral Interface Timing

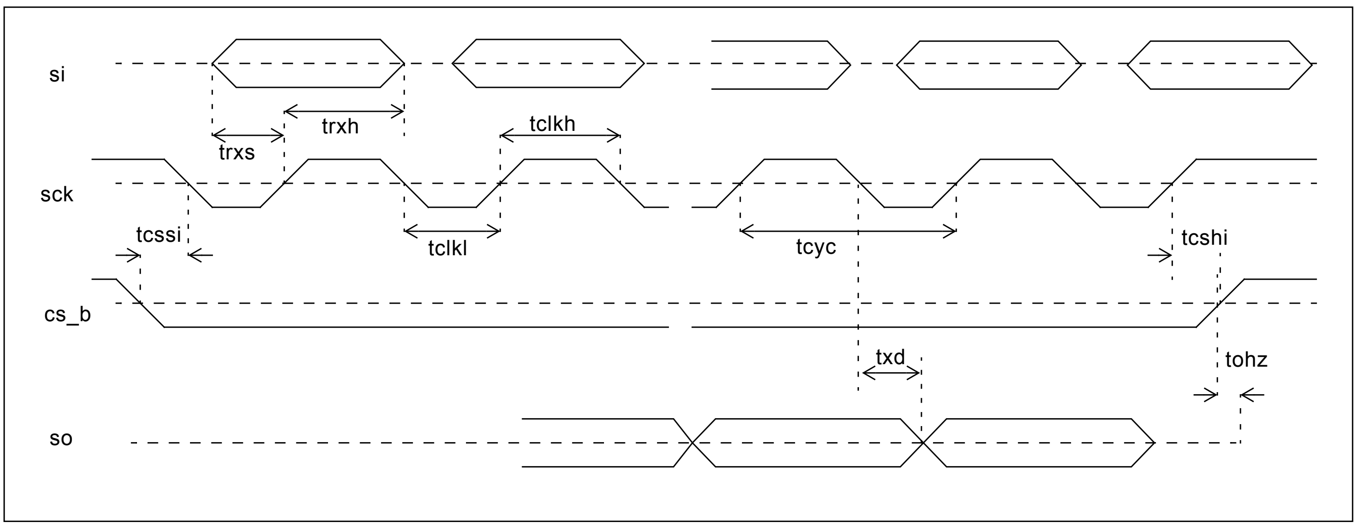


Figure 34 - Serial Peripheral Interface Timing - LSB First Mode

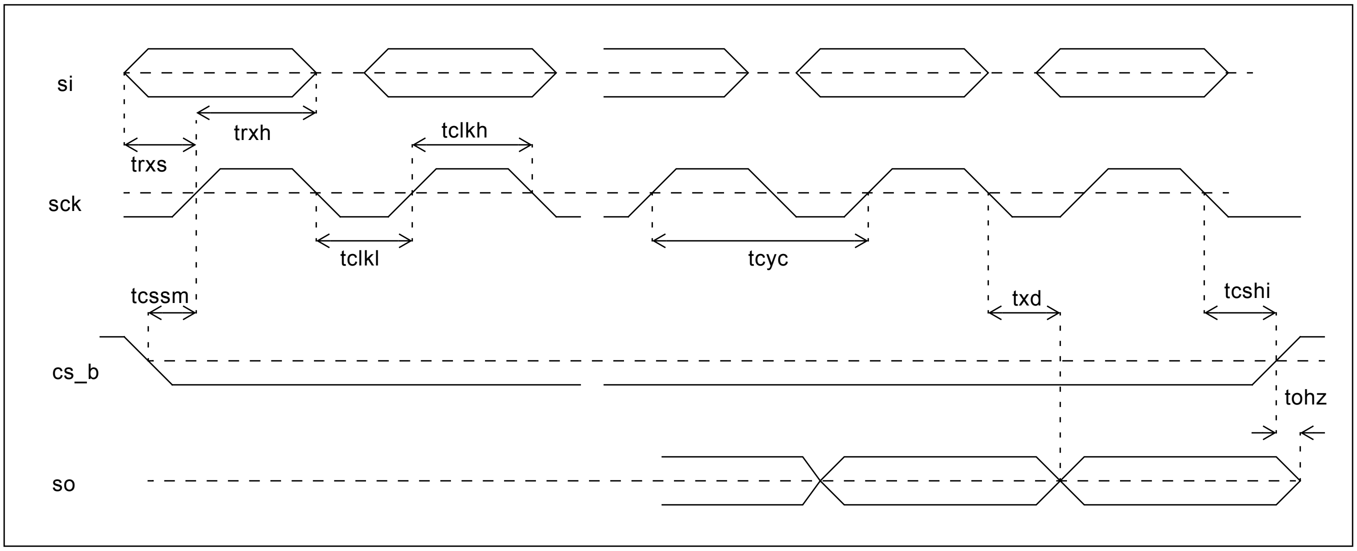


Figure 35 - Serial Peripheral Interface Timing - MSB First Mode

The timing specification for the I^2C interface is shown in Figure 36 and Table 9.

Specification	Name	Min.	Typ.	Max.	Units	Note
SCL clock frequency	f_{SCL}	0		400	kHz	
Hold time START condition	$t_{HD:STA}$	0.6			us	
Low period SCL	t_{LOW}	1.3			us	
Hi period SCL	t_{HIGH}	0.6			us	
Setup time START condition	$t_{SU:STA}$	0.6			us	
Data hold time	$t_{HD:DAT}$	0		0.9	us	
Data setup time	$t_{SU:DAT}$	100			ns	
Rise time	t_r				ns	Determined by choice of pull-up resistor
Fall time	t_f	$20 + 0.1C_b$		250	ns	
Setup time STOP condition	$t_{SU:STO}$	0.6			us	
Bus free time between STOP/START	t_{BUF}	1.3			us	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0		50	ns	
Max capacitance for each I/O pin				10	pF	

Table 9 - I^2C Serial Microport Timing

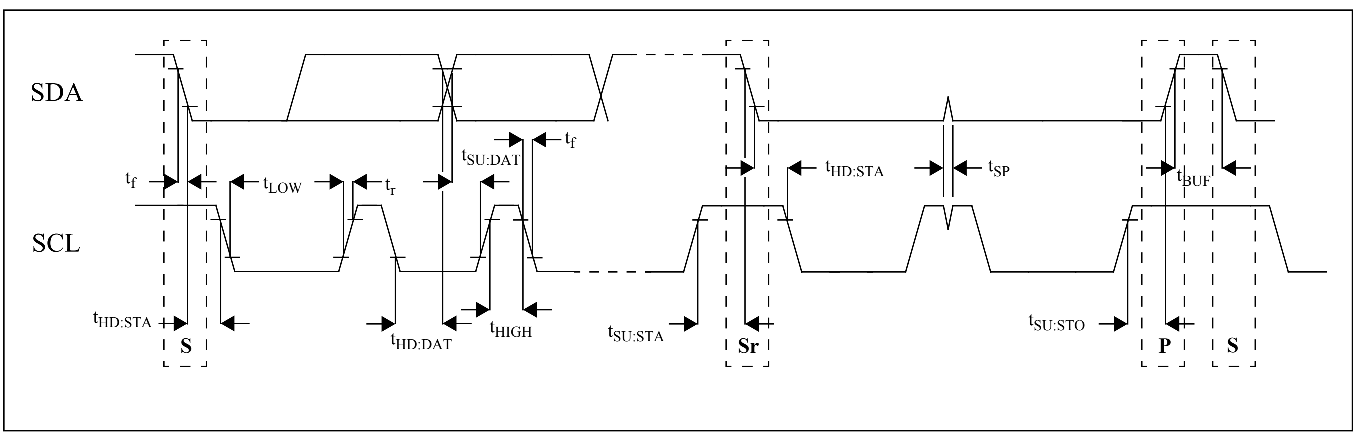


Figure 36 - I^2C Serial Microport Timing

10.0 Performance Characterization

10.1 Output Clocks Jitter Generation

Output Frequency	Jitter Measurement Filter	Max.	Units	Notes
622.08 MHz	50 kHz - 80 MHz	0.63	ps_{rms}	
	12 kHz - 20 MHz	0.73	ps_{rms}	

Table 10 - Jitter Generation Specifications - HPDIFF Outputs

Output Frequency	Jitter Measurement Filter	Max.	Units	Notes
25 MHz	12 kHz - 5 MHz	0.99	ps_{rms}	
77.76 MHz	12 kHz - 20 MHz	0.99	ps_{rms}	
125 MHz	12 kHz - 20 MHz	0.85	ps_{rms}	
156.25 MHz	12 kHz - 20 MHz	0.88	ps_{rms}	

Table 11 - Jitter Generation Specifications - HPOUT Outputs

Output Frequency	Jitter Measurement Filter	Max.	Units	Notes
25 MHz	12 kHz - 5 MHz	4.52	ps_{rms}	
77.76 MHz	12 kHz - 20 MHz	2.78	ps_{rms}	
125 MHz	12 kHz - 20 MHz	5.34	ps_{rms}	
156.25 MHz	12 kHz - 20 MHz	7.78	ps_{rms}	

Table 12 - Jitter Generation Specifications - Configurable Outputs driven from High Performance Synthesizers - Differential Mode

Output Frequency	Jitter Measurement Filter	Max.	Units	Notes
25 MHz	12 kHz - 5 MHz	15.11	ps_{rms}	
77.76 MHz	12 kHz - 20 MHz	15.15	ps_{rms}	
125 MHz	12 kHz - 20 MHz	16.42	ps_{rms}	
156.25 MHz	12 kHz - 20 MHz	16.15	ps_{rms}	

Table 13 - Jitter Generation Specifications - Configurable Outputs driven from General Purpose Synthesizers - Differential Mode

10.2 DPLL Performance Characteristics

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Pull-in/Hold-in Range	+/-52		+/-3900	ppm	user selectable
2	Lock Time *			1	sec	
3	Reference Switching MTIE			5	nsec	
4	Entry into Holdover MTIE			5	nsec	
5	Exit from Holdover MTIE			5	nsec	
6	Holdover Accuracy			50	ppb	
7	Phase gain in the passband			0.1	dB	

Table 14 - DPLL Characteristics

* Lock time of 1 sec is achieved when pulling a 9.2 ppm reference for any selected bandwidth and when phase slope limit is larger than 7.5 usec.

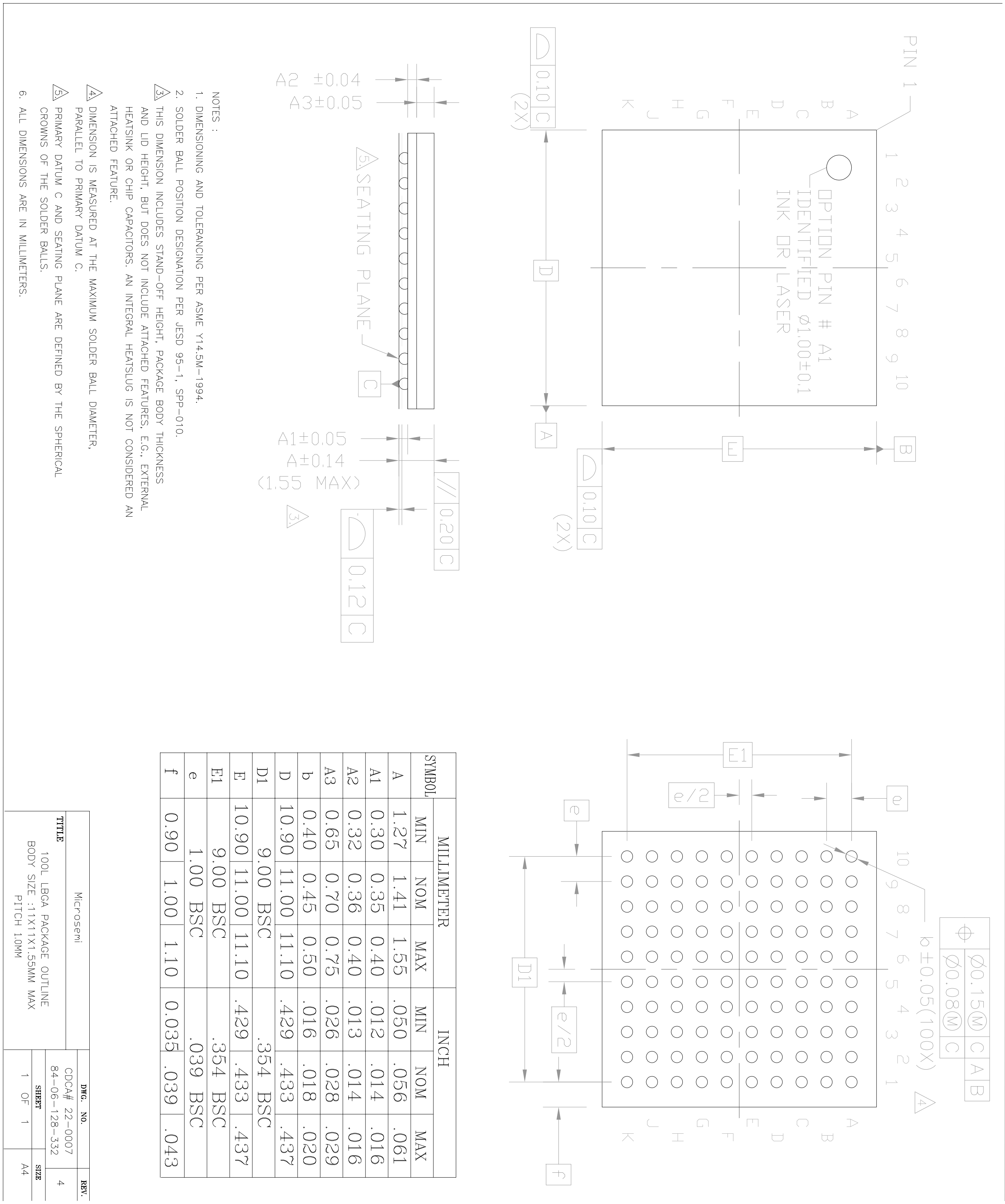
11.0 Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Junction to Ambient Thermal Resistance	θ_{ja}	Still Air 1 m/s 2 m/s	29.7 26.5 25.3	^{o}C/W
Junction to Case Thermal Resistance	θ_{jc}		7.7	^{o}C/W
Maximum Junction Temperature *	T_{jmax}		125	^{o}C
Maximum Ambient Temperature	T_A		85	^{o}C

Table 15 - Thermal Care

* Proper thermal management must be practiced to ensure that T_{jmax} is not exceeded.

12.0 Mechanical Drawing



SYMBOL	MILLIMETER MIN	MILLIMETER NOM	MILLIMETER MAX	INCH MIN	INCH NOM	INCH MAX
A	1.27	1.41	1.55	.050	.056	.061
A1	0.30	0.35	0.40	.012	.014	.016
A2	0.32	0.36	0.40	.013	.014	.016
A3	0.65	0.70	0.75	.026	.028	.029
b	0.40	0.45	0.50	.016	.018	.020
D	10.90	11.00	11.10	.429	.433	.437
D1		9.00 BSC			.354 BSC	
E	10.90	11.00	11.10	.429	.433	.437
E1		9.00 BSC			.354 BSC	
e		1.00 BSC			.039 BSC	
f	0.90	1.00	1.10	0.035	.039	.043

13.0 Package Markings

13.1 100-pin BGA. Package Top Mark Format

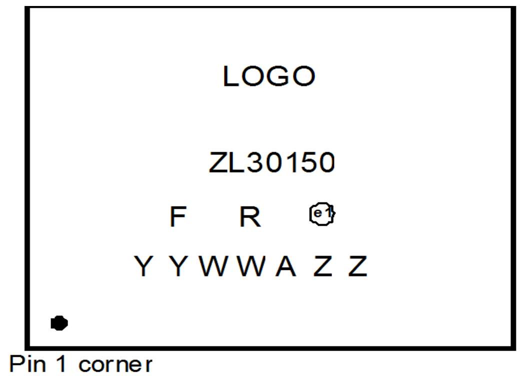


Figure 37 - Non-customized Device Top Mark

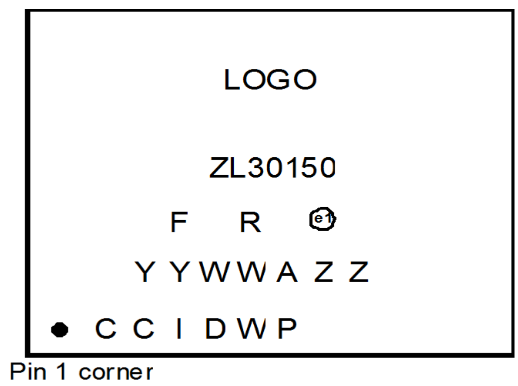


Figure 38 - Custom Factory Programmed Device Top Mark

Line	Characters	Description
1	ZL30150	Part Number
2	F	Fab Code
2	R	Product Revision Code
2	e1	Denotes Pb-Free Package
3	YY	Last Two Digits of the Year of Encapsulation
3	WW	Work Week of Assembly
3	A	Assembly Location Code
3	ZZ	Assembly Lot Sequence
4	CCID	Custom Programming Identification Code
4	WP	Work Week of Programming

Table 16 - Package Marking Legend

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